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(54) DEVICE FOR DRIVING A LIQUID CRYSTAL DISPLAY

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(57) **ABSTRACT**

A device for driving an LCD includes a timing control unit, a gate driving unit having a shift register and an output circuit, and a control signal transmission line for transmitting a data carry signal for enabling the shift register and a signal for controlling an data output by the output circuit using a single signal line. The data carry signal uses a rising edge trigger system, and the output control signal uses a level trigger system. In order to prevent an overlapping of the data carry signal and the output control signal, the output control signal is outputted after one clock from a time point where the data carry signal is latched using the shift register.

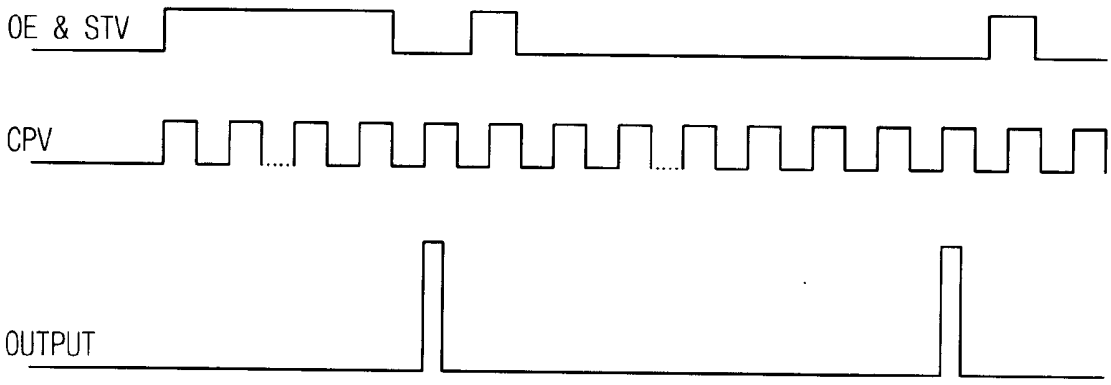


FIG. 1
(Related ART)

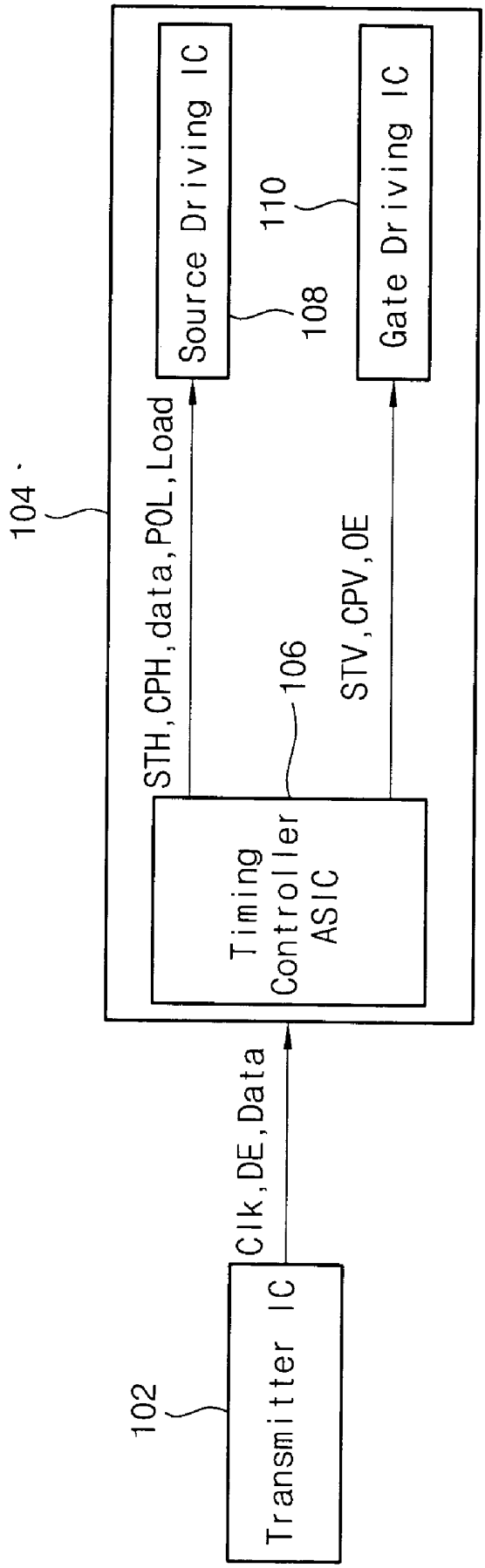


FIG.2

(Related ART)

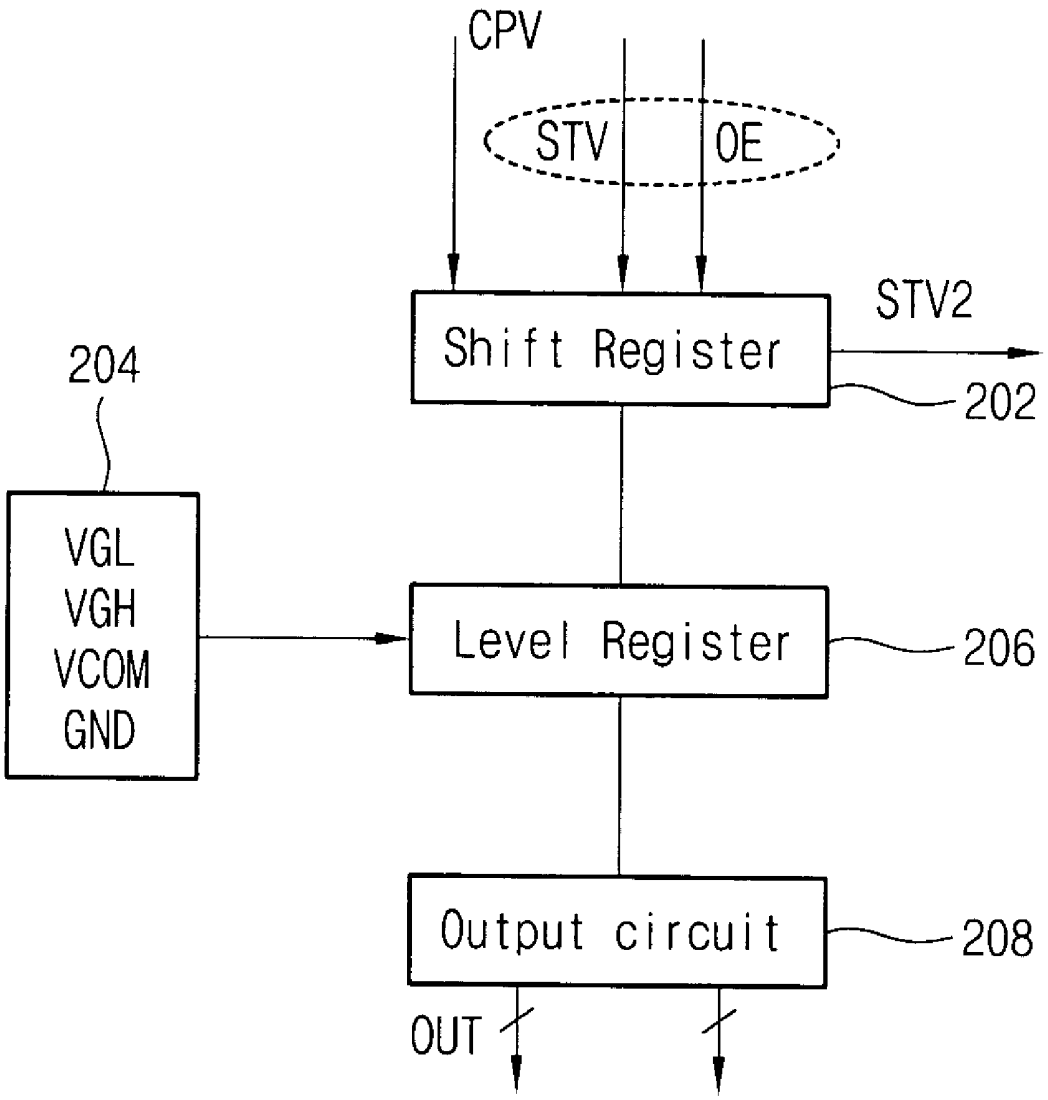


FIG.3
(Related ART)

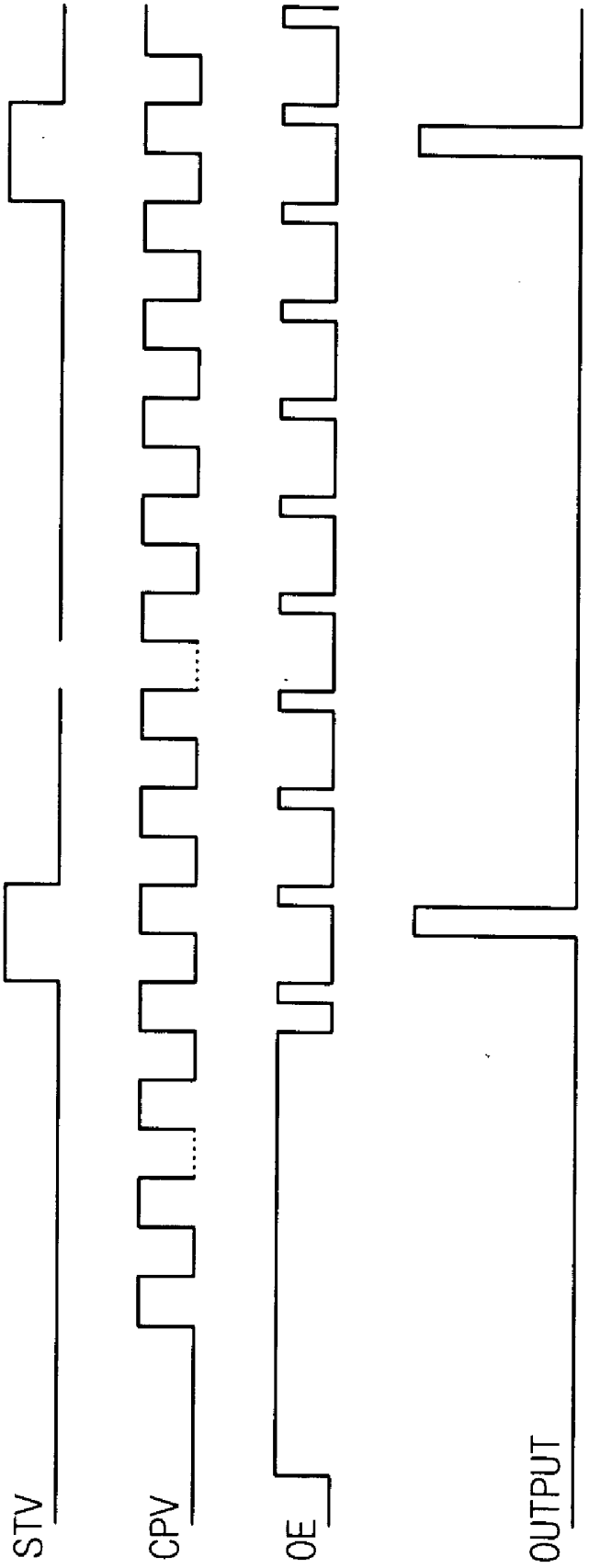
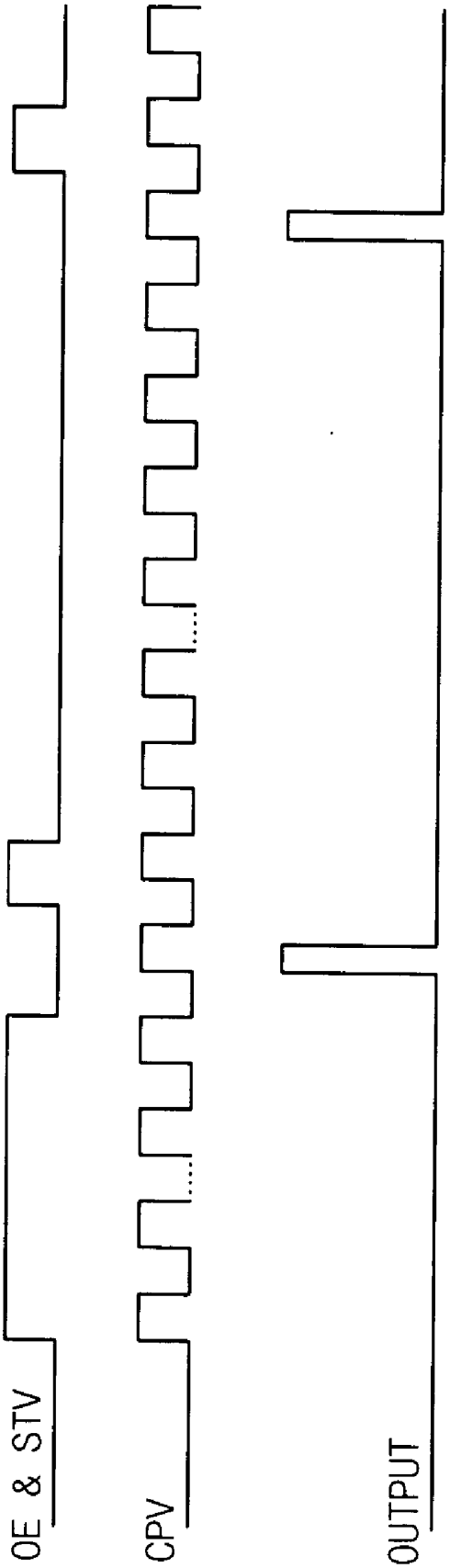


FIG.4



DEVICE FOR DRIVING A LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display, and more particularly to a device for driving a liquid crystal display having an improved control signal transmission system between a timing control IC and a driving IC.

[0003] 2. Description of the Prior Art

[0004] As generally known in the art, in order to drive a liquid crystal display (LCD), a drive IC, a timing control ASIC, and an analog circuit should be provided in the corresponding LCD panel. The timing control ASIC serves to receive an RGB signal through a host interface, distribute data to a source driving IC, and a control gate driving IC.

[0005] Main control signals generated by the timing control ASIC for the purpose of controlling the source driving IC are a carry signal STH for informing the source driving IC of the start of data, a signal POL for reporting the polarity of an output voltage, a signal LOAD for reporting a latch and output of data, etc. Also, main control signals generated by the timing control ASIC for the purpose of controlling the gate driving IC for driving TFTs are a carry signal STV for informing the gate driving IC of the start of data, a clock signal CPV for driving the IC, and an output control signal OE.

[0006] In the control IC of a TFT LCD module, video data and control signals of a pixel driving IC are transmitted in the form of a bus on a printed circuit board (PCB). In this case, it requires a technique having a very high degree of difficulty, designing 36 to 48 image data lines and 10 control signal lines. Especially, due to the development of gates without PCB, wiring to the gate driving IC requires a high degree of difficulty since it should be prepared as a pattern on glass.

[0007] The data of the existing LCD driving IC includes basic image data and data for processing various signals, and it is necessary to reduce the data. Especially, as the resolution and data bits increase, the reduction of signals is necessary for an optimum design of the PCB.

SUMMARY OF THE INVENTION

[0008] Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a device for driving an LCD which can reduce signal lines of a gate driving IC.

[0009] In order to accomplish this object, there is provided a device for driving an LCD comprising a timing control unit, a gate driving unit having a shift register and an output circuit, and a control signal transmission line for transmitting a data carry signal for enabling the shift register and a signal for controlling an data output by the output circuit using a single signal line.

[0010] The data carry signal uses a rising edge trigger system, and the output control signal uses a level trigger system.

[0011] In order to prevent an overlapping of the data carry signal and the output control signal, the output control signal is outputted after one clock from a time point where the data carry signal is latched using the shift register.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0013] **FIG. 1** is a view explaining the operation of the conventional LCD driving IC.

[0014] **FIG. 2** is a block diagram illustrating the internal construction of the conventional driving IC.

[0015] **FIG. 3** is a timing diagram of control signals of the conventional gate driving IC.

[0016] **FIG. 4** is a timing diagram of control signals of an LCD driving device according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Hereinafter, a preferred embodiment of the present invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description on the same or similar components will be omitted.

[0018] **FIG. 1** is a view explaining the operation of the conventional LCD driving IC. A source driving IC latches RGB data sequentially inputted to match a dot clock, and converts a dot-sequence type timing system into a line-sequence type timing system. The source driving IC transfers data stored in a first latch to a second latch to match a transition enable signal for a period of every horizontal line. The data stored in the second latch is converted into an analog voltage through an analog-to-digital converter, and then applied to data lines through a current buffer. For such a data conversion, the following signals are required as basic control signals. In **FIG. 1**, the reference numeral '**102**' denotes a transmitter IC, '**104**' an LCD module, '**106**' a timing controller, '**108**' a source driving IC, and '**110**' a gate driving IC. Also, 'DE' denotes a data enable signal, 'CLK' a horizontal clock signal, 'STH' a data latch enable signal, 'POL' an output polarity signal, 'LOAD' a data output signal, 'CPV' a vertical clock pulse signal, 'STV' a start vertical pulse signal, and 'OE' a gate output control signal for initializing the gate driving IC for one frame.

[0019] The internal construction of the driving IC is illustrated in **FIG. 2**. In **FIG. 2**, '**202**' denotes a shift register, '**204**' a power supply circuit, '**206**' a level shifter, and '**208**' an output circuit. Also, 'VGL', 'VGH', 'VCOM' and 'GND' are reference voltage signals having predetermined levels, respectively.

[0020] The OE signal currently used plays two roles. First is to intentionally intercept a gate output for one frame in order to stabilizing an initial state, and the second is to periodically intercept an output for a predetermined period in order to periodically change the shape of an output pulse. The present invention proposes an integrated use of an OE signal line for the first role with respect to the STV signal.

The OE signal for the second role cannot be used, but the driving thereof causes no problem since it is possible to match the timing by the change of the shape of an analog power supply voltage and by the delay of a load signal.

[0021] **FIG. 3** is a timing diagram for driving a general gate driving IC. The gate driving IC pursues an initial stabilization by using the OE signal. The gate driving IC sends its output simultaneously with the latch of the STV at a rising edge of the CPV, and controls the shape of the gate output pulse using the OE signal having a regular timing.

[0022] Generally, it is recommended to use the OE signal in the initial state, and by initializing the gate for at least one frame period using the OE signal, an excessive voltage drop of the LCD module can be prevented. If the gate is not initialized when the power is on, the initial value of an internal register of the gate driver is unknown. Thus, if the initial value is "1", all channels of the gates having the value of "1" are open at a time, and this causes an instantaneous overload. In the case of XGA, the load is changed according to how many internal registers in 768 lines have the value of "1", and this affects the VDD voltage, so that the gate driving IC may be reset due to the drop of the VDD voltage.

[0023] In addition, a way to solve this problem without using the OE signal is to design the chip so that the initial values of the internal registers become "0". It is also required to intentionally intercept the output through the OE signal line for the initial stabilization, and this initial interception period will be more than a one-frame period in which the 768 internal registers are all "0". However, since the wiring to the gate driving IC should be made in the form of a pattern on a glass according to the development of the gate having no PCB, the reduction of the gate driving control signals is continuously required due to a small installation space.

[0024] Since the timing of using the OE signal should be different from the timing of using the STV signal in a general driving state, a transmission system that uses a single signal line should be adopted. Also, since the high-level period of the STV signal corresponds to an area where the output is prohibited, the timing should be adjusted so as not to disturb the actual data output. Referring to a timing diagram of **FIG. 4**, an initial output prohibition area exists for the common use of the OE signal line, and in a general driving state, a pulse is provided for each frame as an enable signal. In order not to disturb the data output, the OE signal is outputted after one clock from the time point where the STV signal is latched using the shift register.

[0025] As described above, according to the present invention, the number of control signals required for driving the TFT LCD is reduced, and this causes the PCB design to be simplified and the signal interference phenomenon reduced. Also, the present invention provides simple wiring on the glass, simplifies the circuit block of the timing controller, and reduces the installation area.

[0026] Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. A device for driving an LCD comprising:

a timing control unit;

a gate driving unit having a shift register and an output circuit; and

a control signal transmission line for transmitting a data carry signal for enabling the shift register and a signal for controlling an data output by the output circuit using a single signal line.

2. The device as claimed in claim 1, wherein the data carry signal uses a rising edge trigger system, and the output control signal uses a level trigger system.

3. The device as claimed in claim 1, wherein in order to prevent an overlapping of the data carry signal and the output control signal, the output control signal is outputted after one clock from a time point where the data carry signal is latched using the shift register.

* * * * *

专利名称(译)	用于驱动液晶显示器的装置		
公开(公告)号	US20040174467A1	公开(公告)日	2004-09-09
申请号	US10/670020	申请日	2003-09-24
[标]申请(专利权)人(译)	JUNG WOON HYUNG		
申请(专利权)人(译)	JUNG WOON HYUNG		
当前申请(专利权)人(译)	JUNG WOON HYUNG		
[标]发明人	JUNG WOON HYUNG		
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CPC分类号	G09G5/18 G09G3/3685		
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其他公开文献	US7250932		
外部链接	Espacenet USPTO		

摘要(译)

用于驱动LCD的装置包括定时控制单元，具有移位寄存器和输出电路的栅极驱动单元，以及用于发送用于使能移位寄存器的数据进位信号和用于控制数据输出的信号的控制信号传输线通过输出电路使用单个信号线。数据进位信号使用上升沿触发系统，输出控制信号使用电平触发系统。为了防止数据进位信号和输出控制信号的重叠，在使用移位寄存器锁存数据进位信号的时间点的一个时钟之后输出输出控制信号。