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Song et al.(10) **Pub. No.: US 2009/0273553 A1**(43) **Pub. Date: Nov. 5, 2009**(54) **LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF****Publication Classification**(51) **Int. Cl.****G09G 3/36**

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(57)

ABSTRACT

A liquid crystal display and a method of driving the same are disclosed. The liquid crystal display includes a liquid crystal display panel including data lines and gate lines crossing each other and liquid crystal cells, a timing control signal generating unit, a data drive circuit supplying a data voltage to the data lines, and a gate drive circuit. The timing control signal generating unit generates a first gate timing control signal for controlling a scan direction of the liquid crystal display panel in a sequential direction and a second gate timing control signal for controlling the scan direction in a reverse sequential direction. The gate drive circuit supplies a gate pulse to the gate lines while a shift direction of the gate pulse changes in response to the first and second gate timing control signals.

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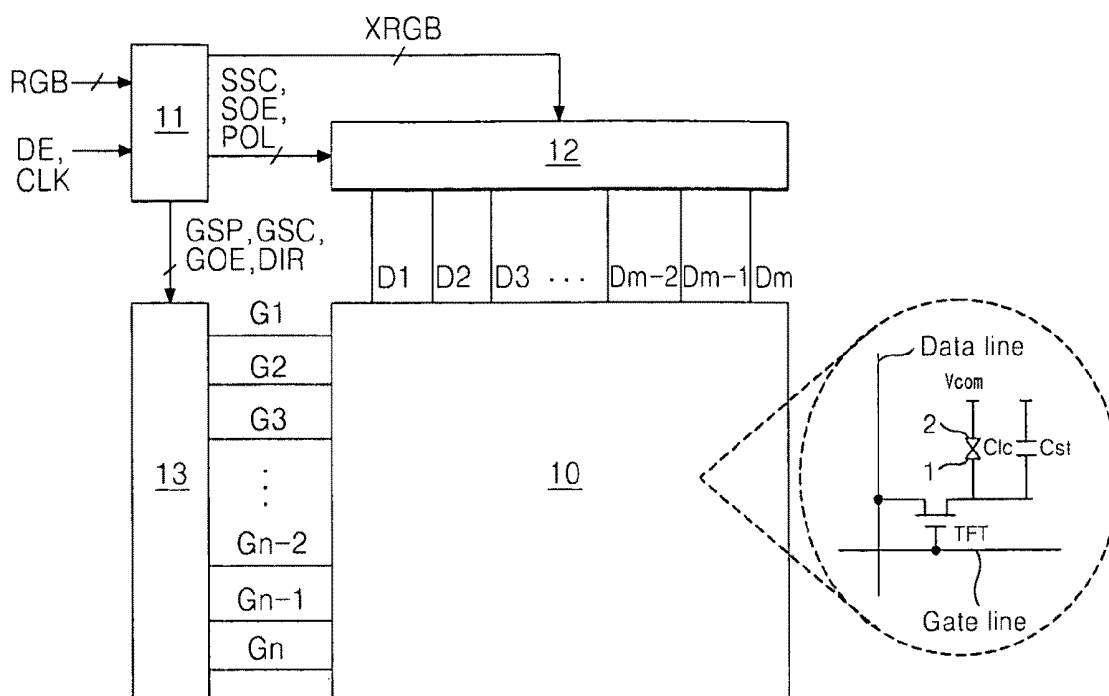


FIG. 1

(Related Art)

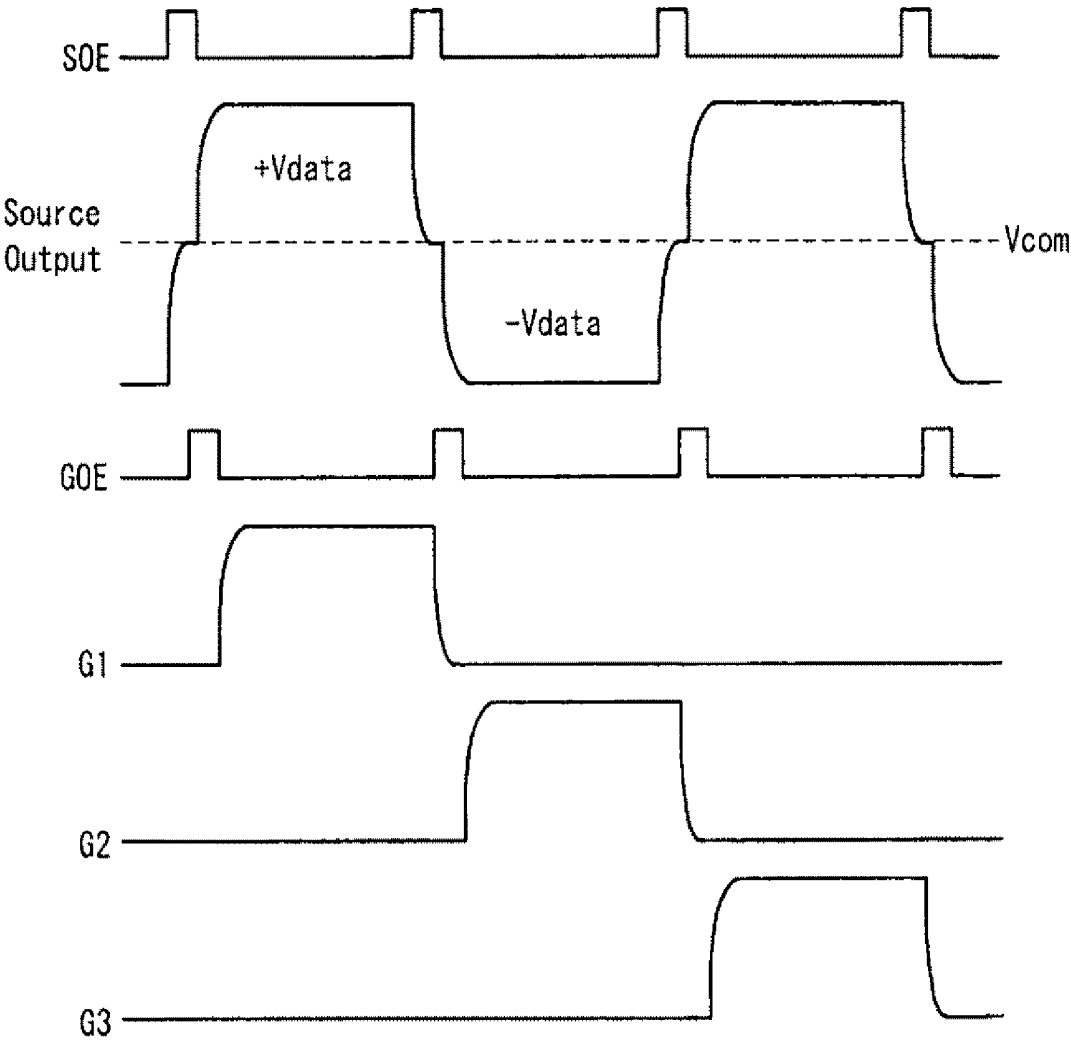


FIG. 2A

(Related Art)

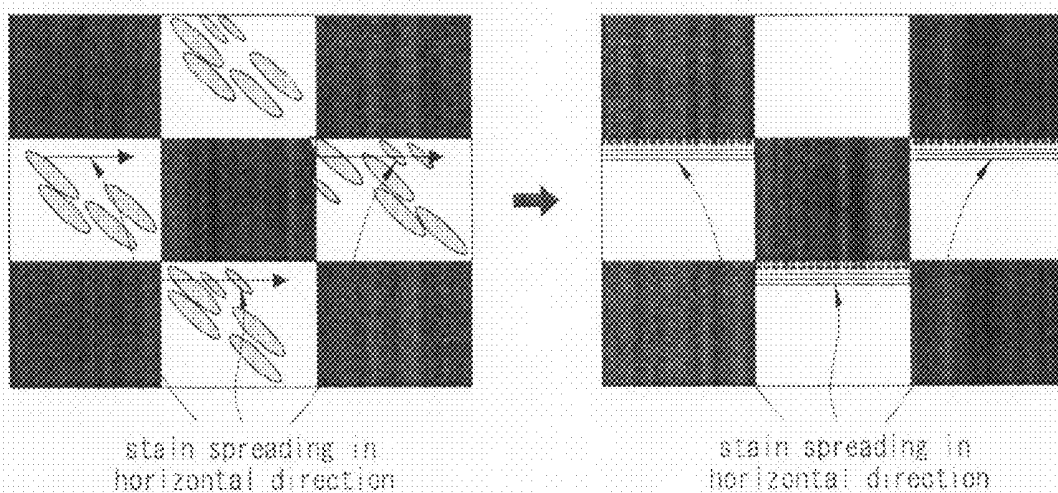


FIG. 2B

(Related Art)

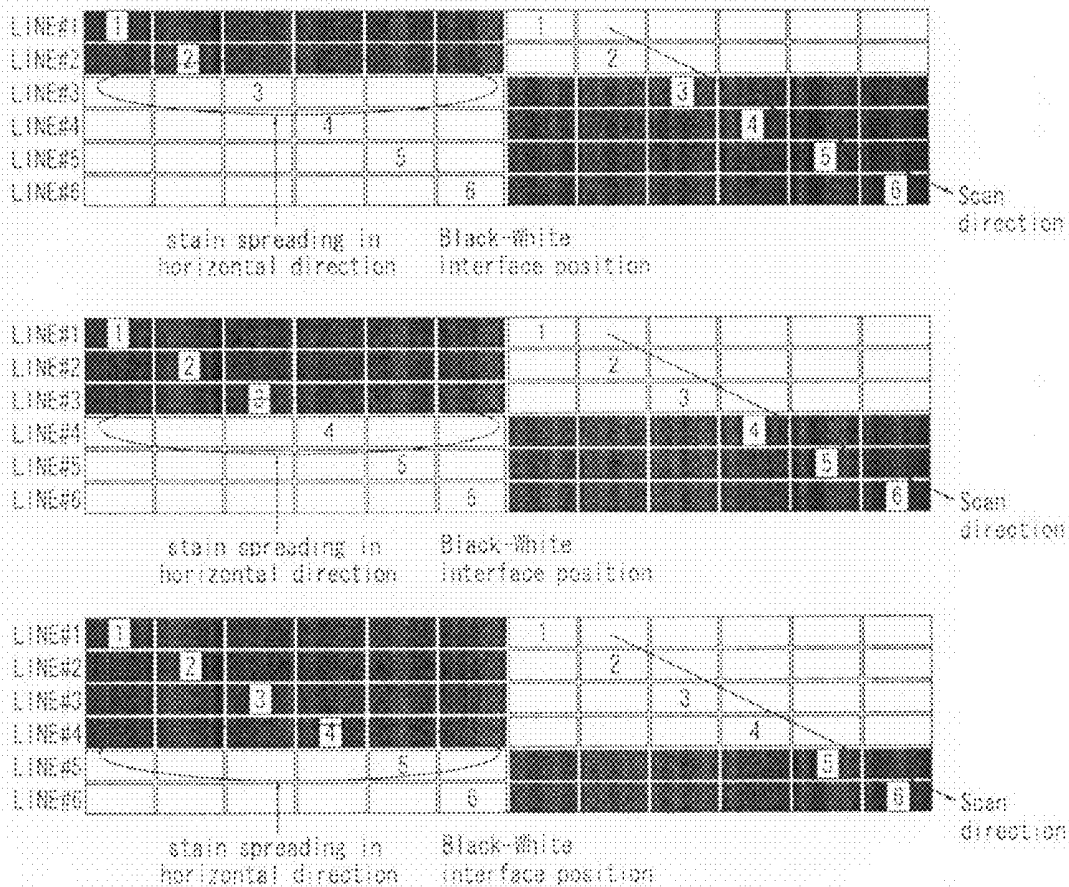


FIG. 3

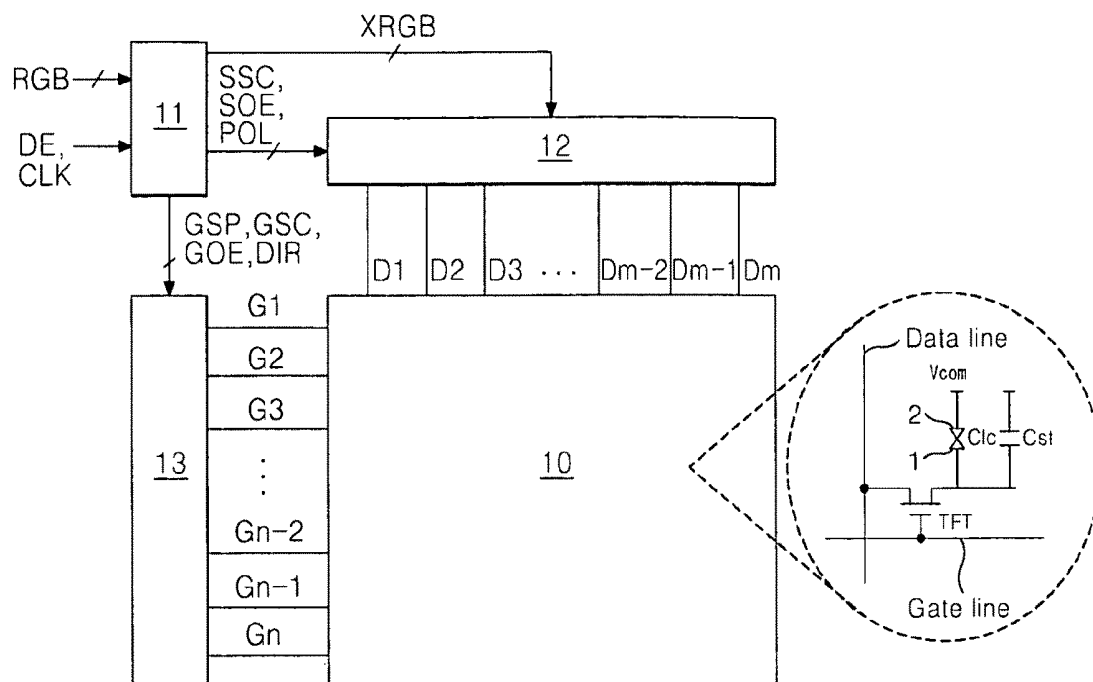


FIG. 4

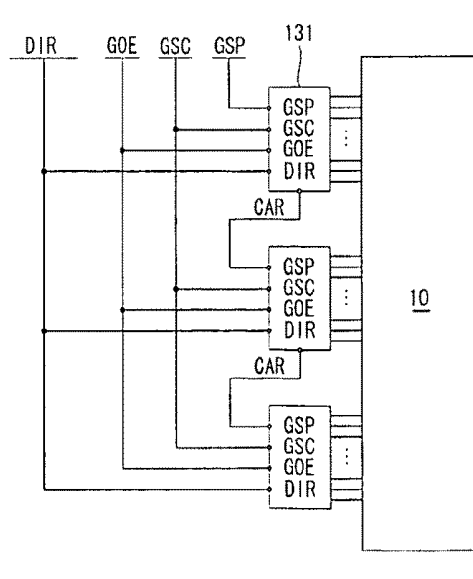


FIG. 5

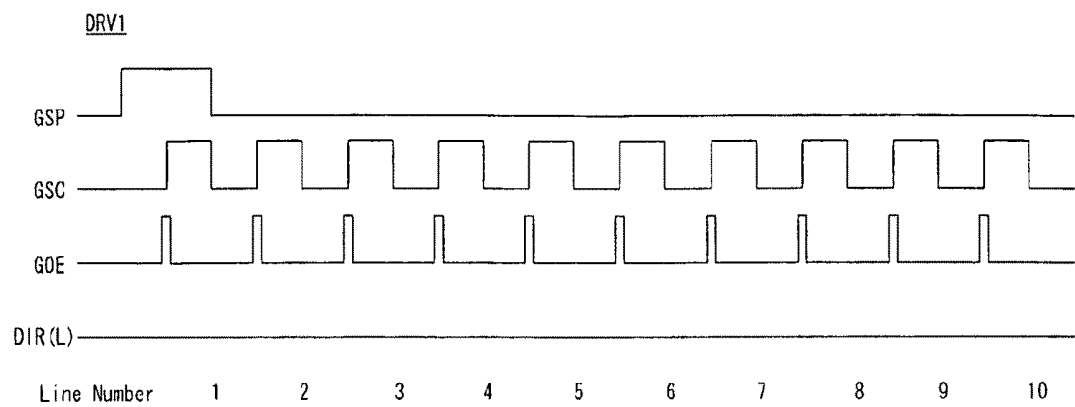


FIG. 6A

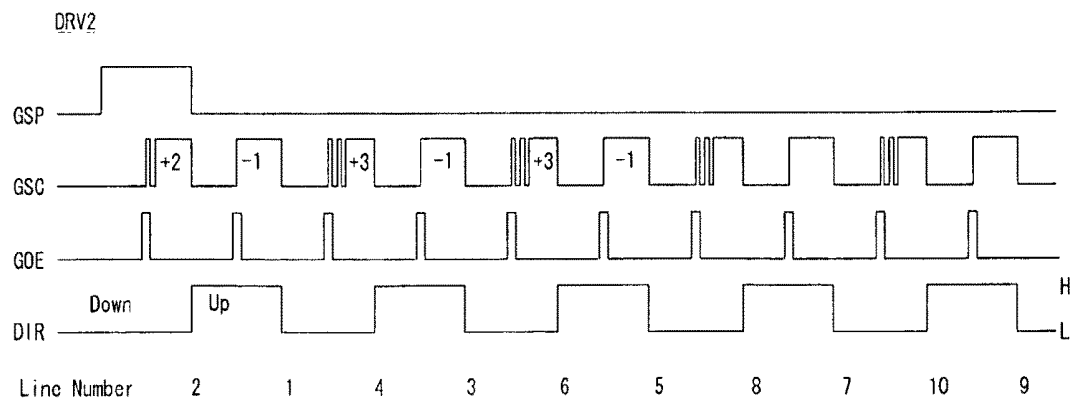


FIG. 6B

DRV2

LINE#1		1						1		W→B		
LINE#2	2							2				
LINE#3		B→W		3						3		
LINE#4			4							4		
LINE#5						5						5
LINE#6					6						6	

Black-White
interface position

LINE#1		1						1				
LINE#2	2							2				
LINE#3				3						B→W		
LINE#4			4							4		
LINE#5						5						5
LINE#6					6						6	

Black-White
interface position

LINE#1		1						1				
LINE#2	2							2				
LINE#3				3						3		
LINE#4			4							4		
LINE#5						5						5
LINE#6					6						6	

Black-White
interface position

FIG. 7A

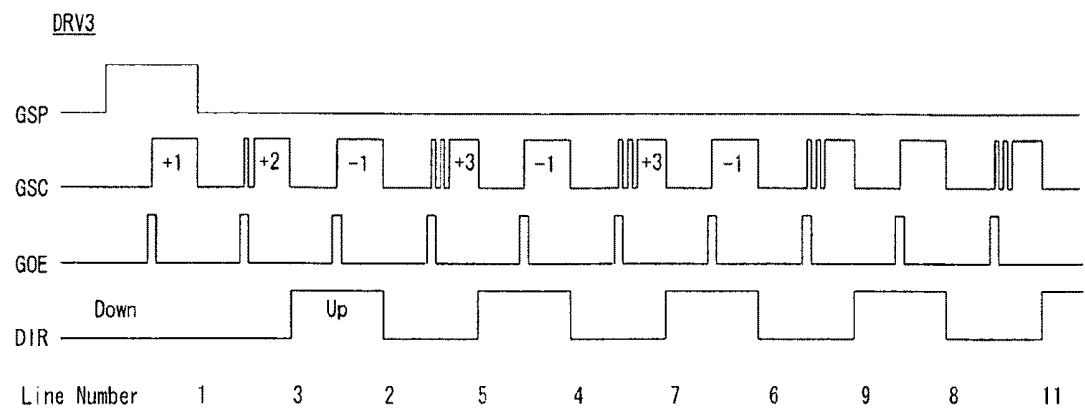


FIG. 7B

DRV3

LINE#1	1						1						
LINE#2			2						2	/B->W			
LINE#3		3	W->B					3					
LINE#4					4							4	
LINE#5				5						5			
LINE#6													

Black-White
interface position

LINE#1	1						1						
LINE#2			2						2				
LINE#3		3						3		W->B			
LINE#4			B->W		4							4	
LINE#5				5						5			
LINE#6													

Black-White
interface position

LINE#1	1						1						
LINE#2			2						2				
LINE#3		3						3				B->W	
LINE#4					4							4	
LINE#5				5	W->B					5			
LINE#6													

Black-White
interface position

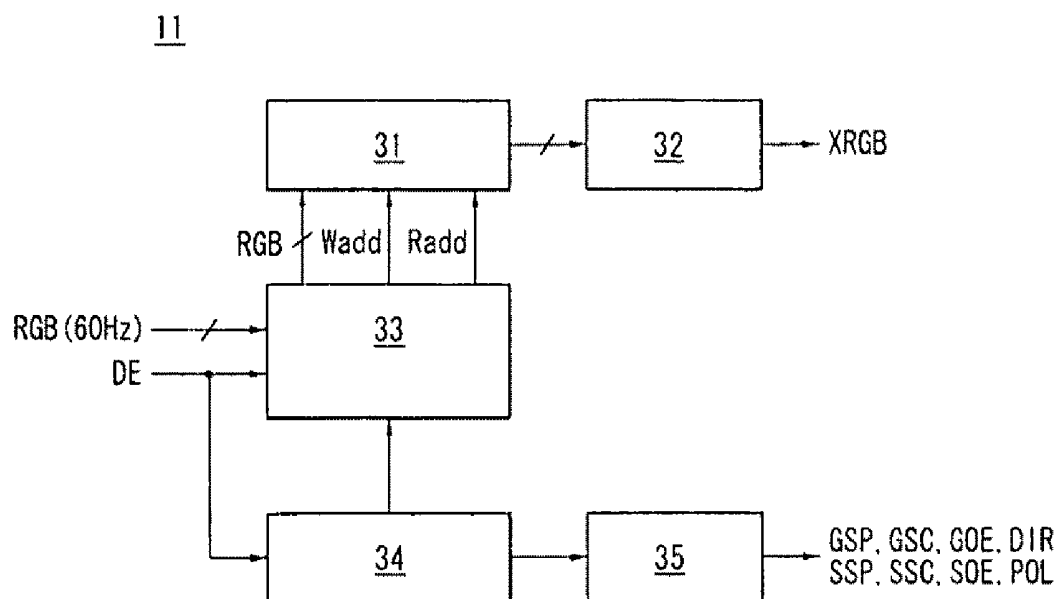
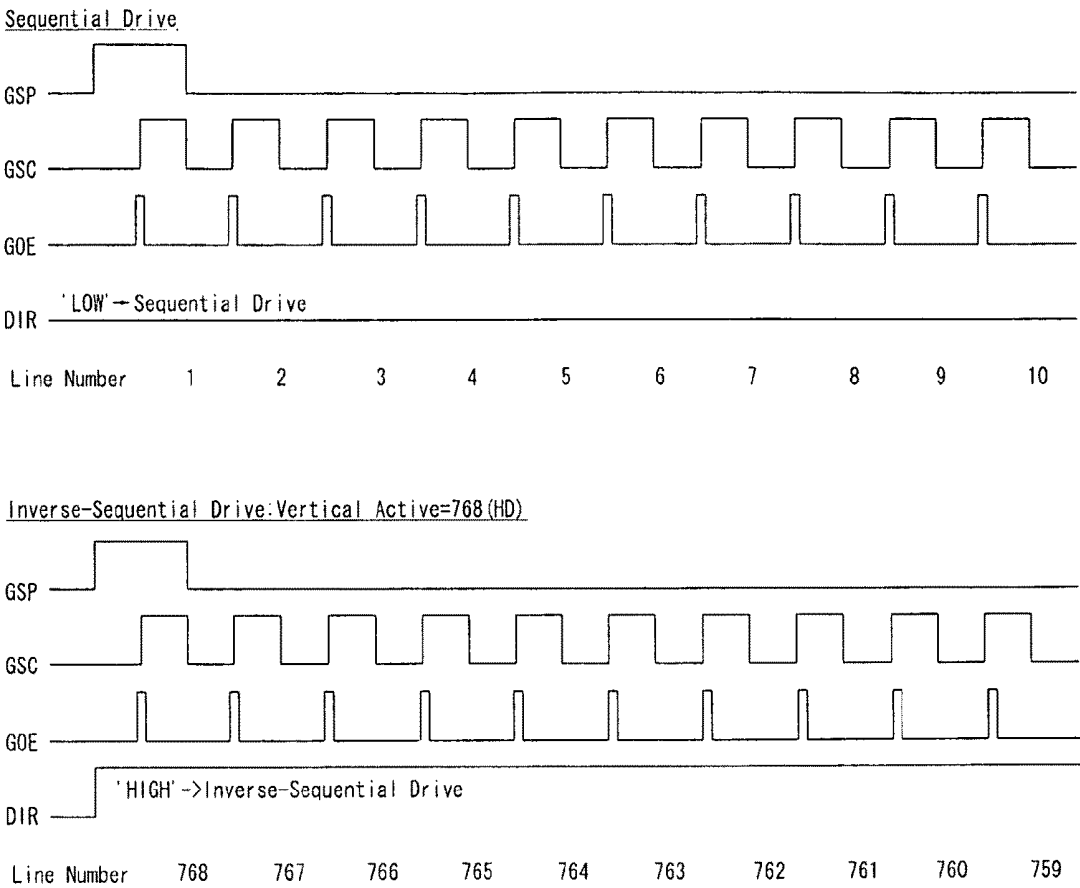
FIG. 8

FIG. 9



LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

[0001] This application claims the benefit of Korea Patent Application No. 10-2008-0040462 filed on Apr. 30, 2008, which is incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] An exemplary embodiment of the invention relates to a liquid crystal display and a method of driving the same.

[0004] 2. Discussion of the Related Art

[0005] Active matrix type liquid crystal displays display a moving picture using a thin film transistor (TFT) as a switching element. The active matrix type liquid crystal displays have been implemented in televisions as well as display devices in portable devices, such as office equipment and computers, because of the thin profile of the active matrix type liquid crystal displays. Accordingly, cathode ray tubes (CRT) are being replaced by active matrix type liquid crystal displays.

[0006] The active matrix type liquid crystal display includes data lines and gate lines crossing each other, and liquid crystal cells arranged at each crossing of the data lines and the gate lines in a matrix format. A thin film transistor (TFT) is formed at each crossing of the data lines and the gate lines. As shown in FIG. 1, data driver integrated circuits (ICs) of a liquid crystal display alternately supply a positive data voltage and a negative data voltage to the data lines during a low logic period of a source output enable signal SOE. Gate driver ICs of the liquid crystal display sequentially supply gate pulses synchronized with the positive and negative data voltages to the gate lines during a low logic period of a gate output enable signal GOE. The gate pulses are sequentially supplied to first to n-th gate lines to scan from an uppermost line of the display screen to a lowermost line of the display screen.

[0007] If a DC voltage is applied to a liquid crystal layer of the liquid crystal display for a long time, negative ions move in the same vector direction and positive ions move in the same vector direction opposite the vector direction of the negative ions depending on a polarity of an electric field applied to liquid crystals. Hence, the ions inside the liquid crystal layer are polarized. As time elapses, the accumulation of negative ions and the accumulation of positive ions increase. As a result, an alignment layer is degraded and alignment characteristics of the liquid crystal are degraded. In other words, if the DC voltage is applied to the liquid crystal display for a long time, stains appear on a display image, and the stains spread as time elapses.

[0008] FIG. 2A shows a mosaic pattern of test data for generating stains in a stain test process. In the mosaic pattern, black gray level blocks with the uniform size and white gray level blocks with the uniform size are alternately positioned upward and downward and right and left. If the liquid crystal display displays the mosaic pattern for a long time, stains appear in interfaces between the black gray level blocks and the white gray level blocks. Further, as time elapses, the stains spread in a transverse direction. In particular, the stains spreading in the transverse direction, as shown in FIGS. 2A and 2B, appear in the interfaces between the black gray level blocks and the white gray level blocks when the scanning of

the data voltages moves from the black gray level blocks to the white gray level blocks, but do not appear when the scanning of the data voltages moves from the white gray level blocks to the black gray level blocks. In FIG. 2B, a line number indicates each line number of the liquid crystal display, namely, a row number of liquid crystal cells, and a numeral inscribed on the black gray level blocks and the white gray level blocks indicates the scan order of the data voltages. The liquid crystal cell adjacent to the liquid crystal cell of the black gray level block is charged to a white gray level voltage while the liquid crystal cell of the black gray level block is held at a black gray level voltage, and ionic impurities mixed with the adjacent liquid crystal cells are polarized. The polarization adversely affects the alignment layer, and thus the stains appear.

[0009] The development of a liquid crystal material with a low dielectric constant or a method for improving an alignment material or an alignment method has been attempted so as to remove the stains. However, the method requires much time and expense to develop the material, and a reduction in a dielectric constant of the liquid crystal may cause a reduction in driving characteristics of the liquid crystal. According to the experimental findings, the appearance of the stains due to the polarization and the accumulation of the ions becomes rapid as the amount of impurities ionized inside the liquid crystal layer increases and a value of an acceleration factor increases. The acceleration factor includes a temperature, time, a DC drive of the liquid crystal, and the like. Accordingly, the stains rapidly appear and a stain level increases as a temperature rises or time for which a DC voltage with the same polarity is applied to the liquid crystal layer increases. Furthermore, because levels and shapes of the stains in the same model panels produced through the same production line are different from each other, the stain cannot be solved by the development of new material or an improvement in the manufacturing method.

SUMMARY OF THE INVENTION

[0010] Accordingly, the present invention is directed to a liquid crystal display and driving method thereof that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0011] An advantage of the present invention is to provide a liquid crystal display and a method of driving the same capable of increasing the display quality by preventing stains.

[0012] Additional features and advantages of the exemplary embodiments of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the exemplary embodiments of the invention. The objectives and other advantages of the exemplary embodiments of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0013] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a liquid crystal display comprises a liquid crystal display panel including a plurality of data lines, a plurality of gate lines crossing the data lines, and a plurality of liquid crystal cells, a timing control signal generating unit that generates a first gate timing control signal for controlling a scan direction of the liquid crystal display panel in a sequential direction and a second gate timing control signal for controlling the scan direction of the liquid crystal display

panel in a reverse sequential direction, a data drive circuit that supplies a data voltage to the data lines, and a gate drive circuit that supplies a gate pulse to the gate lines while a shift direction of the gate pulse changes in response to the first and second gate timing control signals.

[0014] In another aspect of the present invention, a method of driving a liquid crystal display including a liquid crystal display panel including a plurality of data lines, a plurality of gate lines crossing the data lines, and a plurality of liquid crystal cells, a data drive circuit that supplies a data voltage to the data lines, and a gate drive circuit that supplies a gate pulse to the gate lines, the method comprises generating a first gate timing control signal for controlling a scan direction of the liquid crystal display panel in a sequential direction and a second gate timing control signal for controlling the scan direction of the liquid crystal display panel in a reverse sequential direction, and supplying the first and second gate timing control signals to control terminals of the gate drive circuit to supply the gate pulse to the gate lines while a shift direction of the gate pulse changes.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of embodiments of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0017] FIG. 1 is a waveform diagram of a driving signal of a general liquid crystal display;

[0018] FIG. 2A shows a mosaic pattern of test data for generating stains and stains spreading in a transverse direction;

[0019] FIG. 2B shows a location of stains when interfaces between black gray level blocks and white gray level blocks move in the mosaic pattern of FIG. 2A;

[0020] FIG. 3 is a block diagram of a liquid crystal display according to an exemplary embodiment of the invention;

[0021] FIG. 4 shows gate driver integrated circuits (ICs) of a gate drive circuit shown in FIG. 3;

[0022] FIG. 5 is a waveform diagram of a first gate timing control signal;

[0023] FIG. 6A is a waveform diagram of a second gate timing control signal;

[0024] FIG. 6B shows a scan direction of a liquid crystal display panel driven by the second gate timing control signal of FIG. 6A when test data of a mosaic pattern is displayed on the liquid crystal display panel;

[0025] FIG. 7A is a waveform diagram of a third gate timing control signal;

[0026] FIG. 7B shows a scan direction of the liquid crystal display panel driven by the third gate timing control signal of FIG. 7A when test data of a mosaic pattern is displayed on the liquid crystal display panel;

[0027] FIG. 8 shows a circuit of a timing controller for increasing a transmission frequency of digital video data and multiplying data and gate timing control signals;

[0028] FIG. 9 is a waveform diagram of a fourth gate timing control signal; and

[0029] FIG. 10 is a timing diagram showing a data voltage of a mosaic pattern scanned by the fourth gate timing control signal of FIG. 9.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0030] Reference will now be made in detail embodiments of the invention examples of which are illustrated in the accompanying drawings.

[0031] As shown in FIG. 3, a liquid crystal display according to an exemplary embodiment of the invention includes a liquid crystal display panel 10, a timing controller 11, a data drive circuit 12, and a gate drive circuit 13.

[0032] The liquid crystal display panel 10 includes an upper glass substrate, a lower glass substrate, and a liquid crystal layer between the upper and lower glass substrates, all not shown. The lower glass substrate of the liquid crystal display panel 10 includes m data lines D1 to Dm and n gate lines G1 to Gn crossing each other. The liquid crystal display panel 10 includes mxn liquid crystal cells C1c arranged in a matrix format at each crossing of the m data lines D1 to Dm and the n gate lines G1 to Gn. The lower glass substrate further includes a thin film transistor TFT, a pixel electrode 1 of the liquid crystal cell C1c connected to the thin film transistor TFT, and a storage capacitor Cst.

[0033] The upper glass substrate of the liquid crystal display panel 10 includes a black matrix, a color filter, and a common electrode 2. The common electrode 2 is formed on the upper glass substrate in a vertical electric drive manner, such as a twisted nematic (TN) mode and a vertical alignment (VA) mode. The common electrode 2 and the pixel electrode 1 are formed on the lower glass substrate in a horizontal electric drive manner, such as an in-plane switching (IPS) mode and a fringe field switching (FFS) mode. Polarizing plates each having optical axes that cross at a right angle are attached respectively to the upper and lower glass substrates. Alignment layers for setting a pre-tilt angle of the liquid crystal in an interface contacting the liquid crystal are respectively formed on the upper and lower glass substrates.

[0034] The timing controller 11 supplies digital video data XRGB to the data drive circuit 12. The timing controller 11 receives timing signals such as a data enable signal DE and a dot clock signal CLK, and generates a data timing control signal for controlling operation timing of the data drive circuit 12 and a gate timing control signal for controlling operation timing of the gate drive circuit 13.

[0035] The data timing control signal includes a source start pulse SSP, a source sampling clock signal SSC, a source output enable signal SOE, and a polarity control signal POL. The source start pulse SSP indicates a start pixel in 1 horizontal line to which data will be displayed. The source sampling clock signal SSC controls a data latch operation inside the data drive circuit 12 based on a rising or falling edge. The source output enable signal SOE directs an output of the data drive circuit 12. A logic state of the polarity control signal POL is inverted every scan time of 1 line or scan time of 2 lines, and a phase of the polarity control signal POL is inverted in each frame period. The polarity control signal POL controls a polarity of a data voltage to be supplied to the liquid crystal cells C1c of the liquid crystal display panel 10.

[0036] The gate timing control signal includes a gate start pulse GSP, a gate shift clock signal GSC, a gate output enable signal GOE, a scan direction control signal DIR, and the like. The gate start pulse GSP indicates a scan start line (or a row

of the liquid crystal cell) of a scan operation during 1 vertical period in which one screen is displayed. The gate shift clock signal GSC is a timing control signal that is input to a shift resistor installed in the gate drive circuit 13 to sequentially shift the gate start pulse GSP, and has a pulse width corresponding to a turned-on period of the thin film transistor TFT. The gate output enable signal GOE directs an output of the gate drive circuit 13. The scan direction control signal DIR controls a shift direction of the scan pulses.

[0037] The timing controller 11 does not multiply a driving frequency of the liquid crystal display panel 10 and periodically controls a scan direction of the liquid crystal display panel 10. The timing controller 11 controls the scan direction of the liquid crystal display panel 10 in a sequential direction of lines, and periodically controls the scan direction of the liquid crystal display panel 10 in zigzag or in a reverse sequential direction of lines during even-numbered frame periods. The scan direction may change every N frame periods or every N seconds, where N is a positive integer. For this, the timing controller 11 generates the scan direction control signal DIR periodically having a different pattern. When the scan direction control signal DIR is generated in a low logic state, the liquid crystal display panel 10 is scanned in the sequential direction of lines. When the scan direction control signal DIR is generated in a high logic state, the liquid crystal display panel 10 is scanned in the reverse sequential direction of lines.

[0038] The timing controller 11 multiplies the driving frequency of the liquid crystal display panel 10 by N, and thus can periodically control the scan direction of the liquid crystal display panel 10.

[0039] The data drive circuit 12 includes a plurality of data driver integrated circuits (ICs). Each of the data driver ICs includes a shift resistor, a latch, a digital-to-analog converter, a buffer, and the like. The data drive circuit 12 latches the digital video data XRGB under the control of the timing controller 11 and converts the digital video data XRGB into analog positive and negative gamma compensation voltages to supply the analog positive and negative gamma compensation voltages to the data lines D1 to Dm. The data drive circuit 12 inverts a polarity of the data voltage in response to the polarity control signal POL.

[0040] The gate drive circuit 13, as shown in FIG. 4, includes a plurality of gate driver ICs 131. The gate drive circuit 13 includes a shift register, a level shifter for converting an output signal of the shift resistor into a signal having a swing width suitable for a TFT drive of the liquid crystal cell C1c, and an output buffer, all not shown. While the gate drive circuit 13 shifts gate pulses (or scan pulses) upward or downward depending on a logic state of the scan direction control signal DIR, the gate drive circuit 13 outputs the gate pulses. In other words, while the gate driver ICs 131 shift the gate pulses in the sequential direction from the top to the bottom of the screen in response to the scan direction control signal DIR received from the timing controller 11, the gate driver ICs 131 output the gate pulses. Otherwise, while the gate driver ICs 131 shift the gate pulses in the reverse sequential direction from the bottom to the top of the screen, the gate driver ICs 131 output the gate pulses. In FIG. 4, "CAR" indicates a carry signal, that is generated in one gate driver IC 131 and then transmitted to the next gate driver IC 131, among the other gate driver ICs 131 except the first gate driver IC 131 first

outputting the gate pulse. The carry signal CAR serves as a gate state pulse of the other gate driver ICs 131 except the first gate driver IC 131.

[0041] The gate driver ICs 131 are dividedly attached at the left and right sides of the liquid crystal display panel 10 so as to reduce the delay and the voltage drop of the gate pulses in the large-sized liquid crystal display panel 10, and thus the gate driver ICs 131 at both sides of the gate lines can simultaneously apply the gate pulses to the gate lines. In this case, because the liquid crystal display panel 10 is scanned in the sequential direction, the gate driver ICs 131 at the left side of the liquid crystal display panel 10 shift the gate pulses in the sequential direction and output the gate pulses, but the gate driver ICs 131 at the right side of the liquid crystal display panel 10 shift the gate pulses in the reverse sequential direction and output the gate pulses because a direction of output terminals of the gate driver ICs 131 changes. The scan direction control signal DIR is fixed at a predetermined voltage or a predetermined logic level so as to achieve the above-described propose. On the contrary, the liquid crystal display according to the exemplary embodiment of the invention periodically inverts a logic level of the scan direction control signal DIR, and thus allows the gate driver ICs 131 to alternately control a shift direction of the gate pulses in the sequential direction and the reverse sequential direction.

[0042] The liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention alternately apply a first gate timing control signal DRV1 shown in FIG. 5 and a second gate timing control signal DRV2 shown in FIG. 6A to the gate driver ICs 131 of the gate drive circuit 13. As described above, a driving period of the liquid crystal display panel 10 driven by the second gate timing control signal DRV2 is N frame periods or N seconds. Accordingly, the liquid crystal display panel 10 is scanned in the sequential direction in response to the first gate timing control signal DRV1, and a scan direction of the liquid crystal display panel 10 changes in response to the second gate timing control signal DRV2 every N frame periods or N seconds.

[0043] FIG. 5 is a waveform diagram of the first gate timing control signal DRV1.

[0044] As shown in FIG. 5, the first gate timing control signal DRV1 is a control signal for controlling a scan direction of the liquid crystal display panel 10 in the sequential direction.

[0045] In the first gate timing control signal DRV1, a gate start pulse GSP is once generated in the initial of 1 frame period when scan time starts. A pulse of a gate shift clock signal GSC is generated every 1 horizontal period and the generation number of pulses of the gate shift clock signal GSC is equal to the number of gate lines. A gate output enable signal GOE is generated in synchronization with a rising edge of the gate shift clock signal GSC. A scan direction control signal DIR is maintained in a low logic state.

[0046] The gate driver ICs 131 of the gate drive circuit 13 shift the gate pulses synchronized with the positive and negative data voltages in pulses of the gate shift clock signal GSC in the sequential direction, namely, in a shift direction from the top to the bottom in response to the scan direction control signal DIR of the low logic state, and sequentially supply the gate pulses to the gate lines G1 to Gn. Accordingly, if the first gate timing control signal DRV1 is generated, the gate pulse is supplied to the first gate line G1, and then the gate pulses are sequentially supplied to the second to n-th gate lines G2 to

Gn. If the liquid crystal display panel 10 is scanned by the first gate timing control signal DRV1 and displays the test data of the mosaic pattern shown in FIG. 2A, the scan direction of the liquid crystal display panel 10 is the same as the scan direction shown in FIG. 2B.

[0047] FIG. 6A is a waveform diagram of the second gate timing control signal DRV2. FIG. 6B shows a scan direction of the liquid crystal display panel 10 driven by the second gate timing control signal DRV2 when test data of a mosaic pattern is displayed on the liquid crystal display panel 10.

[0048] As shown in FIG. 6A, the second gate timing control signal DRV2 is a control signal for alternately scanning the liquid crystal display panel 10 in the sequential direction and the reverse sequential direction.

[0049] In the second gate timing control signal DRV2, a gate start pulse GSP is once generated in the initial of 1 frame period when scan time starts. In a gate shift clock signal GSC, one pulse with a short width and one pulse with a long width are generated within a first horizontal period. Sequentially, after one pulse with a long width is generated within a second horizontal period, two pulses with a short width and one pulse with a long width are generated within a third horizontal period. Then, in the gate shift clock signal GSC, the pulse waveform generated during the second and third horizontal periods is repeatedly generated during horizontal periods following the third horizontal period. A gate output enable signal GOE is generated in synchronization with a rising edge of the gate shift clock signal GSC. A scan direction control signal DIR is generated in a low logic state during odd-numbered horizontal periods and is generated in a high logic state during even-numbered horizontal periods. A pulse width of the scan direction control signal DIR is larger than a pulse width of the gate shift clock signal GSC and has a pulse width corresponding to 1 horizontal period. A second half portion of each of pulses of the scan direction control signal DIR overlaps the long pulses of the gate shift clock signal GSC generated during the even-numbered horizontal periods and pulses of the gate output enable signal GOE generated during the even-numbered horizontal periods.

[0050] When the scan direction control signal DIR is generated in a low logic state, the gate drive circuit 13 shifts the gate pulses in the sequential direction from the top to the bottom of the screen. When the scan direction control signal DIR is generated in a high logic state, the gate drive circuit 13 shifts the gate pulses in the reverse sequential direction from the bottom to the top of the screen. The number of shift operations of the gate pulses is equal to the number of pulses of the gate shift clock signal GSC generated during 1 horizontal period. Accordingly, if the scan direction control signal DIR and the gate shift clock signal GSC are generated as shown in FIG. 6A, the gate drive circuit 13 shifts the gate start pulse GSP 2 times in the sequential direction during the first horizontal period and supplies the gate pulse to the second gate line G2. Sequentially, after the gate drive circuit 13 shifts the gate pulse once in the reverse sequential direction during the second horizontal period and supplies the gate pulse to the first gate line G1, the gate drive circuit 13 shifts the gate pulse three times in the sequential direction during the third horizontal period and supplies the gate pulse to the fourth gate line G4. Then, the gate drive circuit 13 shifts the gate pulse once in the reverse sequential direction during the fourth horizontal period and supplies the gate pulse to the third gate line G3. After the gate drive circuit 13 shifts the gate pulse three times in the sequential direction during a horizontal period and

supplies the gate pulse to the n-th gate line Gn, the gate drive circuit 13 shifts the gate pulse once in the reverse sequential direction during a next horizontal period and supplies the gate pulse to the (n-1)-th gate line Gn-1.

[0051] Because the liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention scans the liquid crystal display panel 10 while the scan direction of the liquid crystal display panel 10 changes every N frame periods or N seconds, the data voltage is shifted from a white gray level block to a black gray level block in an interface between the black gray level block and the white gray level block even if the liquid crystal display displays the mosaic pattern shown in FIG. 2A for a long time. As a result, the liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention supply the gate pulses to the gate lines while the shift direction of the gate pulses changes, and thus can suppress the polarization of impurity ions inside the liquid crystal layer and can prevent the stains and the stain spreading.

[0052] The liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention alternately apply the first gate timing control signal DRV1 shown in FIG. 5 and a third gate timing control signal DRV3 shown in FIG. 7A to the gate driver ICs 131 of the gate drive circuit 13. As described above, a driving period of the liquid crystal display panel 10 driven by the third gate timing control signal DRV3 is N frame periods or N seconds. Accordingly, the liquid crystal display panel 10 is scanned in the sequential direction in response to the first gate timing control signal DRV1, and a scan direction of the liquid crystal display panel 10 changes in response to the third gate timing control signal DRV3 every N frame periods or N seconds.

[0053] FIG. 7A is a waveform diagram of the third gate timing control signal DRV3. FIG. 7B shows a scan direction of the liquid crystal display panel 10 driven by the third gate timing control signal DRV3 when test data of a mosaic pattern is displayed on the liquid crystal display panel 10.

[0054] As shown in FIG. 7A, the third gate timing control signal DRV3 is a control signal for alternately scanning the liquid crystal display panel 10 in the sequential direction and the reverse sequential direction.

[0055] In the third gate timing control signal DRV3, the gate start pulse GSP is once generated in the initial of 1 frame period when scan time starts. In the gate shift clock signal GSC, one pulse with a long width is generated within a first horizontal period, and then one pulse with a short width and one pulse with a long width are generated within a second horizontal period. Sequentially, after one pulse with a long width is generated within a third horizontal period, two pulses with a short width and one pulse with a long width are generated within a fourth horizontal period. The pulse waveform generated during the third and fourth horizontal periods is repeatedly generated during horizontal periods following the fourth horizontal period. The gate output enable signal GOE is generated in synchronization with a rising edge of the gate shift clock signal GSC. After the scan direction control signal DIR is maintained in a low logic state the first and second horizontal periods, the scan direction control signal DIR is generated in a high logic state during odd-numbered horizontal periods and is generated in a low logic state during even-numbered horizontal periods. A pulse width of the scan direction control signal DIR is larger than a pulse width of the gate shift clock signal GSC and has a pulse width corresponding to 1 horizontal period. A second half portion of each of pulses of

the scan direction control signal DIR overlaps the pulses of the gate shift clock signal GSC generated during the other odd-numbered horizontal periods except the first horizontal period and pulses of the gate output enable signal GOE generated during the odd-numbered horizontal periods.

[0056] When the scan direction control signal DIR is generated in a low logic state, the gate drive circuit 13 shifts the gate pulses in the sequential direction from the top to the bottom of the screen. When the scan direction control signal DIR is generated in a high logic state, the gate drive circuit 13 shifts the gate pulses in the reverse sequential direction from the bottom to the top of the screen. The number of shift operations of the gate pulses is equal to the number of pulses of the gate shift clock signal GSC generated during 1 horizontal period. Accordingly, if the scan direction control signal DIR and the gate shift clock signal GSC are generated as shown in FIG. 7A, the gate drive circuit 13 shifts the gate start pulse GSP once in the sequential direction during the first horizontal period and supplies the gate pulse to the first gate line G1. Sequentially, after the gate drive circuit 13 shifts the gate pulse two times in the sequential direction during the second horizontal period and supplies the gate pulse to the third gate line G3, the gate drive circuit 13 shifts the gate pulse once in the reverse sequential direction during the third horizontal period and supplies the gate pulse to the second gate line G2. Sequentially, after the gate drive circuit 13 shifts the gate pulse three times in the sequential direction during the fourth horizontal period and supplies the gate pulse to the fifth gate line G5, the gate drive circuit 13 shifts the gate pulse once in the reverse sequential direction during the fifth horizontal period and supplies the gate pulse to the fourth gate line G4. The gate drive circuit 13 repeatedly performs the above-described operations, and thus supplies the gate pulses to the gate lines G1 to Gn in order of the (n-4)-th, (n-2)-th, (n-3)-th, n-th, and (n-1)-th gate lines.

[0057] Because the liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention scan the liquid crystal display panel 10 while the scan direction of the liquid crystal display panel 10 changes every N frame periods or N seconds, the data voltage is shifted from a white gray level block to a black gray level block in an interface between the black gray level block and the white gray level block even if the liquid crystal display displays the mosaic pattern shown in FIG. 2A for a long time. As a result, the liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention supply the gate pulses to the gate lines while the shift direction of the gate pulses changes, and thus can suppress the polarization of impurity ions inside the liquid crystal layer and can prevent the stains and the stain spreading.

[0058] FIG. 8 shows a circuit of the timing controller 11 for increasing a transmission frequency of the digital video data and multiplying the data and gate timing control signals.

[0059] As shown in FIG. 8, the timing controller 11 includes a memory 31, an interface transmitting unit 32, a memory controller 33, a frequency multiplier 34, and a timing control signal generating unit 35.

[0060] The memory 31 is implemented as a frame memory. The memory 31 stores the digital video data RGB in response to a write address signal Wadd generated based on the non-multiplied data enable signal DE and outputs the stored digital video data in response to a read address signal Radd, whose frequency rises, based on the multiplied data enable signal DE. The memory 31 successively outputs the same

data two times during a first half period and a second half period of a multiplied frame period under the control of the memory controller 33.

[0061] The interface transmitting unit 32 transmits the digital video data XRGB output from the memory 31 and mini low-voltage differential signaling (LVDS) clock to the data drive circuit 12 in a mini LVDS manner. In case the data is transmitted in the mini LVDS manner, because a pulse following a reset pulse of the mini LVDS clock serves as the source start pulse SSP, the timing control signal generating unit 35 does not need to generate a separate source start pulse SSP.

[0062] The memory controller 33 generates the write address signal Wadd suitable for the input data enable signal DE and generates the read address signal Radd suitable for the data enable signal DE whose an input frequency is multiplied by 2. A reason why an output speed of the memory 31 increases is that the digital video data XRGB is supplied to the data drive circuit 12 when the liquid crystal display panel 10 is driven by the first gate timing control signal DRV1 during a first half period of a frame period as shown in FIG. 9, and then the same data XRGB has to be supplied to the data drive circuit 12 during a second half period of the frame period.

[0063] The frequency multiplier 34 multiplies a frequency of the data enable signal DE by 2. The data enable signal DE is generated every 1 horizontal period based on an input frame frequency of the data enable signal DE. For example, if the input frame frequency is 60 Hz, the liquid crystal display panel 10 is driven at a frame frequency of 120 Hz.

[0064] The timing control signal generating unit 35 generates the gate timing control signals GSP, GSC, GOE and DIR and the data timing control signals SSP, SSC, SOE and POL based on the data enable signal DE whose the frequency is multiplied by 2. Accordingly, frequencies of the gate and data timing control signals output from the timing control signal generating unit 35 is two times higher than frequencies of the gate and data timing control signals generated when the liquid crystal display panel 10 is driven at 60 Hz.

[0065] The liquid crystal display and the method of driving the same, according to the exemplary embodiment of the invention, drive the liquid crystal display panel 10 at 120 Hz by multiplying the frame frequency by 2, and time-divide 1 frame period corresponding to $1/60$ sec into a first half sub-frame period and a second half sub-frame period to drive the liquid crystal display panel 10. Further, the liquid crystal display and the method of driving the same, according to the exemplary embodiment of the invention, apply the first gate timing control signal shown in the top of FIG. 9 to the gate driver ICs 131 during a first half sub-frame period of each frame period to control the scan direction in the sequential direction. Then, the liquid crystal display and the method of driving the same, according to the exemplary embodiment of the invention, apply the fourth gate timing control signal shown in the bottom of FIG. 9 to the gate driver ICs 131 to control the scan direction in the reverse sequential direction.

[0066] FIG. 9 shows first to fourth gate timing control signals. FIG. 10 shows a scan direction of the liquid crystal display panel 10 driven by the gate timing control signal of FIG. 9 when test data of a mosaic pattern is displayed on the liquid crystal display panel 10.

[0067] As shown in FIG. 9, the first gate timing control signal of FIG. 9 is substantially the same as the first gate timing control signal of FIG. 5 except that a frequency of the first gate timing control signal of FIG. 9 is higher than a

frequency of the first gate timing control signal of FIG. 5. The fourth gate timing control signal controls a shift direction of the gate pulse in the reverse sequential direction from the bottom to the top of the screen. In other words, after the gate driver ICs 131 supply a gate pulse to a gate line of the last line LINE#768 in response to the fourth gate timing control signal, the gate driver ICs 131 shift the gate pulse upward by 1 line and lastly supply a gate pulse to a gate line of the first line LINE#1. A gate start pulse GSP, a gate shift clock signal GSC, and a gate output enable signal GOE of the fourth gate timing control signal are substantially the same as those of the first gate timing control signal. On the other hand, a scan direction control signal DIR of the fourth gate timing control signal is generated in a high logic state during the second half sub-frame period.

[0068] The liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention scan the entire screen of the liquid crystal display panel in the sequential direction every 1 frame period as shown in FIG. 10, and then scan the entire screen in the reverse sequential direction. Hence, the data voltage is shifted from a white gray level block to a black gray level block in an interface between the black gray level block and the white gray level block even if the liquid crystal display displays the mosaic pattern shown in FIG. 2A for a long time. As a result, the liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention supply the gate pulses to the gate lines while the shift direction of the gate pulses changes, and thus can suppress the polarization of impurity ions inside the liquid crystal layer and can prevent the stains and the stain spreading.

[0069] Although the exemplary embodiment of the invention has described the mosaic data as the test data, the exemplary embodiment of the invention may drive the liquid crystal display panel when general video data is displayed.

[0070] As described above, the liquid crystal display and the method of driving the same according to the exemplary embodiment of the invention periodically changes a method for scanning the liquid crystal display panel, and thus can suppress the polarization of impurity ions inside the liquid crystal layer and can prevent the stains and the stain spreading. Hence, the display quality of the liquid crystal display can be improved.

[0071] It will be apparent to those skilled in the art that various modifications and variations can be made in the embodiments of the invention without departing from the spirit or scope of the invention. Thus, it is intended that embodiments of the invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines crossing the data lines, and a plurality of liquid crystal cells;

a timing control signal generating unit that generates a first gate timing control signal for controlling a scan direction of the liquid crystal display panel in a sequential direction and a second gate timing control signal for controlling the scan direction of the liquid crystal display panel in a reverse sequential direction;

a data drive circuit that supplies a data voltage to the data lines; and

a gate drive circuit that supplies a gate pulse to the gate lines while a shift direction of the gate pulse changes in response to the first and second gate timing control signals.

2. The liquid crystal display of claim 1, wherein after the gate drive circuit supplies the gate pulse to the gate lines while the gate drive circuit shifts the gate pulse in the sequential direction in response to the first gate timing control signal, the gate drive circuit supplies the gate pulse to the gate lines while the gate drive circuit shifts the gate pulse in the reverse sequential direction in response to the second gate timing control signal.

3. The liquid crystal display of claim 1, wherein the first gate timing control signal includes a first scan direction control signal, that is maintained in a low logic state, for controlling the scan direction of the liquid crystal display panel in the sequential direction, and

the second gate timing control signal includes an alternate type second scan direction control signal, wherein the logic state of the second scan direction control signal is periodically inverted, for alternately controlling the scan direction of the liquid crystal display panel in the sequential direction and in the reverse sequential direction.

4. The liquid crystal display of claim 1, wherein the gate lines include first to fourth gate lines sequentially positioned on the liquid crystal display panel, and

the gate drive circuit sequentially supplies the gate pulses to the first to fourth gate lines in order of the second, first, fourth, and third gate lines in response to the second gate timing control signal.

5. The liquid crystal display of claim 1, wherein the gate lines include first to third gate lines sequentially positioned on the liquid crystal display panel, and

the gate drive circuit sequentially supplies the gate pulses to the first to third gate lines in order of the first, third, and second gate lines in response to the second gate timing control signal.

6. The liquid crystal display of claim 1, further comprising: a memory that stores digital video data and transmits the stored digital video data to the data drive circuit;

a frequency multiplier that multiplies a frequency of an input timing signal, that has a frame frequency of 60 Hz as a base frequency, by 2; and

a memory controller that raises a transmission frequency of the digital video data output from the memory based on the timing signal, wherein the frequency is multiplied by 2,

wherein the timing control signal generating unit raises frequencies of the gate timing control signals to be suitable for a frame frequency of 120 Hz based on the timing signal, wherein the frequency is multiplied by 2.

7. The liquid crystal display of claim 6, wherein the liquid crystal display panel displays an image in each frame period that is time-divided into a first half sub-frame period and a second half sub-frame period,

the first gate timing control signal is generated during the first half sub-frame period and includes a first scan direction control signal, that is maintained in a low logic state, for controlling the scan direction of the liquid crystal display panel in the sequential direction, and

the second gate timing control signal is generated during the second half sub-frame period and includes a second scan direction control signal, that is maintained in a high

logic state, for controlling the scan direction of the liquid crystal display panel in the reverse sequential direction.

8. A method of driving a liquid crystal display including a liquid crystal display panel including a plurality of data lines, a plurality of gate lines crossing the data lines, and a plurality of liquid crystal cells, a data drive circuit that supplies a data voltage to the data lines, and a gate drive circuit that supplies a gate pulse to the gate lines, the method comprising:

generating a first gate timing control signal for controlling a scan direction of the liquid crystal display panel in a sequential direction and a second gate timing control signal for controlling the scan direction of the liquid crystal display panel in a reverse sequential direction; and

supplying the first and second gate timing control signals to control terminals of the gate drive circuit to supply the gate pulse to the gate lines while a shift direction of the gate pulse changes.

9. The method of claim 8, wherein supplying the gate pulse to the gate lines includes alternately supplying the first and second gate timing control signals to the control terminals of the gate drive circuit to supply the gate pulse to the gate lines while the gate pulse is shifted in the sequential direction, and then to supply the gate pulse to the gate lines while the gate pulse is shifted in the reverse sequential direction.

10. The method of claim 8, wherein the first gate timing control signal includes a first scan direction control signal, that is maintained in a low logic state, for controlling the scan direction of the liquid crystal display panel in the sequential direction, and

the second gate timing control signal includes an alternate type second scan direction control signal, whose a logic state is periodically inverted, for alternately controlling the scan direction of the liquid crystal display panel in the sequential direction and in the reverse sequential direction.

11. The method of claim 8, further comprising:

multiplying a frequency of an input timing signal, that has a frame frequency of 60 Hz as a base frequency, by 2; storing digital video data based on the frame frequency of 60 Hz to transmit the digital video data, whose a data transmission frequency increases to a frame frequency of 120 Hz based on the stored timing signal whose the frequency is multiplied by 2, to the data drive circuit; and raising frequencies of the timing control signals to be suitable for the frame frequency of 120 Hz based on the timing signal, whose the frequency is multiplied by 2.

12. The method of claim 11, wherein the liquid crystal display panel displays an image in each frame period that is time-divided into a first half sub-frame period and a second half sub-frame period,

the first gate timing control signal is generated during the first half sub-frame period and includes a first scan direction control signal, that is maintained in a low logic state, for controlling the scan direction of the liquid crystal display panel in the sequential direction, and

the second gate timing control signal is generated during the second half sub-frame period and includes a second scan direction control signal, that is maintained in a high logic state, for controlling the scan direction of the liquid crystal display panel in the reverse sequential direction.

13. The method of claim 8, wherein the gate lines include first to fourth gate lines sequentially positioned on the liquid crystal display panel, and

the gate pulses are sequentially supplied to the first to fourth gate lines in order of the second, first, fourth, and third gate lines.

14. The method of claim 8, wherein the gate lines include first to third gate lines sequentially positioned on the liquid crystal display panel, and

the gate pulses are sequentially supplied to the first to third gate lines in order of the first, third, and second gate lines.

15. The method of claim 8, further comprising:

storing digital video data in a memory and transmitting the stored digital video data to the data drive circuit;

multiplying a frequency of an input timing signal, that has a frame frequency of 60 Hz as a base frequency, by 2;

raising a transmission frequency of the digital video data output from the memory based on the timing signal, whose the frequency is multiplied by 2; and

raising frequencies of the gate timing control signals to be suitable for a frame frequency of 120 Hz based on the timing signal, whose the frequency is multiplied by 2.

16. The method of claim 15, wherein the liquid crystal display panel displays an image in each frame period that is time-divided into a first half sub-frame period and a second half sub-frame period,

the first gate timing control signal is generated during the first half sub-frame period and includes a first scan direction control signal, that is maintained in a low logic state, for controlling the scan direction of the liquid crystal display panel in the sequential direction, and

the second gate timing control signal is generated during the second half sub-frame period and includes a second scan direction control signal, that is maintained in a high logic state, for controlling the scan direction of the liquid crystal display panel in the reverse sequential direction.

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公开(公告)号	US20090273553A1	公开(公告)日	2009-11-05
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摘要(译)

公开了一种液晶显示器及其驱动方法。液晶显示器包括：液晶显示面板，包括彼此交叉的数据线和栅极线；液晶单元；定时控制信号产生单元；数据驱动电路，向数据线提供数据电压；以及栅极驱动电路。定时控制信号产生单元产生用于在顺序方向上控制液晶显示面板的扫描方向的第一栅极定时控制信号和用于在反向顺序方向上控制扫描方向的第二栅极定时控制信号。栅极驱动电路向栅极线提供栅极脉冲，同时栅极脉冲的移位方向响应于第一和第二栅极时序控制信号而改变。

