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(54) **DRIVING CIRCUIT OF LIQUID CRYSTAL DISPLAY**

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(57) **ABSTRACT**

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Disclosed is a driving circuit of a liquid crystal display having a stable operation characteristic. The driving circuit comprises first and second transistors connected in series with each other between an output terminal of an (N-1)th circuit and a Vss terminal, a third transistor operated by a clock signal and having a drain for receiving an inversion signal of the clock signal and a source connected to an Nth gate line, a fourth transistor having a drain connected to the source of the third transistor and a source connected to the Vss terminal, fifth and sixth transistors connected in series with each other between a VDD terminal and the Vss terminal, a seventh transistor operated by an output signal of an (N+1)th circuit, an eighth transistor operated by an output signal of an (N+1)th circuit, a first capacitor formed at a front terminal of a gate of the third transistor, and a second capacitor formed between a gate and a drain of the sixth transistor.

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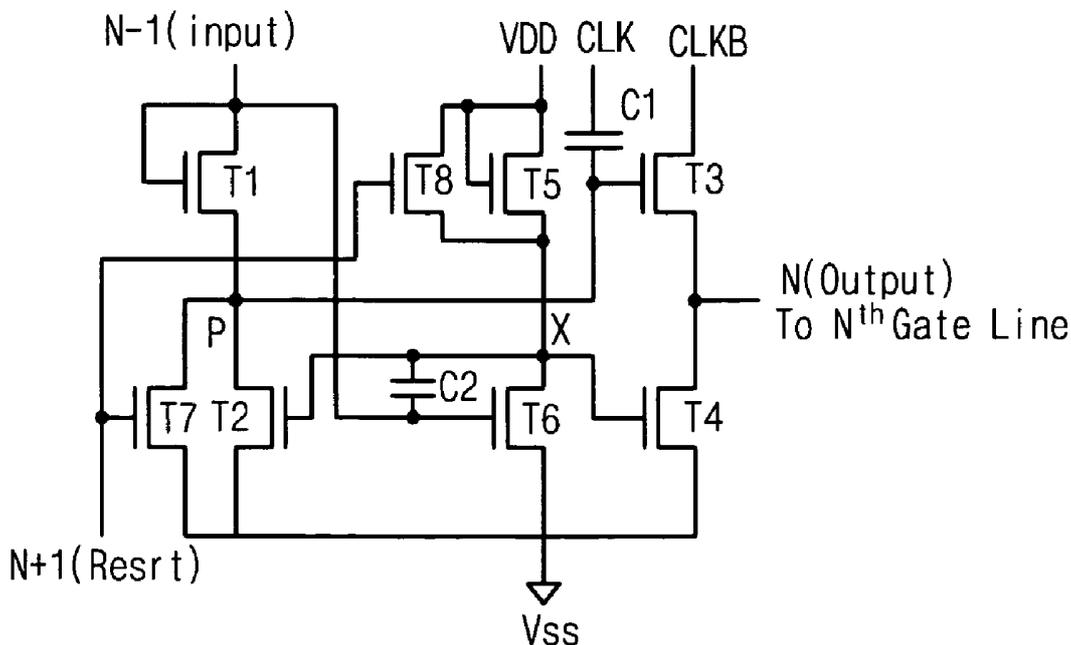


FIG. 1

(PRIOR ART)

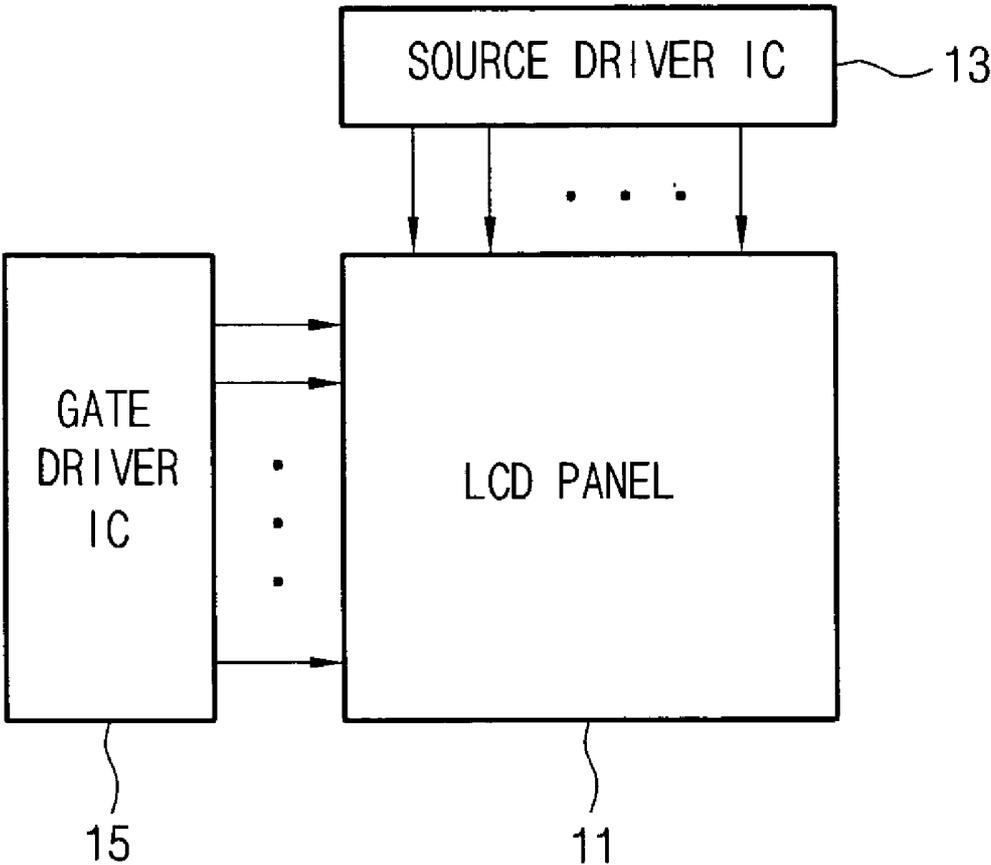


FIG. 2

(PRIOR ART)

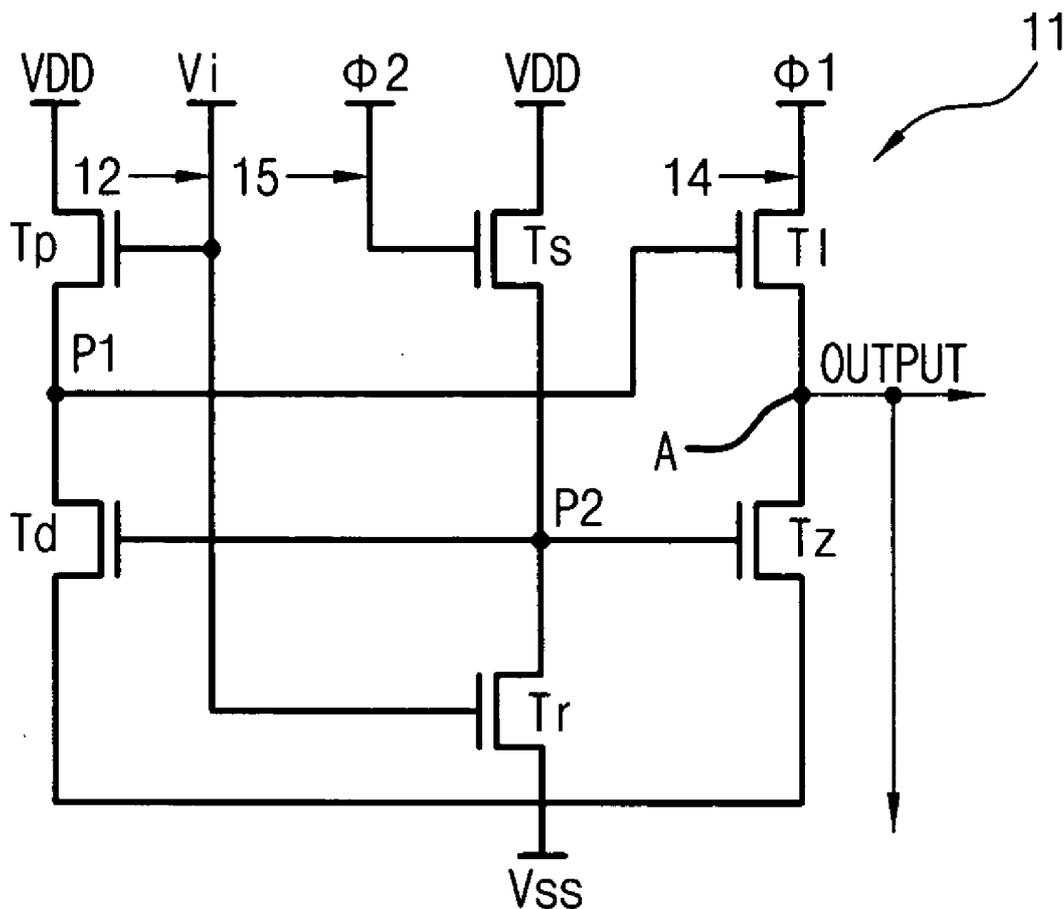


FIG. 3

(PRIOR ART)

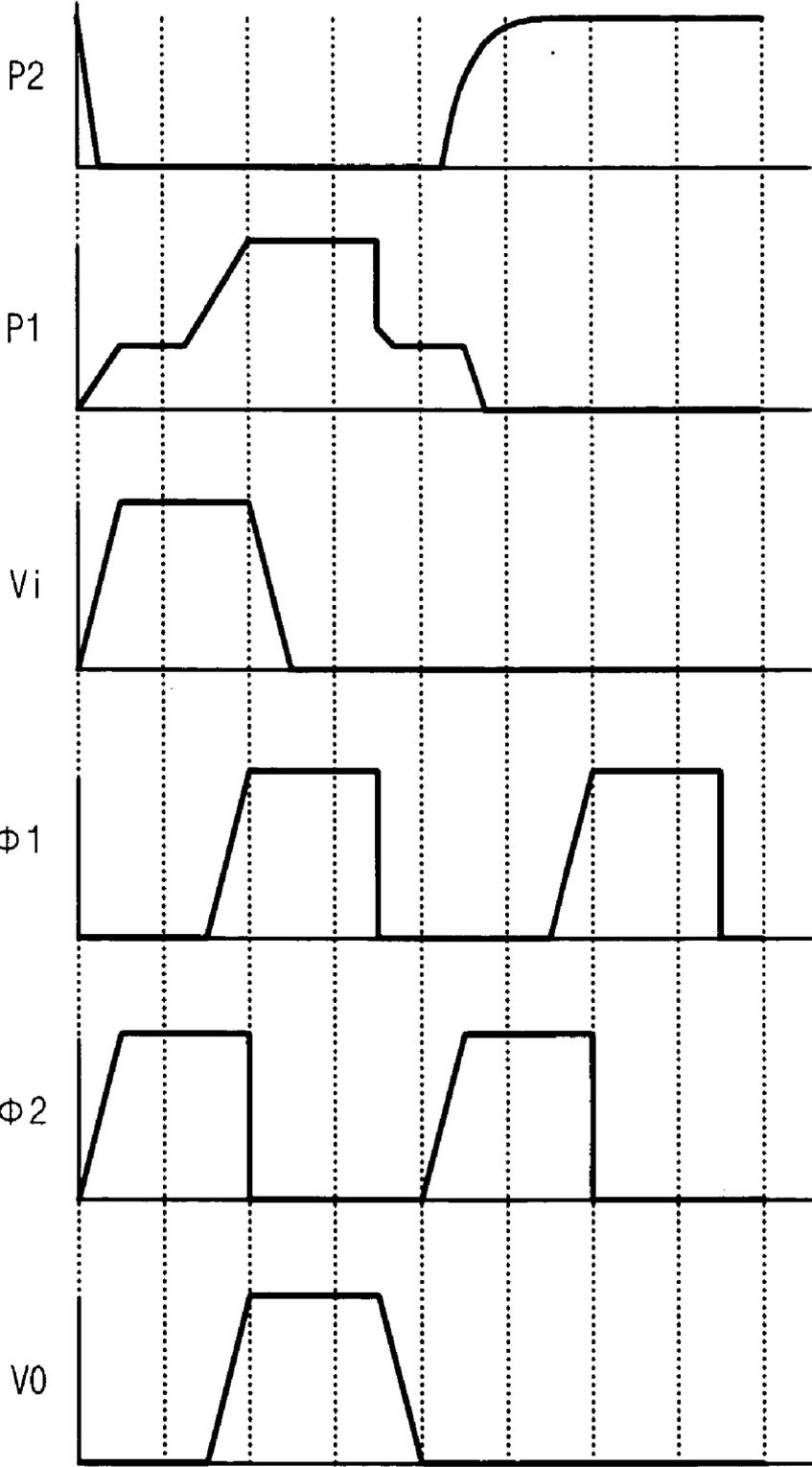


FIG. 4

(PRIOR ART)

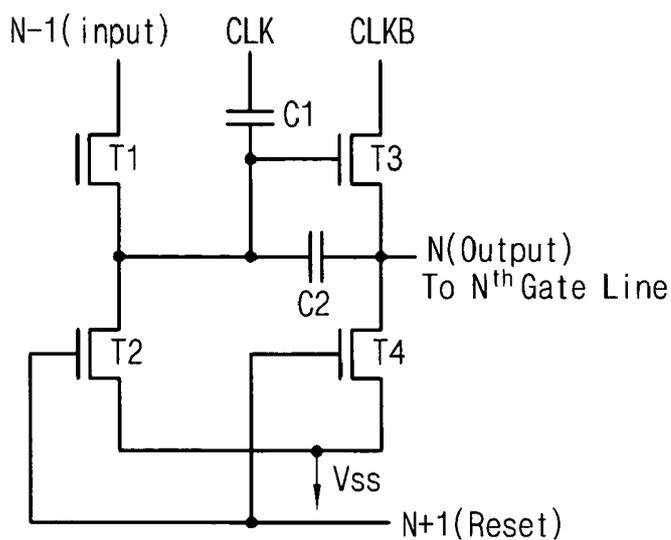


FIG. 5

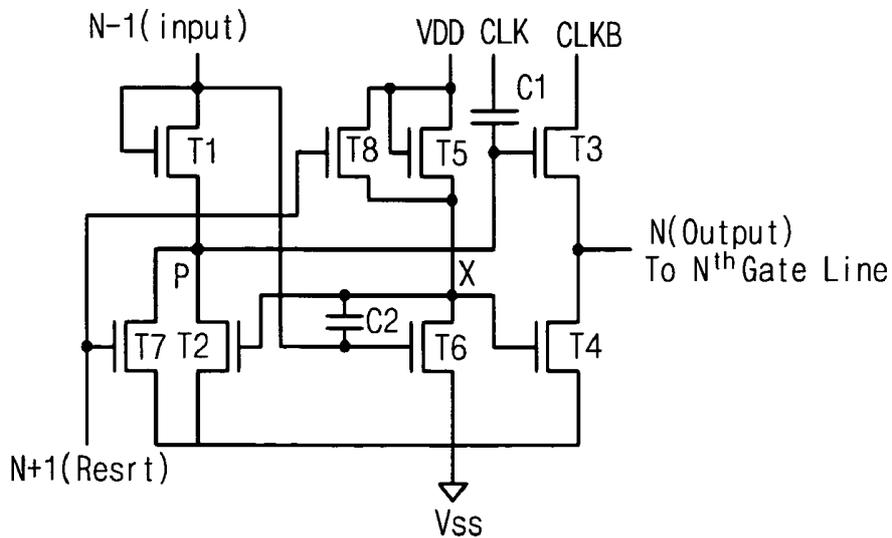


FIG.6A

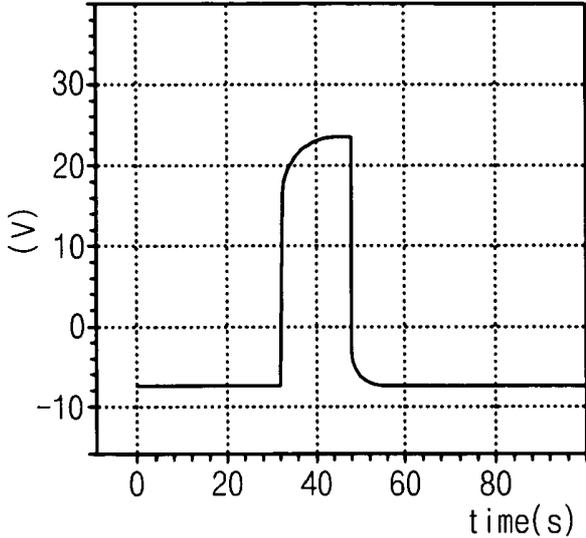
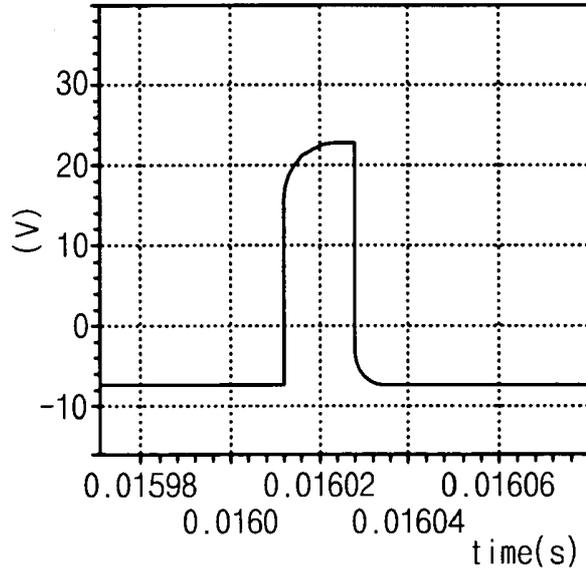


FIG.6B



DRIVING CIRCUIT OF LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the invention

[0002] The present invention relates to a driving circuit of a liquid crystal display, and more particularly to a driving circuit of a liquid crystal display in which the operation characteristic of the driving circuit is greatly improved by stabilizing an OFF level of an output signal and by significantly improving characteristic variation of a device resulting from DC voltage stress.

[0003] 2. Description of the Prior Art

[0004] As generally known in the art, CRTs (Cathode Ray Tubes), which are a kind of display device, have been mainly used as a monitor for various instrumentation devices, information terminals as well as televisions, etc., but they cannot sufficiently satisfy the demand for compact sizes and light weights of electronic devices, owing to the inherent weight and size of a CRT itself.

[0005] In order to replace a CRT, various liquid crystal displays having a lightweight, a slimmer thickness and a compact size, have been actively developed. Recently, such liquid crystal displays have been developed to an extent that they may serve as flat panel displays, so that the demand for liquid crystal displays have been greatly increased.

[0006] As shown in FIG. 1, a liquid crystal display includes a plurality of gate lines and a plurality of data lines which intersect each other. In addition, the liquid crystal display includes an LCD (Liquid Crystal Display) panel 11 having thin film transistors disposed at positions at which each gate line and each data line are intersected so as to display an image, a source driver IC 13 for applying a driving voltage to drive the data lines of the LCD panel 11, and a gate driver IC 15 for applying a driving voltage to drive the gate lines of the LCD panel 11.

[0007] Although it is not shown, the liquid crystal display includes peripheral circuits for providing various control signals to the source driver IC 13 and the gate driver IC 15, and such peripheral circuits include an LVDS section, a timing controller, etc.

[0008] Among such liquid crystal displays, an amorphous-silicon AMLCD (Active Matrix Liquid Crystal Display) has advantages of a reduced fabrication cost, compactness, and lightweight, in spite of low mobility and relatively high threshold voltage and parasitic capacitance, as compared with a polysilicon LCD in view of a driving circuit integration technique. Therefore, many researches of the amorphous-silicon AMLCD have been made. Recently, it becomes possible to construct an active matrix of a driving circuit only with amorphous-silicon TFTs, by means of new design technique and process.

[0009] In general, a gate line driving voltage is outputted from the gate driver IC, and the gate driver IC includes a shift register, a level shift, and a buffer. However, amorphous-silicon row driver must integrate the functions of these devices with only a shift register.

[0010] A shift register of a well-known amorphous-silicon row driver includes four to six transistors, in which the transistors must be designed in mutually different sizes.

[0011] Hereinafter, a driving circuit of the conventional liquid crystal display will be described with reference to the accompanying drawings.

[0012] FIG. 2 is a view showing a first conventional driving circuit of a liquid crystal display in which a shift register includes six transistors, and FIG. 3 is a timing view for showing operations of the circuit shown in FIG. 2.

[0013] First, a driving circuit of the conventional liquid crystal display includes six thin film transistors T_p , T_d , T_s , T_r , T_1 , and T_z . In the driving circuit of the liquid crystal display, since an input signal has a high level at T_0 , a node P2 has a high level, so that a thin film transistor T_z is turned on. At this time, a point A of an output side is biased to a low level by means of a V_{ss} voltage.

[0014] Then, when both of an input signal V_i and a clock signal Φ_2 have a high level, the thin film transistors T_p , T_r , and T_s are simultaneously turned on. At this time, a node P1 becomes positive and has a voltage value obtained by subtracting a threshold voltage of the thin film transistor T_p from a V_{DD} voltage.

[0015] Meanwhile, the node P2 becomes a low level owing to a powerful turning on of the thin film transistor T_r . For reference, the thin film transistor T_r has a size larger than a size of the thin film transistor T_s by ten times.

[0016] When the node P2 is shifted into a low level, the thin film transistor T_z is turned off, but the output is still maintained at a low level. The reason is that a clock signal Φ_1 has a low level.

[0017] Meanwhile, when the clock signal Φ_1 is shifted into a high level, the thin film transistor T_1 becomes a precharged high state, and the voltage of the node P1 becomes approximately 90% of $(V_{DD}-V_{th})+\Phi_1$. At this time, since an output voltage V_o follows the pulse of the clock signal Φ_1 , the output voltage V_o is turned on, so that a shift register function applying a high-level voltage as an input to the next-stage circuit is performed.

[0018] In addition, when the clock signal Φ_2 becomes a high level, the node P2 becomes a high level and the thin film transistor T_z is turned on, so that the point A of the output side becomes a low level.

[0019] Meanwhile, FIG. 4 is a view showing a second conventional driving circuit of a liquid crystal display in which the second conventional driving circuit includes four thin film transistors and two capacitors C1 and C2, unlike the first conventional driving circuit of FIG. 2 including six thin film transistors.

[0020] The operation principle of the driving circuit of a liquid crystal display shown in FIG. 4 is similar to that of the above-mentioned first conventional driving circuit including six thin film transistors, but differs in that a reset signal is applied by receiving an output signal of the next stage.

[0021] However, the conventional driving circuits of a liquid crystal display have problems as follows.

[0022] First, in the case of the first conventional driving circuit including six thin film transistors, since the thin film transistors T_d and T_z for resetting use continuous clock signals as their gate voltages, the thin film transistors T_d and T_z sequentially receive DC stress due to high-level voltages

of the clock signals, so that when the driving circuit is driven for a long time, characteristic variation of the thin film transistors, such as variation of the threshold voltage, may occur, thereby causing a malfunction of the circuit.

[0023] Also, in the case of the second conventional driving circuit including four thin film transistors and two capacitors, a thin film transistor T4, which performs a reset function by an output signal of the next stage, enters an ON state for only one scan period of time but enters a floating state for rest of the time period of the frame. Consequently, a capacitive coupling is created by a voltage of an image signal applied through the data line, thereby causing a fluctuation phenomenon according to variation of electric potential of an image signal without having a V_{goff} characteristic requiring a constant voltage for a predetermined period of time. Such a phenomenon causes an image flickering when the panel is subject to a line inversion drive, thereby significantly deteriorating the quality of the image.

SUMMARY OF THE INVENTION

[0024] Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a driving circuit of a liquid crystal display having a stable operation characteristic, by improving the V_{goff} characteristic which is unstable in a conventional driving circuit including four thin film transistors and two capacitors and by minimizing the characteristic variation of the thin film transistors caused by DC stress which occurs in a conventional driving circuit including six thin film transistors.

[0025] In order to accomplish this object, there is provided a driving circuit of a liquid crystal display, the driving circuit comprising: first and second transistors connected in series with each other between an output terminal of an $(N-1)^{th}$ circuit and a Vss terminal; a third transistor operated by a clock signal, and having a drain for receiving an inversion signal of the clock signal and a source connected to an N^{th} gate line; a fourth transistor having a drain connected to the source of the third transistor and a source connected to the Vss terminal; fifth and sixth transistors connected in series with each other between a VDD terminal and the Vss terminal; a seventh transistor operated by an output signal of an $(N+1)^{th}$ circuit, and having a drain and a source connected to a drain and a source of the second transistor, respectively; an eighth transistor operated by an output signal of an $(N+1)^{th}$ circuit, and having a drain and a source connected to a drain and a source of the fifth transistor, respectively; a first capacitor formed at a front terminal of a gate of the third transistor; and a second capacitor formed between a gate and a drain of the sixth transistor.

[0026] Herein, operation states of the first and sixth transistors are determined according to an output signal of the $(N-1)^{th}$ circuit, operation states of the seventh and eighth transistors are determined according to an output signal of the $(N+1)^{th}$ circuit, operation states of the third transistor are determined according to the clock signal, operation states of the second and fourth transistors are determined according to a drain voltage of the sixth transistor, and operation states of the fifth transistor are determined according to a VDD voltage.

[0027] In addition, the VDD voltage has a voltage range for allowing gate-source voltages larger than threshold volt-

ages of the second, fourth, and fifth transistors to be applied to the second, fourth, and fifth transistors.

[0028] In addition, the seventh transistor is a reset transistor, which is operated by an output signal of the $(N+1)^{th}$ circuit, and the eighth transistor is a transistor for transferring the VDD voltage, which is operated by the output signal of the $(N+1)^{th}$ circuit.

[0029] In addition, the first capacitor stabilizes an OFF characteristic of a signal outputted to an N^{th} gate line, and the second capacitor stabilizes a level of a drain voltage of the sixth transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0031] FIG. 1 is a view showing a construction of a conventional liquid crystal display;

[0032] FIG. 2 is a view showing a construction of a conventional driving circuit of a liquid crystal display including six thin film transistors;

[0033] FIG. 3 is a timing view for showing operations of the circuit shown in FIG. 2;

[0034] FIG. 4 is a view showing a construction of a conventional driving circuit of a liquid crystal display including four thin film transistors and two capacitors;

[0035] FIG. 5 is a view showing a construction of a driving circuit of a liquid crystal display according to one embodiment of the present invention; and

[0036] FIGS. 6A and 6B are views showing simulation waveforms of the driving circuit of the liquid crystal display according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] Hereinafter, a preferred embodiment of the present invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description on the same or similar components will be omitted.

[0038] FIG. 5 is a driving circuit of a liquid crystal display according to one embodiment of the present invention.

[0039] Referring to FIG. 5, a driving circuit of a liquid crystal display according to the present invention includes eight thin film transistors T1, T2, T3, T4, T5, T6, T7, and T8 and two capacitors C1 and C2.

[0040] As shown in FIG. 5, the gate terminal and the drain terminal of the first transistor T1 are connected together to an $(N-1)^{th}$ gate line, the second transistor T2 is connected between the source of the first transistor T1 and a Vss terminal. In addition, the third transistor T3 operated by a clock signal CLK is connected with the fourth transistor T4 in series, in which the source terminal of the fourth transistor T4 is connected to the Vss terminal. Herein, a contact point between the source terminal of the third transistor T3 and the drain terminal of the fourth transistor T4 is an output

terminal N, and a voltage outputted through the output terminal is applied to an Nth gate line. Also, an inverted clock signal CLKB signal is applied to the drain terminal of the third transistor T3.

[0041] Meanwhile, the fifth transistor T5 and the sixth transistor T6 are connected in series with each other between a VDD terminal and the Vss terminal. The seventh transistor T7 and the eighth transistor T8, operation states of which are determined by a reset signal, connected in parallel with each other.

[0042] In addition, a VDD voltage is applied to the drain terminal of the eighth transistor T8 whose operation state is determined by the reset signal. The drain terminal of the eighth transistor T8 and the gate terminal of the fifth transistor T5 are connected together to the VDD terminal.

[0043] Meanwhile, the first capacitor C1 is connected to the gate terminal of the third transistor T3. That is, one electrode of the first capacitor C1 is connected so as to receive the clock signal, and the other electrode of the first capacitor C1 is connected to the gate terminal of the third transistor T3.

[0044] The gate terminal of the second transistor T2 is connected to both of the drain terminal of the sixth transistor T6 and the gate terminal of the fourth transistor T4. One electrode of the second capacitor C2 is connected to the drain terminal of the sixth transistor T6, and the other electrode of the second capacitor C2 is connected to both of the drain terminal of the first transistor T1 and the gate terminal of the sixth transistor T6.

[0045] In the following description, the operation of the above-mentioned driving circuit of the liquid crystal display according to the present invention will be described.

[0046] As shown in FIG. 5, the driving circuit of the liquid crystal display according to the present invention includes eight transistors and two capacitors, in which the respective thin film transistors have different sizes and different functions from each other.

[0047] According to the operation sequence of the driving circuit, first, an output signal of an (N-1)th circuit (not shown) is inputted through the drain terminal of the first transistor T1.

[0048] When the output signal of the (N-1)th circuit (not shown), which is an input signal from the viewpoint of an Nth circuit in the present driving circuit, is inputted through the drain terminal of the first transistor T1, the clock signal CLK is also inputted in synchronization with the input signal.

[0049] At this time, if the input signal has a high level, the first transistor T1 and the sixth transistor T6 are turned on, and a node P becomes a positive level and has an electric potential obtained by subtracting the threshold voltage of the first transistor T1 from the VDD voltage. At this time, a DC voltage of the VDD, which is a voltage higher than a Vss voltage by a few volts, is continuously applied through the fifth transistor T5, and simultaneously, a node X enters a low level owing to a powerful turning on of the sixth transistor T6. For reference, the sixth transistor T6 has a larger size than the fifth transistor T5 by about ten times or more.

[0050] Since the node X has a low level, the fourth transistor T4 is in an OFF state, but the output terminal N is still maintained because the inverted clock signal CLKB is at a low level.

[0051] Meanwhile, when an output signal of an (N+1)th circuit is applied to the seventh transistor T7 and the eighth transistor T8 as a reset signal, seventh and eighth transistors T7 and T8 causes decay of the node P together with the second transistor T2. At this time, the eighth transistor T8 is arranged to improve the reset function since the turning on voltage of the fifth transistor T5 is relatively low.

[0052] Herein, the capacitance of the second capacitor C2 is decided so as to function to stabilize the level of the electric potential of the node X, and the capacitance of the first capacitor C1 is decided so as to function to stabilize the OFF level characteristic of the output signal.

[0053] With the driving circuit of the liquid crystal display according to the present invention as described above, owing to the continuously applied VDD voltage, which is a voltage that is higher than the Vss voltage by a few volts, the gate-source voltages Vgs of the fourth transistor T4 is driven at a relatively lower voltage as compared with the conventional art.

[0054] Referring to the construction of the above-mentioned circuit, an output signal of the (N-1)th circuit, which is an input signal from the viewpoint of the present circuit, not only is inputted only simultaneously both the gate terminal and the drain terminal of the first transistor T1 so that the first transistor T1 may function as a diode, but also is inputted to the gate terminal of the sixth transistor T6.

[0055] The source terminal of the first transistor T1 is connected to both of the drain terminal of the second transistor T2, which is a reset transistor, and the gate terminal of the third transistor T3, which is a driving transistor. In addition, the source terminals of the second transistor T2, the fourth transistor T4, and the sixth transistor T6 are together connected to the Vss terminal.

[0056] The inverted clock signal CLKB is applied to the drain terminal of the third transistor T3, which is a driving transistor. The source electrode of the third transistor T3 is connected to the drain electrode of the fourth transistor T4, and outputs a signal for switching the drive of a gate line.

[0057] For reference, FIGS. 6A and 6B are views showing simulation waveforms of the driving circuit of the liquid crystal display according to the present invention.

[0058] As described above, the driving circuit of the liquid crystal display of the present invention can realize a stable shift register circuit, by improving not only an image flicker phenomenon caused by an unstable OFF voltage, which is a problem in a conventional driving circuit of a liquid crystal display including four thin film transistors and two capacitors, but also a malfunction problem of a circuit resulting from characteristic variation of thin film transistors caused by DC voltage stress continuously applied to reset transistors, which are problems in another conventional driving circuit of a liquid crystal display including six thin film transistors.

[0059] Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. A driving circuit of a liquid crystal display, the driving circuit comprising:

first and second transistors connected in series with each other between an output terminal of an $(N-1)^{\text{th}}$ circuit and a Vss terminal;

a third transistor operated by a clock signal, and having a drain for receiving an inversion signal of the clock signal and a source connected to an N^{th} gate line;

a fourth transistor having a drain connected to the source of the third transistor and a source connected to the Vss terminal;

fifth and sixth transistors connected in series with each other between a VDD terminal and the Vss terminal;

a seventh transistor operated by an output signal of an $(N+1)^{\text{th}}$ circuit, and having a drain and a source connected to a drain and a source of the second transistor, respectively;

an eighth transistor operated by an output signal of an $(N+1)^{\text{th}}$ circuit, and having a drain and a source connected to a drain and a source of the fifth transistor, respectively;

a first capacitor formed at a front terminal of a gate of the third transistor; and

a second capacitor formed between a gate and a drain of the sixth transistor.

2. The driving circuit as claimed in claim 1, wherein, operation states of the first and sixth transistors are determined according to an output signal of the $(N-1)^{\text{th}}$ circuit, operation states of the seventh and eighth transistors are determined according to an output signal of the $(N+1)^{\text{th}}$ circuit, operation states of the third transistor are determined according to the clock signal, operation states of the second and fourth transistors are determined according to a drain voltage of the sixth transistor, and operation states of the fifth transistor are determined according to a VDD voltage.

3. The driving circuit as claimed in claim 2, wherein, the VDD voltage has a voltage range for allowing gate-source voltages larger than threshold voltages of the second, fourth, and fifth transistors to be applied to the second, fourth, and fifth transistors.

4. The driving circuit as claimed in claim 1, wherein, the seventh transistor is a reset transistor, which is operated by an output signal of the $(N+1)^{\text{th}}$ circuit, and the eighth transistor is a transistor for transferring the VDD voltage, which is operated by the output signal of the $(N+1)^{\text{th}}$ circuit.

5. The driving circuit as claimed in claim 1, wherein, the first capacitor stabilizes an OFF characteristic of a signal outputted to an N^{th} gate line, and the second capacitor stabilizes a level of a drain voltage of the sixth transistor.

* * * * *

专利名称(译)	液晶显示器的驱动电路		
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申请号	US11/013051	申请日	2004-12-15
[标]申请(专利权)人(译)	AHN SEONGJ KIM CHEON ^ h YOO SEJ		
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[标]发明人	AHN SEONG JUN KIM CHEON HONG YOO SE JONG		
发明人	AHN, SEONG JUN KIM, CHEON HONG YOO, SE JONG		
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优先权	1020030100226 2003-12-30 KR		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种具有稳定操作特性的液晶显示器的驱动电路。驱动电路包括在第 (N-1) 电路的输出端和Vss端之间彼此串联连接的第一和第二晶体管，由时钟信号操作的第三晶体管，并具有用于接收反相信号的漏极。时钟信号和连接到第N栅极线的源极，第四晶体管，其漏极连接到第三晶体管的源极，源极连接到Vss端子，第五和第六晶体管在VDD端子之间彼此串联连接Vss端子，由第 (N + 1) 电路的输出信号操作的第七晶体管，由第 (N + 1) 电路的输出信号操作的第八晶体管，形成在第一电容器的前端子处的第一电容器第三晶体管的栅极，以及形成在第六晶体管的栅极和漏极之间的第二电容器。

