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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0011556 A1****Morita**(43) **Pub. Date:****Jan. 16, 2003**(54) **LINE DRIVE CIRCUIT, ELECTRO-OPTIC DEVICE, AND DISPLAY DEVICE**(52) **U.S. Cl.** **345/98**(76) **Inventor:** Akira Morita, Suwa-shi (JP)(57) **ABSTRACT**

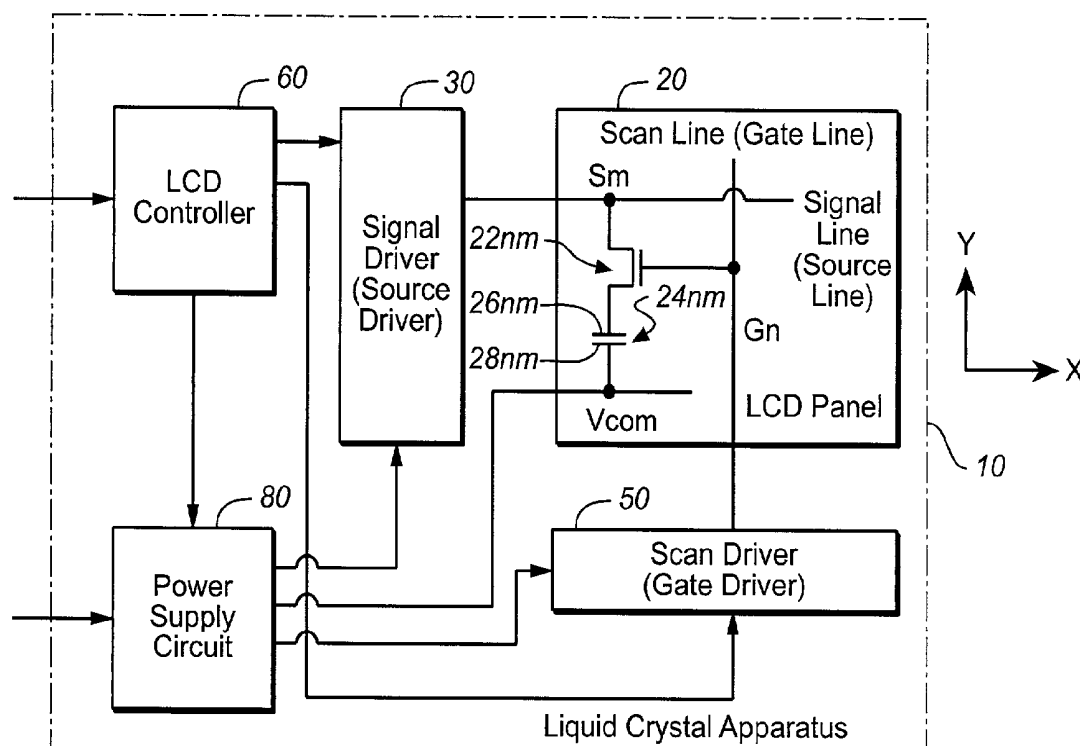
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SAN JOSE, CA 95134 (US)**(21) **Appl. No.:** 10/170,967(22) **Filed:** Jun. 13, 2002(30) **Foreign Application Priority Data**

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A line driver circuit, an electro-optic device, and a display apparatus efficiently reduce cost by reducing process dimensions and effectively shorten display panel development turn-around time by simplifying the reconfiguration of output voltages. The liquid crystal apparatus **10** has an LCD panel **20**, a signal driver **30**, a scan driver **50**, and a power supply circuit **80**, each of which is controlled by an LCD controller **60**. Signal driver **30** contains an interface unit **200** for converting a first voltage specified for a low voltage process to a second voltage specified for a high voltage process. The interface circuitry within interface unit **200** is made up of devices using a medium voltage process. Interface unit **200** receives and converts low voltage signals (i.e. first voltage level) supplied from LCD controller **60** to high voltage signals (i.e. second voltage level), and supplies the level-shifted voltage signal to scan driver **50** or power supply circuit **80**.



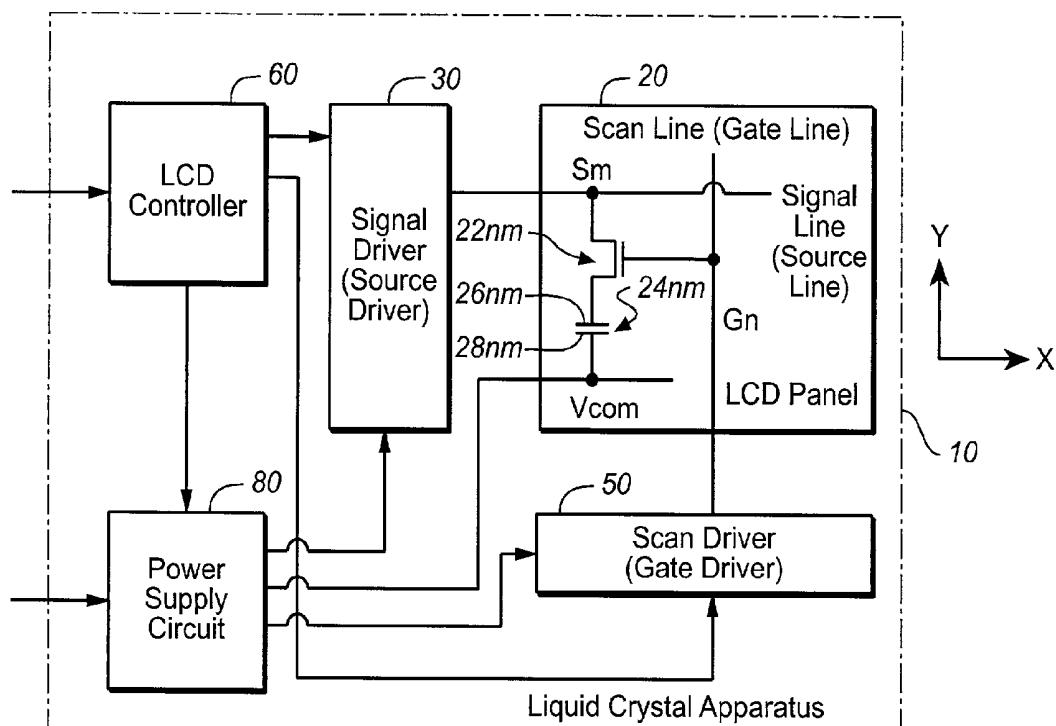


FIG._1

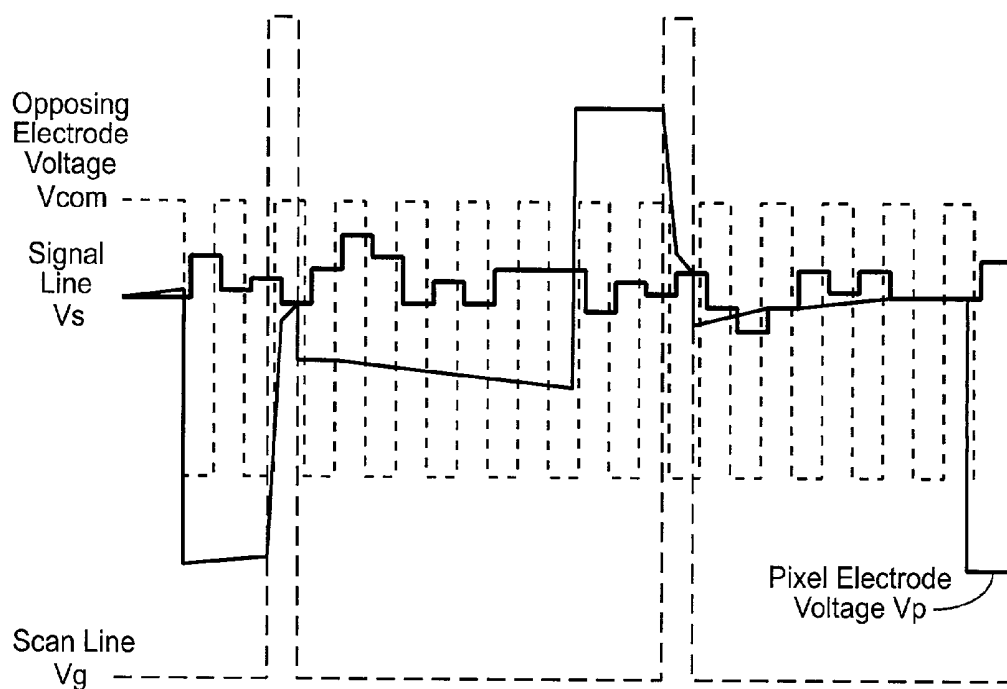


FIG._2

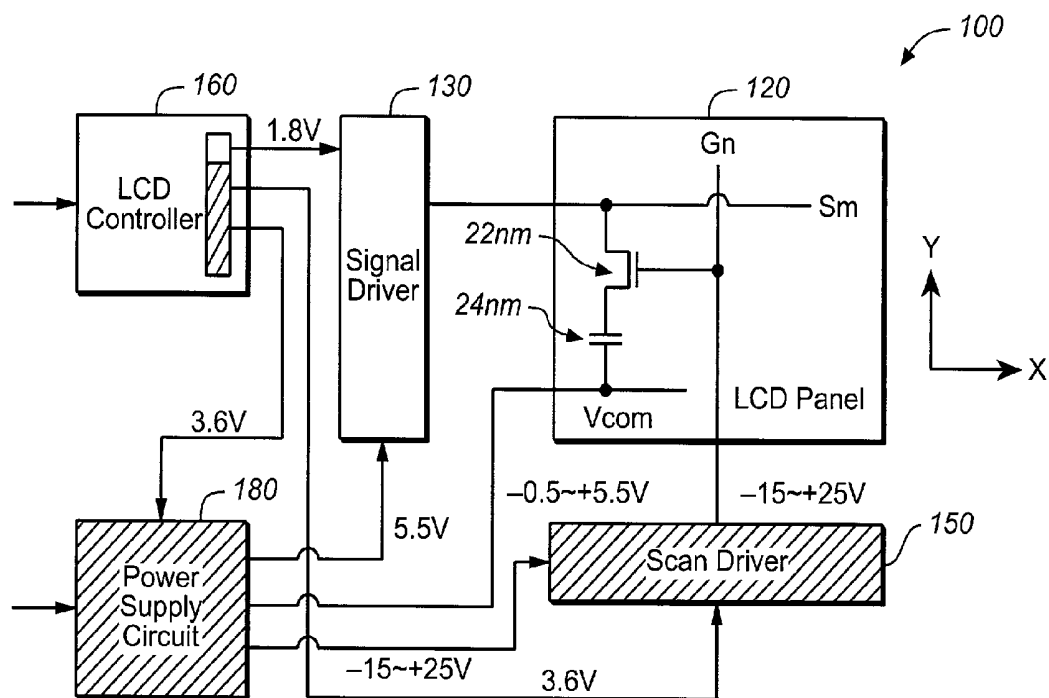


FIG._3

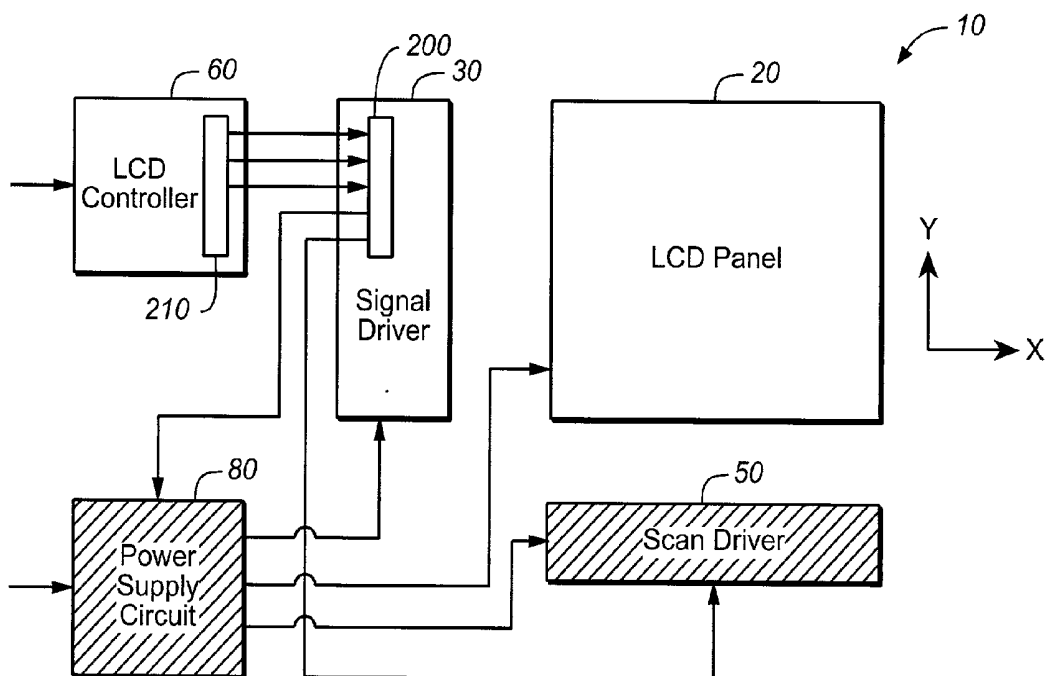


FIG._4

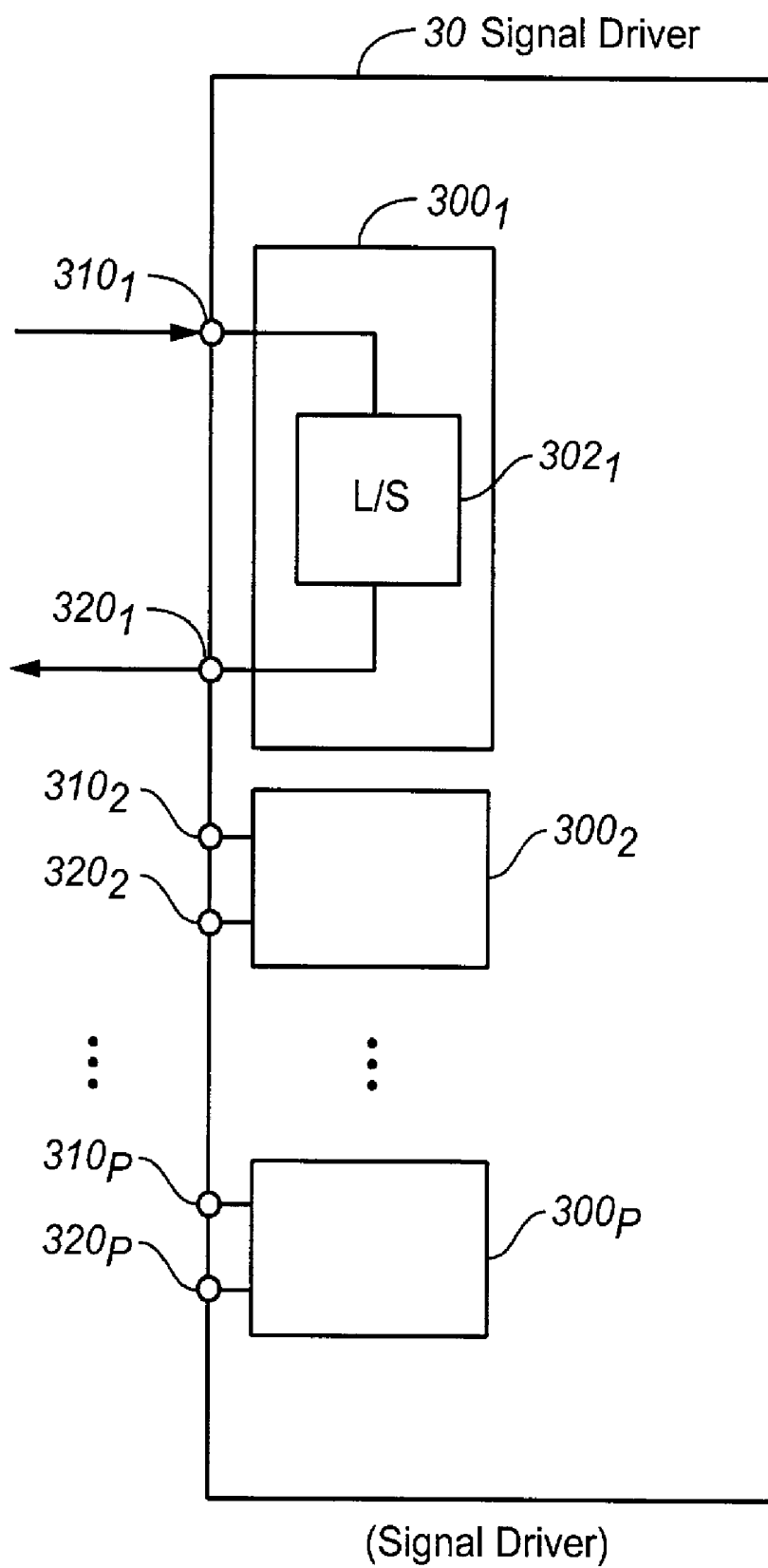


FIG. 5

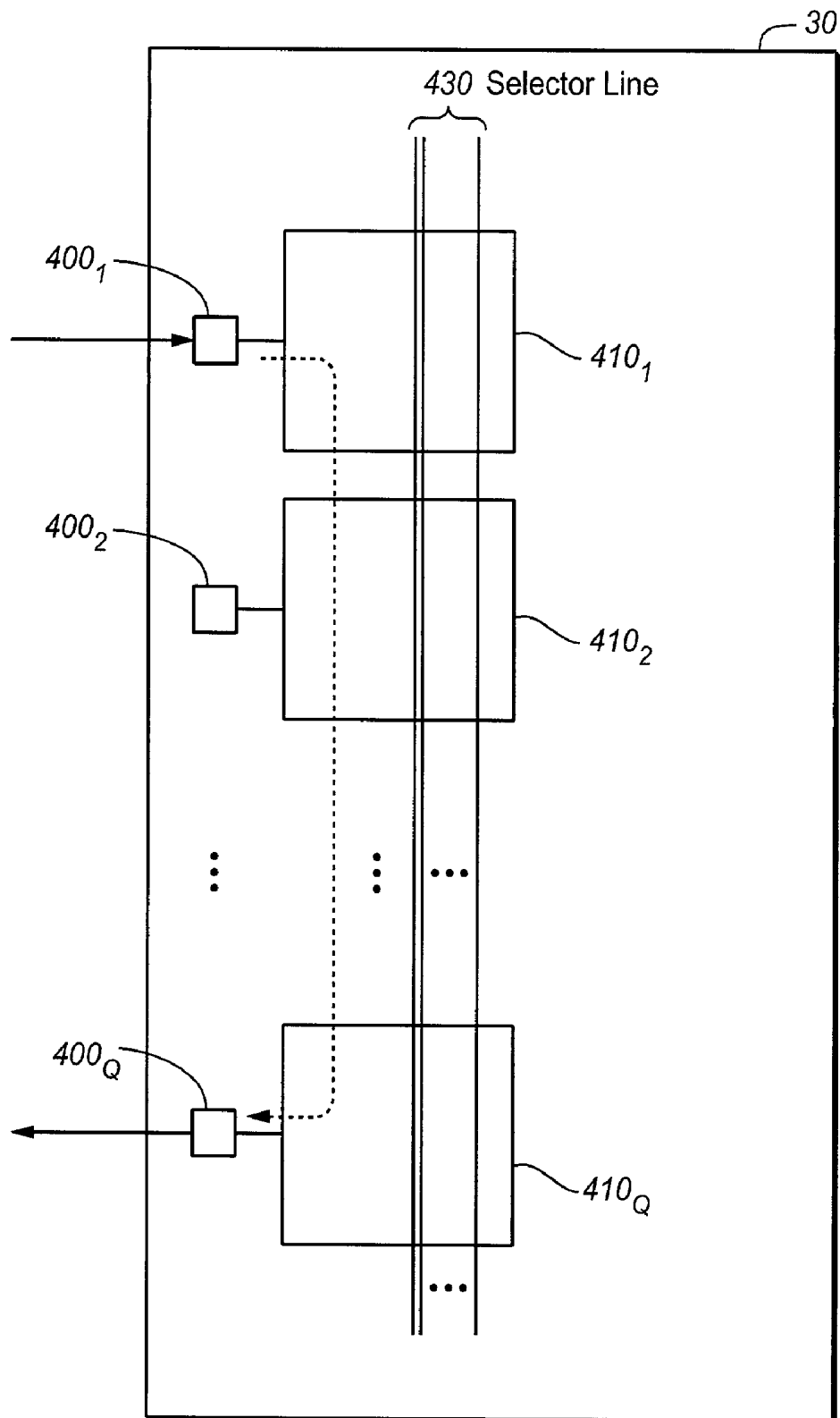


FIG. 6

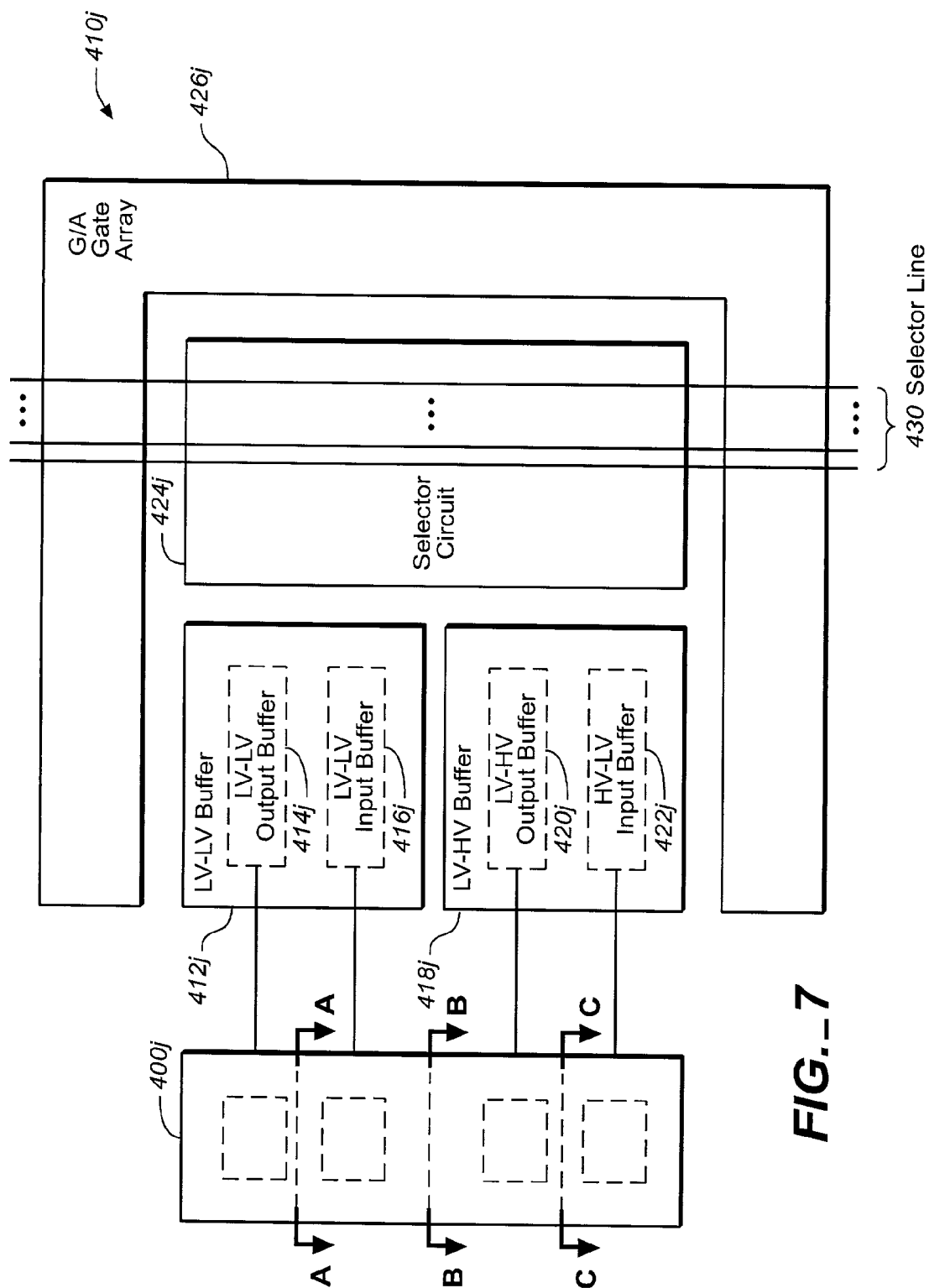


FIG. 7

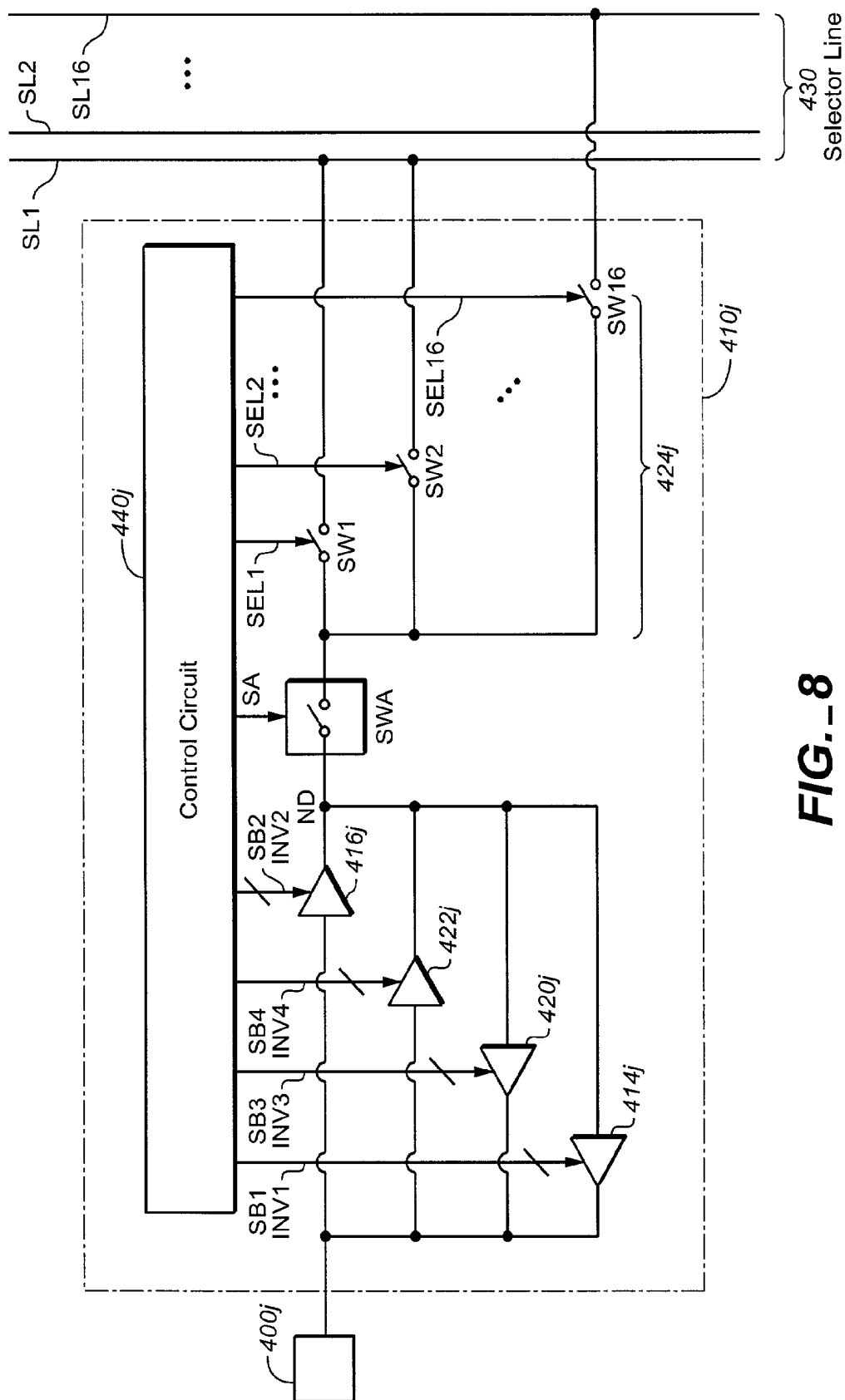


FIG. 8

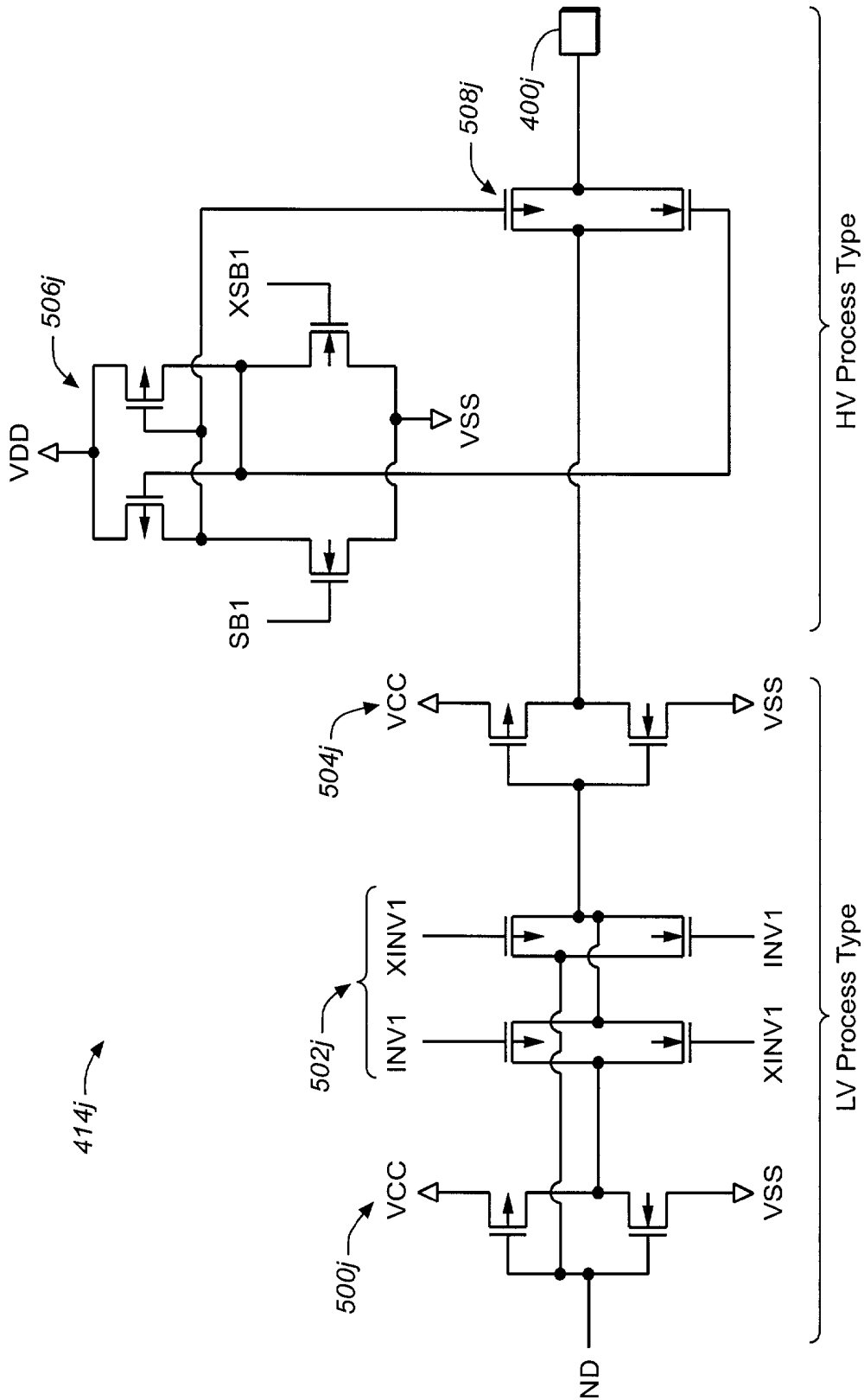


FIG. 9

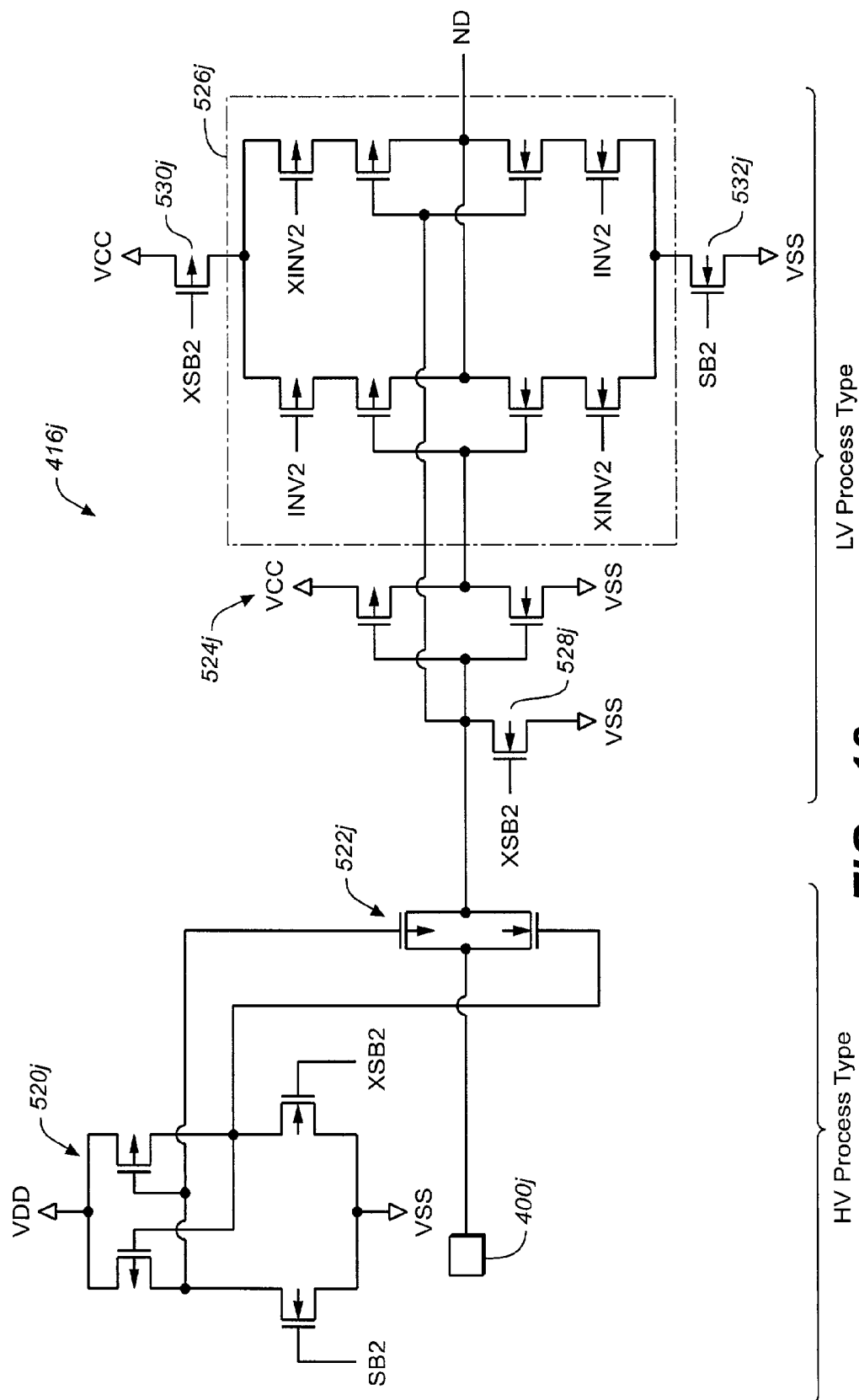


FIG. 10

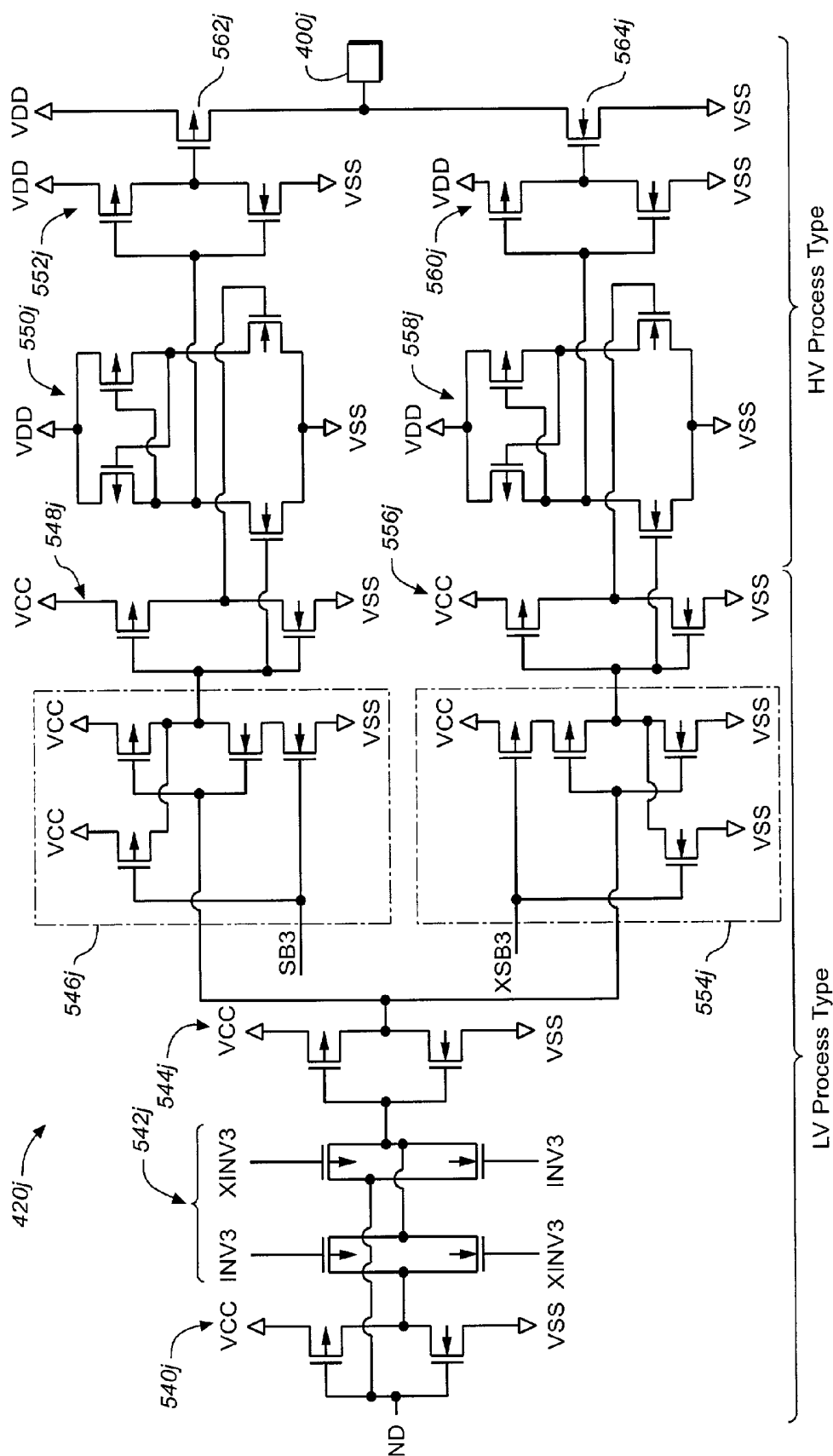


FIG. 11

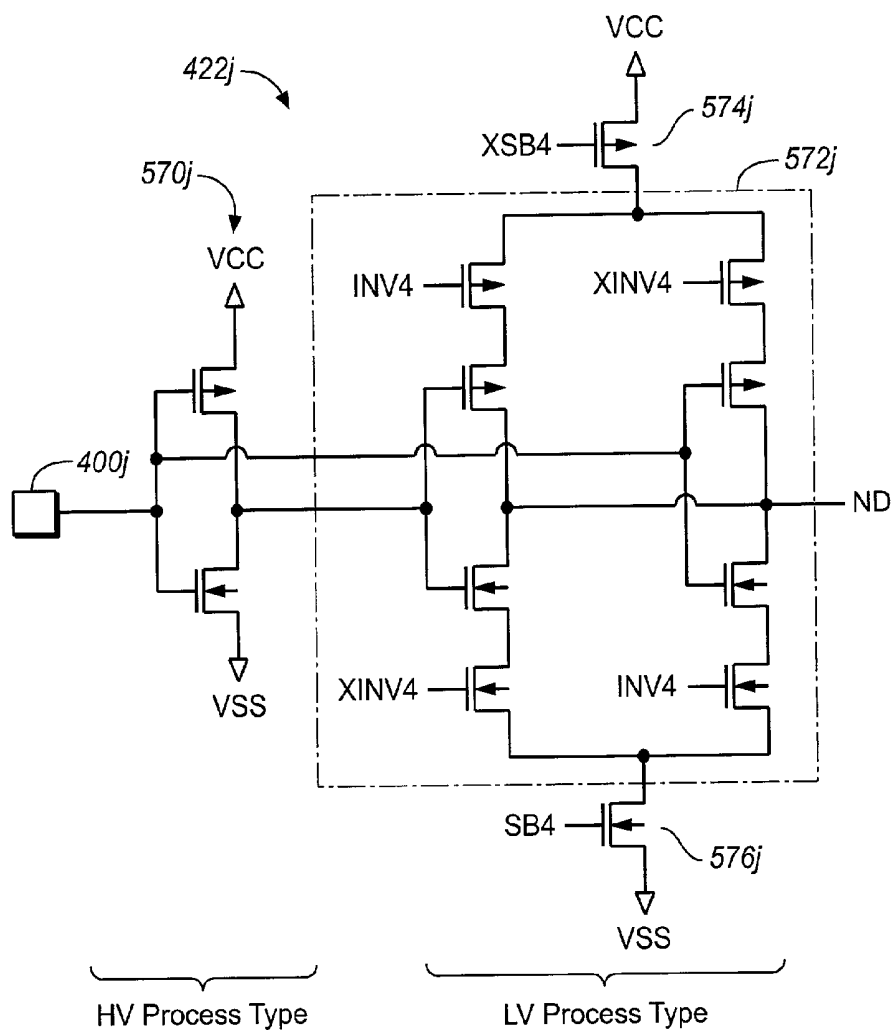


FIG. 12

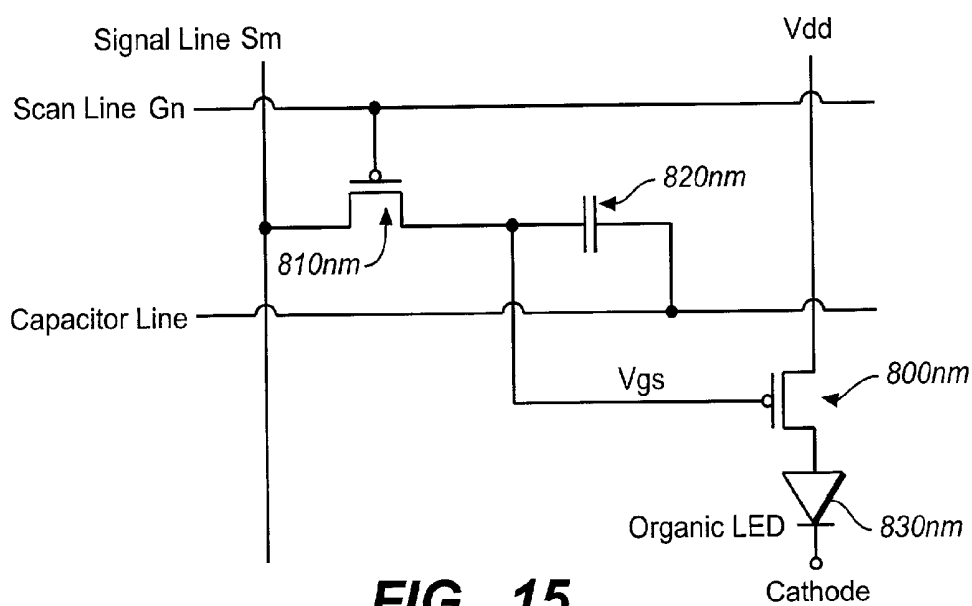


FIG. 15

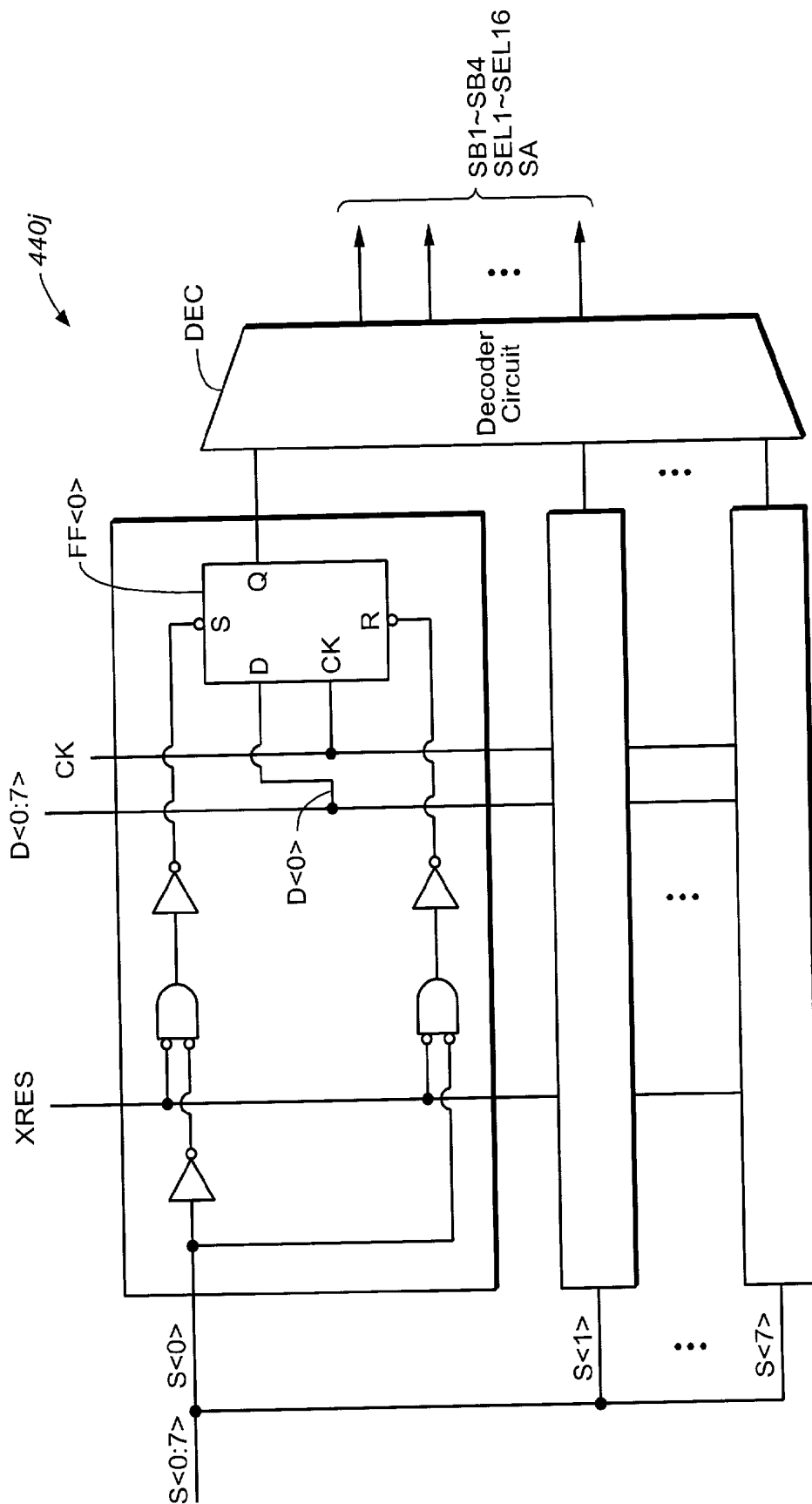


FIG. 13

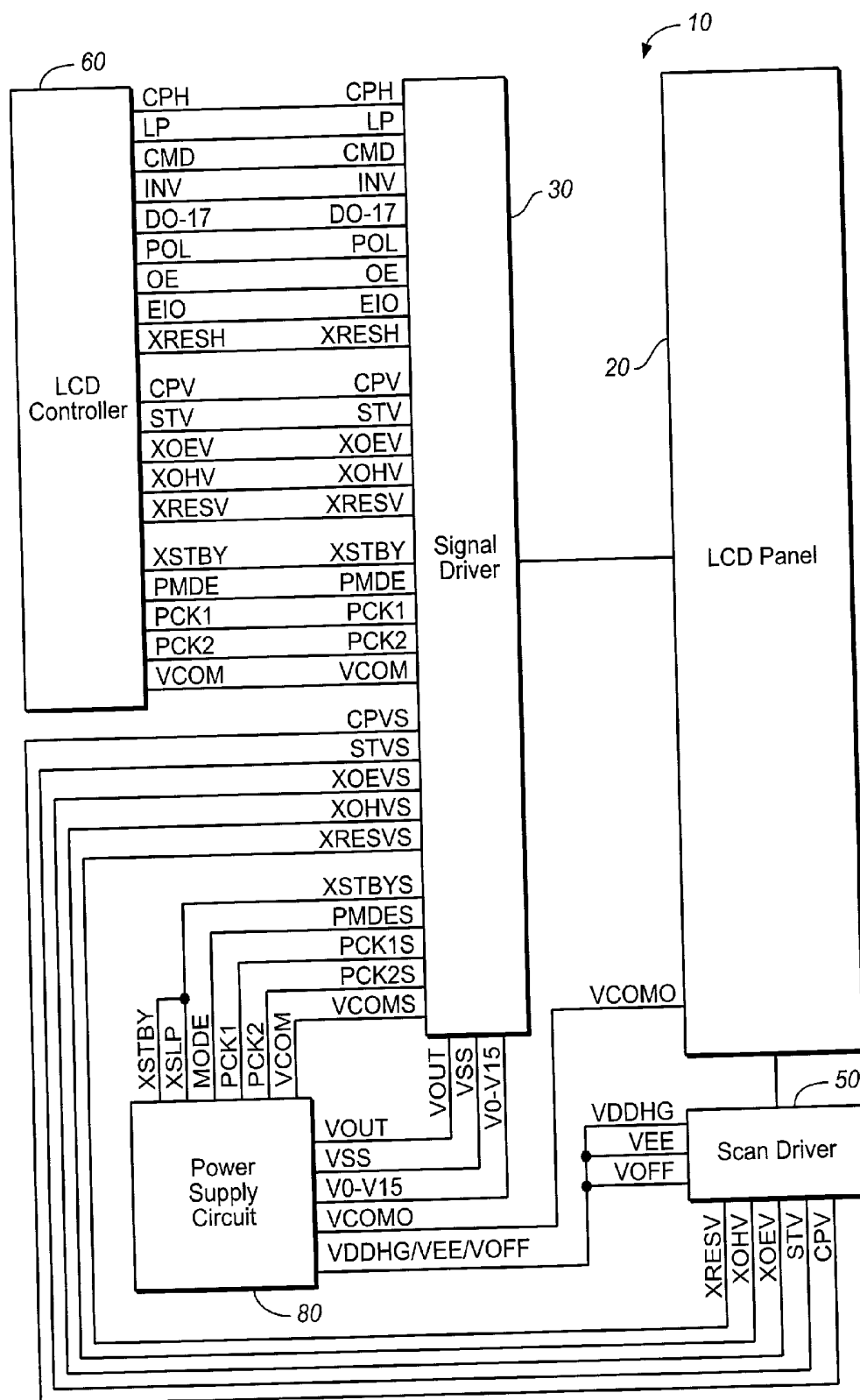


FIG. 14

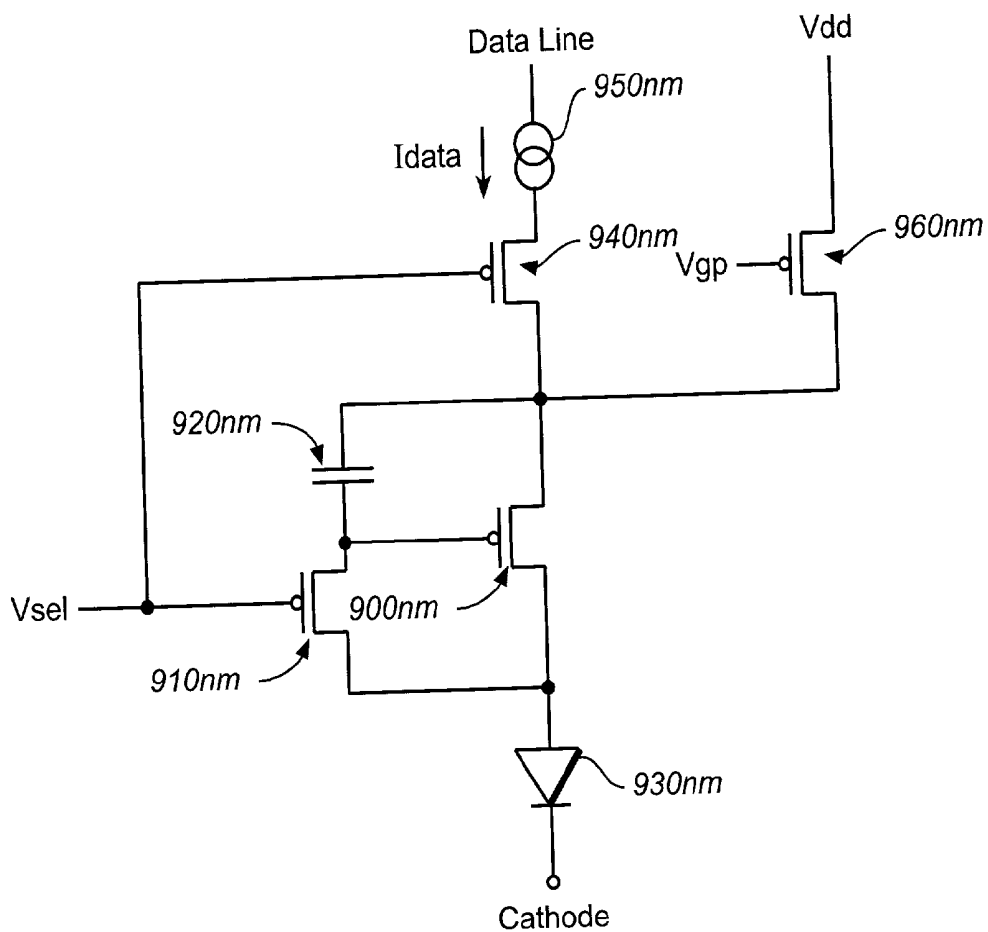


FIG. 16A

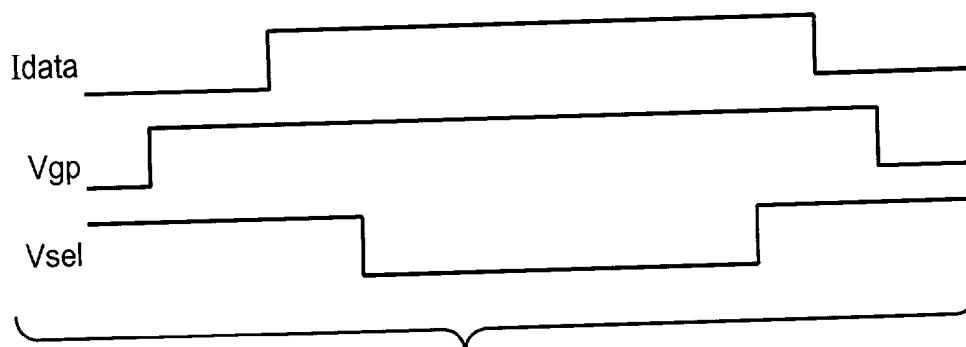


FIG. 16B

LINE DRIVE CIRCUIT, ELECTRO-OPTIC DEVICE, AND DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a line driver circuit, and to an electro-optic device and a display device using the same.

[0003] 2. Description of Related Art

[0004] Display panels, such as liquid crystal displays, are used as display units in electronic devices, such as cell phones for example, in an effort to achieve low power consumption and reduce the size and weight of the electronic devices. Since delivering video and still images with high content value has become possible with the rapid spread and acceptance of cell phones in recent years, high image quality has also become necessary for display panels in cell phones, and other devices used to deliver video/image contents.

[0005] Active matrix liquid crystal panels using thin film transistor ("TFT" below) liquid crystals are known as one type of liquid crystal panel achieving high image quality in the display unit of such electronic devices. Organic EL panels using organic EL elements are another type.

[0006] In an active matrix liquid crystal panel using TFT liquid crystals, a high voltage is required for driving the display, the value of the high voltage being dependent upon the liquid crystal material and TFT transistor capacity. As a result, the driver circuit (line driver circuit) and power supply circuit for driving an active matrix, LCD panel display, must be manufactured using a high breakdown voltage process.

[0007] There is therefore a problem that even as device geometry processes continues to get smaller, the benefits of low cost offered by reduced dimensions cannot be realized in LCD panel drivers.

OBJECT OF THE INVENTION

[0008] The present invention is directed toward solving the technical problems described above.

[0009] An object of the invention is to provide a line driver circuit of reduced cost by applying a smaller design rule than previously practical, and to provide an electro-optic device and display apparatus using this line driver circuit.

SUMMARY OF THE INVENTION

[0010] To achieve these objects, a first line driver circuit according to the present invention for driving a first line of an electro-optic device (which preferably has pixels identified by a plurality of first lines and a plurality of intersecting second lines) has an input terminal that receives signals from a display controller (which controls the display of the electro-optic device). The signals applied to the input terminal are to be supplied to a second line driver circuit for driving the second lines. The first line driver includes a level shifter circuit for shifting signals applied to its input terminal to a specified voltage, and includes an output terminal for outputting to the second line driver circuit the signals shifted to the specified voltage.

[0011] The electro-optic device may include: scan lines 1 to N; intersecting signal lines 1 to M; N×M switching means connected to scan lines 1 to N and to signal lines 1 to M; and N×M pixel electrodes connected to the N×M switching means. The electro-optic device could be an organic EL panel.

[0012] The first line driver circuit and the second line driver circuit cooperate under the control of the display controller to control pixels identified (i.e. addressed) by first and second lines. The first line driver circuit according to the present invention receives signals to be supplied to the second line driver circuit from the display controller, shifts these signals to a specific voltage level, and then supplies the level-shifted signals to the second line driver circuit. It is therefore possible to relay required display driver signals from a display controller (with a complex circuit configuration and excellent general utility) to the second line driver circuit requiring a high driving voltage through a first line driver circuit having a relatively simple circuit configuration, which enables it to be manufactured using a low cost process. It is therefore not necessary to provide a high breakdown voltage interface circuit in the display controller, which was previously, typically required for supplying signals directly to the second line driver circuit. Cost reductions can therefore be achieved by reducing the feature size and using the most advanced low voltage processes.

[0013] Another aspect of the present invention is a line driver circuit for driving a first line of an electro-optic device having pixels identified by a plurality of first lines and a plurality of intersecting second lines, comprising: an input terminal to which signals to be supplied to a power supply circuit are input from a display controller for controlling the display on the electro-optic device; a level shifter circuit for shifting signals input to the input terminal to a specified voltage; and an output terminal for outputting signals shifted to the specified voltage to the power supply circuit.

[0014] This power supply circuit could have a function of supplying multiple voltage levels such as gradation voltages in addition to high and low potential voltages.

[0015] Thus comprised, a line driver circuit and power supply circuit cooperate under the control of a display controller to control pixels identified by first and second lines. Of these, a line driver circuit according to the present invention receives signals to be supplied to the power supply circuit from the display controller, shifts these signals to a specific voltage level, and then supplies the level-shifted signals to the power supply circuit. It is therefore possible to relay required display drive signals from a display controller with a complex circuit configuration and excellent general utility to the power supply circuit requiring high voltage drive through a line driver circuit with a relatively simple circuit configuration enabling manufacturing in a low cost process. It is therefore not necessary to provide the high breakdown voltage interface circuit required for supplying signals directly to the power supply circuit in the display controller, and cost reductions can be achieved by reducing feature size using the most advanced low voltage processes.

[0016] Preferably, the first line is a signal line for supplying a voltage based on image data.

[0017] Thus comprised, signals to be supplied to the circuits are relayed by the signal drive circuit for driving the

signal lines, for example. This makes it possible to reduce the cost of the display controller for controlling the signal drive circuit.

[0018] Yet further preferably the line driver circuit of the invention also has a plurality of selector lines; a first selector circuit for connecting the input terminal and a first selector line selected from among a plurality of selector lines based on a specific first selection signal; and a second selector circuit for connecting the output terminal to the first selector line based on a specific second selection signal.

[0019] Thus comprised, various desirable input terminals and output terminals can be set because the first and second terminal groups are connected by the first and second selector circuits and one of multiple selector lines. It is therefore possible to receive signals from the display controller through a selected desirable terminal of the line driver circuit, and to output the signal from a desired terminal to a downstream supply connection.

[0020] Yet further preferably, the line driver circuit also has a first output buffer circuit for converting the first selector line voltage to the voltage of a low voltage process and supplying the converted voltage to the output terminal; a second output buffer circuit for converting the first selector line voltage to a voltage of a high voltage process and supplying the converted voltage to the output terminal; a first input buffer circuit for supplying a voltage of a low voltage process supplied to the input terminal as a low voltage process voltage to the first selector line; and a second input buffer circuit for converting a voltage of a high voltage process supplied to the input terminal to a voltage of a low voltage process, and supplying the converted voltage to the first selector line. The buffers are exclusively controlled so that only one of the first and second output buffer circuits and first and second input buffer circuits is set to an operating mode at any one time and the other buffer circuits are simultaneously set to a non-operating mode.

[0021] Thus comprised, a circuit for supplying a voltage of an internal low voltage process directly as the voltage of a low voltage process or converting it to the voltage of a high voltage process, or taking the voltage for an internal low voltage process from the voltage of an external low or high voltage process, can be disposed to each terminal by means of the first and second output buffers and first and second input buffers. It is therefore possible to use any terminal as an input terminal or an output terminal. Usability is thus significantly improved.

[0022] An electro-optic device according to a further aspect of the invention has pixels identified by a plurality of first lines and a plurality of intersecting second lines; a line driver circuit as described above; and a second line driver circuit for driving the second lines.

[0023] The invention can thus provide an electro-optic device enabling display controller cost to be reduced by applying a smaller design rule.

[0024] A display apparatus according to a further aspect of the invention is comprised of an electro-optic device having pixels identified by a plurality of first lines and a plurality of intersecting second lines; a line driver circuit as described above; and a second line driver circuit for driving the second lines.

[0025] The invention can thus provide a display apparatus enabling display controller cost to be reduced by applying a smaller design rule.

[0026] Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] In the drawings wherein like reference symbols refer to like parts.

[0028] FIG. 1 is a block diagram showing the basic configuration of a display apparatus containing a line driver circuit according to a preferred embodiment of the invention;

[0029] FIG. 2 shows an example of a driving wave, and other signals, for an LCD panel in a display apparatus in accord with a preferred embodiment of the invention;

[0030] FIG. 3 shows an example of connections between semiconductor devices in an LCD apparatus;

[0031] FIG. 4 shows an example of connections between various semiconductor devices in an LCD apparatus according to a preferred embodiment of the invention;

[0032] FIG. 5 shows the configuration principle of the signal driver in the present embodiment;

[0033] FIG. 6 shows a more detailed configuration of the signal driver of FIG. 5.

[0034] FIG. 7 is a schematic diagram showing the layout of an I/O circuit in a signal driver according to a preferred embodiment of the invention;

[0035] FIG. 8 shows an example of the circuit configuration of the I/O circuit in a preferred embodiment of the invention;

[0036] FIG. 9 shows an example of the circuit configuration of an LV-LV output buffer in a preferred embodiment of the invention;

[0037] FIG. 10 shows an example of the circuit configuration of an LV-LV input buffer in a preferred embodiment of the invention;

[0038] FIG. 11 shows an example of the circuit configuration of an LV-HV output buffer in a preferred embodiment of the invention;

[0039] FIG. 12 shows an example of the circuit configuration of an HV-LV input buffer in a preferred embodiment of the invention;

[0040] FIG. 13 shows an example of the circuit configuration of the control circuit in a preferred embodiment of the invention;

[0041] FIG. 14 shows the basic configuration of a display apparatus applying a signal driver according to the present invention;

[0042] FIG. 15 is a circuit diagram showing one example of a 2-transistor pixel circuit in an organic EL panel; and

[0043] FIG. 16A is a circuit diagram showing one example of a 4-transistor pixel circuit in an organic EL panel, and

[0044] FIG. 16B is a timing chart showing an example of the display control timing of the 4-transistor pixel circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0045] Preferred embodiments of the present invention are described below with reference to the accompanying figures.

[0046] 1. Display Apparatus

[0047] 1.1 Configuration of the Display Apparatus

[0048] The basic configuration of a display apparatus containing a line driver circuit according to the present embodiment of the invention is shown in FIG. 1. The liquid crystal display system 10 according to the present embodiment of a display apparatus of the invention has a liquid crystal display (LCD) panel 20, a signal driver 30 (i.e. a signal drive circuit, a line driver circuit, or more specifically, a source driver), a scan driver 50 (i.e. a scan drive circuit, or more specifically, a gate driver), an LCD controller 60 (more broadly, a display controller), and a power supply circuit 80. The LCD panel (or broadly speaking, any electro-optic device) 20 is formed on a glass substrate, for example. A plurality of scan lines (that is, gate lines or second lines) G1 to Gn (only Gn is shown), where n is a natural number of 2 or more, are disposed in the Y-direction and traverse the X-direction on this glass substrate. A plurality of signal lines (that is, source lines or first lines) S1 to Sm (only Sm is shown), where m is a natural number of 2 or more, are disposed in the X-direction and traverse the Y-direction on this glass substrate. A TFT 22nm (broadly speaking, a switching means) is disposed at the intersection of each scan line and signal line. For example TFT 22nm is disposed at the intersection of scan line Gn (where 1·n·N and n is a natural number) and signal line Sm (where 1·m·M and m is a natural number).

[0049] The gate of TFT 22nm is connected to scan line Gn. The source of TFT 22nm is connected to signal line Sm. The drain of TFT 22nm is connected to pixel electrode 26nm of liquid crystal capacitor 24nm (broadly speaking, a liquid crystal element having an inherent capacitance). Liquid crystal is sealed in LCD capacitor 24nm between pixel electrode 26nm and the opposing electrode 28nm, and the light transmittance of the pixel changes according to the applied voltage between these electrodes.

[0050] Opposing electrode voltage Vcom generated by power supply circuit 80 is supplied to the opposing electrode 28nm.

[0051] Signal driver 30 drives signal lines S1 to Sm of LCD panel 20 based on pixel data for one horizontal scan unit.

[0052] More specifically, the signal driver 30 sequentially latches serial input image data and generates the image data for one horizontal scanning unit. Then, synchronized to the horizontal synchronization signal, the signal driver 30 drives each signal line at a drive voltage based on this image data.

[0053] Synchronized to the horizontal synchronization signal, the scan driver 50 sequentially drives scan lines G1 to Gn in one vertical scanning period.

[0054] More specifically, the scan driver 50 has a flip flop for each scan line 1-n and a shift register to which the flip flops are sequentially connected. The scan driver 50 sequentially selects each scan line in one vertical scanning period by sequentially shifting the vertical synchronization signal supplied from LCD controller 60.

[0055] The LCD controller 60 controls signal driver 30, scan driver 50, and power supply circuit 80 according to content set by a host, such as a central processing unit (CPU), not shown in the figures. More specifically, the LCD controller 60 supplies operating mode settings and the internally generated vertical synchronization signal and horizontal synchronization signal to signal driver 30 and scan driver 50, and supplies the polarization inversion timing of the opposing electrode voltage Vcom to the power supply circuit 80.

[0056] Based on an externally supplied reference voltage, power supply circuit 80 generates opposing electrode voltage Vcom and also generates the voltage levels required to drive the liquid crystals of the LCD panel 20. These various voltage levels are supplied to signal driver 30, scan driver 50, and LCD panel 20. The opposing electrode voltage Vcom is supplied to an opposing electrode disposed opposite the TFT pixel electrodes of the LCD panel 20.

[0057] In a liquid crystal apparatus 10 thus comprised, signal driver 30, scan driver 50, and power supply circuit 80 cooperatively drive LCD panel 20 based on externally supplied image data, as controlled by LCD controller 60, to display an image on LCD panel 20.

[0058] It should be noted that although LCD controller 60 is included in the configuration of the liquid crystal apparatus 10 shown in FIG. 1, the LCD controller 60 can be disposed external to the liquid crystal apparatus 10. It is also possible to incorporate both the LCD controller 60 and host (i.e. cpu) within the liquid crystal apparatus 10.

[0059] 1.2 Liquid Crystal Drive Wave

[0060] FIG. 2 shows an example of a drive wave for the LCD panel 20 in the liquid crystal apparatus 10 described above. A line inversion drive method is shown here.

[0061] Signal driver 30, scan driver 50, and power supply circuit 80 are controlled according to the display timing generated by the LCD controller 60 in this liquid crystal apparatus 10. The LCD controller 60 sequentially passes image data for one horizontal scanning unit to the signal driver 30, and supplies polarity inversion signal POL indicating the internally generated horizontal synchronization signal and inversion drive timing. The LCD controller 60 also supplies the internally generated vertical synchronization signal to the scan driver 50, and supplies opposing electrode voltage polarity inversion signal VCOM to the power supply circuit 80.

[0062] As a result, the signal driver 30 drives signal lines based on image data for one horizontal scanning unit synchronized to the horizontal synchronization signal. Triggered by the vertical synchronization signal, the scan driver 50 drives the scan lines connected to the gates of the TFTs arrayed in a matrix on the LCD panel 20 with sequential drive voltage Vg. The power supply circuit 80 inverts the polarity of the internally generated opposing electrode voltage Vcom synchronized to the opposing electrode voltage

polarity inversion signal VCOM while supplying the opposing electrode voltage Vcom to the opposing electrodes of the LCD panel 20.

[0063] A charge corresponding to the voltage Vcom of the pixel electrode connected to the drain of TFT 22nm and the opposing electrode charges the liquid crystal capacitor 24nm. Image display is possible when the pixel electrode voltage Vp held by the charge stored in the liquid crystal capacitor exceeds a particular threshold value VCL. When the pixel electrode voltage Vp exceeds this particular threshold value VCL, pixel transmittance changes according to the voltage level, and a gray scale display is possible.

[0064] 2. Features of the Present Embodiment

[0065] The voltage required to drive the display of an LCD apparatus is different for the various other semiconductor devices, such as LCD controller 60, signal driver 30, scan driver 50, and power supply circuit 80.

[0066] FIG. 3 shows an example of the connections between semiconductor devices in an LCD apparatus.

[0067] The preferred supply voltage level of the signals communicated between the semiconductor devices is also shown here.

[0068] The LCD panel 120, signal driver 130, scan driver 150, LCD controller 160, and power supply circuit 180 of this liquid crystal apparatus 100 have the same function as the corresponding parts of the liquid crystal apparatus 10 shown in FIG. 1.

[0069] For example, the signal driver 130 is manufactured with a medium voltage process to balance integration and low cost, such as a 0.35 micron process, instead of the most advanced design rule process because the circuit design is not particularly complicated.

[0070] The scan driver 150 does not require shrinking due to its simple circuit design, and is manufactured in a high voltage process in order to drive a high voltage (such as 20 V to 50 V), as determined by the relationship between the liquid crystal material and TFT performance.

[0071] The power supply circuit 180 generates the high voltage supplied to the scan driver 150, and is therefore manufactured in a high breakdown voltage process.

[0072] The LCD controller 160 has a complex circuit configuration and a wide range of applications, and its cost can be greatly reduced by reducing the chip size. The LCD controller 160 is therefore manufactured in the most advance design rule process (such as a 0.18 micron process). Specifically, because the LCD controller 160 is manufactured in a low voltage process, it has both a low voltage process interface circuit and a high voltage process interface circuit.

[0073] The low voltage process interface circuit supplies a signal generated at the supply level of the low breakdown voltage design rule process to signal driver 130, which is manufactured in a medium breakdown voltage process. The high voltage process interface circuit supplies a signal shifted to the supply level for the high breakdown voltage process to the scan driver 150 and power supply circuit 180, which are manufactured in a high breakdown voltage process.

[0074] The LCD controller 160 thus also has a high voltage process interface circuit. The area of this high voltage process interface circuit cannot be made smaller in the IC even as the design rule gets smaller because the design rule includes physical limits needed to assure a sufficient breakdown voltage. It is therefore not possible to derive much benefit from the cost reductions enabled by design rule reduction.

[0075] In a liquid crystal apparatus 10 according to the present invention, however, the signal group to be supplied from LCD controller 60 (which is manufactured in a low breakdown voltage process) to scan driver 50 and power supply circuit 80 (manufactured in a high breakdown voltage process) passes first through the signal driver 30 (which is manufactured in a medium breakdown voltage process), and the signal group is then passed from the signal driver 30 to the scan driver 50 and power supply circuit 80.

[0076] FIG. 4 shows an example of connections between various semiconductor devices in a LCD apparatus according to this embodiment of the invention.

[0077] The signal driver 30 of the present embodiment thus includes interface unit 200, which itself includes an interface circuit constructed with a medium voltage process and effective for converting voltages from low voltage processed components to the voltage of high voltage processed components. Interface unit 200 receives the low voltage signal group supplied from LCD controller 60, and then supplies it to the scan driver 50 or power supply circuit 80 after converting it to the high voltage suitable for the high voltage process.

[0078] This makes it unnecessary to provide an interface circuit for driving a high voltage in interface unit 210 of the LCD controller 60. This enables complex circuit configurations to be scaled down and enables the cost to be reduced in conjunction with reductions in process dimensions.

[0079] 2.1 Configuration Principle of the Present Embodiment

[0080] FIG. 5 illustrates the principle of the signal driver 30 configuration in accord with the present embodiment.

[0081] Signal driver 30 has I/O circuits 300₁ to 300_P (where P is a natural number), and has input terminals 310_i and output terminals 320_i corresponding to each I/O circuit 300_i (where 1 ≤ i ≤ P, and i is a natural number).

[0082] Each I/O circuit 300_i includes a corresponding level shifter 302_i for converting a relatively low voltage from the low breakdown voltage side to a higher voltage for the high breakdown voltage side.

[0083] Level shifter 302_i converts the voltage magnitude of signals from the low breakdown voltage side input applied at input terminals 310_i to higher voltage magnitudes for the high breakdown voltage side supplied at the level-shifter output to output terminals 320_i. Therefore, the cost of LCD controller 60 can be reduced by applying a smaller design rule in its construction, since the outputs of LCD controller 60 are connected to input terminals 310₁ to 310_P, and output terminals 320₁ to 320_P are connected to either scan driver 50 or power supply circuit 80, which are manufactured in high voltage processes.

[0084] 3. Signal Driver (Line Driver Circuit) in this Embodiment

[0085] The signal driver 30 (line driver circuit) is described below in more detail.

[0086] FIG. 6 shows the basic configuration of signal driver 30 in the present embodiment.

[0087] Signal driver 30 has input/output pads 400_1 to 400_Q (where Q is a natural number) disposed according to the terminals of the semiconductor device. Signal driver 30 also has an I/O circuit 410_j (wherein $1 \leq j \leq Q$ and j is a natural number) corresponding to each I/O pad 400_1 to 400_Q . I/O circuits 410_1 to 410_Q are commonly connected to one or more selector lines 430. It should be noted that there are preferably 16 selector lines 430 in this example.

[0088] Each I/O (i.e. input/output) circuit 410_j has multiple selectively enabled input buffers and multiple selectively enabled output buffers, and can therefore function as either an input circuit or an output circuit depending upon an input/output selection signal. For example, if I/O circuit 410_1 is set to function as an input circuit and I/O circuit 410_Q is set to function as an output circuit, then a signal applied to I/O pad 400_1 is input to I/O circuit 410_1 , which then passes the input signal to a particular one of selector lines 430 (identified as a "first selector line" in the present example). High and low voltage signals applied to I/O pads 400_1 to 400_Q from the high or low breakdown voltage side of signal driver 30 are converted to the appropriate output voltage level at this time.

[0089] I/O pad 400_Q of I/O circuit 410_Q is electrically coupled to the "first selector line" by a selector circuit (424j shown in FIG. 7 and described below). In this case signals carried on the first selector line are converted to the voltage level of the high or low breakdown voltage side, as appropriate.

[0090] It is therefore possible to convert signals having a first voltage level and applied to a selected input terminal to a second voltage level appropriate for output on a selected output terminal.

[0091] FIG. 7 is a schematic diagram showing the layout of each of the above-described I/O circuits 410_j . Each of I/O circuits 410_j (where $1 \leq j \leq Q$) include an LV-LV (low voltage to low voltage) buffer 412j electrically connected to the I/O pads 400j, an LV-HV (low voltage to high voltage) buffer 418j, a selector circuit 424j, and a gate array 426j. Note that LV denotes low voltage and HV denotes high voltage.

[0092] LV-LV buffer 412j includes an LV-LV output buffer 414j and an LV-LV input buffer 416j.

[0093] LV-LV output buffer 414j (first output buffer) buffers low voltage signals to a buffer circuit connected to an LV supply voltage level, and outputs to I/O pad 400j.

[0094] LV-LV input buffer 416j (first input buffer) buffers the voltage of LV signals input through I/O pad 400j to a buffer connected to an LV supply voltage level, and outputs to selector circuit 424j.

[0095] The LV-HV buffer 418j has an LV-HV output buffer 420j and HV-LV input buffer 422j.

[0096] The LV-HV output buffer 420j (second output buffer) is a circuit for converting the voltage of LV signals

to the voltage of HV signals, and outputting the converted voltage signal to I/O pad 400j.

[0097] The HV-LV input buffer 422j (second input buffer) is a circuit for buffering the voltage of HV signals input through I/O pad 400j to a buffer circuit connected to an LV supply voltage level, and outputting to selector circuit 424j.

[0098] Selector circuit 424j connects LV-LV output buffer 414j, LV-LV input buffer 416j, LV-HV output buffer 420j, or HV-LV input buffer 422j to one of the selector lines 430.

[0099] Gate array 426j is a logic circuit for generating a control signal for exclusively operating LV-LV output buffer 414j, LV-LV input buffer 416j, LV-HV output buffer 420j, or HV-LV input buffer 422j, and the selection signal for selector circuit 424j.

[0100] LV-LV output buffer 414j, LV-LV input buffer 416j, LV-HV output buffer 420j, or HV-LV input buffer 422j are controlled by gate array 426j such that only one of the four buffers operates at any one time, i.e. to operate exclusively of the other three buffers, with this type of I/O circuit 410_j . That is, the output of at least the unselected input buffers and output buffers is placed in a high impedance state. The selected input buffer or output buffer is electrically connected to a selector line, as specified by gate array 426j. The specified selector line is electrically coupled to a corresponding I/O pad through the I/O circuit.

[0101] By thus freely selecting particular I/O circuits and I/O pads and electrically connecting the selected I/O circuits through selector lines, the voltage of LV signals or HV signals can be converted and output between desired input and output terminals.

[0102] It should be noted that as shown in FIG. 7 LV and HV signal interface functions can be built in to I/O circuit 410_j by breaking I/O pad 400j (which is formed by Al vapor deposition) into electrically isolated pads as indicated by lines A-A, B-B, and C-C.

[0103] FIG. 8 shows an example of the circuit configuration of I/O circuit 410_j .

[0104] I/O pad 400j is electrically connected to the output terminal of LV-LV output buffer 414j, the input terminal of LV-LV input buffer 416j, the output terminal of LV-HV output buffer 420j, and the input terminal of HV-LV input buffer 422j.

[0105] The input terminal of LV-LV output buffer 414j is electrically connected at node ND to the output terminal of LV-LV input buffer 416j, the input terminal of LV-HV output buffer 420j, the output terminal of HV-LV input buffer 422j. Node ND functions as a terminal of the switching circuit SWA.

[0106] The other terminal of switching circuit SWA is connected to selector lines SL1 to SL16 through selector circuit 424j, which contains selector switches SW1 to SW16.

[0107] Control signals SB1 to SB4 exclusively select any one of the buffers. Switching control signal SA switches circuit SWA on and off. Selection signals SEL1 to SEL16 for alternatively select selector switches SW1 to SW16. These control signals are generated by control circuit 440j. As shown in FIG. 7, this control circuit 440j is comprised of a gate array. The control circuit 440j generates control signals

SB1 to SB4 and selection signals SEL1 to SEL16 according to set content from the host (not shown in the figure).

[0108] Switching circuit SWA reduces the output load of LV-LV input buffer 416j and HV-LV input buffer 422j by electrically isolating the buffers and selector switches SW1 to SW16. This makes it possible to shrink the LV-LV input buffer 416j and HV-LV input buffer 422j.

[0109] It should be noted that in the present embodiment LV-LV output buffer 414j, LV-LV input buffer 416j, LV-HV output buffer 420j, and HV-LV input buffer 422j are configured to invert the logic level of their respective input logic (that is, invert the phase), and to output the inverted signal according to control signals SB1 to SB4 and inversion control signals INV1 to INV4 supplied from control circuit 440j.

[0110] The specific configuration of each buffer is described next below.

[0111] The LV supply voltage is denoted below as VCC, the HV supply voltage is denoted as VDD, and the ground level is denoted as VSS. The inverse of control signal CONT is XCONT. Similarly, the inverse logic of any signal is denoted by an "X" in front of the signal name.

[0112] FIG. 9 shows an example of the circuit configuration of LV-LV output buffer 414j.

[0113] LV-LV output buffer 414j has inverter circuits 500j and 504j, multiplexor 502j, level shifter 506j, and transfer circuit 508j. Multiplexor 502j is responsive to control signal INV (and its inverse XINV) to selectively pass either the inverted or non-inverted version of signal ND to inverter circuit 504j. Inverter 500j and multiplexor 502j together form an XOR (exclusive OR) logic gate responsive to signals INV and ND as inputs, and outputting the XOR combination of signals INV and ND to the input of inverter 504j.

[0114] Level shifter 506j and transfer circuit 508j are comprised of HV transistors. Inverter circuits 500j and 504j and multiplexor 502j are LV transistors. HV transistors are formed with a thicker oxide film than LV transistors in order to achieve a higher breakdown voltage. The design rules for HV transistors must therefore be larger than those for LV transistors, and circuit area necessarily increases.

[0115] The level shifter 506j outputs an HV level voltage on one of its outputs as determined by the logic level of control signal SB1 (and its inverted control signal XSB1). The output of level shifter 506j controls the on/off state of transfer circuit 508j.

[0116] Input node ND is connected to the input node of inverter circuit 500j.

[0117] The input node and output node of inverter circuit 500j are connected to multiplexor 502j. Multiplexor 502j together with inverter 500j constitute an XOR and obtain the exclusive OR of the logic levels of inversion control signal INV1 and input node ND, and supply the result to the input node of inverter circuit 504j.

[0118] The output node of inverter circuit 504j is selectively coupled to I/O pad 400j through transfer circuit 508j.

[0119] LV-LV output buffer 414j is thus able to selectively invert the logic level of input node ND based on inversion

control signal INV1. The output node is connected to I/O pad 400j through HV transfer circuit 508j. Damage to LV transistors resulting from mistaken supply of an HV level voltage to the I/O pad 400j can thus be avoided and reliability be maintained. Furthermore, because logic level inversion can be freely controlled by inversion control signal INV1, design changes due to changes in external interface specifications can be avoided, and the development time can be shortened.

[0120] FIG. 10 shows an example of the circuit configuration of LV-LV input buffer 416j.

[0121] The LV-LV input buffer 416j has a level shifter 520j, a transfer circuit 522j, an inverter circuit 524j, and a multiplexor circuit 526j. Inverter circuit 524j and multiplexor circuit 526j together functions as an XOR circuit.

[0122] The level shifter 520j and transfer circuit 522j are comprised of HV transistors. Inverter circuit 524j and multiplexor circuit 526j are comprised of LV transistors.

[0123] Level shifter 520j outputs an HV level voltage on one of its outputs as determined by the logic level of control signal SB2 (and its logic complement, i.e. the inverted control signal XSB2). The output of level shifter 520j controls the on/off state of transfer circuit 522j.

[0124] The I/O pad 400j is selectively coupled to inverter circuit 524j (comprised of LV transistors) through transfer circuit 522j.

[0125] It should be noted that n-type transistor 528j is connected between the input node of inverter circuit 524j and ground level VSS. Inverted signal XSB2 of control signal SB2 is supplied to the gate of n-type transistor 528j. Therefore, when inverted signal XSB2 is HIGH and LV-LV input buffer 416j is not selected, the voltage of the input node to inverter circuit 524j can be fixed to ground level VSS through n-type transistor 528j, and current passing through inverter circuit 524j when unselected can be reduced.

[0126] The input node and output node of inverter circuit 524j are connected to multiplexor circuit 526j. Multiplexor circuit 526j in combination with inverter circuit 524j achieves the exclusive OR function of the logic levels of the inversion control signal INV2 and the input node of inverter circuit 524j, and the result determines the logic level of node ND.

[0127] Multiplexor circuit 526j is connected to LV supply voltage VCC through p-type transistor 530j, and to ground level VSS through n-type transistor 532j. The inverted control signal XSB2 is supplied to the gate of p-type transistor 530j, and control signal SB2 is supplied to the gate of n-type transistor 532j.

[0128] Therefore, when LV-LV input buffer 416j is selected, the result of the above exclusive OR operation is output from node ND, and when LV-LV input buffer 416j is not selected node ND is in a high impedance state.

[0129] The LV-LV input buffer 416j thus receives signals from I/O pad 400j through HV transfer circuit 522j, and can freely invert the logic level by means of XOR circuit combination 524j/526j. As a result, reliability is not impaired even when an HV level voltage (VDD for reference high) is mistakenly supplied to I/O pad 400j, and an LV

level voltage (VCC for reference high) can be supplied to node ND. Furthermore, because the logic level can be freely inverted as controlled by inversion control signal INV2, design changes due to a change in external interface specifications can be avoided and the development time can be shortened.

[0130] FIG. 11 shows an example of the circuit configuration of the LV-HV output buffer 420j.

[0131] The LV-HV output buffer 420j has inverter circuits 540j and 544j, multiplexor circuit 542j, NAND gate 546j, inverter circuits 548j and 552j, level shifter 550j, NOR gate 554j, inverter circuits 556j and 560j, and level shifter 558j. Multiplexor circuit 542j in conjunction with inverter circuit 540j produce an XOR function with signals ND and INV3 as inputs.

[0132] This LV-HV output buffer 420j has p-type transistor 562j and n-type transistor 564j connected between HV supply voltage VDD and ground level VSS for high impedance control of output to I/O pad 400j.

[0133] Inverter circuits 540j, 544j, 548j, and 556j, multiplexor circuit 542j, NOR gate 546j and NAND gate 554j are comprised of LV transistors. The level shifters 550j and 558j, inverter circuits 552j and 560j, p-type transistor 562j, and n-type transistor 564j are comprised of HV transistors.

[0134] The input node ND is connected to the input node of inverter 540j.

[0135] The input node and output node of inverter circuit 540j are connected to multiplexor circuit 542j. Multiplexor circuit 542j together with inverter 540j achieve an XOR function and obtain the exclusive OR of the logic levels of inversion control signal INV3 and input node ND, and supply the result to the input node of inverter circuit 544j.

[0136] The output node of inverter circuit 544j is connected to NOR gate 546j and to NAND gate 554j.

[0137] NOR gate 554j obtains the inverse OR of the logic level of control signal SB3 and the logic level of the output node of inverter circuit 544j, and supplies the result to the input node of inverter circuit 548j.

[0138] NAND gate 546j obtains the inverse AND of the logic level of control signal SB3 and the output node of inverter circuit 544j, and supplies the result to the input node of inverter circuit 556j.

[0139] Level shifter 550j outputs an HV level voltage (i.e. VDD) or ground potential (i.e. VSS) as determined by the logic level of the output of NAND gate 546j (i.e. the input and output nodes of inverter circuit 548j), and supplies the result to the input node of inverter 552j, which is comprised of HV transistors. The output node of inverter circuit 552j is connected to the gate of p-type transistor 562j.

[0140] Level shifter 558j outputs an HV voltage (i.e. VDD) or ground potential (i.e. VSS) as determined by the logic level of the output of NOR gate 554j (i.e. the input and output nodes of inverter circuit 556j), and supplies the result to the input node of inverter circuit 560j, which is comprised of HV transistors. The output node of inverter circuit 560j is connected to the gate of n-type transistor 564j.

[0141] The LV-HV output buffer 420j can thus also freely invert the logic level of the input node ND based on

inversion control signal INV3. The gate control signal generated from the output node and control signal SB3 is also converted to an HV level voltage by level shifter 550j and level shifter 558j for controlling p-type transistor 562j and n-type transistor 564j.

[0142] Because logic level inversion can be freely controlled using the inversion control signal INV3, design changes due to a change in external interface specifications can be avoided and development time can be shortened. It is also possible to provide an output buffer circuit for shifting LV level voltages to HV level voltages and high impedance controlling the output.

[0143] FIG. 12 shows an example of the circuit configuration of the HV-LV input buffer 422j.

[0144] The HV-LV input buffer 422j comprises an inverter circuit 570j and an multiplexor 572j. Inverter circuit 570j and multiplexor 572j together functions as an XOR gate.

[0145] The inverter circuit 570j is comprised of HV transistors, and the LV supply voltage VCC is supplied to the inverter circuit 570j as the supply voltage level.

[0146] The I/O pad 400j is connected to the input node of inverter circuit 570j. As a result, when an LV signal voltage is supplied to the I/O pad 400j, inverter circuit 570j detects the signal and passes the inverted signal to its output node.

[0147] The input and output nodes of the inverter circuit 570j are connected to multiplexor 572j. The combination of inverter circuit 570j and multiplexor 572j obtain the exclusive OR logic combination of the inversion control signal INV4 and the logic level of I/O pad 400j, and the result becomes the logic level of node ND.

[0148] Multiplexor 572j is connected to LV supply voltage VCC through p-type transistor 574j and to ground level VSS through n-type transistor 576j. Inverted control signal XSB4 is supplied to the gate of p-type transistor 574j and control signal SB4 is supplied to the gate of n-type transistor 576j.

[0149] Therefore, when HV-LV input buffer 422j is selected, the result of the exclusive OR operation is output on node ND, and when not selected node ND goes to a high impedance state.

[0150] The HV-LV input buffer 422j thus receives signals from I/O pad 400j through HV inverter circuit 570j connected to LV supply voltage VCC, and can freely invert the logic level by means of multiplexor 572j. As a result, reliability is not impaired even when an HV voltage is mistakenly applied to I/O pad 400j, and an LV level voltage can be supplied to node ND. Furthermore, because the logic level can be freely inverted as controlled by inversion control signal INV4, design changes due to a change in external interface specifications can be avoided and development time can be shortened.

[0151] Control circuit 440j (FIG. 8), which separately controls each of the buffers, generates control signals SB1 to SB4, selection signals SEL1 to SEL16, and switching control signal SA.

[0152] FIG. 13 shows an example of the circuit configuration of control circuit 440j.

[0153] This control circuit 440j generates control signals SB1 to SB4, selection signals SEL1 to SEL16, and switch-

ing control signal SA by setting specific command registers by means of LCD controller 60.

[0154] The inputs to decoder DEC from flip-flops FF<0:7> are synchronized to clock signal CK. In accordance with clock signal CK, flip-flops FF<0:7> latch address decode pulses from corresponding data bus lines D0 to D7, which are generated when a particular command register is accessed by the LCD controller 60. That is, data bus lines D7 to D0 each carry one bit of data representative of a corresponding address decode pulse, and the data bit is stored in corresponding flip-flops FF<0:7>. The flip-flops FF<0:7> are set or reset by the logical combination of default data S7 to S0 and inversion reset signal XRES. For example, if XRES is at a logic low, then a flip-flop (i.e. FF<0>) will be initialized (i.e. will be set) if its corresponding default data (S0) is at a logic high and will be reset if its corresponding default data (S0) is at a logic low. Additionally, default data S7 to S0 can be fixed to either the supply voltage or to ground level by appropriate blowing of AI fuses (or other post-fabrication shorting method, such as the using of a laser to cut metal traces). The default state can thus be permanently set.

[0155] The data stored in each of the flip-flops is thus decoded by decoder circuit DEC to output control signals SB1 to SB4. The control circuit 440j thus comprised can select one selector line from among the plurality of selector lines 430 by means of selector circuit 424j (FIG. 7), and provides separate control for the four buffer circuits.

[0156] It should be noted that the output load of the buffers can be reduced by electrically disconnecting the buffers and selector lines by applying an appropriate switching control signal SA.

[0157] Furthermore, inversion control signals INV1 to INV4 can be likewise generated.

[0158] 4. LCD Apparatus Applying a Signal Driver According to the Present Invention.

[0159] FIG. 14 shows the basic configuration of a liquid crystal apparatus 10 applying a signal driver according to the present invention.

[0160] It should be noted that like parts in FIG. 14 and FIG. 4 are identified by like reference numerals, and further description thereof is omitted below.

[0161] The LCD controller 60 supplies clock signal CPH, latch pulse LP as a horizontal synchronization signal, command signal CMD specifying a particular command, inverse signal INV of a signal, data D0 to D17 representing image data or command data, polarization inversion signal POL indicating the polarity inversion drive timing, output enable signal OE, enable I/O signal EIO, and inversion reset signal XRESH to the signal driver 30 for signal drive control.

[0162] The LCD controller 60 also supplies clock signal CPV, start signal STV as a vertical synchronization signal, inverse output enable signal XOEV, output control signal XOHV for controlling output of all scan lines, and inversion reset signal XRESV to the scan driver 50 for scan drive control. In this embodiment of the invention control signals to be supplied from LCD controller 60 to the scan driver 50 pass through signal driver 30 having I/O circuits as described above for level shifting before being supplied to the scan driver 50.

[0163] The LCD controller 60 also supplies standby control signal XSTBY, step-up mode setting signal PMDE, primary and secondary step-up clocks PCK1 and PCK2, and opposing electrode voltage polarity inversion signal VCOM to the power supply circuit 80 for power supply control. In this embodiment of the invention control signals to be supplied from LCD controller 60 to the power supply circuit 80 pass through signal driver 30 having I/O circuits as described above for level shifting before being supplied to the power supply circuit 80.

[0164] It is therefore not necessary to provide an HV interface circuit in the LCD controller 60, which has a relatively complex circuit configuration, and signals can be shifted and passed by the signal driver 30, which is manufactured in a medium voltage process and does not require shrinking. The LCD controller 60 therefore has wide applicability and significant cost reductions can be achieved by applying a smaller design rule to reduce chip size.

[0165] 5. Other

[0166] The present embodiment has been described using by way of example a liquid crystal display apparatus with an LCD panel using TFT liquid crystals, but the invention shall not be so limited. For example, the invention can also be applied to a signal driver and scan driver for driving an organic EL panel display using organic EL devices disposed at pixel locations defined by the signal lines and scan lines.

[0167] FIG. 15 shows an example of a 2-transistor pixel circuit in an organic EL panel display controlled by a signal driver and scan driver as described above according to the present invention.

[0168] This organic EL panel has a drive TFT 800nm, switch TFT 810nm, storage capacitor 820nm, and organic LED 830nm at the intersection of each signal line Sm and scan line Gn. The drive TFT 800nm is a p-type transistor.

[0169] The drive TFT 800nm and organic LED 830nm are connected in series to the power supply line.

[0170] The switch TFT 810nm is inserted between the gate of drive TFT 800nm and signal line Sm. The gate of switch TFT 810nm is connected to scan line Gn.

[0171] The storage capacitor 820nm is inserted between the gate of drive TFT 800nm and the capacitor line.

[0172] When scan line Gn is driven and switch TFT 810nm turns on in this organic EL device, the voltage of signal line Sm is transferred to storage capacitor 820nm and applied to the gate of drive TFT 800nm. The gate voltage Vgs of drive TFT 800nm is determined by the voltage of signal line Sm, and controls current flow through drive TFT 800nm. Because the drive TFT 800nm and organic LED 830nm are connected in series, current flow through drive TFT 800nm flows directly to organic LED 830nm.

[0173] Therefore, by holding gate voltage Vgs set to the voltage of the signal line Sm in storage capacitor 820nm, a pixel that continues emitting throughout one frame period, for example, can be achieved by supplying a current corresponding to the gate voltage Vgs to organic LED 830nm.

[0174] FIG. 16A shows an example of a 4-transistor pixel circuit in an organic EL panel driven by a signal driver and scan driver as described above. FIG. 16B shows an example of the display control timing for this pixel circuit.

[0175] In this case the organic EL panel has a drive TFT **900nm**, switch TFT **910nm**, storage capacitor **920nm**, and organic LED **930nm**.

[0176] This circuit differs from the 2-transistor pixel circuit shown in **FIG. 15** in that instead of a constant voltage, a constant current I_{data} is supplied to the pixel from constant current source **950nm** through p-type TFT **940nm**, which functions as a switching element. Additionally, storage capacitor **920nm** and drive TFT **900nm** are connected to the power supply line through p-type TFT **960nm**, which functions as a switching element.

[0177] With this organic EL device p-type TFT **960nm** is first turned off by gate voltage V_{gp} to interrupt the power supply line, and p-type TFT **940nm** and switch TFT **910nm** are turned on by gate voltage V_{sel} to supply constant current I_{data} from **950nm** to the drive TFT **900nm**.

[0178] A voltage corresponding to constant current I_{data} is held in storage capacitor **920nm** until current flow to the drive TFT **900nm** stabilizes.

[0179] Gate voltage V_{sel} is then applied to turn off p-type TFT **940nm** and switch TFT **910nm**, and gate voltage V_{gp} is applied to turn on p-type TFT **960nm**, thereby electrically connecting the power supply line, drive TFT **900nm**, and organic LED **930nm**. Current equal to or greater than constant current I_{data} is thus supplied to the organic LED **930nm** at this time based on the voltage held in storage capacitor **920nm**.

[0180] This type of organic EL device can also be configured with the scan lines as gate voltage V_{sel} and the signal lines as the data lines.

[0181] The configuration of the organic LED is not limited and can be configured with the light-emitting layer over the transparent anode (ITO) and a metal cathode on top, or with the light-emitting layer, light-transmitting cathode, and transparent seal on top of the metal anode.

[0182] The display controller for driving an organic EL panel can thus be scaled down by configuring the signal driver for display driving an organic EL panel containing such organic EL devices as described above.

[0183] It will be apparent to one with ordinary skill in the related art that the present invention shall not be limited to the embodiments described above and can be varied in many ways without departing from the scope of the accompanying claims. For example, the invention can also be applied to a plasma display device.

[0184] Furthermore, a signal driver has been described above as the line driver circuit by way of example, but the invention shall also not be so limited.

[0185] Although the present invention has been described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications will be apparent to those skilled in the art. Such changes and modifications are to be understood as included within the scope of the present invention as defined by the appended claims, unless they depart therefrom.

What is claimed is:

1. A line driver circuit for driving a first line of an electro-optic device having pixels identified by a plurality of said first lines and a plurality of intersecting second lines, comprising:

an input terminal for receiving second signals to be supplied to a second line driver circuit for driving said second lines, said signals being supplied from a display controller for controlling the display of said electro-optic device;

a level shifter circuit for shifting to a specified voltage said second signals; and

an output terminal for outputting the level shifted second signals to said second line driver circuit.

2. A line driver circuit as described in claim 1, wherein said first line is a signal line for supplying a voltage dependent on image data.

3. A line driver circuit as described in claim 1, further comprising:

a plurality of selector lines;

a first selector circuit for selectively coupling said input terminal to a first selector line from among said plurality of selector lines as determined by a first selection signal; and

a second selector circuit for selectively coupling said output terminal to said first selector line as determined by a second selection signal.

4. A line driver circuit as described in claim 3, further comprising:

a first output buffer circuit for converting the voltage of said first selector line to a first reference high voltage and supplying the converted first reference high voltage to said output terminal;

a second output buffer circuit for converting the voltage of said first selector line to a second reference high voltage of greater magnitude than said first reference high voltage, and supplying the converted second reference high voltage to the output terminal;

a first input buffer circuit for receiving said first reference high voltage at said input terminal and supplying said first reference high voltage to said first selector line;

a second input buffer circuit for converting said second reference high voltage applied to said input terminal to said first reference high voltage, and supplying the converted first reference high voltage to said first selector line;

wherein said first and second input buffer circuits and said first and second output buffer circuits are each responsive to a separate enable signal; and

wherein said separate enable signals are effective for operating in unison only one of said first and second input buffer circuits and together with one of said first and second output buffer circuits.

5. An electro-optic device comprising:

pixels identified by a plurality of first lines and a plurality of intersecting second lines;

a line driver circuit as described in claim 1; and

a second line driver circuit for driving said second lines.

6. A display apparatus comprising:

an electro-optic device having pixels identified by a plurality of first lines and a plurality of intersecting second lines;

a line driver circuit as described claim 1; and

a second line driver circuit for driving said second lines.

7. A line driver circuit for driving a first line of an electro-optic device having pixels identified by a plurality of said first lines and a plurality of intersecting second lines, comprising:

an input terminal for receiving power signals to be supplied to a power supply circuit, said power signals being supplied by a display controller for controlling the display of said electro-optic device;

a level shifter circuit for shifting to a specified voltage said power signals; and

an output terminal for outputting the level shifted power signals to said power supply circuit.

8. A line driver circuit as described in claim 7, wherein said first line is a signal line for supplying a voltage dependent on image data.

9. A line driver circuit as described in claim 7, further comprising:

a plurality of selector lines;

a first selector circuit for selectively coupling said input terminal to a first selector line from among said plurality of selector lines as determined by a first selection signal; and

a second selector circuit for selectively coupling said output terminal to said first selector line as determined by a second selection signal.

10. A line driver circuit as described in claim 9, further comprising:

a first output buffer circuit for converting the voltage of said first selector line to a first reference high voltage and supplying the converted first reference high voltage to said output terminal;

a second output buffer circuit for converting the voltage of said first selector line to a second reference high voltage of greater magnitude than said first reference high voltage, and supplying the converted second reference high voltage to the output terminal;

a first input buffer circuit for receiving said first reference high voltage at said input terminal and supplying said first reference high voltage to said first selector line;

a second input buffer circuit for converting said second reference high voltage applied to said input terminal to said first reference high voltage, and supplying the converted first reference high voltage to said first selector line;

wherein said first and second input buffer circuits and said first and second output buffer circuits are each responsive to a separate enable signal; and

wherein said separate enable signals are effective for operating in unison only one of said first and second input buffer circuits and together with one of said first and second output buffer circuits.

11. An electro-optic device comprising:

pixels identified by a plurality of first lines and a plurality of intersecting second lines;

a line driver circuit as described in claim 7; and

a second line driver circuit for driving said second lines.

12. A display apparatus comprising:

an electro-optic device having pixels identified by a plurality of first lines and a plurality of intersecting second lines;

a line driver circuit as described claim 7; and

a second line driver circuit for driving said second lines.

* * * * *

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摘要(译)

线路驱动器电路，电光器件和显示装置通过简化工艺尺寸并通过简化输出电压的重新配置有效地缩短显示面板显影周转时间而有效地降低了成本。液晶装置10具有LCD面板20，信号驱动器30，扫描驱动器50和电源电路80，每个都由LCD控制器60控制。信号驱动器30包含用于转换a的LCD接口单元200。为低压过程指定的第一电压到为高压过程指定的第二电压。接口单元200内的接口电路由使用中压过程的装置组成。接口单元200接收从LCD控制器60提供的低电压信号（即第一电压电平）并将其转换为高电压信号（即第二电压电平），并将电平移位的电压信号提供给扫描驱动器50或电源电路80。

