US 20020080318A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0080318 A1

Yamate et al. (43) Pub. Date: Jun. 27, 2002

(54) LIQUID CRYSTAL DISPLAY

(76) Inventors: **Hiroshi Yamate**, Mobara (JP); **Yuuichi Takenaka**, Mobara (JP)

Correspondence Address:
ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

(21) Appl. No.: **10/022,259**

(22) Filed: **Dec. 20, 2001**

(30) **Foreign Application Priority Data**

Dec. 25, 2000 (JP) 2000-392324

Publication Classification

(51) **Int. Cl.**[7] **G02F 1/1345**

(52) **U.S. Cl.** **349/149**

(57) **ABSTRACT**

A liquid crystal display is provided with respective signal lines and a semiconductor chip. Respective output bumps of the semiconductor chip are connected to the corresponding respective signal lines through an anisotropic conductive layer. The respective output bumps include a first group of output bumps which are arranged at a side close to the signal lines and a second group of output bumps which are arranged at a side remote from the signal lines. Area of respective bumps of the second group of output bumps which face the signal lines in an opposed manner is set larger than area of respective bumps of the first group of output bumps which face the signal lines in an opposed manner. Due to such a constitution, the reliable connection between the mounted semiconductor integrated circuit and the signal lines is ensured.

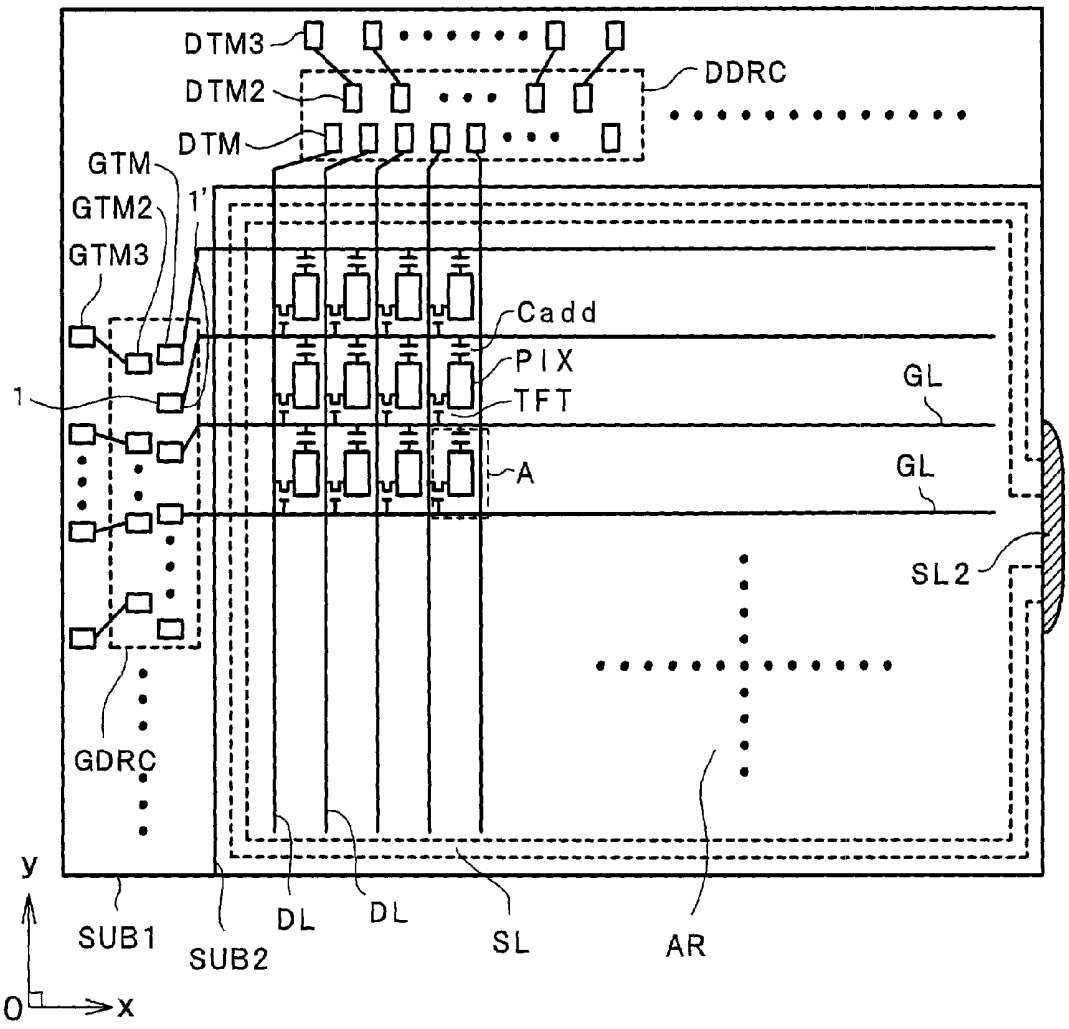


FIG. 1

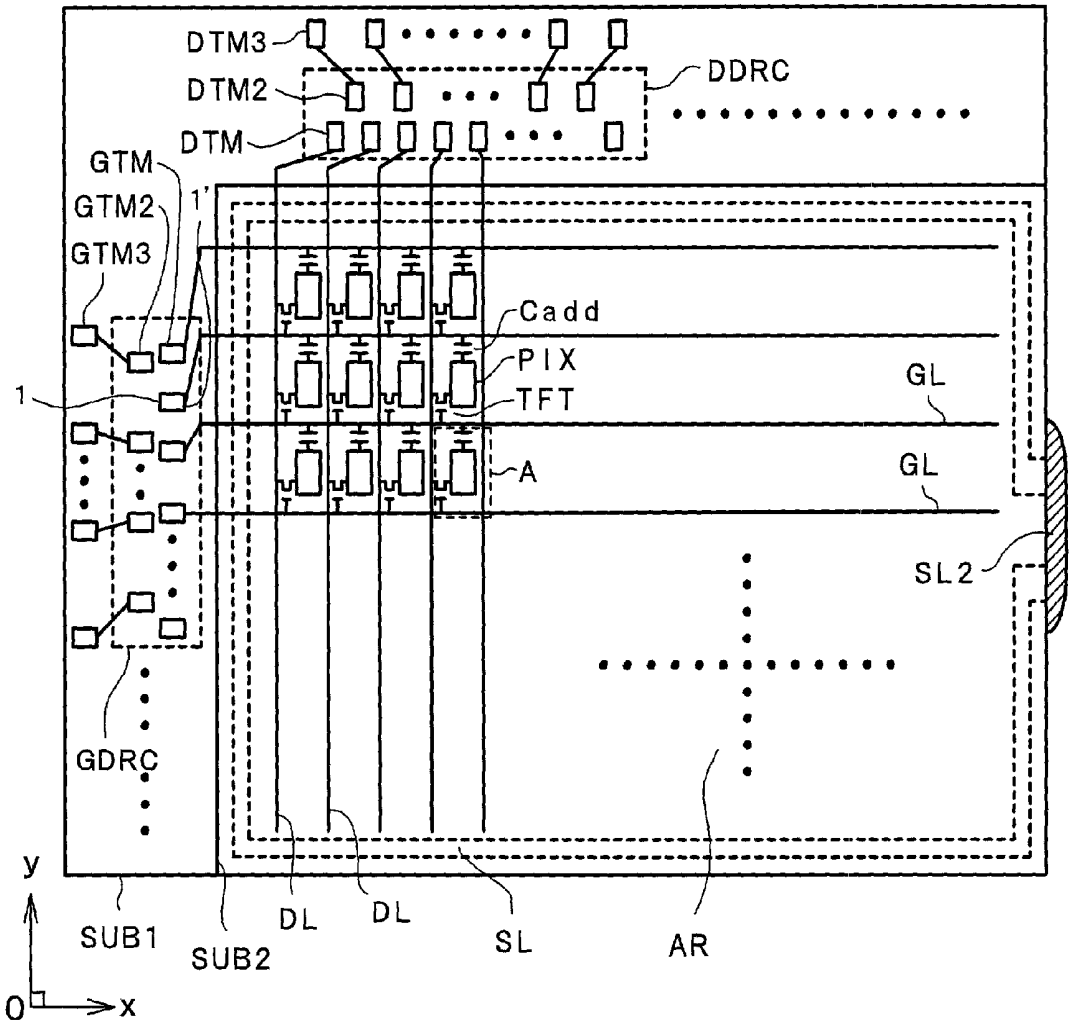

DTM3
DTM2
DTM
DDRC
GTM
GTM2
GTM3
1'
1
Cadd
PIX
TFT
A
GL
GL
SL2
GDRC
y
0
x
SUB1
SUB2
DL
DL
SL
AR

FIG. 2

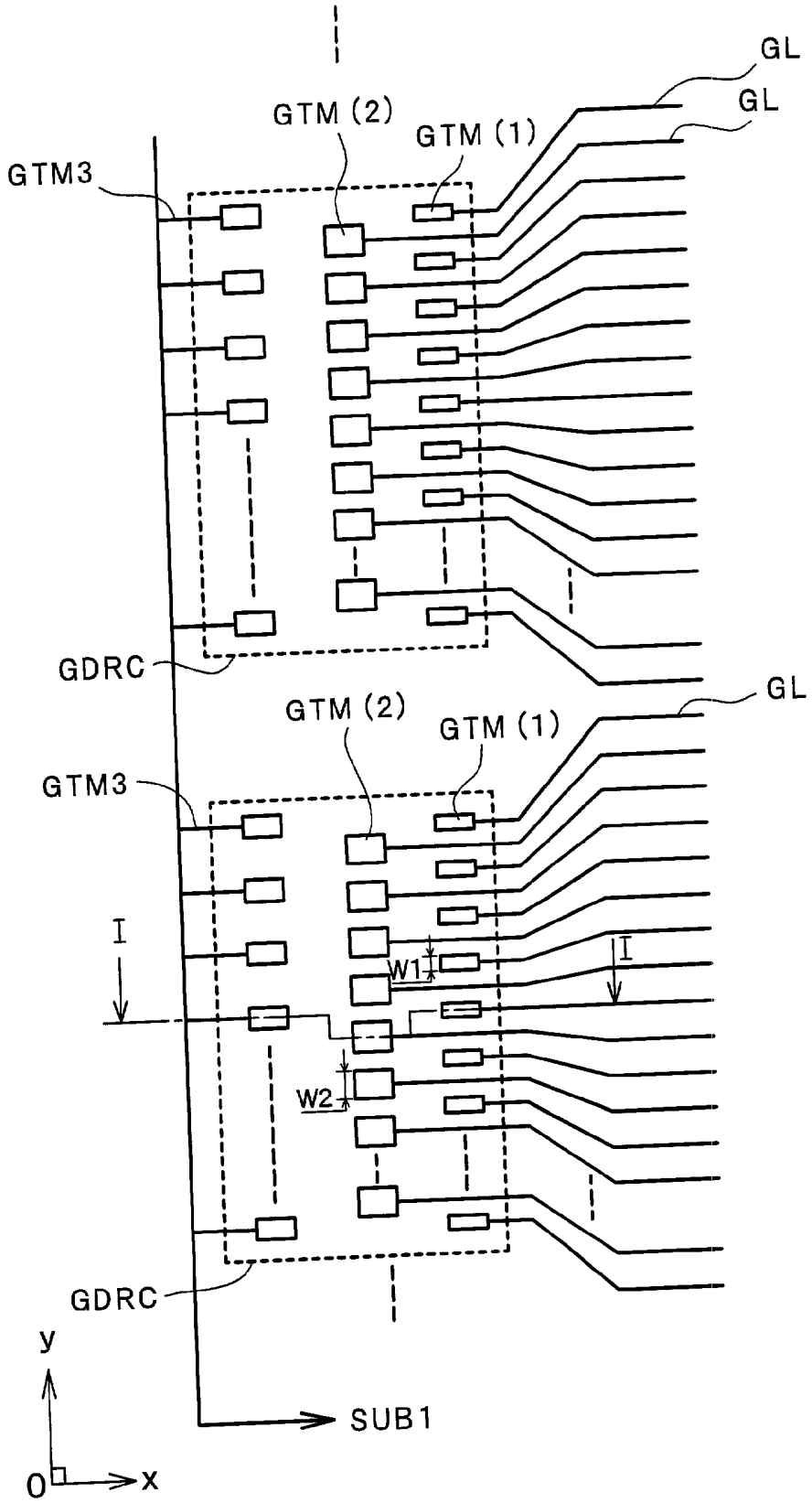

GL
GL
GTM (2)
GTM (1)
GTM3
GDRC
GL
GTM (2)
GTM (1)
GTM3
I
I
W1
W2
GDRC
y
SUB1
0
x

FIG. 3A

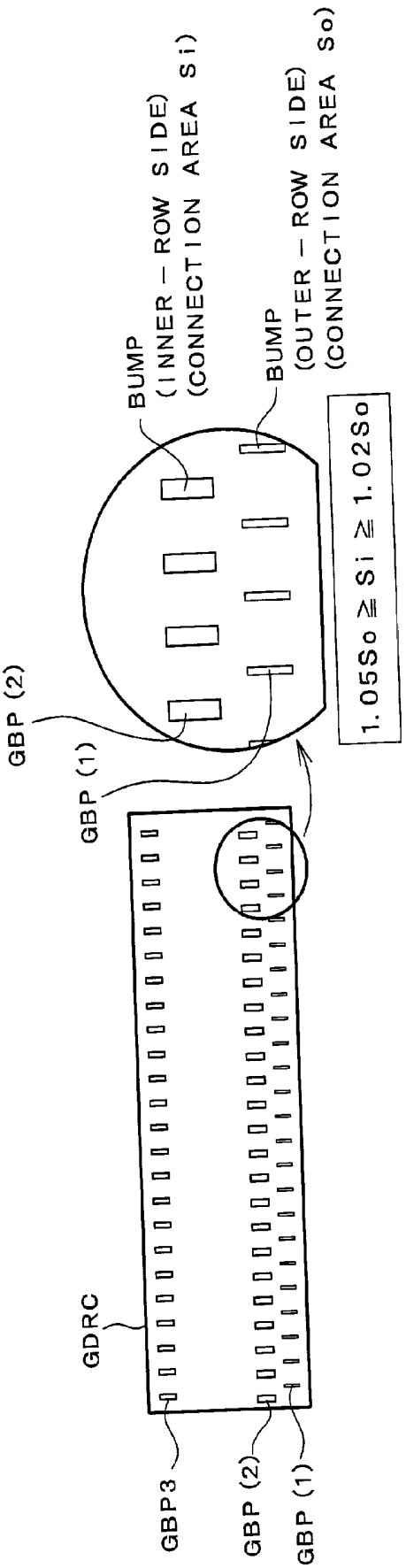

GDRC
GBP3
GBP (2)
GBP (1)
GBP (2)
GBP (1)
BUMP
(INNER – ROW SIDE)
(CONNECTION AREA Si)
BUMP
(OUTER – ROW SIDE)
(CONNECTION AREA So)
1.05So ≧ Si ≧ 1.02So

FIG. 3B

FIG. 4A

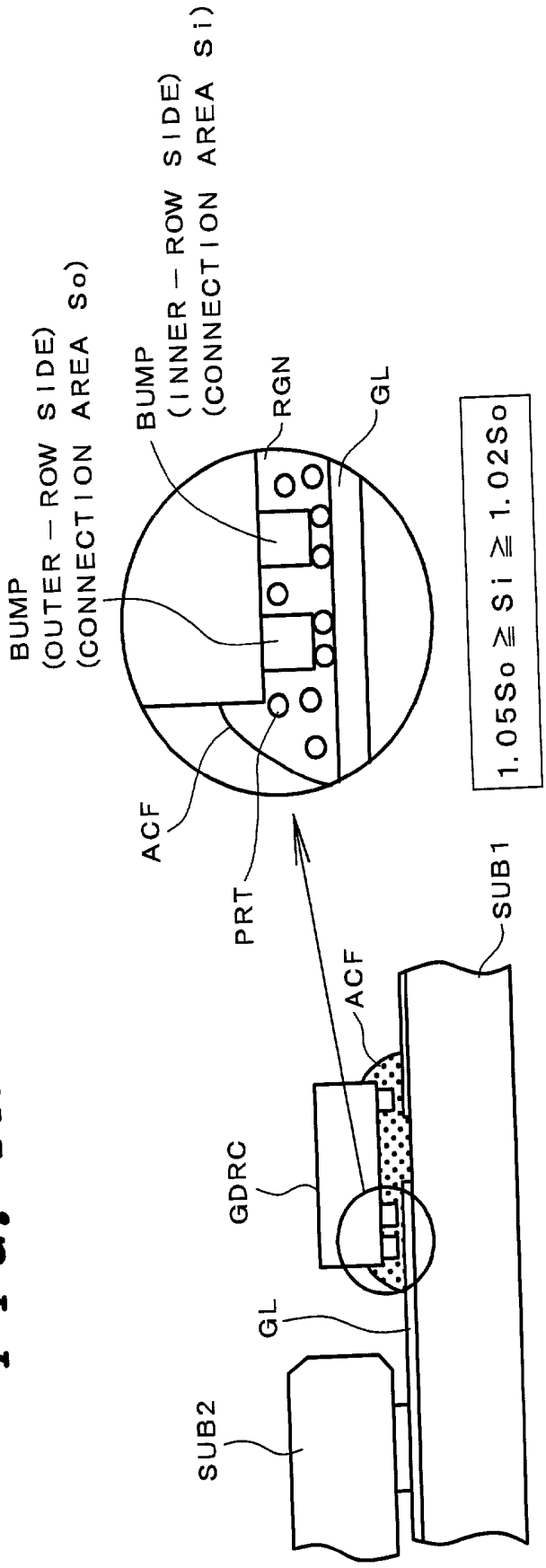

BUMP
(OUTER – ROW SIDE)
(CONNECTION AREA So)
BUMP
(INNER – ROW SIDE)
(CONNECTION AREA Si)
RGN
GL
1.05So ≧ Si ≧ 1.02So
ACF
PRT
ACF
SUB1
GDRC
GL
SUB2

FIG. 4B

FIG. 5A

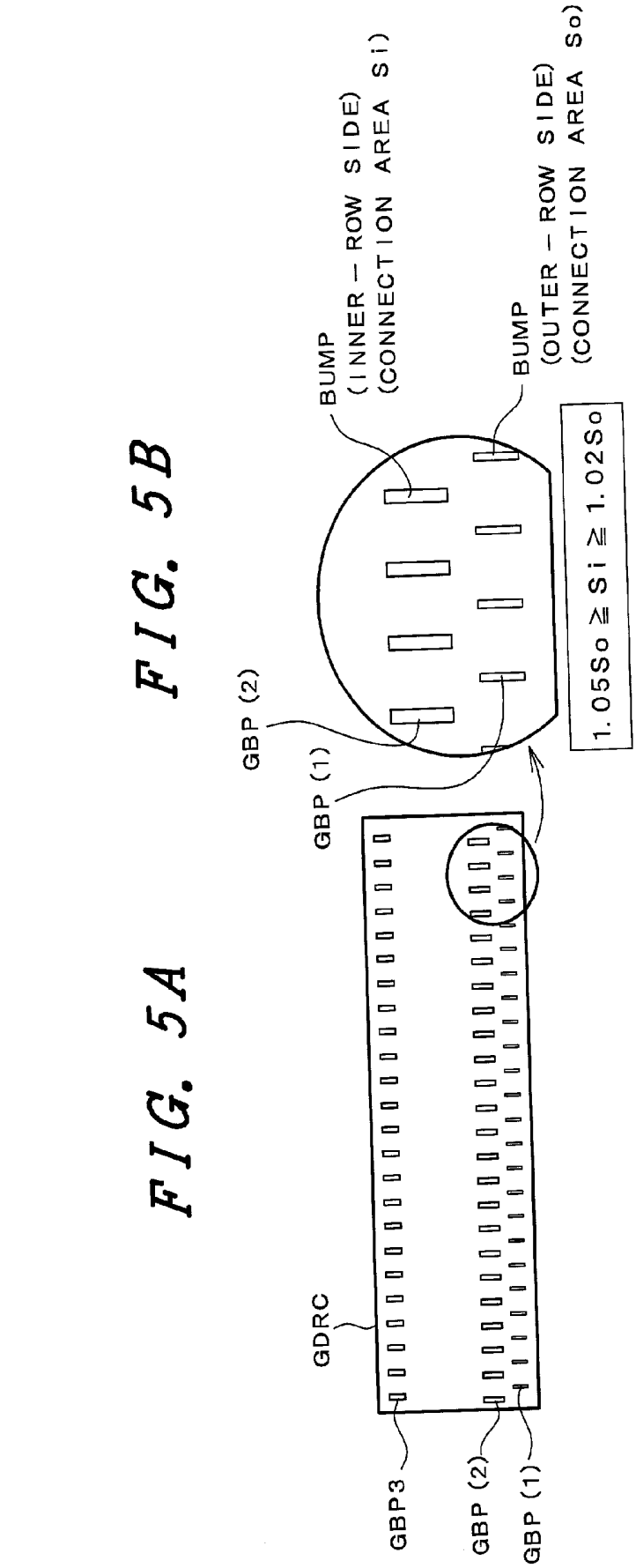

GDRC
GBP3
GBP (2)
GBP (1)

FIG. 5B

BUMP
(INNER – ROW SIDE)
(CONNECTION AREA Si)
BUMP
(OUTER – ROW SIDE)
(CONNECTION AREA So)
GBP (2)
GBP (1)
1.05So ≧ Si ≧ 1.02So

FIG. 6

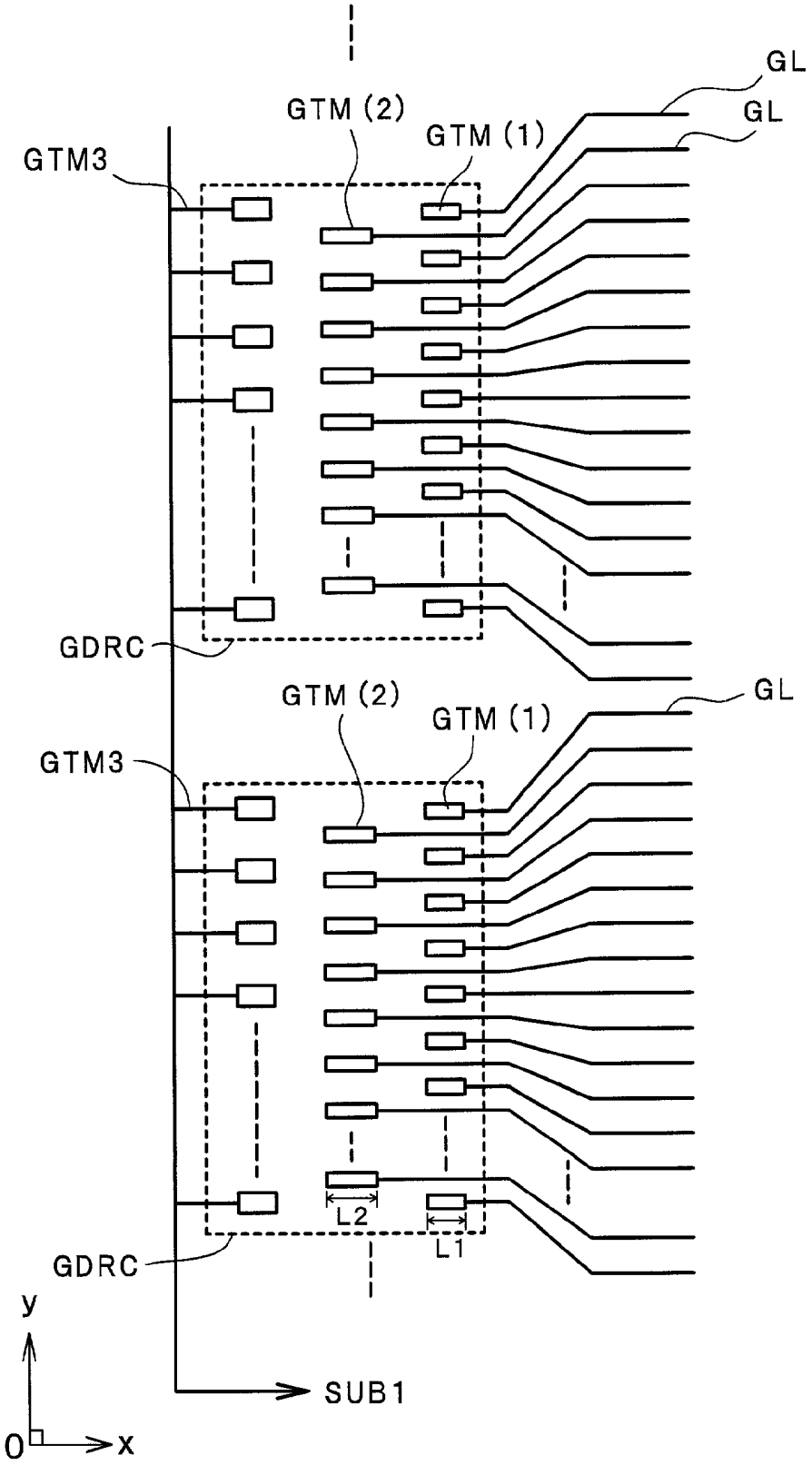


FIG. 7

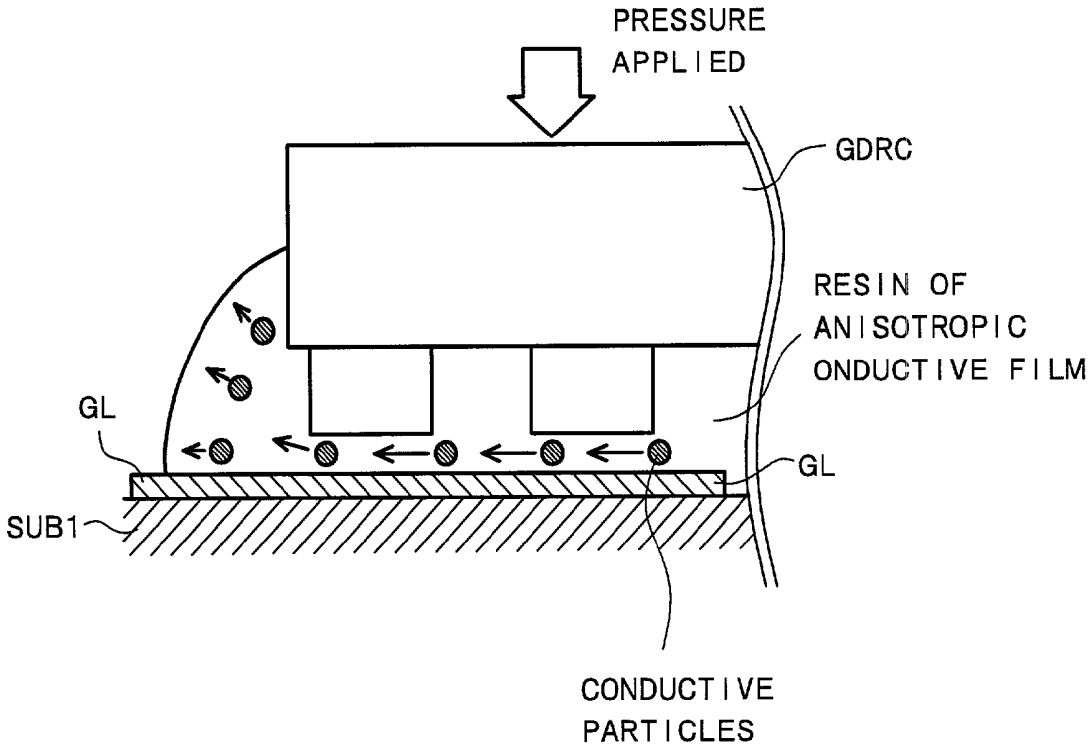

PRESSURE
APPLIED
GDRC
RESIN OF
ANISOTROPIC
ONDUCTIVE FILM
GL
GL
SUB1
CONDUCTIVE
PARTICLES

FIG. 8

Number of ACF particles captured under bumps arranged in two rows and result of area allocation obtained by optimization

Specifications of ACF (Expressed by combination of specifications) resin-diameter of particles density of particles	Number of captured ACF particles under bumps			Change of area by optimization			area difference between inner and outer rows
	inner-row side mi	outer-row side mo	ratio mo/mi	inner-row side Si/S	outer-row side So/S	area ratio So/Si	So/Si-1
resin ① - reference diameter - low	7.72	8.08	104.7%	1.020	0.980	1.041	4.1%
resin ② - reference diameter - reference	8.34	8.65	103.7%	1.016	0.984	1.033	3.3%
resin ② - reference diameter - reference	9.91	10.25	103.4%	1.015	0.985	1.031	3.1%
resin ④ - reference diameter - reference	11.37	11.95	105.1%	1.023	0.977	1.047	4.7%
resin ④ - reference diameter - reference	11.13	11.68	104.9%	1.022	0.978	1.045	4.5%
resin ② - reference diameter - high	13.39	13.69	102.2%	1.010	0.990	1.021	2.1%
resin ③ - reference diameter - high	13.56	13.86	102.2%	1.010	0.990	1.020	2.0%

FIG. 9A (PRIOR ART)

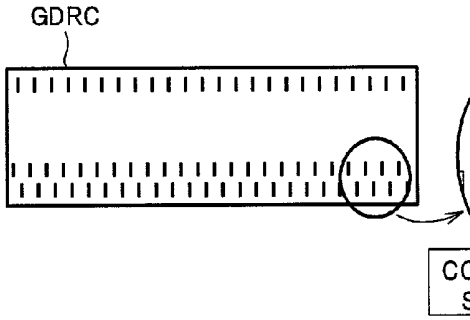


FIG. 9B (PRIOR ART)

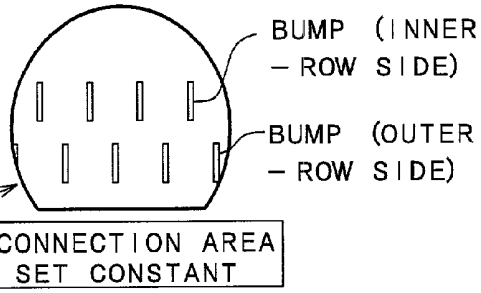


FIG. 10

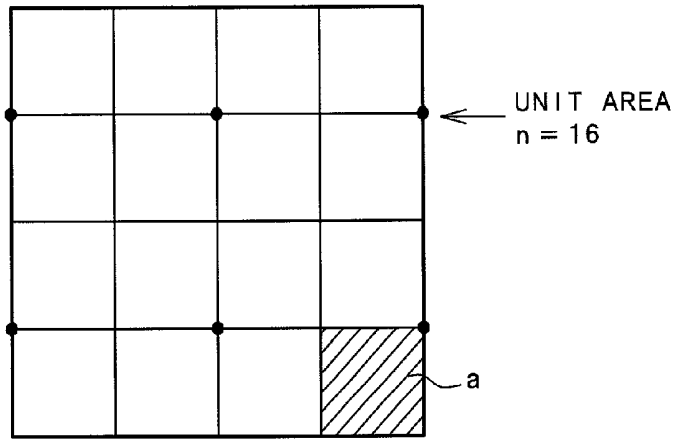
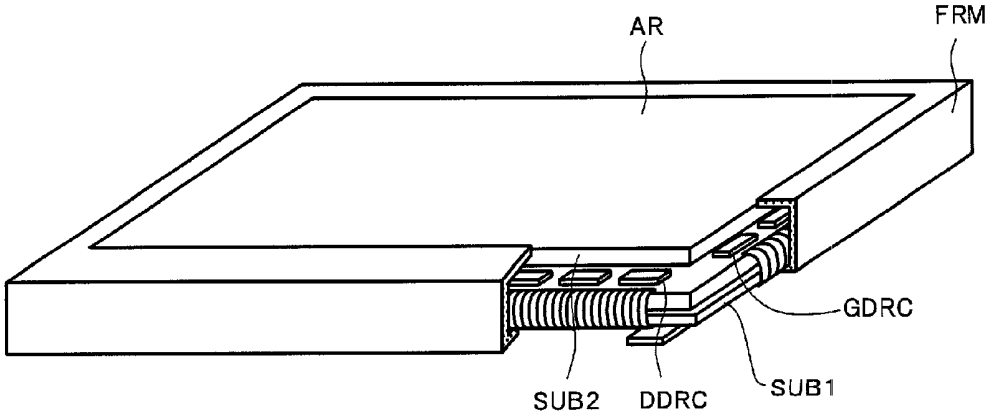


FIG. 11



LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a liquid crystal display, and more particularly, to a liquid crystal display of a so-called active-matrix type.

[0002] The liquid crystal display of this type is provided with a plurality of gate signal lines which are extended in the X direction and are arranged in parallel in the Y direction and a plurality of drain signal lines which are extended in the Y direction and are arranged in parallel in the X direction on a liquid-crystal-side surface of one of two substrates which are arranged to face each other in an opposed manner while inserting liquid crystal therebetween. A region which is surrounded by two neighboring gate signal lines and two neighboring drain signal lines defines a pixel region.

[0003] Each pixel region is provided with a switching element which is driven by scanning signals from one-side gate signal line and a pixel electrode to which video signals are supplied from one-side drain signal line through the switching element.

[0004] On a liquid-crystal-side surface of the other substrate out of a pair of substrates, pixel electrodes which face the pixel electrodes on one substrate in an opposed manner and constitute capacitors are formed.

[0005] By generating an electric field between the pixel electrodes which are respectively formed on two substrates, the light transmittivity of the liquid crystal is controlled.

[0006] Further, on a periphery of the liquid-crystal-side surface of one substrate, a semiconductor integrated circuit (IC chip) which constitutes a scanning signal driving circuit and a semiconductor integrated circuit (IC chip) which constitutes a video signal driving circuit are directly mounted with bump forming surfaces thereof directed downwardly (face down) (COG: Chip On Glass).

[0007] On the substrate on which the IC chips are mounted, signal lines which correspond to the IC chips are extended to positions which face respective output bumps of the IC chips and terminals which are connected with the output bumps are formed on the extended portions or extensions.

[0008] Recently, the liquid crystal displays are requested to meet the further enhancement of the definition thereof. To satisfy this requirement, the number of pixel has been increased and the number of gate signal lines and drain signal lines has been increased correspondingly.

[0009] As bumps (particularly, output bumps) which are connected to the signal lines of the semiconductor integrated circuit, there has been known an arrangement of bumps which has increased the number of bumps, wherein the bumps are constituted of a first group of bumps which are arranged at the signal-line side and a second group of bumps which are arranged at the side remote from the signal lines.

[0010] In the liquid crystal display of a COG type, the semiconductor integrated circuits are fixedly secured to the substrate by way of anisotropic conductive layers and are connected to corresponding respective terminals. Japanese Laid-open Patent Publication 81635/2000 discloses such a technique.

[0011] However, in this case, the connection resistance between the respective bumps which constitutes the second group of bumps and respective terminals connected to these respective bumps becomes larger than the connection resistance between the respective bumps which constitutes the first group of bumps and respective terminals connected to these respective bumps. Accordingly, in a worst case, there arises a possibility that the second group of bumps suffer from the connection failure.

SUMMARY OF THE INVENTION

[0012] The present invention has been made in view of such circumstances and the present invention is able to provide a liquid crystal display which can ensure the connection between semiconductor integrated circuits and signal lines mounted on the liquid crystal display.

[0013] A liquid crystal display according to the present invention is provided with a plurality of signal lines which respectively have connection terminals and a semiconductor chip which is connected to respective terminals of a plurality of signal lines on a liquid-crystal-side surface of one of two substrates which are arranged to face each other while inserting liquid crystal therebetween. The semiconductor chip includes a plurality of bumps and a plurality of these bumps are connected to corresponding respective terminals of respective signal lines through the anisotropic conductive layer. Further, a plurality of these bumps constitute at least groups of bumps arranged in two rows. The bumps include a first group of bumps which are arranged at a side close to an end portion of the semiconductor chip and a second group of bumps which are arranged at a side remote from the end portion, wherein a contact area between the respective bumps of the second group of bumps and the signal lines is set larger than a contact area between the respective bumps of the first group of bumps and the signal lines.

[0014] The liquid crystal display according to the present invention can reduce the resistance value at the contact portion between the respective bumps of the second group of bumps and the signal lines to a level substantially equal to the resistance value at the contact portion between the respective bumps of the first group of bumps and the signal lines.

[0015] Accordingly, it becomes possible to eliminate a phenomenon that the connection resistance between the respective bumps which constitute the second group of bumps and the signal line which are connected to these bumps is increased or the connection failure occurs in a worst case.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **FIG. 1** is an overall equivalent circuit of a liquid crystal display according to the present invention.

[0017] **FIG. 2** is a plan view of a surface of a transparent substrate on which IC chips are mounted.

[0018] **FIG. 3A** is a front view of a face on which bumps of a semiconductor integrated circuit mounted on the liquid crystal display according to the present invention are formed.

[0019] **FIG. 3B** is a partial enlarged view of **FIG. 3A**.

[0020] **FIG. 4A** is a cross-sectional view taken along a line I-I of **FIG. 2**. **FIG. 4B** is a partial enlarged view of **FIG. 4A**.

[0021] **FIG. 5A** is a constitutional view showing other embodiment of the semiconductor integrated circuit mounted on the liquid crystal display according to the present invention and is also a plan view of a face on which bumps are formed.

[0022] **FIG. 5B** is a partial enlarged view of **FIG. 5A**.

[0023] **FIG. 6** is a plan view of a surface of a transparent substrate on which IC chips are mounted.

[0024] **FIG. 7** is a cross-sectional view for explaining the movement of conductive particles when the IC chip is bonded to the transparent substrate under pressure.

[0025] **FIG. 8** is a comparison chart of a bonding area between bumps and connection terminals and the number of conductive particles.

[0026] **FIG. 9A** is a front view of a face on which bumps of a semiconductor integrated circuit mounted on a conventional liquid crystal display are formed.

[0027] **FIG. 9B** is a partial enlarged view of **FIG. 9A**.

[0028] **FIG. 10** is a reference view which is served for obtaining an approximation formula of the distribution of the number of particles on bumps.

[0029] **FIG. 11** is a perspective view with a part in cross section which shows one embodiment of the liquid crystal display according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] Preferred embodiments of a liquid crystal display according to the present invention are explained in conjunction with attached drawings hereinafter.

Embodiment 1

Equivalent Circuit

[0031] **FIG. 1** is an equivalent circuit diagram showing one embodiment of a liquid crystal display according to the present invention. The drawing is the circuit diagram which is drawn corresponding to an actual geometric arrangement.

[0032] One transparent substrate SUB1 is arranged to face the other transparent substrate SUB2 in an opposed manner while inserting liquid crystal therebetween.

[0033] On a liquid-crystal-side surface of the transparent substrate SUB1, a plurality of gate signal lines GL which are extended in the X direction and are arranged in parallel in the Y direction and a plurality of drain signal lines DL which are insulated from the gate signal lines GL and are extended in the Y direction and are arranged in parallel in the X direction are formed. A rectangular region which is surrounded by two neighboring gate signal lines and two neighboring drain signal lines constitutes a pixel region. A display region AR is constituted of a mass of these pixel regions.

[0034] On each pixel region, a thin film transistor TFT which is driven by the supply of scanning signals (voltage) from one-side gate signal line GL and a pixel electrode PIX to which video signals (voltage) are supplied from one-side drain signal line DL through the thin film transistor TFT are formed.

[0035] Further, a capacitive element Cadd is formed between the pixel electrode PIX and the other-side gate signal line GL which is disposed close to the above-mentioned one-side gate signal line GL. This capacitive element Cadd can store the video signals supplied to the pixel electrode PIX for a long time when the thin film transistor TFT is turned off.

[0036] The other transparent substrate SUB2 is provided with a counter electrode CT (not shown in the drawing) on a liquid-crystal-side surface thereof, wherein the counter electrode CT is provided commonly for the respective pixel regions. An electric field is generated between the pixel electrodes PIX and the counter electrode CT which is arranged to face the pixel electrodes PIX in an opposed manner while interposing the liquid crystal therebetween. The light transmittivity of the liquid crystal between respective electrodes is controlled in response to this electric field.

[0037] One ends of respective gate signal lines GL are extended toward one side (left side in the drawing) of the transparent substrate SUB1 and terminal portions GTM are formed at extensions of the respective gate signal lines GL. Bumps of an IC chip GDRC which is constituted of a vertical scanning circuit are connected to the terminal portions GTM.

[0038] Further, one ends of respective drain signal lines DL are extended toward one side (upper side in the drawing) of the transparent substrate SUB1 and terminal portions DTM are formed at extensions of the respective drain signal lines DL. Bumps of a semiconductor integrated circuit DDRC which is constituted of a video signal driving circuit are connected to the terminal portions DTM.

[0039] IC chips GDRC, DDRC per se are respectively directly mounted on the transparent substrate SUB1 thus constituting a so-called COG (Chip-On-Glass) system.

[0040] Respective bumps provided at the input sides of the IC chips GDRC, DDRC are also respectively connected to terminal portions GTM2, DTM2 which are formed on the transparent substrate SUB1. These respective terminal portions GTM2, DTM2 are connected to terminal portions GTM3, DTM3 which are respectively arranged at a peripheral portion of the transparent substrate SUB1 closest to an end surface of the transparent substrate SUB1 out of peripheral portions of the transparent substrate SUB1.

[0041] The transparent substrate SUB2 is arranged to face the transparent substrate SUB1 such that the transparent substrate SUB2 does not cover the area on which the semiconductor integrated circuit is mounted. That is, the area of the transparent substrate SUB2 is made smaller than the area of the transparent substrate SUB1.

[0042] The transparent substrate SUB2 is fixedly secured to the transparent substrate SUB1 using a sealing agent SL which is formed on a periphery of the transparent substrate SUB2. The sealing agent SL also has a function of sealing the liquid crystal between the transparent substrates SUB1 and SUB2.

[0043] As shown in **FIG. 10**, the liquid crystal display having such a constitution is covered with a frame FRM having an opening in a display portion AR thus constituting a liquid crystal display module.

Constitution in the Vicinity of the Semiconductor Integrated Circuit

[0044] **FIG. 2** is a plan view which shows a specific constitution on the surface of the transparent substrate SUB1 in the vicinity of the IC chip GDRC which is mounted on the transparent substrate SUB1.

[0045] In **FIG. 2**, with respect to respective gate signal lines GL which are arranged in the Y direction, the neighboring gate signal lines GL are formed into a group. The distance between the bumps of the IC chip GDRC is set smaller than the distance between respective gate signal lines GL in the display portion AR and hence, respective gate signal lines GL of each group are converged with each other in the vicinity of the region on which the IC chip GDRC is mounted. The terminals GTM are formed at positions which face the respective output bumps of the IC chip GDRC.

[0046] The terminals GTM which are connected to respective output bumps of the IC chip GDRC are constituted of a first group of terminals and a second group of terminals which are arranged in rows.

[0047] Respective terminals GTM(1) which constitute the first group of terminals are positioned at an image-display-region side (also referred to as "outer row side" as will be explained later), while respective terminals GTM(2) which constitute the second group of terminals are positioned at a side remote from the image-display-region side (also referred to as "inner row side" as will be explained later).

[0048] When the IC chip GDRC is mounted on the substrate, the first group of terminals is positioned in the vicinity of the end portion of the IC chip and the second group of terminals is positioned closer to the center of the IC chip than the first group of terminals.

[0049] Further, each terminal GTM(2) is positioned between respective terminals GTM(1) and respective terminals GTM which are constituted of respective terminals GTM(2) and respective terminals GTM(1) are arranged in a so-called staggered pattern.

[0050] Accordingly, each gate signal line GL which is connected to the terminal GTM(2) is formed such that the gate signal line GL is positioned between the gate signal lines GL which are connected to the terminals GTM(1) and runs between the neighboring terminals GTM(1).

[0051] Further, respective terminals GTM(2) which constitute the second group of terminals have a width **W2** thereof made larger than a width **W1** of the respective terminals GTM(1) which constitute the first group of terminals.

[0052] With respect to the terminals GTM(2), the gate signal line GL is not formed between these terminals GTM(2) and hence, the terminals GTM(2) can make the width **W2** thereof larger than the width **W1** of the terminals GTM(1).

[0053] The reason that the width **W2** of the terminals GTM(2) is set large is to make the area of each terminal GTM(2) which faces the corresponding output bump of the IC chip GDRC larger than the area of each terminal GTM(1) which faces the corresponding output bump of the IC chip GDRC. For example, in this embodiment, the area of each terminal GTM(1) which faces the corresponding output bump of the IC chip GDRC is 2400 μm^2. On the other hand, the area of each terminal GTM(2) which faces the corresponding output bump of the IC chip GDRC is set larger than the area of each terminal GTM(1) which faces the corresponding output bump of the IC chip GDRC by 2 to 5%.

[0054] **FIG. 3A** is a plan view which shows a bump forming surface of the IC chip GDRC and **FIG. 3B** is an enlarged view of a portion circled by a solid line indicated in **FIG. 3A**.

[0055] Output bumps GBP of the IC chip GDR C are constituted of the first group of bumps and the second group of bumps which are arranged in rows.

[0056] The respective bumps GBP(1) which constitute a first group of bumps are positioned corresponding to the terminals GTM(1) of the gate signal lines GL, while the respective bumps GBP(2) which constitute a second group of bumps are positioned corresponding to the terminals GTM(2) of the gate signal lines GL.

[0057] The first group of bumps is arranged in the vicinity of the long-side end portion of the rectangular IC chip GDRC and the second group of bumps is arranged closer to the center of the IC chip GDRC than the first group of bumps.

[0058] In the same manner as the arrangement of the terminals GTM, each bump GBP(2) is positioned between respective bumps GBP(1) and respective bumps GBP which are constituted of respective bumps GBP(2) and respective bumps GBP(1) are arranged in a so-called staggered pattern.

[0059] A width of the bumps GBP(2) which constitute the second group of bumps is set larger than a width of the bumps GBP(1) which constitute the first group of bumps. The reason that the width of the bumps GBP(2) is set larger than the width of the bumps GBP(1) is to make the area of each second bump GBP(2) which faces the terminal GTM(2) larger than the area of each first bump GBP(1) which faces the terminal GTM(1).

[0060] In this embodiment, assume the area of the bump GBP(1) of the IC chip GDRC which faces the corresponding terminal GTM(1) as So and the area of the bump GBP(2) of the IC chip GDRC which faces the corresponding terminal GTM(2) as Si, a following formula (1) is established.

$$1.05So >> Si >> 1.02So \quad (1)$$

[0061] **FIG. 4A** is a cross-sectional view showing a case in which the IC chip GDRC is mounted on the transparent substrate SUB1 and corresponds to a cross-sectional view taken along a line I-I of **FIG. 2**. Further, **FIG. 4B** is an enlarged view at a portion circled by a solid line in **FIG. 4A**.

[0062] An anisotropic conductive film ACF is interposed between the IC chip GDRC and the transparent substrate SUB1. The anisotropic conductive film ACF is formed of a resin film RGN in which a large number of conductive particles PRT are scattered. In this embodiment, the aniso-

tropic film ACF in which the conductive particles PRT are scattered at the rate of 30 k pieces/mm^2 is used.

[0063] By heating the anisotropic conductive film ACF and pressing the IC chip GDRC to the transparent substrate SUB1, the IC chip GDRC is fixedly secured to the transparent substrate SUB1 and respective bumps GBP on the IC chip GDRC and the terminals GTM on the transparent substrate SUB1 are electrically connected with each other through the conductive particles in the inside of the anisotropic conductive film ACF.

[0064] When the IC chip GDRC is pressed to the transparent substrate SUB1, the flow of the conductive particles PRT is generated in the inside of the resin film RGN of the anisotropic conductive film ACF.

[0065] In this embodiment, the number of the conductive particles PRT which are interposed between each bump GBP(2) of the group of bumps at the inner-row side of the IC chip GDRC and the terminal GTM(2) which is connected to the bump GBP(2) can be set substantially equal to the number of the conductive particles PRT which are interposed between each bump GBP(1) of the group of bumps at the outer-row side of the IC chip GDRC and the terminal GTM(1) which is connected to the bump GBP(1). Accordingly, the connection resistance between the terminal GTM(2) and the bump GBP(2) can be made substantially equal to the connection resistance between the terminal GTM(1) and the bump GBP(1).

[0066] In the above-mentioned embodiment, the width of the bumps GBP(2) at the inner-row side out of the output bumps GBP of the semiconductor integrated circuit GDLC and the terminals GTM(2) which face the bumps GBP(2) is set larger than the width of the bumps GBP(1) at the outer-row side out of the output bumps GBP of the semiconductor integrated circuit GDLC and the terminals GTM(1) which face the bumps GBP(1).

[0067] **FIG. 5A** is a constitutional view showing another embodiment of the IC chip which is mounted on the liquid crystal display according to the present invention and is a front view of a face on which bumps are formed. **FIG. 5B** is a partial enlarged view of **FIG. 5A**. **FIG. 6** is a plan view of the surface of the transparent substrate on which IC chips shown in **FIG. 5A** are mounted.

[0068] As shown in **FIG. 5**A, **FIG. 5**B and **FIG. 6, a** length L2 of the bumps GBP(2) at the inner-row side and the terminals GTM(2) which face the bumps GBP(2) may be set larger than a length L1 of the bumps GBP(1) at the outer-row side and the terminals GTM(1) which face the bumps GBP(1).

[0069] Further, although the above-mentioned embodiment has been explained with respect to the output bumps GBP of the IC chip GDRC and the terminals BTM of the gate signal lines GL which are connected to the output bumps GBP, the above-mentioned constitution is also applicable to the output bumps of the IC chip DDRC and the terminals DTM of the drain signal lines DL which are connected to the output bumps.

Advantageous Effect Obtained Based on Theory

[0070] As shown in **FIG. 7**, in the mounting based on the COG system, the pressure is applied from the back-surface side of the IC chip GDRC so as to push out an extra amount of resin which is present between the transparent substrate SUB1 and the IC chip GDRC whereby the IC chip GDRC is bonded to the substrate SUB1 under pressure and the bumps are electrically connected to the gate terminals.

[0071] In such a case, the reason that the conductive particles PRT are not captured at the inner-row side is considered to be derived from the flow of the resin at the time of bonding under pressure. That is, in the pressure-bonding process, the resin present in the vicinity of the bumps of the inner-row side is more liable to be pushed uniformly on the surface than the bumps of the outer-row side so that the particles flow parallel to the surface of the transparent substrate SUB1.

[0072] However, at the side of the bumps of the outer-row side which is close to the end surface of the chip, the flow of the particles is interrupted by the resin which is discharged to the end surface so that the flow speed of the particle becomes slow. As a result, compared to the resin which enters below the bumps of the IC chip GDRC, the resin which departs from the position below the IC chip GDRC becomes small transitionally and hence, it is considered that the conductive particles which are sandwiched and remain between the bumps of the IC chip GDRC and the transparent substrate SUB1 are increased in number at the bumps of the outer-row side.

[0073] Accordingly, as explained in the above-mentioned embodiment, by increasing the bonding area of the bump GBP(2) of the inner-row side and the terminal GTM(2), the number of the conductive particles captured in the inside of the bonding region can be made substantially equal to the number of the conductive particles captured in the inside of the bonding region of the bump GBP(1) of the outer-row side and the terminal GTM(1).

[0074] **FIG. 9A** is a front view of a face on which bumps of a semiconductor integrated circuit mounted on a conventional liquid crystal display are formed. **FIG. 9B** is a partial enlarged view of **FIG. 9A**.

[0075] With respect to a conventional structure in which bumps are arranged in two rows, according to the actually measured data, the number of particles is different between the inner row and the outer row and a tendency that, as the mean value, the number of captured particles at the outer-row side is greater than the number of captured particles at the inner-row side by 2 to 5% is recognized.

[0076] Further, the frequency distribution of the captured particles takes the Poisson distribution theoretically and hence, assuming the mean value of the captured particles remaining under the bump as "m", the occurrence probability of the bumps where the particles are not captured can be calculated by exp (−m).

[0077] As a result, assuming that the total area occupied by the inner-row bumps and the outer-row bumps is constant and the mean value of the captured particles is changed in proportion to the change of the bump area, the ratio of the area of the inner-row bumps with respect to the outer-row bumps where the occurrence probability of the bumps which do not capture the particles becomes lowest can be calculated by a following equation (2).

$$F=\exp(-mi')/2+\exp(-mo')/2 \quad (2)$$

[0078] wherein, mi'=Si/S×mi (equation expressing the relationship between the number of captured particles and area of bumps), mo'=So/S×mo (equation expressing the relationship between the number of captured particles and area of bumps), Si+So=2S (condition to make the total area of bumps constant), dF/dSi=0 (condition for optimizing the total area of bumps).

[0079] Further, S; area of bumps which is not optimized (inner-row area and outer-row are being equal), mi; mean captured number of particles PRT captured by inner-row bumps (actually measured data), mo; mean captured number of particles PRT captured by outer-row bumps (actually measured data), Si; area of inner-row bumps which is optimized, So; area of outer-row bumps which is optimized, mi'; mean captured number of particles PRT captured by inner-row bumps after optimizing area (estimated value), mo'; mean captured number of particles PRT captured by outer-row bumps after optimizing area (estimated value), F; estimated occurrence rate of bumps with no particles (per one bump) while assuming the mean number of captured particles by inner-row bumps as mi' and the mean number of captured particles by outer-row bumps as mo'.

[0080] Then, the result obtained by carrying out the equation (2) based on respective measured data is shown in **FIG. 8**.

[0081] Seven kinds of specifications of the anisotropic conductive films are described in **FIG. 8**. These anisotropic conductive films differ from each other in the specification of the resin, the diameter of particles, the density of particles in the film. The total area of bumps is set constant throughout these anisotropic conductive films.

[0082] When the area difference ((So/Si)−1) is less than 2%, the number of captured particles in the inner-row bump portions was smaller than the number of captured particles in the outer-row bump portions and hence, the connection resistance of the inner-row bump portions became higher than the connection resistance of the outer-row bump portions. On the other hand, when the area difference exceeds 5%, the connection resistance of the outer-row bump portions became higher than the connection resistance of the inner-row bump portions. Based on such measured data, the optimal value was obtained when the area difference is set to a range of 2 to 5%.

[0083] The approximate equation of the distribution of the number of particles on bumps can be calculated as follows.

[0084] Assuming the population mean density of particles per unit area after pressure bonding as "n" (pieces/mm^2) and the area of a small region when the unit area is divided in n parts as "a", the probability that the particles are present in the small region is "a". Since the probability P(r) that r pieces of regions which include particles are present when n piece of the small regions are sampled follows the binominal distribution, a following equation is established.

$$P(r)=nCr\cdot a^{r}\cdot(1-a)^{(n-r)} \quad (3)$$

[0085] This equation is also applicable to a small region "b" which has the larger area than "a".

[0086] That is, a following equation (4) is also established.

$$P(r)=nCr\cdot b^{r}\cdot(1-b)^{(n-r)} \quad (4)$$

[0087] In this case, the mean value becomes nb and the dispersion σ^2 becomes nb(1−b).

[0088] When "n" is large or "b" is extremely small, the equation (3) can be approximated by the Poisson distribution and hence, a following equation (5) can be obtained.

$$P(r)=(nb)^{r}\cdot e^{-(nb)}/r! \quad (5)$$

[0089] Since nb is the mean number of particles in the small region, by setting nb as nb=m, the equation (5) can be approximated by a following equation (6).

$$P(r)=m^{r}\cdot e^{-m}/r! \quad (6)$$

[0090] In this case, the dispersion σ^2 becomes a σ^2=m and hence, the probability can be expressed with only one variable m.

[0091] As an application example of the Poisson distribution, the number of bacteria within a visual field of a microscope or defective products among products produced on a mass production basis and the like are known.

[0092] In the above-mentioned embodiments, the liquid crystal display which is provided with the IC chip having groups of bumps of two rows at one side thereof has been explained. With respect to a liquid crystal display which is provided with an IC chip having groups of bumps of three or more rows at one side, the bonding area of a group of bumps which is closest to the end portion of the IC chip is minimized and the bonding area of the bumps is increased as the groups of bumps are moved away from the end portion of the IC chip.

[0093] As can be clearly understood from the above-mentioned explanation, according to the liquid crystal display of the present invention, the reliable connection between the mounted semiconductor integrated circuit and the signal lines can be obtained.

What is claimed is:

1. A liquid crystal display including respective signal lines which are extended in one direction and are arranged in parallel in a direction which intersect one direction and a semiconductor chip which is mounted on one-end sides of the signal lines with a bump forming surface thereof directed downwardly on a liquid-crystal-side surface of one of substrates which are arranged to face each other while inserting liquid crystal therebetween,

the improvement being characterized in that respective output bumps of the semiconductor chip are connected to the corresponding signal lines through an anisotropic conductive layer, and the respective output bumps include a first group of output bumps which are arranged at a side close to an end portion of the semiconductor chip and a second group of output bumps which are arranged at a side remote from the end portion of the semiconductor chip, and area of respective bumps of the second group of output bumps which face the signal lines in an opposed manner is set larger than area of respective bumps of the first group of output bumps which face the signal lines in an opposed manner.

2. A liquid crystal display according to claim 1, wherein the respective bumps of the first group of output bumps and of the second group of output bumps are arranged in a staggered manner.

3. A liquid crystal display according to claim 1, wherein the width of the respective bumps of the second group of output bumps is set larger than the width of the respective bumps of the first group of output bumps.

4. A liquid crystal display according to claim 1, wherein the length of the respective bumps of the second group of output bumps is set larger than the length of the respective bumps of the first group of output bumps.

5. A liquid crystal display according to claim 1, wherein a following relationship is established when the area of respective bumps of the second group of output bumps is set as Si and the area of respective bumps of the first group of output bumps is set as So.

$$1.05So>>Si>>1.02So$$

6. A liquid crystal display according to claim 1, wherein the area of respective bumps of the second group of output bumps is made larger than the area of respective bumps of the first group of output bumps by 2 to 5%.

7. A liquid crystal display according to claim 1, wherein the liquid crystal display defines respective regions which are surrounded by gate signal lines extended in the X direction and arranged in parallel in the Y direction and drain signal lines extended in the Y direction and arranged in parallel in the X direction as pixel regions on the liquid-crystal-side surface of one substrate,

the liquid crystal display further includes switching elements which are operated in response to scanning signals from the one-side gate signal lines and pixel electrodes to which video signal are supplied from the one-side drain signal lines through the switching elements on the pixel regions, and

the signal lines are formed of the gate signal lines and the semiconductor chip is formed of a scanning signal driving circuit.

8. A liquid crystal display according to claim 1, wherein the liquid crystal display defines respective regions which are surrounded by gate signal lines extended in the X direction and arranged in parallel in the Y direction and drain signal lines extended in the Y direction and arranged in parallel in the X direction as pixel regions on the liquid crystal-side surface of one substrate,

the liquid crystal display further includes switching elements which are operated in response to scanning signals from the one-side gate signal lines and pixel electrodes to which video signal are supplied from the one-side drain signal lines through the switching elements on the pixel regions, and

the signal lines are formed of the drain signal lines and the semiconductor chip is formed of a video signal driving circuit.

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专利名称(译)	液晶显示器		
公开(公告)号	US20020080318A1	公开(公告)日	2002-06-27
申请号	US10/022259	申请日	2001-12-20
[标]申请(专利权)人(译)	山手HIROSHI 竹中裕一		
申请(专利权)人(译)	山手HIROSHI 竹中裕一		
当前申请(专利权)人(译)	山手HIROSHI 竹中裕一		
[标]发明人	YAMATE HIROSHI TAKENAKA YUUICHI		
发明人	YAMATE, HIROSHI TAKENAKA, YUUICHI		
IPC分类号	G02F1/13 G02F1/1345 G02F1/1368 G09F9/00 H01L21/60		
CPC分类号	G02F1/1345 G02F1/13452 H01L2224/73204 H01L2224/32225 H01L2224/16225 H01L2924/00 H01L2924/00014 H01L2224/0401		
优先权	2000392324 2000-12-25 JP		
其他公开文献	US6678028		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示器设有各自的信号线和半导体芯片。半导体芯片的各个输出凸块通过各向异性导电层连接到相应的各个信号线。各个输出凸块包括第一组输出凸块和第二组输出凸块，第一组输出凸块布置在靠近信号线的一侧，第二组输出凸块布置在远离信号线的一侧。以相对的方式面对信号线的第二组输出凸块的各个凸块的面积被设置为大于以相对的方式面对信号线的第一组输出凸块的各个凸块的面积。由于这种结构，确保了安装的半导体集成电路和信号线之间的可靠连接。