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(54) LIQUID CRYSTAL DISPLAY DEVICE

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(57) **ABSTRACT**

The invention relates to a liquid crystal display device, comprising a memory that delays a current display data supplied to a liquid crystal panel by one display period, and a reference table memory that holds a reference data containing multiple reference values determined by the current display data and a delayed displayed data. Here, the reference table memory has a compensation signal data written in advance, which substantially completes an optical response of the liquid crystal panel within the one display period. The liquid crystal display device supplies the inputted display data after having been converted always into a compensated signal level data to the liquid crystal panel, thus achieving a high-speed response that is completed within the one display period.

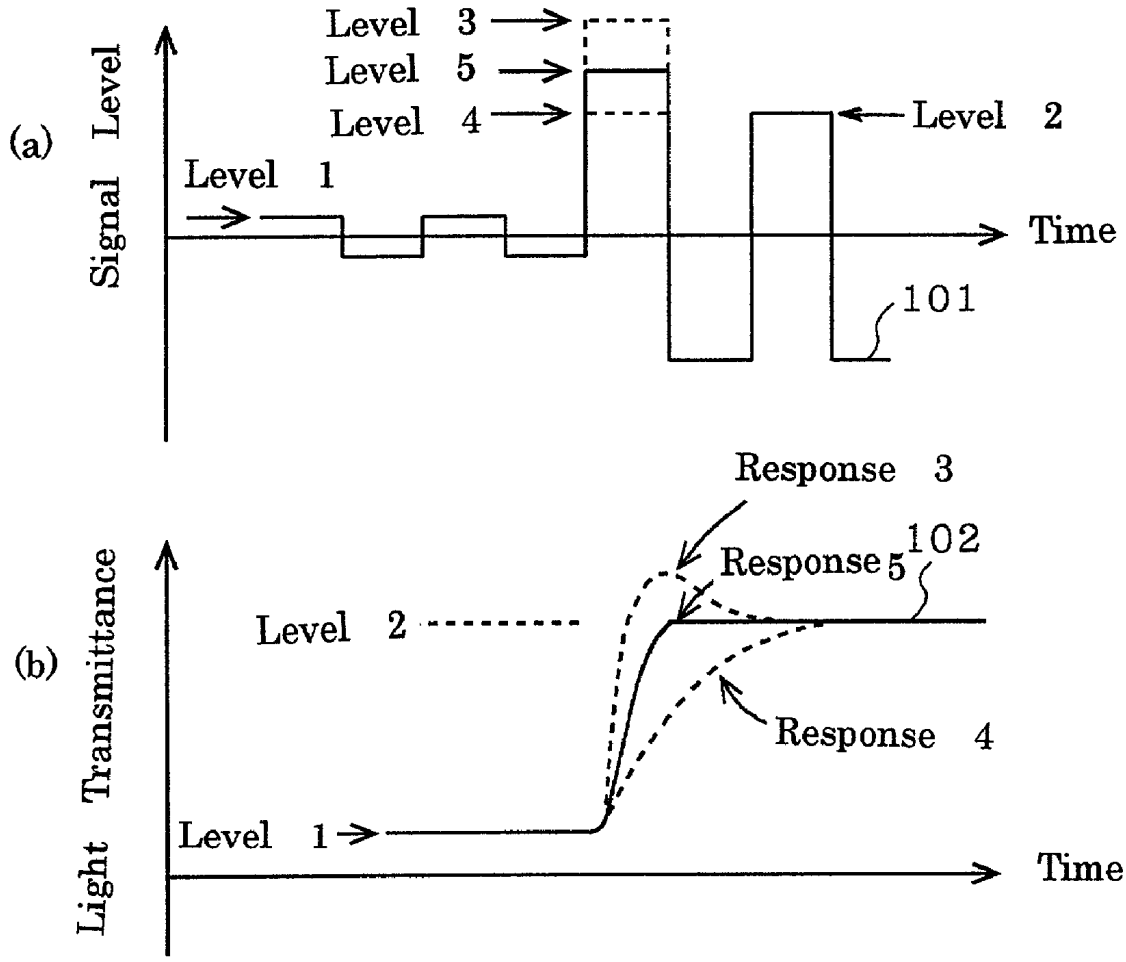


FIG. 1

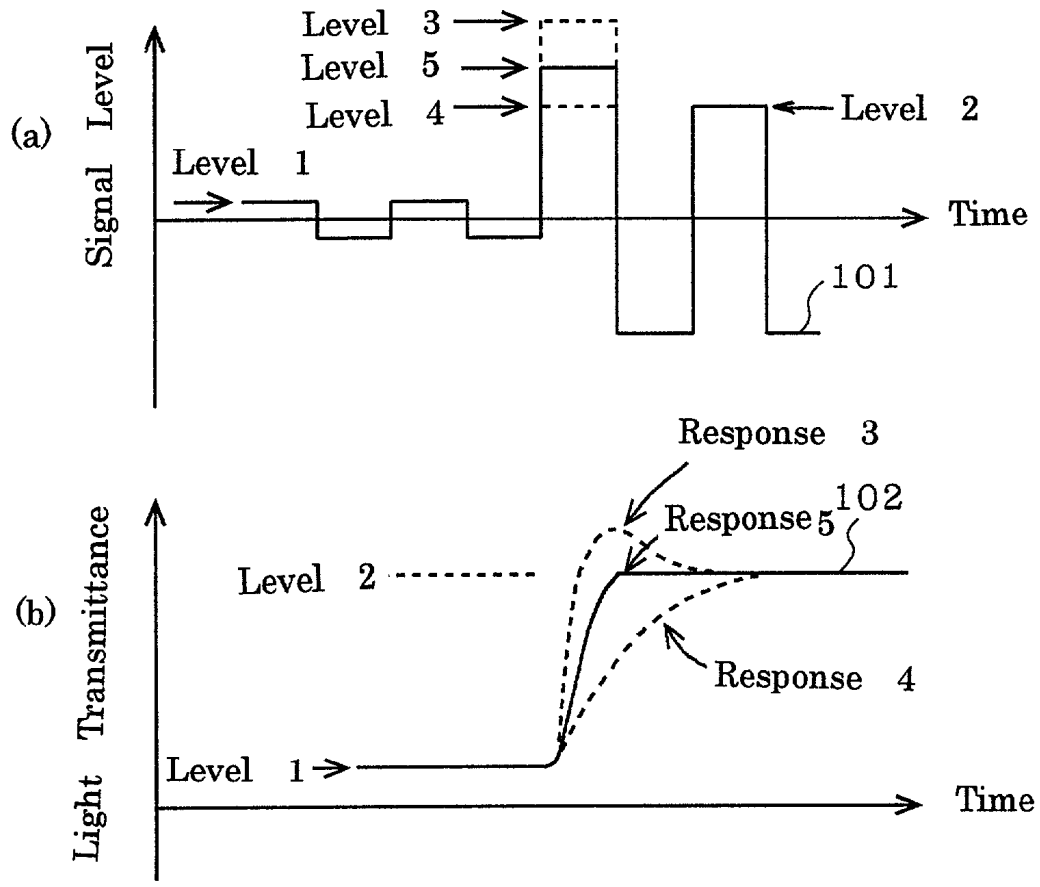

(a)
Signal Level
Level 3
Level 5
Level 4
Level 2
Level 1
Time
101
(b)
Light Transmittance
Response 3
Response 5
102
Level 2
Response 4
Level 1
Time

FIG. 5

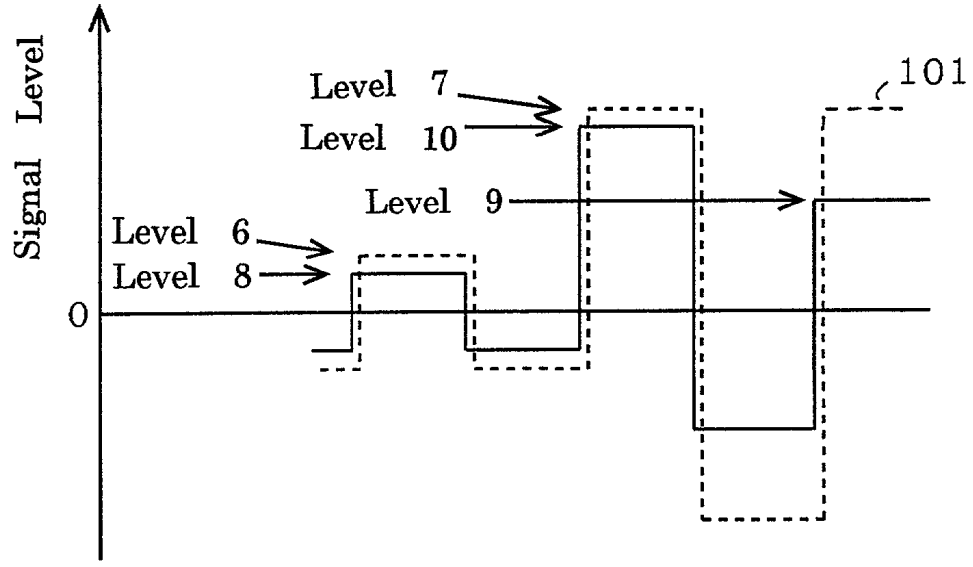

Signal Level
Level 7
Level 10
101
Level 9
Level 6
Level 8
0

FIG. 2

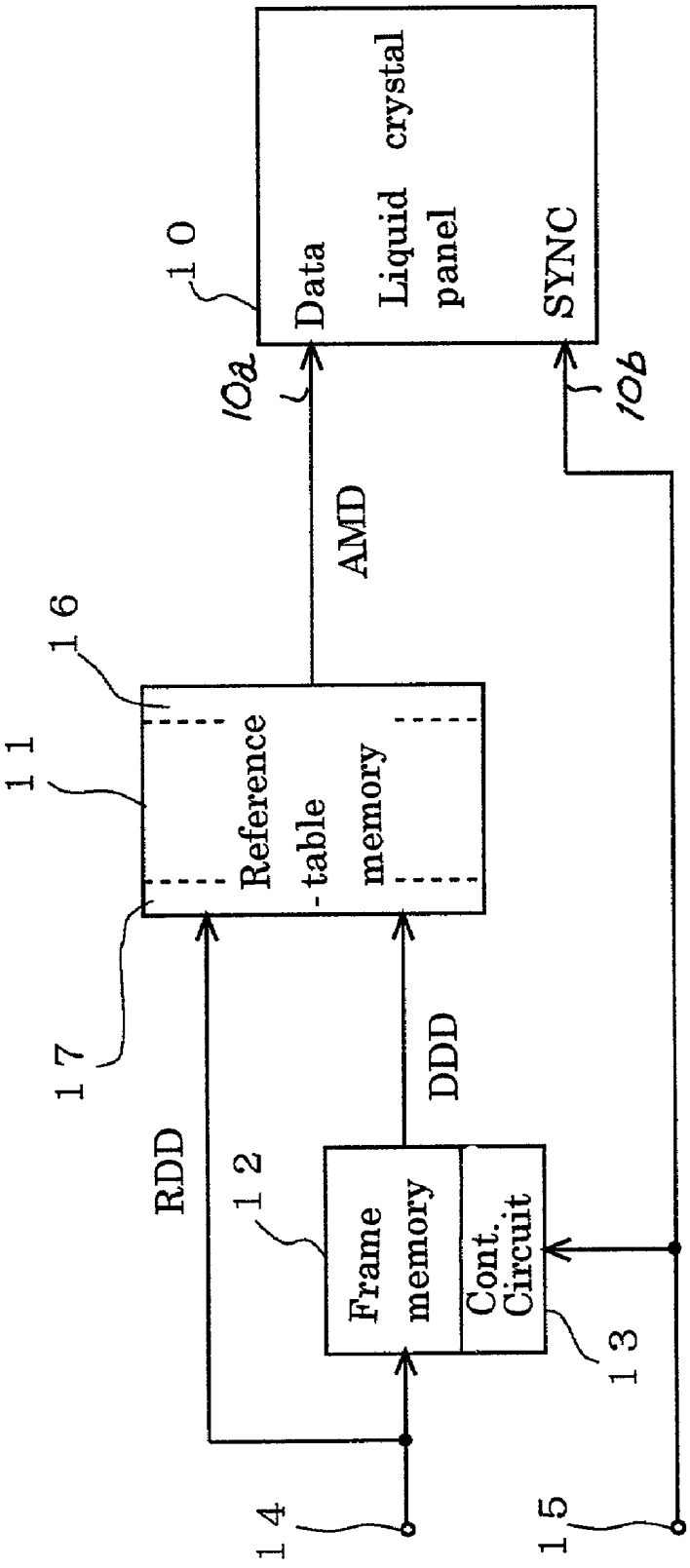

10
Liquid crystal panel
Data
SYNC
10a
10b
AMD
16
11
Reference -table memory
17
RDD
DDD
12
Frame memory
Cont. Circuit
13
14
15

FIG. 3

Address (Delayed display date DDD : 8 bits)	Address (Current display data RDD : 8 bits)															
	0	1	2	3	4	5				250	251	252	253	254	255
0	0	2	4	6	8	9				252	253	254	255	255	255
1	0	1	2	5	7						253	254	255	255	255
2	0	0	2	4	6						253	254	255	255	255
3	0	1	1	3	4						253	254	255	255	255
4	0	2	3	3								254	255	255	255
5	0														255
250	0														255
251	0	0	0	1							251	253	255	255	255
252	0	0	0	1	2						250	252	255	255	255
253	0	0	0	1	2						250	251	253	255	255
254	0	0	0	1	2						249	250	252	254	255
255	0	0	0	1	2	3				247	249	250	252	254	255

FIG. 4

Address (Delayed display date DDD : 8 bits)	Address (Current display data RDD : 8 bits)															
	0	1	2	3	4	5				250	251	252	253	254	255
0	0	2	4	6	8	9				252	253	254	255	255	255
1	0	1	2	5	7						253	254	255	255	255
2	0	0	2	4	6						253	254	255	255	255
3	0	1	1	3	4						253	254	255	255	255
4	0	2	3	3								254	255	255	255
5	0														255
250	0														210
251	0	0	0	1	2						196	198	200	205	208
252	0	0	0	1	2						195	197	200	204	206
253	0	0	0	1	2						195	196	198	200	204
254	0	0	0	1	2						194	195	197	199	202
255	0	0	0	1	2	3				192	194	195	197	199	200

FIG. 6

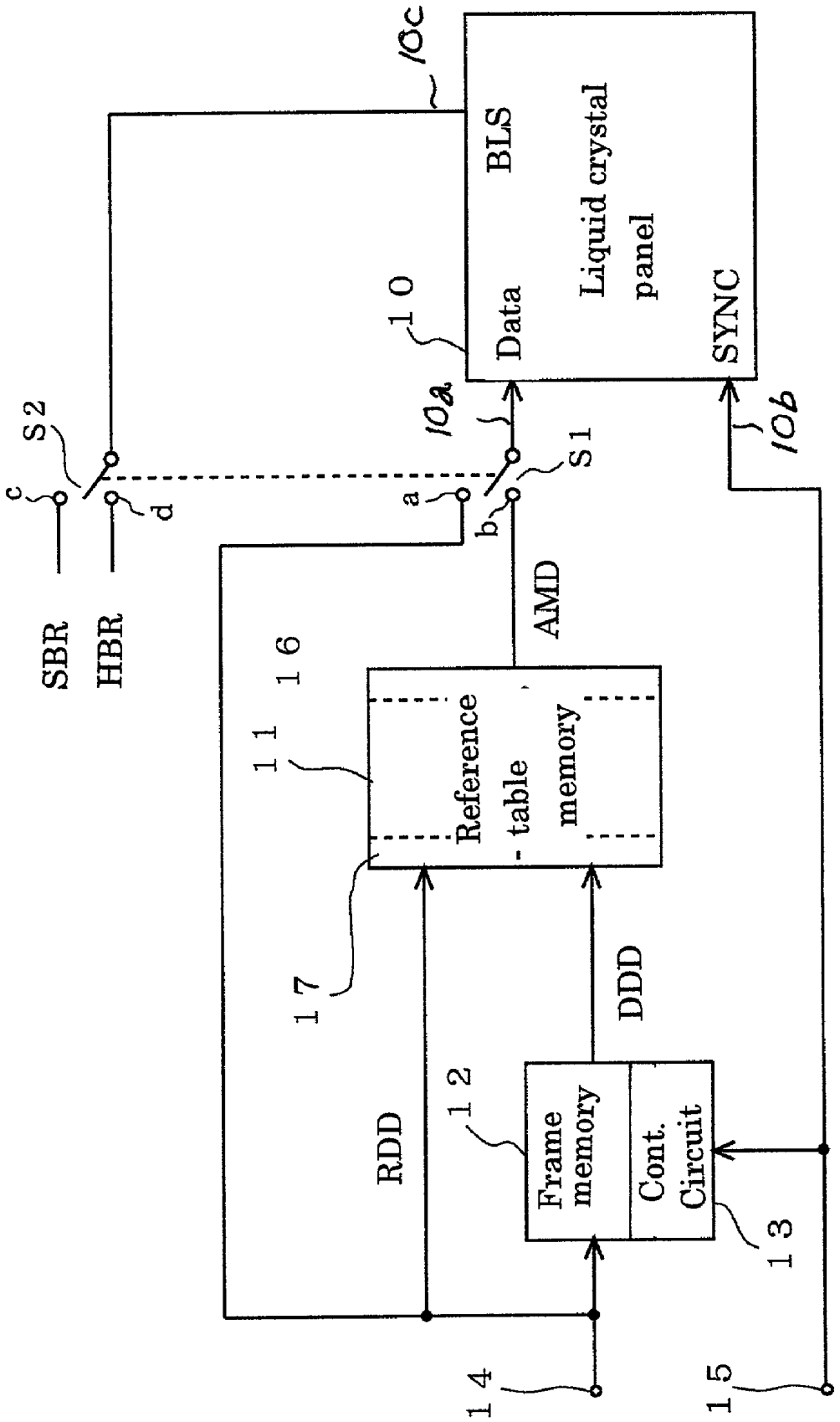
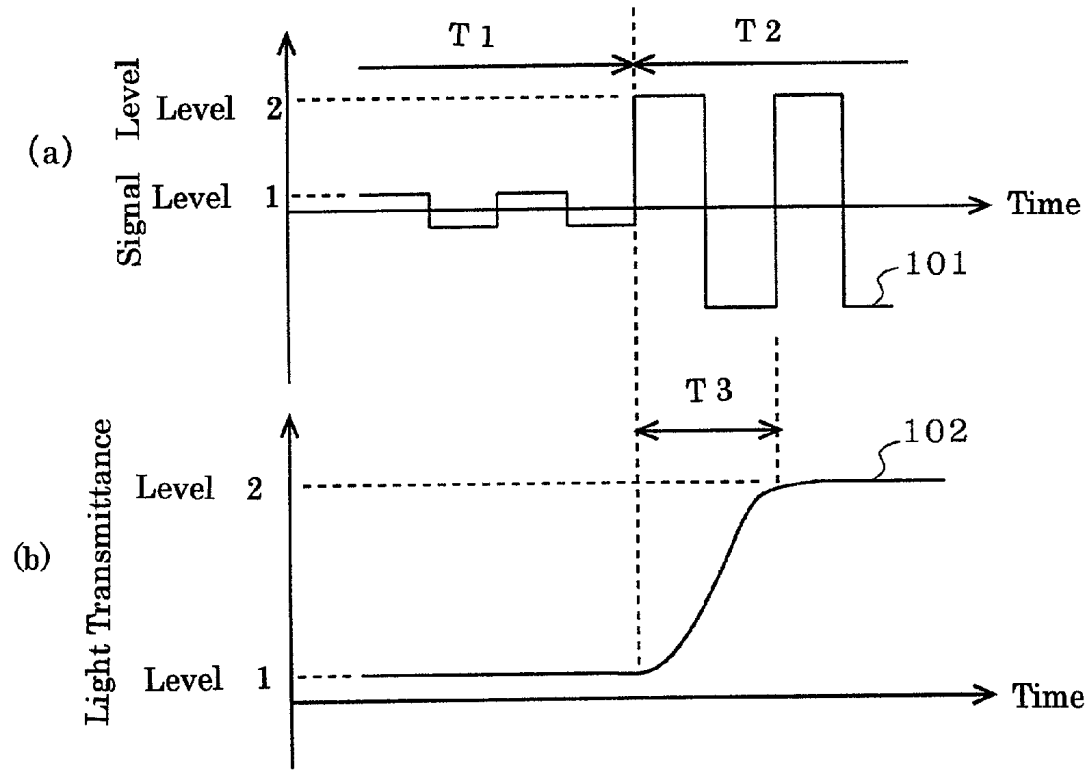
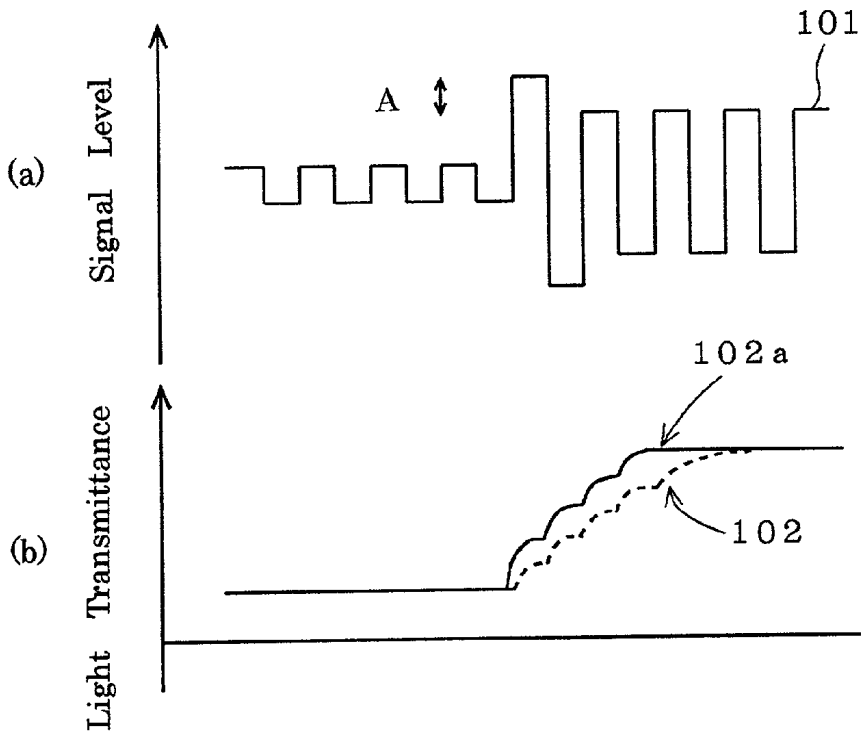

10c
BLS
Liquid crystal panel
Data
SYNC
10
10a
10b
S1
S2
a
b
c
d
SBR
HBR
AMD
16
11
Reference table memory
17
RDD
DDD
12
Frame memory
Cont. Circuit
13
14
15

FIG. 7



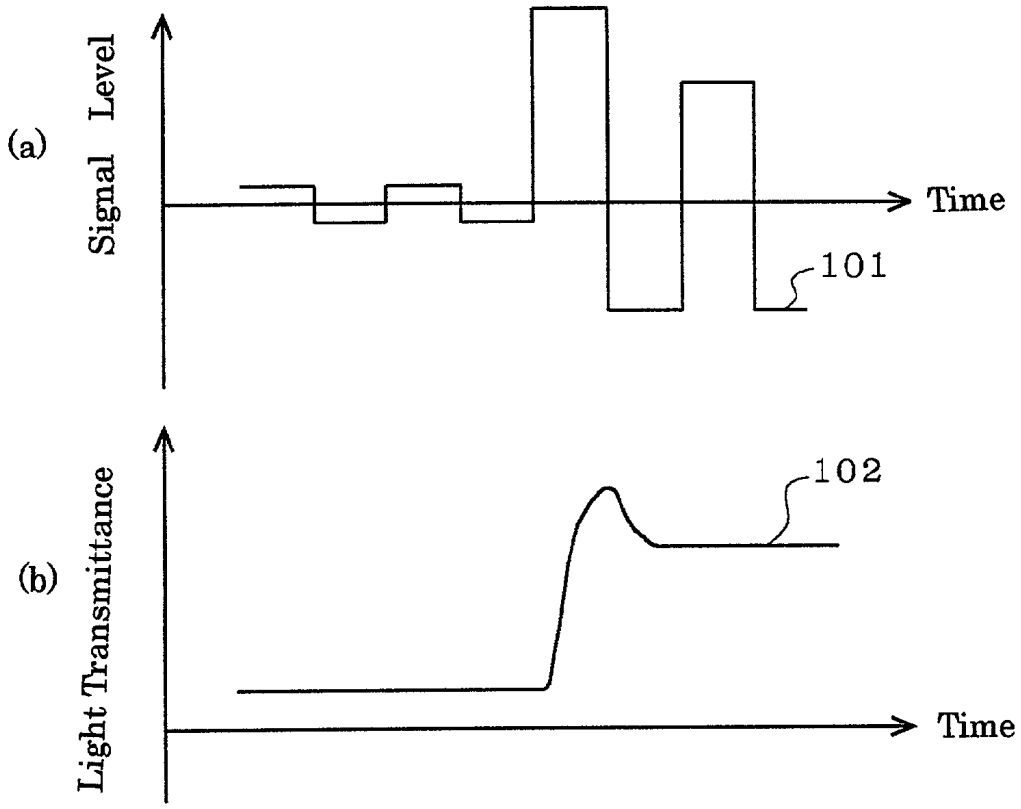
PRIOR ART

FIG. 8



PRIOR ART

FIG. 9



PRIOR ART

LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display device using a liquid crystal panel.

[0003] 2. Related Art

[0004] A liquid crystal panel switches display levels of a picture by switching electrical signals from outside. The liquid crystal panel usually receives display data from outside, converts the display data into electrical signal waveforms of predetermined voltage levels, and applies the waveforms to the liquid crystal elements to thereby display a picture. The switching time of the display levels by the liquid crystal panel is some 10 ms in general.

[0005] **FIG. 7** illustrates an example of response waveform when an electrical signal is applied to one liquid crystal element. In **FIG. 7**(*a*), an electrical signal waveform **101** illustrates a voltage applied to the liquid crystal element. The horizontal axis represents the time and the vertical axis represents the signal level. T1 represents a period of time during which a low signal level **1** is supplied. T2 represents a period of time during which a high signal level **2** is supplied. In **FIG. 7**(*b*), an optical response waveform **102** represents an optical response waveform of the liquid crystal element when the voltage of the electrical signal waveform **101** is applied, the horizontal axis represents the time corresponding to the electrical signal waveform, and the vertical axis represents the level of light transmittance of the liquid crystal element. The light transmittance shows a low level **1** during the period T1, and a high level **2** during the period T2.

[0006] When the signal level of the electrical signal waveform **101** is switched from the low signal level **1** into the high signal level **2**, a transitional period T3 appears between the period T1 and the period T2, due to the delay in the optical response of the liquid crystal element. When the light transmittance level **1** is 0%, and the light transmittance level **2** is 100%, the time required for the light transmittance varying from 10% to 90% is called the rise response time or response speed of the liquid crystal panel. Also, when the signal level is switched from the high signal level **2** into the low signal level **1**, the time required for the light transmittance varying from 90% to 10% is similarly called the fall response time of the liquid crystal panel.

[0007] Usually, the liquid crystal display device is driven by TV signals or signals from the personal computers, and the display switching frequency of these signals are about 60 Hz in general. This means that the display period of one picture screen is approximately 16.7 ms, and the picture screen is always rewritten by this time interval. On the other hand, the response speed of the liquid crystal element of the liquid crystal panel is around 30 to 60 ms in general. Therefore, the response is not complete within the time equivalent to the display switching frequency of 60 Hz.

[0008] As a method of improving such slowness in the response time of a liquid crystal panel, for example, a method of accelerating the movement of a liquid crystal element by temporarily applying a higher or lower signal level at the switching time of a drive signal of the liquid crystal panel has been proposed in the Japanese patent No. 2616652. This method is a technique applied to a liquid crystal panel of the Super Twisted Nematic (STN) mode, wherein the response speed of the liquid crystal element is rather slow as some 100 ms. This technique is effective for the liquid crystal panels with slow response speeds, for example, when the response waveform of the drive electrical signal waveform and the liquid crystal panel using this technique will improve the response speed from an optical response waveform **102** to an optical response waveform **102***a* as shown in **FIG. 8**. **FIG. 8**(*a*) illustrates the signal level variation of the electrical signal waveform **101**, and **FIG. 8**(*b*) illustrates the optical response waveforms **102**, **102***a* that represent the variations of the light transmittance corresponding to the signal level variation. "A" in **FIG. 8**(*a*) represents the level of compensation, and the waveform **102** in **FIG. 8**(*b*) shows the optical response waveform when not compensated, and the waveform **102***a* shows the optical response waveform when compensated.

[0009] However, when this technique is applied to a liquid crystal panel with a comparably high response speed of the liquid crystal element as some 10 ms, such as the recent TFT-LCD using a thin film transistor, for example, when the electrical signal waveform **101** is switched from the low voltage level into the high voltage as shown in **FIG. 9**(*a*), there is a possibility that an overshooting occurs in the optical response waveform **102**, as shown in **FIG. 9**(*b*), which is not desirable in terms of visibility of the display. On the other hand, when the voltage level is switched from the high level to the low level, there is a possibility that an undershooting occurs.

[0010] Furthermore, when the signal level after switching the display reaches the highest level, the compensation signal with a level higher than this highest level cannot be generated, which leads to a problem that disables improvement of the response speed.

SUMMARY OF THE INVENTION

[0011] According to one aspect of the invention, the liquid crystal display device includes: a delay circuit that delays an inputted current display data by one display period and outputs a delayed display data; a reference unit that possesses a reference data containing a plurality of reference values corresponding to both the current display data and the delayed display data, and outputs an output data based on a reference value selected from the plurality of the reference values; and a liquid crystal panel that receives a supply of video signals on the basis of the output data. Further, the reference value selected when the current display data changes from the delayed display data is set so that an optical response of the liquid crystal panel in relation to the change is substantially completed within the one display period.

[0012] Thus, the liquid crystal device of the invention is provided with a reference circuit that possesses a reference data containing a plurality of reference values corresponding to both the current display data and the delayed display data, and with regard to all the combinations of the current display data and the delayed display data, the data are prepared in advance, with which the optical response of a liquid crystal element is completed within the one display period neither too much nor too less. Thereby, the optical response of the

liquid crystal element of the liquid crystal panel can be completed within the one display period without generating an overshooting or an undershooting at any data level changes.

[0013] According to another aspect of the invention, in the liquid crystal display device, the level of the output data is compressed by a specific depth in such a manner that the level of the output data when the delayed display data and the current display data have the same value becomes lower than the level of the current display data, and the reference value selected when the current display data becomes higher than the delayed display data is set to expand the output data within the specific depth.

[0014] According to this, if the level of the current display data has a maximum level, it is possible to expand the output data within the specific depth, whereby the optical response of the liquid crystal element of the liquid crystal panel can be completed within the one display period.

[0015] According to another aspect of the invention, in the liquid crystal display device, the level of the output data is compressed by a specific depth in such a manner that the level of the output data when the delayed display data and the current display data have the same value becomes lower than the level of the current display data, and a lowering of a luminance of the liquid crystal panel based on the compression of the output data is compensated by raising the luminance of a backlighting of the liquid crystal panel.

[0016] According to this, by compensating the lowering of the luminance due to the level compression of the display data with the backlighting, the optical response of the liquid crystal element of the liquid crystal panel can be completed within the one display period, and also the display state with a desirable luminance can be achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Preferred embodiments of the present invention will be described in detail based on the followings, wherein:

[0018] **FIG. 1** is a graph illustrating the electrical signal waveform and the optical response waveform to describe the principle of compensation relating to the invention;

[0019] **FIG. 2** is a block diagram illustrating a major circuit configuration of the liquid crystal display device relating to the Embodiment 1 of the invention;

[0020] **FIG. 3** illustrates an example of data for use in the reference table memory relating to the Embodiment 1;

[0021] **FIG. 4** illustrates an example of data for use in the reference table memory of the liquid crystal display device relating to the Embodiment 2 of the invention;

[0022] **FIG. 5** illustrates an electrical signal waveform compensated by the Embodiment 2;

[0023] **FIG. 6** is a block diagram illustrating a major circuit configuration of the liquid crystal display device relating to the Embodiment 3 of the invention;

[0024] **FIG. 7** illustrates an electrical signal waveform and an optical response waveform of the conventional liquid crystal display device;

[0025] **FIG. 8** illustrates an electrical signal waveform and an optical response waveform of the liquid crystal display device by conventional compensation method; and

[0026] **FIG. 9** illustrates an electrical signal waveform and an optical response waveform of the liquid crystal display device by conventional compensation method.

DESCRIPTION OF PREFERED EMBODIMENTS

[0027] At the beginning, the concept of the present invention will be described with reference to **FIG. 1**. As shown in the graph of **FIG. 1**(*a*), the horizontal axis represents the time, and the vertical axis represents the signal level of an electrical signal waveform **101**. And, **FIG. 1**(*b*) represents the light transmittance of an optical response waveform **102** of a liquid crystal element of the liquid crystal panel to which the electrical signal waveform **101** is applied. **FIG. 1**(*b*) shows the record of variations in the optical response of the liquid crystal element when the signal level of the electrical signal waveform **101** varies from a low signal level **1** to a high signal level **2**. And a level **1** in the light transmittance shows a light transmittance of the liquid crystal element when the electrical signal waveform **101** is in the low signal level **1**. Also, a level **2** of the light transmittance shows a light transmittance of the liquid crystal element when the electrical signal waveform **101** is in the high signal level **2**.

[0028] Signal levels **3**, **4** and **5** represent the signal levels compensated for accelerating the movement of the liquid crystal element when switched from the low signal level **1** into the high signal level **2**. These compensated signal levels **3**, **4** and **5** are the signal levels in which the original signal level **2** is compensated, and are outputted during one display period. When this compensated accelerating signal levels are excessive, such as the signal level **3**, the optical response waveform **102** will overshoot as shown by a response **3**; and also, when the compensation for the signal level is too little in quantity, such as signal level **4**, the response of the optical response waveform is not completed within the one display period as shown by a response **4**. By selecting an optimum compensation signal level such as the level **5**, the response of the optical response waveform can be completed precisely in the one display period as shown by a response **5**.

[0029] The compensated accelerating signal level can be determined optimum value uniquely by the initial signal level **1** and the signal level **2** after switching the display. Therefore, the first method of the invention measures in advance the compensation signal levels covering all the variations of data to be displayed, prepares these as a table, thereby picks out, when the display signal level changes, a compensation signal level that completes the optical response within the one display period neither too much nor too less from the signal level before switching (the delay display data) and the signal level after switching (the current display data), and applies the compensation signal level to the liquid crystal panel.

[0030] For example, the liquid crystal panel that can display n gradations has n^2 combination patterns of display switching. Therefore, the method stores n^2 compensation signal levels in a ROM (Read Only Memory), for example, as a table.

[0031] Here, when the target value of change of the original signal level is either the maximum or the minimum value of the signal level, the compensation signal cannot be generated. In such a case, the problem can be solved by compressing the original signal level. In other words, the

second method relating to the invention compresses the signal level invariably at a certain rate to thereby produce a margin to the signal level, lowers the maximum signal level when there is a signal change toward the maximum signal level, and generates the compensation signal level by using the produced margin.

[0032] And in the second method, since the maximum signal level after compression becomes lower than the maximum value of the original signal level, the second method compensates a fall of the light transmittance of the liquid crystal panel due to this lowering by raising the luminance of the backlighting of the liquid crystal panel so as not to give any sense of incongruity to human eyes.

[0033] The Embodiment 1

[0034] **FIG. 2** is a block diagram of a liquid crystal panel drive circuit for generating a drive signal waveform related to the Embodiment 1 of the invention. In the block diagram, **10** signifies a liquid crystal panel of the liquid crystal display device, which includes a data input unit **10***a* and a synchronizing signal input unit **10***b*. **11** signifies a reference unit, which includes a reference table memory (compensation data ROM). **12** signifies a frame memory, **13** a control circuit, **14** a data input terminal, and the current display data RDD is supplied to this data input terminal **14**. **15** signifies a synchronizing signal input terminal, **16** a data bus for the reference table memory **11**, and **17** an address bus also for the reference table memory **11**.

[0035] The liquid crystal panel **10** of the liquid crystal display device usually inputs display data in a form of digital data, and the display data of this circuit are also assumed as digital. Here, the number of display signal levels, that is, the number of the display data is assumed to be 8 bits with 256 gradations. Since the number of the display data is 256, the number of the compensation signal level data to be prepared in advance is 256. Therefore, by using the compensation data ROM **11** that comprises an 8 bit data bus **16** and a 16 bit address bus **17**, all the data can be stored.

[0036] A current display data RDD inputted through the input terminal **14** is inputted to the 8 bits address bus of the address bus **17** of the reference table memory **11**, and also inputted to the frame memory **12** at the same time. A delayed display data DDD, which is delayed by the one display period, is outputted from the frame memory **12**, and this delayed display data DDD is inputted to the remaining 8 bits address bus of the reference table memory **11**. The reference data are written in advance as a table into the reference table memory **11**, with which the optical response of a liquid crystal element is compensated so as to be completed within the one display period neither too much nor too less, when the signal level changes in all the combinations of the signal level changes relating to the current display data RDD and the delayed display data DDD. The data possesses multiple reference values written in the matrix of 256×256. **FIG. 3** represents a part of the reference data. The reference data in **FIG. 3** is a matrix data corresponding to the previous display data arrayed in the vertical direction (the delayed display data DDD) and the current displayed data RDD arrayed in the horizontal direction, which includes 256 types of reference values from 0 to 255. Naturally, these reference values are stored digitally inside the reference table memory **11**.

[0037] Preparing such a circuit configuration and the reference table memory (ROM) in which the compensation data is written, and selecting, from the reference data stored in this reference table memory, a reference value determined on the basis of the signal level of the current display data RDD to be presently displayed and the signal level of the delayed display data DDD before the one display period, and applying the display signal level corresponding to this reference value as a compensation data AMD to the liquid crystal panel **10** will achieve a display of a high speed response at the switching of any signal levels.

[0038] The Embodiment 2

[0039] Next, a concrete method of generating the compensation signal while always compressing the original signal will be described. In a liquid crystal panel that can provide displays of 8 bits, namely, 256 levels, a data compression standard of 200/256, for example, is set. If the signal level before the one display period (the delayed display data DDD) is equal to the current signal level (the current display data RDD), the diagonal value on the table in **FIG. 3**, for example, will be selected as the compensation data AMD, but in the Embodiment 1, the data of the original signal level was written here on the diagonal as it was. In this Embodiment 2, as shown in **FIG. 4**, as a data when the signal level before the one display period (the delayed display data DDD) is equal to the current signal level (the current display data RDD), the data in which the original data is compressed to 200/256 (compression depth is 256 minus 200) is provided in advance on the diagonal of the table.

[0040] With this arrangement, if the signal level of the original data is 256, the output signal level will be 200, and as a result of giving the compression depth, the remaining signal levels from 201 to 256 can be used for a generation of the compensation signal. **FIG. 5** represents the time-varying characteristics of the electrical signal level when the liquid crystal panel is driven using this method. The dashed line represents the original signal waveform **101**, and the solid line represents a compensated signal waveform **101**A. When the original signal waveform **101** represented by the dashed line changes from a signal level **6** to a maximum signal level **7**, the signal levels **6** and **7** are each compressed to 200/256, and become new signals **8** and **9** represented by the solid line. And, as shown by the signal level **10**, the compensation signal is generated so that the signal level is increased within the compression depth.

[0041] The Embodiment 3

[0042] In the Embodiment 2, since the signal level supplied to the liquid crystal panel is compressed, the luminance will be lowered on the display. Accordingly, there is a possibility that the difference of the luminance brings about a sense of incongruity, when the liquid crystal panel is switched from the regular drive to the drive with a compression. In that case, as shown in **FIG. 6**, the signal compression is carried out during driving the liquid crystal panel, in a manner that the switching of the regular drive and the drive with a compression is interlocked with the luminance switching of the backlighting of the liquid crystal panel. And in this case, the luminance of the backlighting is raised to compensate the lowering of the luminance due to the lowering of the signal level, thereby achieving the display state with a desirable luminance.

[0043] In **FIG. 6**, S1 and S2 signify switches that interlock each other. The switch S1 has a regular drive contact a and

a compression drive contact b, and the switch **S2** has a standard luminance contact c and a high luminance contact d. The movable contact of the switch **S1** selects the current display data RDD from the contact a at the regular drive, and the compensation data AMD from the contact b at the compression drive, and supplies the data input unit **10***a* of the liquid crystal panel **10**. The movable contact of the switch **S2** selects a standard luminance SBR from the contact c at the regular drive, and a high luminance HBR from the contact d at the compression drive, and supplies the selected to a backlighting switch input unit **10***c* of the display panel **10**.

[**0044**] According to the present invention being thus described, the data are prepared in advance, with which the response is completed within the one display period neither too much nor too less, as to all the combinations of the signal level changes. Thereby, the response of the liquid crystal panel can be completed within the one display period without generating an overshooting or an undershooting at any signal level changes.

[**0045**] Further, if the original signal is a signal that has a maximum level or a minimum level, the compensation signal for accelerating the movement of the liquid crystal can be generated by means of the signal compression, thereby completing the response of the liquid crystal panel within the one display period.

[**0046**] Also, by compensating the lowering of the luminance due to the signal compression with the backlighting, the response of the liquid crystal panel can be completed within the one display period, and the display state with a desirable luminance can be achieved as well.

What is claimed is:

1. A liquid crystal display device comprising:

a delay circuit that delays an inputted current display data by one display period and outputs a delayed display data;

a reference unit that possesses a reference data containing a plurality of reference values corresponding to both the current display data and the delayed display data, and outputs an output data based on a reference value selected from a plurality of the reference values; and

a liquid crystal panel that receives a supply of video signals on the basis of the output data, wherein

the reference value selected when the current display data changes from the delayed display data is set so that an optical response of the liquid crystal panel in relation to the change is substantially completed within the one display period.

2. A liquid crystal display device as claimed in claim 1, wherein the level of the output data is compressed by a specific depth in such a manner that the level of the output data when the delayed display data and the current display data have the same value becomes lower than the level of the current display data, and the reference value selected when the current display data becomes higher than the delayed display data is set to expand the output data within the specific depth.

3. A liquid crystal display device as claimed in claim 1, wherein the level of the output data is compressed by a specific depth in such a manner that the level of the output data when the delayed display data and the current display data have the same value becomes lower than the level of the current display data, and a lowering of a luminance of the liquid crystal panel based on the compression of the output data is compensated by raising the luminance of a backlighting of the liquid crystal panel.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US20020047821A1	公开(公告)日	2002-04-25
申请号	US09/930498	申请日	2001-08-16
[标]申请(专利权)人(译)	MIYAKE SHIRO		
申请(专利权)人(译)	MIYAKE SHIRO		
当前申请(专利权)人(译)	MIYAKE SHIRO		
[标]发明人	MIYAKE SHIRO		
发明人	MIYAKE, SHIRO		
IPC分类号	G02F1/133 G09G3/20 G09G3/34 G09G3/36 G09G5/36		
CPC分类号	G09G3/3406 G09G3/3685 G09G5/36 G09G2340/16 G09G2320/0285 G09G2320/0633 G09G2320/0646 G09G2320/0252		
优先权	2000248616 2000-08-18 JP		
其他公开文献	US6747621		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示装置技术领域本发明涉及一种液晶显示装置，包括：存储器，其将提供给液晶面板的当前显示数据延迟一个显示周期;以及参考表存储器，其保持包含由当前显示数据确定的多个参考值的参考数据。和延迟显示的数据。这里，参考表存储器具有预先写入的补偿信号数据，其基本上完成了在一个显示周期内液晶面板的光学响应。液晶显示装置在输入的显示数据总是被转换成补偿信号电平数据之后提供给液晶面板，从而实现在一个显示周期内完成的高速响应。