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(54) **SOURCE DRIVER CIRCUIT AND DRIVING METHOD FOR LIQUID CRYSTAL DISPLAY DEVICE**

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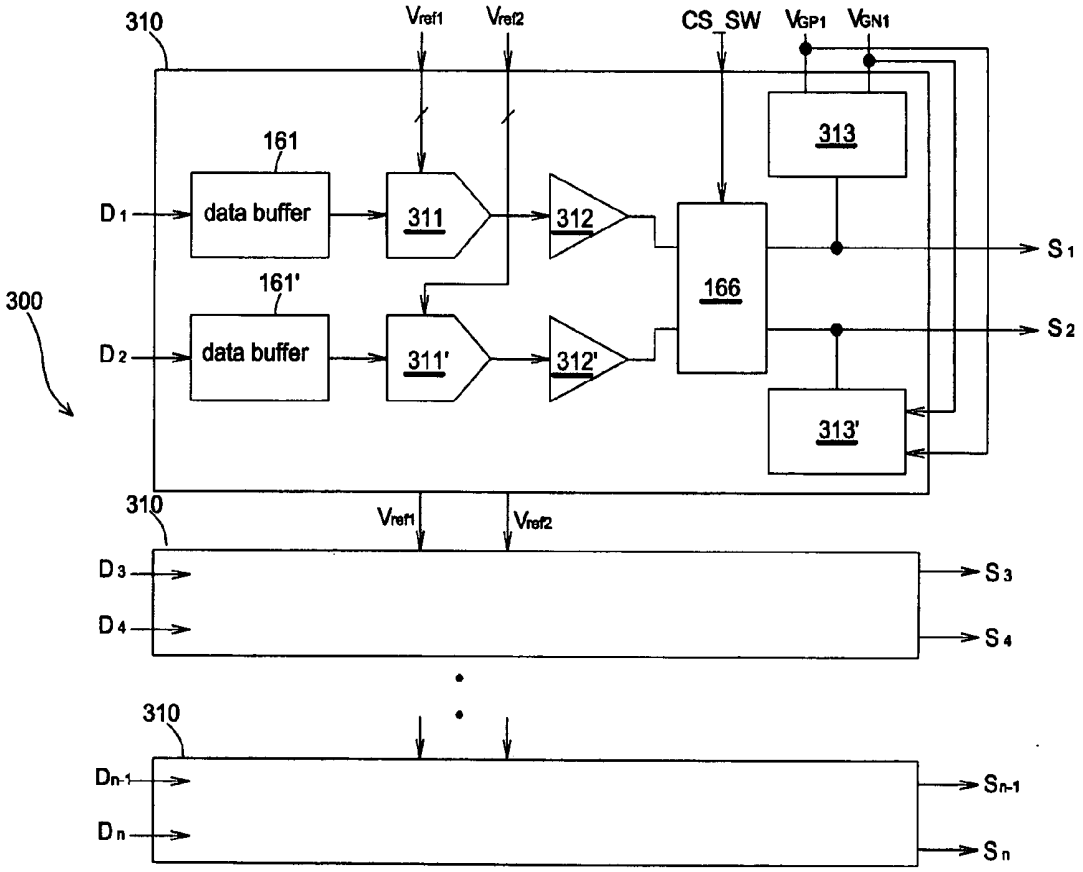
(57) **ABSTRACT**

The invention relates to a source driver circuit and method for a LCD device. The source driver circuit includes a plurality of source drivers. Each source driver includes two data buffers, two digital-to-analog converters, two amplifiers, a switch module and two black insertion units. The invention uses the black insertion units to directly provide black insertion voltages required in a black insertion step without use of digital-to-analog converters and amplifiers, thereby achieving higher the driving speed of the source driver circuit and lower power consumption of the amplifiers.



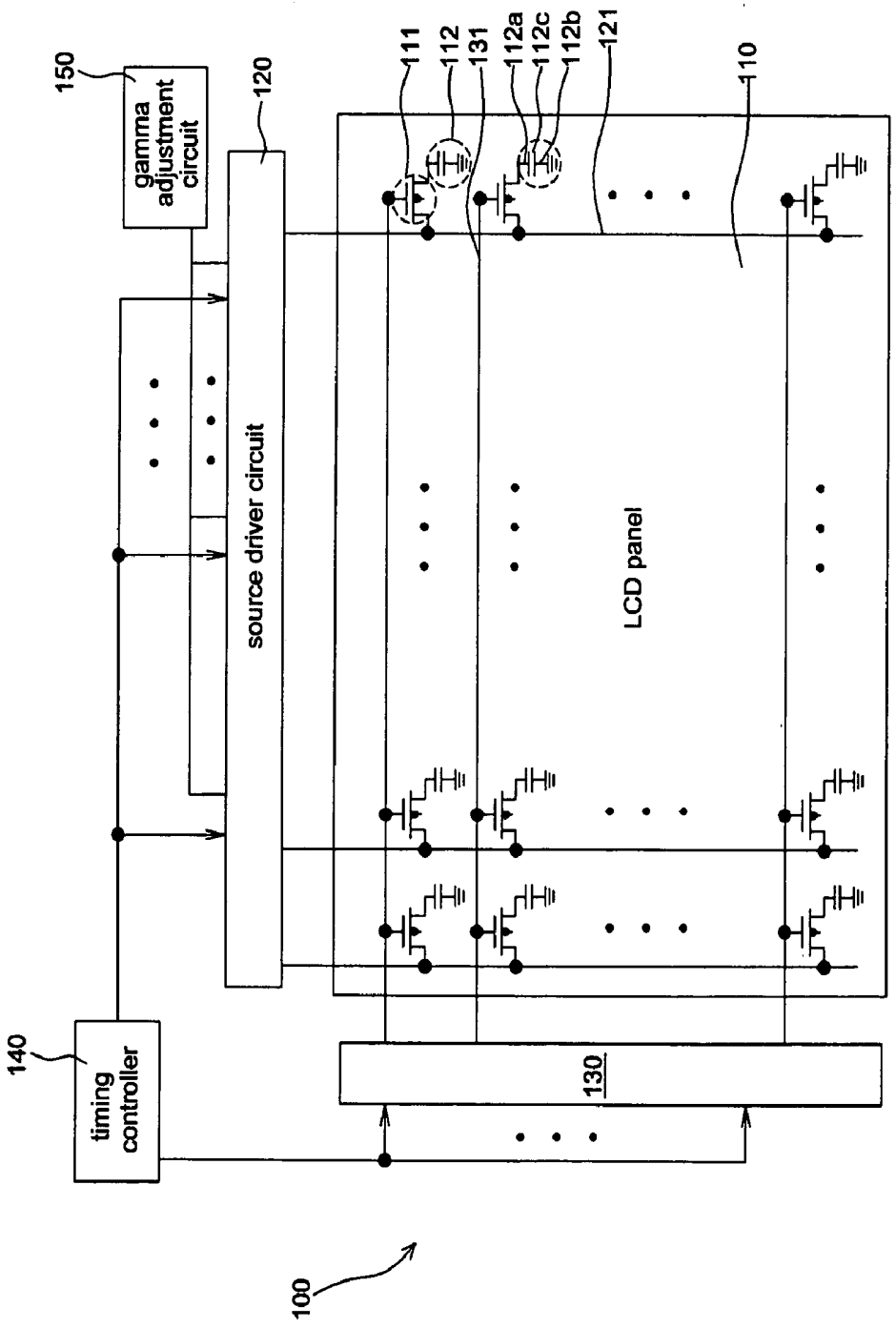


FIG. 1A (PRIOR ART)

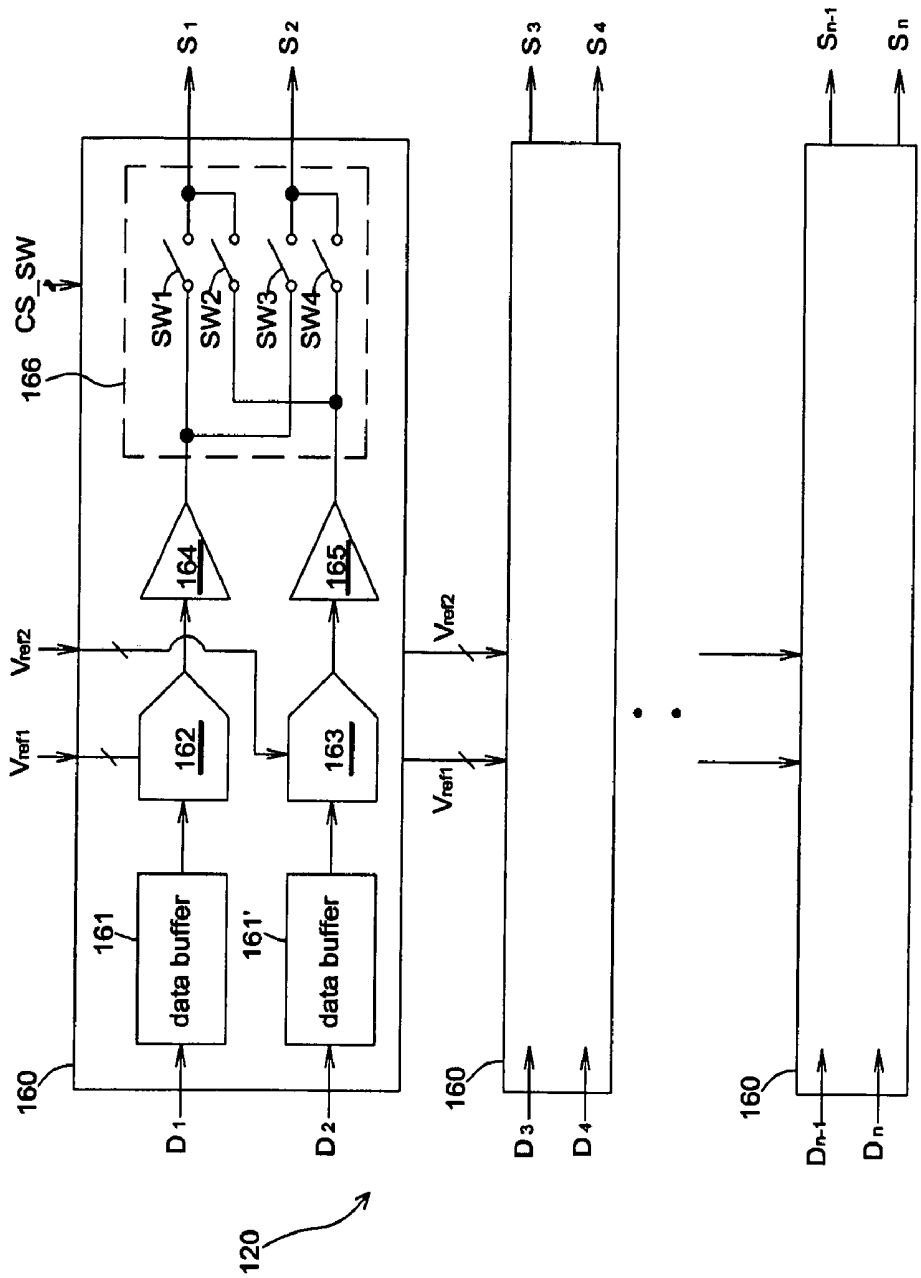


FIG. 1B (PRIOR ART)

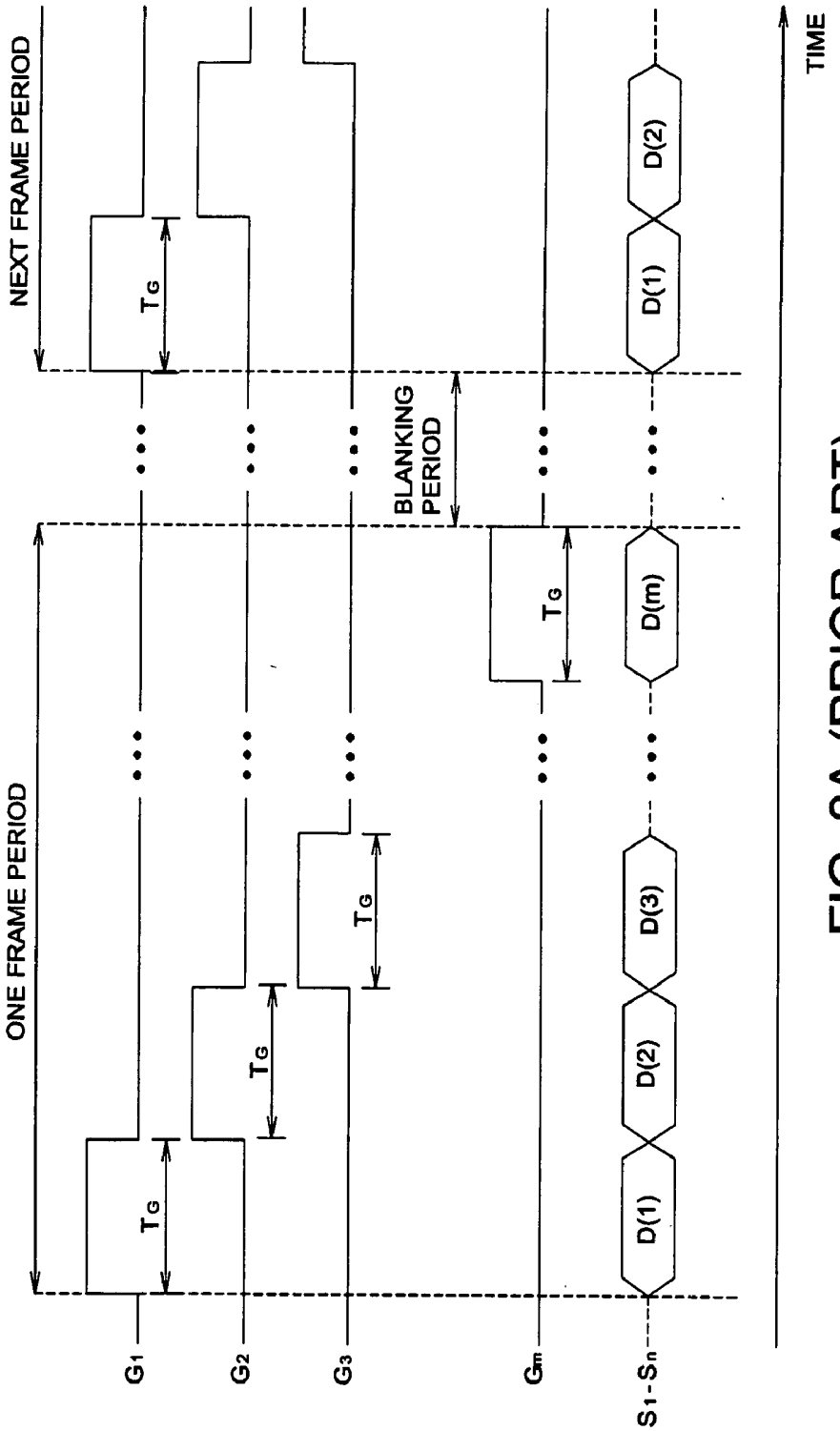


FIG. 2A (PRIOR ART)

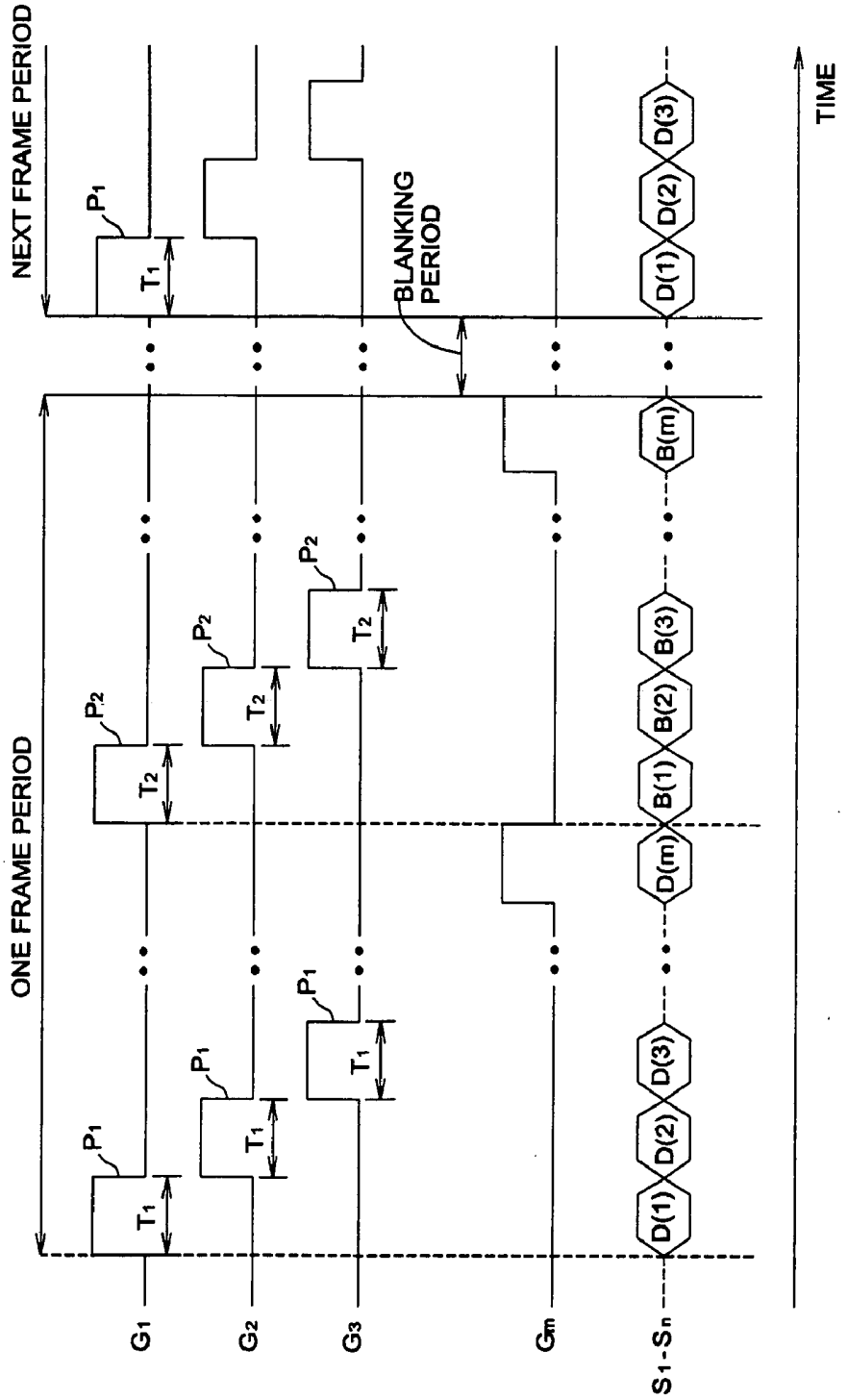


FIG. 2B (PRIOR ART)

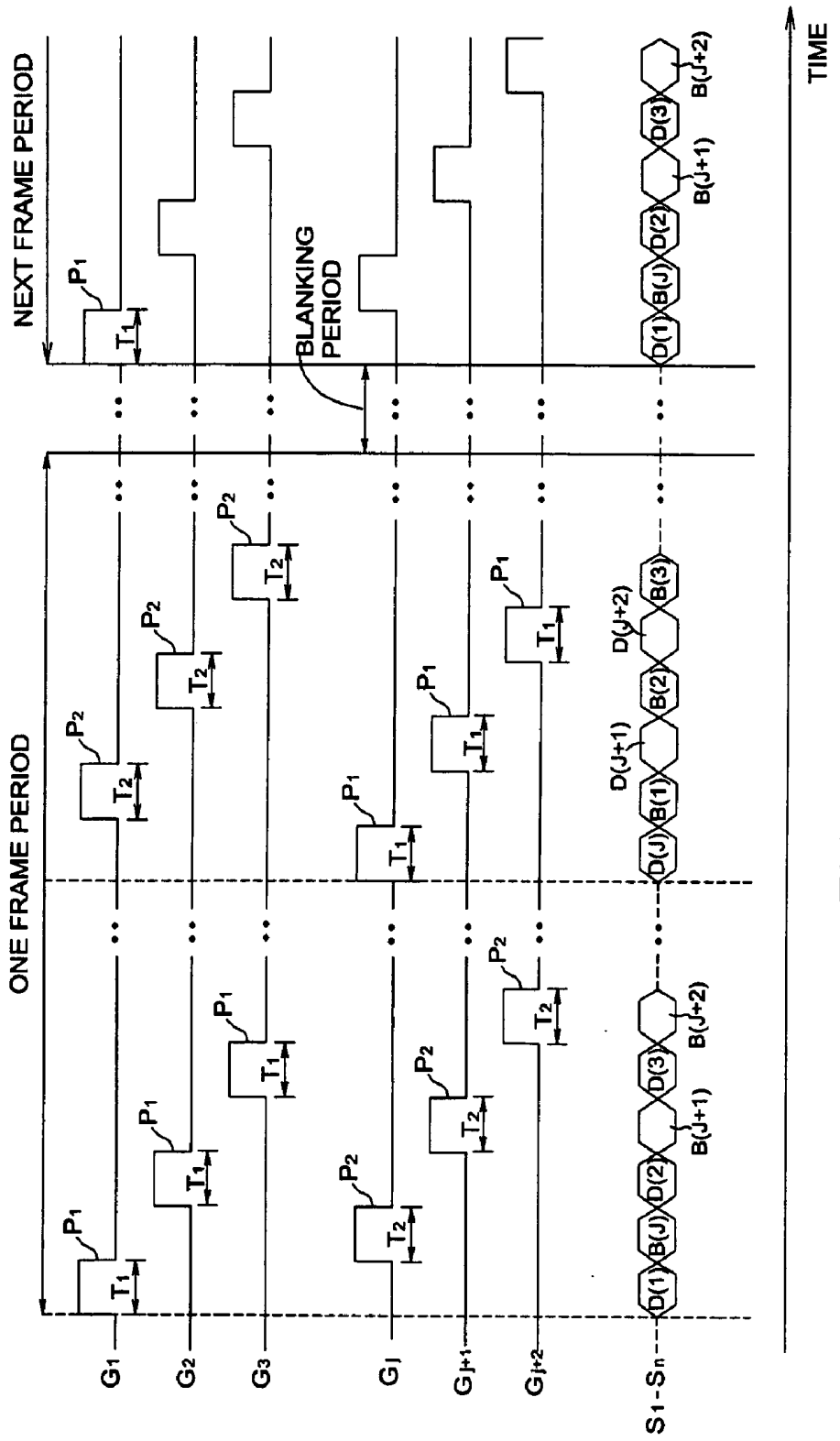


FIG. 2C (PRIOR ART)

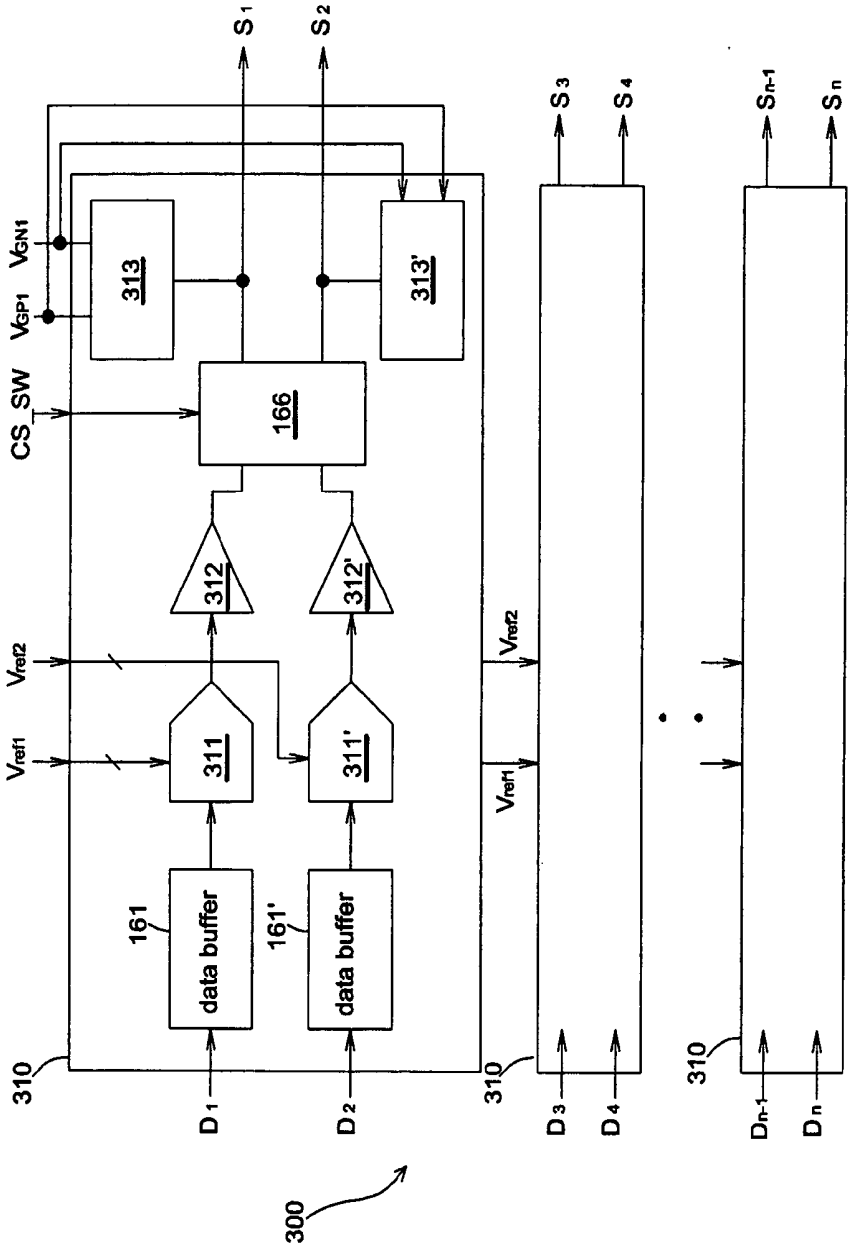

S1
S2
S3
S4
Sn-1
Sn
VGN1
VGP1
313
313'
CS_SW
166
312
312'
Vref2
Vref1
311
311'
161
161'
data buffer
data buffer
310
D1
D2
D3
D4
Dn-1
Dn
300

FIG. 3

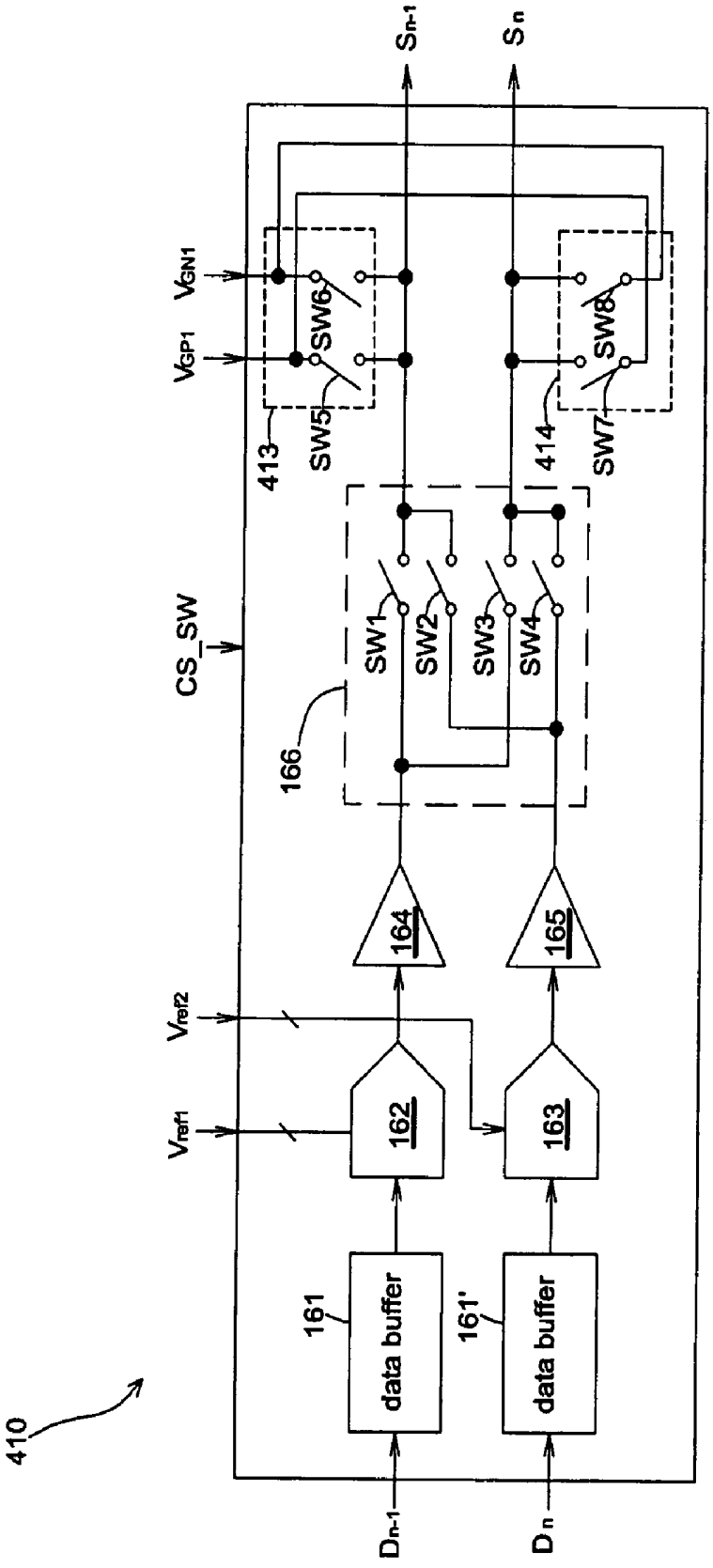

410
data buffer
161
data buffer
161'
162
163
164
165
166
413
414
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
CS_SW
VGN1
VGP1
Vref1
Vref2
Sn-1
Sn
Dn-1
Dn

FIG. 4A

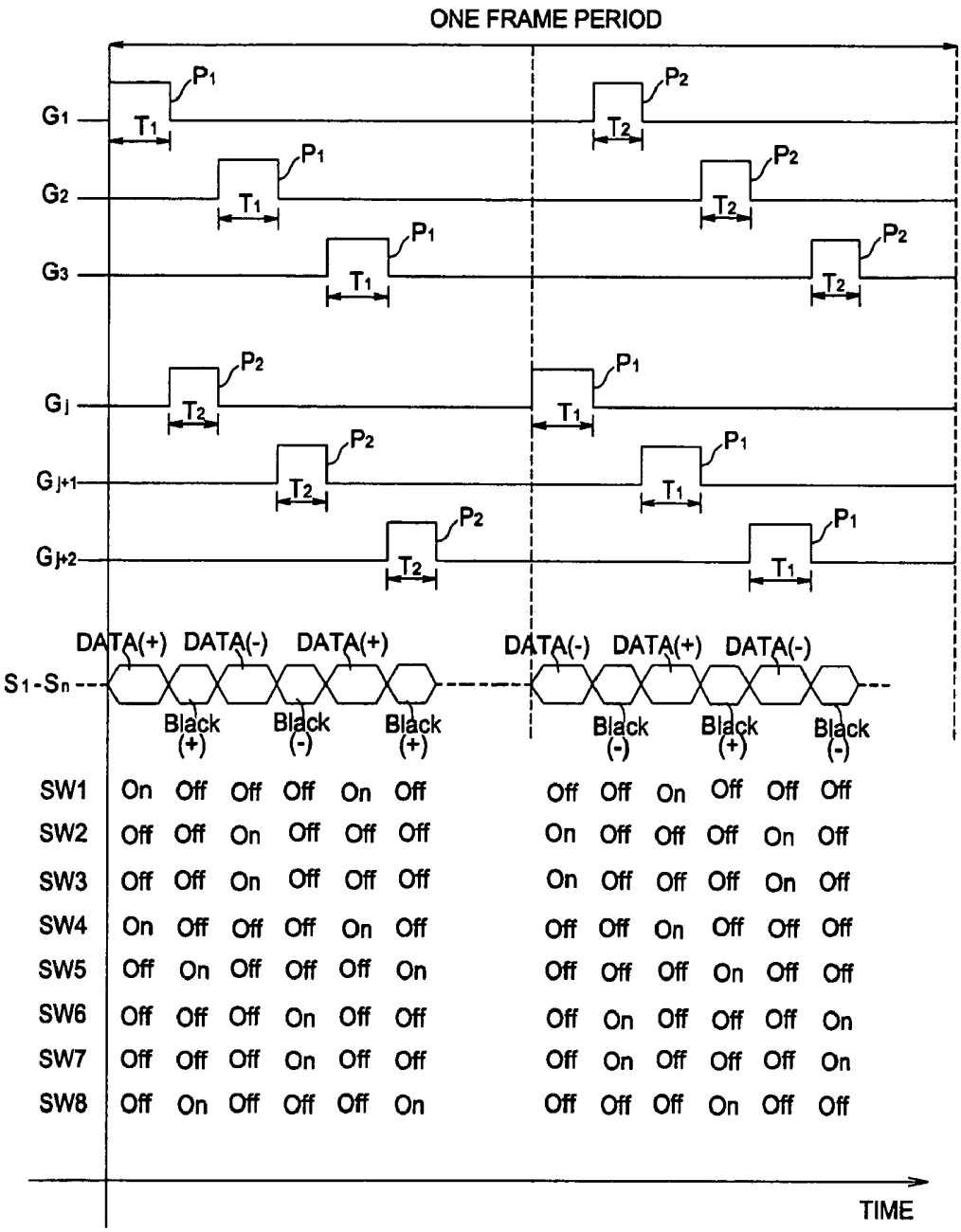

ONE FRAME PERIOD
G1
G2
G3
Gj
Gj+1
Gj+2
P1
P2
T1
T2
DATA(+) DATA(-) DATA(+)
DATA(-) DATA(+) DATA(-)
S1-Sn
Black (+)
Black (-)
Black (+)
Black (-)
Black (+)
Black (-)
SW1 On Off Off Off On Off Off Off On Off Off Off
SW2 Off Off On Off Off Off On Off Off Off On Off
SW3 Off Off On Off Off Off On Off Off Off On Off
SW4 On Off Off Off On Off Off Off On Off Off Off
SW5 Off On Off Off Off On Off Off Off On Off Off
SW6 Off Off Off On Off Off Off On Off Off Off On
SW7 Off Off Off On Off Off Off On Off Off Off On
SW8 Off On Off Off Off On Off Off Off On Off Off
TIME

FIG. 4B

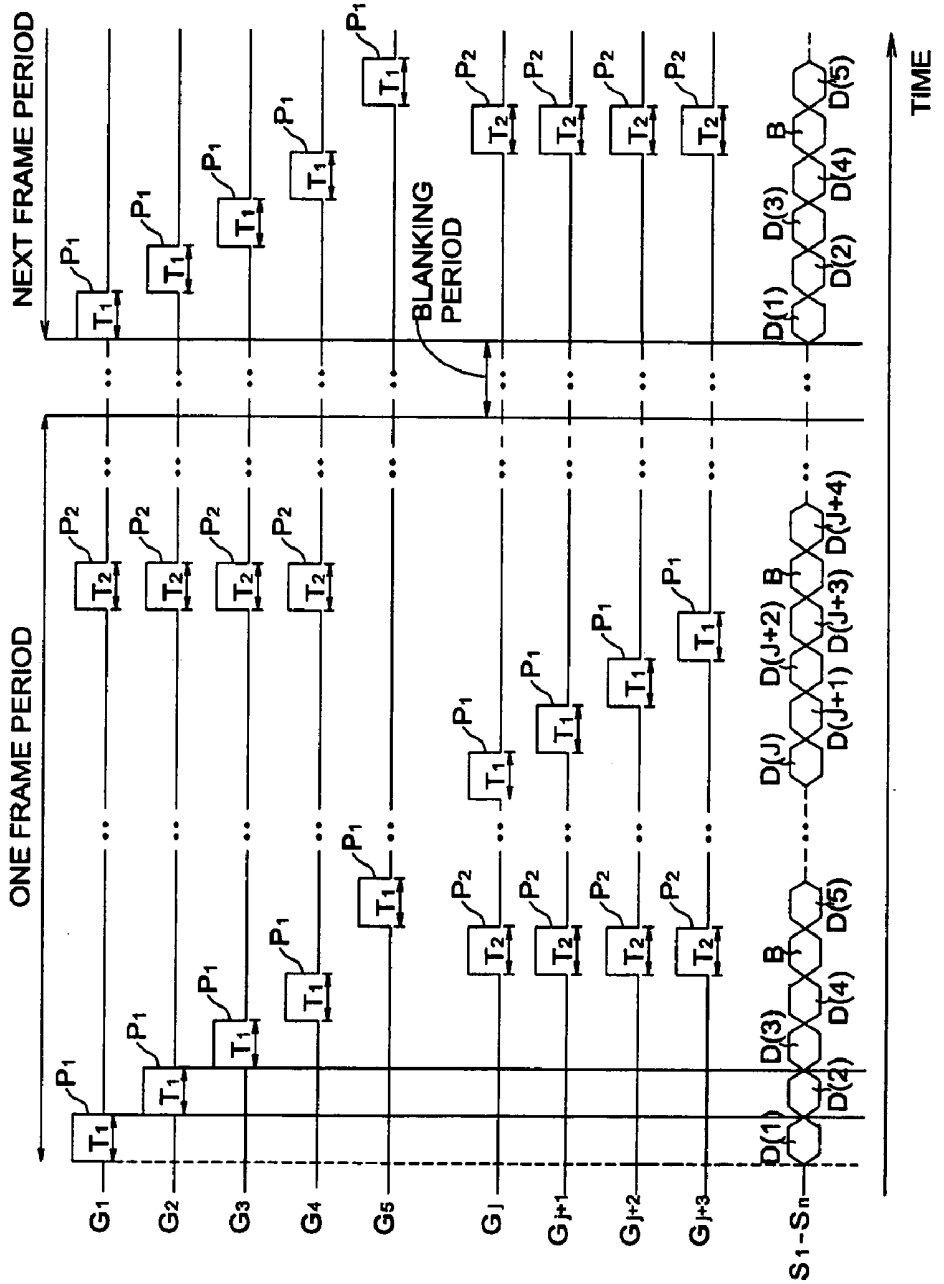
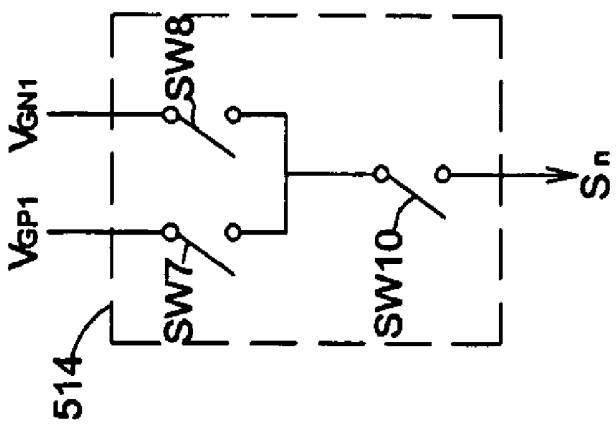

NEXT FRAME PERIOD
ONE FRAME PERIOD
BLANKING PERIOD
TIME
G1
G2
G3
G4
G5
GJ
GJ+1
GJ+2
GJ+3
S1-Sn
P1
P2
T1
T2
D(1)
D(2)
D(3)
D(4)
D(5)
B
D(J)
D(J+1)
D(J+2)
D(J+3)
D(J+4)

FIG. 4C



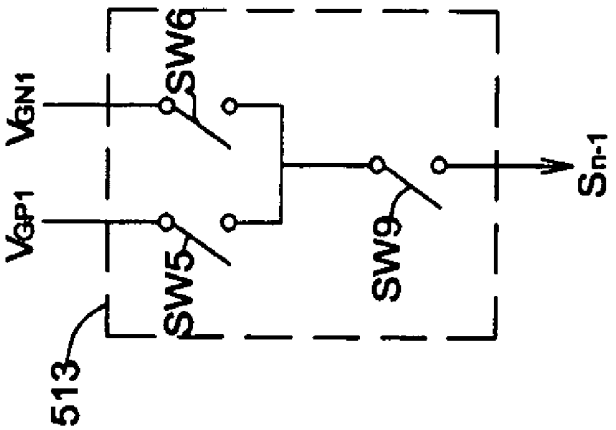


FIG. 5

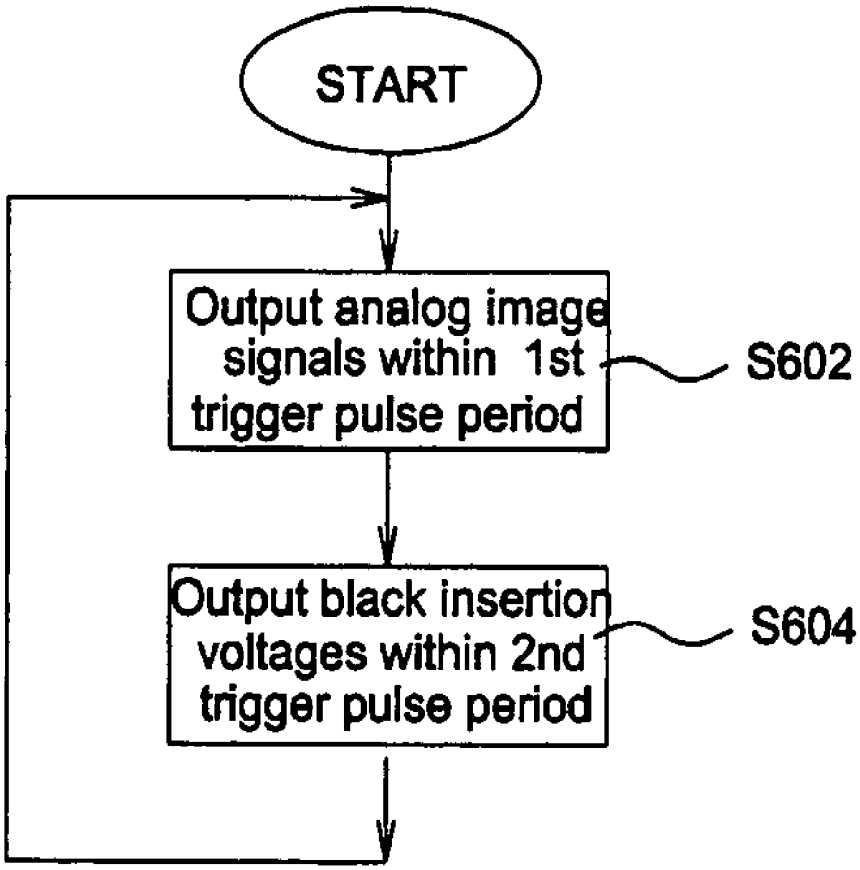

START
Output analog image signals within 1st trigger pulse period
S602
Output black insertion voltages within 2nd trigger pulse period
S604

FIG.6

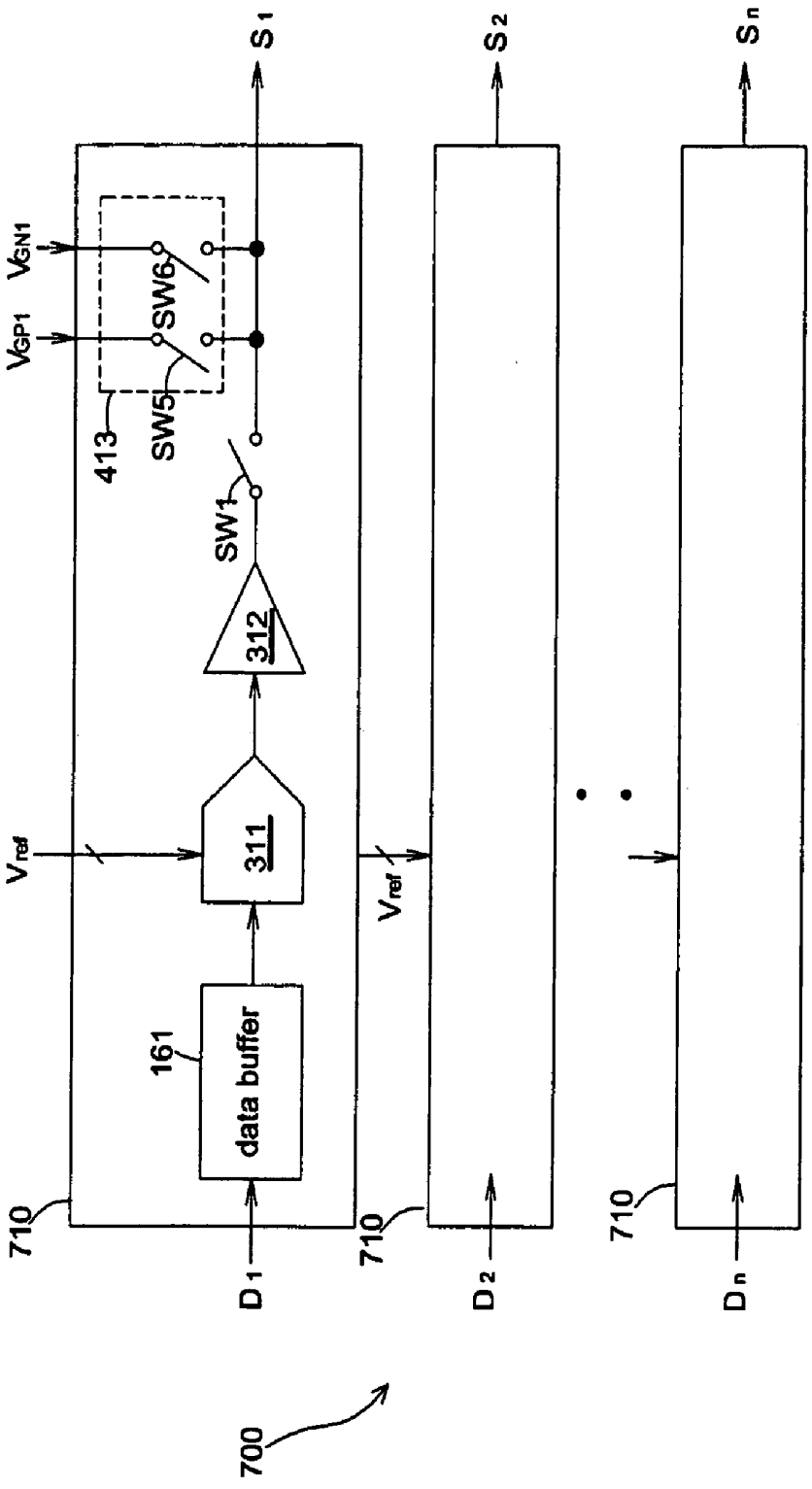

S1
S2
Sn
VGN1
VGP1
SW6
SW5
413
SW1
312
311
Vref
Vref
161
data buffer
710
710
710
D1
D2
Dn
700

FIG. 7

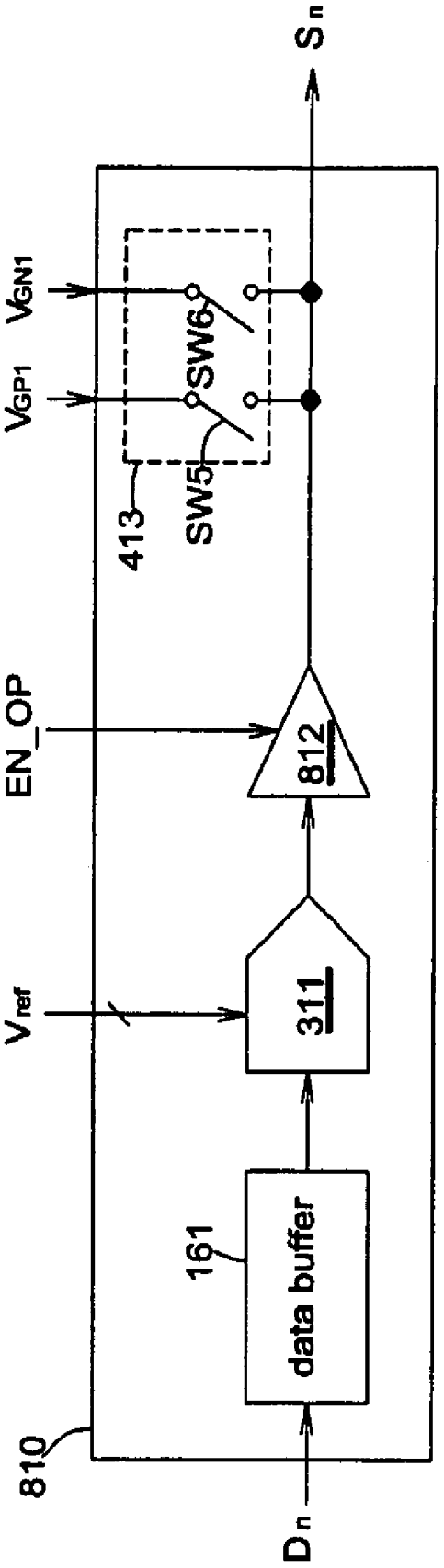

Sn
VGN1
VGP1
SW6
SW5
413
EN_OP
812
Vref
311
161
data buffer
810
Dn

FIG. 8

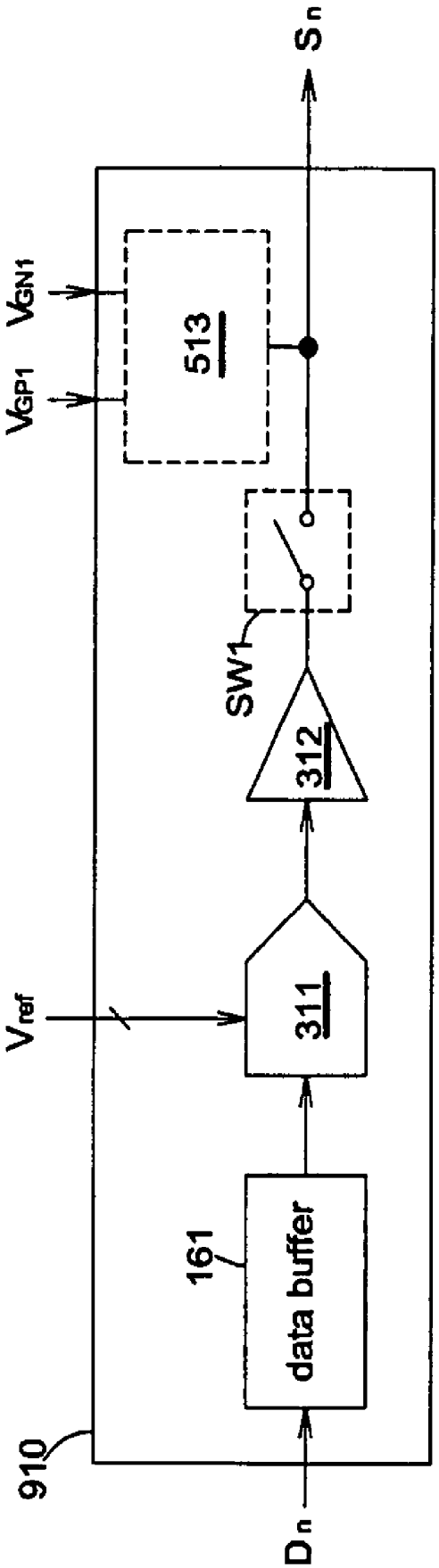


FIG. 9

SOURCE DRIVER CIRCUIT AND DRIVING METHOD FOR LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of the filing date of Taiwan Application Ser. No. 094124799, filed on Jul. 22, 2005, the content of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the invention

[0003] The invention generally relates to a liquid crystal display (LCD), and more particularly, to a source driver circuit and method for a liquid crystal display device.

[0004] 2. Description of the Related Art

[0005] FIG. **1**A shows a schematic configuration of a prior LCD device. Referring to FIG. **1**A, a LCD device **100** includes a LCD panel **110**, a source driver circuit **120**, a gate driver circuit **130**, a timing controller **140** and a gamma adjustment circuit **150**. The LCD panel **110** is used to display images. A plurality of data lines **121** and a plurality of scanning lines **131** (e.g. 640×480) are disposed in a grid like arrangement on the LCD panel **110**. A TFT (thin film transistor) **111** and a capacitor **112** are provided in the vicinity of each point of intersection between the data lines **121** and scanning lines **131**. The capacitor **112** includes a pixel electrode **112***a*, a common electrode **112***b* and a liquid crystal layer **112***c*. A gate electrode of TFT **111** is connected to the scanning line **131**, a source electrode is connected to the data line **121**, and a drain electrode is connected to the pixel electrode **112***a* of the capacitor **112**. The gamma adjustment **150** applies at least a reference voltage to the source driver circuit **120**. Besides, the timing controller **140** generates different control signals and control voltages to the source driver circuit **120** and the gate driver circuit **130**.

[0006] If the liquid crystal material is continuously applied with a DC voltage with same polarity, the liquid crystal material will likely be damaged. To prevent the damage to the liquid crystal material, the polarity of the data signal applied to the liquid crystal material is periodically inverted (so-called AC driving), as well know in the art.

[0007] FIG. **1**B shows a schematic configuration of a prior source driver circuit. The source driver circuit **120** consists of a plurality of source driver **160**. Each source driver **160** includes two data buffers **161**, **161'**, a positive digital-to-analog converter **162**, a negative digital-to-analog converter **163**, a positive amplifier **164**, a negative amplifier **165** and a switch module **166** made up of four switches SW**1**~SW**4**. Based on the AC driving, the source driver **160** respectively receives two digital image signals D_1, D_2, and simultaneously receives a set of positive analog voltage signals V_{ref1} and a set of negative analog voltage signals V_{ref2} from the gamma adjustment **150**. After two digital image signals D_1, D_2 are converted and amplified, a positive analog image signal and a negative analog image signal are alternately output from the output terminals S**1**, S**2** of the driver **160** for every predetermined period of time by controlling four switches SW**1**~SW**4**. Four switches SW**1**~SW**4** are controlled by a control signal CS_SW, which includes a first switch control signal, a second switch control signal, a third switch control signal and a fourth switch control signal for respectively controlling switches SW**1**~SW**4**. Since the method of using the control signal CS_SW to control the switches SW**1**~SW**4** is well known, the description is omitted here.

[0008] If motion picture display is conducted on the prior LCD device, an afterimage problem will arise. The cause of this problem is that because the response speed of the liquid crystal material is low and the response time is relatively long. When an object is moving fast in a frame, the liquid crystal is unable to track the path of the object within a frame period, but produces a cumulative response using several frame periods. Several researches have been conducted to overcome the afterimage problem as follows: (1) Intrinsic property: Convert the property of the liquid crystal material into low viscosity. (2) Overdriving: The response of the liquid crystal material can be increased by overdriving each pixel. (3) Black insertion: Following the display of each image for one frame, the entire screen is switched to a black display by inserting the black data, before the image for the next frame is displayed.

[0009] FIG. **2**A shows a timing diagram for sequentially supplying of the gate driving signals to the scanning lines of a conventional LCD device. In U.S. Pat. No. 6,473,077, IBM discloses a liquid crystal display device using black insertion concept. FIG. **2**B shows a timing diagram of sequential gate driving signals output from a gate driver circuit **130** of the liquid crystal display device to the scanning lines. Based on the same black insertion concept, in U.S. Pat. No. 6,819,311, NEC reveals another liquid crystal display device for displaying motion pictures. FIG. **2**C shows a timing diagram of sequential gate driving signals output from a gate driver circuit **130** of another liquid crystal display device for displaying motion pictures to the scanning lines.

[0010] Referring to FIG. **2**A, there is a gate driving signal with a time period T_G supplied to each scanning line within a frame period while the gate driving signal supplied to each scanning line comprises a first trigger pulse P_1 and a second trigger pulse P_2 within a frame period as shown in FIG. **2**B and **2**C.

[0011] As shown in FIG. **2**B, one frame period is divided into two halves. An image for one frame is displayed during the first half of frame period, and the black image is displayed during the second half of frame period. Referring to FIG. **2**C, the gate driver circuit **130** interlacedly activates a pixel line for image data and then another pixel line for black data which is separated by a predetermined number of scanning lines from the pixel line for image data. In this manner, the interlaced activated pixel lines are sequentially displayed on the LCD device. Comparing FIG. **2**A~**2**C, the scanning frequency of the gate driver circuit **130** in FIG. **2**B or FIG. **2**C is doubled, since the width TG of the gate driving signal on each scanning line in FIG. **2**A is reduced into the width $T_G/2$ of the trigger pulse P_1 or P**2** as shown in FIG. **2**B or FIG. **2**C. That is, the operation time of the gate driver circuit **130** is reduced to one-half, and the data driving speed of the source driver circuit **120** is also doubled in order to coordinate with the scanning frequency of the gate driver circuit **130**.

[0012] Although the afterimage problem can be solved with NEC's or IBM's architecture, the gate driver circuit has to alternately generate image data and black insertion data for implementing the black insertion technique. Since image

data and black insertion data are generated by the digital-to-analog converters and the amplifiers within different time periods, the scanning frequency of the gate driver circuit must be doubled, thereby relatively increasing the load of the source driver circuit and the response speed of the digital-to-analog converter in the source driver circuit.

SUMMARY OF THE INVENTION

[0013] In view of the above-mentioned problems, an object of the invention is to provide a source driver circuit for a LCD device, the black insertion voltages for black pixels of which are directly generated by a gamma adjustment circuit of the LCD device.

[0014] Another object of the invention is to provide a source driver circuit for a LCD device, the black insertion voltages for black pixels of which are directly generated by the gamma adjustment circuit of the LCD device and the scanning frequency of the gate driver circuit need not be doubled.

[0015] To achieve the above-mentioned object, the source driver circuit for a LCD device comprises a plurality of source drivers. After having received two digital image signals, each source driver outputs a first driving signal and a second driving signal. Each gate driving signal has a first trigger pulse and a second trigger pulse within a frame period. Each source driver comprises two data buffer, two digital-to-analog converters, two amplifiers, a switch module, a first black insertion unit and a second black insertion unit.

[0016] Each data buffer receives a digital image signal. Each digital-to-analog converter is connected to the data buffer and converts the data output from the data buffers into an analog image signal according to a set of reference analog voltage signals. Two amplifiers respectively receive and amplify the two analog image signals from the two digital-to-analog converters, and then output a first amplified signal and a second amplified signal. After having received the first and the second amplified signals, the switch module outputs two amplified signals as the first and the second driving signals within the first trigger pulse period. The first and the second black insertion units simultaneously receive the first and the second black insertion voltages, and each selectively outputs one of two black insertion voltages as the first driving signal and the second driving signal, respectively, within the second trigger pulse period.

[0017] Still another object of the invention is to provide a source driving method for a LCD device in which a plurality of scanning lines and a plurality of signal lines are disposed in a grid arrangement. Each gate driving signal supplied to each scanning line has a first trigger pulse and a second trigger pulse within a frame period. The source driving method comprises amplifying and outputting a plurality of analog image signals to the plurality of signal lines after converting a plurality of digital image signals into the plurality of analog image signals within the first trigger pulse period, and directly outputting two black insertion voltages to the plurality of signal lines within the second trigger pulse period.

[0018] Based on the black insertion technique, a unique feature of the present invention is that the relative voltages for full black pixels are supplied by the gamma adjustment circuit without use of the amplifier. The invention not only accelerates the driving speed of the source circuit, but also lowers the power consumption of the amplifier. The invention can make flexible use of the first trigger pulse period since the second trigger pulse period is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. **1**A shows a schematic configuration of a prior LCD device.

[0020] FIG. **1**B shows a schematic configuration of a prior source driver circuit.

[0021] FIG. **2**A shows a timing diagram for sequentially supplying of the gate driving signals to the scanning lines of a conventional LCD device.

[0022] FIG. **2**B shows a timing diagram for sequentially supplying of the gate driving signals to the scanning lines of another conventional LCD device.

[0023] FIG. **2**C shows a timing diagram for sequentially supplying of the gate driving signals to the scanning lines of also another conventional LCD device.

[0024] FIG. **3** shows a schematic configuration of a source driver circuit according to the invention.

[0025] FIG. **4**A shows a schematic configuration of a source driver circuit according to a first embodiment of the invention.

[0026] FIG. **4**B shows a timing diagram for sequentially supplying of the gate driving signals to the scanning lines according to the first embodiment of the invention.

[0027] FIG. **4**C shows another timing diagram for sequentially supplying of the gate driving signals to the scanning lines according to the first embodiment of the invention.

[0028] FIG. **5** shows another schematic diagram of the black insertion unit.

[0029] FIG. **6** is a flow chart illustrating the source driving method according to the invention.

[0030] FIG. **7** shows a schematic configuration of a source driver circuit according to a second embodiment of the invention.

[0031] FIG. **8** shows a schematic configuration of a source driver circuit according to a third embodiment of the invention.

[0032] FIG. **9** shows a schematic configuration of a source driver circuit according to a fourth embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0033] The source driver circuit and method for a liquid crystal display device of the invention will be described with reference to the accompanying drawings.

[0034] FIG. **3** shows a schematic configuration of a source driver circuit according to the invention. The source driver circuit **300** for a liquid crystal display device includes a plurality of source drivers **310**. Each source driver **310** comprises two data buffer **161**, **161'**, two digital-to-analog

converters **311**, **311'**, two amplifiers **312**, **312'**, a switch module **166**, a first black insertion unit **313** and a second black insertion unit **313'**.

[**0035**] Data buffers **161**, **161'** in each source driver **310** respectively receive digital image signals D_{n-1}, D_n, where n is an integer greater than 1. Each digital-to-analog converter **311**(**311'**) receives a set of reference analog voltage signals (V_{ref1} or V_{ref2}) and a digital image signal $D_{n-1}(D_n)$, and then selects a corresponding reference analog voltage signal among the set of reference analog voltage signals (V_{ref1} or V_{ref2}) according to the received digital image signal $D_{n-1}(D_n)$. Two amplifiers **312**, **312'** respectively receive and amplify the output signals from two digital-to-analog converters **311**, **311'**, and then sequentially output a first amplified signal and a second amplified signal. The switch module **166** is located between two amplifiers **312**, **312'** and two output terminals S_n, S_{n-1} of the source driver **310**. The first and the second amplified signals output from two amplifiers **312**, **312'** are under the control of the switch module and output to two output terminals S_n, S_{n-1} as the first and the second driving signals in a normal mode. The normal mode and the black insertion mode will be described in FIG. **4**B, **4**C. The first black insertion unit **313** receives the first and the second black insertion voltages, and then output the first black insertion voltage or the second black insertion voltage as the first driving signal in the black insertion mode. Likewise, the second black insertion unit **313'** receives the first and the second black insertion voltages, and then outputs the first black insertion voltage or the second black insertion voltage as the second driving signal in the black insertion mode.

[**0036**] FIG. **4**A shows a schematic configuration of a source driver circuit according to a first embodiment of the invention. FIG. **4**B shows a timing diagram for sequentially supplying of the gate driving signals to the scanning lines according to the first embodiment of the invention. FIG. **4**C shows another timing diagram for sequentially supplying of the gate driving signals to the scanning lines according to the first embodiment of the invention.

[**0037**] Hereinafter, timing diagrams in FIG. **4**B and **4**C are used as examples to detail the operation and the architecture of the invention. Besides, since the source driver circuit consists of a plurality of equal source drivers, only one source driver will be described below.

[**0038**] According to the invention, referring to FIG. **2**A, **4**B, a time period T_G supplied to the scanning lines by the gate source circuit **130** is divided into a first trigger pulse P_1 with a time period T_1 and a second trigger pulse P_2 with a time period T_2 within a frame period. Therefore, the data outputting status is classified into two modes, which includes a normal mode for the first trigger pulse period T_1 and a black insertion mode for the second trigger pulse period T_2.

[**0039**] As shown in FIG. **4**A, according to the first embodiment of the invention, each source driver **410** includes two data buffers **161**, **161'**, a positive digital-to-analog converter **162**, a negative digital-to-analog converter **163**, a positive amplifier **164**, a negative amplifier **165**, a switch module **166** made up of four switches SW**1**~SW**4**, a first black insertion unit **413** and a second black insertion unit **414**. According to a received a digital image signal D_{n-1}, a corresponding analog voltage signal is selected and output as a positive analog image signal among the set of positive analog voltage signals V_{ref1} by the positive digital-to-analog converter **162**. The positive amplifier **164** receives and amplifies the positive analog image signal, and then outputs as a first amplified signal. According to a received a digital image signal D_n, a corresponding analog voltage signal is selected and output as a negative analog image signal among the set of negative analog voltage signals V_{ref2} by the negative digital-to-analog converter **163**. The negative amplifier **165** receives and amplifies the negative analog image signal, and then outputs as a second amplified signal.

[**0040**] Four switches SW**1**~SW**4** make up the switch module **166** and are respectively controlled by a switch control signal CS_SW. The two terminals of the first switch SW**1** are respectively connected to the positive amplifier **164** and the output terminals S_{n-1} of the source driver **410**. The first switch SW**1** receives the first amplified signal and is under the control of a first switch control signal. The two terminals of the second switch SW**2** are respectively connected to the negative amplifier **165** and the output terminals S_{n-1} of the source driver **410**. The second switch SW**2** receives the second amplified signal and is under the control of a second switch control signal. The two terminals of the third switch SW**3** are respectively connected to the positive amplifier **164** and the output terminals S_n of the source driver **410**. The third switch SW**3** receives the first amplified signal and is under the control of a third switch control signal. The two terminals of the fourth switch SW**4** are respectively connected to the negative amplifier **165** and the output terminals S_n of the source driver **410**. The fourth switch SW**4** receives the second signal and is under the control of a fourth control signal.

[**0041**] Black insertion units **413**, **414** simultaneously receive a first black insertion voltage V_{GP1} and a second black insertion voltage V_{GN1}. The black insertion unit **413** includes two switches SW**5**, SW**6** which respectively receive the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1}, and are respectively under the control of the fifth control signal and the sixth control signal. Only one of switches SW**5**, SW**6** is turned ON in the black insertion mode so that one of the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1} is output to the output terminals S_{n-1} of the source driver **410** as the first driving signal. The black insertion units **414** includes two switches SW**7**, SW**8** which respectively receive the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1}, and are respectively under the control of the seventh control signal and the eighth control signal. Only one of switches SW**7**, SW**8** is turned ON in the black insertion mode so that one of the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1} is output to the output terminals S_n of the source driver **410** as the second driving signal.

[**0042**] To prevent the damage to the liquid crystal material, the polarity of the data signal applied to the liquid crystal material is periodically inverted. Therefore, the source driver **410** alternately inverts the data output to the data lines **121** for every predetermined period of time. Accordingly, each of the switches SW**1**~SW**4** is selectively turned ON or OFF. As shown in FIG. **4**B, if the polarity of the image signal is positive within the first trigger pulse period T_1 (in the normal mode), switches SW**1**, SW**4** are turned ON (i.e. short) and the other switches are turned OFF

(i.e. open), so that the positive and the negative analog signals are respectively output from the output terminals S_{n-1}, S_n of the source driver **410**. Contrarily, if the polarity of the image signal is negative, switches SW**2**, SW**3** are turned ON and the other switches are turned OFF, so that the positive and the negative analog signals are respectively output from the output terminals S_n, S_{n-1} of the source driver **410**.

[**0043**] If the polarity of the black insertion voltage is positive within the second trigger pulse period T_2 (in the black insertion mode), switches SW**5**, SW**8** are turned ON and the other switches are turned OFF, so that the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1} are respectively output from the output terminals S_n, S_{n-1} of the source driver **410**. Contrarily, if the polarity of the black insertion voltage is negative, switches SW**6**, SW**7** are turned ON and the other switches are turned OFF, so that the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1} are respectively output from the output terminals S_{n-1}, S_n of the source driver **410**.

[**0044**] Both the positive analog voltage V_{ref1} and the negative analog voltage V_{ref2} are a set of bus signals, which together with the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1} are supplied by the gamma adjustment circuit **150**. The amplitude of the voltages can be directly set or adjusted from a control chip to apply to different LCD panels. It should be noted that a black display followed an image is used to emphasized the contrast; other colors may also be used with different effects. If a color other than black is used for contrast, a corresponding adjustment must be made to the amplitudes of the first black insertion voltage V_{GP1} and the second black insertion voltage V_{GN1}.

[**0045**] According to the invention, the relative voltages for the full black pixels are directly provided by the gamma adjustment circuit rather than by the amplifier any more. Therefore, the second trigger pulse period T_2 is reduced so that the first trigger pulse period T_1 can be flexibly used, thereby varying the timing design of driver circuit. For example, in the timing diagram of FIG. **4**C, there are four scanning lines, whose activated times of the second trigger pulse period T_2 are the same within a frame period. The scanning method used in FIG. **4**C is that a black insertion mode is inserted for every four normal modes by the gate driver circuit **130**; meanwhile, there are four scanning lines (G_1~G_4 or G_j~G_{j+3}) to which the second trigger pulse are supplied within the second trigger pulse period T_2. Hence, the first trigger pulse period T_1 of the invention is greater than the period $T_G/2$ of each pulse on each scanning line in FIG. **2**B, **2**C. In comparison with the prior art, the time for writing the image signals into the capacitances **112** is longer, and the image quality of the LCD panel is better.

[**0046**] FIG. **5** shows another schematic diagram of the black insertion unit. Referring to FIG. **5**, black insertion units **513**,**514** simultaneously receive a first black insertion voltage V_{GP1} and a second black insertion voltage V_{GN1}. The black insertion unit **513** includes three switches SW**5**, SW**6**, SW**9**, which are electrically connected to the output terminals S_{n-1}, S_n of the source driver. The switches SW**5**, SW**6**, SW**9** are respectively under the control of the fifth control signal, the sixth control signal and the ninth control signal. Both of switches SW**5**, SW**6** cannot be turned ON at the same time. The black insertion unit **514** includes three switches SW**7**, SW**8**, SW**10**, which are respectively under the control of the seventh control signal, the eighth control signal and the tenth control signal. Both of switches SW**7**, SW**8** cannot be turned ON at the same time. Wherein, the abovementioned fifth control signal, the sixth control signal, the seventh control signal, the eighth control signal, the ninth control signal and the tenth control signal are controlled by the switch control signal CS_SW. The switches SW**5**~SW**10** can be implemented using PMOS transistors or NMOS transistors or transmission gates.

[**0047**] In the prior art, image signals or black insertion voltages are passed through amplifiers **164**, **165**, which causes a severe power consumption problem. With regard to the demand for doubling the data driving speed of the source driver circuit **120** to coordinate with the speed of the gate driver circuit **130**, the increased data driving speed of the source driver circuit **120** is, however, limited by the time delay resulted from the operations of the amplifiers **164**, **165**. In comparison with the prior art, the black insertion voltages V_{GP1}, V_{GN1} passed through the switches SW**5**, SW**6**, without going through the amplifiers **164**, **165**, can be output faster from the output terminals S_{n-1}, S_n of the source driver according to the invention. Therefore, the second trigger pulse period T_2 can be less than the first trigger pulse period T_1. During the second trigger pulse period T_2, the amplifiers **164**, **165** can be shut down or prepared for next image signals. Hence, the invention not only lowers the power consumption of the amplifiers **164**, **165**, but also accelerates the data driving speed of the source driver circuit **120**. Accordingly, the second trigger pulse period T_2 is reduced so that first trigger pulse period T_1 can be prolonged sufficiently for writing the image signals to capacitances **112**, thereby enhancing the image quality of the LCD panel.

[**0048**] FIG. **6** is a flow chart illustrating the source driving method according to the invention. The source driving method of the invention will be hereinafter described with referring to FIG. **1**, **4**B, **4**C and **6**.

[**0049**] The source driving method of the invention is applied to a LCD panel **110**. A plurality of scanning lines and a plurality of signal lines are disposed in a grid arrangement on the LCD panel **110**. As mentioned above, each gate driving signal supplied to each scanning line has a first trigger pulse P_1 and a second trigger pulse P_2 within a frame period. The source driving method comprises the following steps. In step S**602**, after a plurality of digital image signals have been converted into the plurality of analog image signals, the plurality of analog image signals are amplified and then output to the plurality of signal lines **121** within the first trigger pulse period T_1. In step S**604**, two different black insertion voltages are output to the corresponding signal lines **121** within the second trigger pulse period T_2 according to the polarities. Then, the flow returns to step **602** to process the following digital image signals.

[**0050**] Wherein, the second trigger pulse of each gate driving signal is not synchronized (shown in FIG. **4**B), or the second trigger pulses of N gate driving signals may be synchronized (shown in FIG. **4**C). One of two sets of reference analog voltage signals is a set of positive analog voltage signals V_{ref1}, and the other is a set of negative analog voltage signals V_{ref2}. Likewise, one of two black insertion voltages is a positive voltage V_{GP1}, and the other is a

negative voltage V_{GN1}. Two sets of analog voltage signals and two black insertion voltages are all supplied by the gamma adjustment circuit **150**.

[**0051**] In step S**602**, according to a set of positive analog voltage signals V_{ref1}, a plurality of digital image signals D_{n-1} are converted into a plurality of positive analog image signals and then are amplified. Meanwhile, according to a set of negative analog voltage signals V_{ref2}, a plurality of digital image signals D_n are converted into a plurality of negative analog image signals and then are amplified. Afterwards, two amplified analog image signals are output to the corresponding signal lines according to the predetermined polarity of each liquid crystal layer within the first trigger pulse period T**1**. In step S**604**, two black insertion voltages are output to the corresponding signal lines according to the predetermined polarity of each liquid crystal layer within the second trigger pulse period T_2. The abovementioned operations are based on the periodic inversion of the polarities of the black insertion voltages and the analog image signals output to the signal lines for every predetermined period of time.

[**0052**] FIG. **7** shows a schematic configuration of a source driver circuit according to a second embodiment of the invention.

[**0053**] Referring to FIG. **7**, the source driver circuit **700** includes a plurality of source drivers **710** according to a second embodiment of the invention. Each source driver **710** receives a digital image signal and then outputs a driving signal. Each gate driving signal supplied to the scanning lines is divided into a first trigger pulse P_1 and a second trigger pulse P_2 within a frame period. Each source driver **710** includes a data buffer **161**, a digital-to-analog converter **162**, an amplifier **164**, a switch SW**1** and a black insertion unit **413**.

[**0054**] The switch SW**1** receives the amplified signal output from the amplifier **164**, and then is turned ON (i.e. short) to output the amplified signal as the driving signal within the first trigger pulse period T_1. During the second trigger pulse period T_2, the switch SW**1** is turned OFF (i.e. open) and the black insertion unit **413** outputs a black insertion voltage as the driving signal. The operations of all devices included in the source driver **710** are described above so the description is omitted.

[**0055**] Since the source driver circuits of the second to the fourth embodiments include a plurality of equal source drivers, only one source driver will be described below.

[**0056**] FIG. **8** shows a schematic configuration of a source driver circuit according to a third embodiment of the invention. FIG. **9** shows a schematic configuration of a source driver circuit according to a fourth embodiment of the invention.

[**0057**] Comparing FIG. **7**, **8**, the source drivers of the second and the third embodiments are quite similar, and the difference between them is that the third embodiment doesn't include the switch SW**1**. The operation of the amplifier **812** is controlled by an enable control signal EN_OP in the source driver **810** of the second embodiment. The amplifier **812** is enabled to output an amplified signal as the driving signal within the first trigger pulse period T**1**. During the second trigger pulse period T_2, the enable control signal EN_OP is disabled so that the output terminal of the amplifier **812** is in a high impedance state. Meanwhile, the black insertion unit **413** outputs a black insertion voltage as the driving signal.

[**0058**] Comparing FIG. **7** and FIG. **9**, the source drivers of the second and the fourth embodiments are quite similar and the difference between them is the structure of the black insertion unit. The black insertion unit **413** is implemented using two switches SW**5**, SW**6** in the second embodiment while the black insertion unit **513** is implemented using three switches SW**5**, SW**6** and SW**9** in the fourth embodiment.

[**0059**] The aim of the invention is to make it easier to implement the black insertion technique. With a simple hardware configuration, the invention efficiently achieves the aim of accelerating the data drive speed of source driver circuit and lowering the power consumption of the amplifiers.

[**0060**] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention should not be limited to the specific construction and arrangement shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. A source driver circuit for a liquid crystal display device, the source driver circuit comprising a plurality of source driver, each source driver receiving two digital image signals and outputting a first driving signal and a second driving signal according to a plurality of gate driving signals, each gate driving signal having a first trigger pulse and a second trigger pulse within a frame period, each source driver comprising:

two data buffers for receiving the two digital image signals respectively;

two digital-to-analog converters for receiving the data output from the data buffers, and converting the data into two analog image signals according to two sets of reference analog voltage signals;

two amplifiers for outputting a first amplified signal and a second amplified signal after receiving and amplifying the two analog image signals;

a switch module for receiving the first and the second amplified signals and outputting the first and the second amplified signals as the first and the second driving signals within the first trigger pulse period;

a first black insertion unit for receiving a first black insertion voltage and a second black insertion voltage and outputting the first black insertion voltage or the second black insertion voltage as the first driving signal within the second trigger pulse period; and

a second black insertion unit for receiving the first black insertion voltage and the second black insertion voltage and outputting the first black insertion voltage or the second black insertion voltage as the second driving signal within the second trigger pulse period.

2. The source driver circuit as claimed in claim 1, wherein the first black insertion voltage, the second black insertion

voltage and the two sets of reference analog voltage signals are provided by a gamma adjustment circuit.

3. The source driver circuit as claimed in claim 1, wherein the switch module comprises:

a first switch which receives the first amplified signal and is controlled by a first switch control signal;

a second switch which receives the second amplified signal and is controlled by a second switch control signal;

a third switch which receives the first amplified signal and is controlled by a third switch control signal; and

a fourth switch which receives the second amplified signal and is controlled by a fourth switch control signal;

wherein the output terminals of the first and the second switches are connected to each other where the first driving signal is output, and the output terminals of the third and the fourth switches are connected to each other where the second driving signal is output.

4. The source driver circuit as claimed in claim 3, wherein the first black insertion unit comprises:

a fifth switch which receives the first black insertion voltage and is controlled by a fifth switch control signal; and

a sixth switch which receives the second black insertion voltage and is controlled by a sixth switch control signal;

wherein the output terminals of the fifth and the sixth switches are connected to each other where the output terminals of the first and the second switches are connected, and both the fifth and the sixth switches are not turned ON simultaneously.

5. The source driver circuit as claimed in claim 3, wherein the first black insertion unit comprises:

a fifth switch which receives the first black insertion voltage and is controlled by a fifth switch control signal;

a sixth switch which receives the second black insertion voltage and is controlled by a sixth switch control signal; and

a ninth switch which is controlled by a ninth switch control signal, and the output terminal of which is connected to the output terminals of the first and the second switches;

wherein the output terminals of the fifth and the sixth switches are connected to each other where the input terminal of the ninth switch is connected, and both the fifth and the sixth switches are not turned ON simultaneously.

6. The source driver circuit as claimed in claim 4, wherein the second black insertion unit comprises:

a seventh switch which receives the first black insertion voltage and is controlled by a seventh switch control signal; and

an eighth switch which receives the second black insertion voltage and is controlled by an eighth switch control signal;

wherein the output terminals of the seventh and the eighth switches are connected to each other where the output terminals of the third and the fourth switches are connected, and both the seventh and the eighth switches are not turned ON simultaneously.

7. The source driver circuit as claimed in claim 4, wherein the second black insertion unit comprises:

a seventh switch which receives the first black insertion voltage and is controlled by a seventh switch control signal;

an eighth switch which receives the second black insertion voltage and is controlled by an eighth switch control signal; and

a tenth switch which is controlled by a tenth switch control signal, and the output terminal of which is connected to the output terminals of the first and the second switches;

wherein the output terminals of the seventh and the eighth switches are connected to each other where the input terminal of the tenth switch is connected, and both the seventh and the eighth switches are not turned ON simultaneously.

8. The source driver circuit as claimed in claim 2, wherein one of the first and the second black insertion voltages is positive, and the other is negative.

9. The source driver circuit as claimed in claim 2, wherein one of two sets of the reference analog voltage signals is a set of positive voltage signals, and the other is a set of negative voltage signals.

10. The source driver circuit as claimed in claim 1, wherein the first trigger pulse period is longer than the second trigger pulse period.

11. The source driver circuit as claimed in claim 1, wherein the first trigger pulse period is equal to the second trigger pulse period.

12. A source driving method for a liquid crystal display device, in which a plurality of scanning lines and a plurality of signal lines are disposed in a grid arrangement, each gate driving signal supplied to each scanning line having a first trigger pulse and a second trigger pulse within a frame period, the source driving method comprising the steps of:

amplifying and outputting a plurality of analog image signals to the plurality of signal lines after converting a plurality of digital image signals into the plurality of analog image signals within the first trigger pulse period; and

outputting two black insertion voltages to the plurality of signal lines within the second trigger pulse period;

wherein the two black insertion voltages are provided by a gamma adjustment circuit in the liquid crystal display device.

13. The source driving method as claimed in claim 12, wherein the time of activating the second trigger pulse for each scanning line is different.

14. The source driving method as claimed in claim 13, wherein the first trigger pulse period is longer than the second trigger pulse period.

15. The source driving method as claimed in claim 12, wherein the times of activating the second trigger pulses for every N scanning lines are the same.

16. The source driving method as claimed in claim 15, wherein N is equal to 4.

17. The source driving method as claimed in claim 12, wherein one of the first and the second black insertion voltages is positive, and the other is negative.

18. The source driving method as claimed in claim 17, wherein the step of outputting two black insertion voltages comprises the step of simultaneously outputting two black insertion voltages to the corresponding signal lines according to the predetermined polarity of each liquid crystal layer within the second trigger pulse period.

19. A source driver circuit for a liquid crystal display device, the source driver circuit comprising a plurality of source driver, each source driver receiving a digital image signal and outputting a driving signal according to a plurality of gate driving signals, each gate driving signal supplied to each scanning line having a first trigger pulse and a second trigger pulse within a frame period, each source driver comprising:

a data buffer for receiving the digital image signal;

a digital-to-analog converter for receiving the data output from the data buffer and converting the data into an analog image signal according to a set of reference analog voltage signal;

an amplifier for outputting an amplified signal after receiving and amplifying the analog image signal from the digital-to-analog converter;

a first switch for receiving the amplified signal and outputting the amplified signals as the driving signal within the first trigger pulse period; and

a black insertion unit for receiving a first black insertion voltage and a second black insertion voltage and outputting the first black insertion voltage or the second black insertion voltage as the driving signal within the second trigger pulse period.

20. The source driver circuit as claimed in claim 19, wherein the first black insertion voltage, the second black insertion voltage and the set of reference analog voltage signals are provided by a gamma adjustment circuit.

21. The source driver circuit as claimed in claim 19, wherein the first black insertion unit comprises:

a fifth switch which receives the first black insertion voltage and is controlled by a fifth switch control signal; and

a sixth switch which receives the second black insertion voltage and is controlled by a sixth switch control signal;

wherein the output terminals of the fifth and the sixth switches are connected to each other where the output terminal of the first switches is connected, and both the fifth and the sixth switches are not turned ON simultaneously.

22. The source driver circuit as claimed in claim 19, wherein the black insertion unit comprises:

a fifth switch which receives the first black insertion voltage and is controlled by a fifth switch control signal;

a sixth switch which receives the second black insertion voltage and is controlled by a sixth switch control signal; and

a ninth switch which is controlled by a ninth switch control signal, and the output terminal of which is connected to the output terminals of the first and the second switches;

wherein the output terminals of the fifth and the sixth switches are connected to each other where the input terminal of the ninth switch is connected, and both the fifth and the sixth switches are not turned ON simultaneously.

23. The source driver circuit as claimed in claim 19, wherein one of the first and the second black insertion voltages is positive, and the other is negative.

24. The source driver circuit as claimed in claim 19, wherein the first trigger pulse period is longer than the second trigger pulse period.

25. The source driver circuit as claimed in claim 19, wherein the first trigger pulse period is equal to the second trigger pulse period.

26. A source driver circuit for a liquid crystal display device, the source driver circuit comprising a plurality of source driver, each source driver receiving a digital image signal and outputting a driving signal according to a plurality of gate driving signals, each gate driving signal supplied to each scanning line having a first trigger pulse and a second trigger pulse within a frame period, each source driver comprising:

a data buffer for receiving the digital image signal;

a digital-to-analog converter for receiving the data output from the data buffer and converting the data into an analog image signal according to a set of reference analog voltage signal;

an amplifier which is controlled by an enable control signal and outputs an amplified signal as the driving signal within the first trigger pulse period after receiving and amplifying the analog image signal from the digital-to-analog converter; and

a black insertion unit for receiving a first black insertion voltage and a second black insertion voltage and outputting the first black insertion voltage or the second black insertion voltage as the driving signal within the second trigger pulse period;

wherein the amplifier outputs the driving signal while the enable control signal is enabled within the first trigger pulse period, and the output terminal of the amplifier is in a high impedance state while the enable control signal is disabled.

27. The source driver circuit as claimed in claim 26, wherein the first black insertion voltage, the second black insertion voltage and the set of reference analog voltage signals are provided by a gamma adjustment circuit.

28. The source driver circuit as claimed in claim 26, wherein the black insertion unit comprises:

a fifth switch which receives the first black insertion voltage and is controlled by a fifth switch control signal; and

a sixth switch which receives the second black insertion voltage and is controlled by a sixth switch control signal;

wherein the output terminals of the fifth and the sixth switches are connected to each other where the output

terminal of the first switches is connected, and both the fifth and the sixth switches are not turned ON simultaneously.

29. The source driver circuit as claimed in claim 26, wherein the first black insertion unit comprises:

a fifth switch which receives the first black insertion voltage and is controlled by a fifth switch control signal;

a sixth switch which receives the second black insertion voltage and is controlled by a sixth switch control signal; and

a ninth switch which is controlled by a ninth switch control signal, and the output terminal of which is connected to the output terminals of the first and the second switches;

wherein the output terminals of the fifth and the sixth switches are connected to each other where the input terminal of the ninth switch is connected, and both the fifth and the sixth switches are not turned ON simultaneously.

30. The source driver circuit as claimed in claim 26, wherein one of the first and the second black insertion voltages is positive, and the other is negative.

31. The source driver circuit as claimed in claim 26, wherein the first trigger pulse period is longer than the second trigger pulse period.

32. The source driver circuit as claimed in claim 26, wherein the first trigger pulse period is equal to the second trigger pulse period.

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摘要(译)

本发明涉及一种用于LCD器件的源极驱动器电路和方法。源极驱动器电路包括多个源极驱动器。每个源驱动器包括两个数据缓冲器，两个数模转换器，两个放大器，一个开关模块和两个黑色插入单元。本发明使用黑色插入单元直接提供黑插入步骤中所需的黑色插入电压，而不使用数模转换器和放大器，从而实现更高的源极驱动器电路的驱动速度和更低的功率放大器。