



US 20030222838A1

(19) **United States**(12) **Patent Application Publication**(10) **Pub. No.: US 2003/0222838 A1****Iida et al.**(43) **Pub. Date:****Dec. 4, 2003**(54) **LIQUID CRYSTAL DISPLAY DEVICE****Publication Classification**

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(51) **Int. Cl.⁷** **G09G 3/36**
(52) **U.S. Cl.** **345/87**

(57) **ABSTRACT**

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The present invention realizes a liquid crystal display device which forms a miniaturized low dielectric strength drive circuit on a substrate on which a display part is also formed. Apart from a drive circuit which supplies gray scale voltages to pixels, a circuit which lowers the pixel potential and realizes alternating driving is provided. Signals of positive polarity are written in a pixel electrode and, after writing, the potential of the pixel electrode is lowered using the capacitance connected to the pixel electrode. Further, between the circuit which lowers the pixel potential and a display region, a pull-up circuit for assisting off-switching is provided for reducing rounding of waveforms of scanning signals is provided.

(21) Appl. No.: **10/445,987**(22) Filed: **May 28, 2003**(30) **Foreign Application Priority Data**

May 29, 2002 (JP) 2002-154947

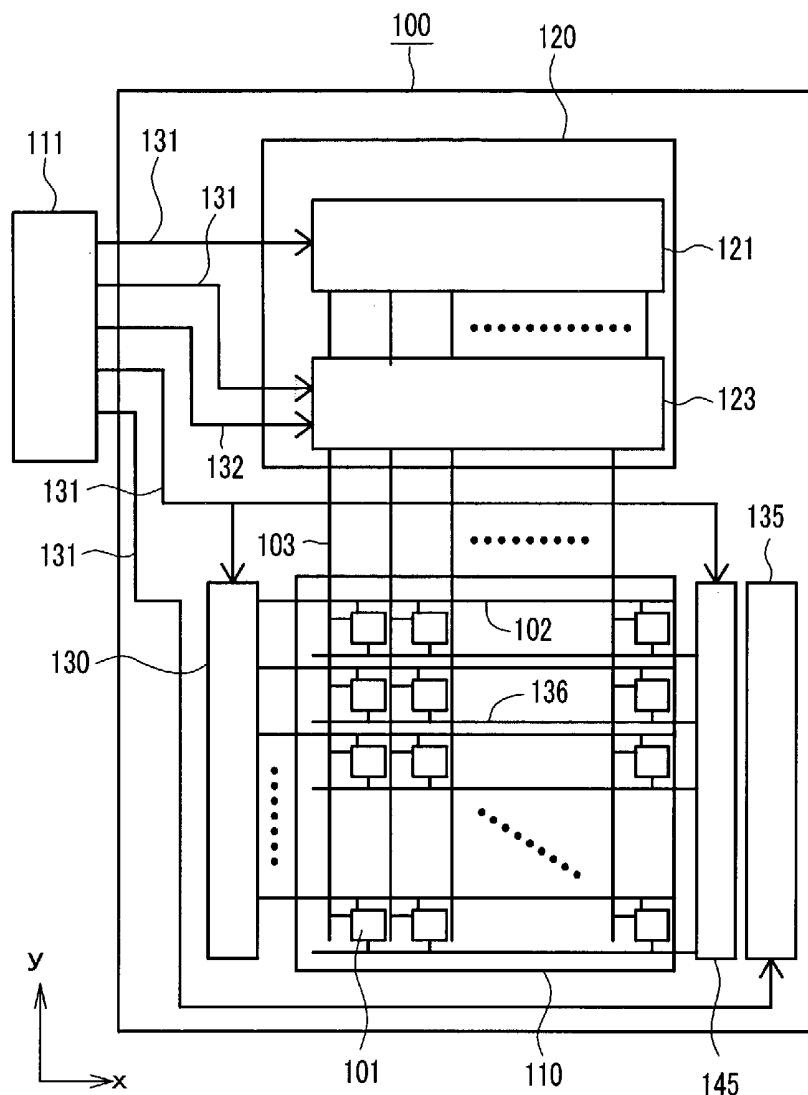


FIG. 1

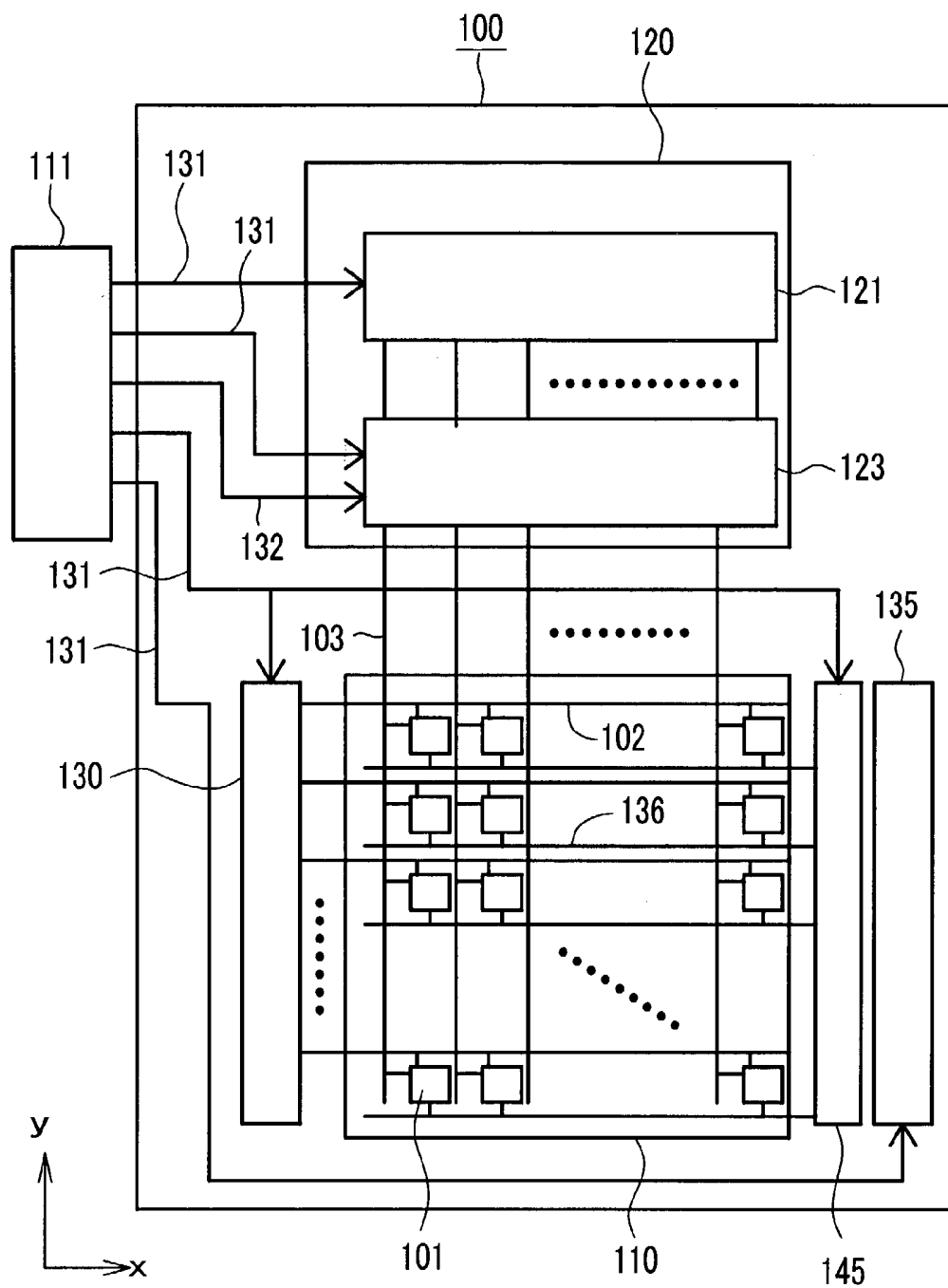


FIG. 3A

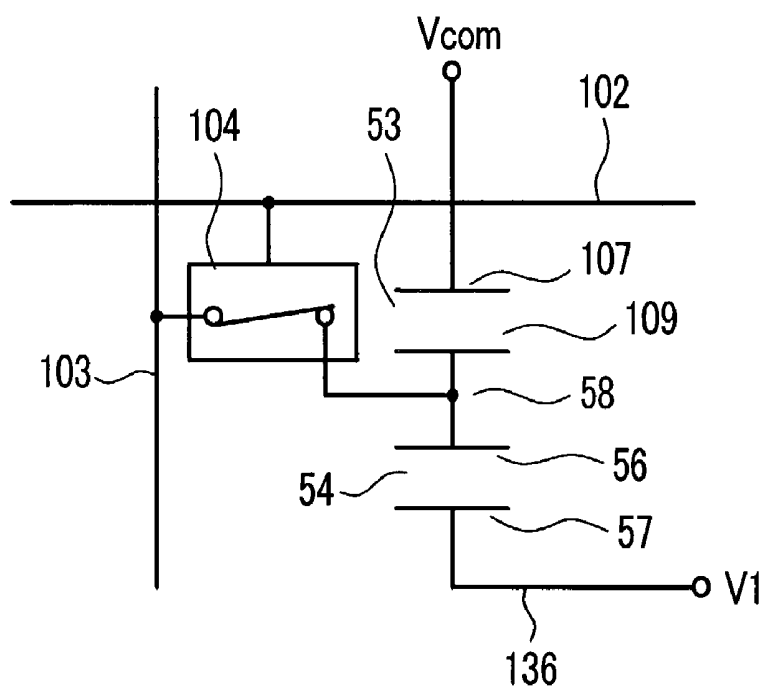


FIG. 3B

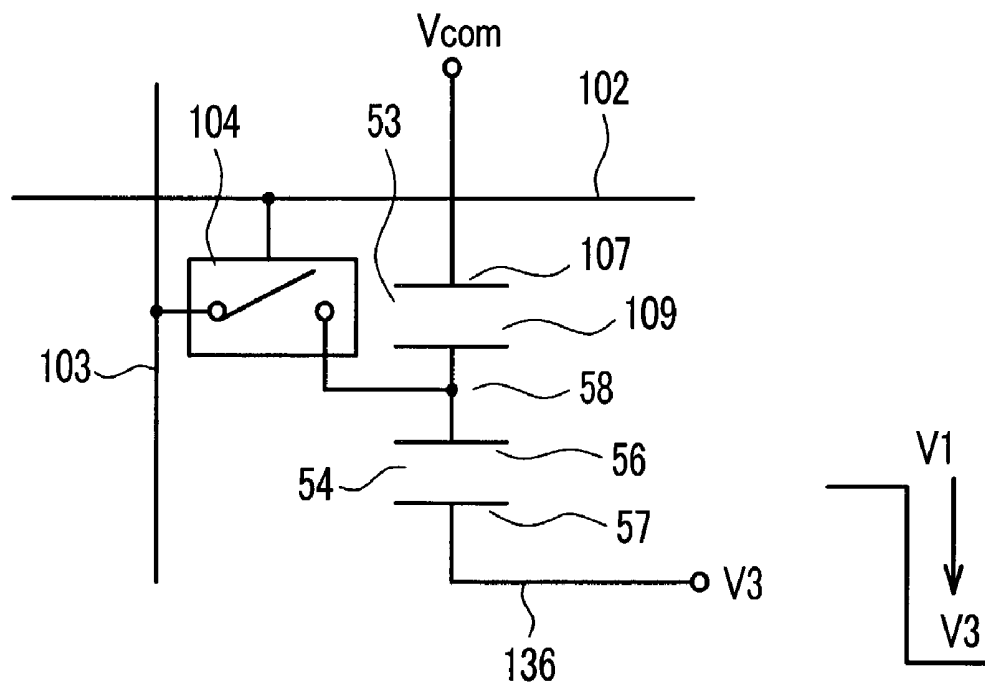


FIG. 4

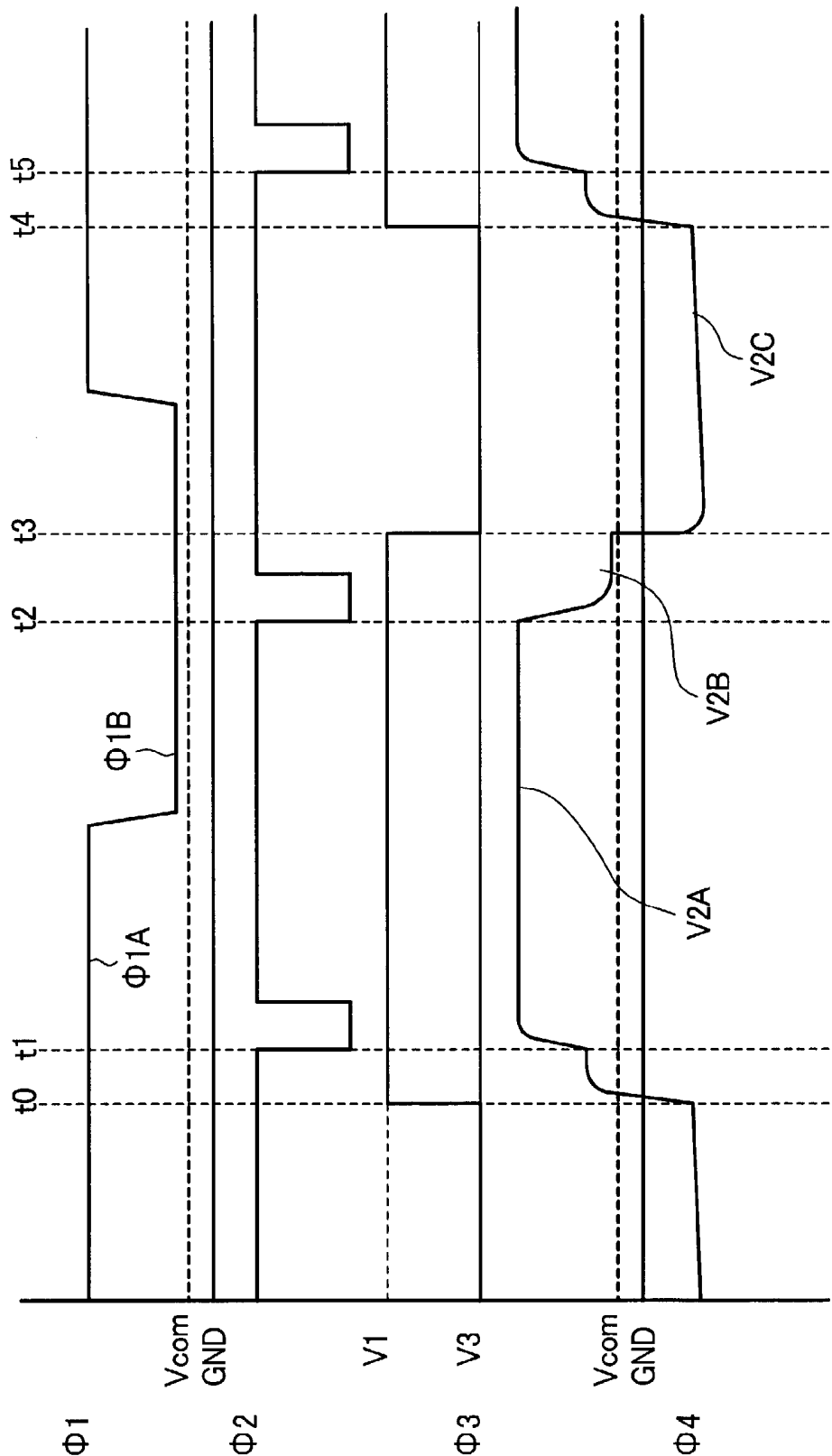


FIG. 5

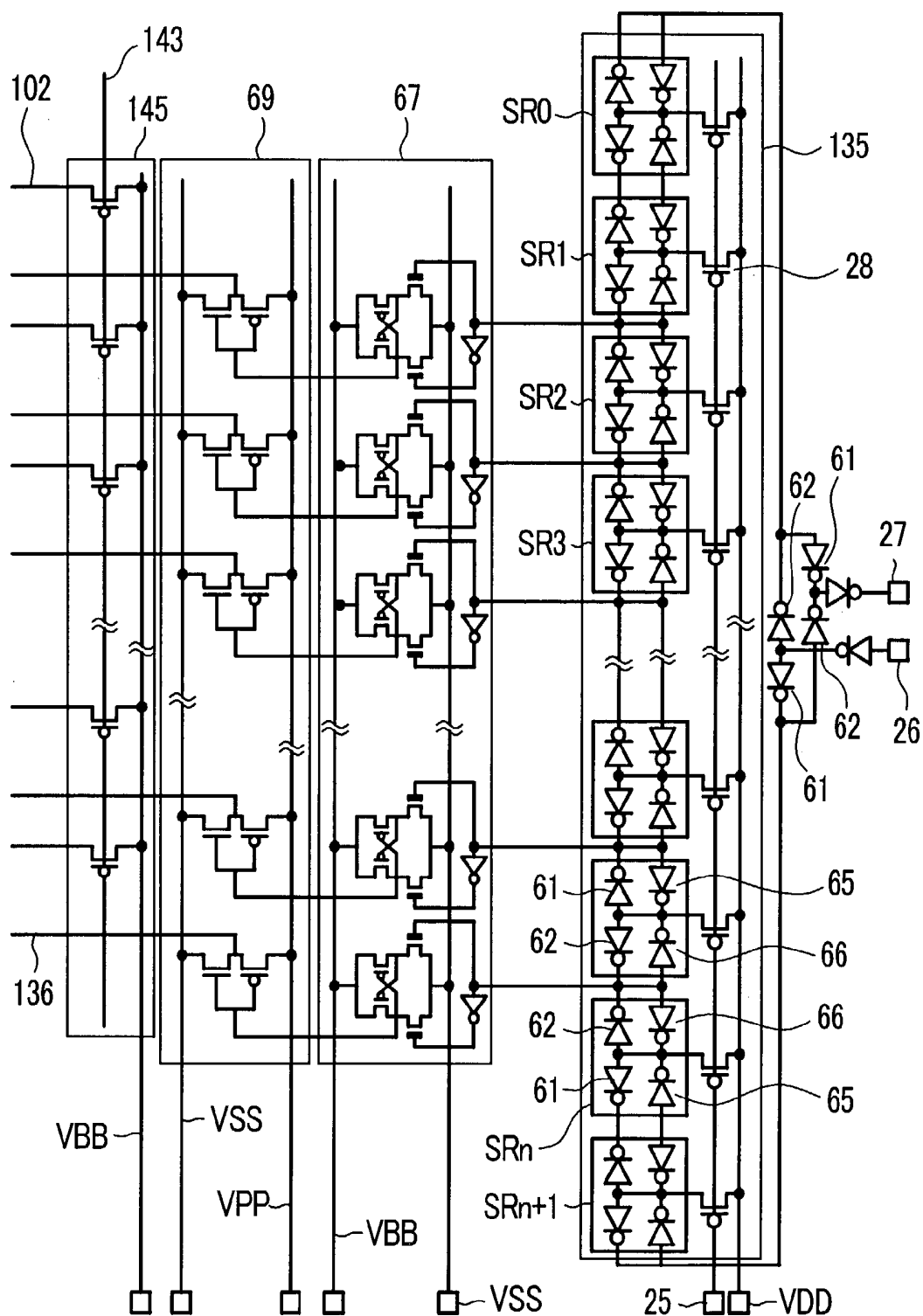


FIG. 6A

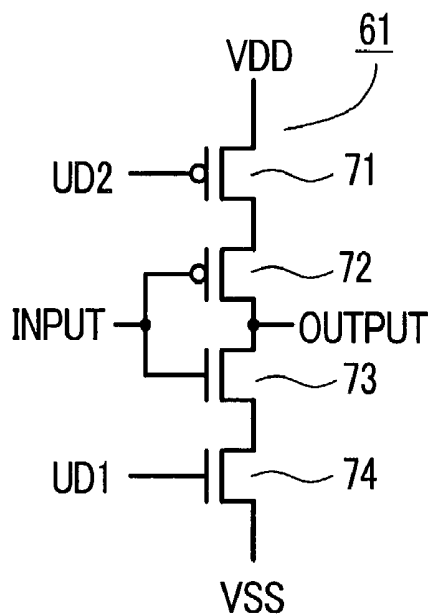


FIG. 6B

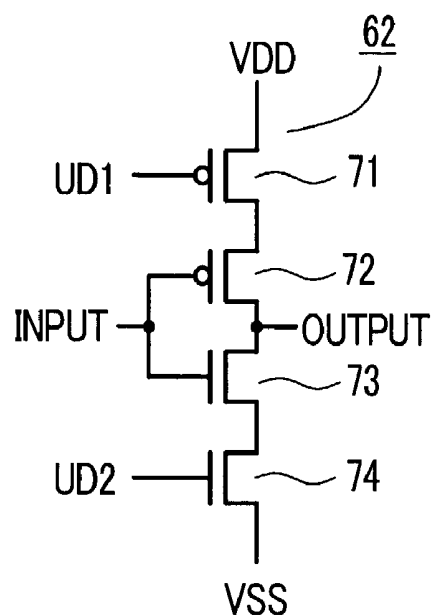


FIG. 6C

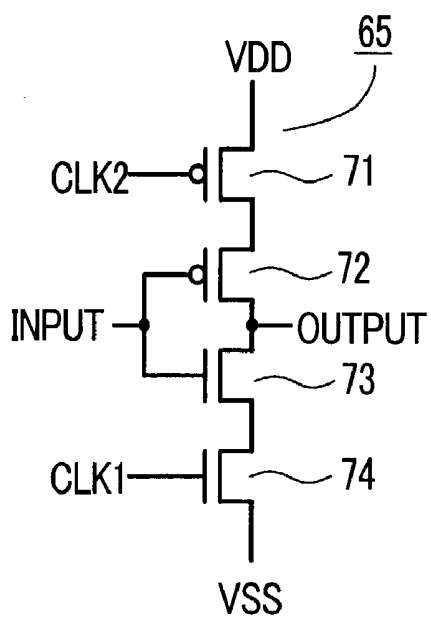


FIG. 6D

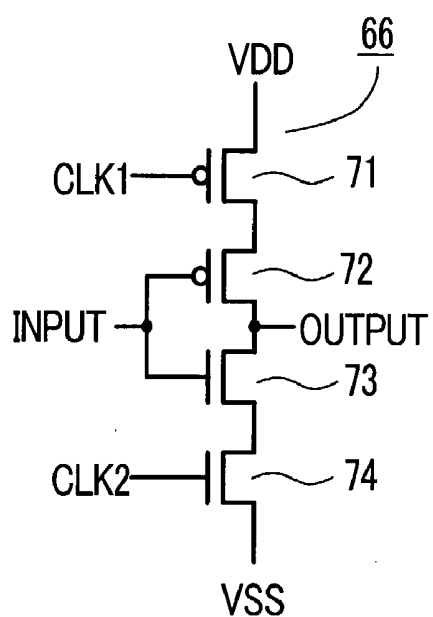


FIG. 7

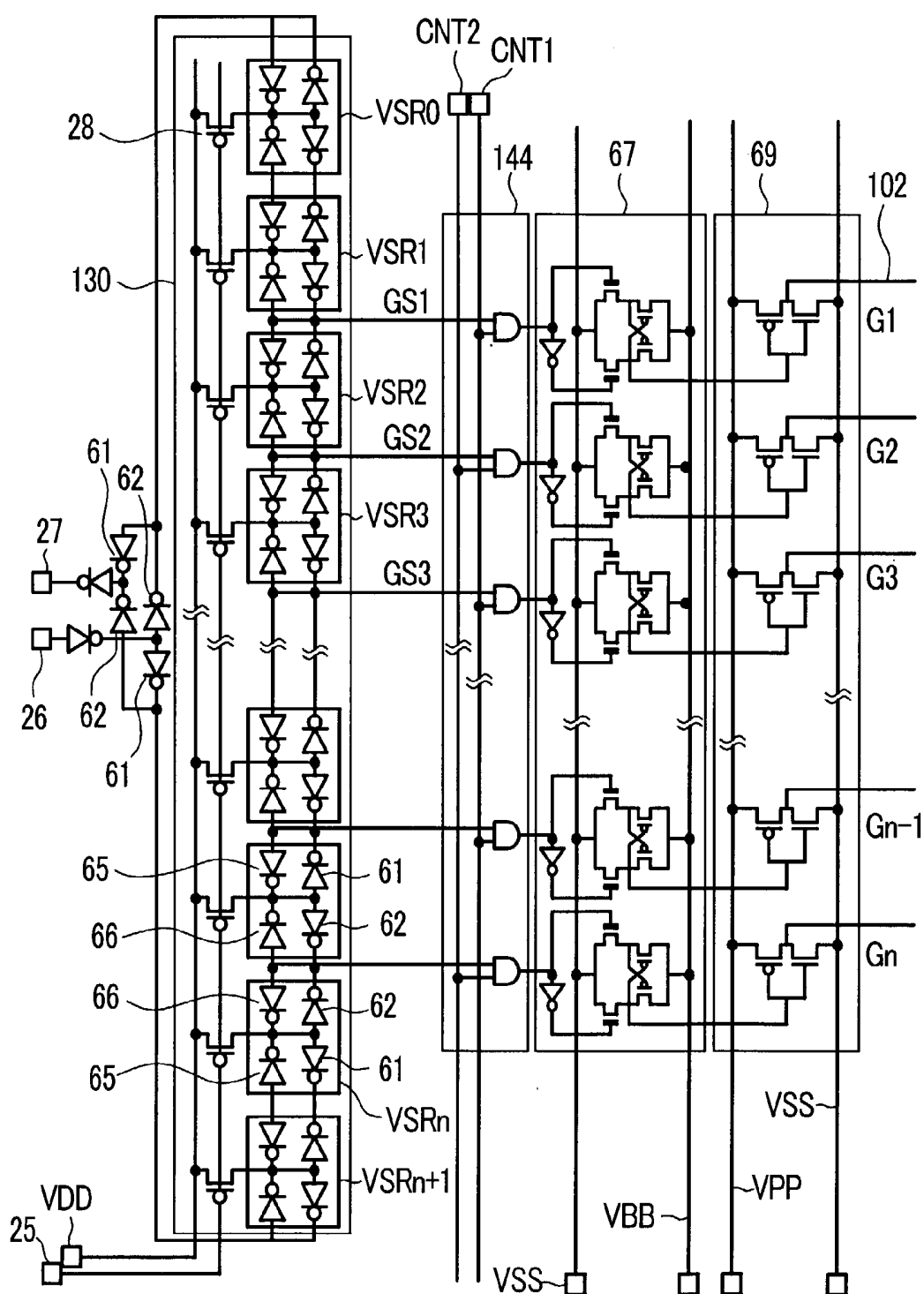


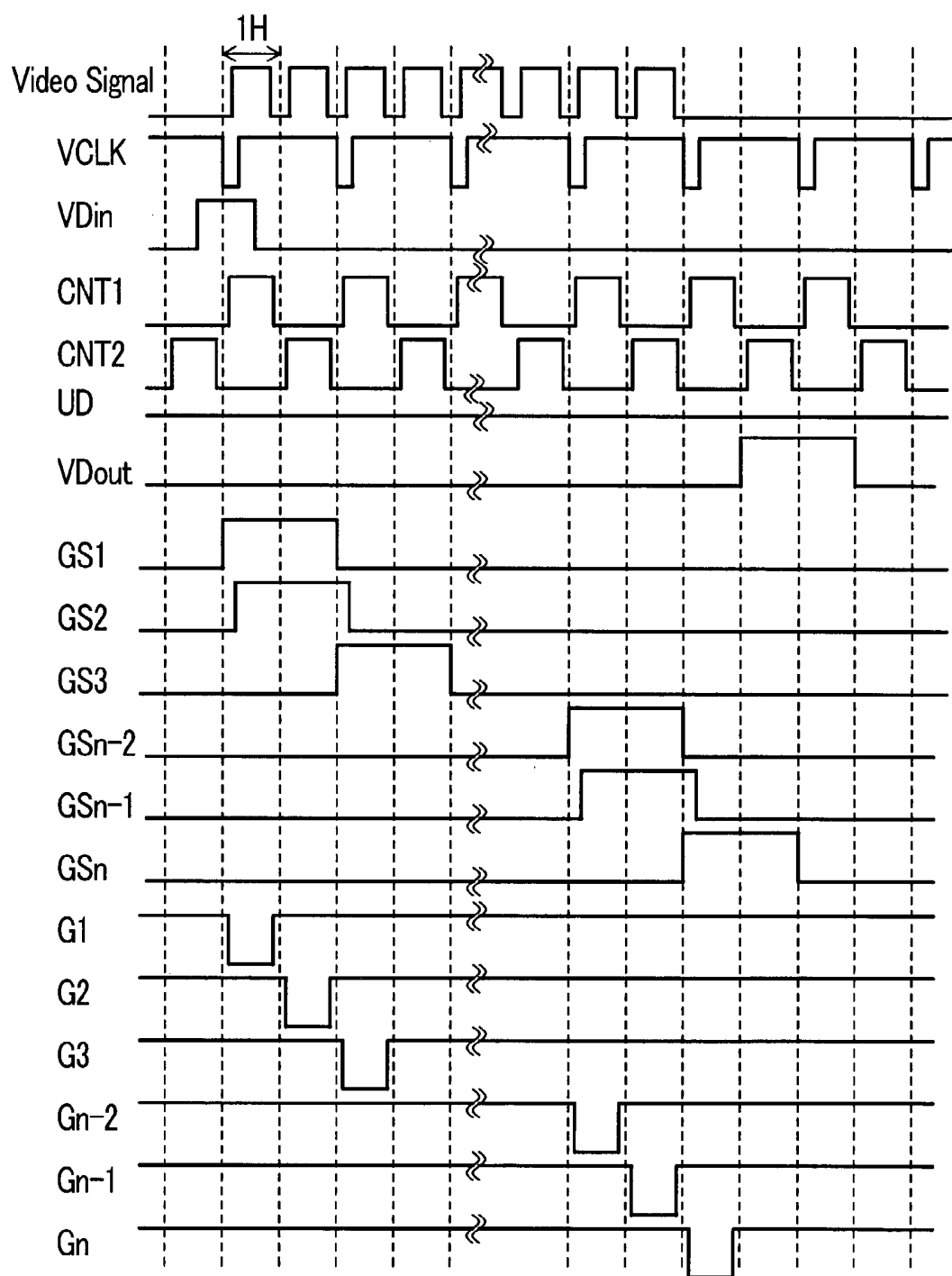
FIG. 8

FIG. 9

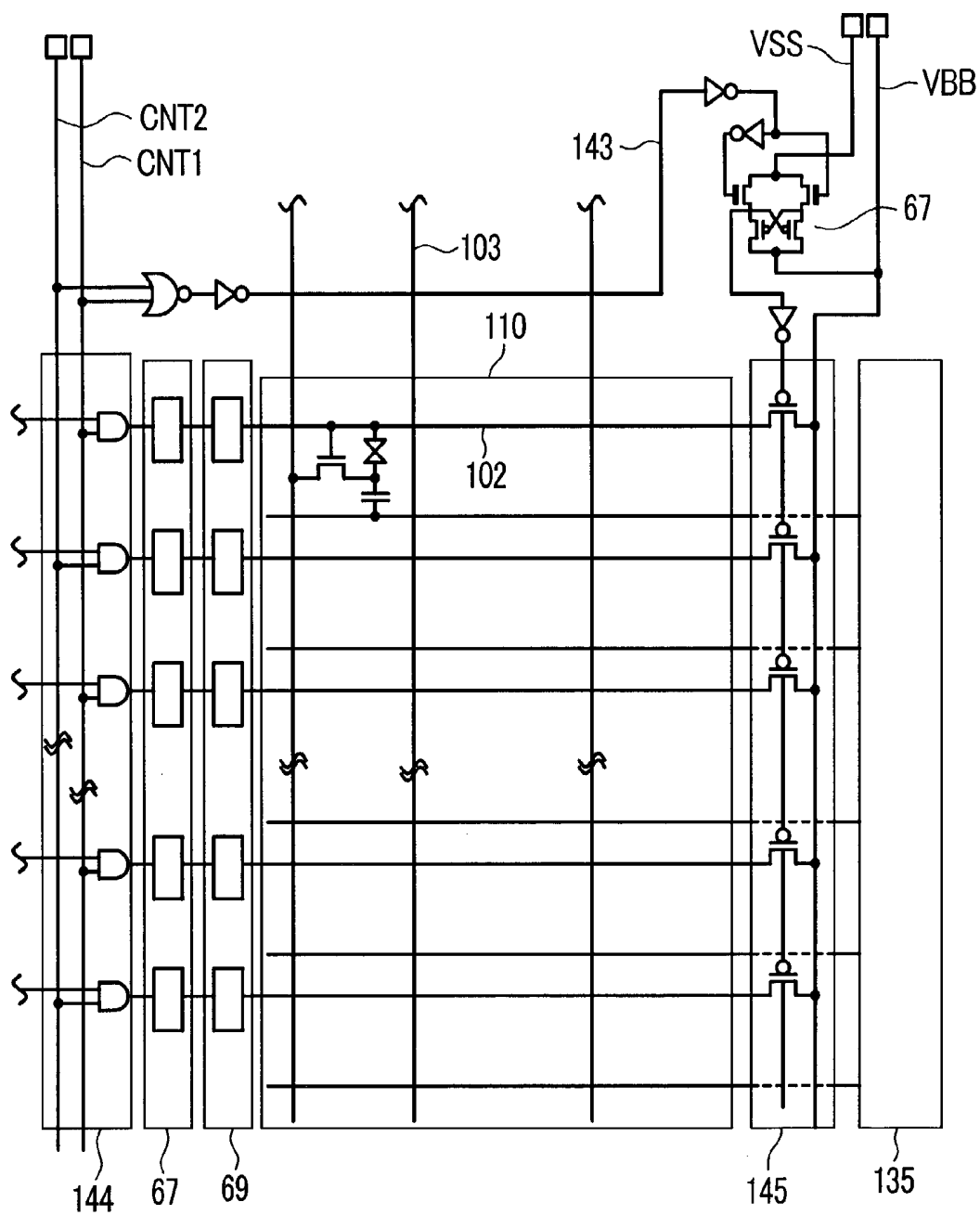


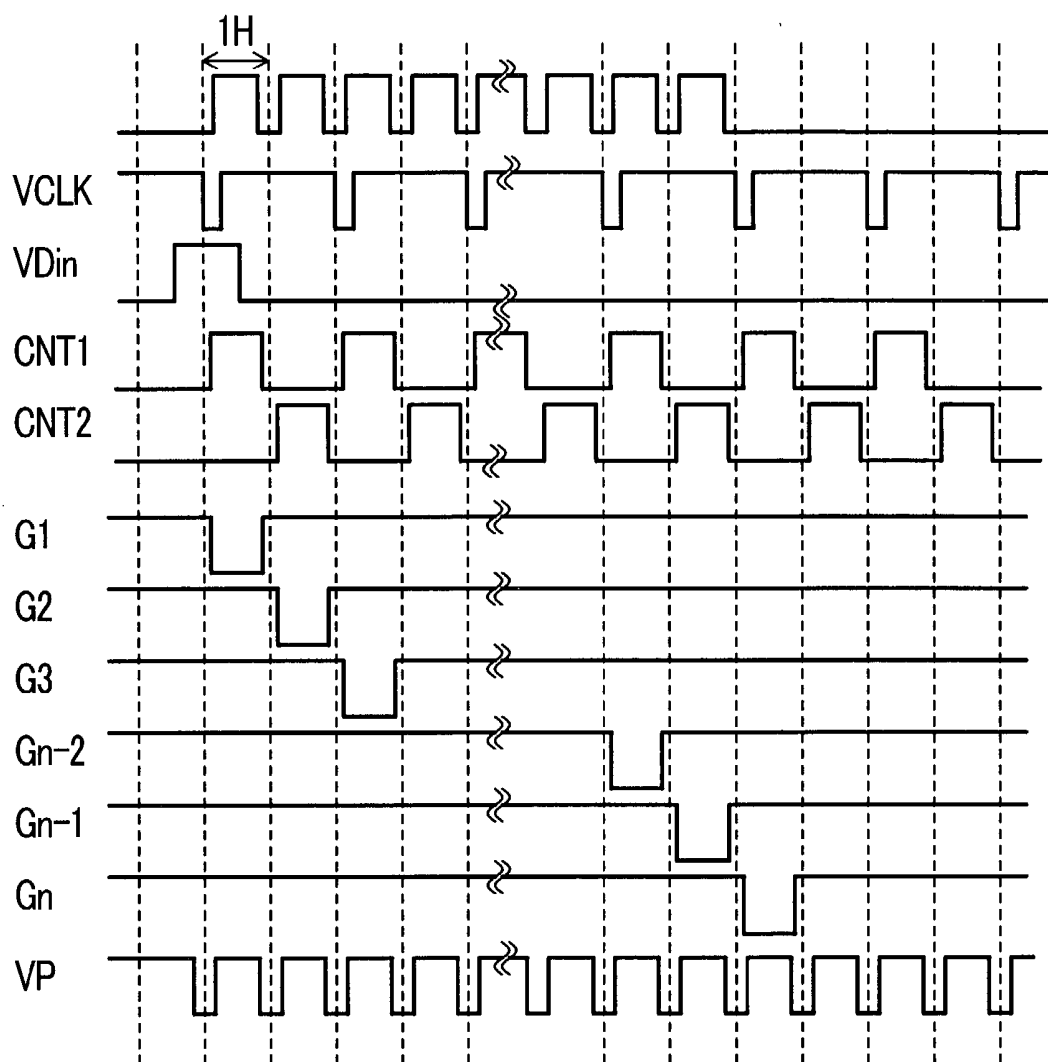
FIG. 10

FIG. 11

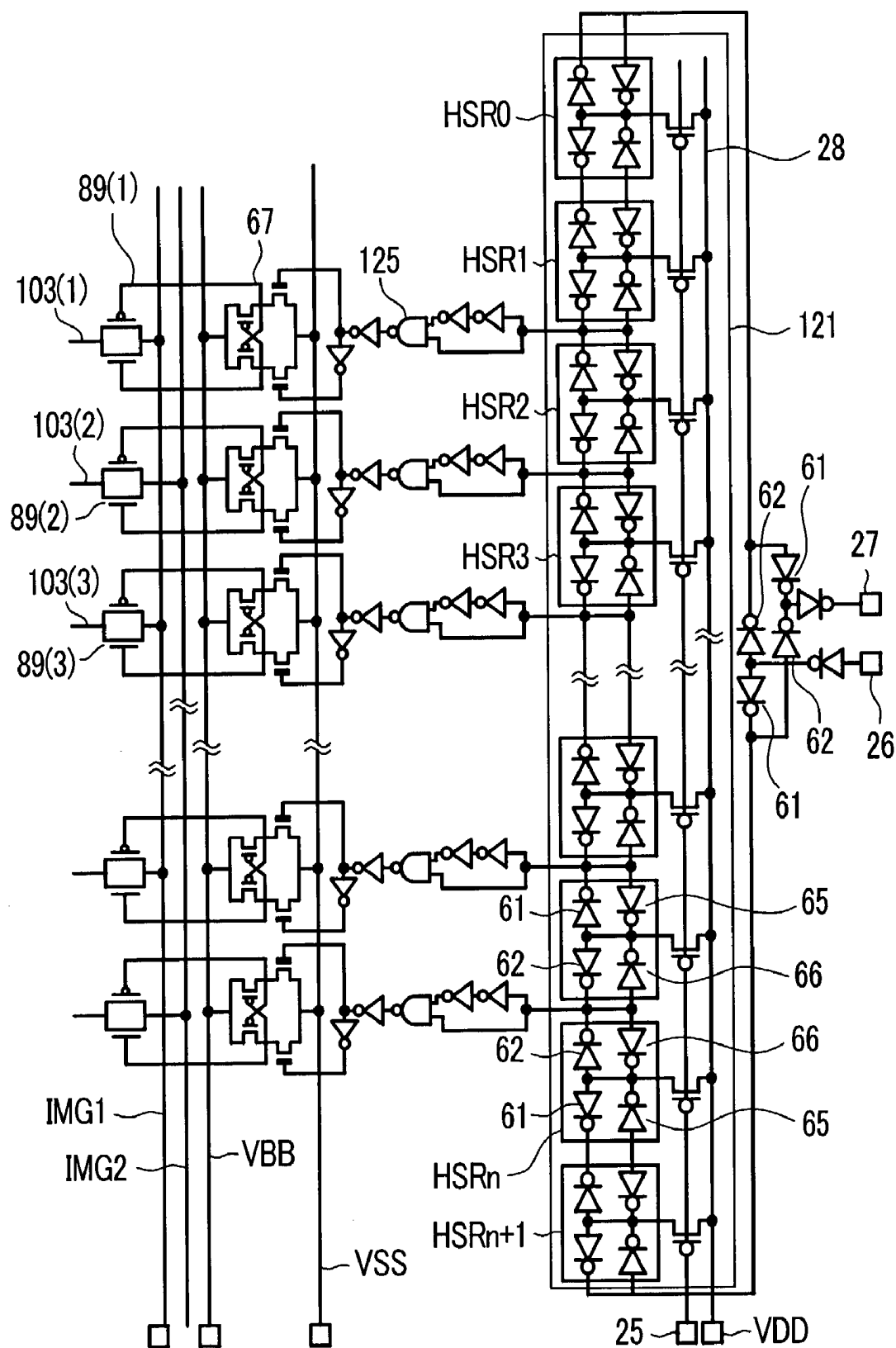


FIG. 12

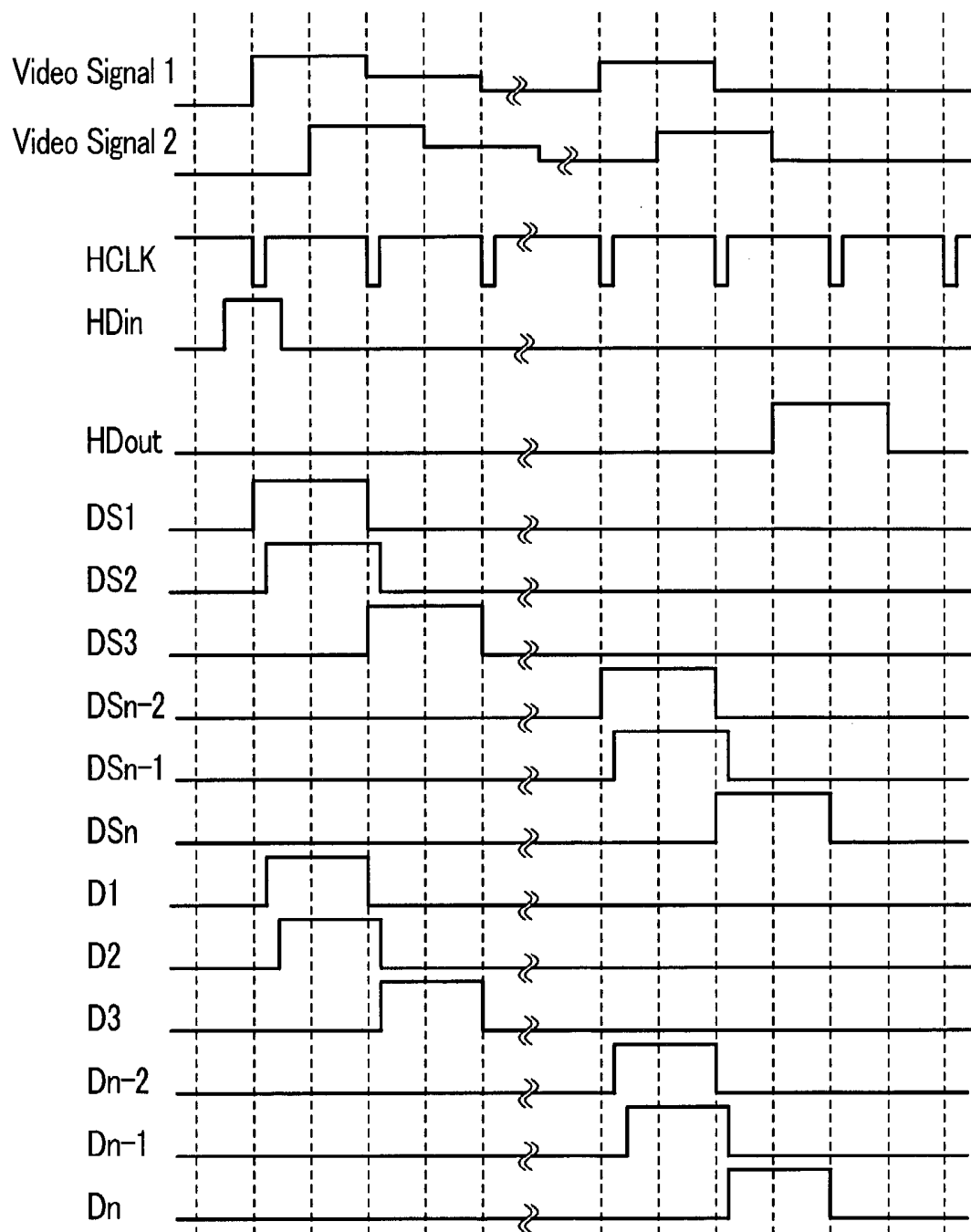


FIG. 14

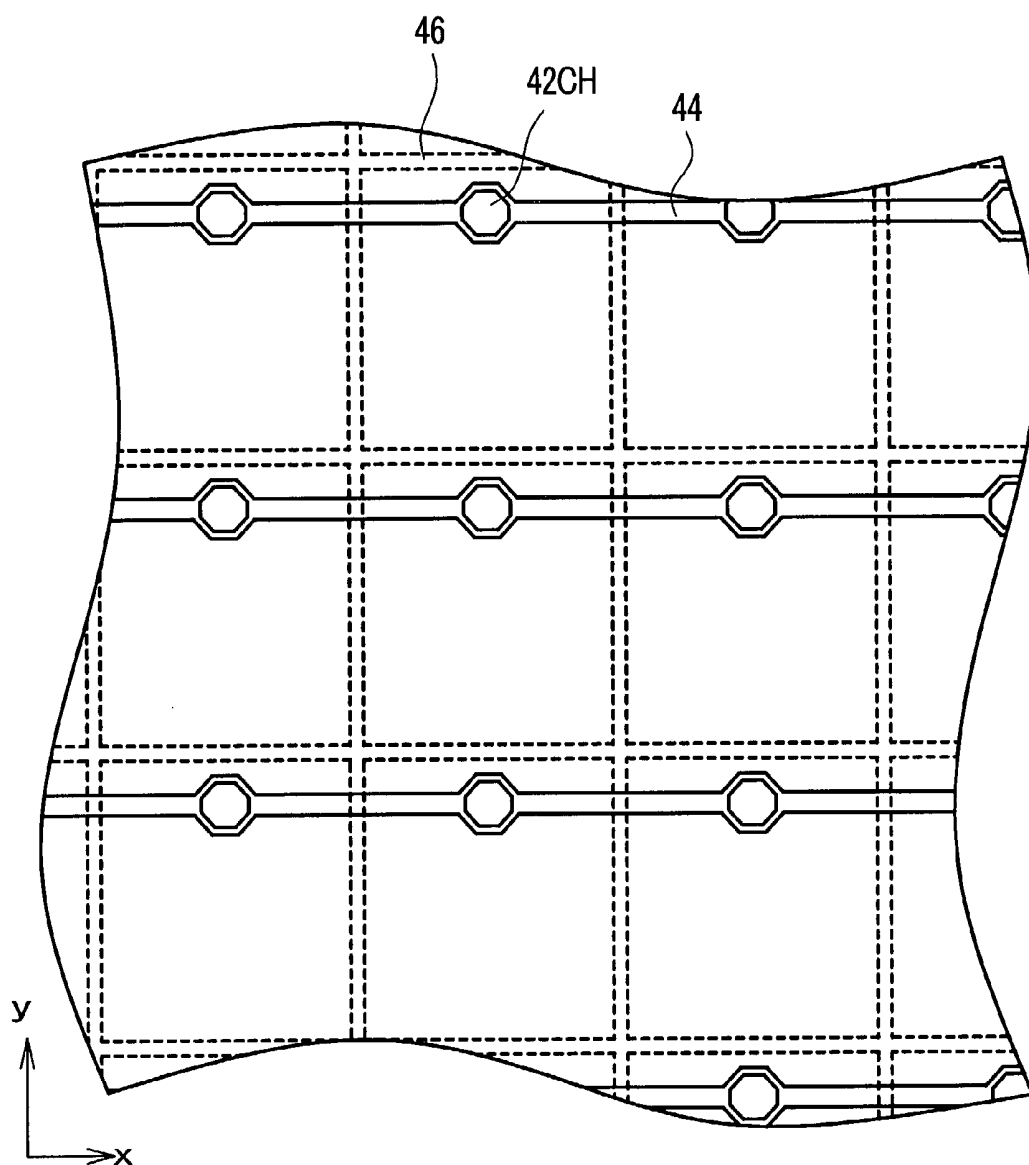


FIG. 15A

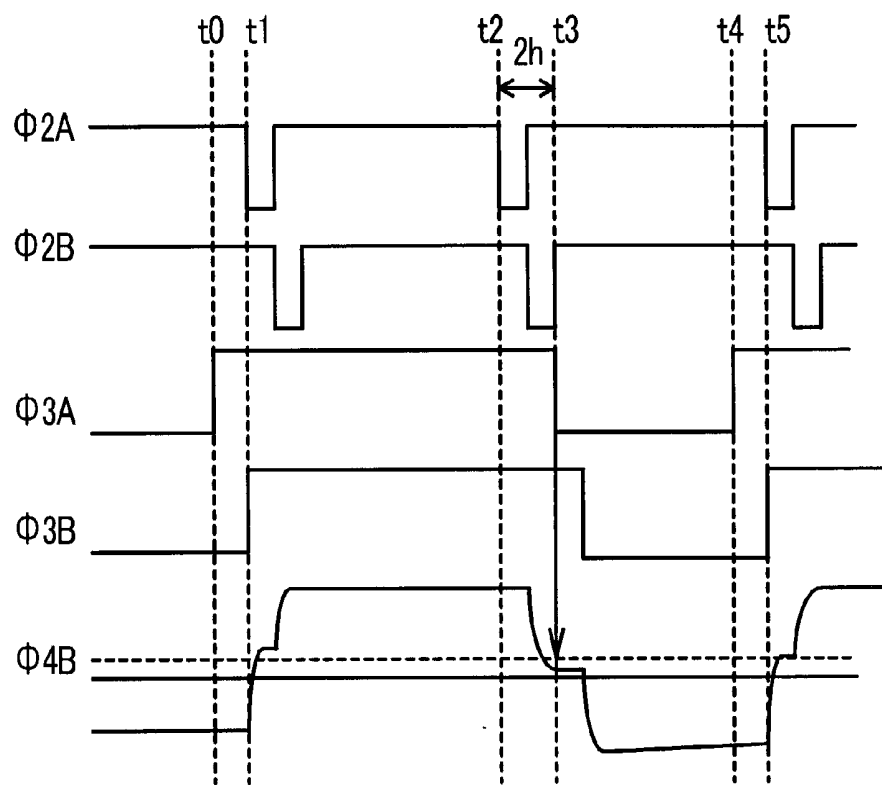


FIG. 15B

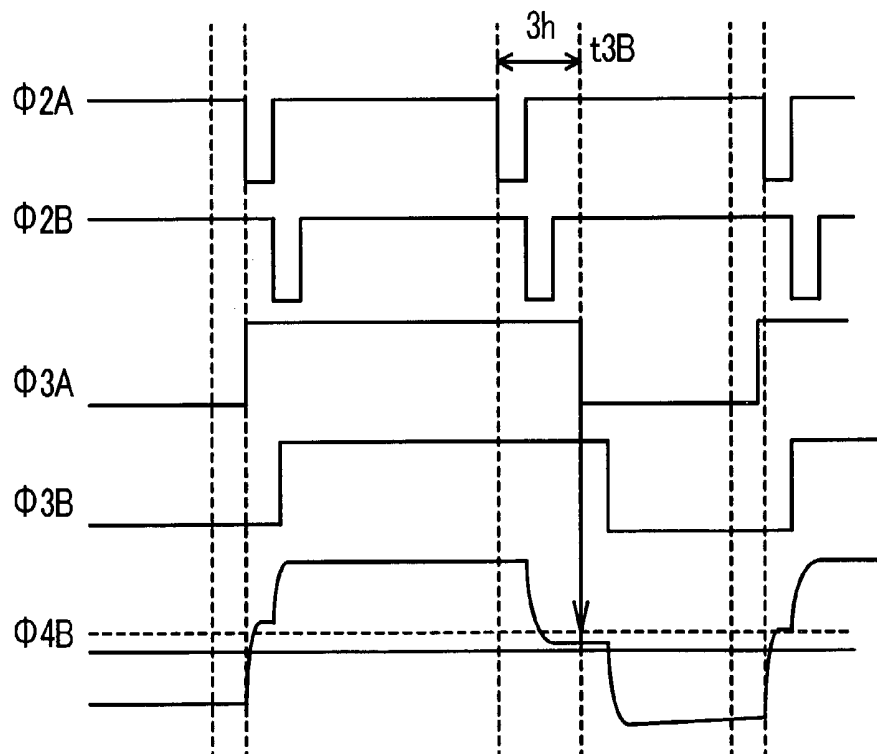


FIG. 16A

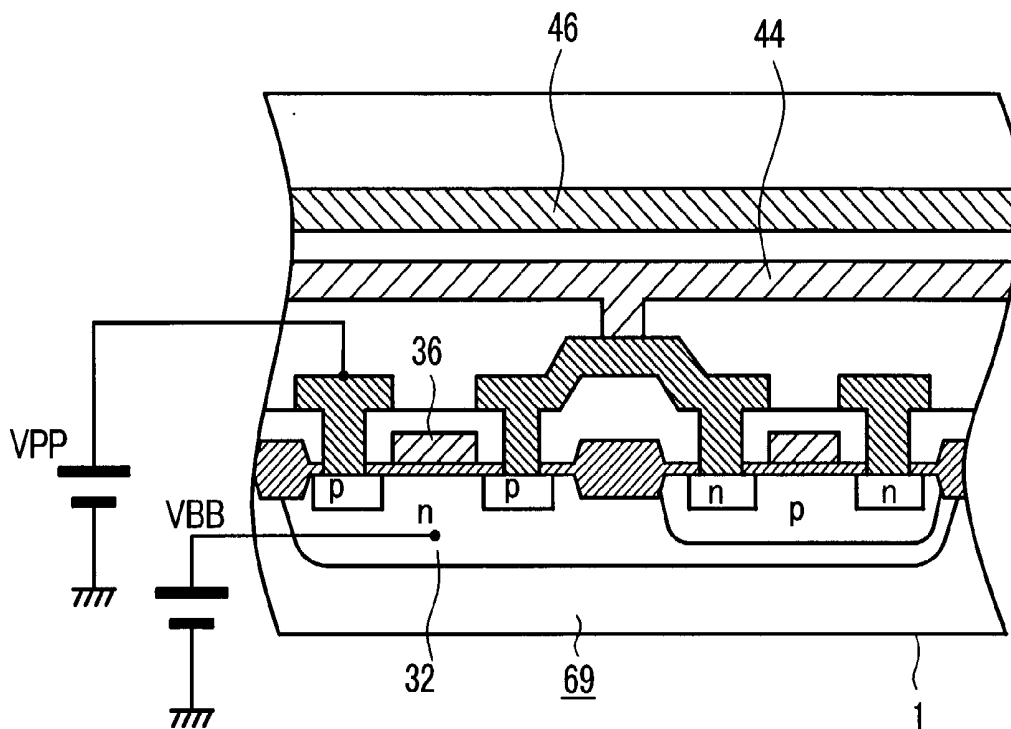


FIG. 16B

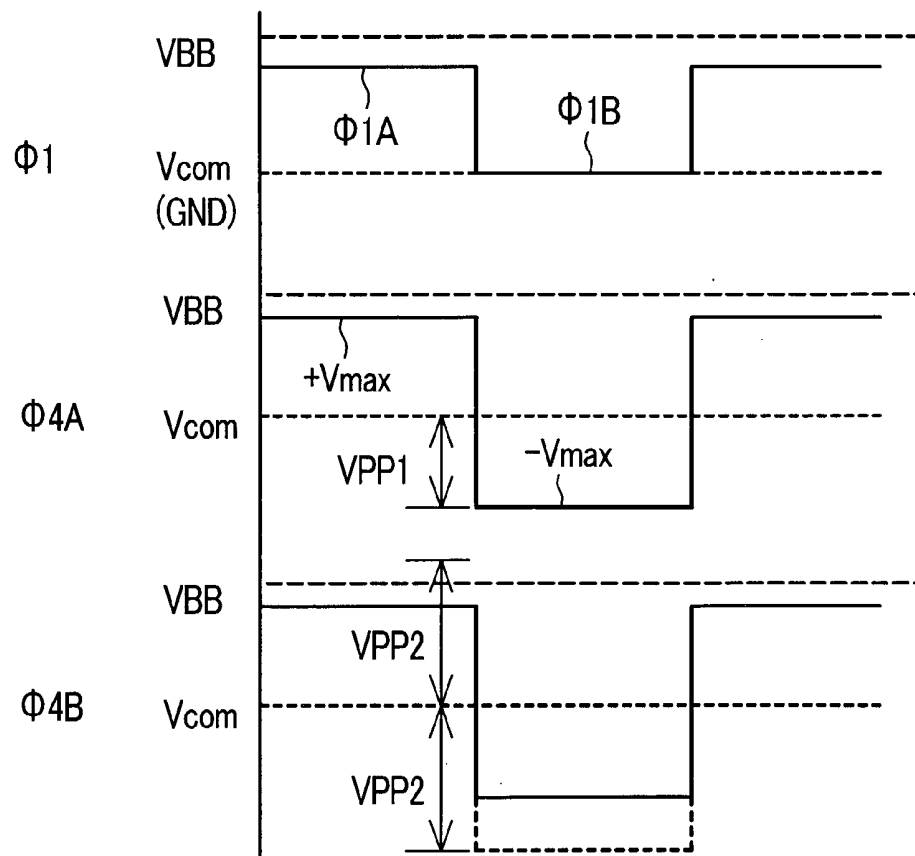


FIG. 17

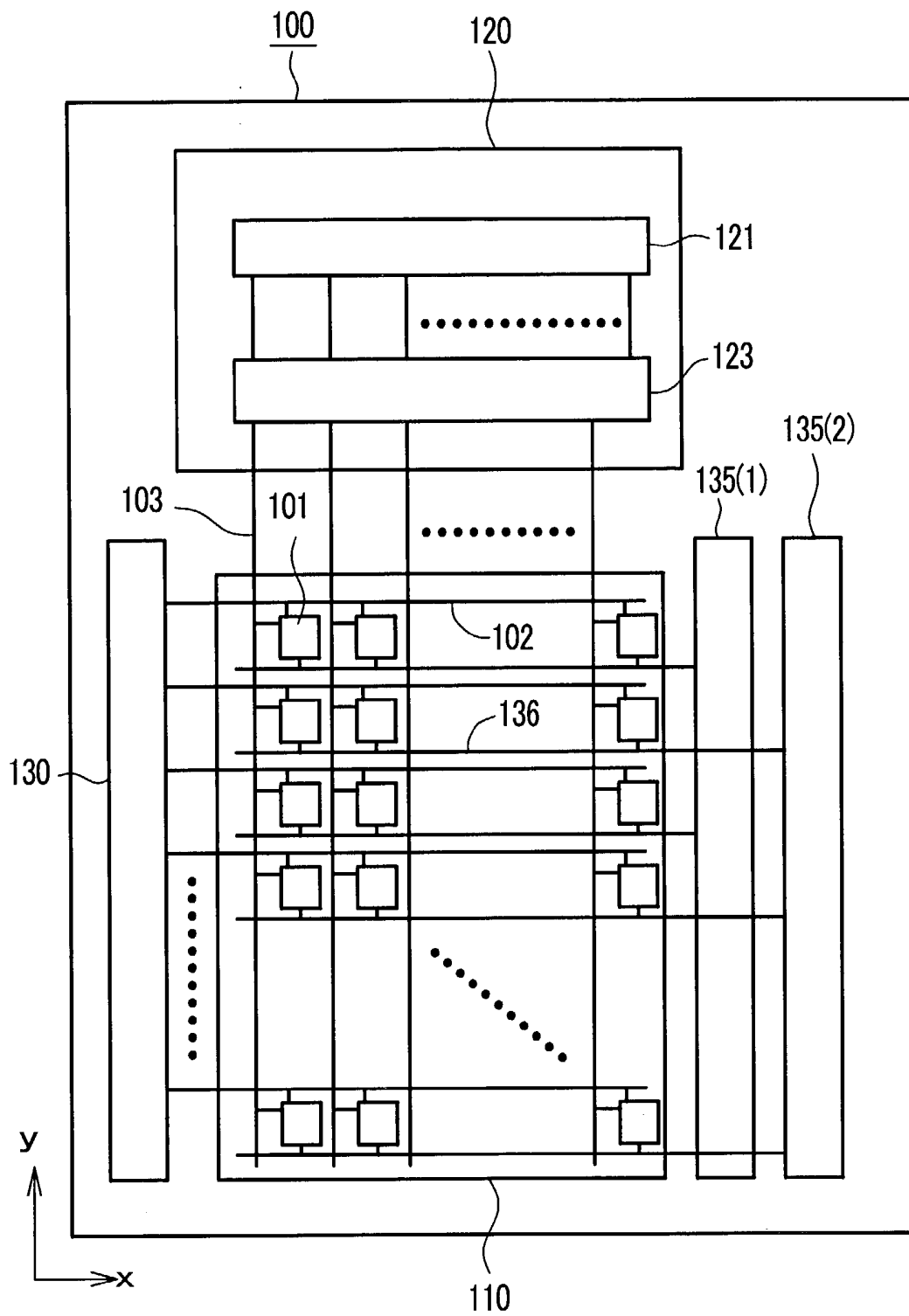


FIG. 18

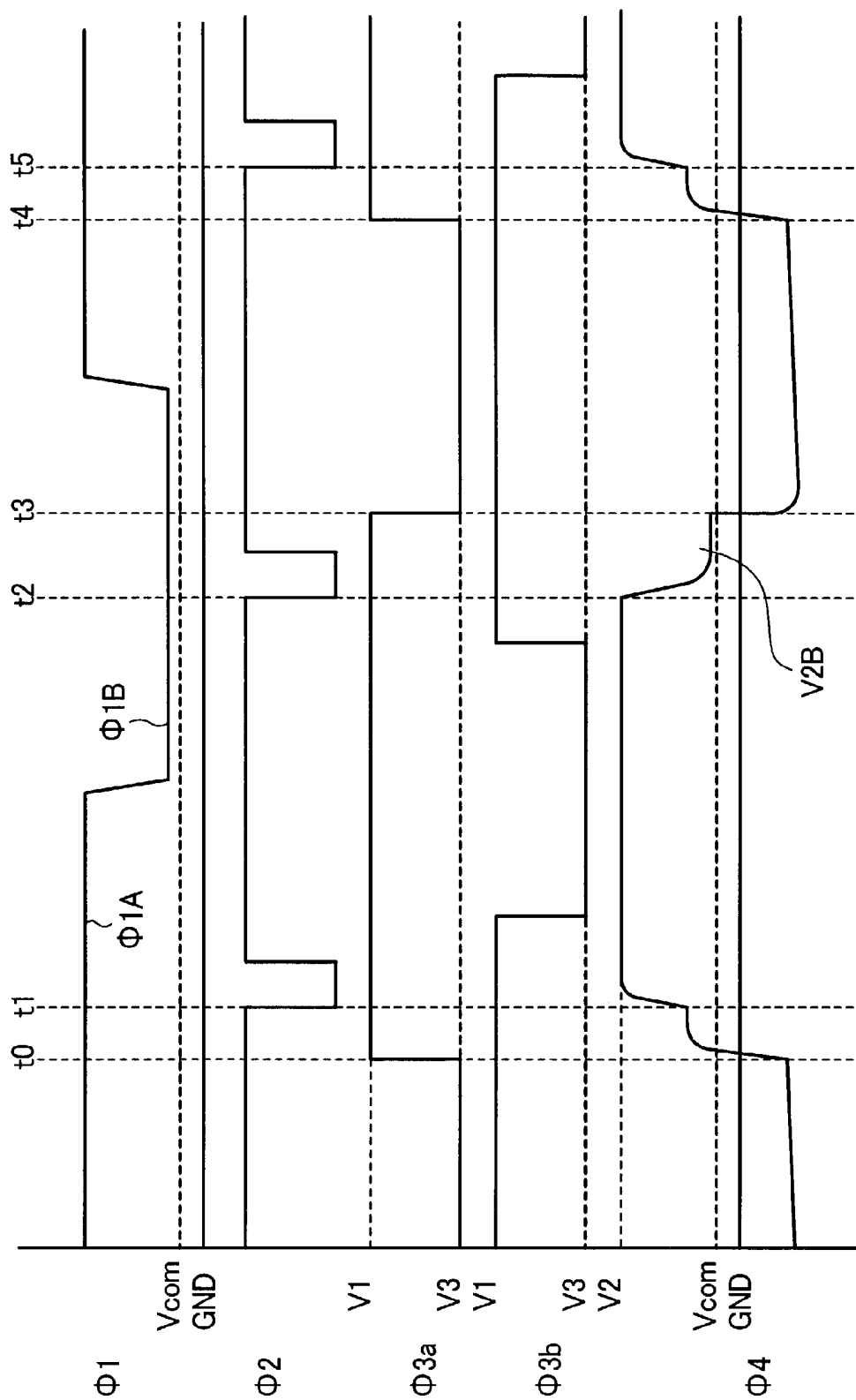


FIG. 19A

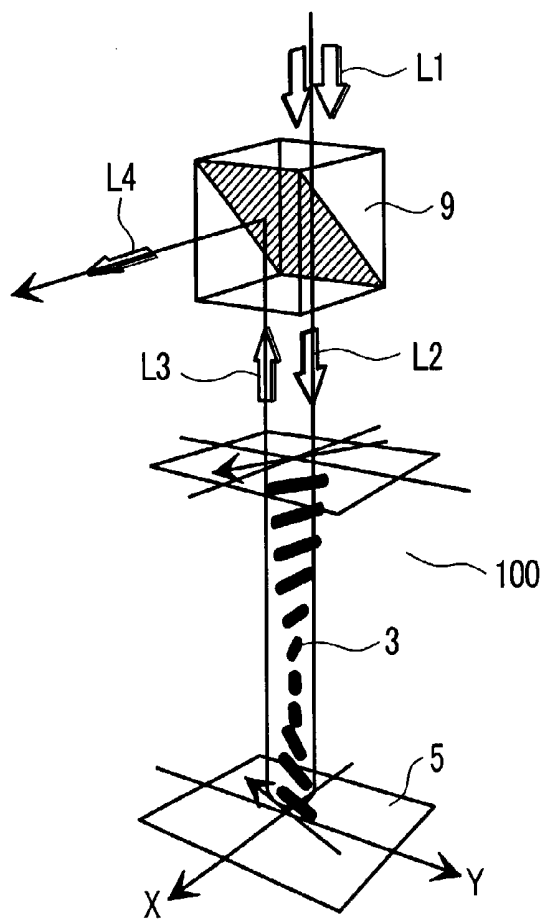


FIG. 19B

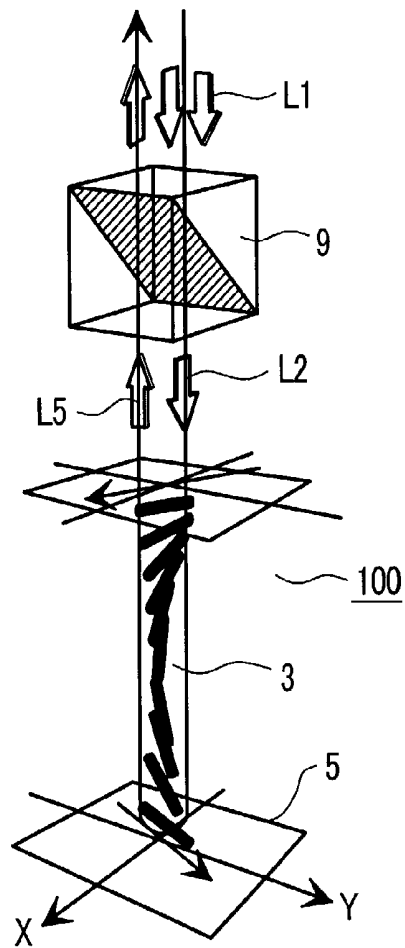


FIG. 20

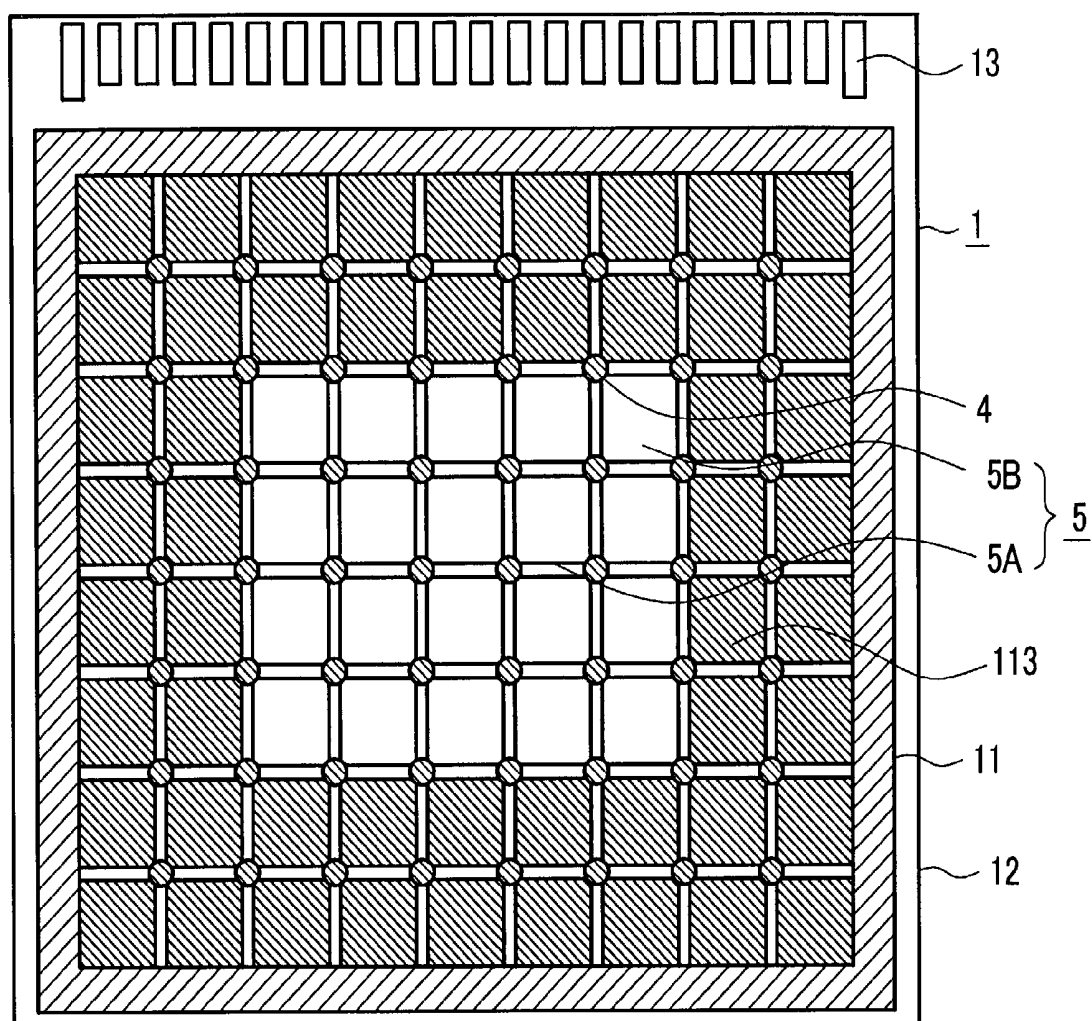


FIG. 21

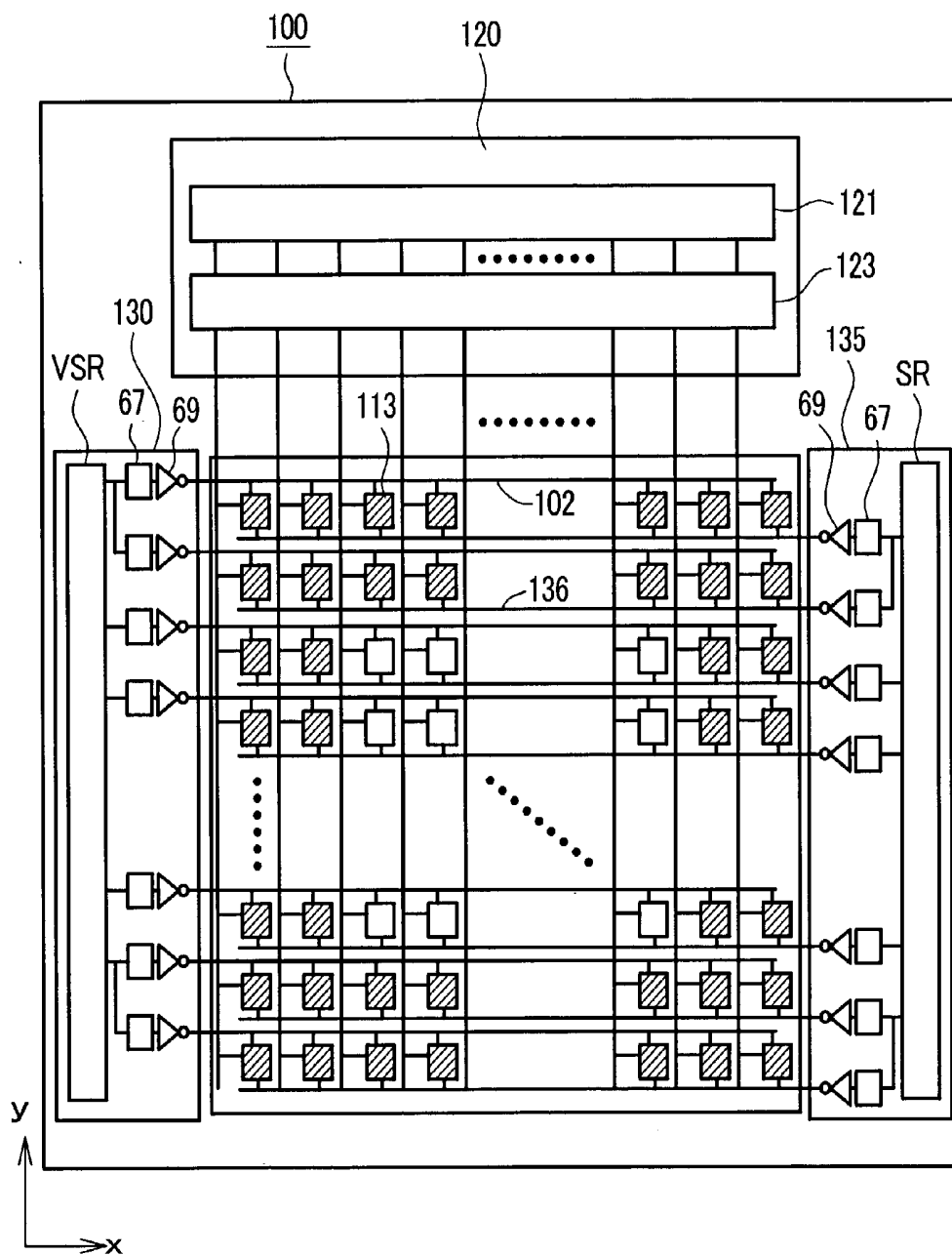


FIG. 22

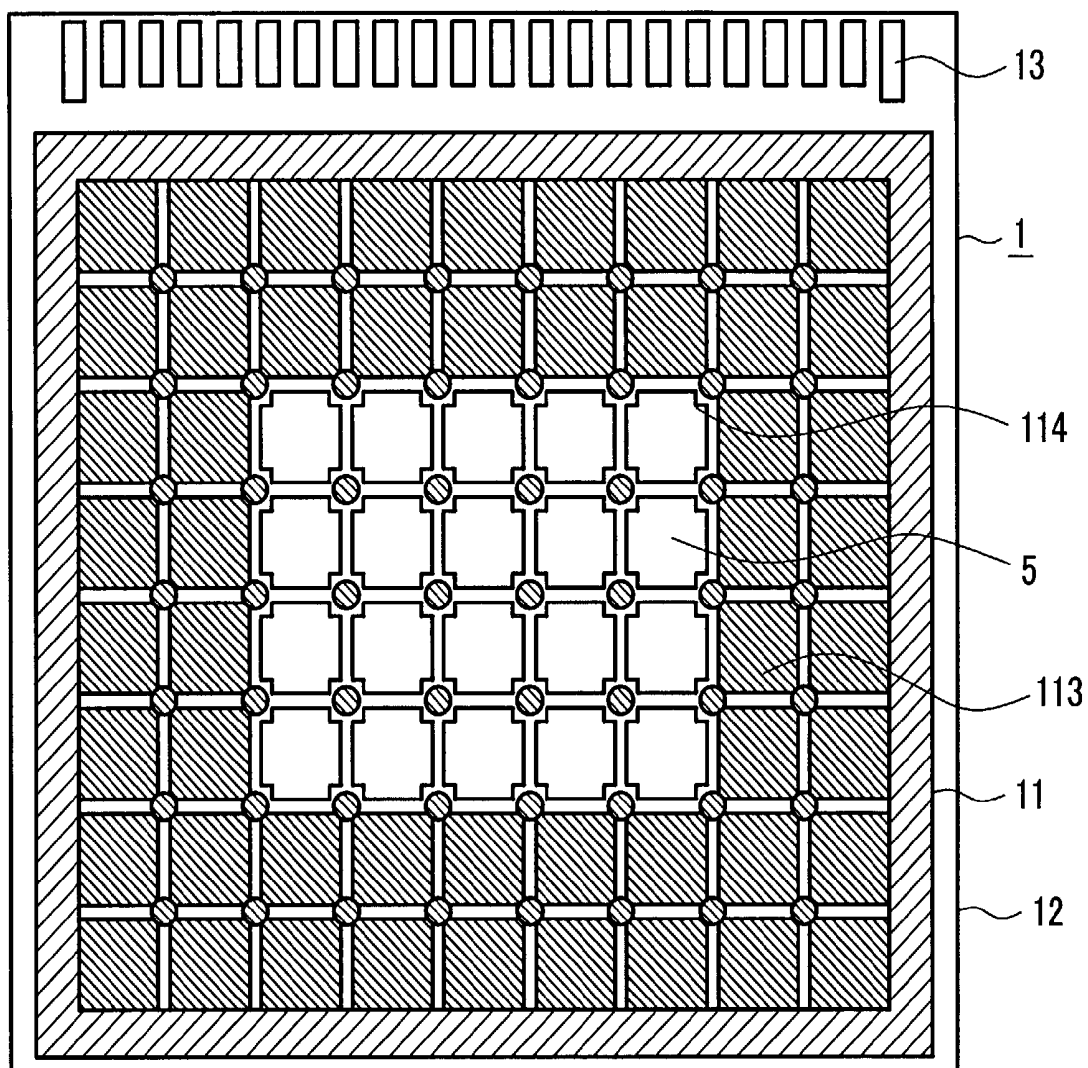


FIG. 23

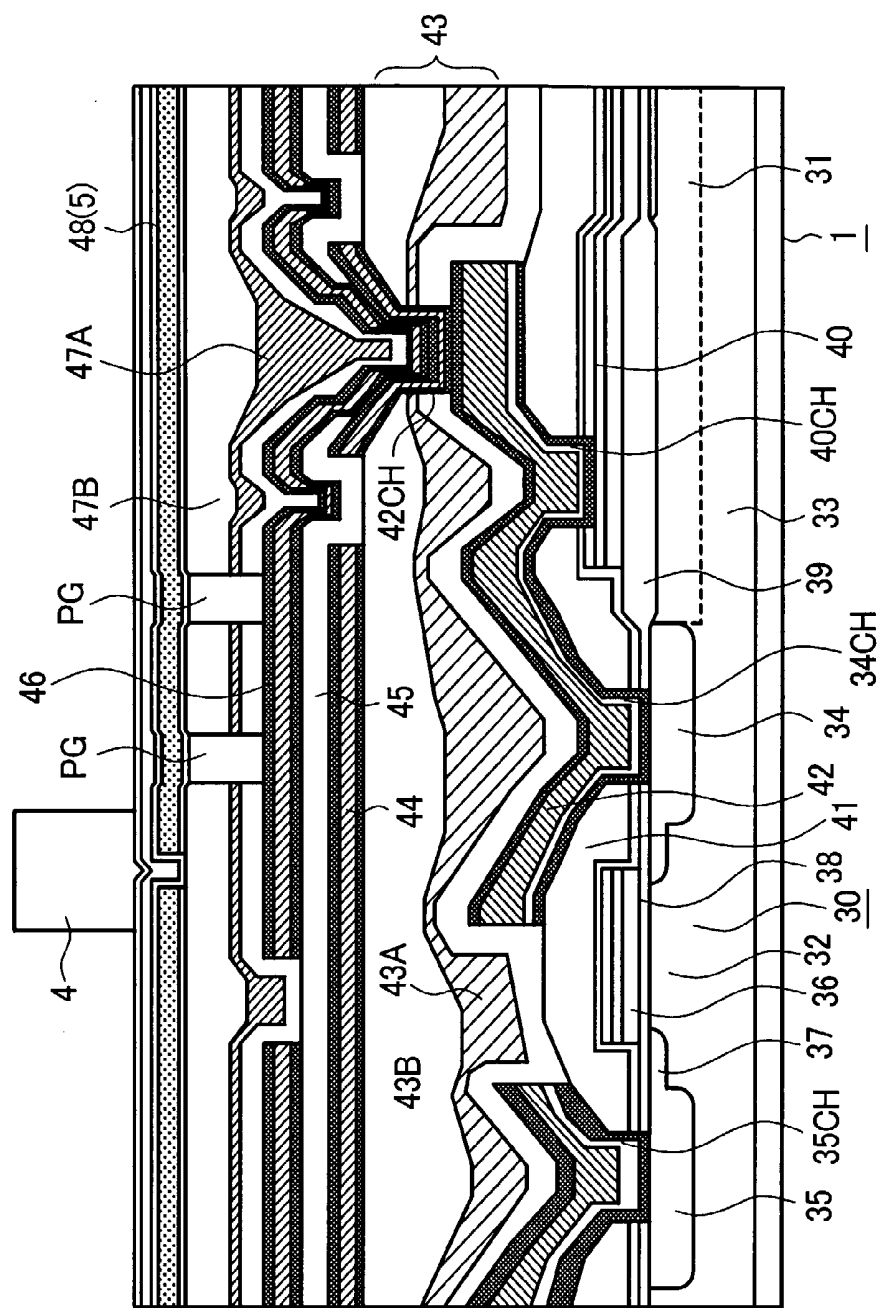


FIG. 24

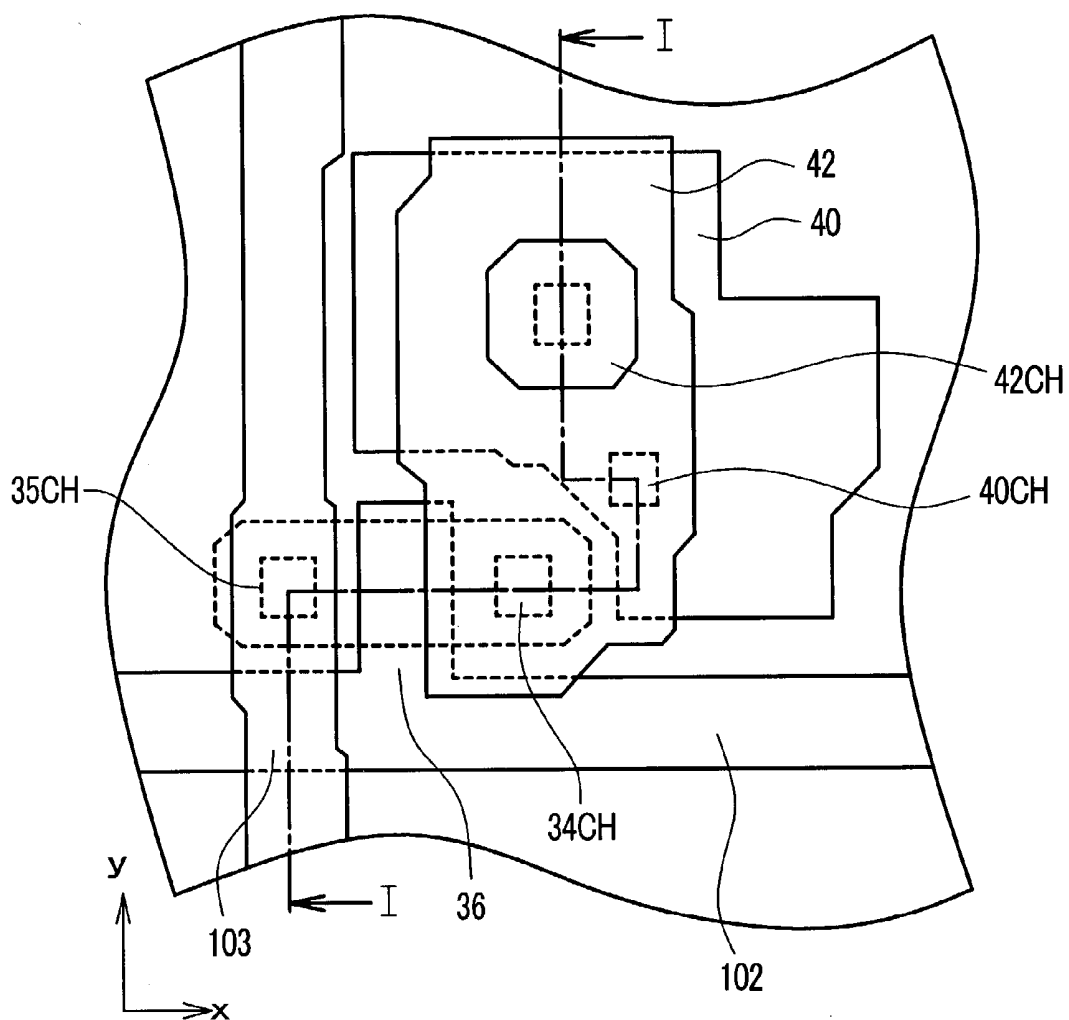


FIG. 25

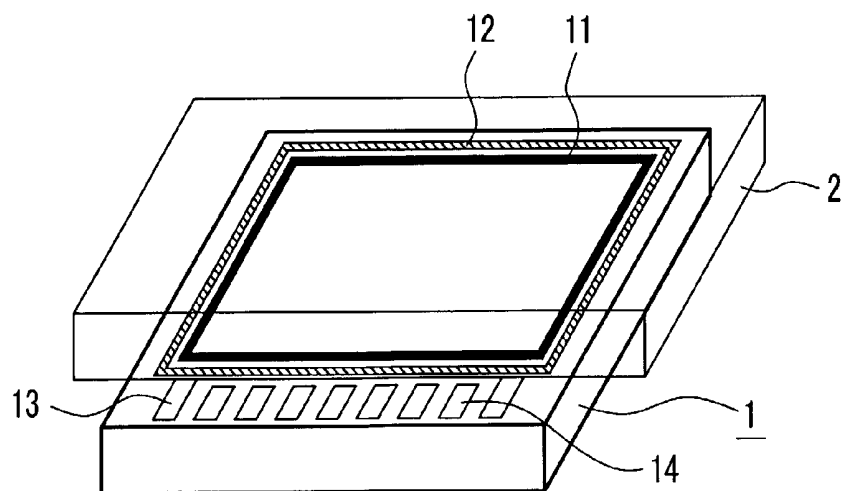


FIG. 26A

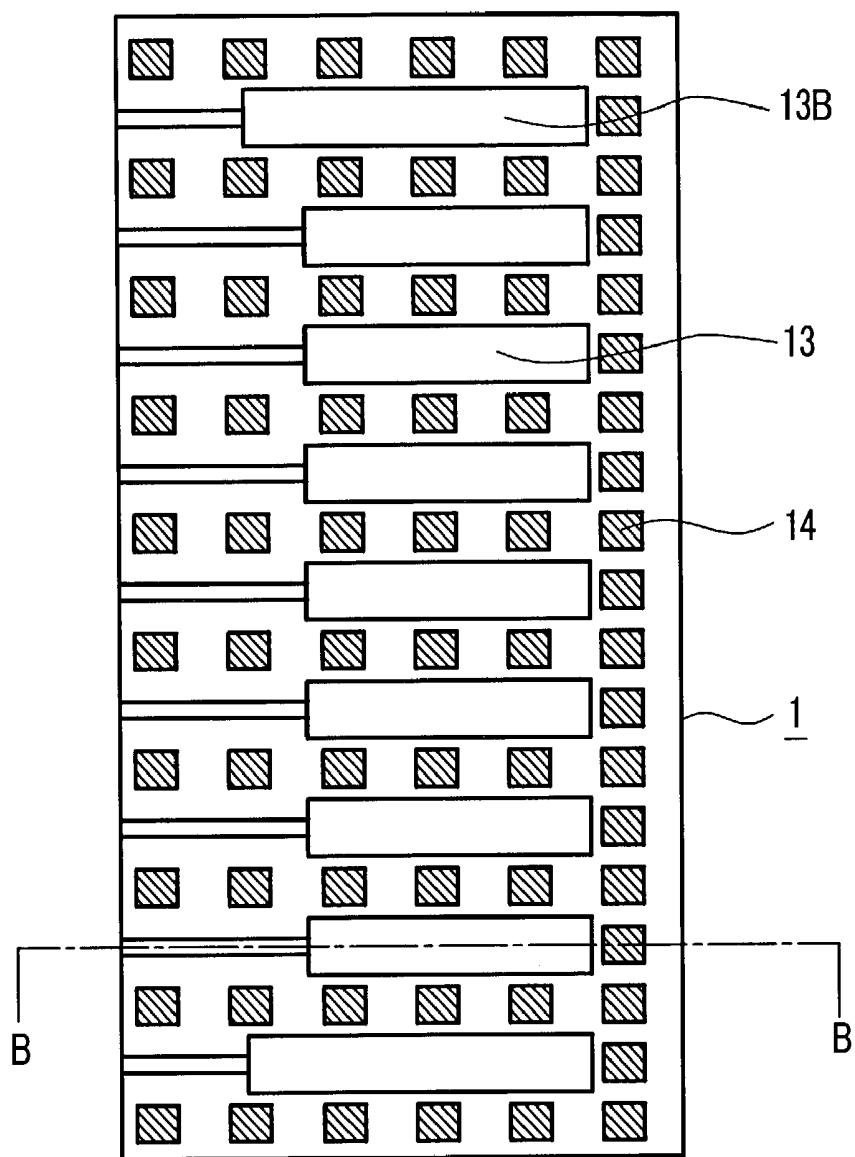


FIG. 26B

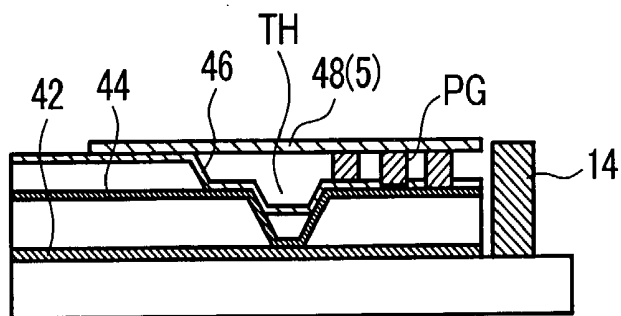


FIG. 27

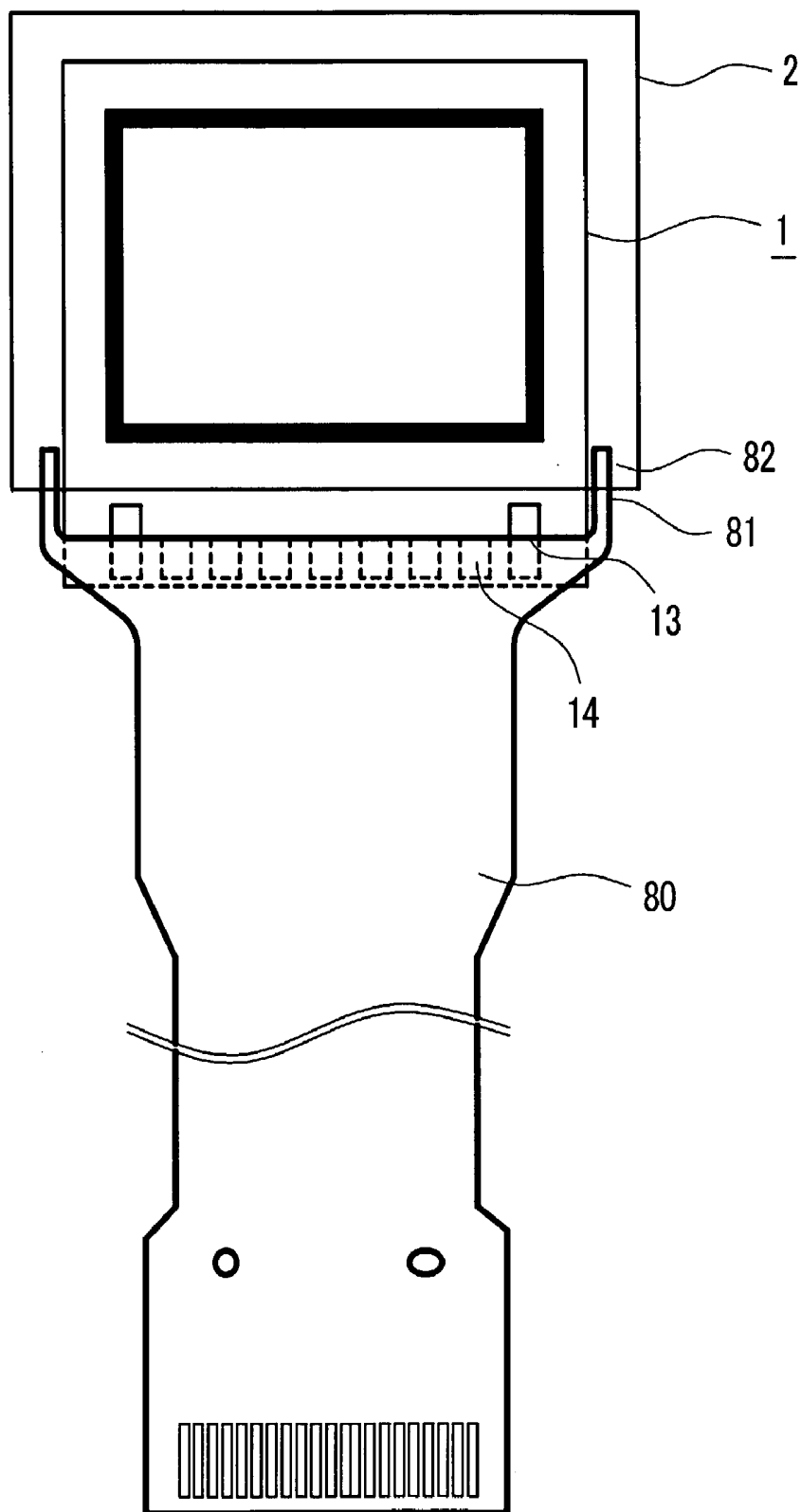


FIG. 28

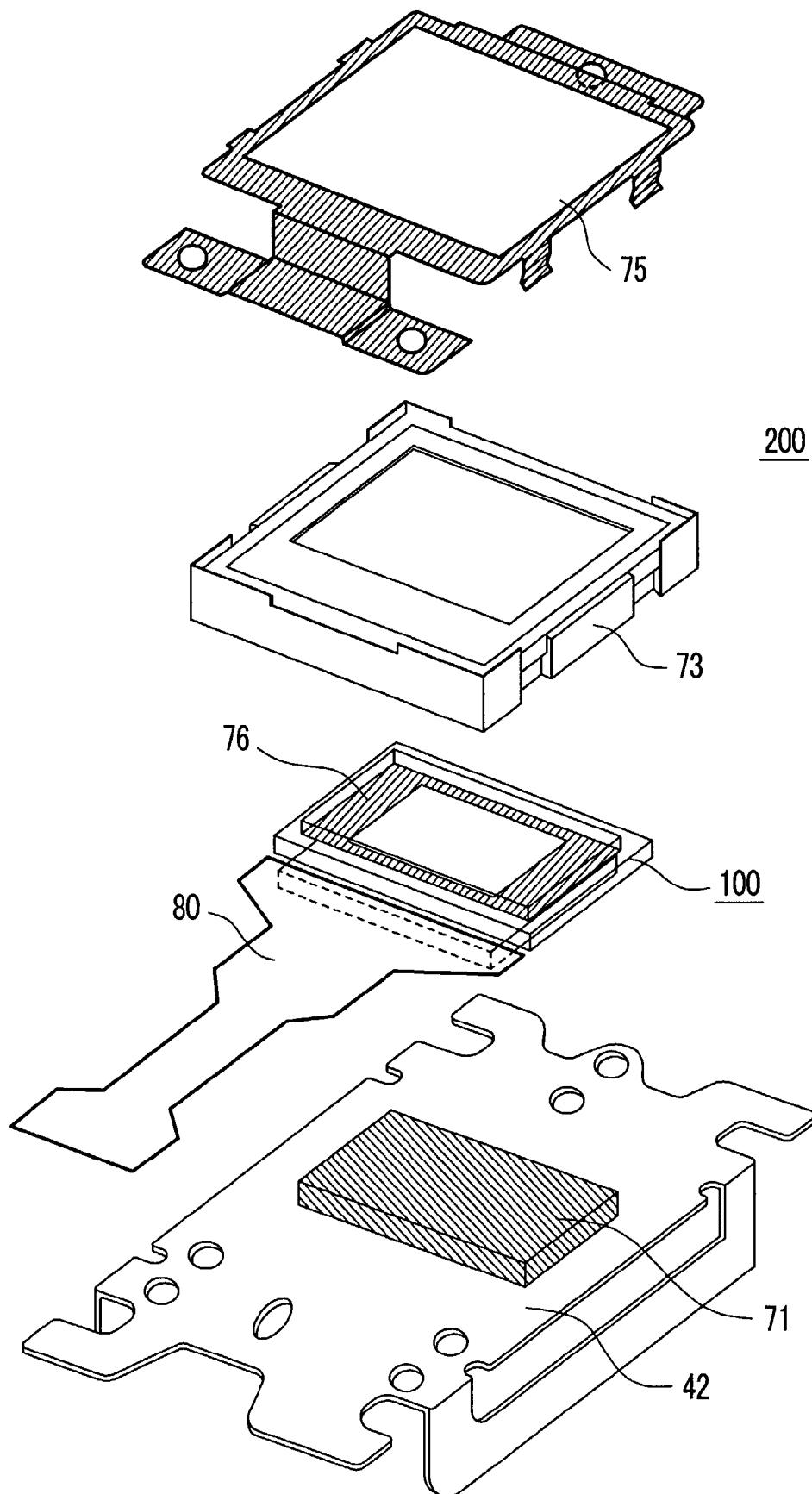
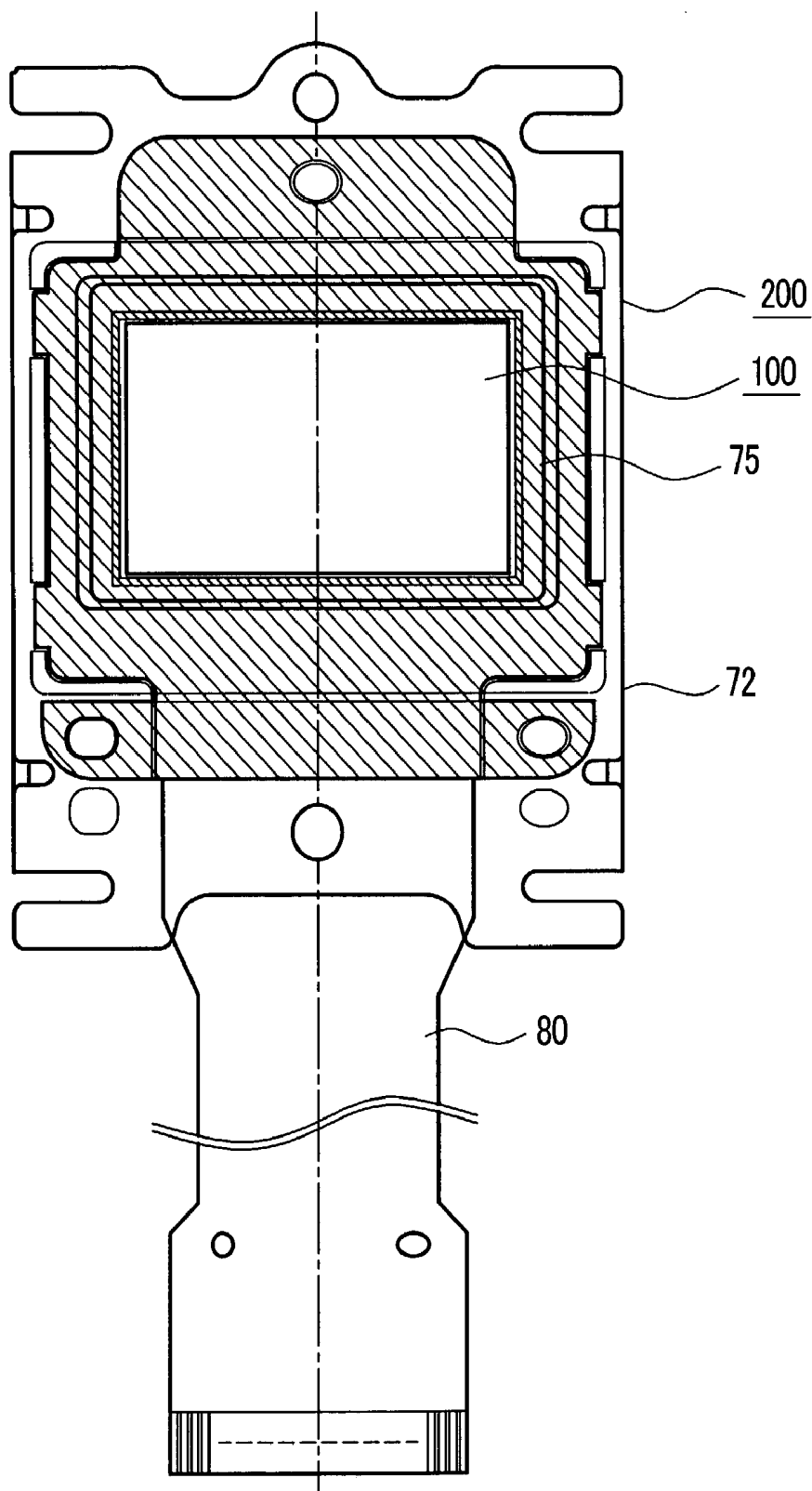


FIG. 29



LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display device, and more particularly to a technique which is effectively applicable to a drive-circuit integral type liquid crystal display device which mounts drive circuits and a display part on the same substrate.

[0003] 2. Description of the Related Art

[0004] Recently, a liquid crystal display device has been popularly used in various applications covering a miniaturized display device and a display terminal of a so-called OA equipment and the like. The liquid crystal display device is basically constituted such that between a pair of insulating substrates at least one of which is made of a transparent substrate (for example, a glass plate or a plastic substrate or the like), a layer made of liquid crystal composition (liquid crystal layer) is sandwiched thus forming a so-called liquid crystal panel (also referred to as a liquid crystal display element or a liquid crystal cell).

[0005] In this liquid crystal panel, a voltage is selectively applied to various electrodes for forming pixels so as to change the orientation direction of liquid crystal molecules constituting the liquid crystal composition of given pixel portions whereby images are displayed. There has been known a liquid crystal panel which forms a display part by arranging pixels in a matrix array. The liquid crystal panel in which the pixels are arranged in a matrix array is largely classified into two types consisting of a single matrix type and an active matrix type. The single matrix type forms a pixel at a crossing point of two stripe-shaped electrodes which are respectively formed on a pair of insulating substrates and cross each other. On the other hand, the active matrix type includes pixel electrodes and active elements (for example, thin film transistors) for selecting pixels, wherein by selecting the active element, the pixel is formed by the pixel electrode which is connected to the active element and a reference electrode which faces the pixel electrode in an opposed manner.

[0006] The active matrix type liquid crystal display device has been popularly used as a display device of a notebook type personal computer or the like. In general, the active matrix type liquid crystal display device adopts a so-called vertical field type in which an electric field for changing the orientation direction of a liquid crystal layer is applied between electrodes formed on one substrate and electrodes formed on another substrate. Further, a so-called lateral field type (also referred to as IPS (In-Plane Switching) type) liquid crystal display device which arranges the direction of an electric field applied to a liquid crystal layer substantially parallel to a surface of a substrate has been practically used.

[0007] On the other hand, as a display device which uses the liquid crystal display device, a liquid crystal projector is practically used. In this liquid crystal projector, an illumination light radiated from a light source is irradiated to a liquid crystal panel and an image of the liquid crystal panel is projected to a screen. The liquid crystal panel used for the liquid crystal projector is classified into a reflection type and a transmission type. When the liquid crystal panel adopts the reflection type, by forming a reflection surface using the

pixel electrodes and by providing constitutions such as wiring below the pixel electrodes, it is possible to use the substantially whole region of a display part as an effective reflection surface and hence, the reflection type is advantageous compared to the transmission type in view of miniaturization, enhancement of high definition and enhancement of brightness of the liquid crystal panel.

[0008] Further, as the active matrix type liquid crystal display device for a liquid crystal projector, in view of an advantage that the miniaturized high-definition liquid crystal display device can be realized, a so-called drive circuit integral type liquid crystal display device which also forms drive circuits for driving the pixel electrodes on a substrate on which the pixel electrodes are formed has been known.

[0009] Further, with respect to the drive circuit integral type liquid crystal display device, a reflection type liquid crystal display device (also referred to as Liquid Crystal On Silicon (LCOS)) which forms pixel electrodes and drive circuits on a semiconductor substrate in place of an insulation substrate has been known.

[0010] Further, in these liquid crystal display devices, alternating driving which periodically reverses the polarity of voltage applied to the liquid crystal layer is performed. The alternating driving is performed for the purpose of preventing the deterioration of the liquid crystal which is caused by the application of a direct current voltage to the liquid crystal. In the active matrix type liquid crystal display device which applies a voltage between the pixel electrodes and the reference electrodes, as one method for performing the alternating driving, there has been known a method in which a fixed voltage is applied to the reference electrodes and a signal voltage of positive polarity and negative polarity are alternately applied to the pixel electrodes. However, in the above-mentioned alternating driving method, a drive circuit must be a circuit having a high dielectric strength which can withstand the potential difference between the maximum voltage at the positive polarity side and the minimum voltage at the negative polarity side. Further, control signals (scanning signals) for controlling turning on and off of thin film transistors must withstand a high voltage.

SUMMARY OF THE INVENTION

[0011] Recently, with respect to the liquid crystal display device, there has been a demand for high resolution such as the specification of HDTV or the like, for example. However, when the number of pixels in the horizontal direction is increased along with high resolution, scanning signal lines (gate lines) are elongated and hence, the deterioration of image quality such as lateral smears arises due to the wiring resistance of the scanning signal lines or parasitic capacitance.

[0012] Further, in the liquid crystal display device, along with the progress of multi-gray scale to 64 gray scales or 256 gray scales, the high definition is also demanded. When the number of gray scales is increased, a size of the circuit becomes large, while when the number of pixels is increased, a drive circuit for supplying signals to respective pixels is driven at a high speed. Further, although an area that the pixels occupy is reduced, with respect to a circuit having high dielectric strength, it is difficult to form respective parts constituting the circuit finely and hence, the size of the circuit becomes large. Particularly, with respect to the

field of the liquid crystal panels where the miniaturization is advanced, even when the increase of the number of pixels is demanded, it is difficult to form the constitution for pixel electrodes such as active elements having high dielectric strength within a limited area of the pixel. Further, in the drive circuit integral type liquid crystal display device which incorporates drive circuits inside a liquid crystal display panel, there arises a problem that an occupying area of drive circuits is expanded and hence, the liquid crystal panel becomes large-sized. Further, in the circuit having high dielectric strength, the area occupied by the electrodes of the active elements or the like is expanded and hence, there arises a problem that capacitive components are increased whereby fast driving becomes difficult and power consumption is increased.

[0013] The present invention has been made to solve the above-mentioned drawbacks of the related art and it is an object of the present invention to provide an optimum scanning signal line drive circuit in a liquid crystal display device, and more particularly to provide a technique which enables alternating driving with a drive circuit having low dielectric strength and enables fast driving by reducing the pixel size and the circuit size of the drive circuits.

[0014] Further, it is an object of the present invention to provide a technique which can reduce the difference in scanning signals which is generated in scanning signal lines due to wiring resistance or the like, that is, so-called rounding of waveforms.

[0015] The above-mentioned objects and novel features of the present invention will become apparent from the description of this specification and attached drawings.

[0016] To briefly explain the summary of typical inventions out of inventions disclosed in this specification, they are as follows.

[0017] A pixel capacitance is connected to a pixel electrode of a liquid crystal display device and a pixel potential control signal is supplied to the pixel capacitance so that the voltage of pixel electrode is changed so as to realize alternating driving. Further, a circuit which pulls up scanning signal lines is provided between a pixel potential control circuit and a display region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 is a block diagram showing the schematic constitution of a liquid crystal display device of an embodiment of the present invention.

[0019] FIG. 2 is a block diagram showing one example of a liquid crystal panel of the embodiment of the present invention.

[0020] FIG. 3A is an explanatory view showing a switch 104 in an ON state and FIG. 3B is an explanatory view showing the switch 104 in an OFF state.

[0021] FIG. 4 is a timing chart showing a driving method of the liquid crystal panel shown in FIG. 2.

[0022] FIG. 5 is a schematic circuit diagram showing the constitution of a pixel potential control circuit of the liquid crystal display device of the embodiment of the present invention.

[0023] FIG. 6A, FIG. 6B, FIG. 6C and FIG. 6D are schematic circuit diagrams showing clocked inverters used in the pixel potential control circuit.

[0024] FIG. 7 is a schematic circuit diagram showing the constitution of a vertical drive circuit of the liquid crystal display device of the embodiment of the present invention.

[0025] FIG. 8 is a timing chart showing an operation of the vertical drive circuit shown in FIG. 7.

[0026] FIG. 9 is a schematic circuit diagram showing the constitution of a pull up circuit of the liquid crystal display device of the embodiment of the present invention.

[0027] FIG. 10 is a timing chart showing the operation of the pull up circuit shown in FIG. 9.

[0028] FIG. 11 is a schematic circuit diagram showing the constitution of a horizontal drive circuit of the liquid crystal display device of the embodiment of the present invention.

[0029] FIG. 12 is a timing chart showing an operation of the horizontal drive circuit shown in FIG. 11.

[0030] FIG. 13 is schematic cross sectional view showing a pixel portion of the liquid crystal display device of the embodiment of the present invention.

[0031] FIG. 14 is a schematic plan view showing the constitution for forming a pixel potential control line using a light shielding film.

[0032] FIG. 15A and FIG. 15B are timing charts showing a driving method of the liquid crystal display device of the embodiment of the present invention.

[0033] FIG. 16A is a schematic cross-sectional view of an inverter circuit used in the pixel potential control circuit of the liquid crystal display device of the embodiment of the present invention and FIG. 16B is a timing chart showing an operation of the inverter circuit.

[0034] FIG. 17 is a schematic plan view showing the liquid crystal display device of the embodiment of the present invention.

[0035] FIG. 18 is a timing chart showing a driving method of the liquid crystal display device of the embodiment of the present invention.

[0036] FIG. 19A is a schematic explanatory view showing an advancing of light when a voltage is not applied to liquid crystal and FIG. 19B is a schematic explanatory view showing an advancing of light when a voltage is applied to liquid crystal.

[0037] FIG. 20 is a schematic plan view showing the liquid crystal panel of the liquid crystal display device of the embodiment of the present invention.

[0038] FIG. 21 is a schematic circuit diagram showing the liquid crystal display device of the embodiment of the present invention.

[0039] FIG. 22 is a schematic plan view showing the liquid crystal display device of the embodiment of the present invention.

[0040] FIG. 23 is a schematic cross-sectional view of a periphery of an active element of the liquid crystal display device of the present invention.

[0041] FIG. 24 is a schematic plan view of a periphery of an active element of the liquid crystal display device of the present invention.

[0042] FIG. 25 is a schematic view showing the liquid crystal panel of the liquid crystal display device of the embodiment of the present invention.

[0043] FIG. 26A is a plan view showing an external connection terminal in an enlarged form and FIG. 26B is a cross-sectional view taken along a line B-B in FIG. 26A.

[0044] FIG. 27 is a schematic view showing a state in which a flexible printed circuit board is connected to the liquid crystal panel of a liquid crystal display device of the embodiment of the present invention.

[0045] FIG. 28 is schematic assembled view showing the liquid crystal display device of the embodiment of the present invention.

[0046] FIG. 29 is a schematic view showing the liquid crystal display device of the embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0047] Preferred embodiments of a liquid crystal display device according to the present invention are explained in detail hereinafter in conjunction with drawings. In all drawings which are served for explaining the embodiments of the present invention, parts having the same functions are indicated by same symbols and their repeated explanation is omitted.

[0048] FIG. 1 is a block diagram showing the schematic constitution of the liquid crystal display device of the embodiment of the present invention.

[0049] The liquid crystal display device of this embodiment is constituted of a liquid crystal panel (liquid crystal display element) 100 and a display control device 111. The liquid crystal panel 100 includes a display part 110 (also referred to as a display region) on which a pixel portions 101 are formed in a matrix array, a horizontal drive circuit (a video signal line drive circuit) 120, a vertical drive circuit (a scanning signal line drive circuit) 130, a pixel potential control circuit 135 and an auxiliary circuit 145. Further, the display part 110, the horizontal drive circuit 120, the vertical drive circuit 130, the pixel potential control circuit 135 and the auxiliary circuit 145 are formed on the same substrate.

[0050] In each pixel portion 101, a pixel electrode, a counter electrode and a liquid crystal layer which is sandwiched between the pixel electrode and the counter electrode are formed (not shown in the drawing). By applying a voltage between the pixel electrode and the counter electrode, the orientation direction or the like of the liquid crystal molecules is changed. A display is performed by making use of the change of the property of the liquid crystal layer with respect to light which is caused by the change of the orientation direction of liquid crystal molecules.

[0051] A display control device 111 controls the horizontal drive circuit 120, the vertical drive circuit 130 and the pixel potential control circuit 135 in response to control signals such as clock signals, display timing signals, horizontal synchronizing signals or vertical synchronizing signals

which are transmitted from the outside. Further, the display control device 111 supplies display signals to be displayed on the liquid crystal panel to the horizontal drive circuit 120. Numeral 131 indicates a control signal line for outputting control signals from the display control device 111 and numeral 132 indicates a display signal line.

[0052] A plurality of video signal lines (also referred to as drain signal lines or vertical signal lines) 103 extend in the vertical direction (the y direction in the drawing) from the horizontal drive circuit 120. Further, the plurality of video signal lines 103 are arranged in parallel in the horizontal direction (the X direction). A plurality of scanning signal lines (also referred to as gate signal lines or horizontal signal lines) 102 extend in the horizontal direction (the x direction) from the vertical drive circuit 130. Further, the plurality of scanning signal lines 102 are arranged in parallel in the vertical direction (the Y direction). A plurality of pixel potential control lines 136 extend in the horizontal direction (the X direction) from the pixel potential control circuit 135. Further, the plurality of pixel potential control lines 136 are arranged in parallel in the vertical direction (the Y direction).

[0053] On a side portion of the display part 110 opposite to the vertical drive circuit 130, an auxiliary circuit 145 is mounted. The scanning signal lines 102 pulled out from the vertical drive circuit 130 are also connected to the auxiliary circuit 145.

[0054] The horizontal drive circuit 120 is constituted of a horizontal shift register 121 and a voltage selection circuit 123. The control signal line 131 and the display signal line 132 pulled out from the display control device 111 are connected to the horizontal shift register 121 and the voltage selection circuit 123, wherein the control signals and the display signals are transmitted to the horizontal shift register 121 and the voltage selection circuit 123. Here, as the display signals, both of analogue signals and digital signals are available. Further, although power source/voltage lines of respective circuits are omitted from the drawings, it is assumed that the necessary voltage is applied.

[0055] When the vertical synchronizing signal is inputted from the outside and, thereafter, the first display timing signal is inputted, the display control device 111 outputs a start pulse to the vertical drive circuit 130 through a control signal line 131. Then, in response to the horizontal synchronizing signal, the display control device 111 outputs shift clocks to the vertical drive circuit 130 such that the scanning signal lines 102 are sequentially selected every one horizontal scanning time (hereinafter referred to as 1 h). In accordance with the shift clocks, the vertical drive circuit 130 selects the scanning signal lines 102 and outputs the scanning signals to the scanning signal lines 102. That is, the vertical drive circuit 130 outputs the signals for selecting the scanning signal lines 102 for one horizontal scanning time 1 h sequentially from the top in FIG. 1.

[0056] Further, when a display timing signal is inputted to the display control device 111, the display control device 111 judges this inputting as starting of display and outputs the display signals to the horizontal drive circuit 120. Although the display signals are sequentially outputted from the display control device 111, the horizontal shift register 121 outputs the timing signals in response to the shift clocks transmitted from the display control device 111. The timing signals indicate timings for fetching the display signals

which the voltage selection circuit **123** has to output to the respective video signal lines **102**.

[0057] When the display signals are analogue signals, the voltage selection circuit **123** fetches fixed voltages out of the analogue signals as the display signals (gray scale voltages) in accordance with the timing signals and outputs the fetched gray scale voltages to the video signal lines **103** as the video signals. When the display signals are digital signals, the voltage selection circuit **123** fetches the display signals in accordance with the timing signal and selects (decodes) the gray scale voltages based on the display signals (the digital data) and outputs the gray scale voltages to the video signal lines **103**. The gray scale voltages outputted to the video signal lines **103** are written in the pixel electrodes of the pixel portions **101** in accordance with the timing that the scanning signals are outputted from the vertical drive circuit **130** as the video signals.

[0058] In response to the control signals from the display control device **111**, the pixel potential control circuit **135** controls the voltage of video signals written in the pixel electrodes. The gray scale voltages written in the pixel electrodes from the video signal lines **103** have a certain potential difference with respect to the reference voltage of the counter electrodes. The pixel potential control circuit **135** supplies the control signals to the pixel portions **101** so as to change the potential difference between the pixel electrodes and the counter electrodes. The pixel potential control circuit **135** will be explained in detail later.

[0059] The auxiliary circuit **145** has output terminals thereof connected to the scanning signal lines **102** and is operated to make the scanning signal lines **102** assume the specific voltage. As described previously, although the scanning signals are outputted to the scanning signal lines **102** from the vertical drive circuit **130**, the auxiliary circuit **145** is a circuit which functions such that the auxiliary circuit **145** assists the outputting of signals from the vertical drive circuit **130** and dissipates the difference in scanning signals (rounding of waveforms) which occurs on the scanning signal lines **102** due to the wiring resistance. In case that auxiliary circuit **145** assists the vertical drive circuit **130** when the output from the vertical drive circuit **130** is of a high voltage, the auxiliary circuit **145** constitutes a pull up circuit, while in case that auxiliary circuit **145** assists the vertical drive circuit **130** when the output from the vertical drive circuit **130** is of a low voltage, the auxiliary circuit **145** constitutes a pull down circuit. The auxiliary circuit **145** will be explained in detail later.

[0060] Subsequently, the pixel portion **101** of the liquid crystal panel **100** which constitutes one embodiment of the present invention is explained in conjunction with FIG. 2. FIG. 2 is a circuit diagram showing an equivalent circuit of the pixel portion **101**. Each pixel portion **101** is provided to a region where two neighboring scanning signal lines **102** and two neighboring video signal lines **103** cross each other (a region surrounded by four signal lines) in the display part **110** and these pixel portions **101** are arranged in a matrix array in the display part **110**. However, to simplify the drawing, only one pixel portion **101** is shown in FIG. 2. Each pixel portion **101** includes an active element (also referred to as a switching element of the pixel portion) **30** and a pixel electrode **109**. Further, a pixel capacitance **115** is connected to the pixel electrode **109**. The pixel capacitance

115 has one electrode thereof connected to the pixel electrode **109** and another electrode connected to a pixel potential control line **136**. On the other hand, the pixel potential control line **136** is connected to the pixel potential control circuit **135**. In FIG. 2, the active element **30** is constituted of a p-type transistor. Further, the active element **30** may be formed of an n-type transistor.

[0061] As mentioned previously, the scanning signals are outputted to the scanning signal lines **102** from the vertical drive circuit **130**. Turning on and off of the active element **30** is controlled in response to the scanning signals. The gray scale voltage is supplied to the video signal lines **103** as video signals. When the active element **30** is turned on, the gray scale voltage is supplied to the pixel electrode **109** from the video signal line **103**. The counter electrode (common electrode) **107** is arranged to face the pixel electrode **109** in an opposed manner and a liquid crystal layer (not shown in the drawing) is formed between the pixel electrode **109** and the counter electrode **107**. Here, with respect to the circuit diagram shown in FIG. 2, the liquid crystal capacitance **108** is equivalently connected between the pixel electrode **109** and the counter electrode **107**. By applying a voltage between the pixel electrode **109** and the counter electrode **107**, the orientation direction or the like of the liquid crystal molecules is changed and, correspondingly, the property of the liquid crystal layer with respect to light is changed whereby the transmissivity (reflectivity) of light of each pixel can be changed. To give the gray scales to the images, the voltages (gray scale voltages) are applied to the pixel electrodes corresponding to the transmissivity of light.

[0062] As a driving method of the liquid crystal display device, as mentioned previously, the alternating driving is performed to prevent the DC current from being applied to the liquid crystal layer. To perform the alternating driving, assume the potential of the counter electrode **107** as the reference potential, the voltage which takes the positive polarity and the negative polarity with respect to the reference potential is outputted as gray scale voltages from the voltage selection circuit **123**. However, when the voltage selection circuit **123** adopts a circuit of high dielectric strength which can withstand the potential difference between the positive polarity and the negative polarity, there arises a problem that the size of the circuit including the active elements **30** is increased or a problem that the operational speed becomes slow.

[0063] Here, the inventors have studied a case in which the alternating driving is performed while using signals of the same polarity with respect to the reference potential as the video signals (gray scale voltages) which are supplied to the pixel electrode **109** from the voltage selection circuit **123**. For example, as the gray scale voltage which is outputted from the voltage selection circuit **123**, the voltage having positive polarity with respect to the reference potential is used. After writing the voltages having the positive polarity with respect to the reference potential, by lowering the voltage of the pixel potential control signal which is applied to the electrode of the pixel capacitance **115** from the pixel potential control circuit **135**, the voltage of the pixel electrode **109** can be lowered whereby it is possible to generate the voltage having negative polarity with respect to the reference potential. With the use of this driving method, the difference between the maximum value and the minimum value which the voltage selection circuit **123** outputs can be

made small and hence, it is possible to adopt a circuit having low dielectric strength as the voltage selection circuit 123. Although a case in which the voltage of positive polarity is written in the pixel electrode 109 and the voltage of negative polarity is generated by the pixel potential control circuit 135 has been explained as an example, in case that the voltage of positive polarity is generated by writing the voltage of negative polarity, the alternating driving can be performed by elevating the voltage of the pixel potential control signal.

[0064] Then, the method for changing the voltage of the above-mentioned pixel electrode 109 is explained in conjunction with FIG. 3A, FIG. 3B. FIG. 3A shows an ON state of the switch 104 and FIG. 3B shows an OFF state of the switch 104. For the explanation purpose, the liquid crystal capacitance 108 is expressed as the first capacitance 53, the pixel capacitance 115 is expressed as a second capacitance 54, and the active element 30 is expressed as the switch 104. An electrode connected to the pixel electrode 109 of the pixel capacitance 115 is formed as an electrode 56 and an electrode connected to the pixel potential control circuit 136 of the pixel capacitance 115 is formed as an electrode 57. Further, a point at which the pixel electrode 109 and the electrode 56 connect each other is indicated as a node 58. Here, for the explanation purpose, other parasitic capacitances can be ignored, wherein the capacitance of the first capacitor 53 is expressed as CL and the capacitance of the second capacitor 54 is expressed as CC.

[0065] First of, as shown in FIG. 3A, the voltage V1 is applied to the electrode 57 of the second capacitor 54 from the outside. Subsequently, when the switch 104 is turned on in response to the scanning signals, the voltages are supplied to the pixel electrodes 109 and the electrode 56 from the video signal line 103. Here, the voltage applied to the node 58 is set to V2.

[0066] Subsequently, as shown in FIG. 3B, at a point of time that the switch 104 is turned off, the voltage (pixel potential control signal) which is supplied to the electrode 57 is dropped from V1 to V3. Here, a total quantity of charge charged to the first capacitor 53 and the second capacitor 54 is not changed and hence, the voltage of the node 58 is changed and the voltage of node 58 assumes a value expressed by $V2 - \{CC/(CL+CC)\} \times (V1 - V3)$.

[0067] Here, when the capacitance CL of the first capacitor 53 is sufficiently smaller than the capacitance CC of the second capacitor 54 ($CL \ll CC$), the relationship $CC/(CL+CC) \approx 1$ is established and the voltage of the node 58 assumes $V2 - V1 + V3$. Here, assume $V2=0$ and $V3=0$, it is possible to set the voltage of the node 58 to $-V1$.

[0068] According to the above-mentioned method, by allowing the voltage supplied to the pixel electrode 109 from the video signal line 103 to assume the positive polarity with respect to the reference potential of the counter electrode 107, the signal of negative polarity can be produced by controlling the voltage (pixel potential control signal) applied to the electrode 57. By producing the signal of negative polarity using such a method, it is unnecessary to supply the signal of negative polarity from the voltage selection circuit 123 whereby it is possible to form the peripheral circuits using parts having low dielectric strength.

[0069] Subsequently, the operational timing of the circuit shown in FIG. 2 is explained in conjunction with FIG. 4. In

the drawing, $\Phi 1$ indicates the gray scale voltage supplied to the video signal line 103. $\Phi 2$ indicates the scanning signal supplied to the scanning signal line 102. $\Phi 3$ indicates the pixel potential control signal (voltage step-down signal) supplied to the pixel potential control signal line 136. $\Phi 4$ indicates the potential of the pixel electrode 109. Here, the pixel potential control signal $\Phi 3$ is a signal which oscillates between the voltage V3 and the voltage V1 shown in FIG. 3.

[0070] To explain the operational timing of the circuit in conjunction with FIG. 4, $\Phi 1$ is indicated as an input signal $\Phi 1A$ for positive polarity and an input signal $\Phi 1B$ for negative polarity. Here, "for negative polarity" means that the voltage applied to the pixel electrode is changed in response to the pixel potential control signal and assumes the negative polarity with respect to the reference potential Vcom. In this embodiment, the explanation is made with respect to a case in which as the input signal $\Phi 1A$ for positive polarity and the input signal $\Phi 1B$ for negative polarity which constitute the video signal $\Phi 1$, the voltages which assume the potential of positive polarity with respect to the reference potential Vcom which is applied to the counter electrode 107 are supplied.

[0071] FIG. 4 shows a case in which during a period from a point of time t0 to a point of time t2, the gray scale voltage $\Phi 1$ assumes the input signal $\Phi 1A$ for positive polarity. First of all, at the point of time t0, the voltage V1 is outputted as the pixel control signal $\Phi 3$. Then, when the scanning signal $\Phi 2$ is selected at a point of time t1, and the scanning signal $\Phi 2$ assumes a low level, the p-type transistor 30 shown in FIG. 2 assumes the ON state and hence, the input signal $\Phi 1A$ for positive polarity which is supplied to the video signal line 103 is written in the pixel electrode 109. The signal written in the pixel electrode 109 is indicated by $\Phi 4$ in FIG. 4. Further, in FIG. 4, the voltage written in the pixel electrode 109 at the point of time t1 is indicated by V2A. Subsequently, when the scanning signal $\Phi 2$ assumes the non-selected state and assumes a high level, the transistor 30 assumes the OFF state and the pixel electrode 109 assumes a state in which the pixel electrode 109 is separated from the video signal line 103 through which the voltage is supplied. The liquid crystal display device displays the gray scales in accordance with the voltage V2A written in the pixel electrode 109.

[0072] Then, a case in which the gray scale voltage $\Phi 1$ assumes the input signal $\Phi 1B$ for negative polarity during a period from a point of time t2 to a point of time t4 is explained. When the gray scale voltage $\Phi 1$ assumes the input signal $\Phi 1B$ for negative polarity, the scanning signal $\Phi 2$ is selected at the point of time t2 and the voltage V2B which is indicated by $\Phi 4$ is written in the pixel electrode 109. Thereafter, the transistor 30 is made to assume the OFF state and hence, at a point of time t3 after a lapse of 2 h (2 horizontal scanning time) from the point of time t2, the voltage supplied to the pixel capacitance 115 is stepped down from V1 to V3 as indicated by the pixel potential control signal $\Phi 3$. When the pixel potential control signal $\Phi 3$ is changed from v1 to V3, the pixel capacitance 115 performs a role of coupling capacitance and hence, the potential of the pixel electrode can be lowered in accordance with the amplitude of the pixel potential control signal $\Phi 3$.

Accordingly, it is possible to produce the voltage V2C having negative polarity with respect to the reference potential Vcom within the pixel.

[0073] By producing the signal of negative polarity in the above-mentioned method, it is possible to form the peripheral circuits using elements having low dielectric strength. That is, the signals outputted from the voltage selection circuit 123 are signals having a narrow positive-polarity-side amplitude and hence, it is possible to form the voltage selection circuit 123 using a circuit having low dielectric strength. Further, when the voltage selection circuit 123 can be driven at the low voltage, since the horizontal shift register 120, the display control device 111 and the like which constitute other peripheral circuit are circuits having low dielectric strength, it is possible to provide the constitution formed of circuits having low dielectric strength as the whole liquid crystal display device.

[0074] Next, the circuit constitution of the pixel potential control circuit 135 is explained in conjunction with FIG. 5. Symbol SR indicates a double-way shift register which is capable of shifting the signals in two ways consisting of upper and lower directions. The double-way shift register SR is constituted of clocked inverters 61, 62, 65, 66. Numeral 67 indicates a level shifter and numeral 69 indicates an output circuit. The double-way shift register SR and the like are operated using a power source voltage VDD. The level shifter 67 converts the voltage level of the signal outputted from the double-way shift register SR. From the level shifter 67, the signal having an amplitude between the power source voltage VBB having a higher potential than the power source voltage VDD and the power source voltage VSS (GND potential) is outputted. The power source voltages VPP and VSS are supplied to the output circuit 69 and the voltage VPP and VSS are outputted to the pixel potential control line 136 in accordance with the signal from the level shifter 67. The voltage V1 of the pixel potential control signal $\Phi 3$ explained in conjunction FIG. 4 assumes the power source voltage VPP and the voltage V3 assumes the power source voltage VSS. Here, in FIG. 5, the output circuit 69 is expressed by an inverter consisting of a p-type transistor and an n-type transistor. By selecting values of the power source voltage VPP supplied to the p-type transistor and the power source voltage VSS supplied to the n-type transistor, it is possible to output the voltages VPP, VSS as the pixel potential control signals $\Phi 3$.

[0075] However, a substrate voltage is supplied to a silicon substrate on which the p-type transistors are formed as explained later and hence, the value of the power source voltage VPP is set to a proper value with respect to the substrate voltage.

[0076] Numeral 26 indicates a start signal input terminal through which a start signal which constitutes one of control signals is supplied to the pixel potential control circuit 135. When the start signal is inputted, the double-way shift registers SR1 to SRn shown in FIG. 5 sequentially output timing signals in accordance with the timing of clock signals supplied from the outside. In accordance with the timing signal, the level shifter 67 outputs the voltage VSS and voltage VBB. In accordance with outputting of the level shifter 67, the output circuit 69 outputs the voltage VPP and the voltage VSS to the pixel potential control signal line 136. By supplying the start signal and the clock signal to the

double-way shift register SR such that the timing indicated by the pixel potential control signal $\Phi 3$ in FIG. 4, it is possible to output the pixel potential control signal $\Phi 3$ at the desired timing from the pixel potential control circuit 315. In the drawing, numeral 25 indicates a reset signal input terminal.

[0077] Here, the positional relationship between the pixel potential control circuit 135 and the vertical drive circuit 130 is studied. As mentioned previously in the explanation of FIG. 4, the pixel potential control signal is driven in an interlocking manner with the scanning signal. Accordingly, the pixel potential control line 136 and the scanning signal line 102 are arranged. In parallel in such a constitution, it is preferable to set the position where the pixel potential control circuit 135 is formed in the vicinity of end portions of the scanning signal lines 102. However, the vertical drive circuit 130 is provided at one ends of the scanning signal lines 102 and hence, the pixel potential control circuit 135 is provided in the vicinity of end portions of the scanning signal lines 102 opposite to the vertical drive circuit 130.

[0078] Conventionally, the vertical drive circuit 130 is provided at one end portions of the scanning signal lines 102. However, when the number of pixels in the horizontal direction is increased, there arises a problem attributed to the rounding of waveform of scanning signals. As a method for solving such a problem, it may be possible to provide the vertical drive circuits 130 at both ends of the scanning signal lines 102. However, when the pixel potential control circuit 135 is formed, it has been found out that there is no tolerance or margin of area for mounting the vertical drive circuits 130 at both ends of the scanning signal lines 102 depending on the circuit size. Accordingly, a circuit having a circuit size smaller than that of the vertical drive circuits 130 is provided as an auxiliary circuit (pull-up circuit) 145 of the vertical drive circuit 130 to solve the problem caused by the rounding of waveform of the scanning signals.

[0079] As shown in FIG. 5, the pull-up circuit 145 is connected to the end portions of the scanning signal lines 102 at the pixel potential control circuit 135 side. The pull-up circuit 145 is controlled in response to signals transmitted through the control signal line 143 and functions such that the power source line having the voltage VBB and the scanning signal line 102 are connected and the potential of the scanning signal line 102 assumes the voltage VBB. The voltage VBB is a voltage which makes the active element 30 (see FIG. 2) of the pixel portion assume the OFF state and the pull-up circuit 145 assists the active element 30 to assume the OFF state. That is, the pull-up circuit 145 functions such that the active element 30 which is remote from the vertical drive circuit 130 and largely receives the rounding of waveform attributed to the wiring resistance sharply assumes the OFF state.

[0080] The rounding of waveform becomes apparent due to the increase of the number of pixels in the horizontal direction which becomes necessary to cope with the demand for high resolution, the increase of wiring resistance of the scanning signal lines and the deterioration of parasitic capacitance. This rounding of waveform is a phenomenon in which with respect to the signal waveform of the near end side from the output terminal of the vertical drive circuit 130 which drives the scanning signal lines, in the rise and the fall of the signal waveform of the far end side, the change of the

voltage is not sharp (becomes dull). The rounding of waveform differs depending on the distance from the vertical drive circuit 130. Due to this difference in the rounding of waveform, there arises a difference in the jump potential thus giving rise to lowering of display quality such as flickers or lateral smears. The jump potential is a phenomenon in which when the scanning signal line assumes the non-selected state due to the gate terminal of the active element 30 and the parasitic capacitance of the pixel electrode, the potential of the pixel electrode is changed.

[0081] In general, due to the jump potential, the direct current component remains in the pixel electrode with respect to the voltage of the counter electrode (common voltage). To eliminate the residual direct current components, the adjustment is made to set the common potential to the optimum voltage (to eliminate the direct current component). However, when the jump potential differs between the left and right of the screen, with the mere adjustment of the common potential, it is difficult to eliminate the difference in direct current component between the left and the right of the screen. Accordingly, in the circuit shown in FIG. 5, the auxiliary circuit (pull-up circuit) 145 is provided and, to solve the problem attributed to the jump potential, the scanning signal line is driven from both ends thereof at the time of off-switching of the active element 30.

[0082] In the auxiliary circuit 145 shown in FIG. 5, to reduce the rounding of waveform at the left and the right of the screen and thereby to set the jump potential at both ends of the scanning signal line to the same level, the display quality is made uniform in the horizontal direction. Further, by using the pull-up circuit as the auxiliary circuit 145, the auxiliary circuit 145 is constituted such that one switching element is provided per one scanning signal line and hence, it is possible to form the auxiliary circuit in the narrow region. Here, although the switching element is formed of the p-type transistor, when the active element 30 is formed of the n-type transistor thus forming the switching element which assumes the OFF state at a low voltage, the auxiliary circuit 145 can be formed of the pull-down circuit and the n-type switching element can be used.

[0083] Next, the clocked inverters 61, 62 used in the double-way shift register SR are explained in conjunction with FIG. 6A and FIG. 6B. In the drawing, symbol UD1 indicates a first direction setting line and symbol UD2 indicates a second direction setting line.

[0084] The first direction setting line UD1 shown in FIG. 6A assumes an H level when the scanning is made from below to above in FIG. 5 and the second direction setting line UD2 shown in FIG. 6A assumes an H level when the scanning is made from above to below in FIG. 5. Although wiring is omitted for facilitating the understanding of the constitution in FIG. 5, both of the first direction setting line UD1 and the second direction setting line UD2 are connected to the clocked inverters 61, 62 which constitute the double-way shift register SR.

[0085] The clocked inverter 61 comprises, as shown in FIG. 6A, p-type transistors 71, 72 and n-type transistors 73, 74. The p-type transistor 71 is connected to the second direction setting line UD2, while the n-type transistor 74 is connected to the first direction setting line UD1. Accordingly, when the first direction setting line UD1 is at the H level and the second direction setting line UD2 is at the L

level, the clocked inverter 61 functions as the inverter, and when the second direction setting line UD2 is at the H level and the first direction setting line UD1 is at the L level, the clocked inverter 61 functions as the high impedance.

[0086] To the contrary, in the clocked inverter 62, as shown in FIG. 6B, the p-type transistor 71 is connected to the first direction setting line UD1, while the n-type transistor 74 is connected to the second direction setting line UD2. Accordingly, the clocked inverter 62 functions as an inverter when the second direction setting line UD2 is at the H level and functions as the high impedance when the first direction setting line UD1 is at the H level.

[0087] Then, the clocked inverter 65 has the circuit constitution shown in FIG. 6C, wherein when the clock signal line CLK1 is at the H level and the clock signal line CLK2 is at the L level, an input is outputted in a reversed manner, while when the clock signal line CLK1 is at the L level and the clock signal line CLK2 is at the H level, the clocked inverter 65 becomes the high impedance.

[0088] Further, the clocked inverter 66 has the circuit constitution shown in FIG. 6D, wherein when the clock signal line CLK2 is at the H level and the clock signal line CLK1 is at the L level, an input is outputted in a reversed manner, while when the clock signal line CLK2 is at the L level and the clock signal line CLK1 is at the H level, the clocked inverter 66 becomes the high impedance. In FIG. 6, although the wiring of the clock signal lines is omitted, the clock signal lines CLK1, CLK2 are connected to the clocked inverters 65, 66 in FIG. 6.

[0089] As explained above, since the double-way shift register SR is constituted of the clocked inverters 61, 62, 65, 66, it is possible to sequentially output the timing signals. Further, since the pixel potential control circuit 135 is constituted of the double-way shift register SR, it is possible to scan the pixel potential control signals $\Phi 3$ in two ways. That is, the vertical drive circuit 130 is also constituted of the similar double-way shift register so that the liquid crystal display device according to the present invention can perform scanning in two ways consisting of upper and lower directions. Accordingly, when an image to be displayed is reversed up side down, the scanning direction is reversed and scanning is performed from below to above in the drawing. Accordingly, when the vertical drive circuit 130 performs scanning from below to above, the pixel potential control circuit 135 also changes setting of the first direction setting line UD1 and the second direction setting line UD2 so as to cope with scanning from below to above. Here, the horizontal shift register 121 is also constituted by the similar double-way shift register.

[0090] Subsequently, the vertical drive circuit 130 is explained in conjunction with FIG. 7 and FIG. 8. FIG. 7 is a schematic circuit diagram of the vertical drive circuit 130 and FIG. 8 is a timing chart of the circuit shown in FIG. 7. The vertical drive circuit 130 shown in FIG. 7 is also constituted of the double-way shift register VSR and is capable of scanning in two directions. Although the vertical drive circuit 130 also has the constitution similar to the constitution of the above-mentioned pixel potential control circuit 135 in the same manner, a vertical scanning control circuit indicated by numeral 144 is added. The vertical scanning control circuit 144 controls an output GS of the double-way shift register VSR through the vertical scanning

control lines CNT1 and CNT2. Upon receiving the signals through the vertical scanning control lines CNT1 and CNT2, the vertical drive circuit 130 can perform various driving including sequential scanning driving, 2 line simultaneous driving and 1 line jump scanning driving. Here, the vertical scanning control lines CNT1 and CNT2 constitute a portion of control signal lines 131 shown in FIG. 1 and the like.

[0091] FIG. 8 shows drive timing when the sequential scanning driving is performed in the normal direction from above to below in the drawing at the vertical drive circuit 130 shown in FIG. 7. As video signals, during 1H (1 horizontal scanning period), arbitrary voltages are outputted as gray scale voltages from the horizontal drive circuit 120. To fetch the gray scale voltages into the pixel electrodes, the vertical drive circuit 130 outputs the scanning signals (G1-Gn) to make the active elements of the pixel portions assume the ON state during 1H.

[0092] Symbol VCLK indicates a clock inputted to the clocked inverters 65, 66 and corresponds to the clock CLK shown in FIG. 6. Symbol VDin indicates a scanning start signal and is inputted through the terminal 26. Symbol UD indicates a signal which determines whether scanning is in the normal direction or in the reverse direction and the normal direction is set when the signal is at the high level in FIG. 8. Symbol VDout indicates a scanning completion signal and is outputted from the terminal 27 after completion of scanning. Symbols CNT1 and CNT2 indicate signals (vertical scanning control signals) of the above-mentioned vertical scanning control lines.

[0093] The double-way shift register VSR1 holds and outputs the input signal at a falling edge of the clock VCLK and holds the value until a falling edge of next clock VCLK. Accordingly, an output from the double-way shift register VSR1 exhibits a waveform indicated by GS1. Further, the double-way shift register VSR2 holds and outputs the input signal at a rising edge of the clock VCLK and holds the value until a rising edge of next clock VCLK. Accordingly, an output from the double-way shift register VSR2 exhibits a waveform indicated by GS2. Then, the vertical scanning control signals CNT1 and CNT2 are outputted as shown in FIG. 8, are subjected to computing in an AND circuit of the vertical scanning control circuit 144, and are outputted to the scanning signal lines 102 as scanning signals G1-Gn from an output buffer 69.

[0094] Subsequently, the operation of the pull-up circuit 145 is explained in conjunction with FIG. 9 and FIG. 10. In FIG. 9, to prevent the drawing from becoming complicated, circuits on the left and right peripheries of the display part 110 are shown. The pull-up circuit 145 is controlled in response to the signals through the above-mentioned vertical scanning control lines CNT1 and CNT2. The control signal line 143 is connected to output terminals of the vertical scanning control lines CNT1 and CNT2 and is connected to an input terminal of the pull-up circuit 145. Here, the level shifter 67 converts the voltage to produce a voltage with which switching elements of the pull-up circuit 145 can be driven.

[0095] Also in FIG. 10, the signals of the vertical scanning control lines CNT1 and CNT2 are outputted in the same manner as FIG. 8. By making the values of the vertical scanning control signals CNT1 and CNT2 subjected to NOR computing, it is possible to produce a control signal VP

outputted to the control signal line 143. The control signal VP makes the switching elements of the pull-up circuit 145 assume the ON state at the timing that the scanning signals G1-Gn assume the high level.

[0096] With the provision of the pull-up circuit 145, at the time of OFF switching in which the active element 30 of the pixel portion is changed from the ON state to the OFF state, it is possible to drive the scanning signal line 103 from both ends and to make the scanning signal line 103 assume the voltage VBB. Here, the case in which the active element 30 of the pixel portion is constituted of the P-type MOS transistor which assumes the ON state when the scanning signal is at the low level has been explained. However, the active element 30 can be constituted of either a P-type MOS transistor or an N-type MOS transistor.

[0097] Subsequently, a circuit which prevents blurring of images in the horizontal direction which is called a ghost in the horizontal drive circuit 120 is explained in conjunction with FIG. 11 and FIG. 12. In FIG. 11, symbol HSR indicates a double-way shift register which constitutes the horizontal shift register 121 of the horizontal drive circuit 120. Symbol 125 is a delay circuit which is served for preventing the ghost by delaying an output signal from the double-way shift register HSR by a fixed period. The delay circuit 125 receives output signals from the double-way shift register HSR through signal lines of two systems, wherein by providing two pieces of inverters to one signal line, inputting of the output signal to the AND circuit is delayed by an amount of time which is necessary for passing the inverter. Accordingly, the rise of the output signal from the AND circuit is delayed by this delayed time.

[0098] An output of the AND circuit is inputted to a gate circuit 89. Symbols VIM1, VIM2 indicate video signal supply lines through which video signals are supplied. When the gate circuit 89 assumes the ON state, the video signal supply lines VIM1, VIM2 and the video signal line 103 assume the conductive state to each other and hence, the video signals are outputted to the video signal lines 103. The gate circuit 89 assumes the ON state when the gate circuit 89 is selected for a fixed period in response to sampling pulses outputted from the double-way shift register HSR. Here, in the circuit shown in FIG. 11, a case in which the video signals are supplied in a form that they are divided in two phases is shown. Accordingly, two signal lines consisting of video signal supply lines IMG1 and IMG2 are alternately connected to the gate circuit 89.

[0099] As one of causes of the ghost, the increase of the width of the sampling pulse is named. From the horizontal shift register 121 shown in FIG. 11, the sampling pulses are outputted as indicated by symbol DS in FIG. 12. However, when the rounding is generated in the sampling pulses DS, the width of sampling pulse is increased and hence, the video signals are simultaneously supplied to two video signal lines or the video signals to be outputted are written in the different video signal lines whereby the images are blurred thus giving rise to the ghost.

[0100] To explain the above by taking the video signal lines 103(1) and 103(3) of the circuit shown in FIG. 11 as an example, when outputs are overlapped at starting and completion of signals as in the case of pulses DS1 and DS3 in FIG. 12, at the completion of outputting of the video signals to the video signal line 103(1) and at the starting of

outputting to the video signal line **103(3)**, in the state that the gate circuit **89(1)** is not completely turned off, the gate circuit **89(3)** assumes the ON state and hence, a portion of data of the video signal line **103(1)** is leaked into the video signal line **103(3)**. Accordingly, there arises a problem that a so-called ghost phenomenon in which displays of the neighboring signal lines are observed in an overlapped manner is generated.

[0101] In the circuit shown in **FIG. 11**, the delay circuit is provided between the output terminal of the horizontal shift resistor **121** and the gate circuit **89** so as to delay the rise of the sampling pulse. As shown in **FIG. 12**, with respect to the fall of the sampling pulse **D1**, the sampling pulse **D3** rises with a delay. Accordingly, it is possible to prevent the video signal to be written in the video signal line **103(1)** due to the gate circuit **89(3)** which is made to assume the ON state in response to the sampling pulse **D3** from being written in the video signal line **103(3)** which is different from the video signal line **103(1)**.

[0102] When the video signals are transmitted in a form that the video signal is developed in a plurality of phases, the video signals which are erroneously written constitute video signals which are separated by several lines and hence, the ghost which is generated due to the rounding of sampling pulse becomes apparent. For example, when the number of gate circuit **89** which the double-way shift register HSR controls is 6, the ghost phenomenon is generated at an interval of 6 rows and hence, there arises a problem that the display quality is remarkably degraded. Here, besides the delay circuit described in **FIG. 11**, it may be possible to adopt the constitution in which the rising speed at the time of turning on the circuit (for example, the level shift circuit **67**) provided between the double-way shift resistor HSR and the gate circuit **89** is delayed and the falling speed at the time of turning off the circuit is increased.

[0103] Next, the pixel portion of the reflection-type liquid crystal display device according to the present invention is explained. **FIG. 13** is a schematic cross-sectional view of reflection-type liquid crystal display device which constitutes one embodiment of the present invention. In **FIG. 13**, numeral **100** indicates a liquid crystal panel, numeral **1** indicates a drive circuit substrate which constitutes a first substrate, numeral **2** indicates a transparent substrate which constitutes a second substrate, numeral **3** indicates liquid crystal composition, and numeral **4** indicate spacers. The spacers **4** are formed so as to form a cell gap *d* which is a fixed gap between the drive circuit substrate **1** and the transparent substrate **2**. The liquid crystal composition **3** is sandwiched in the cell gap *d*. Numeral **5** indicates reflection electrodes (pixel electrodes) which are formed on the drive circuit substrate **1**. Numeral **6** indicates counter electrodes and voltages are applied to the liquid crystal composition **3** filled between the counter electrodes **6** and the reflection electrodes **5**. Numeral **7,8** are orientation films which orient the liquid crystal molecules in a fixed direction. Numeral **30** indicates active elements which supply gray scale voltages to the reflection electrodes **5**.

[0104] Numeral **34** indicates a source region of the active element **30**, numeral **35** indicates a drain region of the active element **30** and numeral **36** indicates a gate electrode. Numeral **38** indicates an insulation film, numeral **31** indicates a first electrode which forms pixel capacitance, and

numeral **40** indicates a second electrode which forms the pixel capacitance. The first electrode **31** and the second electrode **40** form capacitance by way of the insulation film **38**. In **FIG. 7**, the first electrode **31** and the second electrode **40** are indicated as typical electrodes which form the pixel capacitance. However, it is also possible to form the pixel capacitance provided that a conductive layer which is electrically connected to the pixel electrode and a conductive layer which is electrically connected to the pixel potential control signal line face each other while sandwiching a dielectric layer therebetween in an opposed manner.

[0105] Numeral **41** indicates a first interlayer film and numeral **42** indicates the first conductive film. The first conductive film **42** electrically connects the drain region **35** and the second electrode **40**. Numeral **43** indicates a second interlayer film, numeral **44** indicates a first light shielding film, numeral **45** indicates a third interlayer film and numeral **46** indicates a second light shielding film. A through hole **42CH** is formed in the second interlayer film **43** and the third interlayer film **45**, while the first conductive film **42** and the second light shielding film **46** are electrically connected. Numeral **47** indicates a fourth interlayer film and numeral **48** indicates a second conductive film which forms a reflection electrode **5**. The gray scale voltage is transmitted to the reflection electrode **5** from the drain region **35** of the active element **30** through the first conductive film **42**, the through hole **42CH** and the second light shielding film **46**.

[0106] The liquid crystal display device of this embodiment is of a reflection type and a large quantity of light is radiated to the liquid crystal panel **100**. A light shielding film prevents light from being incident on the semiconductor layer of the drive circuit substrate. In the reflection-type liquid crystal display device, the light radiated to the liquid crystal panel **100** is incident from the transparent substrate **2** side (upper side in **FIG. 13**), permeates the liquid crystal composition **3** and is reflected on the reflection electrodes **5**. Then, again, the light permeates the liquid crystal composition **3** and the transparent substrate **2** and is irradiated from the liquid crystal panel **100**. However, a portion of the light radiated to the liquid crystal panel **100** leaks into the drive circuit substrate side through gaps defined between the reflection electrodes **5**. The first light shielding film **44** and the second light shielding film **46** are provided such that the light is not incident on the active element **30**. In this embodiment, the light shielding films are formed of a conductive layer. Further, by electrically connecting the second light shielding film **46** with the reflection electrode **5** and by supplying the pixel potential control signal to the first light shielding film **44**, the light shielding films also function as a portion of the pixel capacitance.

[0107] Here, by supplying the pixel potential control signal to the first light shielding layer **44**, it is possible to provide the light shielding film **44** as an electric shielding layer between the second light shielding film **46** to which the gray scale voltage is applied, the first conductive layer **42** which forms the video signal lines **103** and a conductive layer (a conductive layer formed on the same layer as the gate electrodes **36**) which forms the scanning signal lines **102**. Accordingly, a parasitic capacitance component between the first conductive layer **42** and the gate electrodes **36** and the like and the second light shielding film **46** and the reflection electrodes **5** can be reduced. As mentioned previously, although it is necessary to sufficiently increase the

pixel capacitance CC with respect to the liquid crystal capacitance CL, by providing the first light shielding film 44 as the electric shielding layer, the parasitic capacitance which is connected in parallel to the liquid crystal capacitance LC can be reduced and hence, it is possible to efficiently increase the pixel capacitance CC with respect to the liquid crystal capacitance CL. Further, it is also possible to decrease the jump of noises from the signal lines.

[0108] When the liquid crystal display device is formed of a reflection type and the reflection electrodes 5 are formed on a surface of the drive circuit substrate 1 at the liquid crystal composition 3 side, it is possible to use an opaque silicon substrate or the like as the drive circuit substrate 1. Further, it is possible to mount the active elements 30 and the wiring below the reflection electrodes 5 and hence, the reflection electrodes 5 which constitute the pixels can be widened thus giving rise to an advantageous effect that a so-called high numerical aperture can be realized. Further, it is also possible to obtain an advantageous effect that heat generated due to the light radiated to the liquid crystal panel 100 can be dissipated from a back surface of the drive circuit substrate (also referred to as the silicon substrate) 1.

[0109] Then, the utilization of the light shielding film as a portion of the pixel capacitance is explained. The first light shielding film 44 and the second light shielding film 46 face each other in an opposed manner while sandwiching a third interlayer film 45 therebetween and form a portion of the pixel capacitance. Numeral 49 indicates a conductive layer which forms a portion of the pixel potential control line 136. The first electrode 31 and the first light shielding film 44 are electrically connected by the conductive layer 49. Further, it is also possible to form wiring from the pixel potential control circuit 135 to the pixel capacitance using the conductive layer 49. In this embodiment, the first shielding film 44 is used as the wiring. FIG. 14 shows the constitution in which the first light shielding film 44 is utilized as the pixel potential control line 136.

[0110] FIG. 14 is a plan view showing the arrangement of the first light shielding film 44. Although numeral 46 indicates the second light shielding film, to show the position thereof, they are shown in a dotted line. Numeral 42CH indicates the through holes which are provided for connecting the first conductive film 42 and the second light shielding film 46. Here, in FIG. 14, for facilitating the understanding of the first light shielding films 44, other constitutions are omitted. The first light shielding films 44 have a function of the pixel potential control line 136 and are formed continuously in the X direction in the drawing. Although the first light shielding films 44 are configured to cover the entire surface of the display region so as to function as the light shielding film, to allow the first light shielding films 44 to have also the function of the pixel potential control line 136, the first light shielding films 44 are formed linearly such that they extend in the X direction (the direction parallel to the scanning signal line 102), are arranged in parallel in the Y direction and are connected to the pixel potential control circuit 135. Further, since the first light shielding film 44 also functions as the electrode of the pixel capacitance, the first light shielding film 44 is formed such that the first light shielding film 44 is overlapped to the second light shielding film 46 with an area as large as possible. Furthermore, as the

light shielding film which can reduce leaking of light, a gap between the neighboring first light shielding films 44 is set as narrow as possible.

[0111] However, when the gap between the neighboring first light shielding films 44 is narrowed as shown in FIG. 14, a portion of the first light shielding film 44 is overlapped to the second light shielding film 46 arranged close to the first light shielding film 44. As mentioned previously, the liquid crystal display device of the present invention is capable of performing scanning in two ways. Accordingly, when the pixel potential control signals are scanned in two ways, there arise a case in which the first light shielding film 44 is overlapped to the second light shielding film 46 of next stage and a case in which the first light shielding film 44 is not overlapped to the second light shielding film 46 of next stage. In the case shown in FIG. 14, when the scanning is performed from above to below, the first light shielding film 44 is overlapped to the second light shielding film 46 of next stage.

[0112] Using FIG. 15A and FIG. 15B, a drawback attributed to overlapping of the portion of the first light shielding film 44 to the second light shielding film 46 of the next stage and a method for solving such a drawback are explained. FIG. 15A is a timing chart for explaining the drawback. $\Phi 2A$ indicates a scanning signal of an arbitrary row and is assumed as the scanning signal of the Ath row. $\Phi 2B$ indicates the scanning signal of next-stage row and is assumed as the scanning signal of the Bth row. Here, a period from a point of time t_2 to a point of time t_3 in which the drawback arises is explained and the explanation of other periods is omitted.

[0113] In FIG. 15A, in the Ath row, the pixel potential control signal $\Phi 3A$ is changed at a point of time t_3 after a lapse of 2 h (2 horizontal scanning time) from the point of time t_2 . After a lapse of 1 h from the point of time t_2 , outputting of the scanning signal $\Phi 2A$ is completed and hence, the active elements 30 of the Ath row driven by the scanning signal $\Phi 2A$ assumes the OFF state and the pixel electrodes 109 of the Ath row are separated from the video signal lines 103. At the point of time t_3 after a lapse of 2 h from the point of time t_2 , even when the delay caused by changeover of signals or the like is taken into consideration, the active elements 30 of the Ath row are sufficiently set to the OFF state. However, the point of time t_3 is a point of time that the scanning signal $\Phi 2B$ of the Bth row is changed over.

[0114] Since the first light shielding film 44 of the Ath row and the second light shielding film 46 of the Bth row are overlapped to each other, the capacitance is generated between the pixel electrodes of the Bth row and the pixel potential control signal lines of the Ath row. Since the point of time t_3 is a point of time that the active elements 30 of the Bth row are changed over to the OFF state and hence, the pixel electrodes 109 of the Bth row are not sufficiently terminated from the video signal lines 103. When the pixel potential control signals $\Phi 3A$ having a capacitance component are changed over between the pixel electrodes 109 of the Bth row and the pixel potential control signals $\Phi 3A$ at this point of time, since the pixel electrodes 109 and the video signal lines 103 are not sufficiently terminated, charge is moved between the video signal lines 103 and the pixel electrodes 109. That is, the changeover of the pixel potential

control signals $\Phi 3A$ of the Ath row gives an influence to the voltage $\Phi 4B$ written in the pixel electrodes **109** of the Bth row.

[0115] When the scanning direction of the liquid crystal display device is fixed, the influence attributed to the pixel potential control signals $\Phi 3A$ becomes uniform and hence, it is not apparent. However, when liquid crystal display devices are provided for respective colors of red, green, blue and the like and color display is performed by superposing outputs of respective liquid crystal display devices, due to a reason based on an optical arrangement of the liquid crystal display devices, for example, scanning from below to above is performed only with respect to one liquid crystal display device and scanning is performed from above to below with respect to other liquid crystal display devices. In this manner, when there exist the liquid crystal display devices which differ in scanning directions out of a plurality of liquid crystal display devices, the display quality becomes non-uniform and hence, the aesthetic appearance is damaged.

[0116] Next, the method for solving the above-mentioned drawback is explained in conjunction with FIG. 15B. The pixel potential control signal $\Phi 3A$ of the Ath row is configured to be outputted 3 h later from starting of the scanning signal $\Phi 2A$ of the Ath row. In this case, the scanning signal $\Phi 2B$ of the Bth row is already changed over so that the active elements **30** of the Bth row are sufficiently held in the OFF state and hence, the influence that the pixel potential control signal $\Phi 3A$ of the Ath row gives to the voltage $\Phi 4B$ written in the pixel electrodes **109** of the Bth row is reduced.

[0117] Although the period in which an input signal for negative polarity is written is shortened by 3 h with respect to an input signal for positive polarity, when the number of scanning signal lines **102** exceeds 100, for example, this takes a value equal to or less than 3%. Accordingly, the difference in effective value between the input signal for negative polarity and the input signal for positive polarity can be adjusted based on the value of the reference potential V_{com} or the like.

[0118] Next, the relationship between the voltage V_{PP} supplied to the pixel capacitance and the substrate potential V_{BB} is explained in conjunction with FIG. 16A and FIG. 16B. FIG. 16A indicates an inverter circuit which constitutes an output circuit **69**.

[0119] In FIG. 16A, numeral **32** indicates a channel region of a p-type transistor, wherein an n-type well is formed in a silicon substrate **1** by a method such as ion implantation. The substrate voltage V_{BB} is supplied to the silicon substrate **1** so that the potential of the n-type well **32** is set to V_{BB} . The source region **34** and the drain region **35** are formed of a p-type semiconductor layer and these regions are formed on the silicon substrate **1** by a method such as ion implantation or the like. When a voltage having a potential lower than the substrate voltage V_{BB} is applied to the gate electrode **36** of the p-type transistor **30**, the source region **34** and the drain region **35** become conductive with each other.

[0120] In view of the fact that it is unnecessary to provide insulation portions and hence, the structure can be simplified in general, the common substrate potential V_{BB} is applied to the transistors mounted on the same silicon substrate. In the liquid crystal display device of the present invention, transistors of the drive circuit portions and the transistors of

the pixel portions are formed on the same silicon substrate **1**. Due to the similar reason, the substrate voltage V_{BB} of the same potential is applied to the transistors of the pixel portions.

[0121] In the inverter circuit shown in FIG. 16A, the voltage V_{PP} supplied to the pixel capacitance is applied to the source region **34**. The source region **34** is a p-type semiconductor layer and a pn junction is formed between the source region **34** and the n-type well **32**. When the potential of the source region **34** exceeds the potential of the n-type well **32**, there arises a drawback that an electric current flows into the n-type well **32** from the source region **32**. Accordingly, the voltage V_{PP} is set to the potential lower than the substrate voltage V_{BB} .

[0122] As mentioned previously, assuming the voltage written in the pixel electrode as V_2 , the liquid crystal capacitance as CL , the pixel capacitance as CC , and amplitudes of the pixel electrode control signal as V_{PP} and V_{SS} , the voltage of the pixel electrode after voltage drop is expressed by an equation $V_2 - \{CC/(CL+CC)\} \times (V_{PP} - V_{SS})$. Here, when a GND potential is selected as V_{SS} , the magnitude of the voltage change of the pixel electrodes is determined based on the voltage V_{PP} , the liquid crystal capacitance CL and the pixel capacitance CC .

[0123] The relationship between the $CC/(CL+CC)$ and the voltage V_{PP} is explained in conjunction with FIG. 16B. Here, to simplify the explanation, the reference voltage V_{com} is set to the GND potential. Further, a case which adopts a method in which a white display is performed when the voltage is not applied (normally white) and a gray scale voltage which produces a black display (minimum gray scale) is applied to the pixel electrodes is explained. $\Phi 1$ in FIG. 16B indicates the gray scale voltage which is written in the pixel electrodes from the voltage selection circuit **123**. $\Phi 1A$ is the gray scale voltage of positive polarity and $\Phi 2A$ is the gray scale voltage of negative polarity. Since the black display is adopted, both gray scale voltages $\Phi 1A$, $\Phi 1B$ are set such that the potential difference between the reference voltage V_{com} and the gray scale voltage written in the pixel electrode assumes a maximum value. In FIG. 16B, since the gray scale voltage $\Phi 1A$ is a signal for positive polarity, the gray scale voltage $\Phi 1A$ is set to $+V_{max}$ such that the potential difference between the reference voltage V_{com} and the gray scale voltage $\Phi 1A$ takes the maximum value in the same manner as the conventional technique, while the gray scale voltage $\Phi 1B$ is written in the pixel electrode as the reference voltage V_{com} (GND) and, thereafter, is lowered using the pixel capacitance.

[0124] Both of $\Phi 4A$, $\Phi 4B$ indicate the voltages of pixel electrodes, wherein the voltage $\Phi 4A$ shows a case in which $CC/(CL+CC)=1$ is ideal and the voltage $\Phi 4B$ indicates a case in which $CC/(CL+CC)$ is equal to or less than 1. When the voltage $\Phi 4A$ has negative polarity, since the reference voltage V_{com} (GND) is written in the gray scale voltage $\Phi 1B$, $-V_{max}$ which is lowered in accordance with the amplitude V_{PP} of the pixel electrode control signal is set to $-V_{max} = -V_{PP}$ based on the equation $CC/(CL+CC)=1$.

[0125] To the contrary, with respect to the voltage $\Phi 4B$ of the pixel electrodes, since $CC/(CL+CC)$ is equal to or less than 1, it is necessary to supply the pixel electrodes control signal such that the relationship $+V_{max} < V_{PP2}$ is established. As mentioned previously, it is necessary to satisfy the

relationship $V_{PP} < V_{BB}$, the relationship $+V_{max} < V_{PP} < V_{BB}$ is established. Here, to provide the circuits having low dielectric strength, a method which lowers the pixel voltage is adopted. However, when the voltage V_{PP} of the pixel electrode control signal assumes the high voltage, there arises a drawback that the substrate voltage V_{BB} also assumes the high voltage and hence, circuits having high dielectric strength are provided. Accordingly, it is necessary to determine the values of CL and CC such that $CC/(CL+CC)$ approaches 1 as close as possible. That is, the relationship $CL \ll CC$ is established.

[0126] Here, in the conventional liquid crystal display device which forms thin film transistors on a glass substrate, it is necessary to make the pixel electrodes as wide as possible (so-called high numerical aperture) and hence, the relationship which can be realized is $CL=CC$ at best. Further, since the drive circuit portions and the pixel portions are formed on the same silicon substrate according to the liquid crystal display device of the present invention, the liquid crystal display device has a drawback that when the substrate potential V_{BB} assumes the high voltage, lowering of dielectric strength cannot be realized.

[0127] As shown in FIG. 16, since the pixel electrode control signal can be set using the power source voltage of the inverter circuit and hence, with respect to the voltage V_{PP} , it is possible to form the optimum voltage within the circuit and it is also possible to supply the voltage V_{PP} from the outside and to adjust the voltage V_{PP} to the maximum voltage.

[0128] Next, an embodiment in which line inversion driving is performed is explained in conjunction with FIG. 17 and FIG. 18. The liquid crystal display device 100 shown in FIG. 17 has a pixel potential control circuit 135(1) for odd-numbered lines and pixel potential control circuit 135(2) for even-numbered lines. In the line inversion driving, when the gray scale voltage having positive polarity is written in the pixel electrodes of the odd-numbered row, for example, the gray scale voltage having negative polarity is written in the pixel electrodes of even-numbered rows so as to perform the alternating driving. In the line inversion driving, since the polarity is inverted every row, it is necessary to change over the waveform of the pixel potential control signal for every row. Accordingly, as shown in FIG. 17, the pixel potential control signal circuits for odd-numbered rows and even-numbered rows are provided so as to alternately output two types of waveforms like the pixel potential control signals $\Phi 3a$, $\Phi 3b$ as shown in FIG. 18 thus realizing the line inversion driving.

[0129] Subsequently, the reflection-type liquid crystal display device is explained. As one of reflection-type liquid crystal display devices, there has been known an electrically controlled birefringence mode. In this electrically controlled birefringence mode, a voltage is applied between reflection electrodes and counter electrodes, the molecular arrangement of the liquid crystal composition is changed and, eventually, the refractive index anisotropy is changed in the liquid crystal panel. The electrically controlled birefringence mode forms images by making use of the change of the refractive index anisotropy as the change of the optical transmittance.

[0130] Further, using FIG. 19A and FIG. 19B, a single polarizer twist nematic mode (SPTN) which constitutes one

of the electrically controlled birefringence modes is explained. Numeral 9 indicates a polarized beam splitter which divides an incident light L1 from a light source (not shown in the drawing) into two polarized lights and irradiates light L2 which is formed into linear polarized light. Although light (P wave) which penetrates the polarization beam splitter 9 is used as light to be incident on the liquid crystal panel 100 in FIG. 19A and FIG. 19B, it is possible to use light (S wave) which is reflected on the polarization beam splitter 9. The liquid crystal composition 3 has a long axis of liquid crystal molecules arranged parallel to a drive circuit substrate 1 and a transparent substrate 2 and adopts nematic liquid crystal having positive dielectric anisotropy. Further, the liquid crystal molecules are oriented in a state that they are twisted by approximately 90 degrees due to the orientation films 7, 8.

[0131] First of all, a case in which the voltage is not applied is shown in FIG. 19A. Light which is incident on the liquid crystal panel 100 is formed into an elliptical polarized light due to birefringence of the liquid crystal composition 3 and is formed into a circular polarized light on a surface of the reflection electrode 5. The light which is reflected on the reflection electrode 5 again passes the inside of the liquid crystal composition 3 and is formed into the elliptical polarized light again and returns to the linear polarized light at the time of irradiation and thereafter, is irradiated as the light L3 (S wave) whose phase is rotated by 90 degrees with respect to the incident light L2. Although the irradiated light L3 is again incident on the polarization beam splitter 9, the irradiated light L3 is reflected on the polarization surface and is formed into the irradiated light L4. This irradiated light L4 is radiated to a screen or the like for performing a display. In this case, a so-called normally white (normally open) display method is adopted in which light is radiated when the voltage is not applied.

[0132] To the contrary, a case in which the voltage is applied to the liquid crystal composition 3 is shown in FIG. 19B. When the voltage is applied to the liquid crystal composition 3, the liquid crystal molecules are arranged in the electric field direction and hence, a rate that the birefringence is generated in the liquid crystal is reduced. Accordingly, the light L2 incident on the liquid crystal panel 100 due to the linear polarization is directly reflected on the reflection electrode 5 and light L5 having the same polarization direction as incident light L2 is irradiated. The irradiation light L5 passes the polarization beam splitter 9 and returns to the light source. Accordingly, light is not irradiated to the screen or the like thus the black display is performed.

[0133] In the single polarizer twist nematic mode, the orientation direction of the liquid crystal is parallel to the substrate and hence, it is possible to use the general orientation method and favorable process stability is obtained. Further, to use the liquid crystal display device in the normally white mode, it is possible to have tolerance with respect to a defective display which occurs at the low voltage side. That is, in the normally white method, the dark level (black display) is obtained in a state that the high voltage is applied. In the case of this high voltage, most of the liquid crystal molecules are arranged in the electric field direction vertical to the substrate surface and hence, the display of dark level does not largely depend on the initial orientation direction at the time of low voltage. Further,

human eyes recognize the brightness irregularities as the relative rate of brightness and has a reaction which approximates a logarithmic scale with respect to the brightness. Accordingly, human eyes are sensitive to the change of dark level. Due to such a reason, the normally white method is an advantageous display method for brightness irregularities attributed to the initial orientation state.

[0134] In the above-mentioned electrically controlled birefringence mode, the high accuracy of cell gaps is required. That is, the electrically controlled birefringence mode makes use of the phase difference between the abnormal light and the normal light which are generated during the period in which the light passes the inside of the liquid crystal and hence, the intensity of the transmitting light depends on the retardation And between the abnormal light and the normal light. Here, Δn is the birefringence anisotropy and d is the cell gap between the transparent substrate 2 and the drive circuit substrate 1 formed by the spacers 4.

[0135] Accordingly, in this embodiment, the cell gap accuracy is set to a value equal to or less than $\pm 0.5 \mu\text{m}$ by taking the display irregularities into consideration. Further, in the reflection-type liquid crystal display device, the light which is incident on the liquid crystal is reflected on the reflection electrodes and again passes the liquid crystal and hence, when the liquid crystal having the same birefringence anisotropy Δn is used, the cell gap d is halved compared to the transmission-type liquid crystal display device. While the cell gap d is set to 5 to $6 \mu\text{m}$ with respect to the generally available transmission type liquid crystal display device, the cell gap is approximately $2 \mu\text{m}$ in this embodiment.

[0136] In this embodiment, to cope with the demand for higher cell gap accuracy and narrower cell gap, a method which forms columnar spacers on the drive circuit substrate 1 in place of a conventional bead scattering method is adopted.

[0137] FIG. 20 is a schematic plan view for explaining the arrangement of the reflection electrodes 5 and the spacers 4 mounted on the drive circuit substrate 1. A large number of spacers 4 are formed in a matrix array on the whole surface of the drive circuit substrate to hold the fixed distance or gap. The reflection electrode 5 is a minimum pixel of an image which the liquid crystal display device forms. In FIG. 20, for the sake of brevity, four pixels are shown in the longitudinal direction and five pixels are shown in the lateral direction by symbols 5A, 5B.

[0138] In FIG. 20, the pixels which are arranged in a matrix formed of four pixels in the longitudinal direction and five pixels in the lateral direction form the display region. An image to be displayed by the liquid crystal display element is formed on this display region. Outside the display region, dummy pixels 113 are provided. A peripheral frame 11 which is formed of the same material as the spacers 4 is provided to the periphery of the dummy pixels 113. Further, to the outside the peripheral frame 11, a sealing material 12 is applied. Numeral 13 indicates an external connection terminal which is served for supplying external signals to the liquid crystal panel 100.

[0139] A resin material is used as a material of the spacers 4 and the peripheral frame 11. As the resin material, for example, a chemical amplifying negative type resist "BPR-111" (product name) produced by JSR Corporation can be

used. To an upper surface of the drive circuit substrate 1 on which the reflection electrodes 5 are formed, a resist material is applied by a spin coating method or the like and the resist is exposed into a pattern of the spacers 4 and the peripheral frame 11 using a mask. Thereafter, the resist is developed using a removing agent so as to form the spacers 4 and the peripheral frame 11.

[0140] By forming the spacers 4 and the peripheral frame 11 using the resist material or the like as the raw material, it is possible to control the height of the spacers 4 and the peripheral frame 11 by adjusting a film thickness of the applying material so that the spacers 4 and the peripheral frame 11 can be formed with high accuracy. Further, positions of the spacers 4 can be determined using the mask pattern and hence, it is possible to accurately mount the spacers 4 at desired positions. In a liquid crystal projector, when the spacers 4 are present on the pixels, there may arise a drawback that shadows attributed to the spacers may appear in an enlarged projected image. By forming the spacers 4 by exposure and developing using the mask pattern, it is possible to mount the spacers 4 at positions which do not cause such a drawback when the image is displayed.

[0141] Further, since the peripheral frame 11 is simultaneously formed with the spacers 4, as a method for filling the liquid crystal composition 3 into a space defined between the drive circuit substrate 1 and the transparent substrate 2, a method in which the liquid crystal composition 3 is dropped onto the drive circuit substrate 1 and, thereafter, the transparent substrate 2 is laminated to the drive circuit substrate 1 can be used.

[0142] After arranging the liquid crystal composition 3 between the drive circuit substrate 1 and the transparent substrate 2 and assembling the liquid crystal panel 100, the liquid crystal composition 3 is held in a region surrounded by the peripheral frame 11. Further, a sealing material 12 is applied to the outside of the peripheral frame 11 and hence, the liquid crystal composition 3 is sealed in the inside of the liquid crystal panel 100. As mentioned previously, since the peripheral frame 11 is formed using the mask pattern, it is possible to form the peripheral frame 11 on the drive circuit substrate 1 with high accuracy. Accordingly, it is possible to define the boundary of the liquid crystal composition 3 with high accuracy. Further, with the use of the peripheral frame 11, it is possible to define a boundary of the region in which the sealing material 12 is formed with high accuracy.

[0143] The sealing material 12 has a role of fixing the drive circuit substrate 1 and the transparent substrate 2 as well as a role of preventing the intrusion of substances harmful to the liquid crystal composition 3. When applying the sealing material 12 having fluidity, the peripheral frame 11 performs a role of stopper for the sealing material 12. By providing the peripheral frame 11 as the stopper for the sealing material 12, it is possible to ensure the sufficient design tolerance with respect to the boundary of the liquid crystal composition 3 and the boundary of the sealing material 12 so that it is possible to narrow a distance between a peripheral side to the display region of the liquid crystal panel 100 (narrowing of picture frame).

[0144] The dummy pixels 113 are arranged between the peripheral frame 11 and the display region. The dummy pixels 113 are provided for making the display quality of the

outermost pixels **5B** and the inner pixels **5A** uniform. Since the neighboring pixels are present with respect to the inner pixels **5A**, an undesired electric field is generated between the neighboring pixels and hence, the display quality is degraded compared to the display quality when the neighboring pixels are not present. To the contrary, at the outermost pixels **5B**, when the dummy pixels **113** are not present, since an undesired electric field which degrades the display quality is not generated, the display quality is improved compared to the display quality of the inner pixel **5B**. When the difference in display quality is generated with respect to some pixels, this causes the display irregularities. Accordingly, by providing the dummy pixels **113** and by supplying signals in the same manner as the inner pixels **5A** and the outermost pixels **5B**, the display quality of the outermost pixels **5A** and the display quality of the inner pixels **5B** are made uniform.

[0145] Further, since the peripheral frame **11** is formed such that the peripheral frame **11** surrounds the display region, at the time of applying the rubbing treatment to the drive circuit substrate **1**, there arises a drawback that it is difficult to perform rubbing of the vicinity of the peripheral frame **11** due to the presence of the peripheral frame **11**. To orient the liquid crystal composition **3** in a fixed direction, an orientation film is formed and the rubbing treatment is applied to the orientation film. In this embodiment, after forming the spacers **4** and the peripheral frame **11** on the drive circuit substrate **1**, the orientation film **7** is formed by coating. Thereafter, the rubbing treatment is performed such that the orientation film **7** is rubbed with a cloth to orient the liquid crystal composition **3** in the fixed direction.

[0146] In the rubbing treatment, since the peripheral frame **11** is projected from the drive circuit substrate **1**, the orientation film **7** in the vicinity of the peripheral frame **11** is not sufficiently rubbed due to stepped portions formed by the peripheral frames **11**. Accordingly, portions where the orientation of the liquid crystal composition **3** is not uniform is liable to be formed in the vicinity of the peripheral frame **11**. Accordingly, to make the display irregularities attributed to the orientation defect of the liquid crystal composition **3** less apparent, several pixels arranged along the inner side of the peripheral frame **11** are formed as the dummy pixels **113** thus forming pixels which do not contribute to the display.

[0147] However, when the dummy pixels **113** are formed and the signals are supplied to the dummy pixels **113** in the same manner as the pixels **5A**, **5B**, since the liquid crystal composition **3** is present between the dummy pixels **113** and the transparent substrate **2**, there arises a drawback that the display by the dummy pixels **113** is also observed. In using the liquid crystal display device in the normally white mode, when the voltage is not applied to the liquid crystal composition **3**, the dummy pixels **113** are displayed in white. Accordingly, the boundary of the display region becomes indefinite and hence, the display quality is degraded. Although it may be considered to provide light shielding to the dummy pixels **113**, since the gap between the pixels is several μm , it is difficult to form light shielding frames on the boundary of the display region with high accuracy. Accordingly, in this embodiment, the voltage is applied to the dummy pixels **113** such that the dummy pixels **113** perform the black display whereby a black frame which surrounds the display region is observed.

[0148] The method for driving the dummy pixels **113** is explained in conjunction with FIG. 21. To apply the voltage which makes the dummy pixels **113** perform the black

display, the region where the dummy pixels **113** are provided is formed into a black display over the entire surface thereof. When the entire surface is turned into the black display, it is unnecessary to individually form the dummy pixels as in the case of the pixels formed in the display region. That is, it is possible to form an integral pixel by electrically connecting a plurality of dummy pixels. Further, to consider the time necessary for driving, it is wasteful to provide writing time for respective dummy pixels. Accordingly, it is possible to form one dummy pixel electrode by continuously forming electrodes of a plurality of dummy electrodes. However, when one dummy pixel is formed by connecting a plurality of dummy pixels, the area of pixel electrode is increased and hence, the liquid crystal capacitance is increased. As mentioned previously, when the liquid crystal capacitance is increased, the efficiency of lowering the pixel voltage using the pixel capacitance is deteriorated.

[0149] Accordingly, the dummy pixels are formed individually in the same manner as the pixels of the display region. However, when writing is performed for every one line in the same manner as the effective pixels, time necessary for driving a plural rows of newly provided dummy pixels is prolonged and hence, there arises a problem that time for performing writing in the effective pixels becomes short. To the contrary, in performing the display of high definition, since the fast video signals (signal having high dot clock) are inputted, the restriction on the writing time of the pixels is increased.

[0150] Accordingly, to save the writing time for several lines during the writing time of one screen, as shown in FIG. 21, with respect to the dummy pixels, timing signals for a plurality of rows are outputted from the vertical double-way shift register VSR of the vertical drive circuit **130** and are inputted to a plurality of level shifters **67** and an output circuit **69** so as to make the output circuit **69** output the scanning signals. Further, the timing signals for a plurality of rows are also outputted to the pixel electrode control circuit **135** from the double-way shift register SR in the same manner and are inputted to a plurality of level shifters **67** and the output circuit **69** so as to make the pixel electrode control circuit **135** output the pixel electrode control signals.

[0151] Next, FIG. 22 shows the constitution which is provided with pixel electrodes having notches in the vicinity of the spacers **4**. As mentioned previously, at the time of performing the rubbing treatment of the orientation film **7**, the orientation film **7** is not sufficiently rubbed due to the stepped portions attributed to the peripheral frame **11**. The smaller the pixels, there arise regions also in the vicinity of the spacers **4** where the orientation film **7** is not sufficiently rubbed. Then, in these regions where the orientation film **7** is not sufficiently rubbed, leaking of light is generated and hence, a contrast is lowered whereby the display quality is remarkably degraded. Accordingly, as shown in FIG. 22, notches **114** are formed at portions of the pixel regions **5** in the regions where the rubbing is not sufficiently performed. By providing the notches **114**, it is possible to prevent the occurrence of leaking of light so that the contrast can be enhanced.

[0152] Then, the constitution of the active element **30** formed on the drive circuit substrate **1** and the periphery thereof is explained in conjunction with FIG. 23 and FIG. 24. In FIG. 23 and FIG. 24, symbols in FIG. 23 and FIG. 24 which are equal to symbols used in FIG. 13 have the identical constitution. Here, FIG. 24 is a schematic plan view showing the periphery of the active element **30** and

FIG. 23 is a cross-sectional view taken along a line I-I in **FIG. 24**. However, it must be noted that **FIG. 23** and **FIG. 24** do not coincide with each other with respect to the distance between respective constitutions. Further, **FIG. 24** is provided for showing the positional relationship among a scanning signal line **102**, a gate electrode **36**, a video signal line **103**, a source region **35**, a drain region **34**, a second electrode **40** forming pixel capacitance, a first conductive layer **42**, and contact holes **35CH**, **34CH**, **40CH**, **42CH**. Other constitutions are omitted from **FIG. 24**.

[0153] In **FIG. 23**, numeral **1** indicates a silicon substrate which constitutes a drive circuit substrate, numeral **32** indicates a semiconductor region (a p-type well) formed in the silicon substrate **1** by ion implantation, numeral **33** indicates a channel stopper, numeral **34** indicates a drain region which is formed in the p-type well **32** and is made conductive by ion implantation, numeral **35** indicates a source region which is formed in the p-type well by ion implantation, and numeral **31** indicates a first electrode having pixel capacitance which is formed in the p-type well **32** and is made conductive by ion implantation. Here, although the active element **30** is constituted of a p-type transistor in this embodiment, the active element **30** may be formed of an n-type transistor.

[0154] Further, in these drawings, numeral **36** indicates the gate electrode, numeral **37** indicates an offset region which attenuates the intensity of electric field of an end portion of the gate electrode, numeral **38** indicates an insulation film, numeral **39** indicates a field oxide film which electrically separates between transistors, and numeral **40** indicates a second electrode which forms the pixel capacitance and forms the capacitance between the first electrode **21** formed on the silicon substrate **1** and the second electrode **40** by way of an insulation film **38**. The gate electrode **36** and the second electrode **40** are formed of a two-layered film consisting of a conductive layer which is formed on the insulation layer **38** for lowering a threshold value of the active element **30** and a conductive layer having low resistance. As the two-layered film, it is possible to use a film made of polysilicon and tungsten silicide, for example. Numeral **41** indicates a first interlayer film and numeral **42** indicates a first conductive film. The first conductive film **42** is formed of a multi-layered film including a barrier metal which prevents contact failure and a conductive film having low resistance. As the first conductive film, for example, it is possible to use the multi-layered metal film made of titanium tungsten and aluminum which is formed by sputtering.

[0155] In **FIG. 24**, numeral **102** indicates a scanning signal line. In **FIG. 24**, the scanning signal lines **102** extend in the X direction and are arranged in parallel in the Y direction. Scanning signals which turn on/off the active element **30** are supplied to the scanning signal lines **102**. The scanning signal line **102** is formed of a two-layered film in the same manner as the gate electrode. For example, a two-layered film which is formed by laminating a polysilicon and tungsten silicide can be used. Video signal lines **103** extend in the Y direction and are arranged in parallel in the X direction. Video signals which are written in the reflection electrodes **5** are supplied to the video signal lines **103**. The video signal line **103** is formed of a multi-layered metal film in the same manner as the first conductive film **42**. For example, a multi-layered metal film made of titanium tungsten and aluminum can be used.

[0156] The video signals pass the contact hole **35CH** formed in the insulation film **38** and the first interlayer film

41 and are transmitted to the drain region **35** via the first conductive film **42**. When the scanning signals are supplied to the scanning signal lines **102**, the active elements **30** are turned on and the video signals are transmitted from the semiconductor region (p-type well) **32** to the source region **34**, and then, are transmitted to the first conductive film **42** via the contact hole **34CH**. The video signals transmitted to the first conductive film **42** are transmitted to the second electrode **40** having the pixel capacitance via the contact hole **40CH**. Further, as shown in **FIG. 23**, the video signals pass the contact hole **42CH** and are transmitted to the reflection electrode **5**. The contact hole **42CH** is formed over the field oxide film **39**. Since the field oxide film **39** has a large film thickness, an upper surface of the field oxide film **39** is positioned at a high level compared to other constitutions. By forming the contact hole **42CH** over the field oxide film **39**, it is possible to provide the contact hole **42CH** at a position closer to the conductive film which constitutes an upper layer so that a length of a connection portion of the contact hole **42CH** can be shortened.

[0157] The second interlayer film **43** is insulated from the first conductive film **42** and the second conductive film **44**. The second interlayer film **43** has a two-layered structure consisting of a leveling film **43A** which embeds the surface irregularities formed by various constitutional elements and an insulation film **43B** which covers the leveling film **43A**. The leveling film **43A** is formed by applying SOG (spin on glass). The insulation film **43B** is a TEOS film which is a SiO₂ film formed by CVD using TEOS (Tetraethylorthosilicate) as a reaction gas.

[0158] After forming the second interlayer film **43**, the second interlayer film **43** is polished by CMP (Chemical Mechanical Polishing). Being polished by CMP, the second interlayer film **43** is leveled or smoothed. The first light shielding film **44** is formed on the leveled second interlayer film **42**. The first light shielding film **44** is formed of a multi-layered metal film made of tungsten and aluminum in the same manner as the first conductive film **42**.

[0159] The first light shielding film **44** covers substantially the whole surface of the drive circuit substrate **1** and an opening is merely constituted of the portion of contact hole **42CH** shown in **FIG. 23**. On the first light shielding film **44**, the third interlayer film **45** made of a TEOS film is formed. The second light shielding film **46** which is formed of a multi-layered film made of tungsten and aluminum in the same manner as the first conductive film **42** is formed on the third interlayer film **45**. The second light shielding film **46** is connected to the first conductive film **42** via the contact hole **42CH**. In the contact hole **42CH**, to establish the connection, a metal film which constitutes the first light shielding film **44** and a metal film which constitutes the second light shielding film **46** are laminated to each other.

[0160] The first light shielding film **44** and the second light shielding film **46** are formed of a conductive film. By forming the third interlayer film **45** made of an insulation film (a dielectric film) between the first light shielding film **44** and the second light shielding film **46**, by supplying the pixel potential control signal to the first light shielding film **44**, and by supplying the gray scale voltage to the second light shielding film **46**, it is possible to form the pixel capacitance by the first light shielding film **44** and the second light shielding film **46**. Further, to take the dielectric strength of the third interlayer film **45** with respect to the gray scale voltage and the increase of capacitance by decreasing the film thickness of the third interlayer film **45** into consider-

ation, the film thickness of the third interlayer film **45** is preferably 150 nm to 450 nm and, more preferably approximately 300 nm.

[0161] The connection between the second light shielding film **46** and the second conductive film **48** is established using a plug PG. The plug PG is formed by forming a throughhole in the fourth interlayer film **47** and by filling the through hole with tungsten or the like. Accordingly, compared to the contact hole **42CH** or the like, the surface irregularities of the film (reflection electrode **5**) which is formed over the plug PG is reduced and hence, it is possible to form the reflection electrode **5** using a flat film. Since the surface irregularities of the reflection electrode **5** reduces the reflectance of the liquid crystal panel **100**, conventionally, a contact hole which is served for connecting the reflection electrode **5** (second conductive film **48**) and a layer below the reflection electrode **5** is formed such that one contact hole is formed for each pixel. However, by connecting the second light shielding film **46** and the second conductive film **48** (reflection electrode **5**) using the plug PG, since the reflection electrode **5** above the plug **5** is relatively flat, it is possible to form a plurality of plugs PG for each pixel.

[0162] Then, FIG. 25 shows a state in which the transparent substrate **2** is overlapped to the drive circuit substrate **1**. On a peripheral portion of the drive circuit substrate **1**, the peripheral frame **11** is formed. The liquid crystal composition **3** is held in a space surrounded by the peripheral frame **11**, the drive circuit substrate **1** and the transparent substrate **2**. Between the overlapped drive circuit substrate **1** and the transparent substrate **2** and outside the peripheral frame **11**, a sealing material **12** is applied. By fixing the drive circuit substrate **1** and the transparent substrate **2** by adhesion using the sealing material, the liquid crystal panel **100** is formed. Numeral **13** indicates external connection terminals.

[0163] FIG. 26A and FIG. 26B schematically show the external connection terminals **13** in an enlarged form. FIG. 26A is a plan view and FIG. 26B is a cross-sectional view taken along a line B-B in FIG. 26A. In the drawing, numeral **13B** indicates an external connection terminal which is formed longer than other terminals for facilitating the positioning at the time of connection. Further, numeral **14** indicates a dummy pattern which is formed in the periphery of the external connection terminals **13**. In the inside of the drive circuit substrate **1**, for preventing short-circuiting at the time of connecting between external terminals **13**, the constitution other than the external connection terminal **13** is not provided. Accordingly, the pattern density is dense compared to other region in the drive circuit substrate **1**. Portions where the pattern density is coarse give rise to a drawback that a polishing quantity of interlayer film is increased compared to other regions. Accordingly, the dummy pattern is provided in the periphery of the external connection terminals **13** so that the pattern density can be made uniform and thin and uniform films can be formed by polishing.

[0164] The conductive film which constitutes the terminal is, as shown in FIG. 26B, formed by laminating the first conductive film **42**, the first light shielding film **44**, the second light shielding film **46** and the second conductive film **48** (metal film forming the reflection electrode **5**). The connection between the second light shielding film **46** and the second conductive film **48** at the connection portion is established using the plug PG in the same manner as the pixel portions. With the use of the plug PG, it is possible to form the external connection terminals **13** in a relatively flat

shape. Further, since the plug PG can be formed in close contact with them using metal such as tungsten or the like, even when conductive particles of the anisotropic conductive film penetrates the second conductive film **48** because of small thickness of the second conductive film **48**, the conductive particles are brought into contact with the plug PG such that the conductive particles are embedded into the plug PG whereby the reliability of electric connection is ensured.

[0165] Next, the manner in which the flexible printed circuit board **80** is connected is shown. The flexible printed circuit board **80** is provided for supplying signals from the outside to the liquid crystal panel **100**. As mentioned previously, the flexible printed circuit board **80** is connected to the external connection terminals **13** using an anisotropic conductive film (not shown in the drawing). Terminals of the flexible printed circuit board **80** which are positioned at both outer sides thereof are formed relatively long compared to other terminals and are connected to the counter electrodes **5** formed on the transparent substrate **2** thus forming terminals **81** for counter electrodes. That is, the flexible printed circuit board **80** is connected to both of the drive circuit substrate **1** and the transparent substrate **2**.

[0166] Conventional wiring to the counter electrodes **5** is performed by connecting a flexible printed wiring board to external connection terminals formed on the drive circuit substrate **1** and hence, the flexible printed wiring board is connected to the counter electrodes **5** via the drive circuit substrate **1**. To the transparent substrate **2** of this embodiment, the connection portion **82** with the flexible printed circuit board **80** is provided and hence, the flexible printed circuit board **80** and the counter electrodes **5** are directly connected to each other. That is, although the liquid crystal panel **100** is formed by overlapping the transparent substrate **2** and the drive circuit substrate **1**, a portion of the transparent substrate **2** is projected outside of the drive circuit substrate **1** thus forming the connection portion **82** and the counter electrodes **5** and the flexible printed circuit board **80** are connected to each other at this projected portion of the transparent substrate **2**.

[0167] FIG. 28 and FIG. 29 show the constitution of the liquid crystal display device **200**. FIG. 28 is an exploded assembly view of respective constitutional parts or components which constitute the liquid crystal display device **200**. Further, FIG. 29 is a plan view of the liquid crystal display device **200**.

[0168] As shown in FIG. 28, the liquid crystal panel **100** to which the flexible printed circuit board **80** is connected is arranged on a radiator plate **72** while sandwiching a cushion material **71** therebetween. The cushion material **71** has high thermal conductivity and fills a gap defined between the radiator plate **72** and the liquid crystal panel **100** so as to play a role of facilitating the transfer of heat of the liquid crystal panel **100** to the radiator plate **72**. Numeral **73** indicates a mold which is fixed to the radiator plate **72** by adhesion. Numeral **76** indicates a light shielding frame and displays an outer frame of the display region of the liquid crystal display device **200**.

[0169] Further, as shown in FIG. 29, the flexible printed circuit board **80** passes through between the mold **73** and the radiator plate **72** and is pulled out to the outside of the mold **73**. Numeral **75** indicates a light shielding plate and prevents light emitted from light source from being radiated to other parts which constitute the liquid crystal display device **200**.

[0170] Although the inventions made by the inventors have been specifically explained in conjunction with the

above-mentioned embodiments, it is needless to say that the present inventions are not limited to the above-mentioned embodiments and various modification can be made without departing from the gist of the present invention.

[0171] To briefly recapitulate the advantageous effects obtained by the typical inventions among inventions disclosed in this specification, they are as follows.

[0172] According to the present invention, in assembling the drive circuit into the liquid crystal display device, it is possible to use the circuit of low dielectric strength as the drive circuit and hence, an area occupied by the circuit and an area occupied by one pixel can be reduced whereby fast driving of the circuit can be realized. Further, according to the present invention, it is possible to provide the liquid crystal display device having a miniaturized constitution and high definition. Still further, according to the present invention, the rounding of waveform of the scanning signals can be reduced using a miniaturized auxiliary circuit.

What is claimed is:

1. A liquid crystal display device comprising:

a first substrate;

a second substrate;

liquid crystal composition which is sandwiched between the first substrate and the second substrate;

a plurality of pixel portions which are formed on the first substrate;

switching elements which are provided to the pixel portions;

scanning signal lines which are connected to control terminals of the switching elements;

a scanning signal circuit which supplies scanning signals to the scanning signal lines;

a video signal circuit which supplies video signals to the pixel portions;

pixel capacitances which are connected to the pixel portions;

pixel potential control signal lines which are connected to the pixel capacitances; and

a pixel potential control circuit which supplies pixel potential control signals to the pixel potential control signal lines, wherein

the scanning signal circuit is provided at one ends of the scanning signal lines and an auxiliary circuit which supplies voltages to the scanning signal lines is provided to another ends of the scanning signal lines.

2. A liquid crystal display device according to claim 1, wherein the first substrate is formed of a silicon substrate.

3. A liquid crystal display device comprising:

a first substrate;

a second substrate;

liquid crystal composition which is sandwiched between the first substrate and the second substrate;

a display region which is formed on the first substrate;

a plurality of pixel electrodes formed in the display region;

switching elements which supply video signals to the pixel electrodes;

video signal lines which supply video signals to the switching elements;

scanning signal lines which supply scanning signals for controlling the switching elements;

a video signal circuit which outputs the video signals to the video signal lines;

a scanning signal circuit which outputs the scanning signals to the scanning signal lines;

pixel capacitances which are connected to the pixel electrodes;

pixel potential control signal lines which supply pixel potential control signals to the pixel capacitances;

a pixel potential control circuit which outputs the pixel potential control signals to the pixel potential control signal lines; and

an auxiliary circuit which supplies a voltage which makes the switching elements assume the OFF state to the scanning signal lines, wherein

in the first substrate which sandwiches the display region between a first side and a second side, the scanning signal circuit is provided at the first side and the pixel potential control signal circuit is provided at the second side, and

the auxiliary circuit is provided between the pixel potential control signal circuit at the second side and the display region.

4. A liquid crystal display device according to claim 3, wherein the first substrate is formed of a silicon substrate.

5. A liquid crystal display device according to claim 3, wherein

a light shielding film is provided between the pixel electrodes and the first substrate, and the pixel potential control signal lines which supply the potential control signals to the pixel capacitances are formed of the light shielding film.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US20030222838A1	公开(公告)日	2003-12-04
申请号	US10/445987	申请日	2003-05-28
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IPC分类号	G02F1/1333 G02F1/133 G02F1/1335 G02F1/1343 G09G3/20 G09G3/36		
CPC分类号	G09G3/2011 G09G3/3614 G09G3/3655 G09G3/3677 G09G2320/0223 G09G2300/0876 G09G2310/0232 G09G2310/0283 G09G2300/0408		
优先权	2002154947 2002-05-29 JP		
外部链接	Espacenet USPTO		

摘要(译)

本发明实现了一种液晶显示装置，该液晶显示装置在其上也形成有显示部分的基板上形成小型化的低介电强度驱动电路。除了向像素提供灰度级电压的驱动电路之外，还提供降低像素电位并实现交替驱动电路。在像素电极中写入正极性信号，并且在写入之后，使用连接到像素电极的电容降低像素电极的电位。此外，在降低像素电位的电路和显示区域之间，提供了用于辅助切换的上拉电路，用于减少扫描信号的波形的舍入。

