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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2001/0006411 A1****Awane et al.**(43) **Pub. Date: Jul. 5, 2001**(54) **MANUFACTURING METHOD OF DISPLAY DEVICE**

continuation of application No. 08/604,548, filed on Feb. 21, 1996, now Pat. No. 5,982,469.

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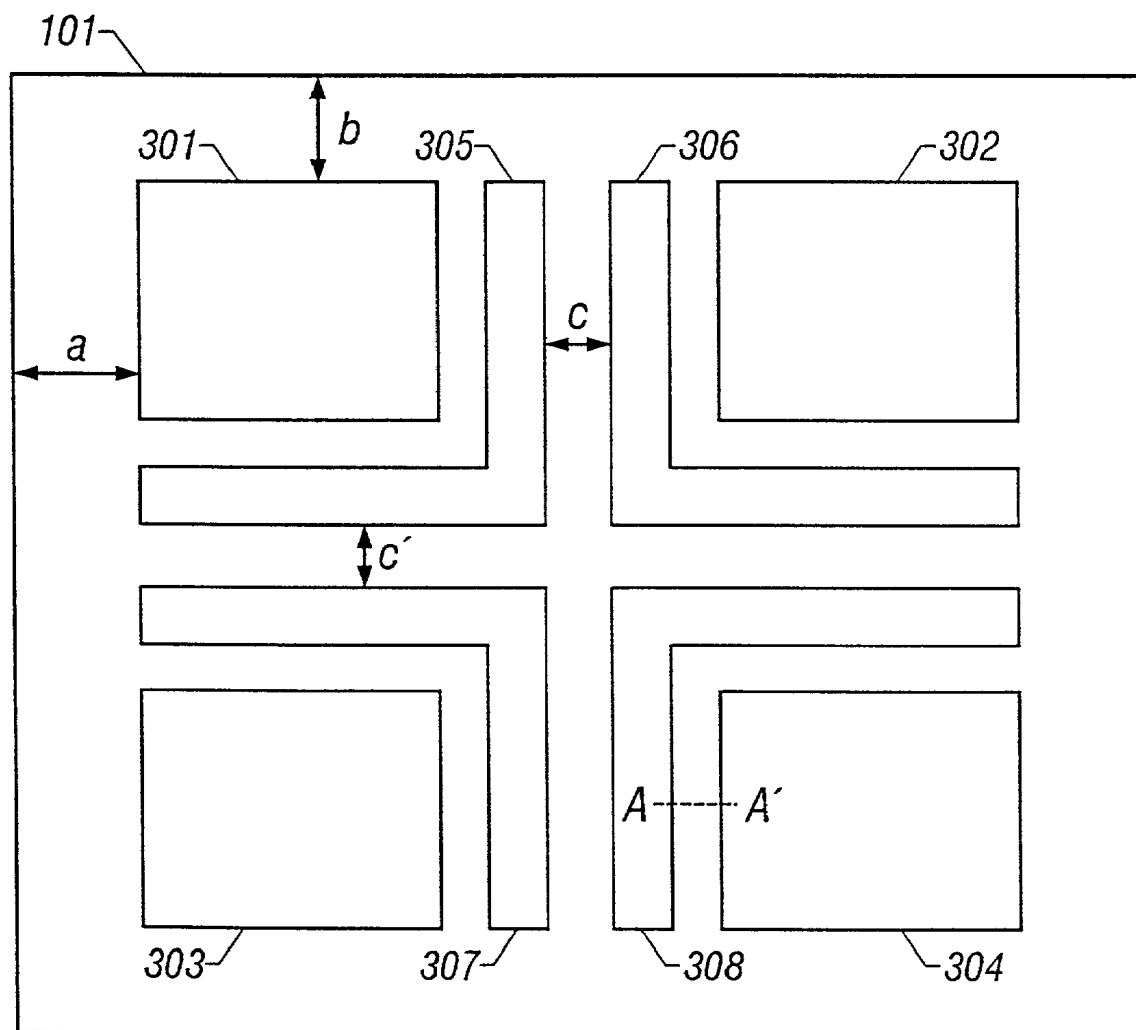
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SAN DIEGO, CA 92122 (US)**Publication Classification**(51) **Int. Cl.⁷** **G02F 1/1337**(52) **U.S. Cl.** **349/191**(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**(57) **ABSTRACT**(21) Appl. No.: **09/774,815**(22) Filed: **Jan. 30, 2001****Related U.S. Application Data**

(63) Continuation of application No. 09/425,117, filed on Oct. 20, 1999, now Pat. No. 6,201,591, which is a

In forming four liquid crystal panels on a glass substrate, layout is so made that peripheral driving circuit areas of the respective panels are opposed to each other. With this layout, the peripheral driving circuit areas, which are prone to be affected by particles, are prevented from existing in regions close to the perimeter of the glass substrate. This allows liquid crystal panels to be produced at a high yield, as well as enables efficient use of the glass substrate.



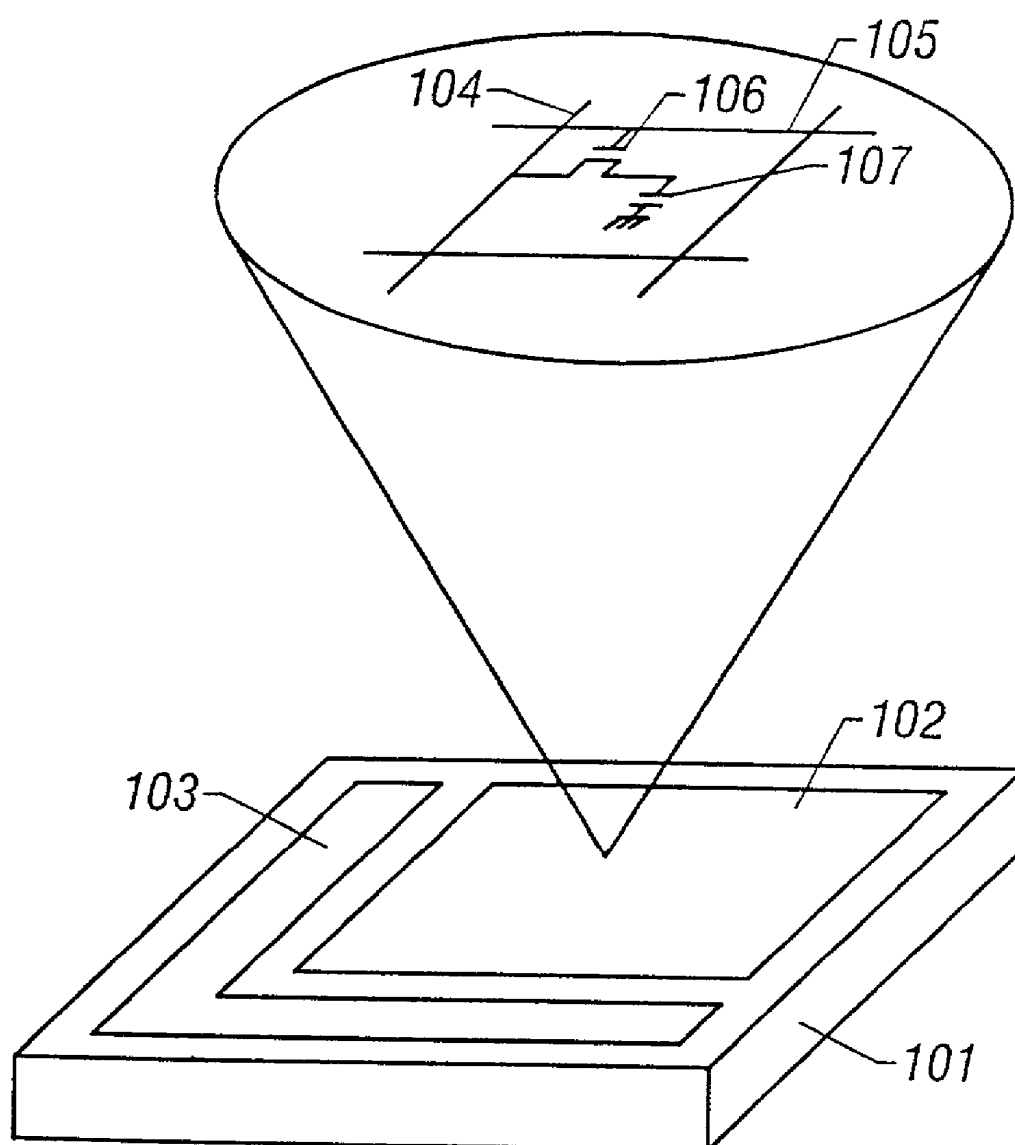


FIG. 1
(Prior Art)

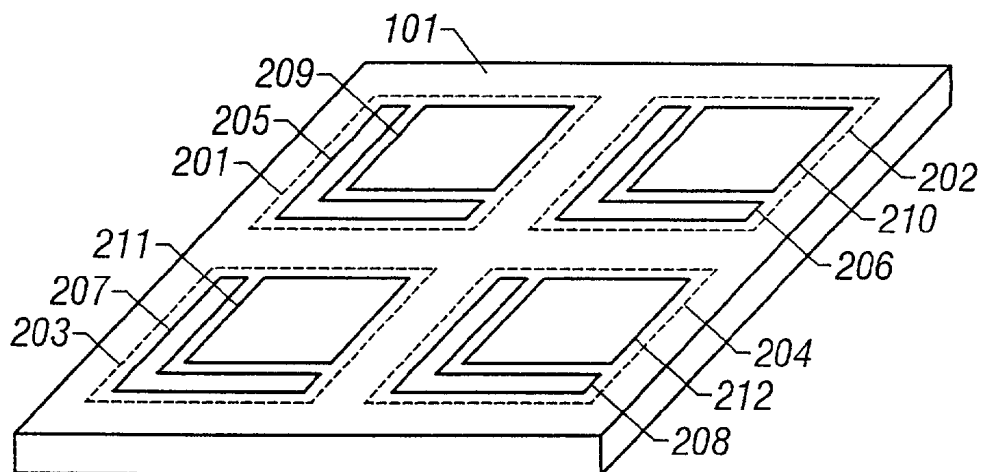


FIG. 2
(Prior Art)

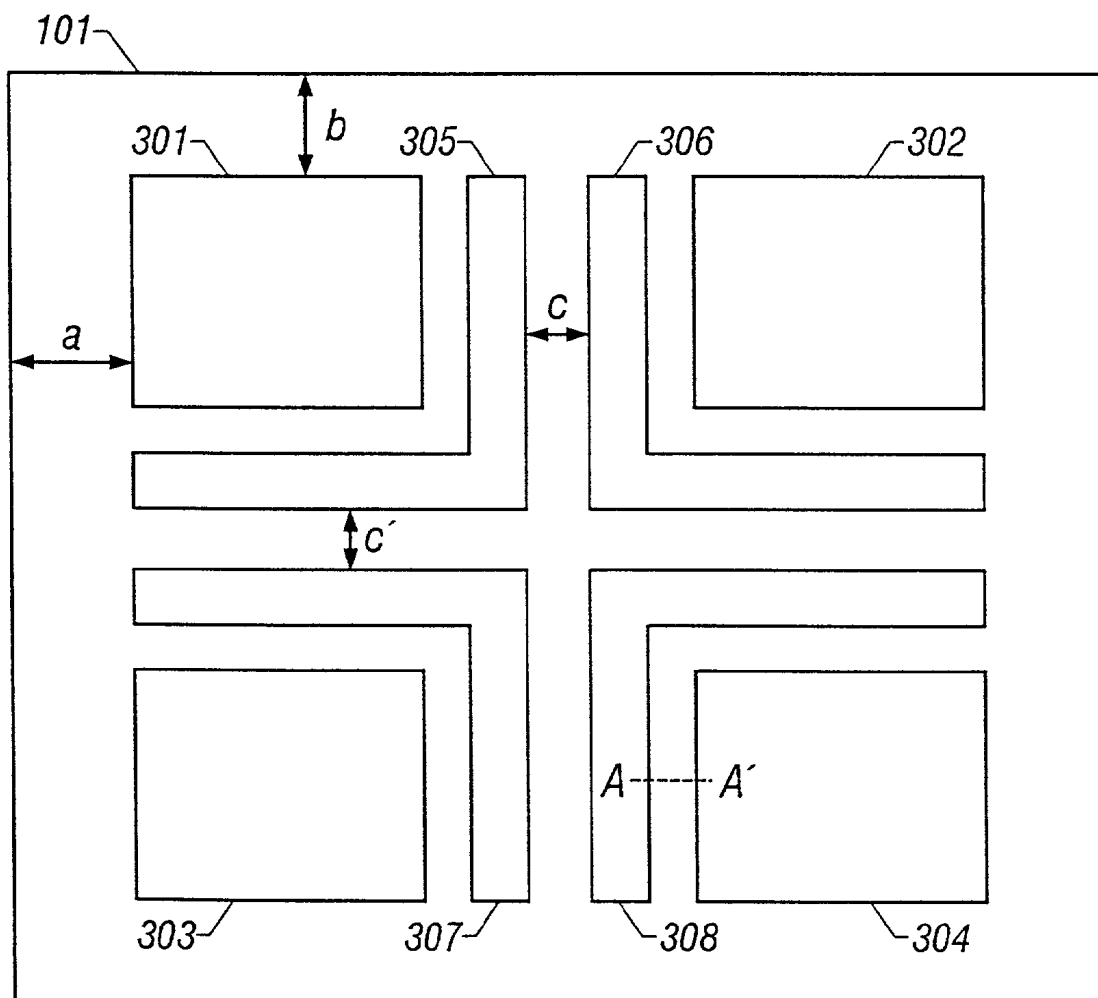


FIG. 3

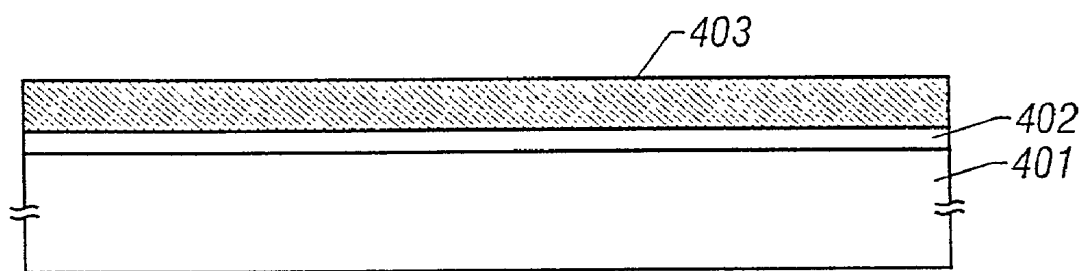


FIG. 4A

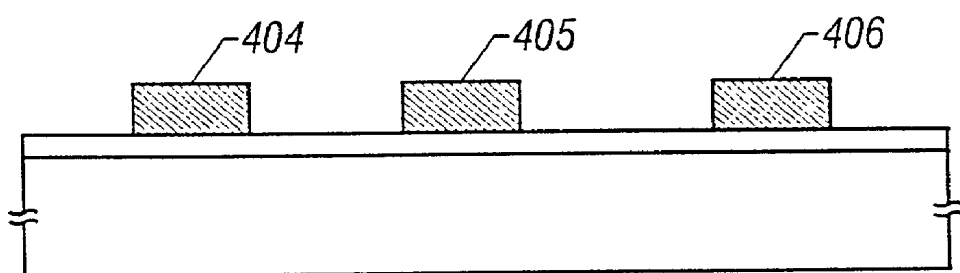


FIG. 4B

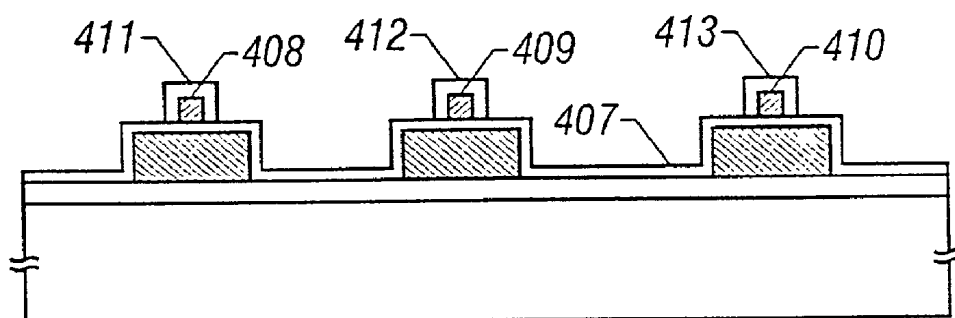


FIG. 4C

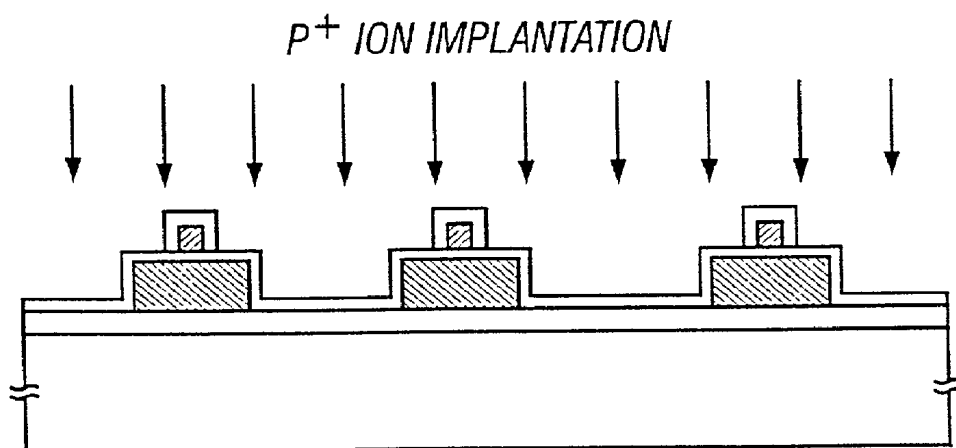


FIG. 4D

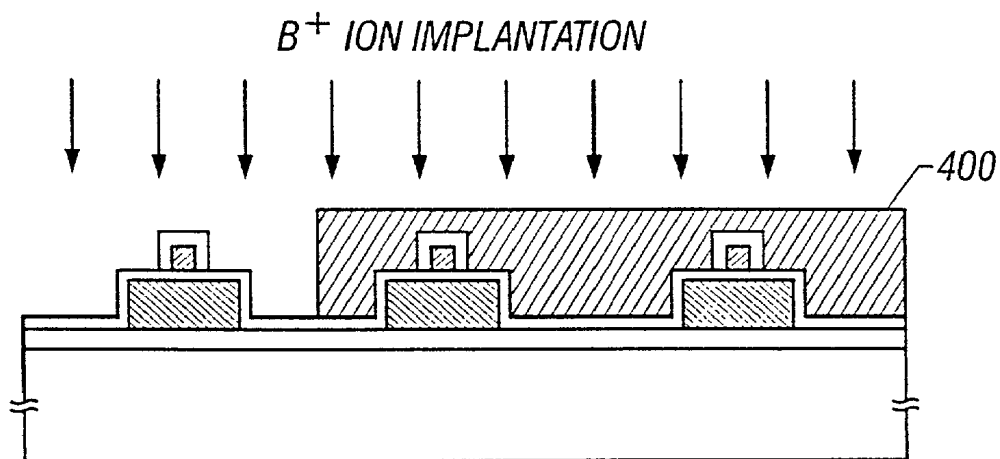


FIG. 5A

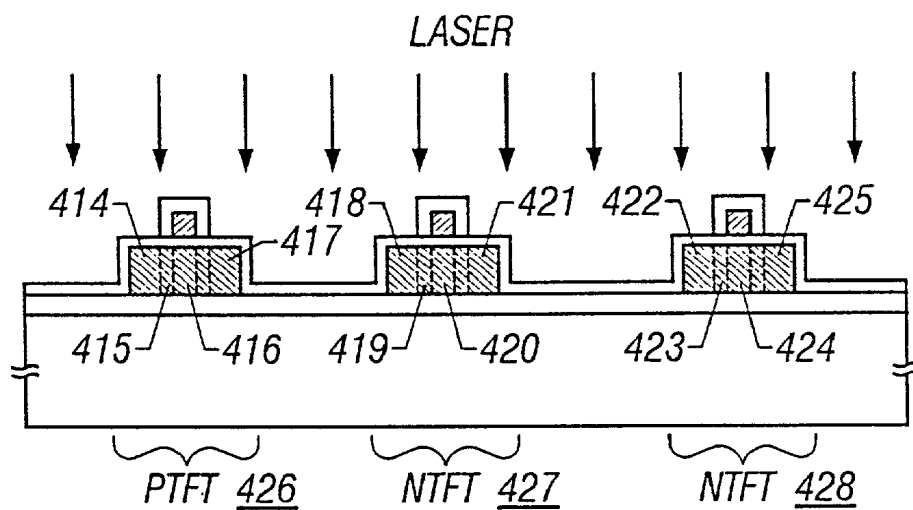


FIG. 5B

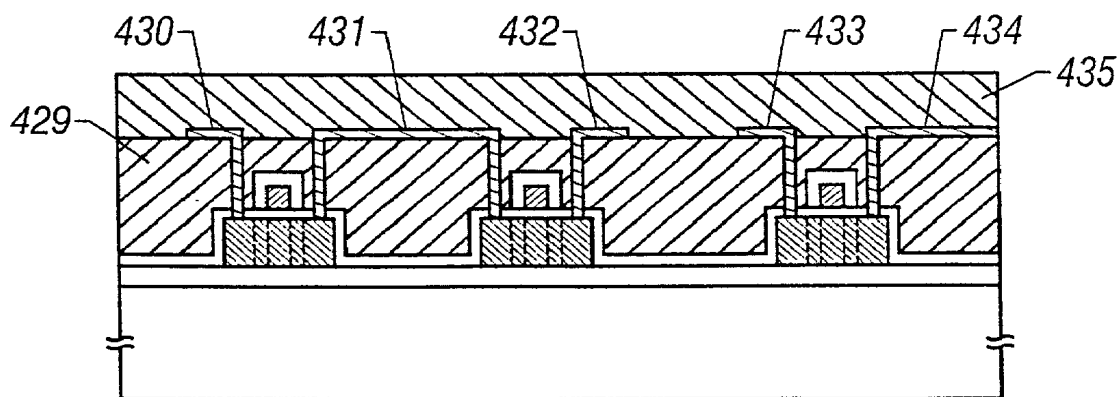


FIG. 5C

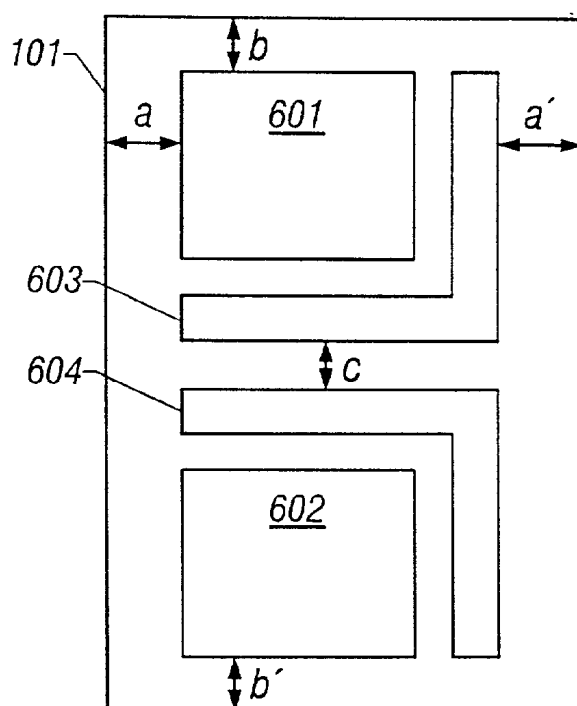


FIG. 6

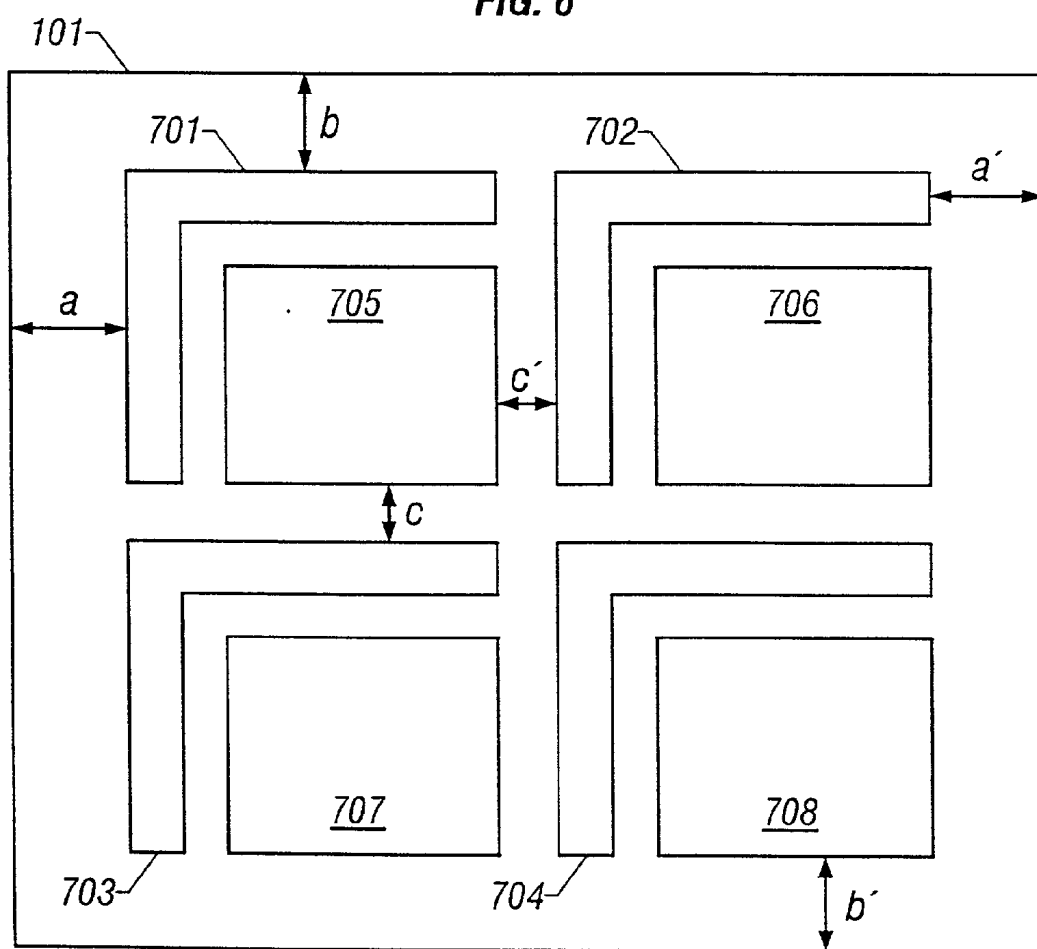


FIG. 7

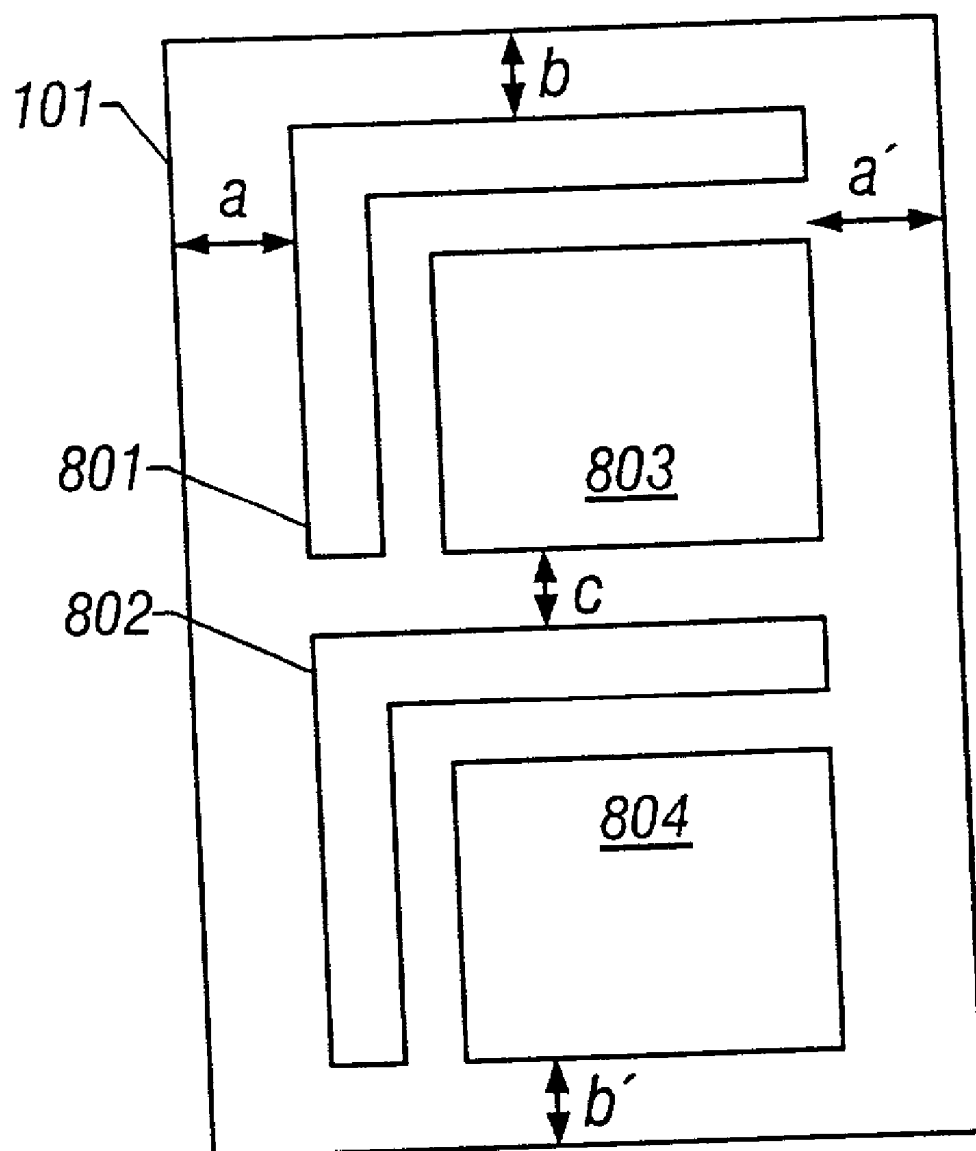
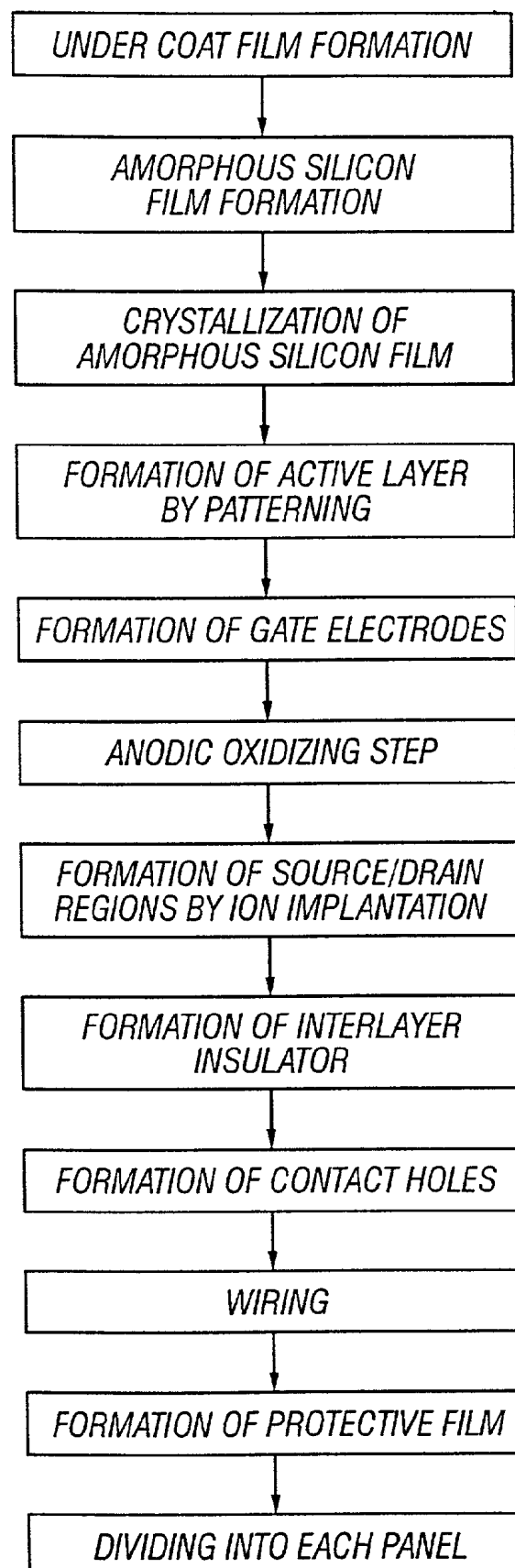


FIG. 8

**FIG. 9**

MANUFACTURING METHOD OF DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a manufacturing method of a display device having a pixel area and a peripheral driving circuit area and, more specifically, to a manufacturing method of an active matrix type liquid crystal display device.

[0003] 2. Description of the Related Art

[0004] An active matrix liquid crystal display device is conventionally known. In the active matrix liquid crystal display device, a structure is known in which a pixel area having pixels that are arranged in a matrix form and a peripheral driving circuit for driving thin-film transistors that are arranged in the pixel area are integrated on the same substrate.

[0005] FIG. 1 shows a general configuration of a panel of an active matrix liquid crystal display device in which a pixel area and a peripheral driving circuit area are integrated on a glass substrate 101. Reference numeral 102 denotes a pixel area in which pixels are arranged in a matrix of several hundred by several hundred. The fundamental configuration of the pixel area 102 is such that source lines 104 and gate lines 105 are arranged in a matrix form, thin-film transistors 106 are arranged at each intersection of the source and gate lines, and the drains of the thin-film transistors 106 are connected to electrodes (pixel electrodes) for applying an electric field to a liquid crystal 107.

[0006] Reference numeral 103 denotes a peripheral driving circuit area for driving the thin-film transistors for the respective pixels. The peripheral driving circuit area 103 is also constituted of thin-film transistors. The standardized configuration of the peripheral driving circuit includes a shift register circuit and an analog buffer circuit that allows a low-impedance current flow.

[0007] In general, plural panels of the active matrix liquid crystal display device shown in FIG. 1 are produced at the same time by forming a plurality of FIG. 1 configurations on a large glass substrate and then cutting the glass substrate, because this method can reduce the manufacturing cost from the case of producing the panel of FIG. 1 one by one.

[0008] FIG. 2 shows a general layout of active matrix liquid crystal display panels. That is, in FIG. 2, a single glass substrate 101 is allocated to four active matrix liquid crystal display panels 201 to 204. The number of panels to which a single glass substrate is allocated is not limited to four, but may be set as desired.

SUMMARY OF THE INVENTION

[0009] The layout as shown in FIG. 2 can provide an advantage that the manufacturing cost of the active matrix liquid crystal display device can be reduced. However, it has been found that if panels are actually produced with the layout as shown in FIG. 2, failures likely occur with a particular tendency.

[0010] For example, if the single glass substrate 101 is allocated to the four panels 201 to 204 in the manner shown

in FIG. 2, failures occur at a high probability in the panels 201, 203 and 204. The reason is explained as follows. It has been found that where the active matrix liquid crystal display panel of FIG. 1 is produced singly, more than 80% of circuit failures occur in the peripheral driving circuit area 103. Further, observations with an optical microscope have revealed that failures are caused mainly by particles.

[0011] The fact that failures occur in the peripheral driving circuit area 103 at a high probability attributes to two concurrent factors. First, the peripheral driving circuit area 103 has a much higher degree of integration than the pixel area 102. The second factor is as follows. In general, as exemplified in FIG. 9, a thin-film transistor manufacturing process includes many steps. For example, when a substrate is moved in a transition from one step to the next, minute particles fall on the substrate more likely in a region closer to the perimeter of the substrate.

[0012] Since the peripheral driving circuit area 103 has a higher degree of integration than the pixel area 102 as described above, a failure is caused by particles at a higher probability in the peripheral driving circuit area 103. On the other hand, where semiconductor devices are formed on a single substrate, particles (dust) are distributed on the substrate in each step (in general, semiconductor devices are formed through many steps) at a higher percentage in a region closer to the perimeter of the substrate. Therefore, when a panel is produced as shown in FIG. 1, a failure occurs at a higher probability in the peripheral driving circuit area 103. Once a failure occurs in the peripheral driving circuit area 103, no signal current flows through a gate line or a source line that is connected to a location of failure, resulting in a line defect. Even if the failure does not cause a line defect, it will cause a flicker on the screen or an unclear display.

[0013] Now, where the respective cells are produced with the layout of FIG. 2, it is seen that the peripheral driving circuit areas 205, 207 and 208, which themselves are prone to a failure due to particles, exist in regions close to the perimeter of the glass substrate 101 in which regions particles occur at a high probability. Thus, it is understood that failures occur at a high probability in the peripheral driving circuit areas 205, 207 and 208.

[0014] Based on the recognition of the foregoing problem, an object of the present invention is to provide a technique of suppressing failures in a case where a plurality of panels are produced from one substrate as shown in FIG. 2.

[0015] According to one aspect of the invention, there is provided a method for manufacturing a panel that constitutes a liquid crystal display device in which a pixel area and a peripheral driving circuit area are formed in an integral manner on a substrate having an insulating surface, wherein layout is so made that a distance between the perimeter of the substrate and the peripheral driving circuit area is longer than a distance between the perimeter of the substrate and the pixel area.

[0016] In the above method, usually a glass substrate is employed as the substrate having an insulating surface. Alternatively, a quartz substrate or a resin substrate may also be used.

[0017] The pixel area has a number of pixels that are arranged in a matrix form. Each pixel has at least one

switching thin-film transistor and, if necessary, a holding capacitor. The peripheral driving circuit area includes circuits for driving the thin-film transistors in the pixel area. The peripheral driving circuit may include thin film transistors formed on the same substrate as the switching transistors.

[0018] FIG. 7 shows a specific example of the feature "layout is so made that a distance between the perimeter of the substrate and the peripheral driving circuit area is longer than a distance between the perimeter of the substrate and the pixel area." The example of FIG. 7 is directed to a case of producing four panels from a glass substrate 101. In this case, distances a and b between the perimeter of the glass substrate 101 and a peripheral driving circuit area 701 are set larger than distances a' and b'. A similar layout may be used for a case where the number of panels produced from a single substrate is larger than four. In accordance with a preferred embodiment of the invention, when the substrate 101 is 127 mm×127 mm, the distance a' and b' from the periphery of the substrate 101 to the pixel areas should be at least 10 mm so that the minimum quality of the thin films can be guaranteed. Also, the distance a and b from the periphery of the substrate 101 to the peripheral circuit region should be at least 1.5 times larger than the distance a' and b'. Also, the distance c and c' is preferably 5 mm or smaller.

[0019] According to another aspect of the invention, there is provided a method for simultaneously manufacturing four panels that constitute respective liquid crystal display devices in each of which a pixel area and a peripheral driving circuit area are formed in an integral manner on a single substrate having an insulating surface, wherein layout is so made that the peripheral driving circuit areas of the respective panels are opposed to each other.

[0020] FIG. 3 shows a specific example of the above method, i.e., a layout for producing four panels from one glass substrate 101. In FIG. 3, layout is so made that peripheral driving circuit areas 305 to 308 are opposed to each other.

[0021] Where a and b are set larger than a' and b' as shown in FIG. 7, the rate of occurrence of failures in the peripheral driving circuit areas 701 to 703, which have a high degree of integration and are as much prone to be affected by particles, can be reduced. In addition, it becomes possible to use the substrate 101 more efficiently.

[0022] Where layout is so made that the peripheral driving circuit areas 305 to 308 are opposed to each other as shown in FIG. 3 in producing four panels from one substrate 101, occurrence of failures in the peripheral driving circuit areas 305 to 308 can be suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] FIG. 1 shows a general configuration of a panel of an active matrix liquid crystal display device incorporating peripheral driving circuits;

[0024] FIG. 2 shows a conventional layout of panels that constitute active matrix liquid crystal display devices;

[0025] FIG. 3 shows a layout of panels that constitute respective active matrix display devices according to a first embodiment of the present invention;

[0026] FIGS. 4A to 4D and FIGS. 5A to 5C are sectional views showing a manufacturing process of a panel that constitutes an active matrix liquid crystal display device according to the first embodiment;

[0027] FIG. 6 shows a layout of panels that constitute respective active matrix display devices according to a second embodiment of the invention;

[0028] FIG. 7 shows a layout of panels that constitute respective active matrix display devices according to a third embodiment of the invention;

[0029] FIG. 8 shows a layout of panels that constitute respective active matrix display devices according to a fourth embodiment of the invention; and

[0030] FIG. 9 is a flow chart generally showing the manufacturing process of FIGS. 4A to 4D and FIGS. 5A to 5C.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] Embodiment 1

[0032] FIG. 3 shows a layout of substrates which constitutes an active matrix liquid crystal display device according to this embodiment. This embodiment is directed to a case of allocating one glass substrate 101 to four panels. In FIG. 3, reference numerals 305 to 308 denote peripheral driving circuit areas and 301 to 304 denote pixel areas.

[0033] With the layout of FIG. 3, most part of the peripheral driving circuit areas 305 to 308, which are prone to a failure due to the existence of particles, can be located in regions of the substrate 101 where particles exist at a relatively low probability. Therefore, the occurrence of failures due to the existence of particles can be suppressed from the case of the layout as shown in FIG. 2.

[0034] In the configuration of FIG. 3, distances a and b can be set equal to each other. To efficiently using the substrate 101, it is preferred that the distances a and b be set as short as possible within a range of not reducing the yield. Since the pixel areas 301 to 304 are less likely affected by particles than the peripheral driving circuit areas 305 to 308, the distances a and b can be set relatively short. A distance c can be set shorter than the distances a and b.

[0035] It should be noted that where panels produced with the layout of FIG. 3 include two pairs of panels having an opposite positional relationship between the peripheral driving circuit area and the pixel area.

[0036] FIGS. 4A to 4D and FIGS. 5A to 5C show a manufacturing process of a panel in which a peripheral driving circuit area and a pixel area are formed on the same substrate, i.e., a panel incorporating peripheral driving circuits. FIG. 9 is a flow chart generally showing the same process.

[0037] More specifically, FIGS. 4A to 4D and FIGS. 5A to 5C show a process of simultaneously forming a thin-film transistor CMOS circuit that constitutes a peripheral driving circuit area and N-channel thin-film transistors in a pixel area. Each of FIGS. 4A to 4D and FIGS. 5A to 5C is part of a cross-section taken along line A-A' in FIG. 3.

[0038] First, a silicon oxide film **402** as an undercoat film is deposited on the surface of a glass substrate **401** by sputtering at a thickness of 3,000 Å, for instance. An amorphous silicon film **403** is deposited thereon by plasma CVD or low-pressure thermal CVD at a thickness of 500 Å, for instance. The amorphous silicon film **403** is crystallized by illuminating it with laser light. This results in a structure shown in **FIG. 4A**. Alternatively, the amorphous silicon film **403** may be crystallized by heating, or a combination of heating and laser light illumination.

[0039] By patterning the crystallized silicon film, active layers **404** and **405** to constitute a CMOS circuit of the peripheral driving circuits and an active layer **406** to constitute an N-channel thin-film transistor in the pixel area are obtained. This results in a structure shown in **FIG. 4B**.

[0040] Thereafter, a silicon oxide film **407** to serve as a gate insulating film is deposited by sputtering at a thickness of 1,000 Å, for instance. A film mainly made of aluminum and containing a very small amount of scandium is formed thereon by sputtering or electron beam evaporation at a thickness of 6,000 Å, for instance. By patterning the film just formed, gate electrodes **408** to **410** are formed.

[0041] Subsequently, the substrate is subjected to anodic oxidation in an electrolyte in which the gate electrodes **408** to **410** are used as anodes, to form oxide layers **411** to **413** having a thickness of 2,000 Å, for instance. This results in a structure shown in **FIG. 4C**. The oxide layers **41** to **413** will become a mask in a subsequent impurity ion implanting step, that is, will serve to form offset gate regions.

[0042] Thereafter, P⁺ ions (phosphorus ions) are accelerated and implanted into the active layers **404** to **406** by ion doping or plasma doping. (**FIG. 4D**)

[0043] After a prescribed area is covered with a resist mask **400**, B⁺ ions (boron ions) are accelerated and implanted by plasma doping or ion doping. (**FIG. 5A**) After the resist mask **400** is removed, laser light is applied to re-crystallize the regions where impurity ions have been implanted and to activate the introduced impurity ions. (**FIG. 5B**)

[0044] Thus, a source region **414**, a channel forming region **416**, a drain region **417**, and offset gate regions **415** of a P-channel thin-film transistor (PTFT) **426**, and a drain region **418**, a channel forming region **420**, a source region **421**, and offset gate regions **419** of an N-channel thin-film transistor (NTFT) **427** are formed. The P-channel thin-film transistor **426** and the N-channel thin-film transistor **427** constitute a CMOS circuit, which is part of peripheral driving circuits.

[0045] Further, a source region **422**, a channel forming region **424**, a drain region **425**, and offset gate regions **423** of an N-channel thin-film transistor (NTFT) **428** are formed at the same time as the above TFTs **426** and **427**.

[0046] Subsequently, a silicon oxide film as an interlayer insulating film **429** is deposited by plasma CVD at a thickness of 7,000 Å, for instance. After contact holes are formed, source wiring lines **430**, **432** and **433**, and a drain wiring line **431** are formed with aluminum or some other appropriate metal material. The drain wiring line **431** is common to the PTFT **426** and the NTFT **427**, which constitute the CMOS circuit. Further, an ITO electrode **434**

is so formed as to extend to a pixel electrode. A protection film **435** is then formed. Thus, as shown in **FIG. 5C**, the peripheral driving circuit area and the pixel area are simultaneously formed on the glass substrate **401**.

[0047] Thereafter, the respective panels are cut out to produce individual panels. Thus, the panels to constitute active matrix liquid crystal display devices can be obtained.

[0048] Embodiment 2

[0049] This embodiment is directed to a case of producing two panels from one glass substrate. **FIG. 6** shows a general layout of this embodiment. In **FIG. 6**, reference numerals **603** and **604** denote peripheral driving circuit areas and numerals **601** and **602** represent pixel areas. With the configuration of **FIG. 6**, the yield of the panel formation can be increased by making a' longer than a . That is, by making the dimension a' long, which considerably affects the rate of occurrence of failures, the reduction of the utilization ratio of a substrate **101** can be minimized as well as the yield can be made high. As for dimensions a , b and b' , a relationship $b \approx b' \approx a$ may be established in terms of minimum necessary values. Distance c can be set smaller than a , a' , b and b' . That is, a relationship $a, a', b, b' > c$ can be established.

[0050] While the relationships among a , a' , b , b' and c are given as described above, specific values of these parameters depend on a necessary yield, conditions of device manufacturing process, and the cleanliness of the process and need to be determined experimentally.

[0051] Embodiment 3

[0052] This embodiment is directed to a case of producing four panels from one glass substrate **101** with a layout shown in **FIG. 7**. In **FIG. 7**, reference numerals **701** to **704** denote peripheral driving circuit areas and numerals **705** to **708** represent pixel areas. With the layout of **FIG. 7**, the rate of occurrence of failures due to particles that fall on the peripheral driving circuit areas **701** to **704** can be suppressed by establishing a relationship $a' < a$ and $b' < b$. At the same time, by making a' and b' short, panels can be produced with efficient use of the glass substrate **101**. Relationships $a \approx b$ and $a' \approx b'$ may be established. Distances c and c' can be set shorter than a , a' , b and b' , that is, can be selected within such ranges as to satisfy a relationship $c, c' < a, a', b, b'$. Further, a relationship $c = c'$ may be established.

[0053] With the layout of **FIG. 7**, the positional relationship between the peripheral driving circuit area and the pixel area can be made identical in any of the panels. Therefore, this layout is advantageous over the layout of **FIG. 3** in being capable of producing panels having the same configuration.

[0054] Embodiment 4

[0055] This embodiment is directed to a case of producing two panels with a layout shown in **FIG. 8**. In **FIG. 8**, reference numerals **801** and **802** denote peripheral driving circuit areas and numerals **803** and **804** represent pixel areas.

[0056] With the layout of **FIG. 8**, the rate of occurrence of failures in the peripheral driving circuit areas **801** and **802** can be suppressed by establishing relationships $a > a'$ and $b > b'$, as well as a glass substrate **101** can be used efficiently. A relationship $a = b$ may be established as long as there is no particular problem. Similarly, a relationship $a' = b'$ may be

established as long as there is no particular problem. Distance c can be so set as to satisfy a condition $a, a', b, b' > c$.

[0057] As described above, in the manufacture of the active matrix liquid crystal display device, the invention can improve the yield while efficiently using glass substrates.

What is claimed is:

1. A method for manufacturing a plurality of display panels comprising steps of:

arranging a plurality of panel portions over a substrate, each panel portion having a pixel area and at least one driving circuit area, and positional relationship between the driving circuit area and the pixel area being the same in any of the panel portions over said substrate; and

dividing said substrate into said plurality of display panels,

wherein a shortest distance between one side of the substrate and a nearest driving circuit area in one of said panel portions is larger than a shortest distance between another side of the substrate and a nearest pixel area in another one of said panel portions over the substrate.

2. A method according to claim 1, wherein said one side of the substrate mostly faces driving circuit areas of said panel portions and said another side of the substrate mostly faces pixel areas of said panel portions.

3. A method according to claim 1, wherein each display panel constitutes a liquid crystal display device.

4. A method according to claim 1, wherein said pixel areas and said driving circuit areas comprise a plurality of thin film transistors formed over said substrate, each thin film transistor having an active layer comprising a crystalline semiconductor film formed over said substrate.

5. A method according to claim 1, wherein said substrate comprises a material selected from the group consisting of glass, quartz, and resin.

6. A method according to claim 1, wherein said plurality of panel portions are arranged in a matrix form over said substrate.

7. A method according to claim 1, wherein said one panel portion and said another one panel portion are diagonally arranged over said substrate.

8. A method for manufacturing a plurality of display panels comprising steps of:

arranging a plurality of panel portions over a substrate, each panel portion having a pixel area and at least one driving circuit area, and positional relationship between the driving circuit area and the pixel area being the same in any of the panel portions over said substrate; and

dividing said substrate into said plurality of display panels,

wherein a shortest distance between one side of the substrate and a driving circuit area in one panel portion located nearest to the one side of the substrate is larger than a shortest distance between another side of the substrate and a pixel area in another one panel portion located nearest to the another side of the substrate.

9. A method according to claim 8, wherein said one side of the substrate mostly faces driving circuit areas of said

panel portions and said another side of the substrate mostly faces pixel areas of said panel portions.

10. A method according to claim 8, wherein each display panel constitutes a liquid crystal display device.

11. A method according to claim 8, wherein said pixel areas and said driving circuit areas comprise a plurality of thin film transistors formed over said substrate, each thin film transistor having an active layer comprising a crystalline semiconductor film formed over said substrate.

12. A method according to claim 8, wherein said substrate comprises a material selected from the group consisting of glass, quartz, and resin.

13. A method according to claim 8, wherein said plurality of panel portions are arranged in a matrix form over said substrate.

14. A method according to claim 8, wherein said one panel portion and said another one panel portion are diagonally arranged over said substrate.

15. A method for manufacturing a plurality of display panels comprising steps of:

arranging a plurality of panel portions over a substrate, each panel portion having a pixel area and at least one driving circuit area, and positional relationship between the driving circuit area and the pixel area being the same in any of the panel portions over said substrate; and

dividing said substrate into said plurality of display panels,

wherein shortest distances between at least one driving circuit area of one panel portion and two adjacent sides of the substrate are larger than shortest distances between a pixel area of another one panel portion and another two adjacent sides of the substrate, and

wherein said two adjacent sides of the substrate are close to said one panel portion and said another two adjacent sides of the substrate are close to said another one panel portion.

16. A method according to claim 15, wherein each display panel constitutes a liquid crystal display device.

17. A method according to claim 15, wherein said pixel areas and said driving circuit areas comprise a plurality of thin film transistors formed over said substrate, each thin film transistor having an active layer comprising a crystalline semiconductor film formed over said substrate.

18. A method according to claim 15, wherein said substrate comprises a material selected from the group consisting of glass, quartz, and resin.

19. A method according to claim 15, wherein said plurality of panel portions are arranged in a matrix form over said substrate.

20. A method according to claim 15, wherein said one panel portion and said another one panel portion are diagonally arranged over said substrate.

21. A method for manufacturing a plurality of display panels comprising steps of:

arranging a plurality of panel portions over a substrate, each panel portion having a pixel area and at least one driving circuit area, and positional relationship between the driving circuit area and the pixel area being the same in any of the panel portions over said substrate; and

dividing said substrate into said plurality of display panels,

wherein shortest distances between at least one driving circuit area of one panel portion and two adjacent sides of the substrate are larger than shortest distances between a pixel area of another one panel portion and another two adjacent sides of the substrate, and

wherein said two adjacent sides of the substrate are mainly facing driving circuit areas of plural panel portions and said another two adjacent sides of the substrate are mainly facing pixel areas of plural panel portions.

22. A method according to claim 21, wherein each display panel constitutes a liquid crystal display device.

23. A method according to claim 21, wherein said pixel areas and said driving circuit areas comprise a plurality of thin film transistors formed over said substrate, each thin film transistor having an active layer comprising a crystalline semiconductor film formed over said substrate.

24. A method according to claim 21, wherein said substrate comprises a material selected from the group consisting of glass, quartz, and resin.

25. A method according to claim 21, wherein said plurality of panel portions are arranged in a matrix form over said substrate.

26. A method according to claim 21, wherein said one panel portion and said another one panel portion are diagonally arranged over said substrate.

* * * * *

专利名称(译)	显示装置的制造方法		
公开(公告)号	US20010006411A1	公开(公告)日	2001-07-05
申请号	US09/774815	申请日	2001-01-30
[标]申请(专利权)人(译)	株式会社半导体能源研究所		
申请(专利权)人(译)	半导体能源研究所有限公司.		
当前申请(专利权)人(译)	半导体能源研究所有限公司.		
[标]发明人	AWANE KATUNOBU YAMAZAKI SHUNPEI		
发明人	AWANE, KATUNOBU YAMAZAKI, SHUNPEI		
IPC分类号	G02F1/136 G02F1/13 G02F1/1333 G02F1/1362 G02F1/1368 H01L29/786 G02F1/1337		
CPC分类号	G02F1/133351 G02F1/13454		
优先权	1995056482 1995-02-21 JP		
其他公开文献	US6327015		
外部链接	Espacenet USPTO		

摘要(译)

在玻璃基板上形成四个液晶面板时，布局使得各个面板的外围驱动电路区域彼此相对。利用这种布局，可以防止易于受到颗粒影响的外围驱动电路区域存在于靠近玻璃基板周边的区域中。这允许以高产率生产液晶面板，并且能够有效地使用玻璃基板。

