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(54) LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING METHOD THEREOF

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(52) U.S. Cl. 345/98

(57) ABSTRACT

To an interface of a liquid crystal display device which converts the number of pixels of image signals inputted from an external signal source such as a host computer into image signals having the less number of pixels and fetches the image signals into drain drivers at double edges of a clock signal of low frequency, clock surveillance means comprising a clock synthesizer and a clock comparator circuit which detects the presence or the absence of the irregularity of timing of a pixel clock signal inputted from the external signal source and outputs a determination signal of normal/irregular of the pixel clock signal are mounted. When it is determined that the pixel clock signal is irregular, the supply of the image data to the drain drivers from a parallel-serial converter is stopped so that the generation of the irregularity of display in the liquid crystal display devices can be obviated.

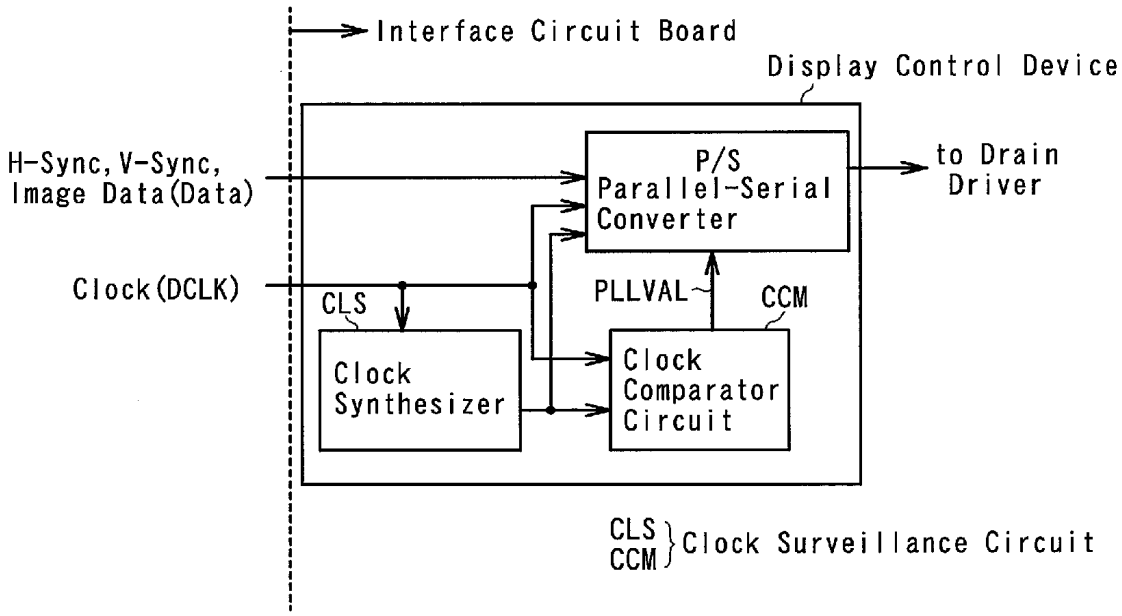


FIG. 1

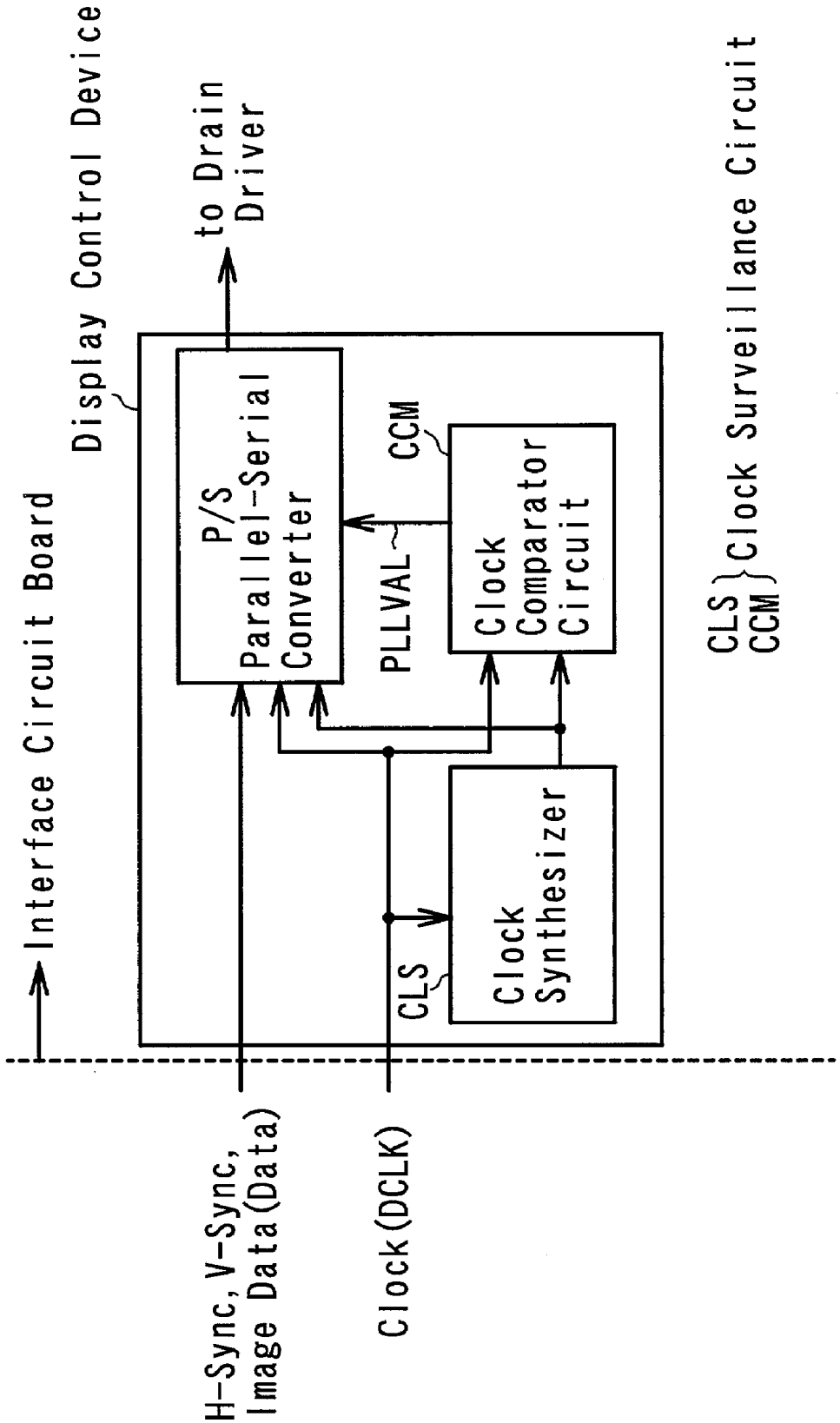

Interface Circuit Board
Display Control Device
to Drain Driver
P/S Parallel-Serial Converter
PLLVAL
CCM
Clock Comparator Circuit
CLS
Clock Synthesizer
CLS
CCM
Clock Surveillance Circuit
H-Sync, V-Sync, Image Data(Data)
Clock(DCLK)

FIG. 2

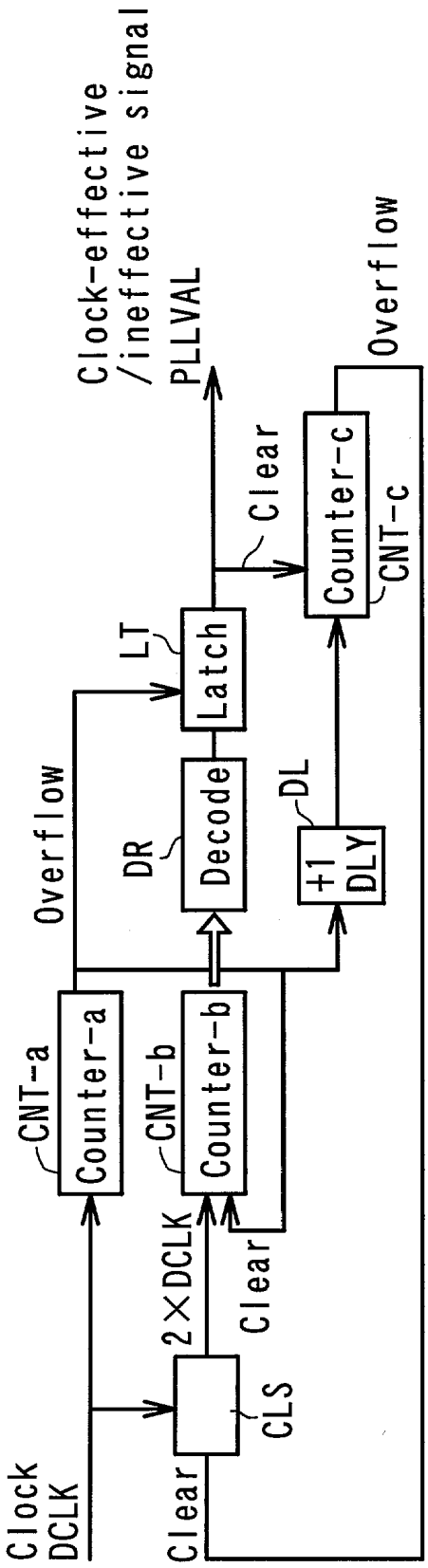

Clock
DCLK
Clear
CLS
2×DCLK
Clear
CNT-a
Counter-a
CNT-b
Counter-b
Overflow
DR
Decode
LT
Latch
Clock-effective
/ineffective signal
PLLVAL
Clear
DL
+1
DLY
Counter-c
CNT-c
Overflow

FIG. 3

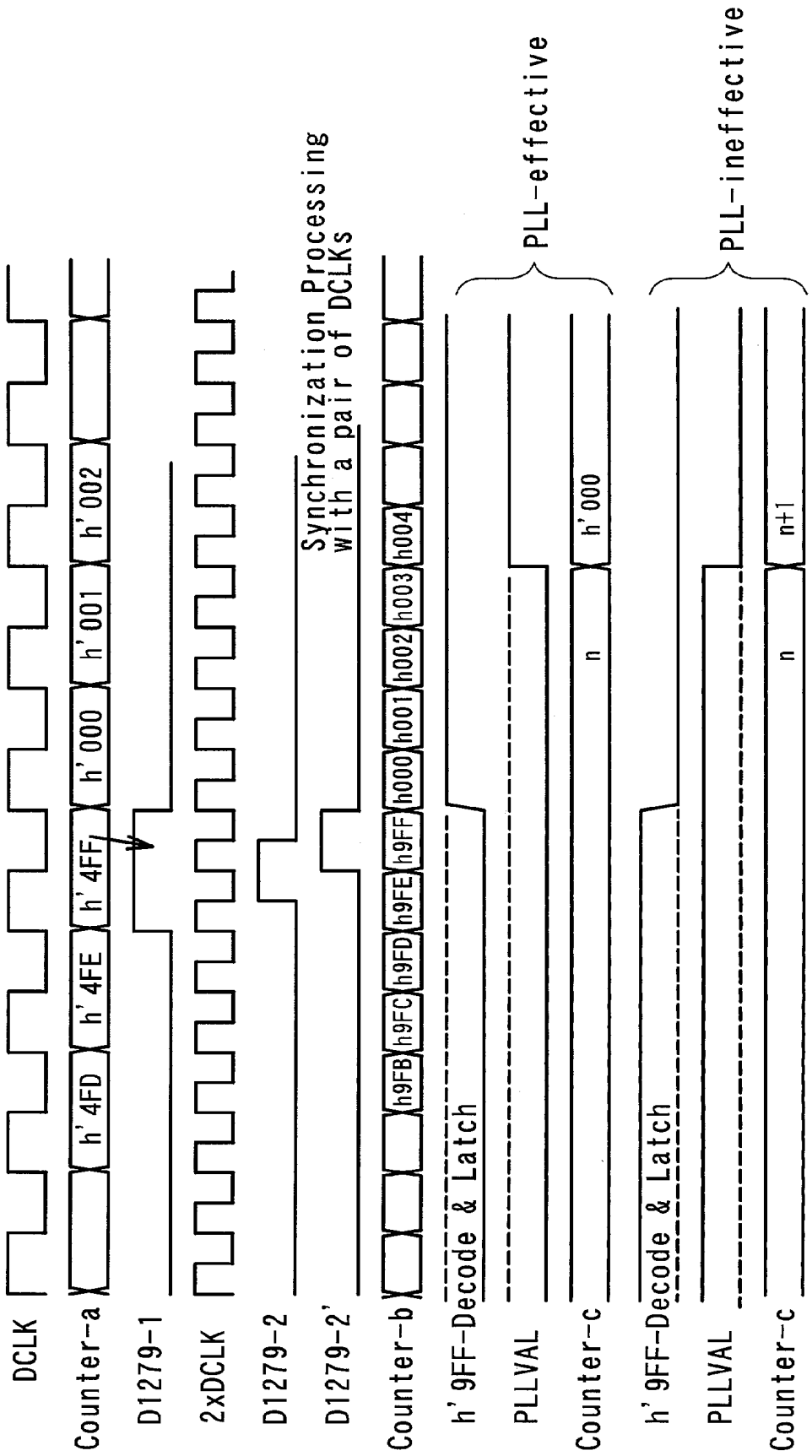

DCLK
Counter-a
h'4FD
h'4FE
h'4FF
h'000
h'001
h'002
D1279-1
2xDCLK
D1279-2
Synchronization Processing
with a pair of DCLKs
D1279-2'
Counter-b
h9FB
h9FC
h9FD
h9FE
h9FF
h000
h001
h002
h003
h004
h'9FF-Decode & Latch
PLL-effective
PLLVAL
Counter-c
n
h'000
h'9FF-Decode & Latch
PLL-ineffective
PLLVAL
Counter-c
n
n+1

FIG. 4

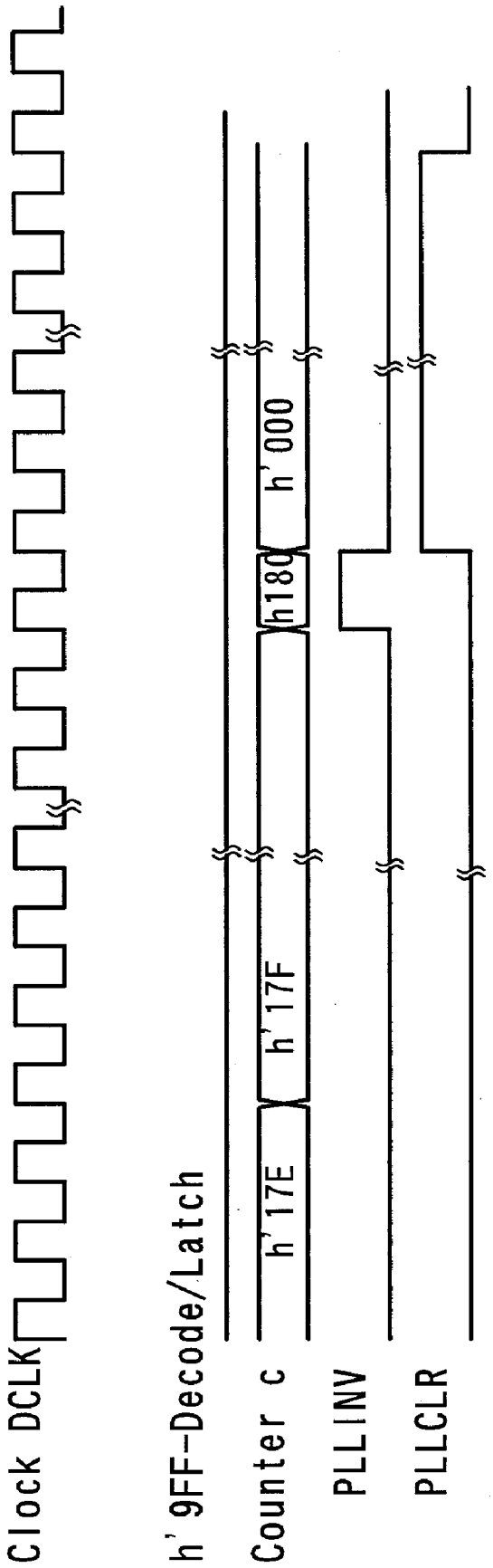

Clock DCLK
h'9FF-Decode/Latch
Counter c
h'17E
h'17F
h180
h'000
PLLINV
PLLCLR

FIG. 5

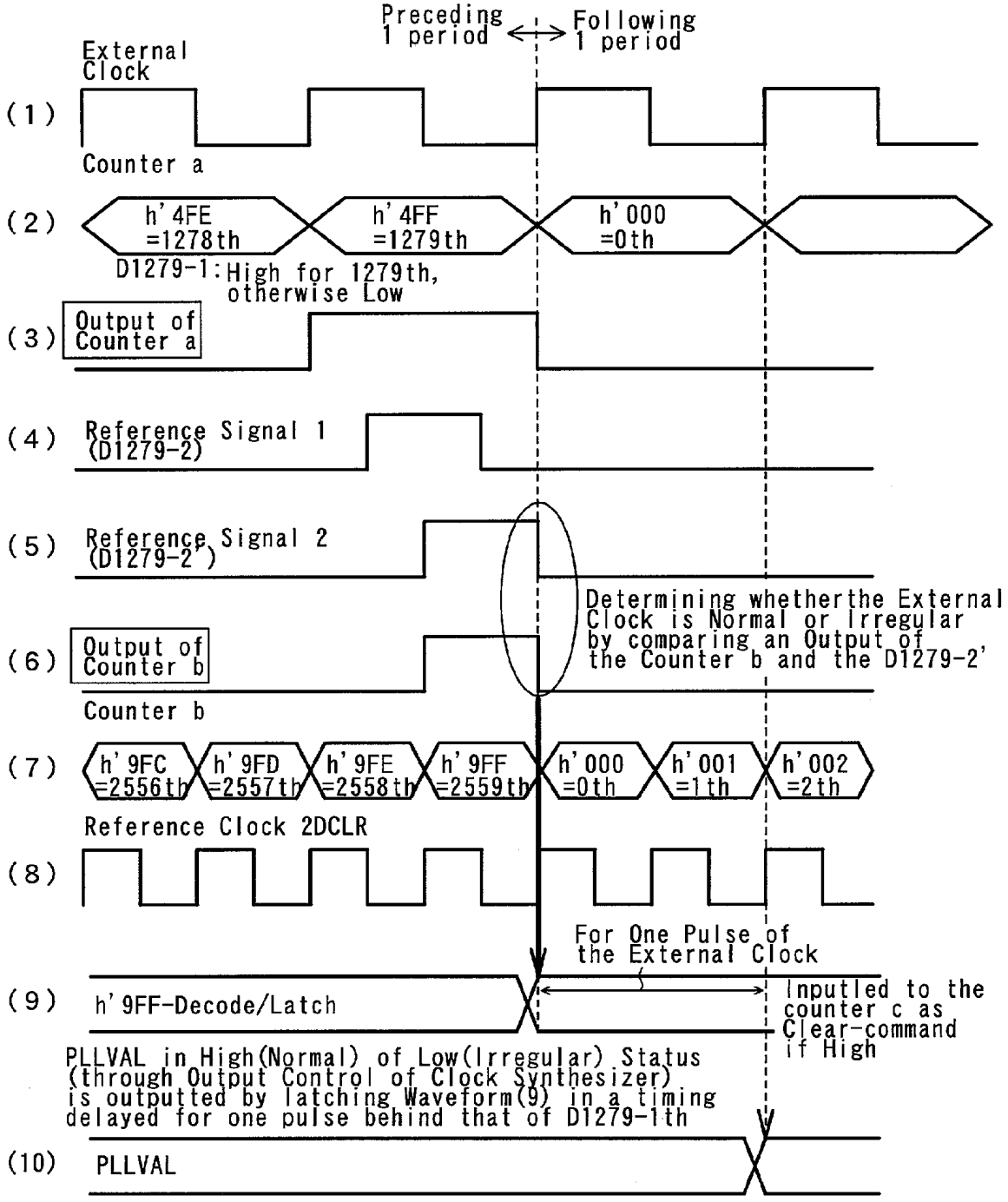

Preceding 1 period
Following 1 period
External Clock
(1)
Counter a
(2)
h'4FE =1278th
h'4FF =1279th
h'000 =0th
D1279-1: High for 1279th, otherwise Low
(3)
Output of Counter a
(4)
Reference Signal 1 (D1279-2)
(5)
Reference Signal 2 (D1279-2')
Determining whether the External Clock is Normal or Irregular by comparing an Output of the Counter b and the D1279-2'
(6)
Output of Counter b
Counter b
(7)
h'9FC =2556th
h'9FD =2557th
h'9FE =2558th
h'9FF =2559th
h'000 =0th
h'001 =1th
h'002 =2th
Reference Clock 2DCLR
(8)
For One Pulse of the External Clock
(9)
h'9FF-Decode/Latch
Inputted to the counter c as Clear-command if High
PLLVAL in High(Normal) of Low(Irregular) Status (through Output Control of Clock Synthesizer) is outputted by latching Waveform(9) in a timing delayed for one pulse behind that of D1279-1th
(10)
PLLVAL

FIG. 6

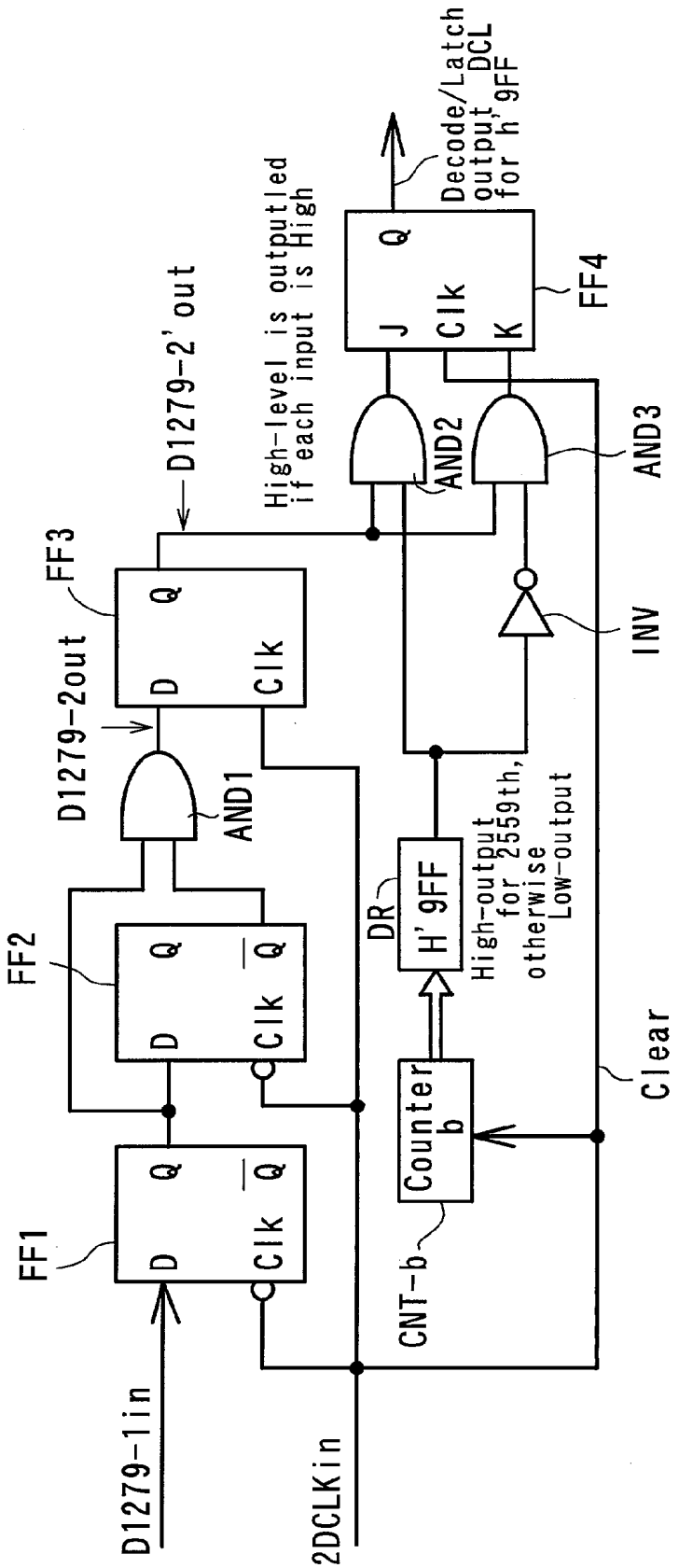

D1279-1in
2DCLKin
FF1
FF2
FF3
FF4
D
Q
Clk
J
K
AND1
AND2
AND3
INV
D1279-2out
D1279-2' out
High-level is outputted if each input is High
Decode/Latch output DCL for h' 9FF
DR
H' 9FF
High-output for 2559th, otherwise Low-output
Counter b
CNT-b
Clear

FIG. 7

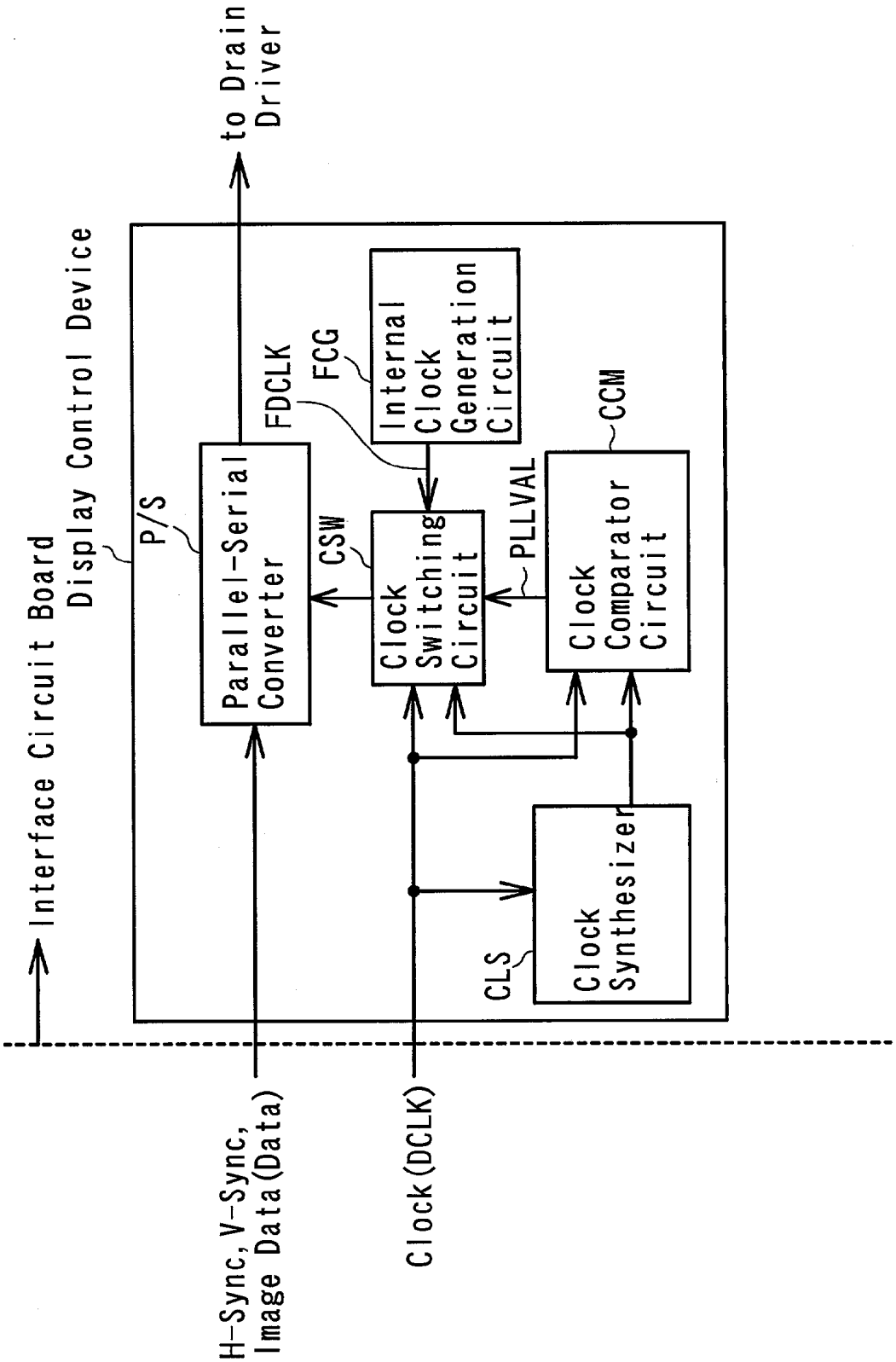

to Drain Driver
Interface Circuit Board
Display Control Device
P/S
Parallel-Serial Converter
FDCLK
FCG
Internal Clock Generation Circuit
CSW
Clock Switching Circuit
PLLVAL
CCM
Clock Comparator Circuit
CLS
Clock Synthesizer
H-Sync, V-Sync, Image Data(Data)
Clock(DCLK)

FIG. 8

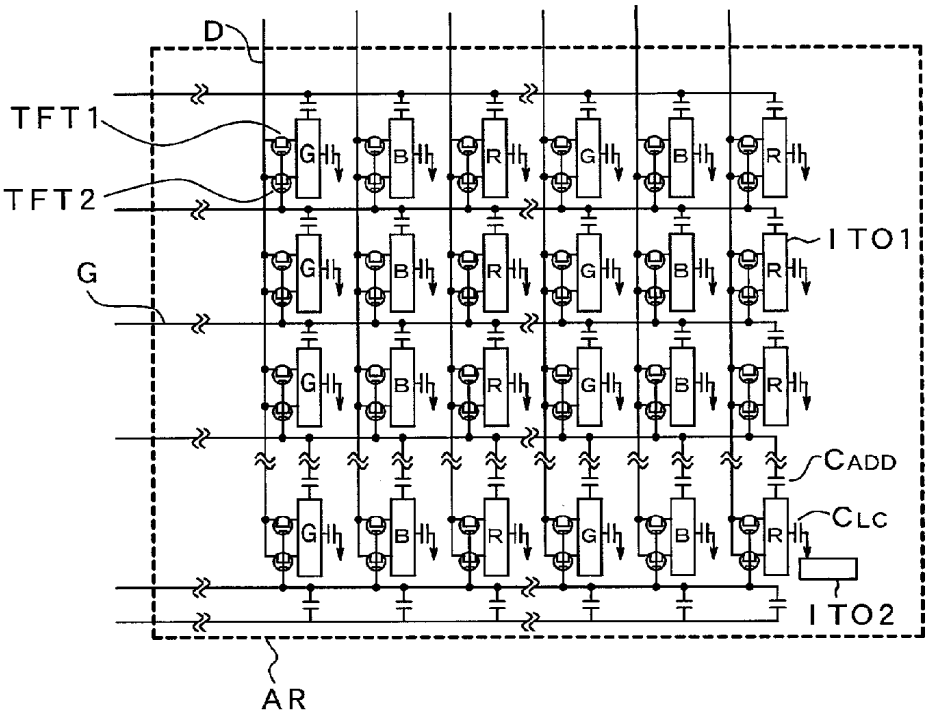

D
TFT1
TFT2
G
ITO1
CADD
CLC
ITO2
AR

FIG. 9

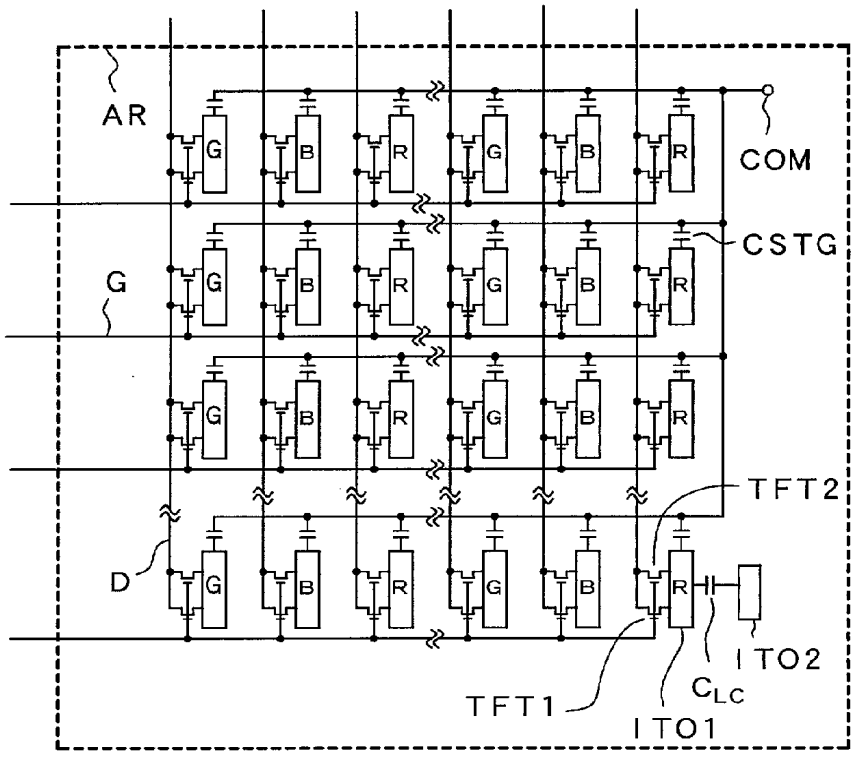

AR
COM
CSTG
G
TFT2
D
ITO2
CLC
TFT1
ITO1

FIG. 10

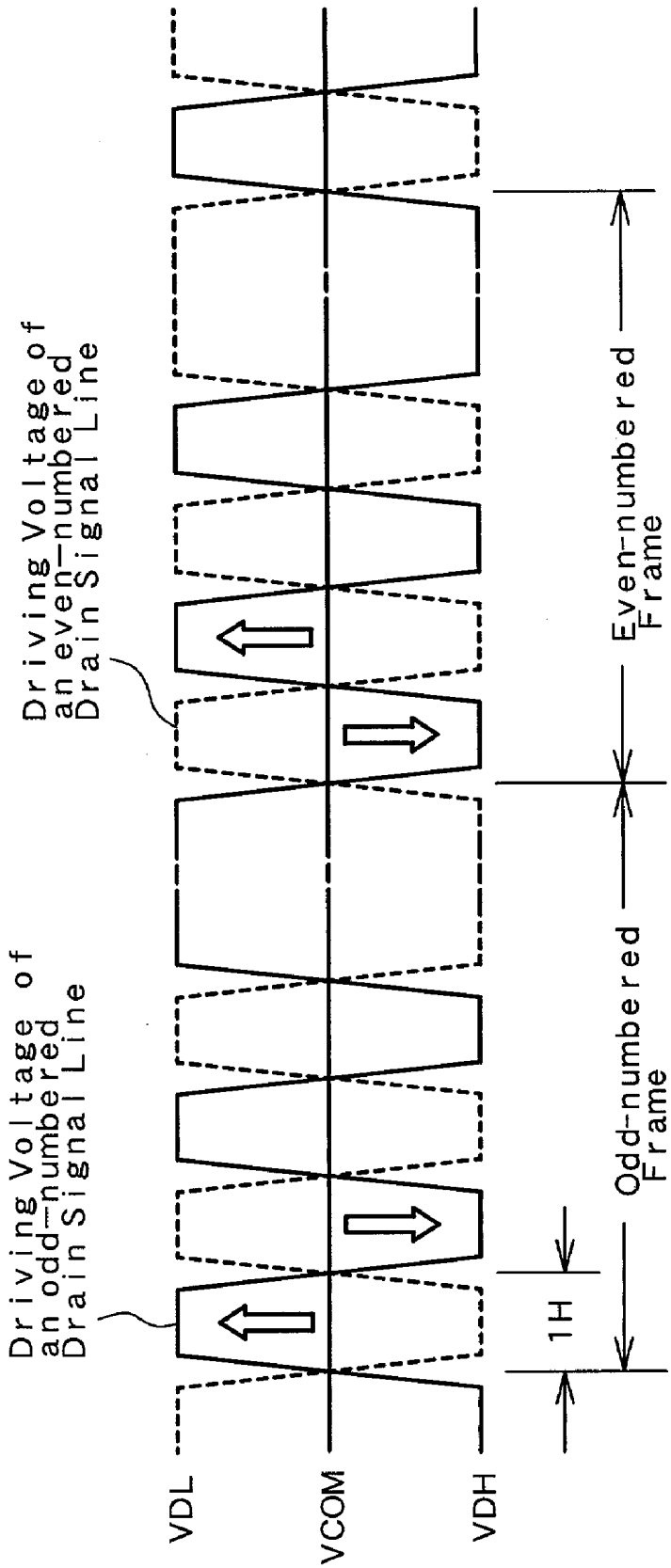

Driving Voltage of an even-numbered Drain Signal Line
Driving Voltage of an odd-numbered Drain Signal Line
Even-numbered Frame
Odd-numbered Frame
1H
VDL
VCOM
VDH

FIG. 11A

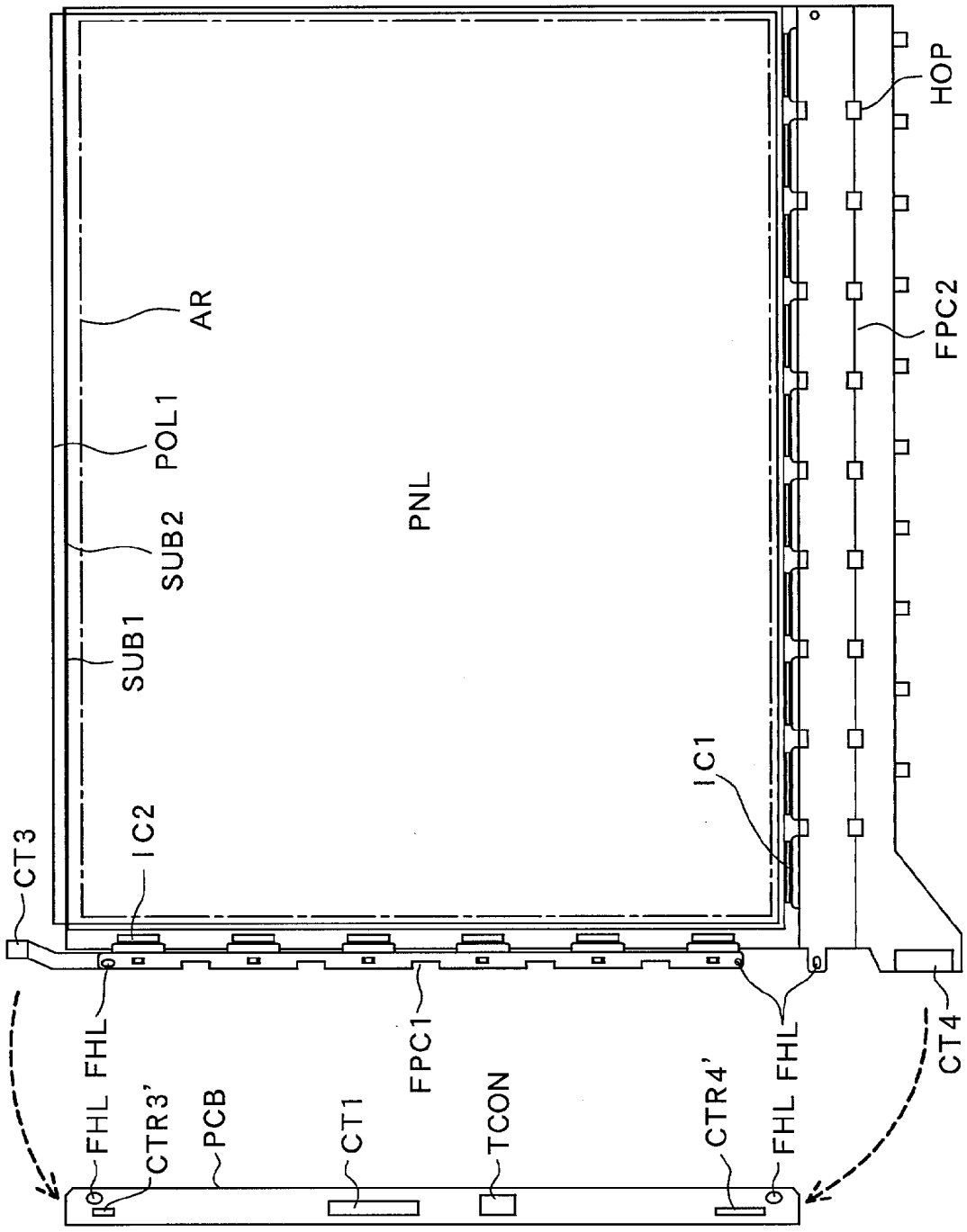


FIG. 11B

FIG. 12

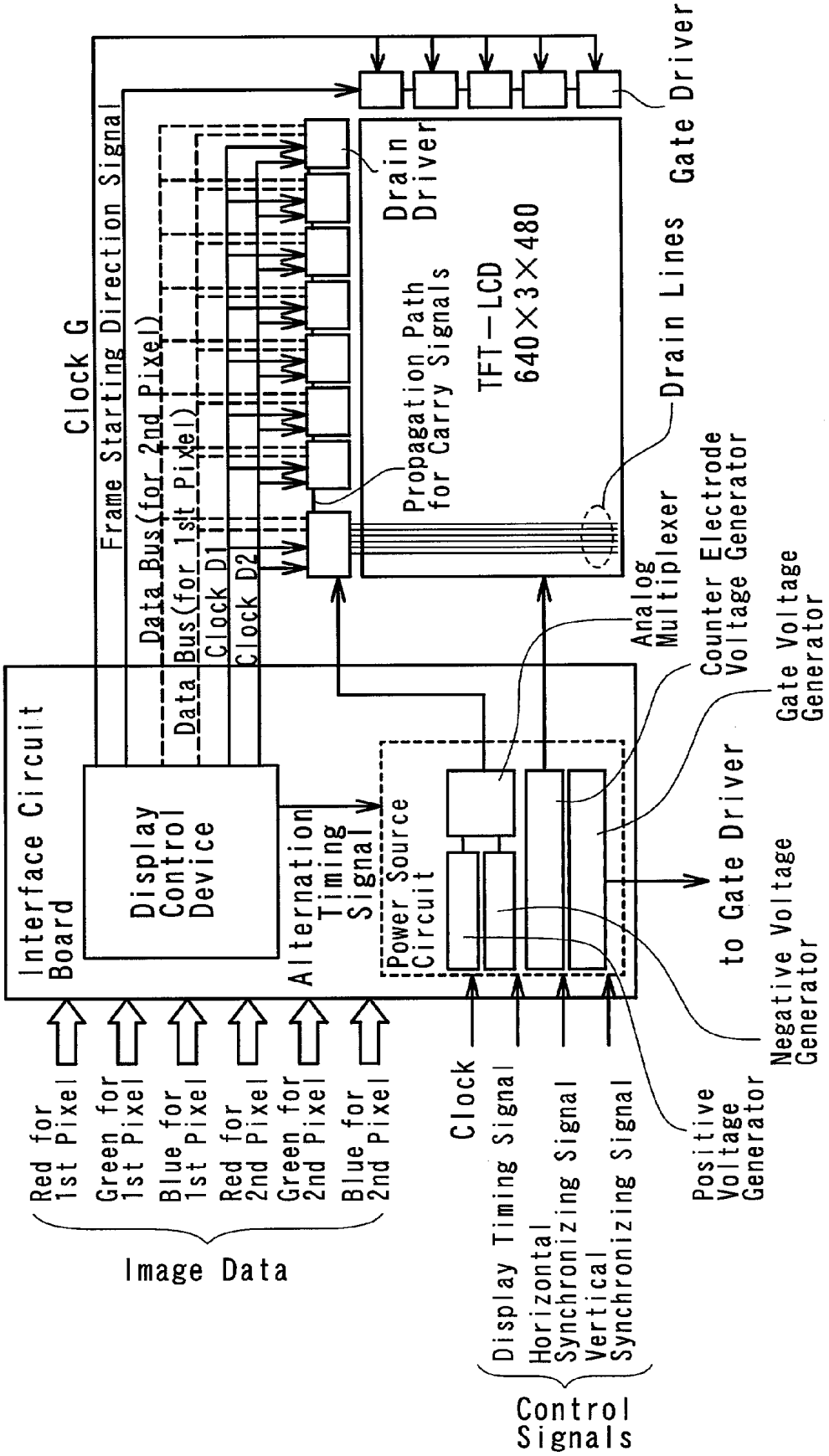

Gate Driver
Drain Lines
Drain Driver
TFT—LCD
640×3×480
Propagation Path for Carry Signals
Analog Multiplexer
Counter Electrode Voltage Generator
Gate Voltage Generator
Negative Voltage Generator
Positive Voltage Generator
to Gate Driver
Clock G
Frame Starting Direction Signal
Data Bus(for 2nd Pixel)
Data Bus(for 1st Pixel)
Clock D1
Clock D2
Interface Circuit Board
Display Control Device
Alternation Timing Signal
Power Source Circuit
Red for 1st Pixel
Green for 1st Pixel
Blue for 1st Pixel
Red for 2nd Pixel
Green for 2nd Pixel
Blue for 2nd Pixel
Image Data
Clock
Display Timing Signal
Horizontal Synchronizing Signal
Vertical Synchronizing Signal
Control Signals

FIG. 13

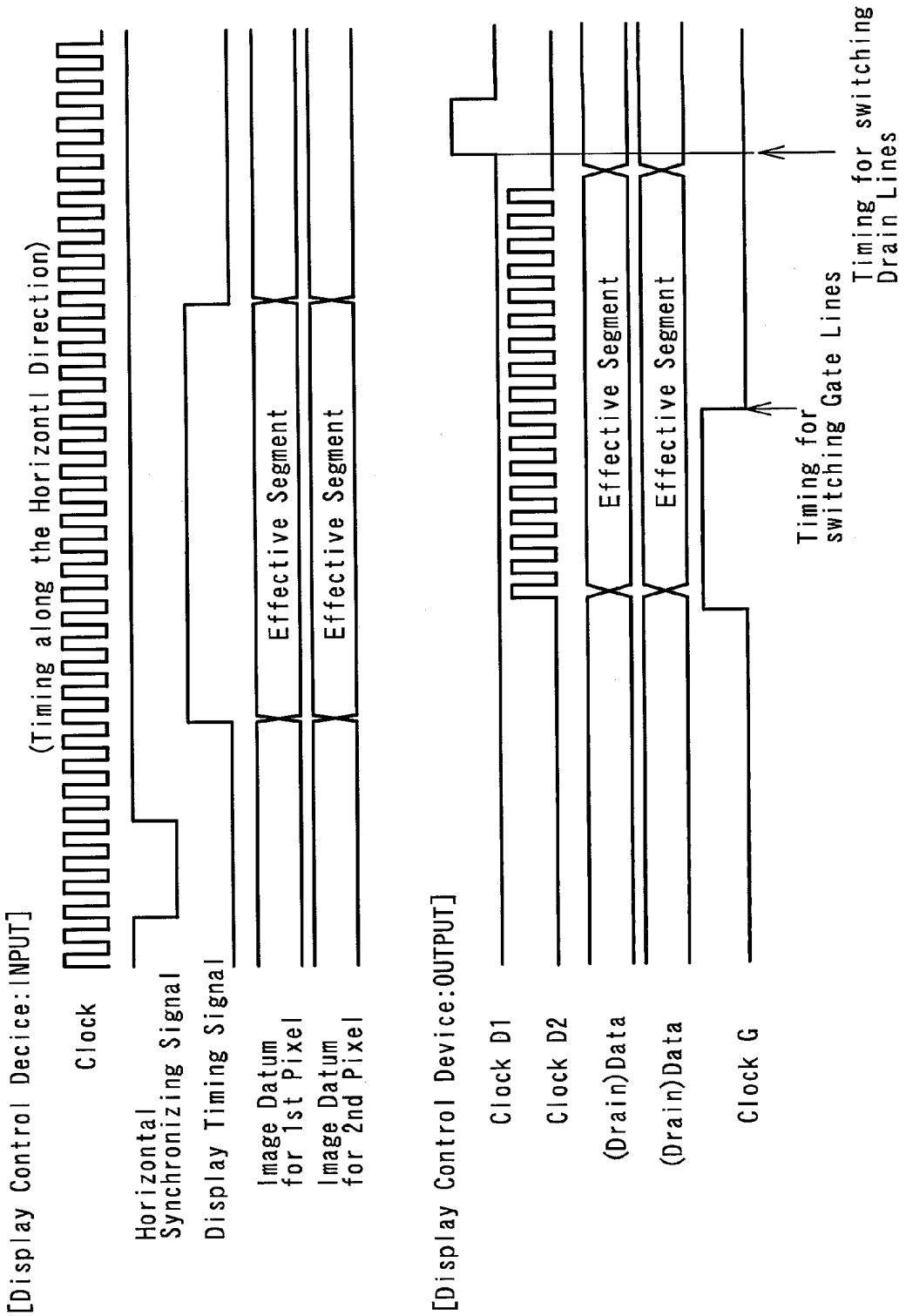

[Display Control Decice:INPUT]
(Timing along the Horizontl Direction)
Clock
Horizontal Synchronizing Signal
Display Timing Signal
Image Datum for 1st Pixel
Image Datum for 2nd Pixel
Effective Segment
Effective Segment
[Display Control Device:OUTPUT]
Clock D1
Clock D2
(Drain)Data
(Drain)Data
Clock G
Effective Segment
Effective Segment
Timing for switching Gate Lines
Timing for switching Drain Lines

FIG. 14

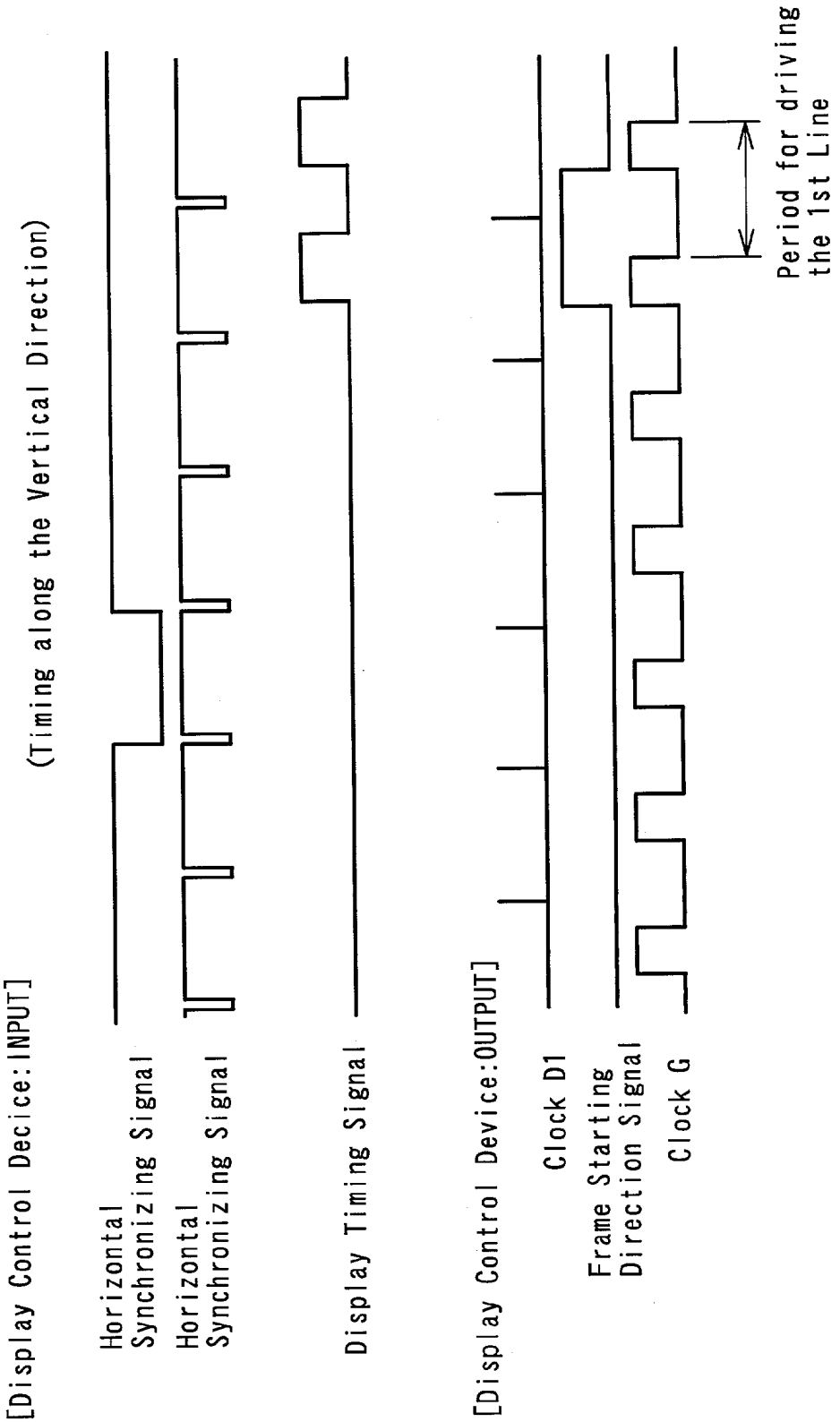

[Display Control Decice:INPUT]
(Timing along the Vertical Direction)
Horizontal Synchronizing Signal
Horizontal Synchronizing Signal
Display Timing Signal
[Display Control Device:OUTPUT]
Clock D1
Frame Starting Direction Signal
Clock G
Period for driving the 1st Line

FIG. 15 (a)

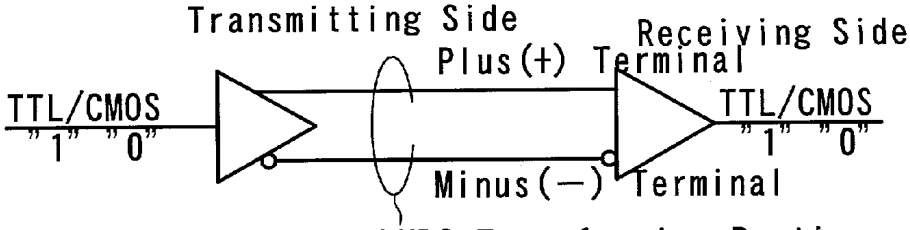


FIG. 15 (b)

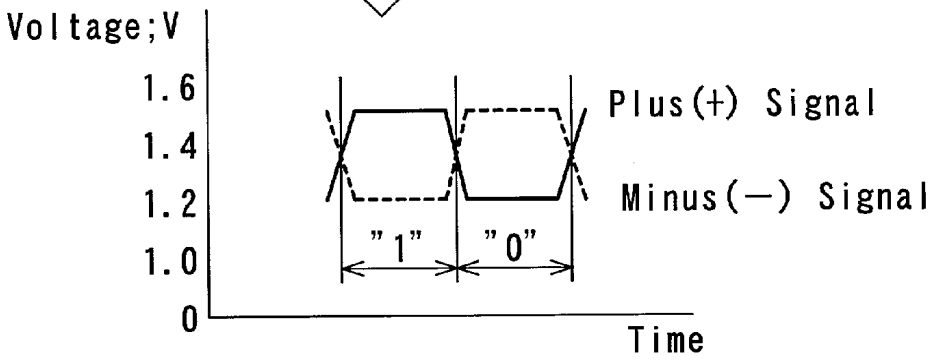


FIG. 16 (a)

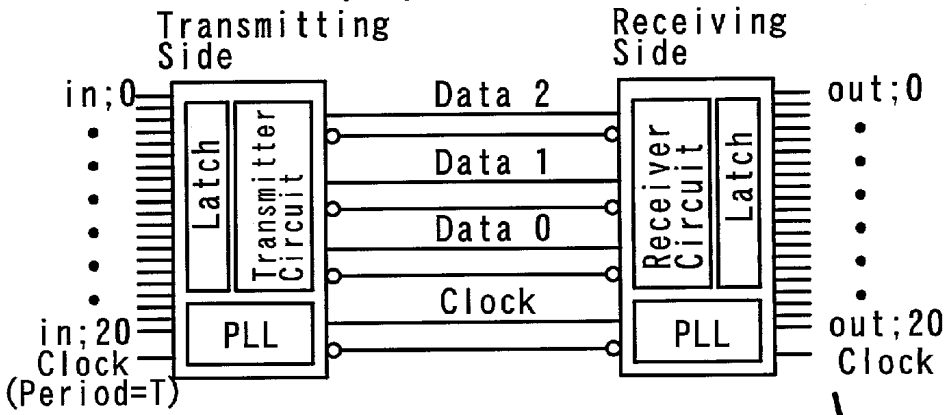


FIG. 16 (b)

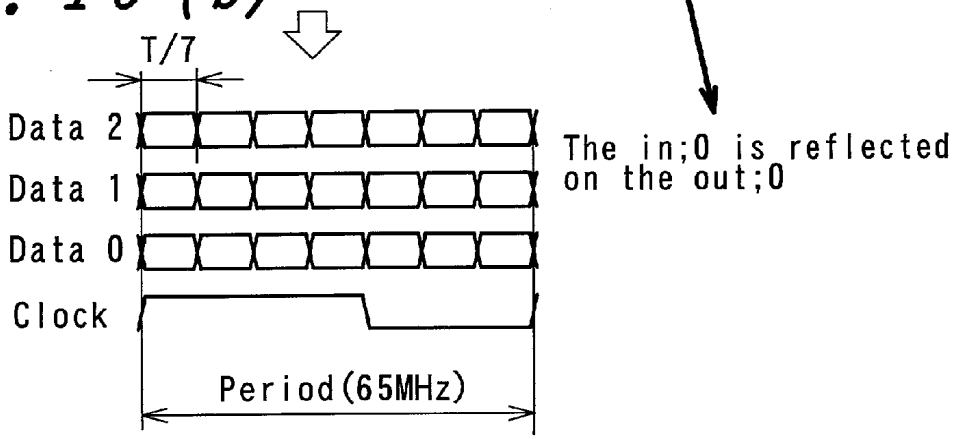


FIG. 17

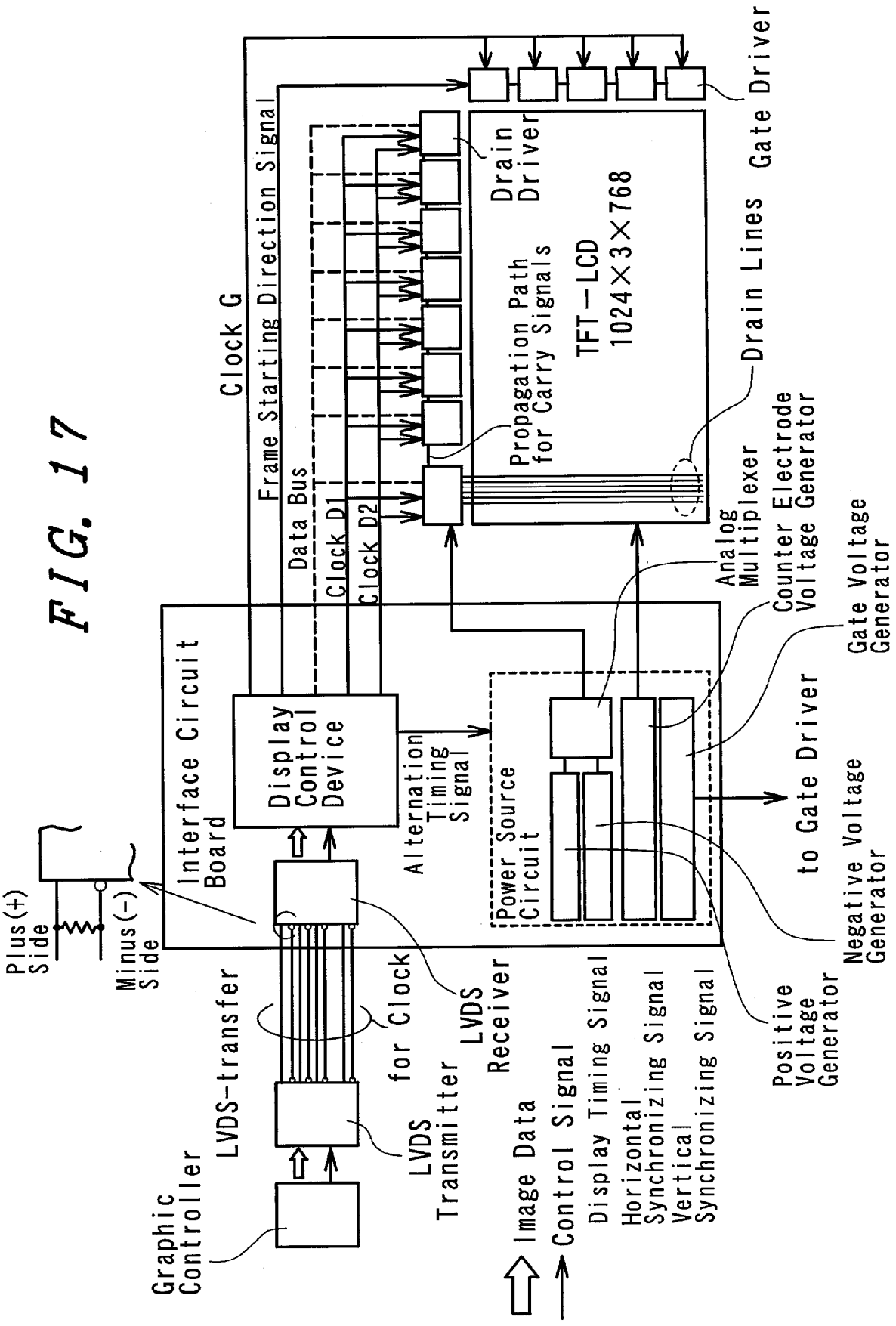

Gate Driver
Drain Lines
Drain Driver
TFT—LCD
1024×3×768
Propagation Path for Carry Signals
Clock G
Frame Starting Direction Signal
Data Bus
Clock D1
Clock D2
Analog Multiplexer
Counter Electrode Voltage Generator
Gate Voltage Generator
Interface Circuit Board
Display Control Device
Alternation Timing Signal
Power Source Circuit
to Gate Driver
Negative Voltage Generator
Positive Voltage Generator
Plus(+) Side
Minus(-) Side
LVDS-transfer for Clock
LVDS Receiver
LVDS Transmitter
Graphic Controller
Image Data
Control Signal
Display Timing Signal
Horizontal Synchronizing Signal
Vertical Synchronizing Signal

FIG. 18

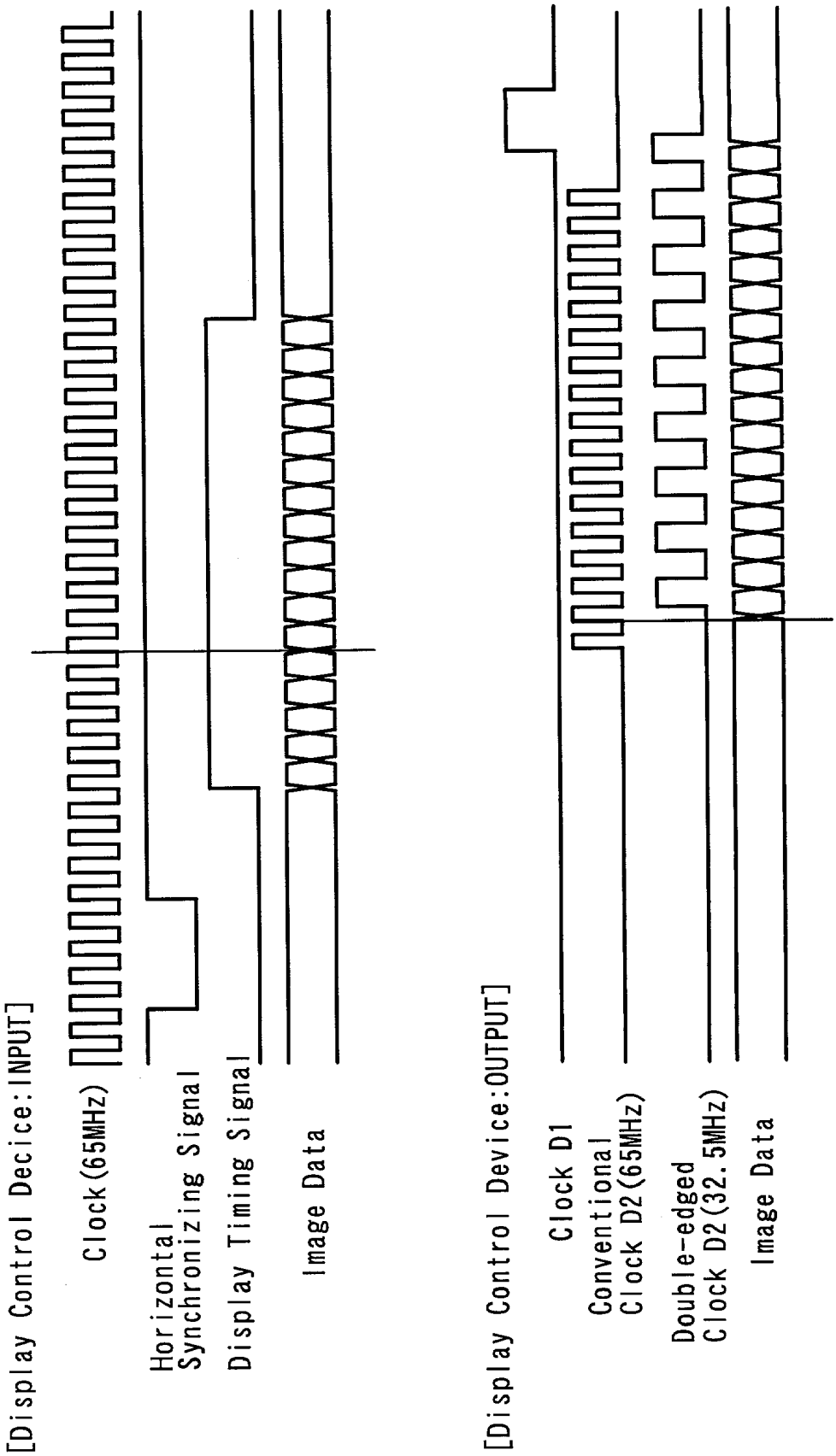

[Display Control Decice:INPUT]
Clock(65MHz)
Horizontal Synchronizing Signal
Display Timing Signal
Image Data
[Display Control Device:OUTPUT]
Clock D1
Conventional Clock D2(65MHz)
Double-edged Clock D2(32.5MHz)
Image Data

FIG. 19

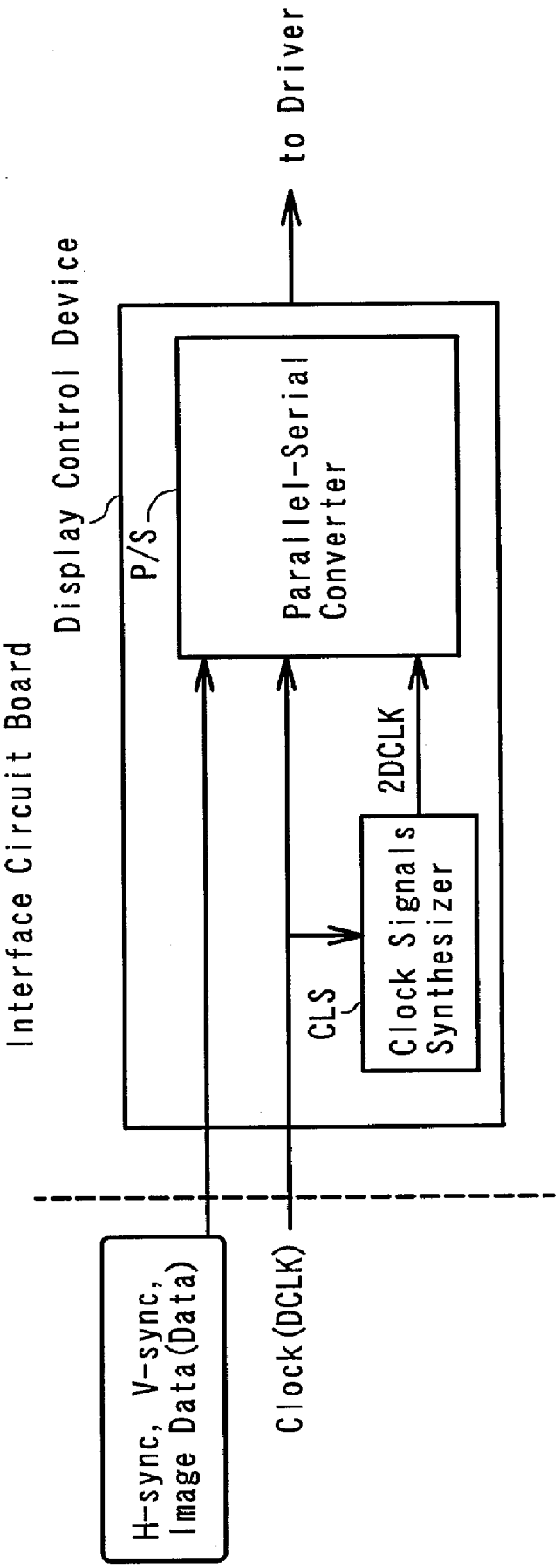

to Driver
Interface Circuit Board
Display Control Device
P/S
Parallel-Serial Converter
2DCLK
CLS
Clock Signals Synthesizer
H-sync, V-sync, Image Data(Data)
Clock(DCLK)

FIG. 20

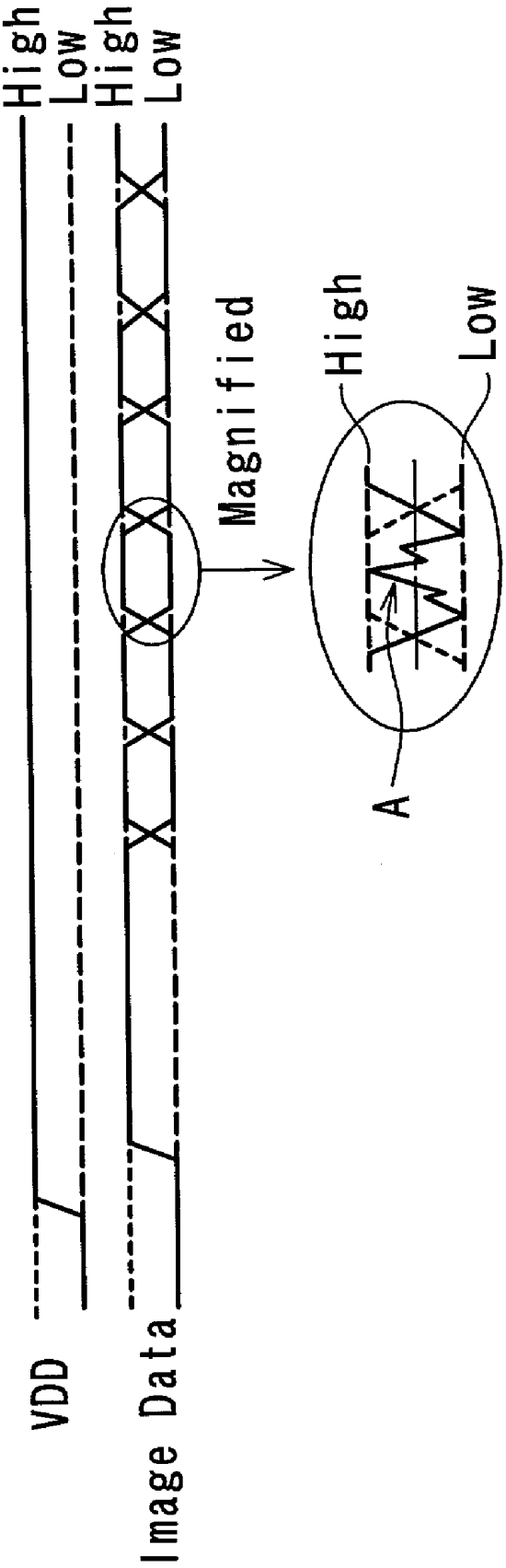
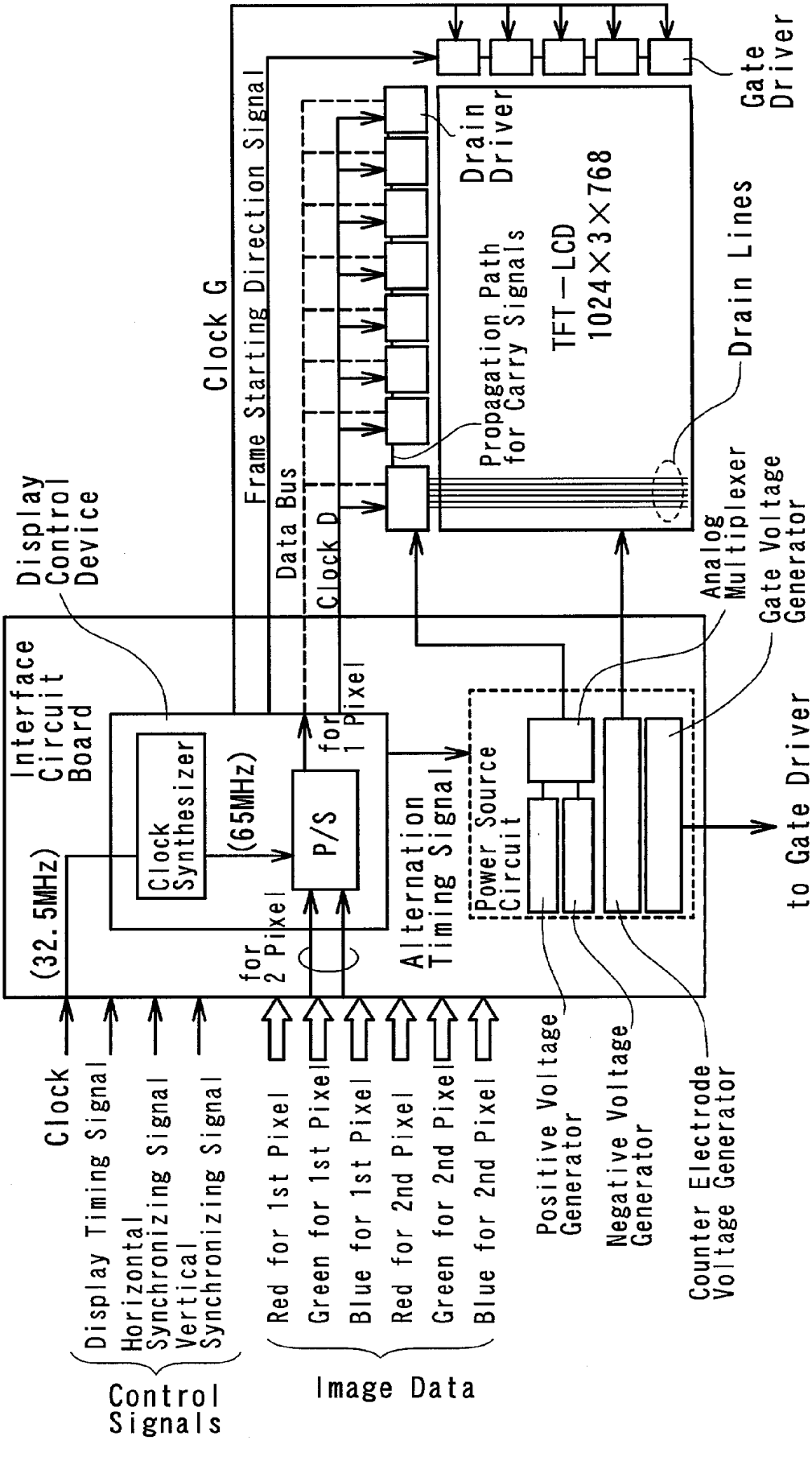


FIG. 21


Gate Driver
Drain Driver
TFT—LCD
1024×3×768
Propagation Path for Carry Signals
Drain Lines
Clock G
Frame Starting Direction Signal
Data Bus
Clock D
Display Control Device
Interface Circuit Board
Clock Synthesizer
(32.5MHz)
(65MHz)
P/S
for 1 Pixel
for 2 Pixel
Alternation Timing Signal
Power Source Circuit
Analog Multiplexer
Gate Voltage Generator
to Gate Driver
Clock
Display Timing Signal
Horizontal Synchronizing Signal
Vertical Synchronizing Signal
Red for 1st Pixel
Green for 1st Pixel
Blue for 1st Pixel
Red for 2nd Pixel
Green for 2nd Pixel
Blue for 2nd Pixel
Positive Voltage Generator
Negative Voltage Generator
Counter Electrode Voltage Generator
Control Signals
Image Data

LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING METHOD THEREOF

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display device, and more particularly to a liquid crystal display device which can prevent the disturbance of display caused by the abnormality of timing of pixel clock signals for generating image data supplied to a driving circuit for driving liquid crystal and a driving method therefor.

[0003] 2. Description of the Related Art

[0004] In an active matrix type liquid crystal display device which includes active elements such as thin film transistors (TFT) for respective pixels and performs the switching driving of these active elements, liquid crystal driving voltages (gray scale voltages) are applied to pixel electrodes through the active elements and hence, there is no cross talk between respective pixels whereby it is possible to perform a multi-gray-scale display without using a particular driving method for preventing cross talks which occurs in a simple matrix type liquid crystal display device.

[0005] **FIG. 12** is a block diagram for explaining a constitutional example of an active matrix type liquid crystal display device, while **FIG. 13** and **FIG. 14** are explanatory views of lateral-direction timing, that is, horizontal-direction timing and longitudinal-direction timing, that is, vertical-direction timing with respect to a display control shown in **FIG. 12**.

[0006] The liquid crystal display device is provided with an interface circuit board on which an interface circuit is mounted, wherein the interface circuit applies pixel data, pixel clock signals and various types of driving voltages to a liquid crystal display panel TFT-LCD upon receiving control signals including image data and pixel clock signals (the pixel clock signals being referred to as pixel clock or simply clock hereinafter) supplied from an external signal source such as a host computer or the like and other clock signals for synchronization.

[0007] The interface circuit includes a display control device and a power source circuit and outputs a data bus which transfers a first pixel, a data bus which transfers a second pixel, clocks D1, D2 for fetching pixel data into drain drivers, frame starting direction signal for driving gate drivers and gate clocks (clocks G) to the liquid crystal display panel TFT-LCD. Further, the power source circuit is constituted of a positive voltage generation circuit, a negative voltage generation circuit, a multiplexer which synthesizes a positive voltage and a negative voltage, a counter electrode voltage generation circuit and a gate voltage generation circuit.

[0008] The number of display pixels of the liquid crystal display panel TFT-LCD which constitutes the liquid crystal display device is 1024 in the lateral direction×768 in the longitudinal direction. The interface circuit board which receives display data and various types of control signals from the host computer transfers the data and the signals for 2 pixel unit to the liquid crystal display panel. That is, the interface circuit board synthesizes respective one data of red (R), green (G), blue (B) as a set and transfers the data and the symbols for 2 pixels every unit time to the liquid crystal display panel TFT-LCD through a data line which is indicated by a bold arrow in the drawing.

[0009] With respect to the clock which becomes the reference with respect to the unit time, one half of the frequency for one pixel is transmitted from the host computer (also referred to as an external signal source hereinafter) to the drain drivers of the liquid crystal display panel TFT-LCD through clock lines indicated by narrow arrows in the drawing. As a specific example, the frequency of the clock becomes 32.5 MHz which is one half of 65 MHz.

[0010] To explain the constitution of the liquid crystal display panel TFT-LCD, assuming a display screen as the reference, the drain drivers (TFT drivers) are arranged in the lateral direction and these drain drivers are connected to drain lines of thin film transistors TFT so as to supply voltages for driving liquid crystal to the thin film transistors TFT. Further the gate drivers are connected to gate lines so as to supply voltages to gates of the thin film transistors TFT for a fixed time (1 horizontal operation time, display time for 1 line).

[0011] The display control device is constituted of a semiconductor integrated circuit (LSI) which is also referred to as a TCON and receives the image data and control signals from the host computer and outputs the data and signals for 2 pixels to the drain drivers and the gate drivers based on these data and signals. Here, the data line for one pixel transmits data of 18 bits (6 bits for each R, G, B). Accordingly, by adopting 2-pixel data outputting, the total data line transmits data of 36 bits.

[0012] The reason that the number of pixel data transferred from the host computer to the display control device of the liquid crystal display device and the number of pixel data transferred from the display control device to the drain drivers of the liquid crystal display panel are respectively provided for 2 pixels is as follows. That is, when 65 MHz which is the reference clock for 1 pixel is adopted, there arises a problem that the data cannot be transferred between these devices and between the device and drain drivers. Accordingly, 2 pixel transfer is adopted.

[0013] As shown in **FIG. 13** and **FIG. 14**, pulses of 1 horizontal time period are supplied to the gate drivers based on the horizontal synchronizing signal and the display timing signal such that the voltage is supplied to the gate lines of the thin film transistors TFT for every 1 horizontal time. In accordance with every frame period, a frame starting direction signal is also given based on the vertical synchronizing signal such that the display is performed from the first line.

[0014] The positive voltage generation circuit, the negative voltage generation circuit and the multiplexer of the power source circuit alternate the voltage applied to the liquid crystal every fixed time such that the same voltage is not applied to the same liquid crystal for a long time. Here, "to alternate" means to change the voltage given to the drain drivers to the positive voltage side and the negative voltage side every fixed time using a counter electrode voltage as the reference. Here, the period of alternation is performed in accordance with every frame period.

SUMMARY OF THE INVENTION

[0015] With respect to the above-mentioned thin film transistor type liquid crystal display device which consti-

tutes the conventional technique, since the transfer of image data to the liquid crystal display panel becomes plural in number (for 2 pixels), the size of the printed circuit board which constitutes a wiring path becomes large and this constitutes one of factors which pushes up the manufacturing cost.

[0016] To cope with such a problem, a so-called LVDS (Low Voltage Differential Signaling) transferring method is adopted for transferring the image data from the host computer to the liquid crystal display device. The LVDS transferring method is a method which transfers data at a high speed by making use of the differential signals of + (plus) and − (minus) with a small amplitude.

[0017] FIGS. **15**(*a*), **15**(*b*), **16**(*a*), and **16**(*b*) are explanatory views of the LVDS transferring method. FIGS. **15**(*a*) and **15**(*b*) are conceptual views of the LVDS transferring method, wherein **FIG. 15**(*a*) is a conceptual view of the LVDS transfer method and **FIG. 15**(*b*) is an explanatory view of alternation. FIGS. **16**(*a*) and **16**(*b*) are basic constitutional views of the LVDS transferring method, wherein **FIG. 16**(*a*) is a constitutional view of a transferring lines of the LVDS and **FIG. 16**(*b*) is an explanatory view of display data and clocks which are transferred through the transferring lines of the LVDS.

[0018] To reduce the number of transfer lines at the host computer which constitute the transmitting side, the parallel data of 7 bits, for example, is converted into the serial data and this data is transferred with one pair of data per one clock (here, 65 MHz). The transferred data is restored to the parallel data of 7 bits at the liquid crystal display side. This data is inputted to the display control device.

[0019] The transfer of data from the display control device to the drain drivers of the liquid crystal display panel is configured such that the data can be transferred with the data width for 1 pixel by setting the clock D2 to a half cycle and using drain drivers having a double-edged specification.

[0020] **FIG. 17** is a block diagram for explaining a constitutional example of a liquid crystal display device which adopts an LVDS transferring method. Further, **FIG. 18** is a timing chart of an input and an output of the display control device which adopts a double-edged image data fetching method.

[0021] In **FIG. 17**, symbols and explanations identical with those shown in **FIG. 12** indicate parts having same functions. A graphic controller and an LVDS transmitting circuit are arranged at a host computer side and an LVDS receiving circuit is arranged at a liquid crystal display device side. Display data and control signals outputted from the host computer side are converted into the above-mentioned differential signals by the LVDS transmitting circuit and then are inputted to the LVDS receiving circuit mounted on an interface substrate of a liquid crystal display device.

[0022] The display data and the control signals which are restored by the LVDS receiving circuit are supplied to a liquid crystal display panel TFT-LCD through a display control device. The display data is transferred by a data bus for 1 pixel and, as shown in **FIG. 18**, here, is fetched to the drain drivers at double edges (rising edge, falling edge) of a clock D2 of 32.5 MHz. The maximum frequency of the reference clock (clock D2) to the drain drivers of the liquid crystal display device TFT-LCD and the display data becomes 32.5 MHz.

[0023] In this manner, using the drain drivers adopting the LVDS method and the double-edged specification, it is possible to realize a thin film transistor type liquid crystal display device of a low manufacturing cost without increasing the size of a printed circuit board on which an interface circuit is mounted.

[0024] However, the above-mentioned constitution of the conventional liquid crystal display device has a problem that it is necessary to change also the host computer side constitution in accordance with the LVDS specification.

[0025] To cope with such a problem, the applicant of the present application proposed a liquid crystal display device which enables the fetching of data to drain drivers at the low clock frequency using an interface which does not change the host computer side constitution, that is, with an interface which does not adopt the above-mentioned LVDS method (Japanese laid-open patent publication 338938/2000).

[0026] The above-mentioned proposal is configured to be capable of converting the number of pixels from the host computer to the less number of pixels and also of using drain drivers of a double-edged specification which enables the fetching of the number of pixels into the drain drivers using the clock signals of low frequency.

[0027] To be more specific, to fetch the display data into the drain drivers at both edges (double edges) of rising and falling of the clock signal, the device is equipped with a clock multiplying circuit for multiplying the frequency of the clock signal inputted from the host computer and the image data inputted from the host computer is converted into the less number of display data using the multiplied clock signal.

[0028] **FIG. 19** is a block diagram for explaining the constitution of an essential part adopting a double-edged image data fetching method and **FIG. 20** is a waveform diagram for explaining an operation thereof. In **FIG. 19, a** display control device mounted on an interface circuit board of a liquid crystal display device receives clock signals (DCLK) inputted from a host computer, n pieces of image data (Data) and other control signals (H-Sync: horizontal synchronizing signals, V-Sync: vertical synchronizing signals and the like).

[0029] The clock signal (DCLK) which constitutes a basic clock is inputted to a parallel-serial converter P/S and, at the same time, is supplied to a clock signal synthesizer CLS. The clock signal synthesizer CLS multiplies the inputted clock signal DCLK "a" times (here, a =2) to form **2**DCLK and this clock signal is supplied to the parallel-serial converter circuit P/S.

[0030] The display control device converts n pieces of image data into m pieces of image data ($m \leqq n$) in the parallel-serial converter P/S and the image data is fetched at double edges consisting of a rising edge and a falling edge of the basic clock DCLK by the drain drivers of the doubled-edged specification and the image data are displayed on the liquid crystal panel.

[0031] **FIG. 21** is a block diagram for explaining a constitutional example of a liquid crystal display device which adopts the above-mentioned double-edged fetching method. A liquid crystal display panel TFT-LCD is a high definition panel having 1024×3×768 pixels similar to the panel

explained in conjunction with **FIG. 17**. A plurality of drain drivers having the double-edged specification are arranged corresponding to rows of pixels in the lateral direction and a plurality of gate drivers are arranged corresponding to columns of pixels in the longitudinal direction.

[**0032**] A display control device and a power source circuit are mounted on an interface circuit board. Further, a PLL which multiplies a clock DCLK (reference clock) of 32.5 MHz which constitutes a pixel clock inputted from a host computer twice is mounted on the interface circuit board. That is, the reference clock of 32.5 MHz inputted from the host computer is supplied to a 1 pixel data converting circuit of the display control device after the frequency is multiplied to 65 MHz by a clock synthesizer (constituted of the PLL).

[**0033**] 2 pixels inputted from the host computer, that is, pixel data (red (R), green (G), blue (B)) for the first pixel and pixel data (red (R), green (G), blue (B)) for the second pixel are converted into serial data of 1 pixel by the 1 pixel data converting circuit which constitutes a parallel-serial converter and then are outputted to the drain drivers. Further, the display control device outputs a clock D of the frequency equal to that of the reference clock inputted from the host computer to the drain drivers and also outputs a frame starting direction signal and a gate clock (clock G) to the gate drivers.

[**0034**] The power source circuit includes a positive voltage generation circuit, a negative voltage generation circuit, an analogue multiplexer, a counter electrode generation circuit and a gate voltage generation circuit. The power source circuit is configured to perform the alternation driving of the drain drivers which has been explained in the above-mentioned paragraph of the related art using the positive voltage generation circuit, the negative voltage generation circuit and the analogue multiplexer.

[**0035**] The drain drivers fetch and latch the pixel data inputted from the display control device through a data bus at both edges (double edges) consisting of a rising edge and a falling edge of the clock D and output the pixel data to lines to be selected by the gate drivers so as to perform the display of the pixels.

[**0036**] Due to such a constitution, even when the data constitution of the drain drivers is for 1 pixel, the device can cope with the inputting of display data for 2 pixels so that a liquid crystal display device of high definition can be obtained by using the interface circuit having the conventional constitution without necessitating the high-speed transfer of display data from the host computer.

[**0037**] Due to such a constitution, the pixel data from the host computer is converted into pixel data with less number of pixels and the pixel data can be fetched by drain drivers with a clock of low frequency so that the high-speed transfer of image data can be realized without adopting the LVDS method.

[**0038**] The host computer, at the time of starting thereof, transmits the image data from a graphic controller to the liquid crystal display device side by sequentially converting the resolution of the image data (for example, 640(720)×350→640×480→640×350→1024×768).

[**0039**] An image signal ineffective signal is transmitted in conformity with the converting timing of the resolution so as to suppress the influence of the conversion of resolution to an image display. However, in this transitional transmission time, there may be a case that the disturbance is generated with respect to waveforms of the clock, the horizontal synchronizing signal H-Sync, the vertical synchronizing signal V-Sync and image data signals. That is, as indicated with an arrow A in **FIG. 20** in an enlarged form, a signal level which is to be recognized as a low level (Low) has the fluctuation in a waveform and hence, the signal level is erroneously recognized as a high level (High).

[**0040**] Conventionally, assuming that there exist no irregularities with respect to the clock inputted from the outside (also referred to as an external clock), such irregularities of the clock has not been taken into consideration. However, in an actual operation, there may be a case that the above-mentioned a fluctuation is generated and this induces a miscounting of the clock whereby the transmission of the image signal ineffective signal is disturbed.

[**0041**] Accordingly, it is an object of the present invention to provide a liquid crystal display device and a driving method thereof which can obviate the generation of display irregularities by recognizing normal/irregular of the above-mentioned external clock and stopping the supply of image signals to drivers of a liquid crystal display device or performing the display by replacing the external clock with a pseudo clock from a pseudo clock generation circuit which is separately provided when the external clock is in error.

[**0042**] To achieve the above-mentioned object, the present invention is directed to a liquid crystal display device which converts the number of pixels from a host computer into the less number of pixels and drain drivers of a double-edged specification which fetches these pixels in the drain drivers with a clock signal of low frequency can be used, wherein

[**0043**] the display control devices is further provided with clock surveillance means which detects the presence or the absence of irregularity of timing of a pixel clock signal inputted from the host computer which constitutes an external signal source. To describe typical constitution of the present invention, they are as follows.

[**0044**] First of all, as a driving method of a liquid crystal display device according to the present invention, following constitutions are considered.

[**0045**] (1) In a method for driving a liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply display signals based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning signals to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers as the display signals,

[**0046**] the display control device includes clock surveillance means for detecting the presence or the

absence of the irregularity of timing of the pixel clock signals inputted from the external signal source, and

[0047] when the clock surveillance means detects the presence of the irregularity of timing, the supply of the image data from the display control device to the drain drivers is stopped.

[0048] Due to such a constitution, when the clock surveillance means detects the irregularity of timing of the clock, the clock surveillance means determines that the clock is not normally inputted. That is, it is determined that this state is a state in which the host computer side has not been completely started or the state is a transitional period which follows the change of an operation mode and hence, it is possible to take the protective processing for preventing the generation of the irregularity of display by bringing an inner power source into an inoperable state at the liquid crystal display device side.

[0049] (2) In a method for driving a liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply driving voltages based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning voltages to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers,

[0050] the display control device includes clock surveillance means for detecting the presence or the absence of the irregularity of timing of the pixel clock signals inputted from the external signal source and inner pixel clock signal generating means for generating pseudo clock signals equivalent to the pixel clock signals, and

[0051] when the clock surveillance means detects the presence of the irregularity of timing, the pseudo clock signals generated by the inner pixel clock signal generating means are supplied to the display control device.

[0052] Due to such a constitution, when the clock surveillance means detects the irregularity of timing of the clock, an irregular display is obviated by performing a pseudo image display so that a normal image display can be performed at a point of time that the above-mentioned timing is restored.

[0053] Following devices are considered as liquid crystal display devices of the present invention which are driven by the above-mentioned driving method.

[0054] (3) In a liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply driving voltages based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning voltages to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers,

[0055] wherein the display control device includes a clock signal synthesizer which generates reference clock signals which are formed by multiplying the frequency of the pixel clock signals inputted from the external signal source "a" times and a clock signal comparator circuit which compares the inputted pixel clock signals and an output of the reference clock signals of the clock signal synthesizer, determines whether it is effective or ineffective based on the presence or the absence of the irregularity of timing of the pixel clock signals, and outputs a clock ineffective signal which stops the supply of the pixel clock signals to the parallel-serial converting means when the result of the determination is ineffective.

[0056] Due to such a constitution, it is possible to obtain a liquid crystal display device which, when the clock surveillance means detects the irregularities of timing of the clock, can determine that the clock is not normally inputted and brings the inner power source into an inoperable state at the liquid crystal display device side so as to prevent the generation of the irregularity of display.

[0057] (4) In a liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply driving voltages based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning voltages to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers,

[0058] wherein the display control device includes a clock signal synthesizer which generates reference clock signals which are formed by multiplying the frequency of the pixel clock signals inputted from the external signal source "a" times, a clock signal comparator circuit which compares the inputted pixel clock signals and an output of the reference clock signals of the clock signal synthesizer and determines whether it is effective or ineffective based on the presence or the absence of the irregularity of timing of the pixel clock signals, an inner clock signal generation circuit which generates pseudo clock signals equivalent to the image clock signals, and a clock signal switching circuit which stops the supply of the pixel clocks to the parallel-serial converting means and also supplies the pseudo clock

signals outputted from the inner clock generation circuit to the parallel-serial converter when the result of the determination of the clock signal comparator circuit is ineffective.

[0059] Due to such a constitution, it is possible to obtain a liquid crystal display device which performs the pseudo image display when the clock surveillance means detects the irregularity of timing of the clock so as to prevent the generation of irregularity of display.

[0060] Further, specific constitutions of the liquid crystal display device of the present invention are listed hereinafter.

[0061] (5) In the constitution (3) or (4), the number of multiplication "a" of the clock signal synthesizer is n or 1/n, wherein n is an integer and satisfies $n \geqq 2$.

[0062] (6) In any one of the constitutions (3) to (5), provided that the number of the image data is set to N pieces, the number of display data inputted to the drain drivers of the liquid crystal display panel is set to M pieces, and N/M is set to satisfy the relationship of 1/a (a: integer), the N pieces of display data is converted into M pieces of display data($M \leqq N$) based on clocks a×CL which is obtained by multiplying the frequency "a" times using the clock multiplying circuit and, thereafter, the M pieces of display data are inputted to the drain drivers at double edges consisting of rising of signal and falling of signal of the clocks CL.

[0063] (7) In any one of constitutions (3) to (6), the number N of image data from the external signal source is 2, the number M of image data inputted to the liquid crystal display panel is 1, the clock signal synthesizer is a PLL, and the multiplication number "a" thereof is 2.

[0064] (8) In any one of constitutions (3) to (7), the frequency of the pixel clock signals inputted from the external signal source is 32.5 MHz and the drain driver is a drain driver corresponding to double edges.

[0065] The above-mentioned PLL which generates the clock signal has a simple constitution and other circuits which constitute the interface circuit and the drain drivers can be constituted of existing semiconductor circuits so that there is no problem with respect to the reliability of operation.

[0066] Here, it is needless to say that the present invention is not limited to the above-mentioned constitutions and various modifications are possible without departing from the technical concept of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0067] **FIG. 1** is a block diagram for explaining the constitution of an essential part of a first embodiment of a liquid crystal display device according to the present invention;

[0068] **FIG. 2** is a block diagram for explaining a constitutional example of a clock surveillance circuit in **FIG. 1**;

[0069] **FIG. 3** is a timing chart for explaining an operation of the clock surveillance circuit shown in **FIG. 2**;

[0070] **FIG. 4** is a timing chart for explaining an operation of the clock surveillance circuit shown in **FIG. 2**;

[0071] **FIG. 5** is a waveform diagram for explaining the operation shown in **FIG. 2** of the clock surveillance circuit in further detail;

[0072] **FIG. 6** is a block diagram for explaining one constitutional example of a clock comparator circuit CCM constituting the clock surveillance circuit shown in **FIG. 1**;

[0073] **FIG. 7** is a block diagram for explaining the constitution of an essential part of a second embodiment of a liquid crystal display device according to the present invention;

[0074] **FIG. 8** is an equivalent circuit for explaining one example of a pixel portion of a liquid crystal display panel constituting a liquid crystal display device according to the present invention;

[0075] **FIG. 9** is an equivalent circuit for explaining another example of the pixel portion of the liquid crystal display panel constituting the liquid crystal display device according to the present invention;

[0076] **FIG. 10** is a timing chart for explaining in detail the relationship between the liquid crystal driving voltage outputted to drain signal lines from the drain drivers and the liquid crystal driving voltage applied to a common electrode;

[0077] **FIGS. 11A and 11B** are explanatory drawings for the mounting position of the interface printed circuit board at liquid crystal display panel, wherein **FIG. 11A** is a plan view of the liquid crystal display panel PNL having a flexible printed circuit board FPC**1** connected thereto and **FIG. 11B** is a plan view of the interface printed circuit board PCB mounted on a back surface of the flexible printed circuit board FPC**1**;

[0078] **FIG. 12** is a block diagram for explaining a constitutional example of an active matrix type liquid crystal display device;

[0079] **FIG. 13** is an explanatory view of the timing in the lateral direction, that is, in the horizontal direction with respect to the display control in **FIG. 12**;

[0080] **FIG. 14** is an explanatory view of the timing in the longitudinal direction, that is, in the vertical direction with respect to the display control in **FIG. 12**;

[0081] **FIG. 15**(*a*) and **15**(*b*) are conceptual views of the LVDS transferring method, wherein **FIG. 15**(*a*) is a conceptual view of the LVDS transfer method and **FIG. 15**(*b*) is an explanatory view of alternation;

[0082] FIGS. **16**(*a*) and **16**(*b*) are basic constitutional views of the LVDS transferring method, wherein **FIG. 16**(*a*) is a constitutional view of transferring lines of the LVDS and **FIG. 16**(*b*) is an explanatory view of display data and clocks which are transferred through the transferring lines of the LVDS;

[0083] **FIG. 17** is a block diagram for explaining a constitutional example of a liquid crystal display device adopting the LVDS transfer method;

[0084] **FIG. 18** is a timing chart of an input and an output of the display control device using a double-edged specification;

[0085] **FIG. 19** is a block diagram for explaining the constitution of an essential part of a double-edged image data fetching method;

[0086] **FIG. 20** is a waveform diagram for explaining the operation shown in **FIG. 19**; and

[0087] **FIG. 21** is a block diagram for explaining a constitutional example of the liquid crystal display device adopting a double-edged image data fetching method.

DETAILED DESCRIPTION

[0088] Embodiments of the present invention are explained in detail in conjunction with drawings which show these embodiments hereinafter.

[0089] **FIG. 1** is a block diagram for explaining the constitution of an essential part of a first embodiment of a liquid crystal display device according to the present invention. In **FIG. 1, a** display control device which is mounted on an interface circuit board includes a parallel-serial converter P/S, a clock synthesizer (PLL) CLS and a clock comparator circuit CCM. The clock synthesizer CLS and the clock comparator circuit CCM constitute a clock surveillance circuit.

[0090] The display control device receives a clock DCLK, n pieces of image data (Data) and other control signals (H-Sync: horizontal synchronizing signal, V-Sync: vertical synchronizing signal and the like).

[0091] The clock DCLK which constitutes a basic clock is inputted to the parallel-serial converter P-S and, at the same time, is supplied to the clock synthesizer CLS. The clock synthesizer CLS multiplies the inputted clock DCLK "a" times (here, a=2) so as to form **2** DCLK and this **2** DCLK is supplied to the parallel-serial converter P/S and the clock comparator circuit CCM.

[0092] n pieces of image data inputted into the parallel-serial converter are converted into m pieces of image data ($m \leqq n$) and the image data are fetched at double edges consisting of a rising edge and a falling edge of the basic clock DCLK in drain drivers of the double-edged specification and are displayed on a liquid crystal display panel.

[0093] The clock comparator circuit CCM compares the reference clock DCLK and twice-multiplied-clock **2** DCLK so as to determine whether the frequency of the clock DCLK is normal or irregular and an output of the result of determination (determination output) PLLVAL (normal=high level: High, irregular=low level: Low) is supplied to the parallel-serial converter P/S.

[0094] When it is determined that the frequency of the clock DCLK is abnormal, the output PLLVAL becomes the low level: Low and the supply of the image data from the parallel-serial converter P/S to the drain drivers is stopped with the output PLLVAL of the low level.

[0095] **FIG. 2** is a block diagram for explaining a constitutional example of the clock surveillance circuit shown in **FIG. 1**. Further, **FIG. 3** and **FIG. 4** show timing charts for explaining the operation shown in **FIG. 2**. In this embodiment, an explanation is made in accordance with an example in which the number of multiplication is set to "2", the clock DCLK is set to 1280 pulses so that the multiplied clock (reference clock) 2=DCLK is set to 2560 pulses. However, the embodiment is not limited to such an example. The number of multiplication is n times or 1/n times ($n \geqq 2$, n being an integer). Hereinafter, the operation of the clock surveillance circuit shown in **FIG. 2** is explained in conjunction with **FIG. 3** and **FIG. 4**.

[0096] The clock DCLK which constitutes the reference clock signal inputted from the host computer is inputted to a count-up clock of a counter-a CNT-a and a clock synthesizer CLS. 2×DCLK which constitutes an output of the clock synthesizer CLS is inputted to a counter-b CNT-b as an counter-up clock.

[0097] Upon receiving the input of the clock DCLK, the counter-a CNT-a increases a count value by +1. Then, when the count value becomes 1280, the value of the counter-b CNT-b is checked.

[0098] When the value of counter-b CNT-b is 2560 (=1280×2), it is determined that the clock synthesizer CSL is normally operated or the clock DCLK is normally inputted. In this circuit, when it is determined normal, the determining output PLLVAL assumes a high level.

[0099] When the value of counter-b CNT-b is not 2560, it is determined that the operation of the clock synthesizer CLS is irregular and the output of the PLLVAL assumes the low level. Here, a counter (counter-c CNT-c) which is served for storing the number of the occurrence of irregularities performs the counting-up by +1. When the clock synthesizer CLS restores the normal operation (when the value of counter-b CNT-b becomes 2560), the counter-c CNT-c is cleared.

[0100] As a case which prevents the clock synthesizer CLS from assuming the normal operation, there is a case that a PLL which constitutes the clock synthesizer CLS is locked so that a clock of irregular frequency is outputted. Accordingly, the clock synthesizer CLS is to be reset when the value of the counter-c CNT-c becomes 384 (predetermined value).

[0101] When the count value of the counter-a CNT-a becomes 1280, the counter-a CNT-a and the counter-b CNT-b are cleared and perform their operations again continuously. Further, 1280 which is a decode value of the above-mentioned counter-a CNT-a is determined based on the performance of the PLL which constitutes the clock synthesizer in operation.

[0102] 384 which is the predetermined value of the counter-c CNT-c is determined in accordance with an approximately 1 frame time of a thin film transistor TFT type liquid crystal display device and the value is arbitrarily set. The count value of the counter-b CNT-b depends on the output frequency of the clock synthesizer CLS and is set to 2560 by multiplying twice in the above-mentioned example. However, the count value becomes 3840 by multiplying three times and 5120 by multiplying four times.

[0103] **FIG. 5** is a waveform diagram for explaining of the operations in **FIG. 2** in further detail. In the drawing, the order of count values is indicated by D (for example, the 1279th count value is indicated as D **1279**th).

[0104] In **FIG. 5, a** waveform **(1)** is an external clock inputted from a host computer (image clock=reference clock=1280), and a waveform **(2)** indicates the count value of the counter-a, respectively. Moreover in **FIG. 5, a** waveform **(3)** indicates a decode signal of the counter-a, a

waveform (4) indicates a pulse generated by synthesizing an output of the counter-a and the reference clock (a pair of DCLKs) (=D1279-2=reference signal 1), a waveform (5) indicates a reference signal 2 (=D1279-2') generated by synthesizing the reference signal 1 and the reference clock, and a waveform (6) indicates a decode signal of the counter-b, respectively. Furthermore in **FIG. 5, a** waveform (7) indicates the count value of the counter-b, a waveform (8) indicates the reference clock (2DCLK), a waveform (9) indicates a decode/latch output, and a waveform (10) indicates a determination output PLLVAL, respectively.

[0105] First of all, the counter-a counts the external clock DCLK The output of the counter-a assumes the high level when the count D is at the 1279th (D1279th) and assumes the low level when the counter D is at other order.

[0106] The determination of normal/irregular of the external clock is performed by a logic circuit (a clock comparator circuit) shown in **FIG. 6**, for example, in accordance with a following sequence. That is, the count/decode signal D1279-1 (3) of the counter-a and a pair of DCLKs (8) which constitute the reference clock are synthesized by a group of circuits consisting of Flip-Flops FF1, FF2 and an AND circuit AND1 so as to obtain the first reference signal D1279-2 (4). Thereafter, the second reference signal D1279-2' (5) which is obtained by synthesizing the first reference signal D1279-2 and the reference clock (8) using the Flip-Flop FF3 is compared with the decode signal (6) of the counter-b.

[0107] Assuming a case in which the reference clock of 2560 pulse is generated by multiplying the frequency of the external clock of 1280 pulse twice, at a point of time that a certain 1 period (for example, 1 frame period or 1 vertical scanning period), is completed and the next 1 period which succeeds the certain 1 period is started, the external clock outputs the 1279th signal (h'4FF) at the last stage of the above-mentioned "certain 1 period" and the reference clock generates the 2559th signal (h'9FF) at the last stage of the above-mentioned "certain 1 period" and, thereafter, generates 0th signals (h'000) of the above-mentioned following period respectively.

[0108] In case that the counter-b outputs the signal (6) of high level only when the b counter recognizes the reaching of the count value (7) to h'9FF of the reference clock, that is, the 2559th signal (the last clock signal in the above-mentioned certain period), the signal (6) and the output (5) of the above-mentioned reference signal 2 are collated with each other by means of a group of circuits consisting of AND circuits AND2, AND3 and a Flip-Flop FF4 and when both agree to each other at the high level, the decode/latch signal is set to the high level. The decode/latch signal is inputted to the counter-c which will be explained later and the counter-c performs either one of the integration of the number of the occurrence of irregularity of the external clock or resetting of the value in response to the level (high or low) of the decode/latch signal.

[0109] In the above-mentioned example, it is determined that the external clock is normal when the reference signal 2 (5) and the output of the counter-b (6) agree to each other and hence, the decode/latch signal of high level corresponding to the normal external clock resets the number of generation of irregularities of the integrated external clocks at the counter-c.

[0110] On the other hand, when the reference signal 2 (5) and the counter-b output (6) do not agree to each other, (that is, when at least one of the reference signal 2 (5) and the counter-b output (6) assumes the low level in the above-mentioned example), the decode/latch signal assumes the low level and the counter-c integrates the number of the generation of irregularities of the external clock for the above-mentioned every 1 period.

[0111] The levels of the reference signal 2 (5), the counter-b output (6) which are used for the determination of the external clock and the decode/latch signal indicative of the output of the result of the determination are not limited to the above-mentioned example and may be suitably inverted in response to the constitutions of the clock comparator circuit and the counter-c.

[0112] Further, when the frequency of the reference clock is set lower than the frequency of the external clock, for example, the decode signal of the counter-b (outputting a peculiar signal with respect to the last clock signal in the above-mentioned certain 1 period) is synthesized with the external clock thus generating the reference signal and the reference signal may be used as the decode signal of the above-mentioned counter-a.

[0113] The determination output PLLVAL (9) is inputted to the parallel-serial converter which is arranged as a latter stage of the clock comparator circuit and the counter-c. The counter-c recognizes the fluctuation of the determination output PLLVAL (10) at a timing that the external clock DCLK is delayed by 1 pulse from the output D1279-1th of the counter-a.

[0114] When the determination output PLLVAL (10) indicates the low level, the counter-c counts up the number of generation of irregularities of the external clock for the above-mentioned every 1 period. When this count-up numerical value reaches the previously mentioned predetermined value, the counter-c reset the clock synthesizer as mentioned previously.

[0115] **FIG. 6** is a block diagram for explaining one constitutional example of the clock comparator circuit CCM which constitutes the clock surveillance circuit shown in **FIG. 1**. This circuit is, as illustrated in the drawing, comprised of the Flip-Flops FF1, FF2, FF3, FF4, and AND circuits AND1, AND2, AND3, an inverter INV, the counter-b CNT-b and the decoder DR of (h'9FF).

[0116] Respective clocks, count values and other signals in the drawing correspond to respective signals in **FIG. 1** to **FIG. 5** and are served for obtaining the decode/latch output DCL of the decoder DR from the Flip-Flop FF4.

[0117] Due to the first embodiment of the present invention which has been explained heretofore, when the clock surveillance means detect the irregularity of timing of the clock, it is determined that the clock is not inputted normally. That is, it can be determined that this state is the state in which the host computer has no yet completely reached the operable state or is the transitional period which follows the change of the operation mode and hence, the protective processing which prevents the generation of the display irregularity can be performed by bringing the inner power source into the inoperable state at the liquid crystal display side.

[0118] **FIG. 7** is a block diagram for explaining the constitution of an essential part of a second embodiment of a liquid crystal display device according to the present invention. In this embodiment, the liquid crystal display device includes clock surveillance means which is constituted of a clock synthesizer CLS and a clock comparator circuit CCM and detects the presence or the absence of the irregularity of timing of a clock signal DCLK inputted from an external signal source, and an inner clock generation circuit FCG which generates a pseudo clock FDCLK equivalent to the clock signal DCLK.

[0119] In the previous embodiment, when the irregularity of timing of the clock is generated, the protective processing which prevents the generation of irregularity of display by bringing the inner power source into the inoperable state is performed. However, in this embodiment, when the clock surveillance means detects the irregularity of timing, the pseudo clock signal generated by the above-mentioned inner clock signal generation circuit is supplied to the display control device so as to display a pseudo image.

[0120] The inner clock signal generation circuit is controlled in response to the resistance, the capacitance or a quartz oscillator and generates the clocks for an image display. These electronic components may be mounted at the outside of the inner clock signal generation circuit or an integrated circuit element (large-scale integrated circuit) which surrounds the inner clock signal generation circuit. For example, these electronic components may be mounted on the same printed circuit board together with the above-mentioned integrated circuit elements.

[0121] Due to this embodiment, when the clock surveillance means detects the irregularity of timing by the clock, the pseudo screen display is performed so as to obviate the irregular display and the normal image display can be performed at a point of time that the above-mentioned timing is restored.

[0122] Subsequently, the liquid crystal display panel and other constitutional portions which constitute the liquid crystal display device according to the present invention are explained.

[0123] **FIG. 8** is an equivalent circuit for explaining one example of a pixel portion of the liquid crystal display panel which constitutes the liquid crystal display device according to the present invention. Here, the drawing corresponds to an actual geometric arrangement of pixels and a plurality of pixels which are arranged in a matrix array in an effective display area AR (pixel portion) are constituted of two thin film transistors TFT (TFT1, TFT2) per one pixel.

[0124] Symbol D indicates drain signal lines, symbol G indicates gate signal lines, R, G and B are pixel electrodes of respective colors (red, green, blue) and are formed of ITO1. Further, ITO2 indicates a counter electrode (common electrode), CLC indicates a liquid crystal capacitance for indicating a liquid crystal layer equivalently and CADD indicates an additional capacitance formed between a source electrode of the thin film transistor TFT and the gate signal line G of a preceding stage.

[0125] **FIG. 9** is an equivalent circuit for explaining another example of a pixel portion of a liquid crystal display panel which constitutes a liquid crystal display device according to the present invention. This drawing also corresponds to an actual geometric arrangement of pixels. In the same manner as **FIG. 1, a** plurality of pixels which are arranged in a matrix array in an effective display area AR (pixel portion) are constituted of two thin film transistors TFT (TFT1, TFT2) per one pixel. Although two thin film transistors TFT are provided per one pixel in **FIG. 8** and **FIG. 9**, there has been known a liquid crystal display device which constitutes one thin film transistor TFT per one pixel.

[0126] In the same manner, symbol D indicates drain signal lines, symbol G indicates gate signal lines, R, G and B are pixel electrodes of respective colors (red, green, blue), ITO2 indicates a counter electrode (common electrode), CLC indicates a liquid crystal capacitance for indicating a liquid crystal layer equivalently and CSTG indicates holding capacitances formed between common signal lines COM and the source electrodes. However, this liquid crystal display device differs from the liquid crystal display device in **FIG. 8** in that the additional capacitance CADD in **FIG. 3** is formed between the source electrode and the gate signal line G of preceding stage.

[0127] In the above-mentioned liquid crystal display panel shown in **FIG. 8** or **FIG. 9**, the drain electrodes of thin film transistors TFT (TFT1, TFT2) of respective pixels which are arranged in the column direction are respectively connected to the drain signal lines D and respective drain signal lines D are connected to the drain drivers to which voltages of display data of the pixels arranged in the column directions are applied.

[0128] Further, the gate electrodes of the thin film transistors (TFT1, TFT2) in respective pixels arranged in the line direction are respectively connected to the gate signal lines G, and respective gate signal lines G are connected to the gate drivers which supply scanning driving voltages (positive or negative bias voltages) to the gates of the thin film transistors TFT (TFT1, TFT2) for 1 horizontal scanning time.

[0129] Although the present invention is applicable to any liquid crystal display device using the liquid crystal display panels which have the constitutions shown in the above-mentioned **FIG. 8** and **FIG. 9**, in the former liquid crystal display panel, the pulses of the gate signal line G of preceding stage jumps into the pixel electrodes ITO1 through the additional capacitance CADD, while in the latter liquid crystal display panel, there is no such jumping of pulses so that it is possible to obtain the more favorable display.

[0130] **FIG. 10** is a timing diagram which explains in detail the relationship between the liquid crystal driving voltages outputted to the drain signal lines from the drain drivers, that is, the liquid crystal driving voltage applied to the pixel electrodes ITO1 and the liquid crystal driving voltage applied to the common electrode ITO2. Here, the liquid crystal driving voltage outputted to the drain signal lines D from the drain drivers is served for displaying black on a display surface of the liquid crystal display panel.

[0131] As shown in **FIG. 10**, the liquid crystal driving voltage VDH outputted to the odd-numbered drain signal lines D from the drain drivers and the liquid crystal driving voltage VDL outputted to the even-numbered drain signal lines D from the drain drivers have an inverse polarity with respect to the liquid crystal driving voltage VCOM applied

to the common electrode ITO2. That is, when the liquid crystal driving voltage VDH outputted to the odd-numbered drain signal lines D has the positive polarity (or negative polarity), the liquid crystal driving voltage VDL outputted to the even-numbered drain signal lines D has the negative polarity (or positive polarity).

[0132] Further, the polarity is inverted every 1 line (1H) and the polarity for every line is inverted every frame. With the use of this dot inversion method, the voltages applied to the neighboring drain signal lines D have polarities opposite each other and hence, the currents which flow into the neighboring common electrodes ITO2 and the neighboring gate signal lines G cancel each other so that the power consumption can be reduced.

[0133] Further, since the current which flows into the common electrode ITO2 is small, the voltage drop is not increased whereby the voltage level of the common electrode ITO2 becomes stable and the deterioration of the display quality can be minimized.

[0134] **FIG. 11A** is a plan view of the liquid crystal display panel for explaining the mounting position of the interface circuit board. On a lower side of the liquid crystal display panel PNL, a flexible printed circuit board FPC2 which mounts drain drivers IC1 bent along a column of holes HOP toward a back surface of the liquid crystal display panel PNL as indicated by **FIG. 11A** is mounted.

[0135] Further, on a left side of the liquid crystal display panel PNL, the flexible printed circuit board FPC1 which mounts the gate drivers IC2 bent toward the back surface of the liquid crystal display panel PNL are mounted.

[0136] On a back surface of the flexible printed circuit board FPC1, the interface printed circuit board PCB shown in **FIG. 11B** is mounted. The TCON which is mounted on the interface printed circuit board PCB is a semiconductor integrated circuit which constitutes the display control device.

[0137] Various signals such as the clocks and image data from the host computer are inputted to a connector CT1 of the interface printed circuit board PCB. A connector CT3 of the flexible printed circuit board FPC1 is connected to a connector CT3' of the interface printed circuit board PCB and a connector CT4 of the flexible printed circuit board FPC2 is connected to a connector CT4' of the interface printed circuit board PCB so that the above-mentioned clocks and image data outputted from the TCON of the display control device are supplied.

[0138] Here, in the liquid crystal display panel PNL, a liquid crystal layer is inserted into a gap formed between an upper substrate SUB1 and a lower substrate SUB2 which are laminated to each other and an upper polarizer POL1 is laminated on an uppermost layer of the liquid crystal display panel PNL. Although not shown in the drawing, a lower polarizer is laminated to an uppermost layer of a back surface of the liquid crystal display panel. AR indicates the effective display area.

[0139] By applying the above-mentioned embodiments to the liquid crystal display device having the above-mentioned constitution, the liquid crystal display device recognizes whether the external clock is normal or not and stops the supply of the video signals to the drivers of the liquid crystal display devices or performs the display by replacing the external clock with the pseudo clock from the pseudo clock generation circuit provided separately when the external clock is irregular so that it is possible to obtain the liquid crystal display device which can obviate the generation of the display irregularity and can perform the image display of high definition without necessitating the high-speed transfer of the display data from the host computer.

[0140] As has been explained heretofore, according to the present invention, with the use of the interface which does not change the constitution of the host computer side, that is, with the use of the interface which does not adopt the LVDS method, it is possible to fetch the display data into the drain drivers using double edges of the low pixel clock frequency. Further, the liquid crystal display device recognizes whether the external clock is normal or not and stops the supply of the image signals to the drain drivers of the liquid crystal display devices or performs the display by replacing the external clock with the pseudo clock from the pseudo clock generation circuit provided separately when the external clock is irregular so that it is possible to provide the liquid crystal display device which can obviate the generation of the display irregularity and can perform the image display of high definition.

What is claimed is:

1. A method for driving a liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply display signals based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning signals to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers as the display signals,

wherein the display control device includes clock surveillance means for detecting the presence or the absence of the irregularity of timing of the pixel clock signals inputted from the external signal source, and

when the clock surveillance means detects the presence of the irregularity of timing, the supply of the image data from the display control device to the drain drivers is stopped.

2. A method for driving a liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply driving voltages based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning voltages to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers,

wherein the display control device includes clock surveillance means for detecting the presence or the absence of the irregularity of timing of the pixel clock signals inputted from the external signal source and inner pixel clock signal generating means for generating pseudo clock signals equivalent to the pixel clock signals, and

when the clock surveillance means detects the presence of the irregularity of timing, the pseudo clock signals generated by the inner pixel clock signal generating means are supplied to the display control device.

3. A liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply driving voltages based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning voltages to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers,

wherein the display control device includes a clock signal synthesizer which generates reference clock signals which are formed by multiplying the frequency of the pixel clock signals inputted from the external signal source "a" times and a clock signal comparator circuit which compares the inputted pixel clock signals and an output of the reference clock signals of the clock signal synthesizer, determines whether it is effective or ineffective based on the presence or the absence of the irregularity of timing of the pixel clock signals, and outputs a clock ineffective signal which stops the supply of the pixel clock signals to the parallel-serial converting means when the result of the determination is ineffective.

4. A liquid crystal display device comprising a liquid crystal display panel which has a plurality of pixels being constituted of active elements and formed in a matrix array, a plurality of drain drivers which apply driving voltages based on control signals including image data and pixel clock signals inputted from an external signal source to a plurality of pixels in the lateral direction of the matrix, a plurality of gate drivers which apply scanning voltages to a plurality of pixels in the longitudinal direction of the matrix, and a display control device which has parallel-serial conversion means which performs the parallel-serial conversion of the image data based on the pixel clock signals and supplies the image data to the drain drivers,

wherein the display control device includes a clock signal synthesizer which generates reference clock signals which are formed by multiplying the frequency of the pixel clock signals inputted from the external signal source "a" times, a clock signal comparator circuit which compares the inputted pixel clock signals and an output of the reference clock signals of the clock signal synthesizer and determines whether it is effective or ineffective based on the presence or the absence of the irregularity of timing of the pixel clock signals, an inner clock signal generation circuit which generates pseudo clock signals equivalent to the image clock signals, and a clock signal switching circuit which stops the supply of the pixel clock signals to the parallel-serial converting means and also supplies the pseudo clock signals outputted from the inner clock signal generation circuit to the parallel-serial converter when the result of the determination of the clock signal comparator circuit is ineffective.

5. A liquid crystal display device according to claim 3, wherein the number of multiplication "a" of the clock signal synthesizer is n or 1/n, wherein n is an integer and satisfies $n \geqq 2$.

6. A liquid crystal display device according to claim 3, wherein provided that the number of the image data is set to N pieces, the number of display data inputted to the drain drivers of the liquid crystal display panel is set to M pieces, and N/M is set to satisfy the relationship of 1/a (a: integer), the N pieces of display data is converted into M pieces of display data($M \leqq N$) based on clocks a×CL which is obtained by multiplying the frequency "a" times using a clock multiplying circuit and, thereafter, the M pieces of display data are inputted to the drain drivers at double edges consisting of rising of signal and falling of signal of the clocks CL.

7. A liquid crystal display device according to claim 3, wherein the number N of image data from the external signal source is 2, the number M of image data inputted to the liquid crystal display panel is 1, the clock signal synthesizer is a PLL, and the multiplication number "a" thereof is 2.

8. A liquid crystal display device according to claim 3, wherein the frequency of the pixel clock signals inputted from the external signal source is 32.5 MHz and the drain driver is a drain driver corresponding to double edges.

9. A liquid crystal display device according to claim 4, wherein the number of multiplication "a" of the clock signal synthesizer is n or 1/n, wherein n is an integer and satisfies $n \geqq 2$.

10. A liquid crystal display device according to claim 4, wherein provided that the number of the image data is set to N pieces, the number of display data inputted to the drain drivers of the liquid crystal display panel is set to M pieces, and N/M is set to satisfy the relationship of 1/a (a: integer), the N pieces of display data is converted into M pieces of display data($M \leqq N$) based on clocks a×CL which is obtained by multiplying the frequency "a" times using a clock multiplying circuit and, thereafter, the M pieces of display data are inputted to the drain drivers at double edges consisting of rising of signal and falling of signal of the clocks CL.

11. A liquid crystal display device according to claim 4, wherein the number N of image data from the external signal source is 2, the number M of image data inputted to the liquid crystal display panel is 1, the clock signal synthesizer is a PLL, and the multiplication number "a" thereof is 2.

12. A liquid crystal display device according to claim 4, wherein the frequency of the pixel clock signals inputted from the external signal source is 32.5 MHz and the drain driver is a drain driver corresponding to double edges.

* * * * *

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摘要(译)

液晶显示装置的接口，其将从诸如主计算机的外部信号源输入的图像信号的像素数转换为具有较少像素数的图像信号，并且将图像信号提取到处于双边缘的漏极驱动器中。低频时钟信号，时钟监视装置包括时钟合成器和时钟比较器电路，它检测从外部信号源输入的像素时钟信号的定时的不规则性的存在或不存在，并输出正常/的确定信号安装了不规则的像素时钟信号。当确定像素时钟信号是不规则的时，停止从并行 - 串行转换器向漏极驱动器提供图像数据，从而可以避免在液晶显示装置中产生不规则的显示。