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Ohta et al.(10) **Pub. No.: US 2001/0012086 A1**(43) **Pub. Date: Aug. 9, 2001**(54) **LIQUID CRYSTAL DISPLAY DEVICE****Publication Classification**(51) **Int. Cl.⁷** G02F 1/136; G02F 1/1343(52) **U.S. Cl.** 349/143; 349/42(76) **Inventors:** Masuyuki Ohta, Kariya (JP); Junichi Ohwada, Mobara (JP); Nobutake Konishi, Mobara (JP); Masayuki Hikiba, Mobara (JP)

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EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834 (US)**(21) **Appl. No.:** 09/823,370(22) **Filed:** Mar. 30, 2001**Related U.S. Application Data**

(63) Continuation of application No. 09/760,385, filed on Jan. 11, 2001.

(30) **Foreign Application Priority Data**

Jan. 12, 2000 (JP) 2000-003348

(57) **ABSTRACT**

A liquid crystal display device includes a first substrate and a second substrate facing the first substrate. A liquid crystal layer is provided between the first and second substrates. First and second gate lines are extending in a first direction, and first and second drain lines are extending in a second direction. A pixel area is defined by the gate lines and drain lines. A counter electrode assigned to the pixel area and having a hollow portion is provided adjacent to a solid portion. The hollow and solid portions are extending in the second direction. One hollow portion is provided after N number of the solid portions, the N being a number equal to or greater than 3. A pixel electrode is assigned to the pixel area and is opposing the counter electrode. The pixel electrode has a connecting portion extending in the first direction and first and second extending portions extending in the second direction. The connection portion connects the first and second extending portions, wherein the first extending portion is vertically aligned to the hollow portion of the counter electrode and the second extending portion is vertically aligned to the solid portion of the counter electrode. An insulating layer is provided between the counter and pixel electrodes.

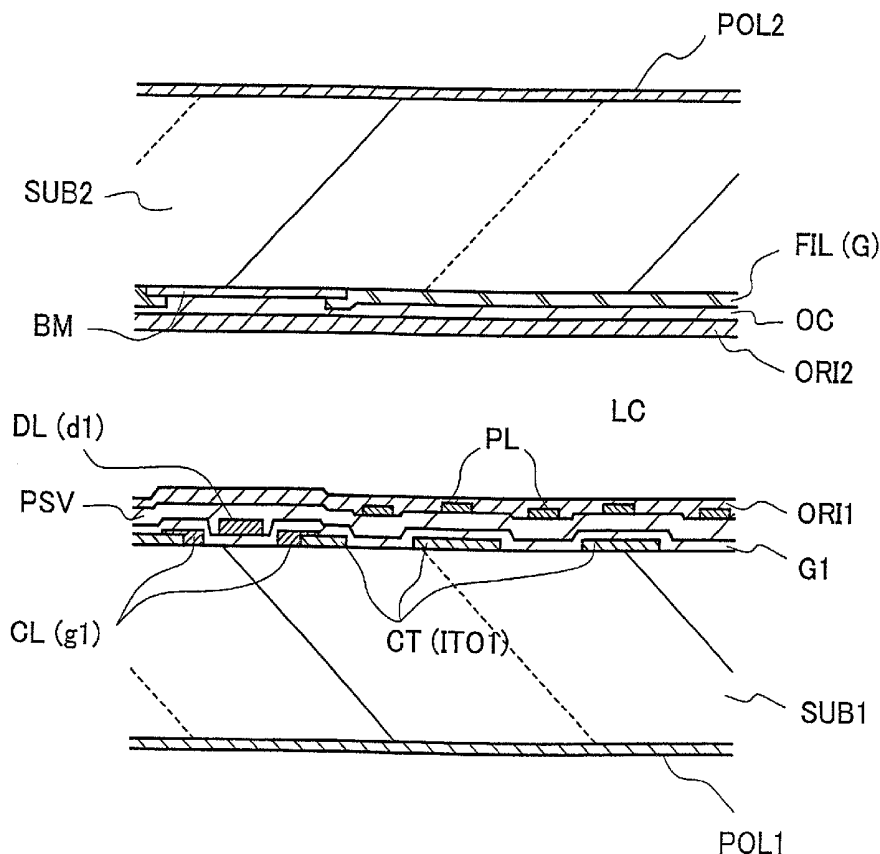


FIG. 1

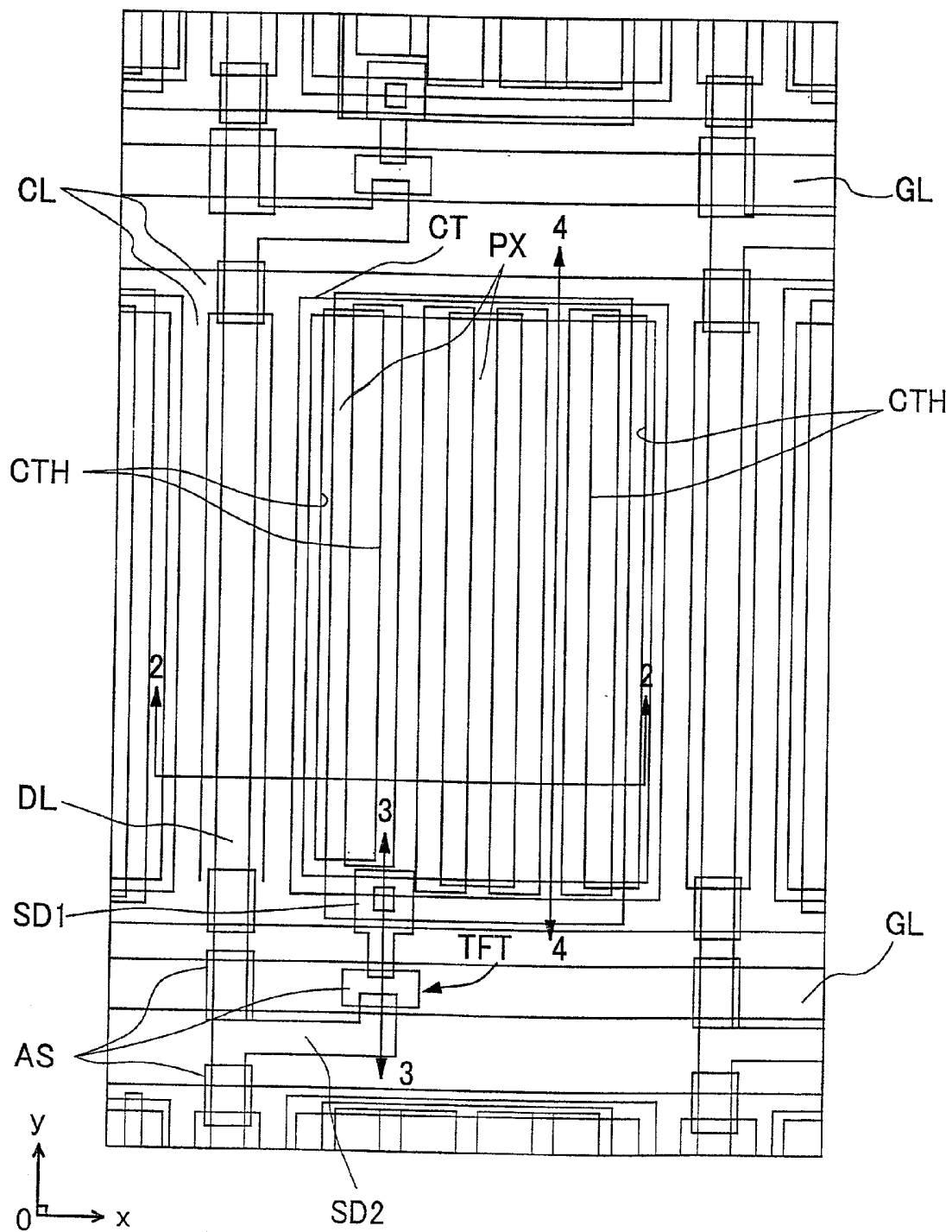
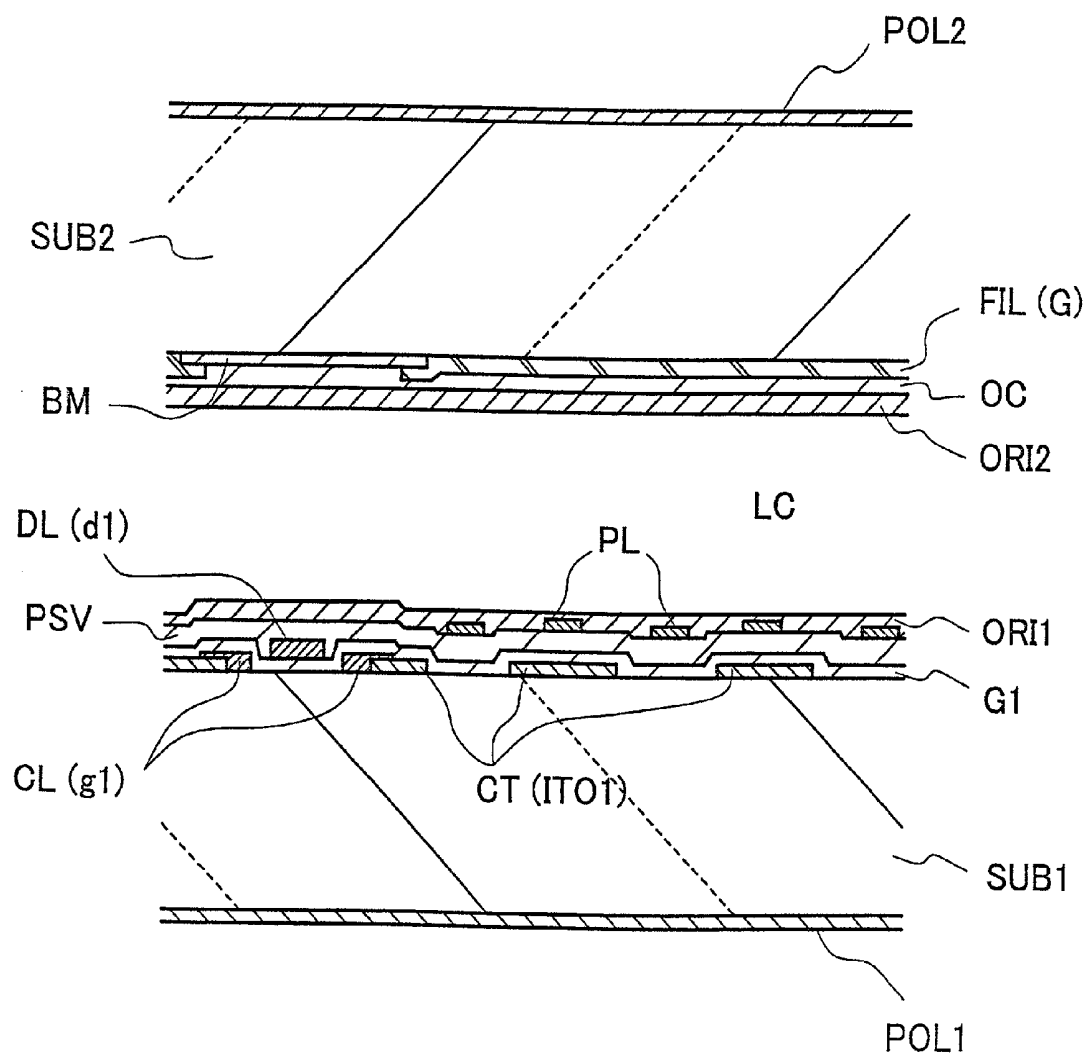


FIG. 2



3
G.
F.

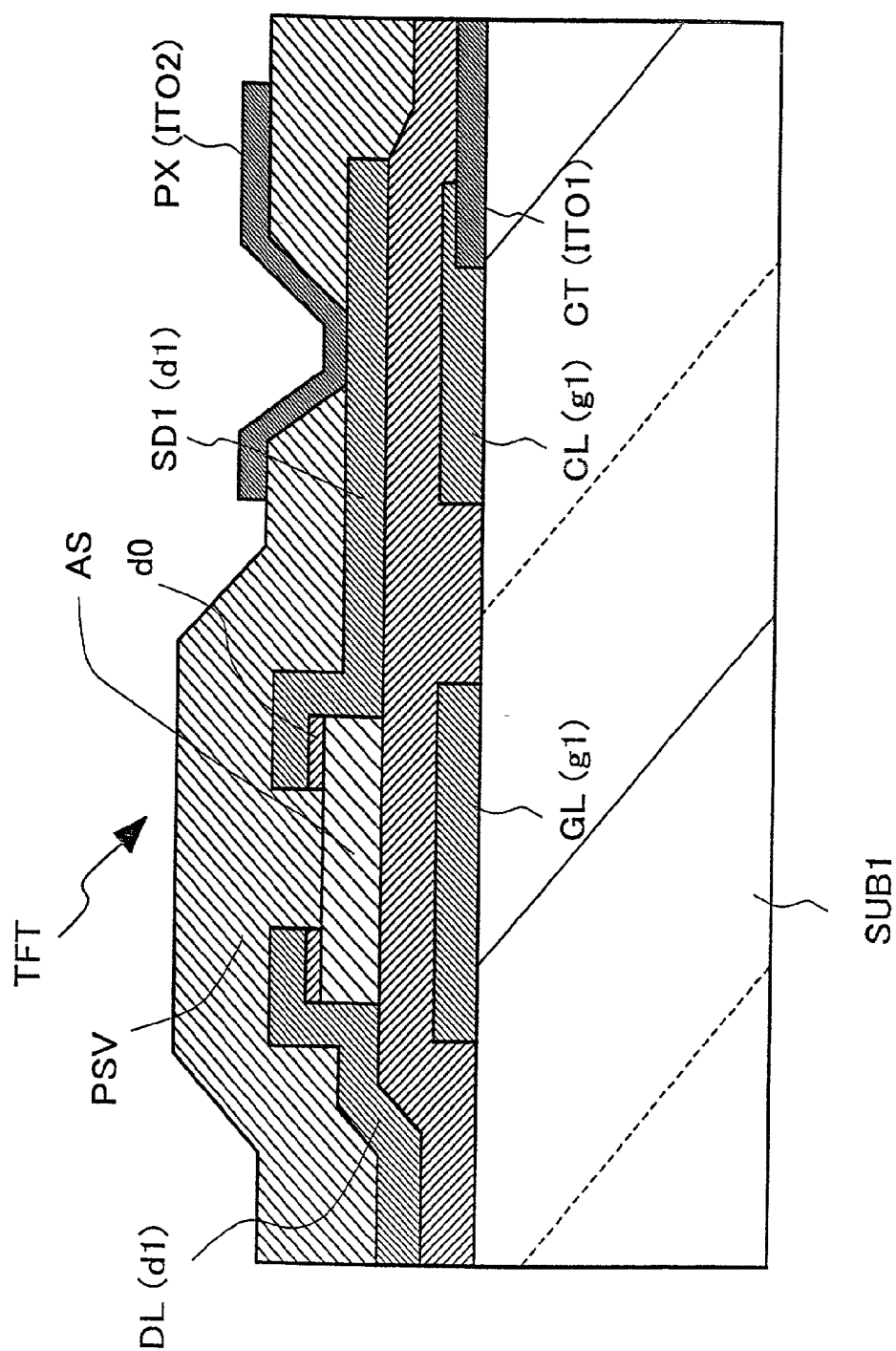


FIG. 4

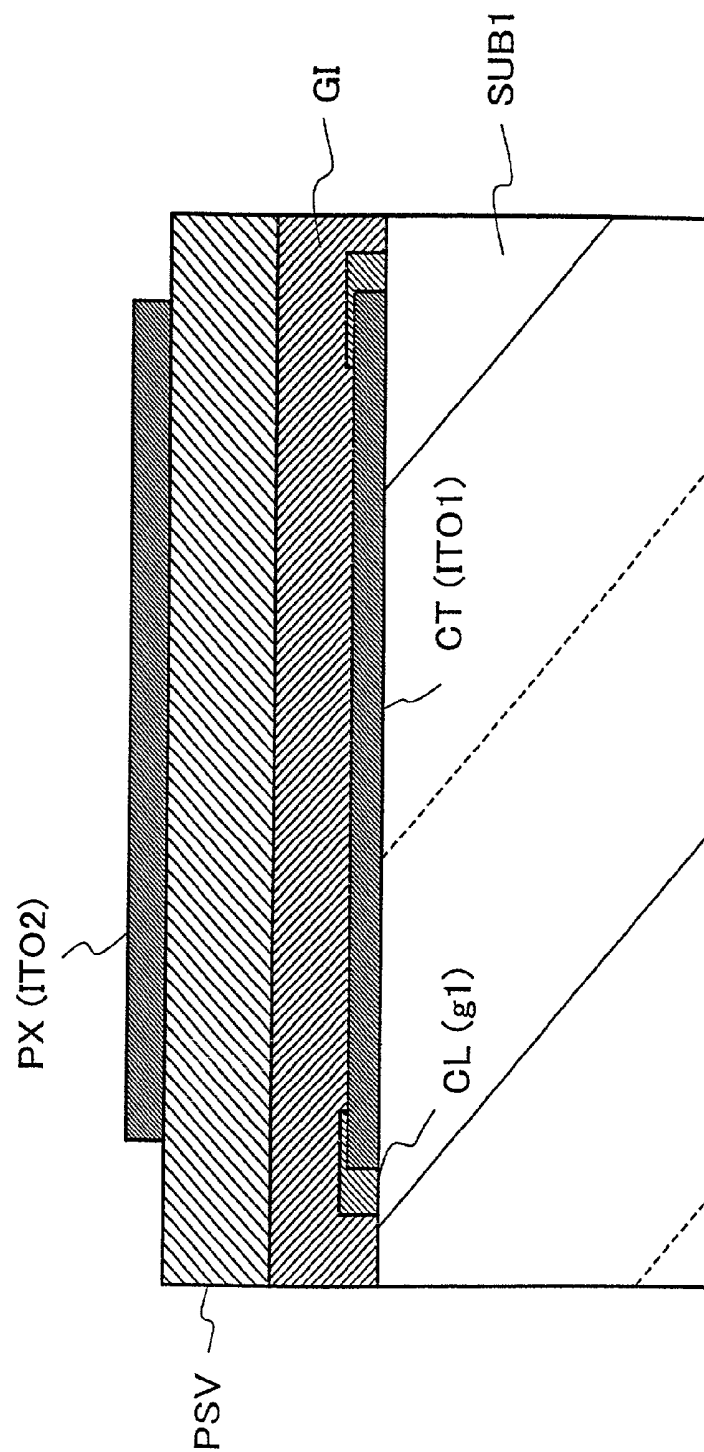


FIG. 5

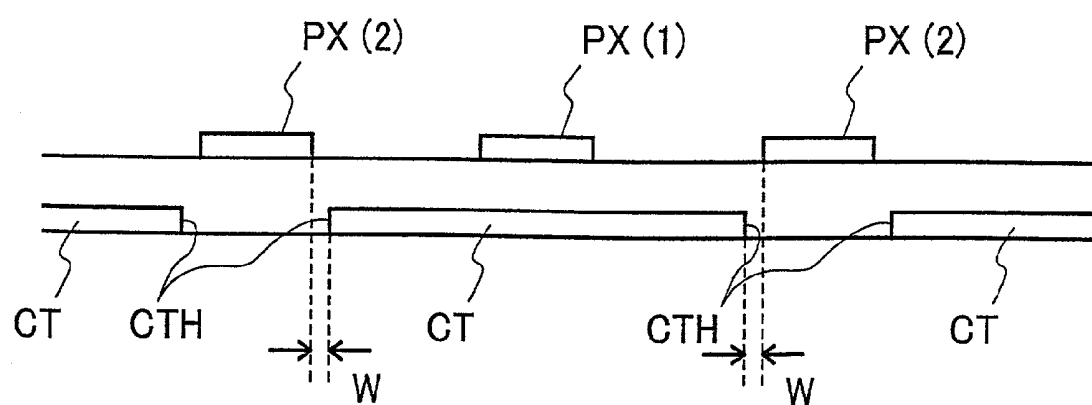


FIG. 6

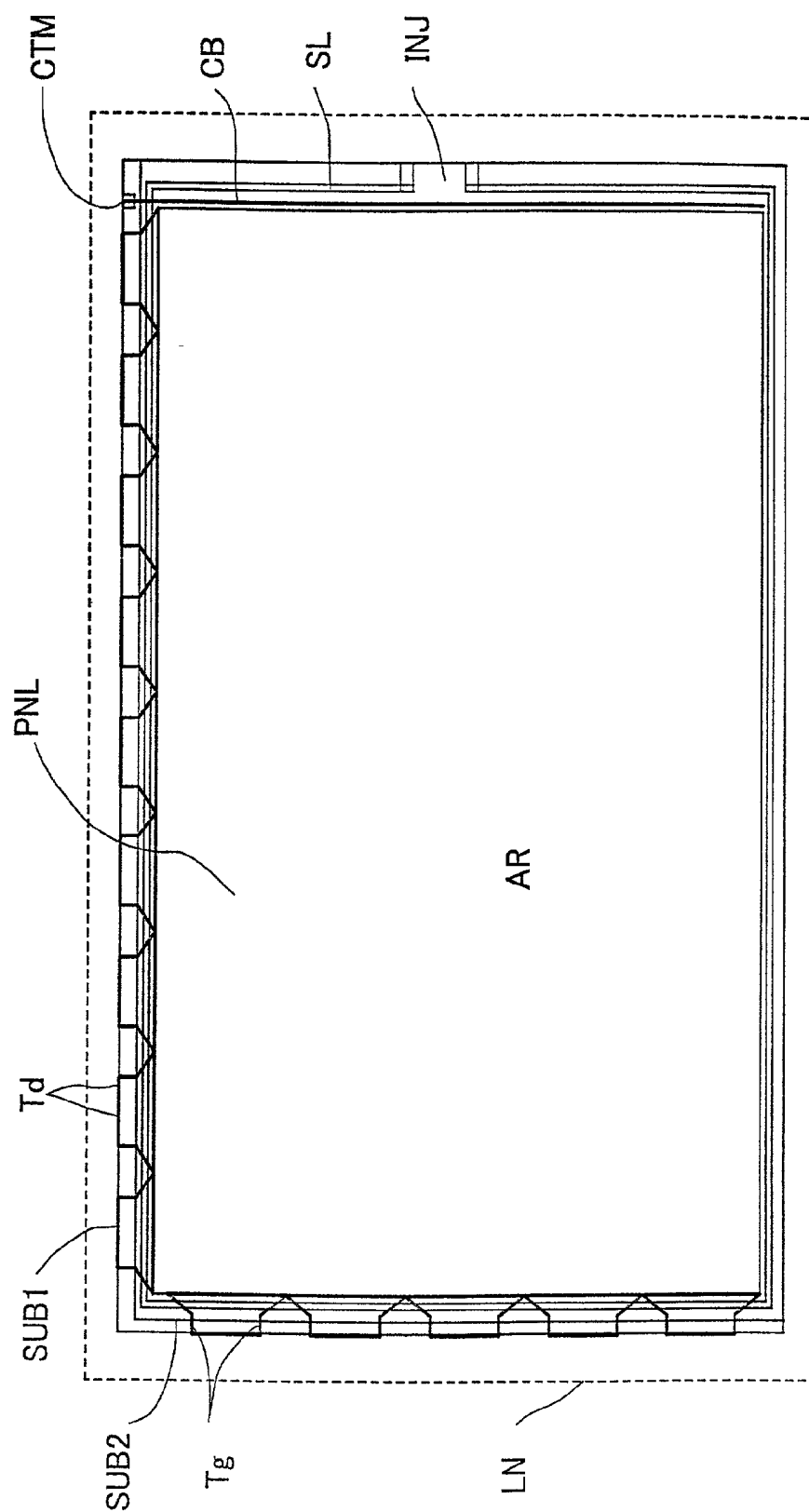


FIG. 7

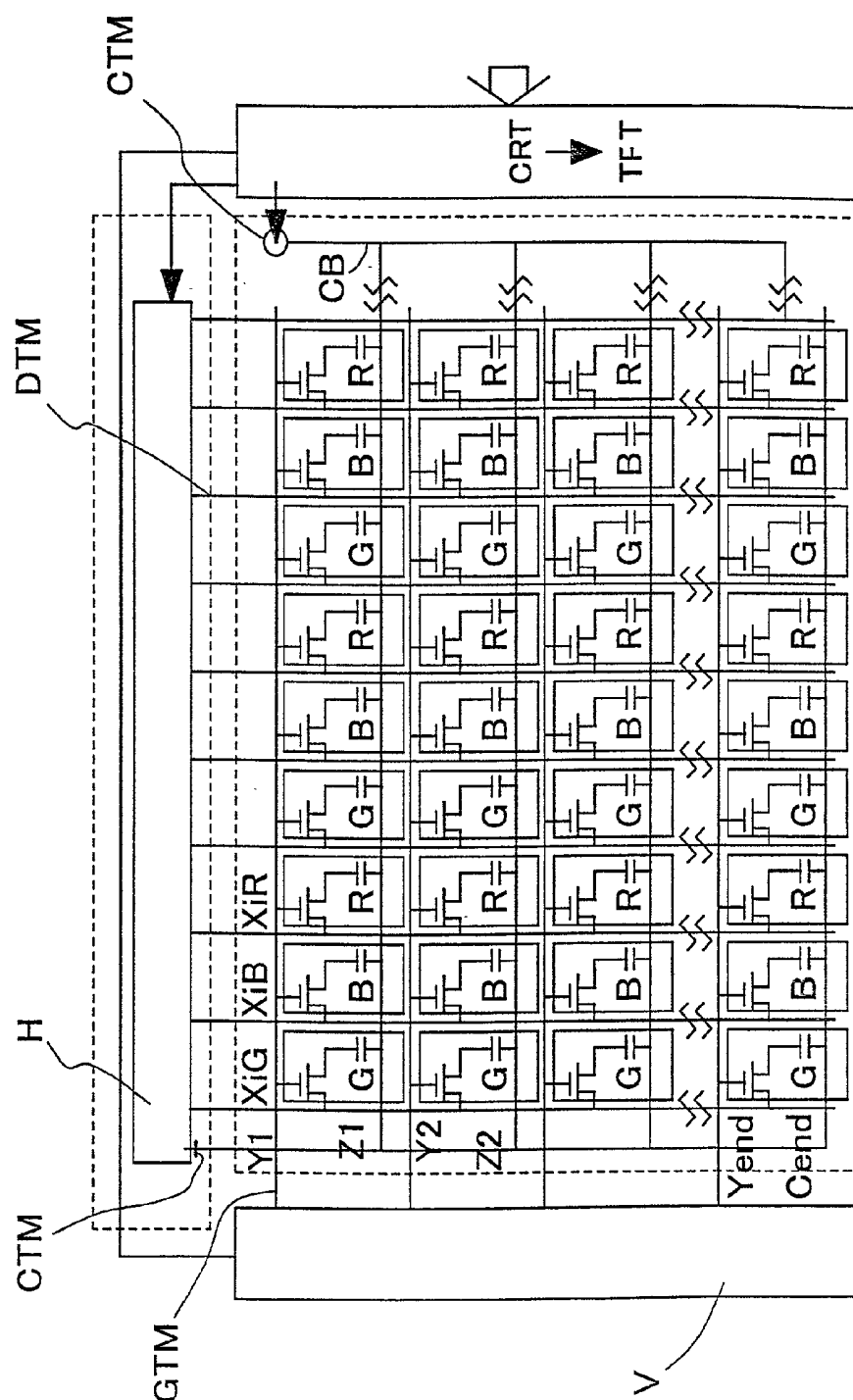


FIG. 8

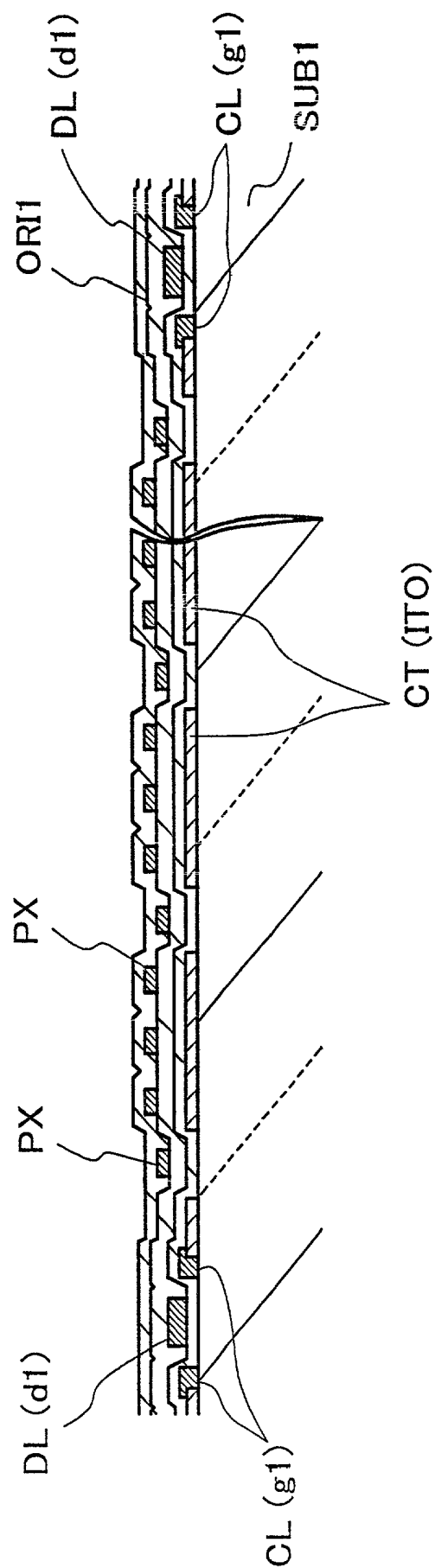
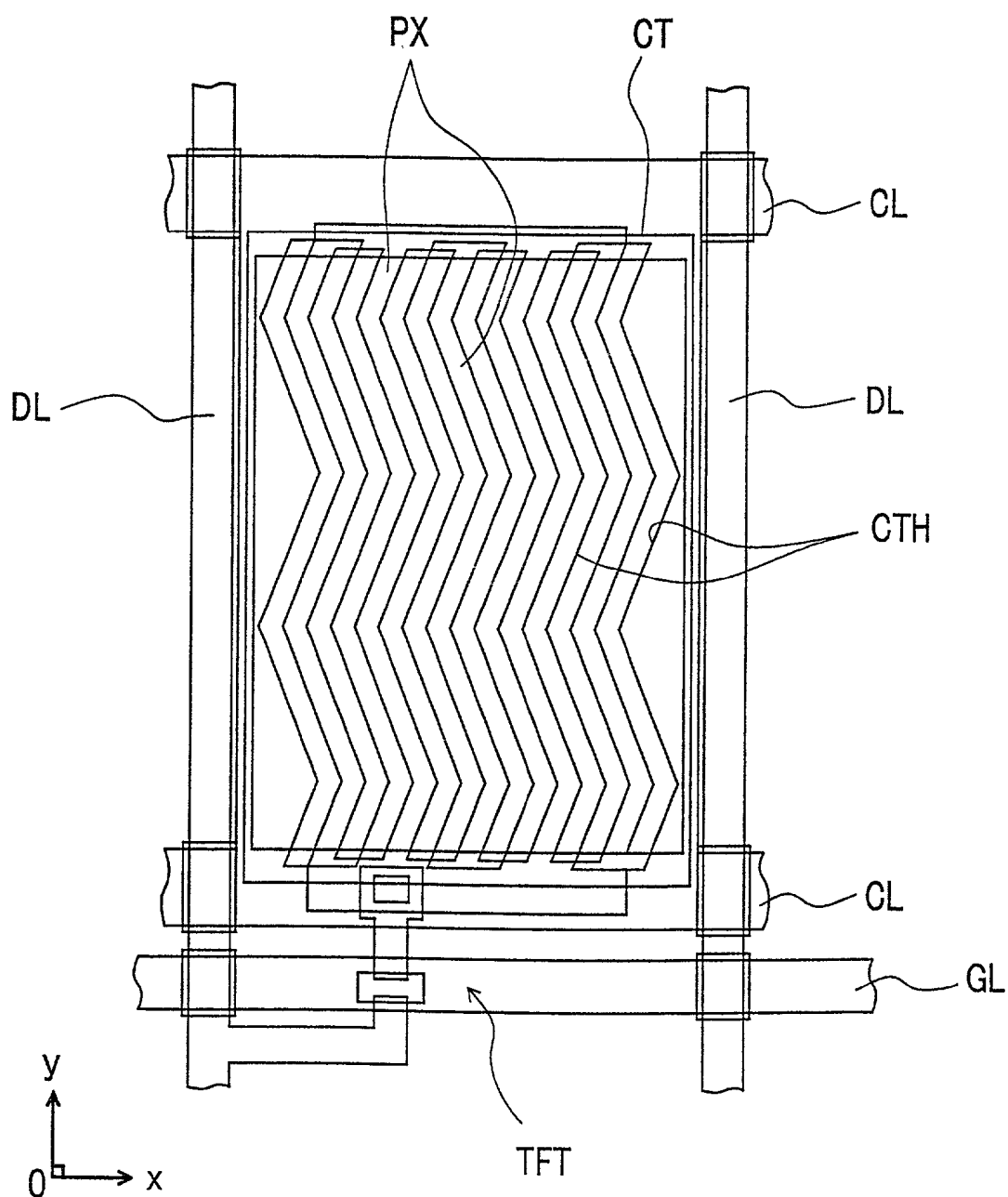


FIG. 9



LIQUID CRYSTAL DISPLAY DEVICE

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] The present application is a continuation application of U.S. Pat. No. 09/760,385, filed on Jan. 11, 2001, which claims priority from Japanese Patent Application No. 2000-003348, filed Jan. 12, 2000, the disclosures of which are incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a liquid crystal display device and, more particularly, to a liquid crystal display device which is called In-Plane Switching Mode.

[0003] Liquid crystal display device which is called In-Plane Switching Mode has a construction in which a pixel electrode and a counter electrode which causes an electric field (an in-plane electric field) having a component parallel to transparent substrates to be generated between the counter electrode and the pixel electrode are formed in each liquid crystal-side pixel area of one of the transparent substrates disposed in opposition to each other with a liquid crystal interposed therebetween.

[0004] This type of liquid crystal display device is constructed so that the amount of light to be transmitted through the area between the pixel electrode and the counter electrode is controlled by the driving of the liquid crystal to which the electric field is applied.

[0005] Such a liquid crystal display device is known as a type which is superior in so-called viewing angle characteristics and enables a displayed image to be unchanged even when its display surface is observed from an oblique direction.

[0006] The pixel electrode and the counter electrode have so far been formed of a metal layer which does not transmit light therethrough.

[0007] In recent years, a liquid crystal display device constructed in the following manner has been known: a counter electrode made of a transparent electrode is formed over the entire area of a pixel area except the periphery thereof, and strip-shaped pixel electrodes are formed on the counter electrode with an insulating film interposed therebetween, in such a manner as to be extended in one direction and to be juxtaposed in a direction traverse to the one direction.

[0008] The liquid crystal display device having this construction causes an in-plane electric field to be generated between each of the pixel electrodes and the counter electrode, and is still superior in viewing angle characteristics and is greatly improved in aperture ratio.

[0009] Incidentally, this art is described, for example, in SID (Society for Information Display) 99 DIGEST: pp. 202-205 and Japanese Patent Laid-Open No. 202356/1999.

[0010] However, in the liquid crystal display device having this construction, the occurrence of so-called horizontal smear is visually observed on its display portion, and the occurrence of image retention is also visually observed.

[0011] It has been found out that the cause of the occurrence of horizontal smear is that the capacitance between the

counter electrode formed over the entire area of the pixel area except the periphery thereof and the plural strip-shaped pixel electrodes formed in juxtaposition on the counter electrode with the insulating film interposed therebetween becomes larger than in previous type and the charge of the pixel electrodes with signal voltages becomes insufficient, and also the voltage of the counter electrode is distorted and the time required for the distorted voltage to be restored to its original state becomes long.

[0012] It has also been found out that the cause of the occurrence of image retention is that an electric field other than an electric field which has a component parallel to the substrate between the pixel electrode and the counter electrode and contributes to the control of the optical transmissivity of the liquid crystal, i.e., an electric field having a component perpendicular to the substrate between the counter electrode and the pixel electrode, is excessively strong.

SUMMARY OF THE INVENTION

[0013] The present invention has been made on the basis of the above-described situations, and provides a liquid crystal display device which can restrain the occurrence of horizontal smear.

[0014] The present invention also provides a liquid crystal display device which can restrain the occurrence of image retention.

[0015] A representative aspect of the invention disclosed in the present application will be described below in brief.

[0016] In one embodiment, a liquid crystal display device includes a first substrate and a second substrate facing the first substrate. A liquid crystal layer is provided between the first and second substrates. First and second gate lines are extending in a first direction, and first and second drain lines are extending in a second direction. A pixel area is defined by the gate lines and drain lines. A counter electrode assigned to the pixel area and having a hollow portion is provided adjacent to a solid portion. The hollow and solid portions are extending in the second direction. One hollow portion is provided after N number of the solid portions, the N being a number equal to or greater than 3. A pixel electrode is assigned to the pixel area and is opposing the counter electrode. The pixel electrode has a connecting portion extending in the first direction and first and second extending portions extending in the second direction. The connection portion connects the first and second extending portions, wherein the first extending portion is vertically aligned to the hollow portion of the counter electrode and the second extending portion is vertically aligned to the solid portion of the counter electrode. An insulating layer is provided between the counter and pixel electrodes.

[0017] In one embodiment, a liquid crystal display device according to the present invention includes a pair of substrates, a liquid crystal layer interposed between the pair of substrates, a plurality of pixel parts being constructed with a plurality of gate lines and a plurality of drain lines arranged in a matrix on one of the pair of substrates, at least one pair of the first electrodes and the second electrodes provided for each pixel part between one of the pair of substrates and the liquid crystal layer, wherein the first electrode and the second electrode being disposed with an insulating film

interposed therebetween, and the second electrode is transparent electrode formed in a rectangular shape and having a slit formed in a portion which is superposed on the first electrodes.

[0018] In the liquid crystal display device constructed in this manner, the selected ones of the plural electrodes of the other electrode (for example, pixel electrodes) are formed not to be superposed on the one of the pair of electrodes (for example, a counter electrode).

[0019] Accordingly, it is possible to decrease the capacitance occurring between the pixel electrode and the counter electrode, whereby it is possible to restrain the occurrence of horizontal smear.

[0020] In addition, it is possible to weaken an electric field other than an electric field which contributes to the control of the optical transmissivity of the liquid crystal, i.e., an electric field having a component perpendicular to the substrate between the counter electrode and the pixel electrode, from among electric fields occurring between the pixel electrode and the counter electrode, whereby it is possible to restrain the occurrence of image retention.

[0021] Moreover, since the holes formed in the other-side electrode are disposed with respect to one-side electrodes that are not adjacent to one another, the holes are formed with a comparatively large space, whereby the holes have the advantage of being easily worked.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The present invention will be more apparent from the following detailed description, when taken in conjunction with the accompanying drawings, in which:

[0023] **FIG. 1** is a plan view showing one embodiment of a pixel of a liquid crystal display device according to the present invention;

[0024] **FIG. 2** is a cross-sectional view taken along line 2-2 of **FIG. 1**;

[0025] **FIG. 3** is a cross-sectional view taken along line 3-3 of **FIG. 1**;

[0026] **FIG. 4** is a cross-sectional view taken along line 4-4 of **FIG. 1**;

[0027] **FIG. 5** is an explanatory view showing the positional relationship between pixel electrodes and holes formed in a counter electrode of the liquid crystal display device according to the present invention;

[0028] **FIG. 6** is a plan view showing one embodiment of the whole of the liquid crystal display panel of the liquid crystal display device according to the present invention;

[0029] **FIG. 7** is a view showing the equivalent circuit of the liquid crystal panel according to the present invention;

[0030] **FIG. 8** is a cross-sectional view showing another embodiment of the liquid crystal display device according to the present invention; and

[0031] **FIG. 9** is a plan view showing another embodiment of the liquid crystal display device according to the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

[0032] Preferred embodiments of the liquid crystal display device according to the present invention will be described below.

[0033] [Embodiment 1]

[0034] <<Construction of Pixel>>

[0035] **FIG. 1** is a plan view showing the construction of a pixel area of a liquid crystal display device (panel) according to the present invention as viewed from the liquid-crystal side of one of transparent substrates disposed in opposition to each other with a liquid crystal interposed therebetween.

[0036] **FIG. 2** is a cross-sectional view taken along line 2-2 of **FIG. 1**, **FIG. 3** is a cross-sectional view taken along line 3-3 of **FIG. 1**, and **FIG. 4** is a cross-sectional view taken along line 4-4 of **FIG. 1**.

[0037] Referring first to **FIG. 1**, gate signal lines GL are disposed to be extended in the x-direction of **FIG. 1** and to be juxtaposed in the y-direction of **FIG. 1**, and the gate signal lines GL are formed of, for example, chromium (Cr). These gate signal lines GL form a rectangular area together with drain signal lines DL which will be described below, and the area constitutes a pixel area.

[0038] A counter electrode CT which generates an electric field between the counter electrode CT and pixel electrodes PX which will be described below are formed in this pixel area. This counter electrode CT is formed in the central portion of the pixel area except the periphery thereof, and is made of, for example, ITO1 (Indium-Tin-Oxide) which forms a transparent conductive layer.

[0039] As will be described later in detail, the plural pixel electrodes PX are formed in juxtaposition, and the counter electrode CT is formed in such a manner as to be superposed on the plural pixel electrodes PX with an insulating film GI interposed therebetween. Holes CTH are respectively formed in the portions of the counter electrode CT that are superposed on every other one of the pixel electrodes PX.

[0040] A counter voltage signal line CL is formed to be connected to the counter electrode CT in such a manner as to border the entire periphery thereof. This counter voltage signal line CL is formed integrally with counter voltage signal lines CL which are similarly formed at the respective counter electrodes CT in the right and left pixel areas as viewed in **FIG. 1** (i.e., the corresponding one of the pixel areas arrayed along the gate signal lines GL).

[0041] In this case, the counter voltage signal lines CL are connected to one another at each of locations above and below the pixel areas. This construction is intended to minimize the portion of superposition of each of the counter voltage signal lines CL and the adjacent one of the drain signal lines DL which will be described later, thereby reducing the capacitance generated therebetween.

[0042] Each of these counter voltage signal lines CL is formed of an opaque material made of, for example, chromium (Cr). In this case, even if an electric field which acts as noise is generated between any of the drain signal lines DL which will be described later and the periphery of the adjacent one of the counter electrodes CT and the optical

transmissivity of the liquid crystal is not obtained as desired, that portion is shielded by the counter voltage signal line CL, whereby it is possible to solve a problem in terms of display quality.

[0043] This also means that it is possible to solve a problem due to an electric field (noise) which is generated between any of the gate signal lines GL and the periphery of the adjacent one of the counter electrodes CT.

[0044] In addition, as described above, since the material of the counter voltage signal lines CL is identical to that of the gate signal lines GL, the counter voltage signal lines CL and the gate signal lines GL can be formed in the same process, whereby it is possible to avoid an increase in the number of manufacturing steps.

[0045] It goes without saying that the material of the counter voltage signal lines CL is not limited to Cr and the counter voltage signal lines CL may be formed of, for example, Al or a material which contains Al.

[0046] In this case, it is effective to position the counter voltage signal lines CL as a layer which overlies the counter electrodes CT. This is because Al is easily melted by an etching solution (for example, HBr) for selectively etching an ITO film which constitutes the counter electrodes CT.

[0047] Furthermore, it is effective to interpose a high melting point metal such as Ti, Cr, Mo, Ta or W at least the interface between each of the counter voltage signal lines CL and the adjacent one of the counter electrodes CT. This is because ITO which constitutes the counter electrodes CT oxidizes Al of the counter voltage signal lines CL and generates a high-resistance layer.

[0048] For this reason, as one example, if the counter voltage signal lines CL made of Al or a material which contains Al are to be formed, it is preferable to form each of the counter voltage signal lines CL as a multilayered structure having a first layer made of the high melting point metal.

[0049] In this manner, the counter electrodes CT, the counter voltage signal lines CL and the gate signal lines GL are formed over the transparent substrate, and the insulating film GI made of, for example, SiN is formed over the transparent substrate in such a manner as to cover all of the counter electrodes CT, the counter voltage signal lines CL and the gate signal lines GL.

[0050] The insulating film GI has the function of an interlayer insulating film for insulating the drain signal lines DL from the counter voltage signal lines CL and the gate signal lines GL. The insulating film GI also has the function of a gate insulating film in each area in which a thin film transistor TFT which will be described below is formed, as well as the function of a dielectric film in each area in which a capacitance element Cstg which will be described below is formed.

[0051] The thin film transistor TFT is formed to be superposed on a portion of the gate signal line GL (the bottom left portion of FIG. 1), and in this portion, a semiconductor layer AS made of, for example, amorphous silicon (a-Si) is formed on the insulating film GI.

[0052] A source electrode SD1 and a drain electrode SD2 are formed on the upper surface of the semiconductor layer

AS, whereby an inverted staggered structure MIS transistor is formed which uses a portion of the gate signal line GL as its gate electrode. The source electrode SD1 and the drain electrode SD2 are formed at the same time as the drain signal line DL.

[0053] Specifically, the drain signal lines DL which are disposed to be extended in the y-direction of FIG. 1 and to be juxtaposed in the x-direction of FIG. 1 are formed, and a portion of an adjacent one of the drain signal lines DL is extended to the surface of the semiconductor layer AS and constitutes the drain electrode SD2 of the thin film transistor TFT.

[0054] During the formation of the adjacent drain signal line DL, the source electrode SD1 is formed, and this source electrode SD1 is extended to the inside of the pixel area, thereby integrally forming a contact portion which provides connection between the thin film transistor TFT and the pixel electrode PX which will be described below.

[0055] As shown in FIG. 3, a contact layer d0 which is doped with, for example, an n type impurity is formed at the interface between the source electrode SD1 and the drain electrode SD2 of the semiconductor layer AS.

[0056] This contact layer d0 is formed by forming an n type impurity-doped layer over the entire surface of the semiconductor layer AS, and, after forming the source electrode SD1 and the drain electrode SD2, etching the n type impurity-doped layer on the portion of the surface of the semiconductor layer AS that is exposed between these electrodes SD1 and SD2, by using each of these electrodes SD1 and SD2 as a mask.

[0057] In Embodiment 1, the semiconductor layer AS is formed not only in the area in which the thin film transistor TFT is formed, but also at the intersection of the drain signal line DL and the gate signal line GL and at the intersection of the drain signal line DL and the counter voltage signal line CL. This construction is intended to strengthen the function of the interlayer insulating film.

[0058] A protective film PSV covers the thin film transistor TFT formed over the surface of a transparent substrate SUB1 on which the thin film transistor TFT is formed. The protective film is generally made of a dielectric material, for example, SiN. The protect film prevents the thin film transistor TFT from coming into direct contact with the liquid crystal LC.

[0059] Furthermore, the pixel electrode PX which is made of a transparent conductive film are formed over the upper surface of the protective film PVS. The pixel electrode PX is generally made of a conductive material, for example, Indium-Tin-Oxide (ITO).

[0060] In Embodiment 1, five pixel electrodes PX are formed to be superposed on an area in which the counter electrode CT is formed, and are also formed to be extended in the y direction of FIG. 1 and to be equidistantly spaced apart from one another. Both ends of each of the five pixel electrodes PX are connected to the respective ends of the adjacent one by layers made of the same material which is formed to be extended in the x direction of FIG. 1.

[0061] In this construction, three pixel electrodes PX which are respectively disposed at the first, third and fifth

positions as viewed from the left side of **FIG. 1** are positioned in the respective holes CTH formed in the counter electrode CT.

[0062] Specifically, within a substantial pixel area, i.e., within the aperture of a black matrix, each of the first, third and fifth pixel electrodes PX is formed without being superposed on the counter electrode CT, and the other pixel electrodes PX which are respectively disposed at the second and fourth positions as viewed from the left side of **FIG. 1** are formed to be superposed on the counter electrode CT.

[0063] In the case where the pixel electrodes PX are formed in this manner, since the area of superposition of the pixel electrodes PX and the counter electrodes CT can be decreased, the capacitance between the pixel electrodes PX and the counter electrodes CT can be decreased, whereby it is possible to decrease the occurrence of so-called horizontal smear.

[0064] In this construction, the holes CTH are formed in the counter electrode CT in such a manner as to correspond to every other one of the pixel electrodes PX. This construction is intended to facilitate the working of the holes CTH by increasing the spaces between the adjacent holes CTH.

[0065] In Embodiment 1, the number of pixel electrodes PX per pixel area is five, but there actually are cases in which dozens of pixel electrodes are formed per pixel area. In such a case, the holes CTH may be formed at positions which correspond to not only every other one of the pixel electrodes PX but also every third one, every fourth one and so on, whereby it is possible to achieve far easier working of the holes CTH.

[0066] **FIG. 8** is a view which shows such a construction and corresponds to **FIG. 2**. In the construction shown in **FIG. 8**, the holes CTH are formed in the counter electrode CT which underlies the juxtaposed multiple pixel electrodes PX, at positions which correspond to every fourth one of the pixel electrodes PX.

[0067] In addition, in this embodiment, the central axis of every fourth one of the pixel electrodes PX agrees with that of the corresponding one of the holes CTH formed in the counter electrode CT, and each of the holes CTH is formed to have a width larger than the corresponding one of the pixel electrodes PX.

[0068] **FIG. 5** is a cross-sectional view (which corresponds to the cross-sectional view of **FIG. 2**) showing the positional relationship between the pixel electrodes PX and the holes CTH formed in the counter electrode CT.

[0069] As can be seen from **FIG. 5**, each of the counter electrodes CT which are separated by the formation of the holes CTH (but are connected for electrical connection at their opposite peripheral ends) is formed to be superposed on pixel electrodes PX(2) adjacent to a pixel electrode PX(1) which is one of the pixel electrodes PX, and to be extended to the area between each of the pixel electrodes PX(2) and the pixel electrode PX(1) as viewed in the direction of juxtaposition of the pixel electrodes PX. Thus, each of the counter electrodes CT is formed to have an area superposed on the pixel electrode PX(1) and widths W.

[0070] The widths W are mainly determined from the point of view of decreasing an electric field other than an electric field which contributes to the control of the optical

transmissivity of the liquid crystal between the pixel electrode PX and the counter electrode CT, that is to say, an electric field which has a component perpendicular to the substrate between the counter electrode CT and the pixel electrode PX. Accordingly, it is appropriate to make each of the widths W smaller than the separation distance between the pixel electrode PX(1) and each of the pixel electrodes PX(2) adjacent to the pixel electrode PX(1).

[0071] The widths W are preferably as wide as possible, but slightly smaller than the respective separation distances.

[0072] In other words, the peripheral outline portion of the counter electrode CT has only to lie at the intermediate position between the pixel electrode PX(1) and each of the pixel electrodes PX(2) adjacent to the pixel electrode PX(1), and the counter electrode CT has to be wider than the pixel electrode PX(1), preferably slightly wider.

[0073] The reason for this is that the existence of the widths W makes it possible to strengthen an electric field having a component approximately parallel to the transparent substrate in each pixel area and to decrease an electric field which occurs in a direction perpendicular to the substrate and adversely affects the phenomenon of image retention. In addition, as the widths W are made larger, the absorption loss of light due to transparent electrodes becomes smaller and higher optical transmissivity can be obtained.

[0074] The bottom-end same-material layer of each of the pixel electrodes PX which are formed in this manner is connected to a contact portion of the source electrode SD1 of the thin film transistor TFT through a contact hole formed in the protective film PSV. The top-end same-material layer is formed to be superposed on the counter voltage signal line CL.

[0075] In the case of this construction, a capacitance element Cstg which uses as a dielectric film a stacked film made of the insulating film GI and the protective film PSV is formed in the portion of superposition of the counter electrode CT and each of the pixel electrodes PX.

[0076] This capacitance element Cstg is formed for purposes such as storing a video signal in the pixel electrode PX for a comparatively long period even if the thin film transistor TFT is turned off after the video signal from the drain signal line DL is applied to the pixel electrode PX via the thin film transistor TFT.

[0077] An alignment film ORI1 which covers the pixel electrodes PX is formed over the surface of the transparent substrate SUB1 over which the pixel electrodes PX are formed in the above-described manner. This alignment film ORI1 is a film which is in direct contact with the liquid crystal LC and determines the initial alignment direction of the liquid crystal LC.

[0078] Incidentally, in Embodiment 1, the initial alignment direction is made 75° with respect to the direction of application of an electric field. The initial alignment direction is not limited to 75°, and may be greater than 0° and less than 90°, preferably 10° to 80° so that high-speed responses (drivable at low voltages) can be achieved.

[0079] In the above-described embodiment, the gate signal lines GL, the counter voltage signal lines CL and the drain signal lines DL are formed of chromium (Cr). However, it

goes without saying that another high melting point metal such as Mo, W, Ti or Ta or an alloy of two or more kinds of such metals or a stacked film made of two or more kinds of such metals may also be used.

[0080] Moreover, although in the above description the transparent conductive film is made of ITO, it goes without saying that similar advantages can be obtained even with IZO (Indium-Zinc-Oxide).

[0081] The transparent substrate constructed in this manner is called a TFT substrate, and a transparent substrate disposed in opposition to this TFT substrate with the liquid crystal LC interposed therebetween is called a filter substrate.

[0082] <<Filter Substrate>>

[0083] As shown in FIG. 2, on the liquid crystal-side surface of the filter substrate, a black matrix BM is formed to separate the pixel areas from one another, and a filter FIL is formed to cover each aperture of the black matrix BM that determines a substantial pixel area.

[0084] An overcoat layer OC made of, for example, a resin layer is formed to cover the black matrix BM and the filter FIL, and an alignment layer ORI2 is formed on the overcoat layer OC.

[0085] The alignment direction of the alignment layer ORI2 is selected to be the same as that of the alignment film ORI1 when the alignment film ORI1 is superposed on the alignment layer ORI1. That is to say, the alignment of the molecules of the liquid crystal LC is made homogeneous.

[0086] <<Liquid Crystal Layer>>

[0087] In Embodiment 1, a liquid crystal having a dielectric anisotropy $\Delta\epsilon$ of, for example, -5 is used, whereby it is possible to obtain a high optical transmissivity. This is because the directors of the liquid crystal molecules of a liquid crystal of negative $\Delta\epsilon$ do not greatly change due to an electric-field component perpendicular to a substrate surface.

[0088] Embodiment 1 uses a liquid crystal of negative $\Delta\epsilon$, but even if a liquid crystal of positive $\Delta\epsilon$ is used, the effects and advantages of the present invention can similarly be obtained.

[0089] Since the liquid crystal of positive $\Delta\epsilon$ is large in $\Delta\epsilon$ and low in viscosity compared to the liquid crystal of negative $\Delta\epsilon$, the liquid crystal of positive $\Delta\epsilon$ has the advantage of being drivable at lower voltages and at higher response speeds.

[0090] <<Entire Construction of Liquid Crystal Display Panel>>

[0091] FIG. 6 is a view of the entire construction of the liquid crystal display panel, showing a display area AR constructed of an assembly of pixel areas arranged in matrix form.

[0092] A transparent substrate SUB2 is formed to be slightly smaller than the transparent substrate SUB1, and the right and bottom sides (as viewed in FIG. 6) of the transparent substrate SUB2 are disposed to be approximately in flush with the corresponding sides of the transparent substrate SUB1.

[0093] Accordingly, areas which are not covered with the transparent substrate SUB2 are respectively formed along the left and top sides (as viewed in FIG. 5) of the transparent substrate SUB1, and gate signal terminals Tg and drain signal terminals Td are formed in the respect areas. The gate signal terminals Tg are formed for supplying scanning signals to the respective gate signal lines GL, while the drain signal terminals Td are formed for supplying video signals to the respective drain signal lines DL.

[0094] The transparent substrate SUB2 is secured to the transparent substrate SUB1 by a sealing material SL formed along the periphery of the transparent substrate SUB2, and this sealing material SL also has the function of a sealing material for sealing the liquid crystal LC between the transparent substrates SUB1 and SUB2.

[0095] A liquid crystal filling port INJ is disposed in a portion of the sealing material SL, and after the gap between the transparent substrates SUB1 and SUB2 has been filled with the liquid crystal LC through the liquid crystal filling port INJ, the liquid crystal filling port INJ is sealed by a liquid crystal sealing material (not shown).

[0096] Polarizers are respectively stuck to the outside surfaces of the transparent substrates SUB1 and SUB2 in such a manner that the transparent substrates SUB1 and SUB2 are interposed between the polarizers.

[0097] <<Equivalent Circuit>>

[0098] FIG. 7 is a view showing the equivalent circuit of the liquid crystal panel as well as the external circuits of the liquid crystal panel.

[0099] Scanning signals (voltage signals) are sequentially supplied to the individual gate signal lines GL disposed to be extended in the x-direction of FIG. 7 and to be juxtaposed in the y-direction of FIG. 7, by a vertical scanning circuit V.

[0100] The thin film transistors TFT in the respective pixel areas arranged along the one of the gate signal lines GL to which a scanning signal is supplied are turned on by the scanning signal.

[0101] At this timing, video signals are supplied to the individual drain signal lines DL from a video signal driver circuit H, and these video signals are applied to the respective pixel electrodes PX via the thin film transistors of the corresponding pixel areas.

[0102] In the respective pixel areas, counter voltages are applied to the counter electrodes CT formed together with the pixel electrodes PX via the counter voltage signal lines CL, so that electric fields can be generated between the pixel electrodes and the counter electrodes CT.

[0103] The optical transmissivity of the liquid crystal LC is controlled by the ones (in-plane electric fields) of these electric fields each of which has a component parallel to the transparent substrate SUB1.

[0104] Incidentally, in FIG. 7, the symbols R, G and B shown in the individual pixel areas represent that a red filter, a green filter and a blue filter are formed in the respective pixel areas.

[0105] <<Other Embodiments>>

[0106] In the above-described embodiment, the counter electrodes CT are formed below the pixel electrodes PX with

the insulating film GI interposed therebetween. However, the present invention is not limited to this construction, and it goes without saying that the pixel electrodes PX are formed below the counter electrodes CT with the insulating film GI interposed therebetween.

[0107] In the above-described embodiment, the pixel electrodes PX formed in juxtaposition are formed as rectilinear strip-shaped electrodes in the respective pixel areas.

[0108] However, the present invention is not limited to this construction, and it goes without saying that each of the pixel electrodes PX may be an element having one or more bent portions in the direction of extension of the pixel electrode PX.

[0109] Such an electrode is called a multi domain scheme in which the direction of an electric field generated between the electrode and the counter electrode CT is made different to provide the advantage of canceling a difference in the optical transmissivity of a liquid crystal when a display area is viewed in any direction different from the direction normal to its front surface.

[0110] Even in this case, the holes CTH can be formed in the counter electrode CT at locations corresponding to the bent extended portion of the pixel electrode PX.

[0111] FIG. 9 is a plan view which corresponds to FIG. 1, showing an example to which the multi domain scheme is applied.

[0112] Each of the pixel electrodes PX has, for example, a zigzag pattern along its extension direction, and the holes CTH each having a zigzag shape along the zigzag pattern are respectively formed in the counter electrodes CT which are superposed on some of the pixel electrodes PX (for example, every other one of the pixel electrodes PX).

[0113] The extension direction of the pixel electrodes PX is along the y-direction of FIG. 9, but the present invention is not limited to this construction and can, of course, be applied to a construction in which the extension direction of the pixel electrodes PX is along the x-direction of FIG. 9.

[0114] In the above-described embodiment, an electrode which is formed over nearly the whole of the central portion of the pixel area except the periphery thereof serves as the counter electrode CT, while plural strip-shaped electrodes which are juxtaposed in one direction serve as the pixel electrodes PX. However, an electrode which is formed over the central portion of the pixel area except the periphery thereof may be used as the pixel electrode PX, while plural strip-shaped electrodes which are juxtaposed in one direction may be used as the counter electrode CT.

[0115] As is apparent from the foregoing description, in accordance with the liquid crystal display device according to the present invention, it is possible to prevent the occurrence of horizontal smear and image retention.

What is claimed is:

1. A liquid crystal display device comprising:
 - a first substrate;
 - a second substrate facing the first substrate;

a liquid crystal layer provided between the first and second substrates;

first and second gate lines extending in a first direction;

first and second drain lines extending in a second direction;

a pixel area defined by the gate lines and drain lines;

a counter electrode assigned to the pixel area and having a hollow portion provided adjacent to a solid portion, the hollow and solid portions extending in the second direction, wherein one hollow portion is provided after N number of the solid portions, the N being a number equal to or greater than 3;

a pixel electrode assigned to the pixel area and opposing the counter electrode, the pixel electrode having a connecting portion extending in the first direction and first and second extending portions extending in the second direction, the connection portion connecting the first and second extending portions, wherein the first extending portion is vertically aligned to the hollow portion of the counter electrode and the second extending portion is vertically aligned to the solid portion of the counter electrode; and

an insulating layer provided between the counter and pixel electrodes.

2. The display device of claim 1, wherein the counter electrode has a plurality of hollow portions and a plurality of solid portions, and the pixel electrodes have more than two extending portions.

3. The display device of claim 1, wherein the hollow portion has a first width, the solid portion has a second width, the first extending portion has a third width, and the second extending portion has a fourth width, wherein the first, second, third, and fourth widths are distances in the first direction.

4. The display device of claim 3, wherein the first width of the hollow portion is greater than the third and fourth widths of the first and second extending portions.

5. The display device of claim 4, wherein the first and second extending portions are separated by a first distance, and an edge of the hollow portion extends beyond an edge of the first extending portion by a second distance in the first direction, wherein the first distance is greater than the second distance.

6. The display device of claim 5, wherein the second distance is as great as possible without being greater than the first distance, in order to obtain higher optical transmissivity.

7. The display device of claim 5, wherein an edge of the solid portion in the first direction is provided within a space between the first and second extending portions to strengthen an electric field substantially parallel to the first substrate and weaken an electric field substantially perpendicular to the first substrate.

8. The display device of claim 3, wherein the second width of the solid portion is greater than the third and fourth widths of the first and second extending portions.

9. The display device of claim 1, wherein the N is an integer.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US20010012086A1	公开(公告)日	2001-08-09
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摘要(译)

一种液晶显示装置，包括第一基板和面向第一基板的第二基板。在第一和第二基板之间提供液晶层。第一和第二栅极线沿第一方向延伸，第一和第二漏极线沿第二方向延伸。像素区域由栅极线和漏极线限定。分配给像素区域并具有中空部分的对电极邻近实心部分设置。中空和实心部分沿第二方向延伸。在N个实心部分之后提供一个中空部分，N是等于或大于3的数。像素电极被分配给像素区域并且与对电极相对。像素电极具有沿第一方向延伸的连接部分和沿第二方向延伸的第一和第二延伸部分。连接部分连接第一和第二延伸部分，其中第一延伸部分垂直地对准对电极的中空部分，第二延伸部分垂直地对准对电极的实心部分。在计数器电极和像素电极之间提供绝缘层。

