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(54) **LIQUID CRYSTAL DISPLAY**

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*C09K 19/02* (2006.01)

(52) **U.S. Cl.** ..... **349/38**; 349/167

(57) **ABSTRACT**

A liquid crystal display includes a thin film transistor, a liquid crystal capacitor, which is electrically connected to the thin film transistor and includes a liquid crystal layer, and a storage capacitor, which is electrically connected to the thin film transistor in parallel to the liquid crystal capacitor, wherein the liquid crystal layer has a positive dielectric anisotropy and is disposed in a twisted nematic mode, and a capacitance ratio of a capacitance of the storage capacitor to a capacitance of the liquid crystal capacitor is approximately 0.4 or more.

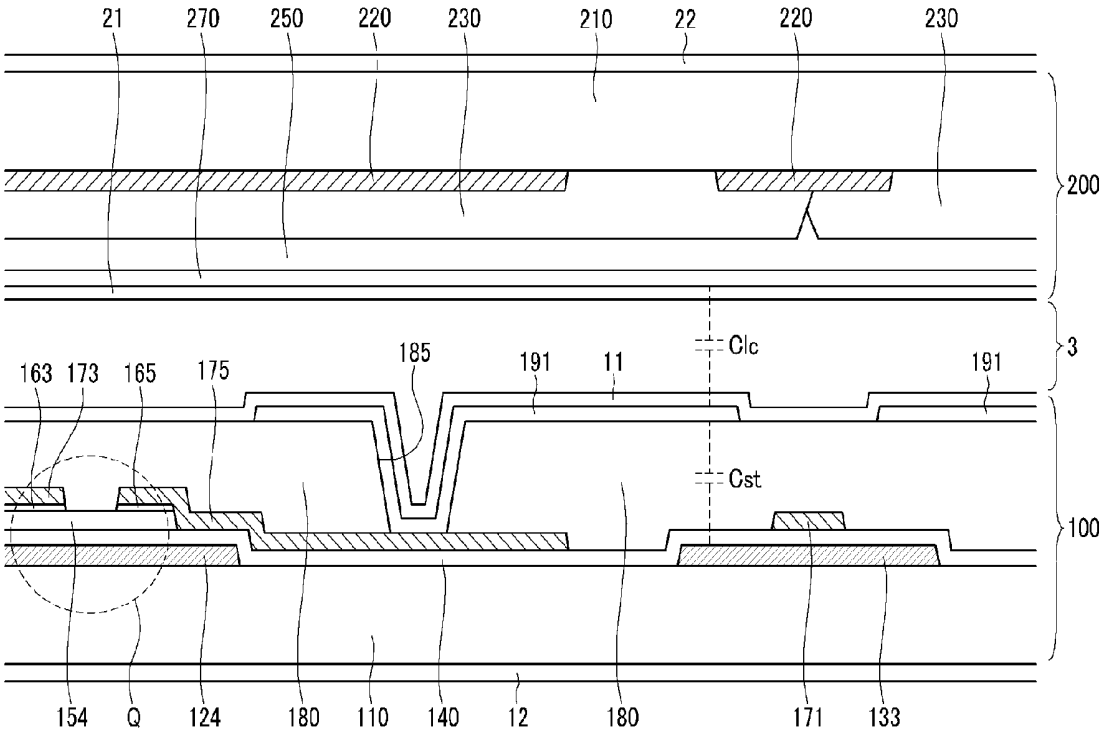


FIG. 1

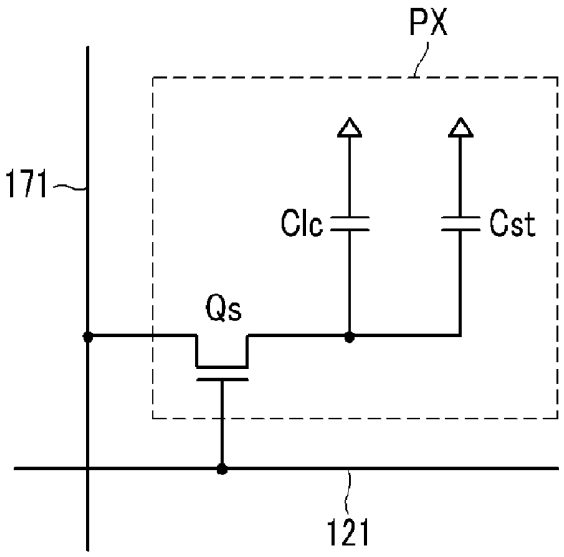

PX
171
Clc
Cst
Qs
121

FIG. 2

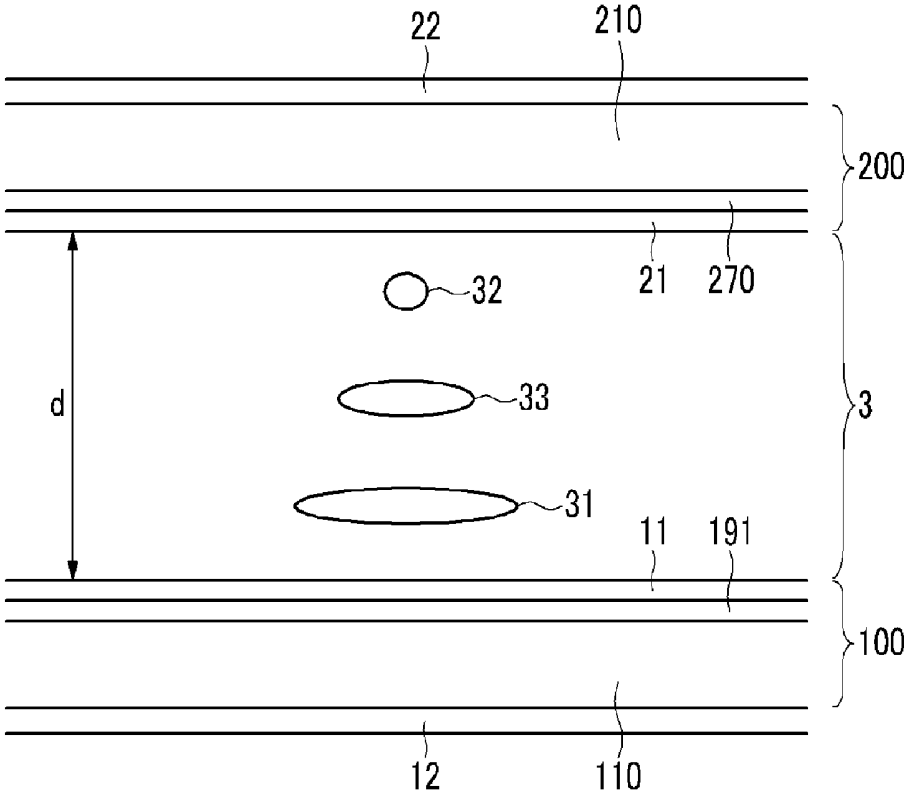

22
210
200
21
270
32
d
33
3
31
11
191
100
12
110

FIG. 3

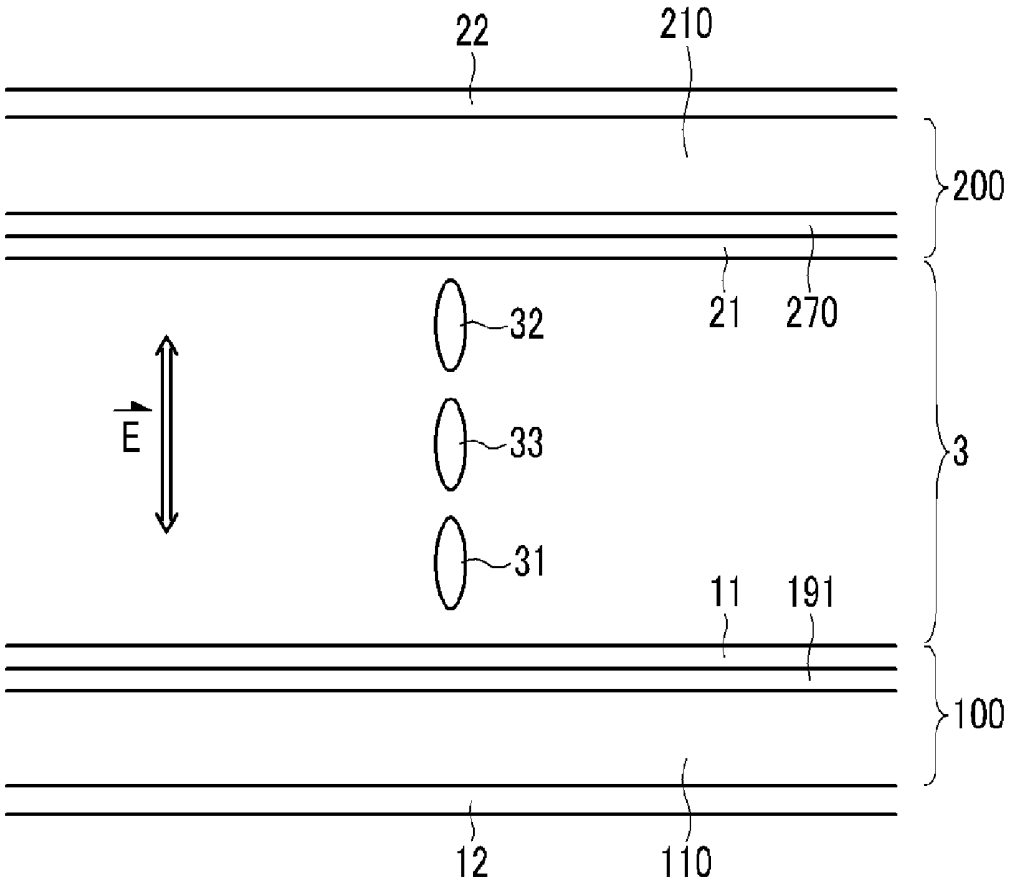


FIG. 4

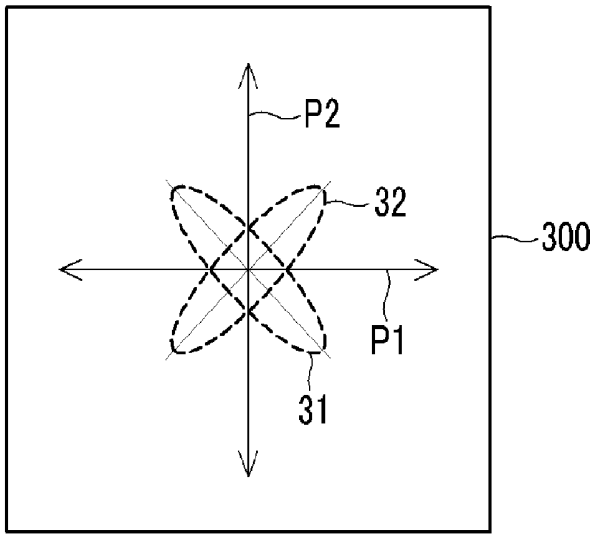



FIG. 5

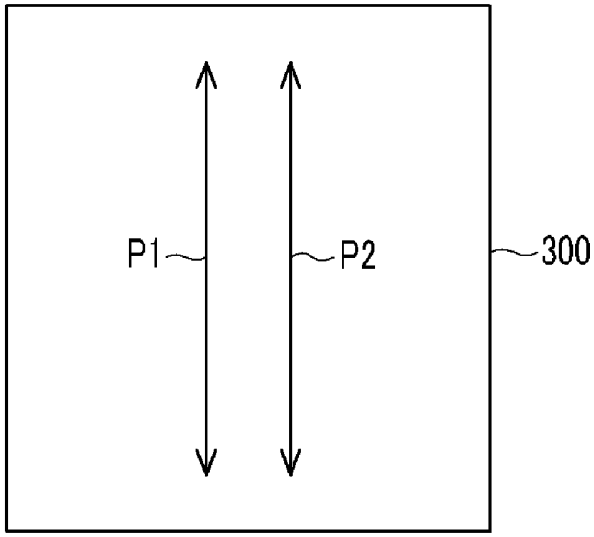


FIG. 6

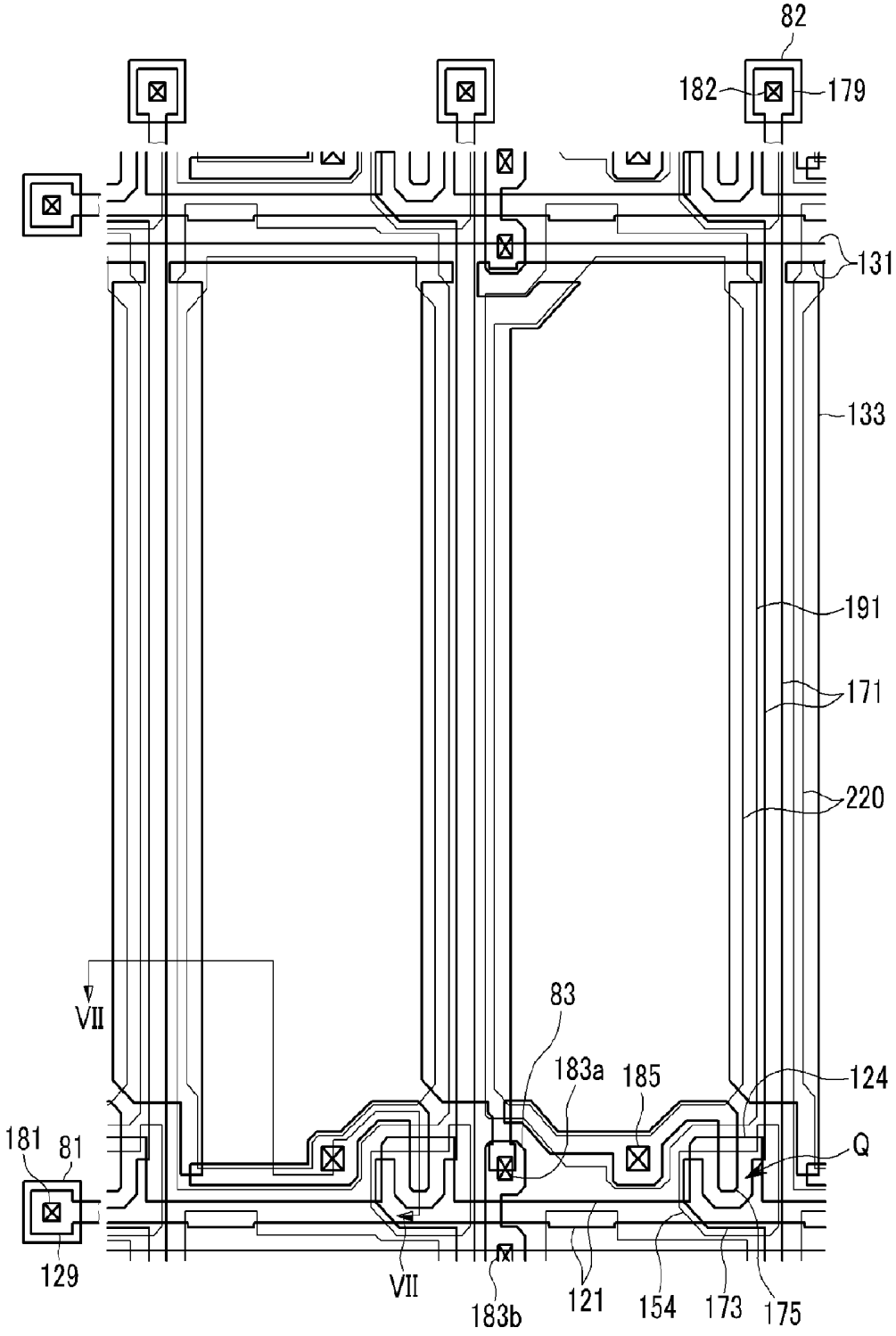
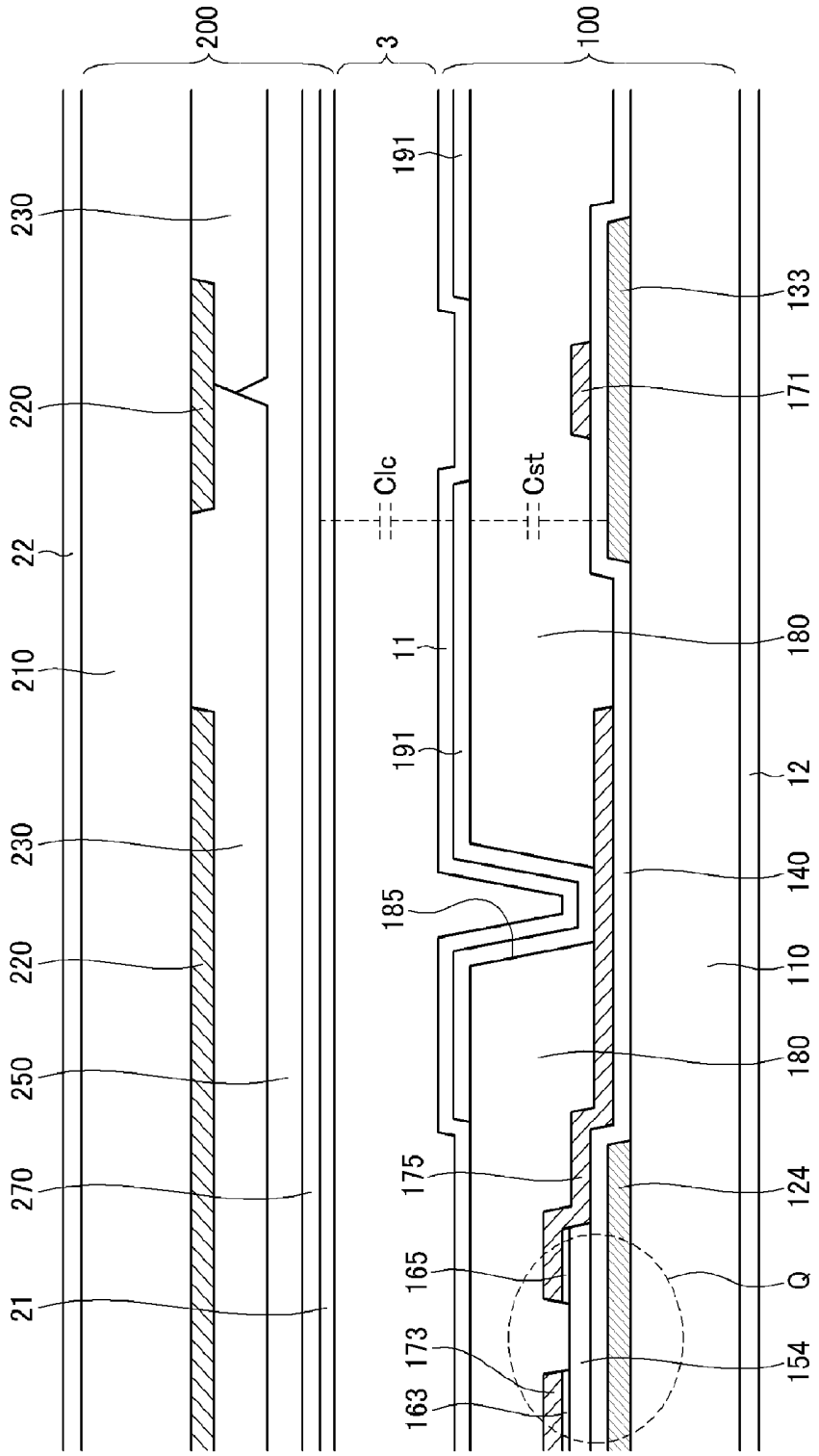

82
182
179
131
133
191
171
220
VII
83
183a
185
124
Q
181
81
129
VII
183b
121
154
173
175

FIG. 7


200
3
100
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220
22
210
230
220
250
270
21
191
Clc
Cst
11
191
185
175
165
173
163
133
171
180
12
140
110
180
124
Q
154

FIG. 8A

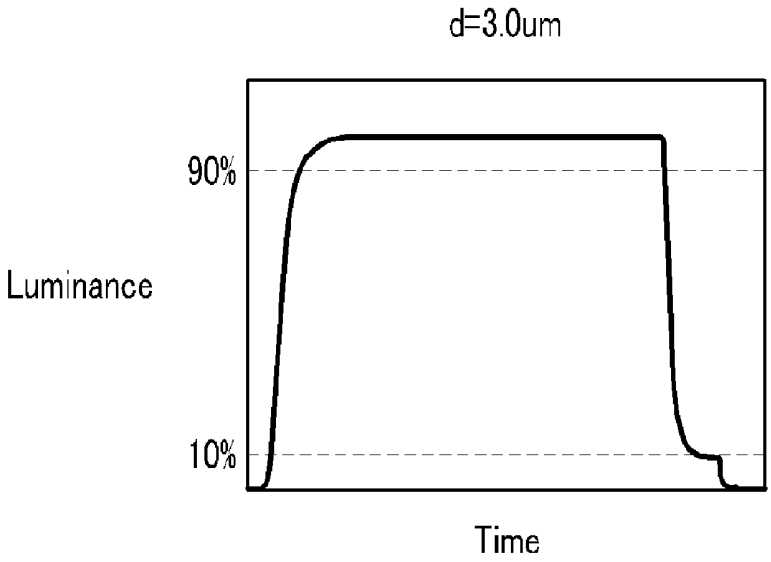



FIG. 8B

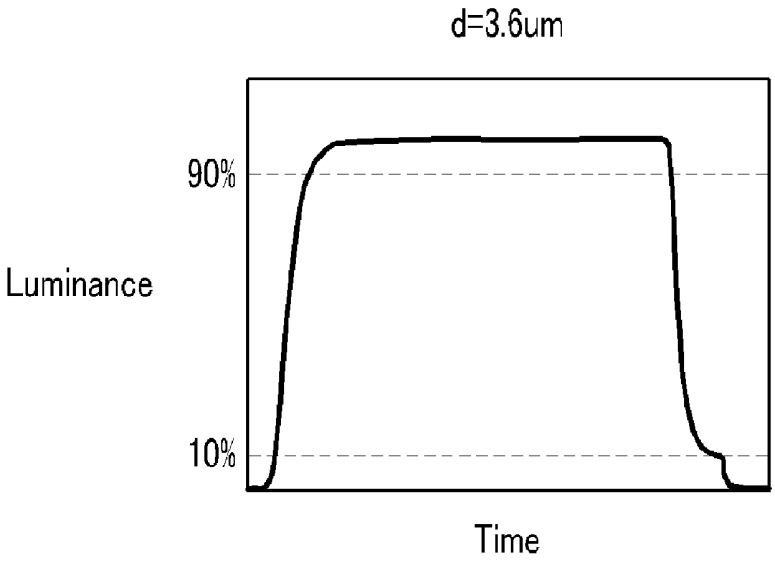


FIG. 8C

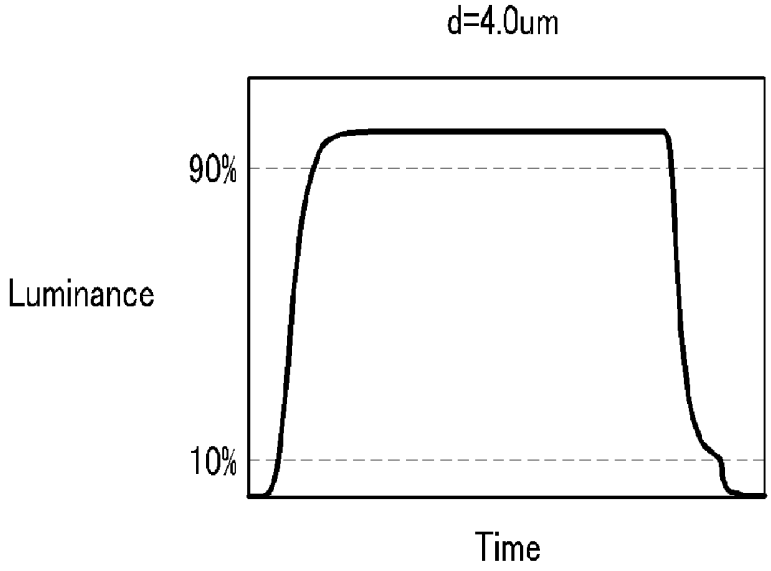



FIG. 9A

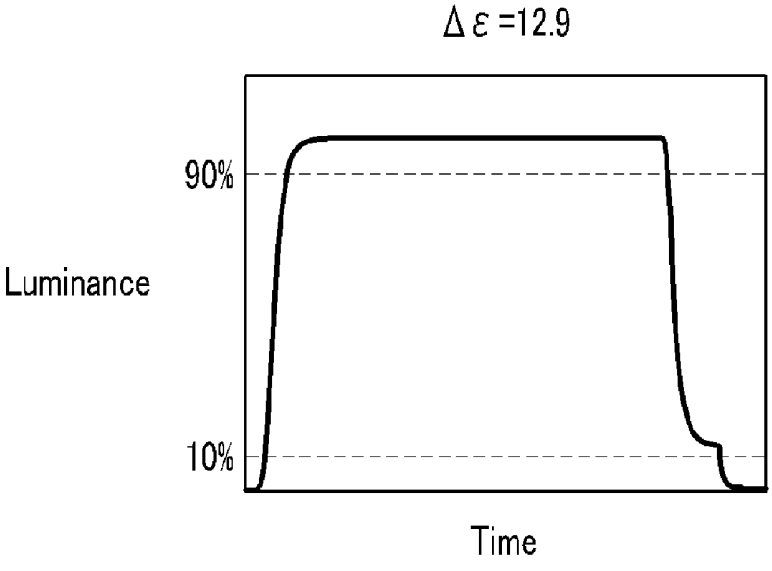


FIG. 9B

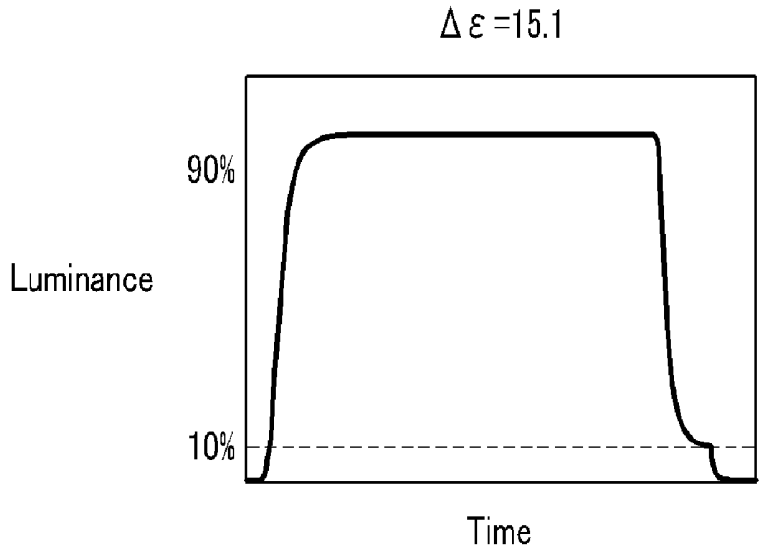



FIG. 9C

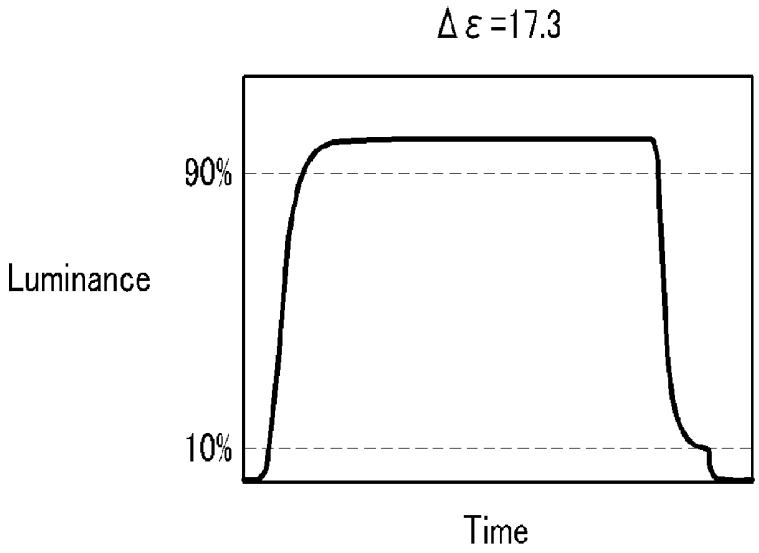


FIG. 10

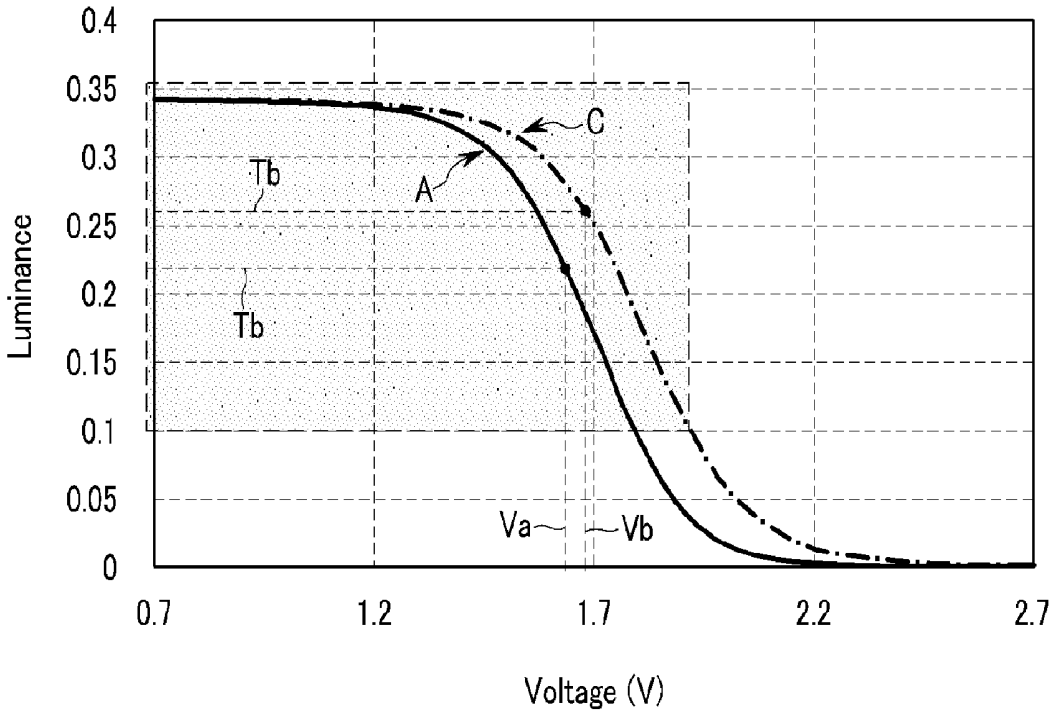

0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
Luminance
Tb
Tb
A
C
Va
Vb
0.7
1.2
1.7
2.2
2.7
Voltage (V)

FIG. 11A

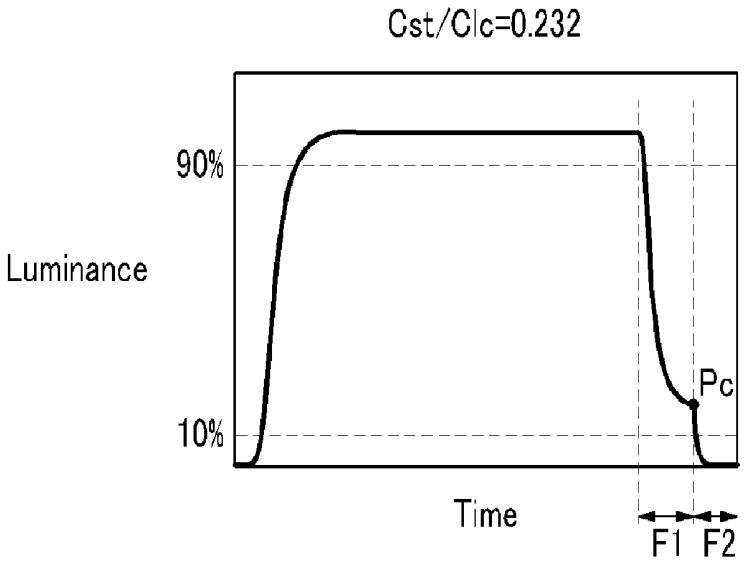



FIG. 11B

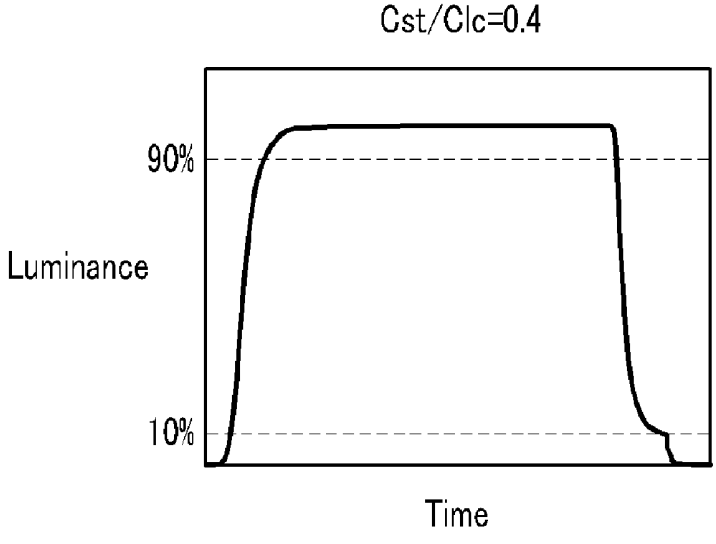


FIG. 11C

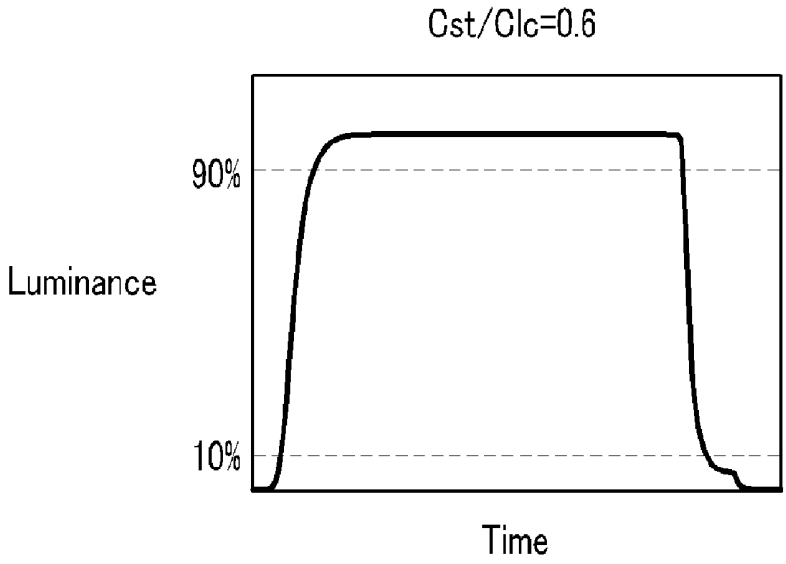



FIG. 12A

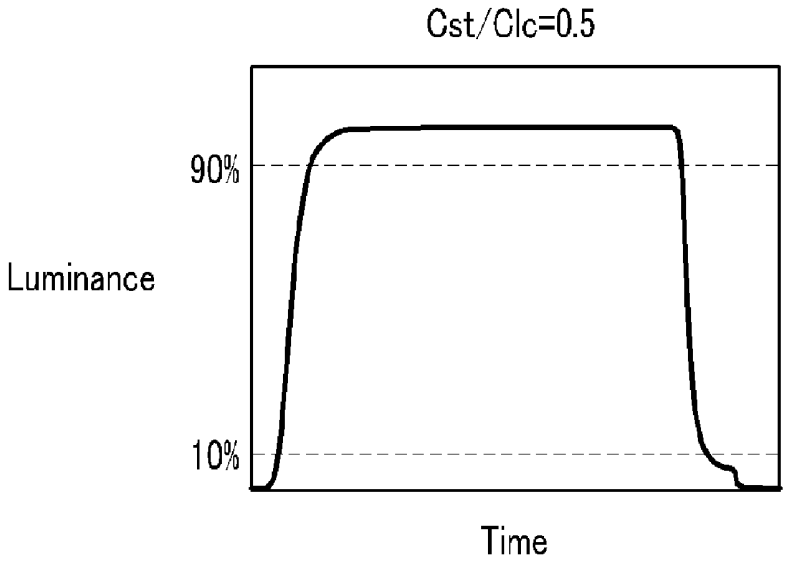


FIG. 12B

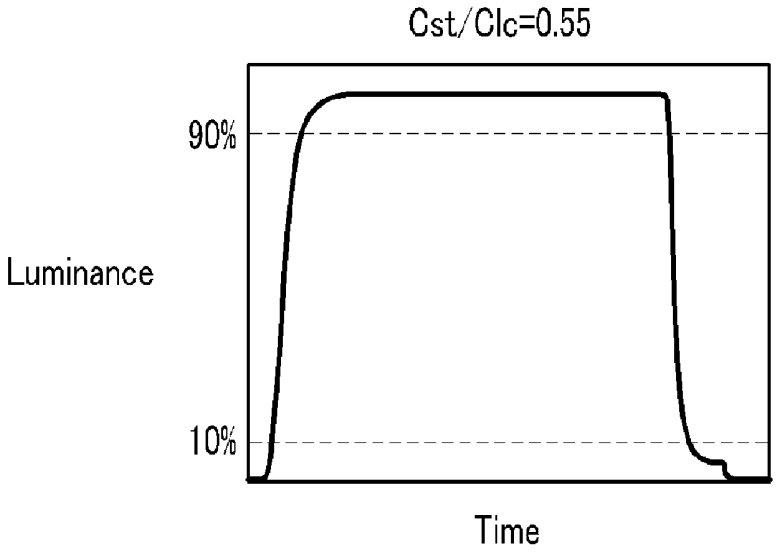



FIG. 12C

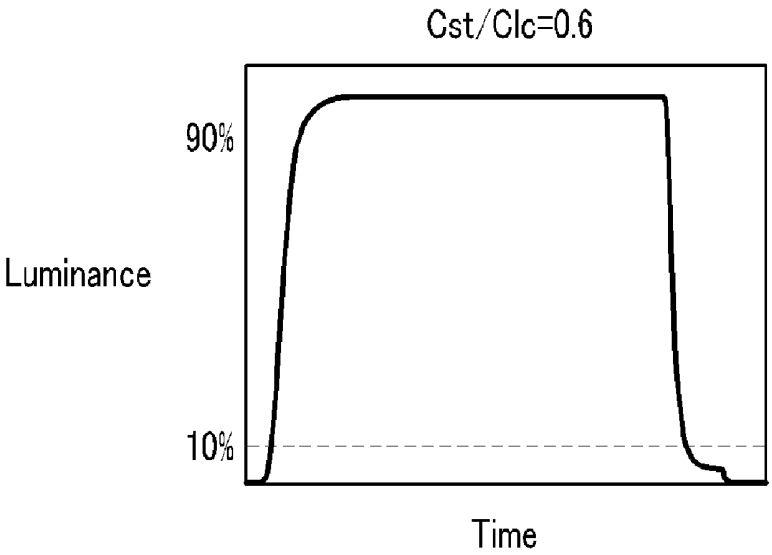


FIG. 13A

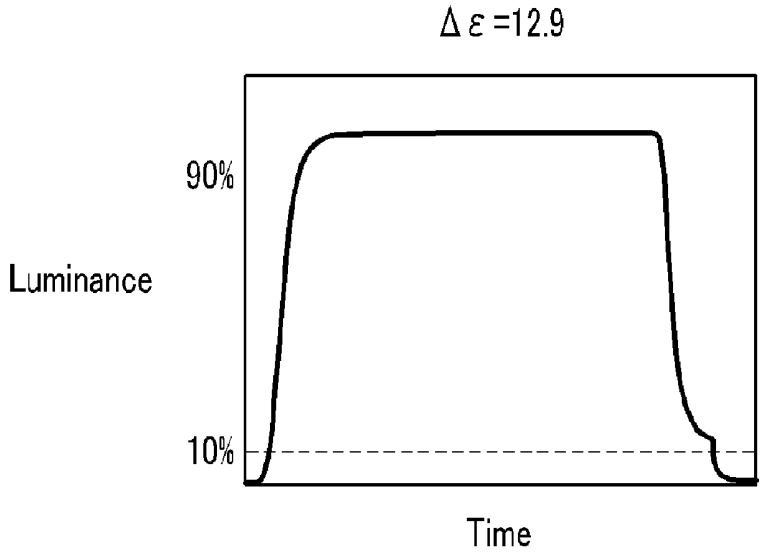



FIG. 13B

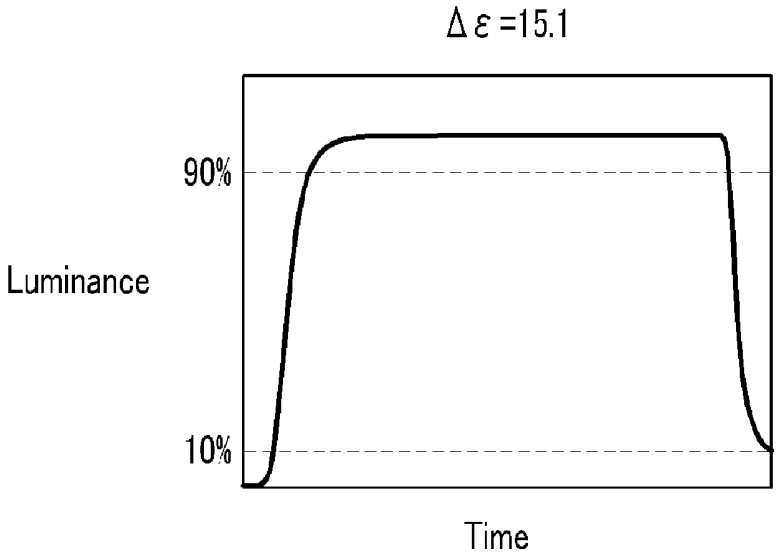


FIG. 13C

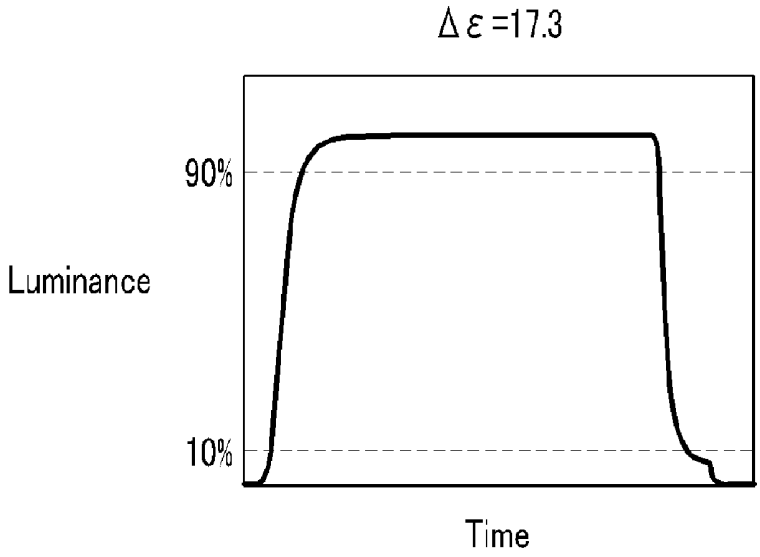



FIG. 14A

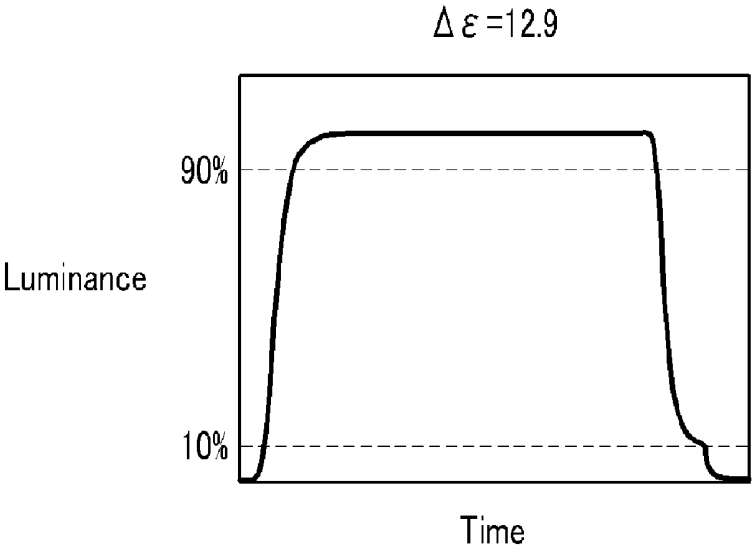


FIG. 14B

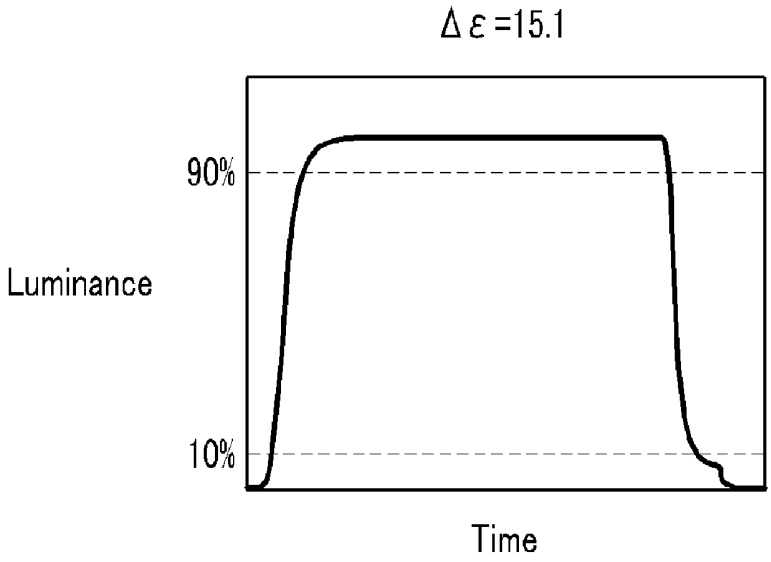



FIG. 14C

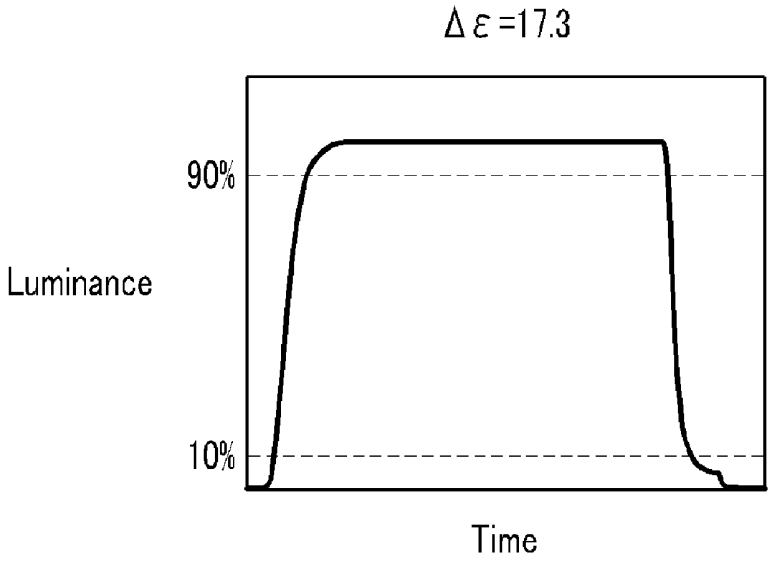


FIG. 15A

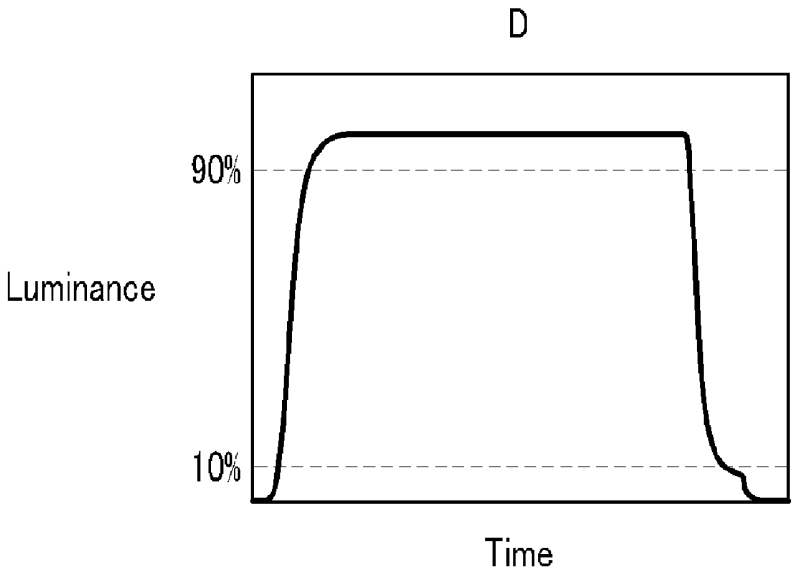



FIG. 15B

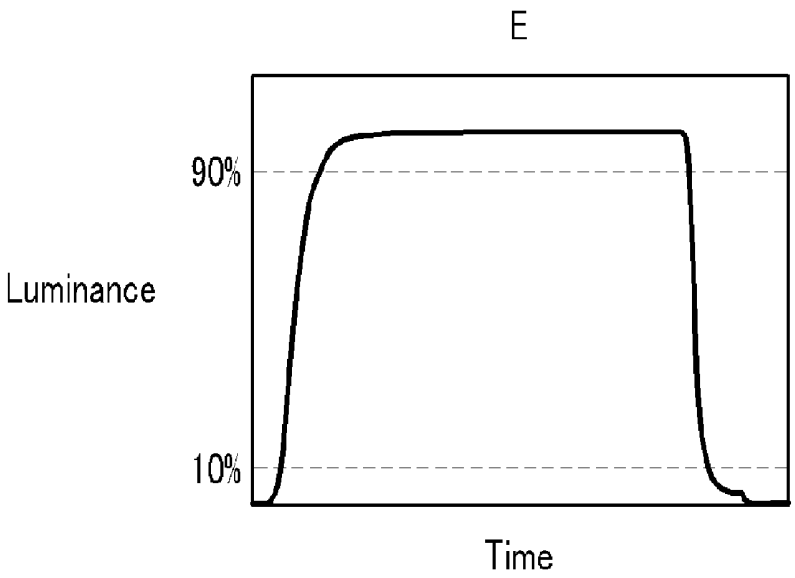


FIG. 16A

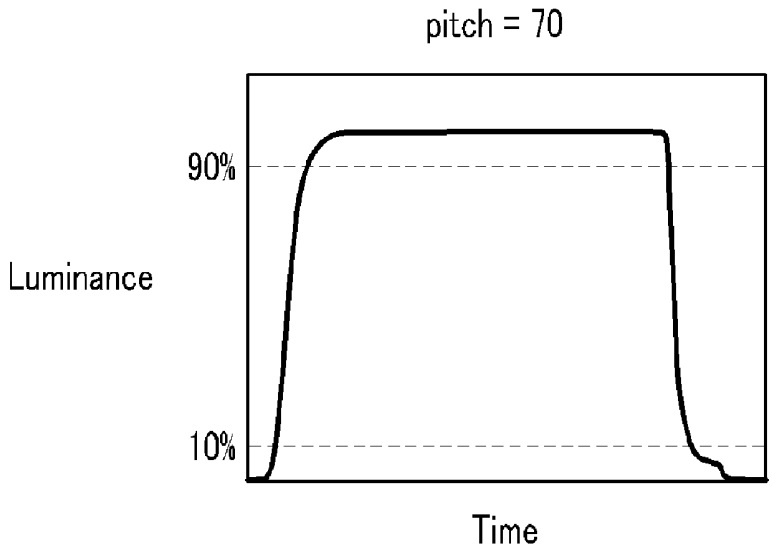



FIG. 16B

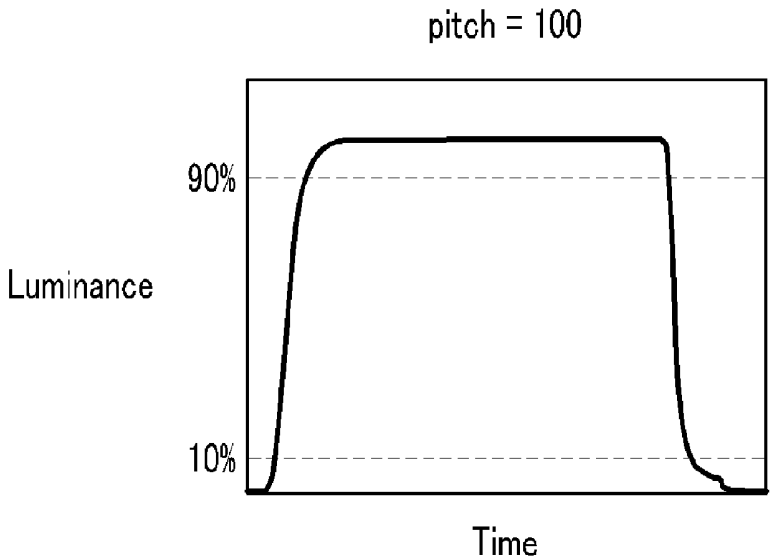
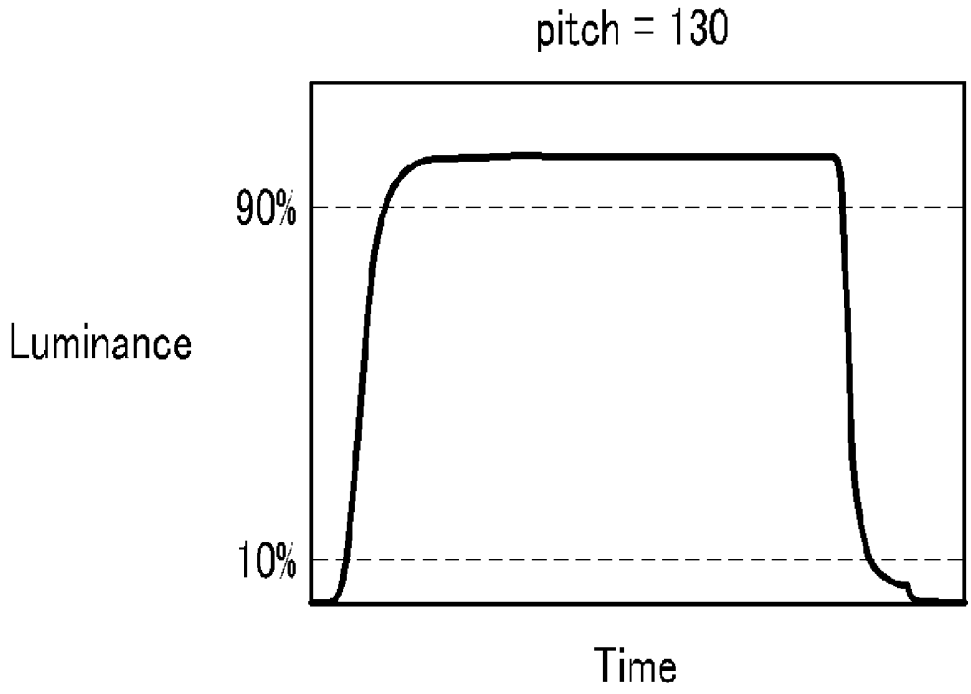


FIG. 16C



# LIQUID CRYSTAL DISPLAY

[0001] This application claims priority to Korean Patent Application No. 10-2008-0090626, filed on Sep. 16, 2008, and all the benefits accruing therefrom under 35 U.S.C. §119, the contents of which in its entirety are herein incorporated by reference.

## BACKGROUND OF THE INVENTION

[0002] (a) Field of the Invention

[0003] This disclosure relates to a liquid crystal display.

[0004] (b) Description of the Related Art

[0005] A liquid crystal display, which is a widely used type of flat panel display, includes two panels on which field generating electrodes, such as pixel electrodes, common electrodes, or the like, are disposed. A liquid crystal layer is interposed between the panels. A voltage is applied to the field generating electrodes to generate an electric field across the liquid crystal layer. The alignment of liquid crystal molecules in the liquid crystal layer is determined by the electric field. The liquid crystal molecules control a polarization of incident light, thereby displaying an image.

[0006] The liquid crystal display can be used for various applications. In particular, the liquid crystal display can be used as the display in a portable apparatus such as a laptop computer. Since a portable display device is desirably easy to carry and light-weight, a battery incorporated in the portable display device has a practical capacity limit. Therefore, it is desirable for the display device to have low power consumption.

## BRIEF SUMMARY OF THE INVENTION

[0007] In order to reduce the power consumption of the liquid crystal display, it is desirable to reduce a driving voltage, and it is important to select a condition wherein an excellent image quality can be displayed at a low driving voltage.

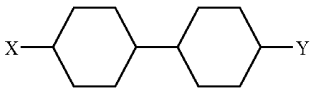
[0008] Disclosed is a liquid crystal display, which can display an image having an excellent image quality at a low driving voltage.

[0009] The above described and other drawbacks are alleviated by a liquid crystal display including a thin film transistor; a liquid crystal capacitor, which is electrically connected to a thin film transistor and comprises a liquid crystal layer; and a storage capacitor, which is electrically connected to the thin film transistor in parallel to the liquid crystal capacitor, wherein the liquid crystal layer has a positive dielectric anisotropy and is disposed in a twisted nematic mode, and a capacitance ratio of a capacitance of the storage capacitor to a capacitance of the liquid crystal capacitor is approximately 0.4 or more.

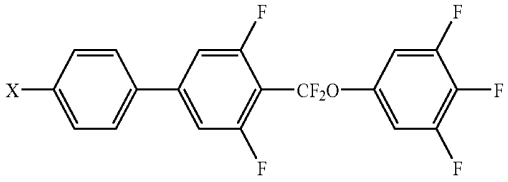
[0010] In an embodiment, the capacitance ratio may be approximately 0.7 or less.

[0011] In an embodiment, a dielectric anisotropy of the liquid crystal layer may be approximately 14 or more. In an embodiment, the dielectric anisotropy of the liquid crystal layer is in a range of approximately 15 to approximately 18. In an embodiment, the dielectric anisotropy of the liquid crystal layer may be in a range of approximately 15.1 to approximately 17.3.

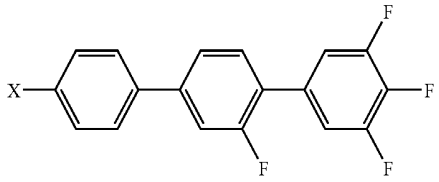
[0012] In an embodiment, the liquid crystal layer comprises a liquid crystal composition selected from the group consisting of liquid crystal compositions I to IV, wherein the liquid crystal composition I comprises compounds of formulas



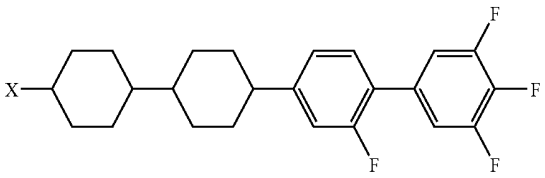

in an amount of approximately 31.5 weight percent,



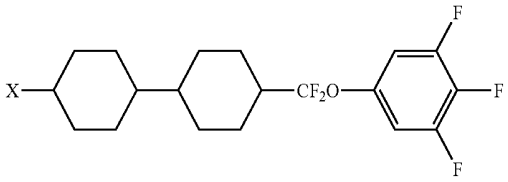

in an amount of approximately 15 weight percent,



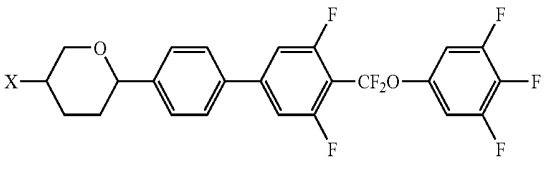

in an amount of approximately 10 weight percent,



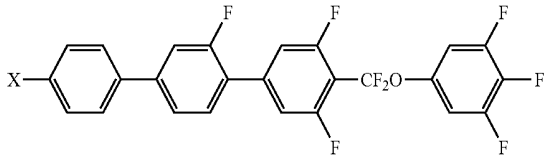

in an amount of approximately 7 weight percent,



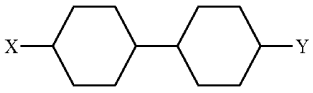

in an amount of approximately 18.5 weight percent,



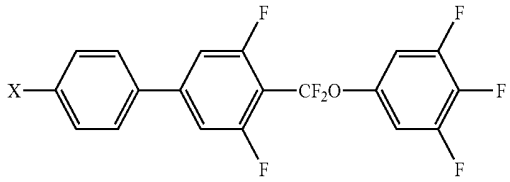

in an amount of approximately 12 weight percent,



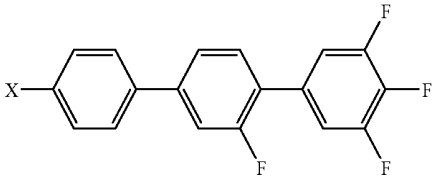
in an amount of approximately 6 weight percent, the liquid crystal composition II comprises compounds of the formulas



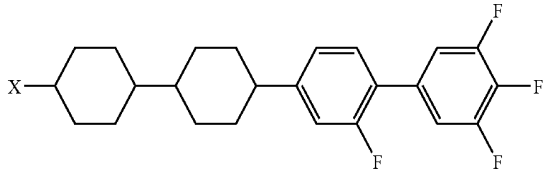
in an amount of approximately 41 weight percent,



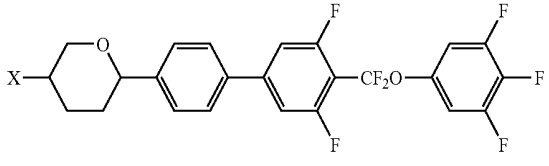
in an amount of approximately 13 weight percent,



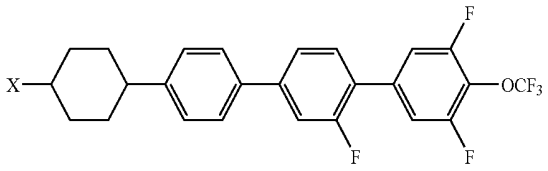
in an amount of approximately 8.5 weight percent,



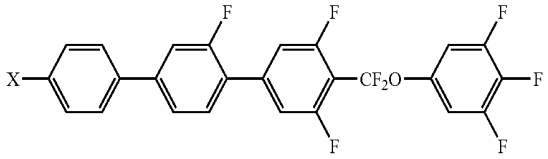
in an amount of approximately 6.5 weight percent,



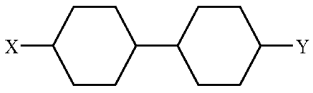
in an amount of approximately 12 weight percent,



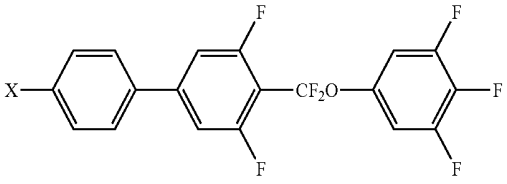
in an amount of approximately 6 weight percent,



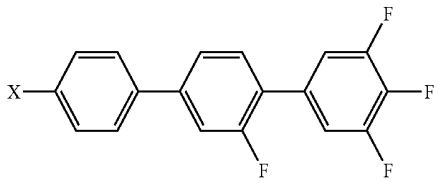
in an amount of approximately 5 weight percent, the liquid crystal composition III comprises compounds of the formulas



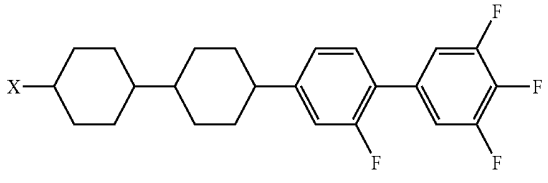
in an amount of approximately 21.5 weight percent,



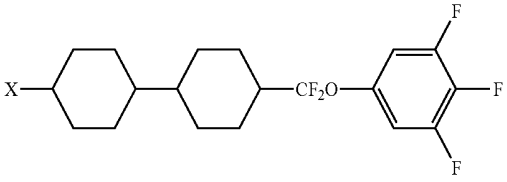
in an amount of approximately 10 weight percent,



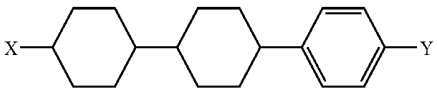
in an amount of approximately 7 weight percent,



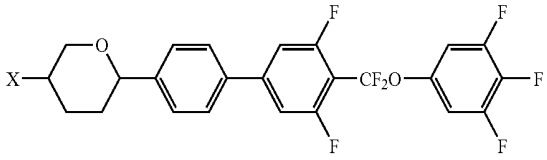
in an amount of approximately 5 weight percent,



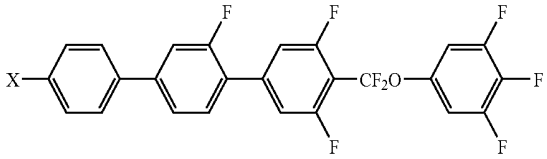
in an amount of approximately 27 weight percent,



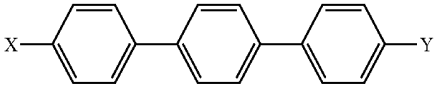
in an amount of approximately 10 weight percent,



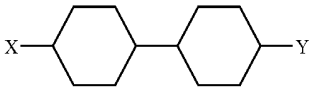
in an amount of approximately 13.5 weight percent,



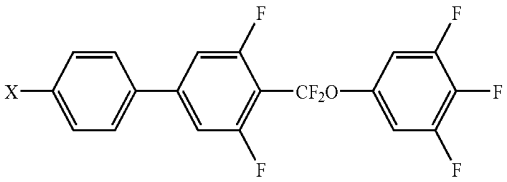
in an amount of approximately 2 weight percent,



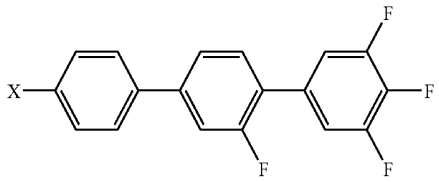
in an amount of approximately 4 weight percent, and the liquid crystal composition IV comprises compounds of the formulas



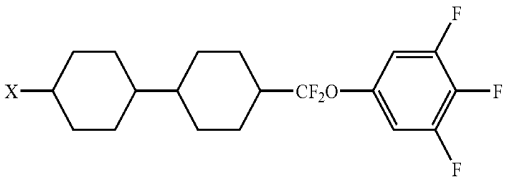
in an amount of approximately 12 weight percent,



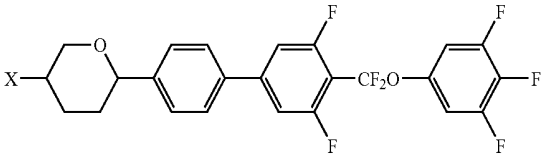
in an amount of approximately 5.5 weight percent,



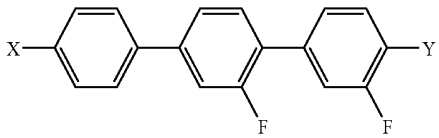
in an amount of approximately 10 weight percent,



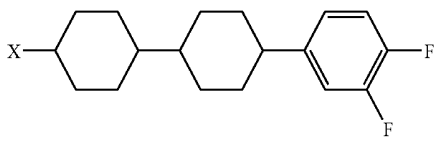
in an amount of approximately 35 weight percent,



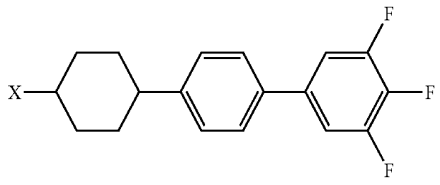
in an amount of approximately 14 weight percent,



in an amount of approximately 5 weight percent,



in an amount of approximately 8.5 weight percent,



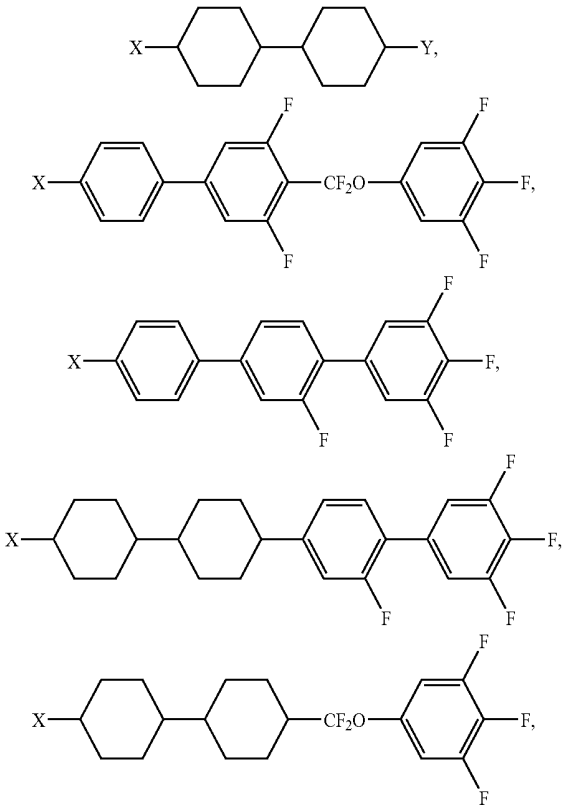
in an amount of approximately 10 weight percent, based on a total weight of the liquid crystal composition, and X and Y may be independently one of an alkyl group, an alkynyl group and an alkoxy group.

**[0013]** In an embodiment, a thickness of the liquid crystal layer may be in a range of approximately 3 micrometers ("μm") to approximately 4 μm. In an embodiment, the thickness of the liquid crystal layer is in a range of approximately 3.3 μM to approximately 3.6 μM.

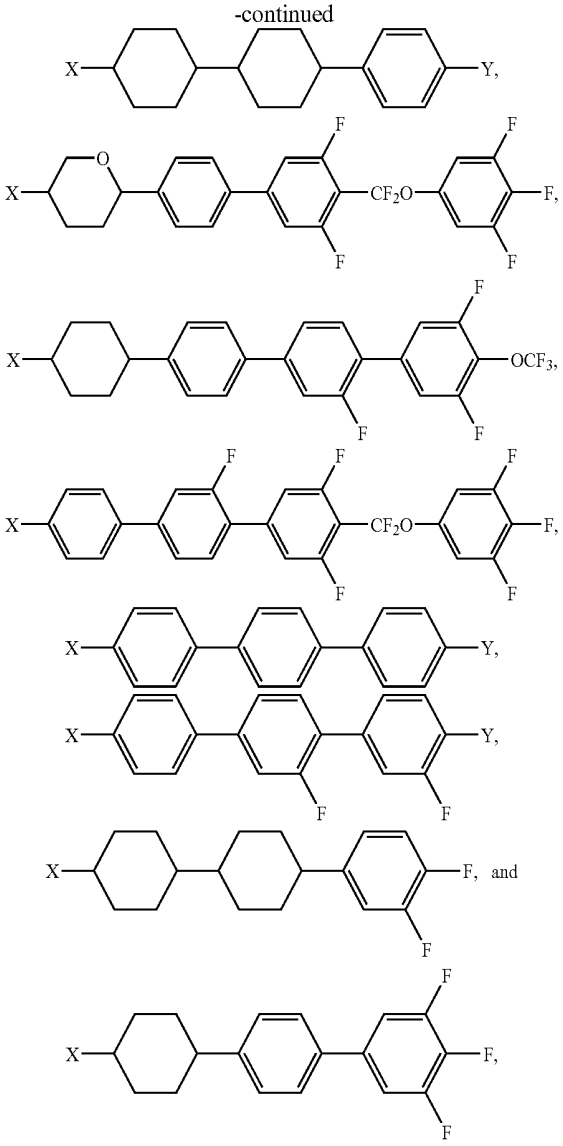
**[0014]** In an embodiment, an effective elastic coefficient of the liquid crystal layer may be approximately 10 or less. In an embodiment, a pitch of the liquid crystal layer may be approximately 100 or more.

**[0015]** In an embodiment, the liquid crystal display is in a normally white mode, and a final luminance is approximately 10 percent or less for one frame when a voltage difference between both ends of the liquid crystal capacitor is changed from 0 volts ("V") to 2.5 V.

**[0016]** In an embodiment, the liquid crystal layer comprises a liquid crystal composition comprising at least one compound of the formula



-continued



and X and Y may be independently one of an alkyl group, an alkynyl group and an alkoxy group.

**[0017]** The disclosed liquid crystal display can provide excellent image quality at a low driving voltage.

**[0018]** These and other features, aspects, and advantages of the disclosed embodiments will become better understood with reference to the following description and appended claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0019]** The disclosed subject matter is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the disclosed embodiments are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

**[0020]** FIG. **1** is an equivalent circuit diagram showing an exemplary embodiment of a pixel in a liquid crystal display;

**[0021]** FIGS. **2** and **3** are cross-sectional views showing an exemplary embodiment of a liquid crystal display;

**[0022]** FIGS. **4** and **5** are diagrams illustrating a polarization direction of an exemplary embodiment of a polarizer in an embodiment of a liquid crystal display;

**[0023]** FIG. **6** is a plan view showing an exemplary embodiment of a liquid crystal display;

**[0024]** FIG. **7** is a cross-sectional view showing an exemplary embodiment of a liquid crystal display taken along line of FIG. **6**;

**[0025]** FIG. **8**A to FIG. **9**C are graphs illustrating the luminance of an exemplary embodiment of a liquid crystal display with respect to time;

**[0026]** FIG. **10** is a graph illustrating luminance with respect to voltage for an exemplary embodiment of a liquid crystal display; and

**[0027]** FIG. **11**A to FIG. **16**C are graphs illustrating the luminance of an exemplary embodiment of a liquid crystal display with respect to time.

**[0028]** The detailed description explains the preferred embodiments, together with advantages and features, by way of example with reference to the drawings.

## DETAILED DESCRIPTION OF THE INVENTION

**[0029]** The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiment's of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

**[0030]** Aspects, advantages, and features of the present invention and methods of accomplishing the same may be understood more readily by reference to the following detailed description of preferred embodiments and the accompanying drawings. The present invention may, however, may be embodied in many different forms, and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art, and the present invention will only be defined by the appended claims. Like reference numerals refer to like elements throughout the specification.

**[0031]** In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. When an element such as a layer, a film, a region, a plate, or the like is referred to as being "above" another element, the element may be "directly on" another element or there may be an intervening element present therebetween. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

**[0032]** It will be understood that, although the terms first, second, third, etc., may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer, or section from another region, layer, or section. Thus, a first element, component, region, layer, or section discussed below could be termed a second element, component, region, layer, or section without departing from the teachings of the present invention.

**[0033]** Spatially relative terms, such as "below", "lower", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "lower" relative to other elements or features would then be oriented "above" relative to the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

**[0034]** The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

**[0035]** Embodiments of the invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments (and intermediate structures) of the invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing.

**[0036]** For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the invention.

**[0037]** Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

**[0038]** All methods described herein can be performed in a suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g., "such as"), is intended merely to better illustrate the invention and does not pose a limitation on the scope of the invention unless otherwise claimed. No language in the specification should be construed as indicating any non-claimed element as essential to the practice of the invention as used herein.

**[0039]** Hereinafter, referring to FIG. **1** to FIG. **5**, a liquid crystal display according to an exemplary embodiment is described in detail.

**[0040]** FIG. **1** is an equivalent circuit diagram of an exemplary embodiment of a pixel in a liquid crystal display, FIG. **2** and FIG. **3** are cross-sectional views of an exemplary embodiment of a liquid crystal display, and FIG. **4** and FIG. **5** are diagrams illustrating a polarization direction of a polarizer in an exemplary embodiment of a liquid crystal display.

**[0041]** Referring to FIG. **1**, the liquid crystal display includes a plurality of pixels PX, which are disposed approximately in a matrix, and a plurality of gate lines **121** and a plurality of data lines **171**, which are connected thereto. The gate lines **121** transmit gate signals and the data lines **171** transmit data voltages. Each of the pixels includes a switching element Qs, and a liquid crystal capacitor Clc and a storage capacitor Cst, which are connected thereto. The switching element Qs controls a data voltage in response to a gate signal. The switching element Qs is activated for a short time to allow the data voltage to be transmitted, and is turned off for a remaining time. The data voltages applied to each of the pixels PX are stored at the liquid crystal capacitor Clc and the storage capacitor Cst. The liquid crystal capacitor Clc includes a liquid crystal material as a dielectric material, and the storage capacitor Cst includes a different insulator.

**[0042]** Referring to FIG. **2** and FIG. **3**, the liquid crystal display according to an exemplary embodiment includes a thin film transistor array panel **100** and a common electrode panel **200**, which face each other, and a liquid crystal layer **3** interposed between the thin film transistor array panel **100** and the common electrode panel **200**. The liquid crystal display further includes a pair of first and second polarizers **12** and **22**, disposed in a crossed or parallel configuration, which are disposed on exterior surfaces of the thin film transistor array panel **100** and the common electrode **200**, respectively. FIG. **4** illustrates an exemplary embodiment wherein the first and second polarizers **12** and **22** are disposed in a crossed configuration, and FIG. **5** illustrates an exemplary embodiment wherein the first and second polarizers **12** and **22** are disposed in a parallel configuration in a liquid crystal display **300**.

**[0043]** The thin film transistor array panel **100** includes a first substrate **110**, pixel electrodes **191**, and a first homogeneous alignment layer **11**, which are disposed on an interior surface of the first substrate **110**. The common electrode panel **200** includes a second substrate **210**, and a common electrode **270** and a second homogeneous alignment layer **21**, which are disposed on an interior surface of the second substrate **210**. Liquid crystal capacitors Clc comprise pixel electrodes **191**, the common electrode **270**, and the liquid crystal layer **3** interposed therebetween. A selected voltage, which can be a common voltage, is applied to the common electrode **270**, and data voltages transmitted through the switching elements Q are applied to the pixel electrodes **191**. The pixel electrodes **191** may also form storage capacitors Cst by being superimposed with another conductor (not shown) of the thin film transistor array panel **100**.

**[0044]** The liquid crystal layer **3** has positive dielectric anisotropy and is disposed in a twisted nematic ("TN") mode. In an embodiment, when a voltage is not applied, long axes of the liquid crystal molecules **31**, **32**, and **33** are parallel to surfaces of the first and second substrates **110** and **210**, respectively, and the long axes gradually twist from a surface of one of the first and second homogeneous alignment layers **11** and **21** to a surface of the other of the first and second homogeneous alignment layers **21** and **11**. In this state, the long axes of the liquid crystal molecules **31** and **32** near the surfaces of the first and second homogeneous alignment layers **11** and **21** may each form an angle of approximately 45 degrees with polarization axes of the first and second polarizers **12** and **22**, as shown in FIG. **4**.

**[0045]** When a potential difference is applied between the pixel electrodes **191** and the common electrode **270** in the liquid crystal display, an electric field E, which is substantially perpendicular to the surfaces of the first and second substrates **110** and **210**, is generated as shown in FIG. **3**. As a result, the liquid crystal molecules **31** to **33** are arranged so that the long axes are parallel to the electric field E. When the intensity of the electric field E is large enough, the long axes of most of the liquid crystal molecules **31** to **33** may be substantially parallel to the electric field E.

**[0046]** Light passing through any one of the first and second polarizers **12** and **22** is linearly polarized according to polarization axes P**1** and P**2**, respectively, and a polarization of the light is changed when the light passes through the liquid crystal layer **3**. The incident light, having passed through the liquid crystal layer **3**, is again linearly polarized by the other of the polarizers **22** and **12**. Thus, in an embodiment, the intensity of outgoing light depends on a degree of polarization change by the liquid crystal layer **3**. The degree of polarization change of light, which passes through the liquid crystal layer **3**, depends on an arrangement of the liquid crystal molecules **31** to **33**. In an embodiment, as shown in FIG. **3**, when most of the liquid crystal molecules **31** to **33** are perpendicular to the surfaces of the first and second substrates **110** and **210**, there is little polarization change of the light passing through the liquid crystal layer **3**. Accordingly, when the first and second polarizers **12** and **22** are crossed, as shown in FIG. **4**, transmission of incident light is prevented, and when the first and second polarizers **12** and **22** are parallel, as shown in FIG. **5**, the incident light is substantially transmitted. In an embodiment, as shown in FIG. **2**, when an electric field is not applied across the liquid crystal layer **3**, thus the liquid crystal molecules **31** to **33** are substantially parallel to the surfaces of the first and second substrates **110** and **210** and are maximally twisted, there occurs the largest polarization change of light passing through the liquid crystal layer **3**. Accordingly, when the first and second polarizers **12** and **22** are crossed, as shown in FIG. **4**, the incident light can pass, and when the first and second polarizers **12** and **22** are parallel, as shown in FIG. **5**, transmission of the incident light is prevented. Therefore, the embodiment shown in FIG. **4** is called a normally white mode, and the embodiment shown in FIG. **5** is called a normally black mode.

**[0047]** The arrangement of the liquid crystal molecules **31** to **33** is controlled by the intensity of the electric field E, and the intensity of the electric field E is controlled by a difference in voltage between the pixel electrodes **191** and the common electrode **270**. Therefore, it is possible to control an intensity of outgoing light by varying the data voltage applied to the pixel electrodes **191**, and thus, it is possible to control a luminance of the pixels PX.

**[0048]** In a liquid crystal display the common voltage may be approximately 2.5 volts ("V") and the data voltage may vary in a range of approximately 0 V to approximately 5 V, specifically between approximately 0.25 V to approximately 7 V, more specifically between approximately 0.5 V to approximately 6V. In an embodiment, when a data voltage of

2.5 V is applied for a sufficient time, an arrangement the liquid crystal molecules is like that of FIG. **2**, and a maximum luminance may be displayed by configuring the polarizers in a crossed configuration, and a minimum luminance may be displayed by configuring the polarizers in a parallel configuration. In another embodiment, when a data voltage of approximately 0 V or approximately 5 V is applied for a sufficient time, a minimum luminance may be displayed by configuring the polarizers in crossed configuration, and a maximum luminance may be displayed by configuring the polarizers in a parallel configuration, as shown in FIG. **3**.

**[0049]** A ratio of a capacitance of the storage capacitor Cst to a capacitance of the liquid crystal capacitor Clc, Cst/Clc (hereinafter, the ratio Cst/Clc is referred to as a capacitance ratio, and the capacitor and the capacitance thereof will be represented by the same reference numeral), is approximately 0.2 or more, specifically approximately 0.4 or more, more specifically approximately 0.6 or more. The capacitance ratio may be about 0.7 or less, and when the capacitance ratio is over 0.7, the aperture ratio may be substantially reduced, hindering display of an image. The dielectric anisotropy of the liquid crystal layer **3** may be approximately 10 or more, specifically approximately 14 or more, more specifically 16 or more. In an embodiment, the dielectric anisotropy may be in a range of approximately 15 to approximately 18. Furthermore, the dielectric anisotropy may be in a range of approximately 15.1 to approximately 17.3. A thickness d of the liquid crystal layer, also termed a cell gap, is between approximately 3.0 micrometers "μm" to approximately 4.0 μm, specifically between approximately 3.3 μm to approximately 3.6 μm. An effective elastic coefficient Keff of the liquid crystal layer **3** may be approximately 15 or less, specifically approximately 10 or less, and a pitch of the liquid crystal layer **3** may be approximately 50 or more, specifically approximately 100 or more.

**[0050]** Exemplary embodiments of the liquid crystal display shown in FIG. **1** to FIG. **5** are described in detail with reference to FIG. **6** and FIG. **7**.

**[0051]** FIG. **6** is a plan view showing an exemplary embodiment of a liquid crystal display, and FIG. **7** is a cross-sectional view showing an exemplary embodiment of a liquid crystal display taken along line VII-V**11** of FIG. **6**.

**[0052]** Referring to FIG. **6** and FIG. **7**, the liquid crystal display includes a thin film transistor array panel **100**; a common electrode panel **200**, a liquid crystal layer **3**, and first and second polarizers **12** and **22**.

**[0053]** First, the common electrode panel **200** is described.

**[0054]** A light blocking member **220** is disposed on a second substrate **210**, which may comprise transparent glass, plastic, or the like, or a combination comprising at least one of the foregoing materials. The light blocking member **220** is also referred to as a black matrix and has a plurality of openings, which are arranged in a matrix.

**[0055]** A plurality of color filters **230** are also disposed on the second substrate **210**. A portion of the color filters **230** are disposed in the openings and may be disposed along a column of the openings of the light blocking member **220** in a vertical direction. Each of the color filters **230** may have one of three primary colors, e.g., red, green, and blue. Adjacent color filters **230** may be superimposed over each other.

**[0056]** An overcoat **250** is disposed on the color filters **230** and the light blocking member **220**. The overcoat **250** may comprise an organic insulator, or the like. The overcoat **250** can substantially reduce or prevent exposure of the color filter **230** and can provide a flat surface. The overcoat **250** may be omitted.

**[0057]** The common electrode **270** is disposed on the overcoat **250**. The common electrode **270** may comprise a transparent conductor, such as indium tin oxide ("ITO"), indium zinc oxide ("IZO"), or the like, or a combination comprising at least one of the foregoing materials.

**[0058]** The second homogeneous alignment layer **21** is disposed on the common electrode **270**. The second homogeneous alignment layer **21** may be a homogenous alignment layer, and may be rubbed in one direction.

**[0059]** Next, the thin film transistor array panel **100** is described.

**[0060]** Gate lines **121** and storage electrode lines **131** are disposed on a second substrate **110**, which may comprise transparent glass, plastic, or the like, or a combination comprising at least one of the foregoing materials.

**[0061]** The gate lines **121** transmit gate signals and extend mainly in a horizontal direction. Each of the gate lines **121** includes a plurality of gate electrodes **124**, which project upwards, and a gate line end portion **129** for electrical connection with another layer or an external driving circuit. A gate driving circuit (not shown) generates gate signals and may be mounted on a flexible printed circuit film (not shown) attached onto the second substrate **110**, may be mounted directly on the second substrate **110**, or integrated on the second substrate **110**. In an embodiment where the gate driving circuit is integrated on the second substrate **110**, the gate lines **121** may extend to and be electrically connected directly to the gate driving circuit.

**[0062]** A selected voltage is applied to the storage electrode lines **131**. The storage electrode lines **131** each include a branch line extending substantially parallel to the gate lines **121**, and a plurality of storage electrodes **133** branching from the branch line. The storage electrode lines **131** are disposed between adjacent gate lines **121** and the branch line is closer to upper portions of the gate lines **121** and between two of the gate lines **121**. The storage electrodes **133** each include a fixed end electrically connected to the branch line, a free end opposite thereto, and a main body therebetween. The fixed end and the free end have widths which are smaller than a width of the main body. The fixed end is electrically connected to the center of the main body and the free end is electrically connected to any one side of the main body. Upper-right portions of the main body of the storage electrodes **133** have a shape which is different than a shape of other portions of storage electrodes **133**. The portions of the storage electrodes **133** disposed in the center of FIG. **6** protrude to the right side in FIG. **6**, and the portions of the storage electrodes **133** shown at either side of FIG. **6** are flat. In other embodiments, the storage electrode lines **131** may have various shapes and various arrangement patterns.

**[0063]** A gate insulating layer **140**, which may comprise silicon nitride ($SiN_x$), silicon oxide ($SiO_x$), or the like, or a combination comprising at least one of the foregoing materials is disposed on the gate lines **121** and the storage electrode lines **131**.

**[0064]** Semiconductor islands **154**, which may comprise hydrogenated amorphous silicon ("a-Si"), polysilicon, or the like, or a combination comprising at least one of the foregoing materials, are disposed on the gate insulating layer **140**. The semiconductor islands **154** are disposed on the gate elec-

trodes **124**, and an upper right portion of each of the semiconductor islands **154** can protrude slightly.

**[0065]** A pair of first and second ohmic contacts **163** and **165** are disposed on the semiconductor islands **154**. The first and second ohmic contacts **163** and **165** may comprise a material such as n+ hydrogenated amorphous silicon doped with an n-type impurity at high concentration, silicide, or the like, or a combination comprising at least one of the foregoing materials.

**[0066]** Data lines **171** and drain electrodes **175** are disposed on the first and second ohmic contacts **163** and **165**, respectively, and on the gate insulating layer **140**.

**[0067]** The data lines **171** extend mainly in a vertical direction and intersect the gate lines **121** near the gate electrodes **124**, respectively. The data lines **171** also intersect the storage electrode lines **131** and are superimposed on the storage electrodes **133**. The data lines **171** each include a source electrode **173**, which have a 'J' shape and are disposed on the gate electrodes **124**, and a data line end portion **179** for electrically connecting with another layer or an external driving circuit. A data driving circuit (not shown) generates the data voltages and may be mounted on the flexible printed circuit film (not shown), which is attached to the first substrate **110**, may be mounted directly on the first substrate **110**, or may be integrated on the first substrate **110**. In an embodiment the data driving circuit is integrated on the first substrate **110** and the data lines **171** may extend to and be electrically connected directly to the data driving circuit.

**[0068]** The drain electrodes **175** extend upward from one end, are partially surrounded by the source electrodes **173**, and are bent and elongated in the horizontal direction. Further, the drain electrodes have a part having a large area in the middle thereof. The drain electrodes **175** can comprise two different shapes which are each disposed on every other of the drain electrodes **175**, and a portion of the drain electrodes **175** corresponding to the protruding upper-right corner of each of the storage electrodes **133** also protrudes upwards.

**[0069]** One of each of the gate electrodes **124**, the source electrodes **173**, the drain electrodes **175**, and the semiconductor islands **154** constitute a thin film transistor ("TFT"), which is a switching element Q shown in FIG. **1**. A channel of the thin film transistor is disposed on each of the semiconductor islands **154** between each of the source electrodes **173** and the drain electrodes **175**.

**[0070]** The first and second ohmic contacts **163** and **165** are disposed only between the underlying semiconductor islands **154** and the overlying data lines **171** and the drain electrodes **175**, and reduce a contact resistance therebetween. The semiconductor islands **154** each include an exposed portion not covered by the data lines **171** and the drain electrodes **175**, such as a portion between the source electrodes **173** and the drain electrodes **175**.

**[0071]** A passivation layer **180** is disposed on the data lines **171**, the drain electrodes **175**, and the exposed portions of the semiconductor islands **154**. The passivation layer **180** may comprise an inorganic insulator, an organic insulator, or the like, or a combination comprising at least one of the foregoing insulators, and may have a flat surface. The inorganic insulator may include silicon nitride, silicon oxide, or the like, or a combination comprising at least one of the foregoing materials. The organic insulator may be photosensitive. The dielectric constant of the organic insulator may be approximately 2 or less, specifically approximately 4 or less, more specifically approximately 6 or less. In an embodiment, the passivation layer **180** may have a dual-layer structure composed of a lower inorganic layer and an upper organic layer to reduce or substantially prevent the exposed portions of the semiconductor islands **154** from being damaged without significantly altering the properties of the organic layer.

**[0072]** First contact holes **182**, which expose the data line end portions **179** of the data lines **171**, and second contact holes **185**, which expose the wide portions of the drain electrodes **175**, are disposed in the passivation layer **180**. Third contact holes **181**, which expose the gate line end portions **129** of the gate lines **171**, and fourth contact holes **183***b*, which expose a part of the branch line of each of the storage electrode lines **131** located near the fixed end of the storage electrodes **133**, and a fifth contact holes **183***a*, which expose the free end of the storage electrodes **133**, are disposed in the passivation layer **180** and the gate insulating layer **140**. The fourth and fifth contact holes **183***a* and **183***b* are disposed at the protruding upper-right corner of each of the storage electrodes **133** and the upwardly-protruding portions of the drain electrodes **175**.

**[0073]** Pixel electrodes **191**, overpasses **83**, and first and second contact assistants **81** and **82** are disposed on the passivation layer **180**. They may comprise a transparent conductive material, such as ITO or IZO, or a reflective metal such as aluminum, silver, chromium, an alloy thereof, or the like, or a combination comprising at least one of the foregoing materials.

**[0074]** The pixel electrodes **191** are physically and electrically connected to the drain electrodes **175** through the second contact holes **185** and data voltages from the drain electrodes **175** are applied to the pixel electrodes **191**. The pixel electrodes **191** are superimposed on the common electrode **270**, and the liquid crystal layer **3** is interposed therebetween to constitute liquid crystal capacitors Clc, while the pixel electrodes **191** are superimposed on the storage electrode lines **131** as well as the storage electrodes **133** to constitute storage capacitors Cst. The capacitance of the storage capacitors Cst can be selected by selecting the superimposing area of the pixel electrodes **191** and the storage electrode lines **131**. When the superimposing area is increased to increase the capacitance, an opening ratio may be reduced.

**[0075]** The pixel electrodes **191** face an opening of the light blocking member **220**. The drain electrodes **175** are superimposed on the pixel electrodes **191** along a bottom side of the pixel electrodes **191**.

**[0076]** The overpasses **83** intersect the gate lines **121** and are electrically connected to an exposed edge of a free end of the storage electrodes **133** and an exposed portion of the branch line of each of the storage electrode lines **131** through the contact holes **183***a* and **183***b*, which are disposed opposite to each other with respect to the gate lines **121**. One overpass **83** can be disposed per every two pixels in a row direction. The pixel electrodes **191**, the drain electrodes **175**, the storage electrodes **133**, and the light blocking member **220** may have different shapes according to whether the optional overpasses **83** are present. In an embodiment, when the overpasses **83** are present, a large portion of the corner of each of the pixel electrodes **191** is cut off, and thus the shapes of the pixel electrodes **191**, the drain electrodes **175**, the storage electrodes **133**, and the light blocking member **220** are changed accordingly. The storage electrode lines **131**, including the storage electrodes **133**, together with the overpasses **83**, may be used to correct a defect of the gate lines **121**, the data lines **171**, or a thin film transistor.

**[0077]** A capacitance ratio, which is a capacitance of the storage capacitor Cst to a capacitance of the liquid crystal capacitor Clc, may be approximately 0.2 or more, specifically 0.4 or more, more specifically 0.6 or more. The capacitance ratio may be approximately 0.7 or less. When the capacitance ratio is greater than 0.7, an aperture ratio is decreased, thereby interrupting display of an image. The dielectric anisotropy of the liquid crystal layer **3** may be approximately 14 or more. In particular, the dielectric anisotropy of the liquid crystal layer **3** may be in a range of approximately 14 to approximately 15. Furthermore, the dielectric anisotropy of the liquid crystal layer **3** may be in a range of approximately 15.1 to approximately 17.3. The thickness d of the liquid crystal layer, which is a cell gap, may be approximately 3.0 μm to approximately 4.0 μm, specifically approximately 3.3 μm to approximately 3.6 μm, more specifically approximately 3.5 μm. An effective elastic coefficient Keff of the liquid crystal layer **3** may be approximately 10 or less, and a pitch of the liquid crystal layer **3** may be approximately 100 or more.

**[0078]** In a liquid crystal display according to an exemplary embodiment, the common voltage may be approximately 2.5V and the data voltage may vary in a range of approximately 0V to 5V.

**[0079]** The above-described conditions have been observed in experimental examples described below with reference to FIG. **8**A to FIG. **16**C. Each of FIG. **8**A to FIG. **9**C, and FIG. **11**A to FIG. **16**C illustrates a curve representing a luminance of a pixel with respect to time when the data voltage is selected to be 0 V, 2.5 V, or 5 V in a normally white mode liquid crystal display. In the experiments, a data voltage of 2.5 V was applied for several frames at a state of 0 V, and then a data voltage of 5 V was applied for several frames. The driving frequency was 60 hertz ("Hz"). The resolution of the liquid crystal display was 1280 by 800 pixels.

**[0080]** In the experiments, five liquid crystal compositions, A to E, were used. The five liquid crystal compositions A to E comprised at least one of the compounds listed in Table 1 in the amounts listed in Table 1, which are in weight percent, based on the total weight of the liquid crystal composition.

TABLE 1

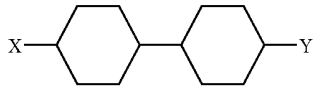
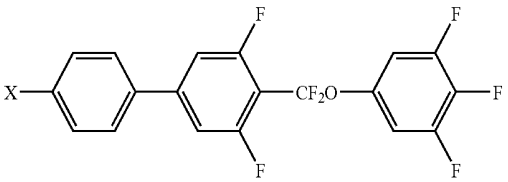
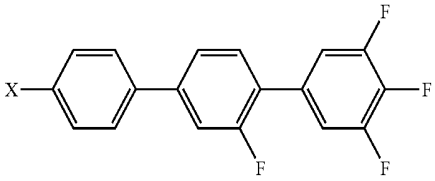
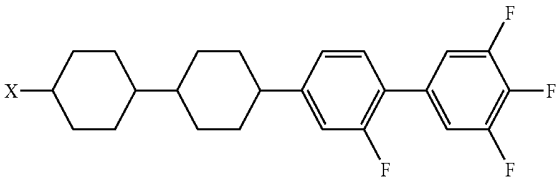
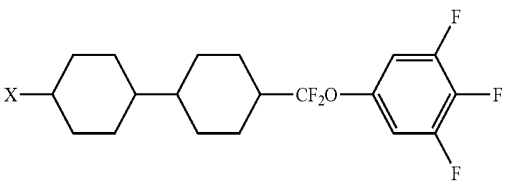
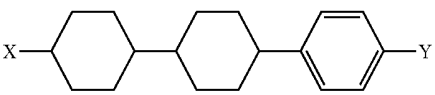
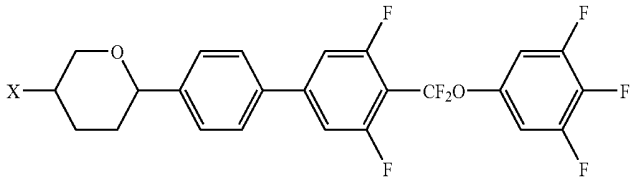
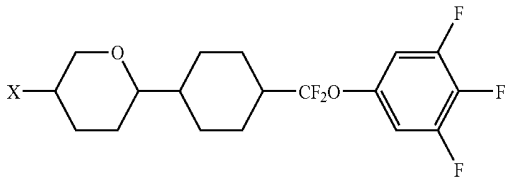
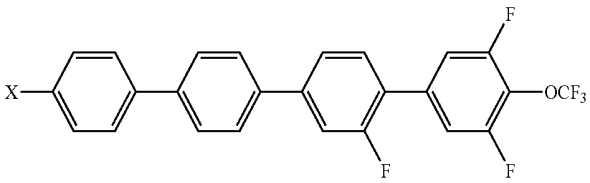
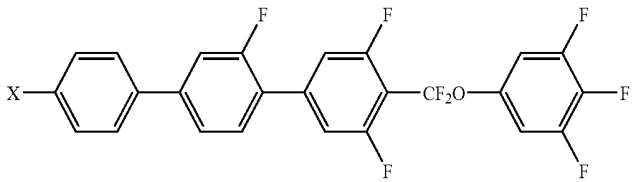
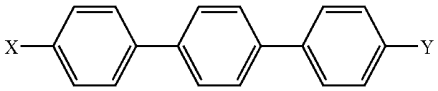
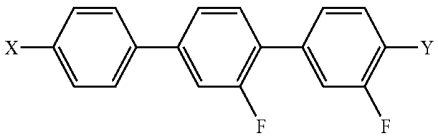
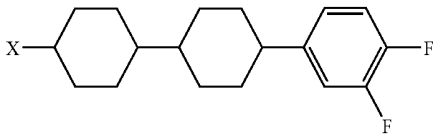
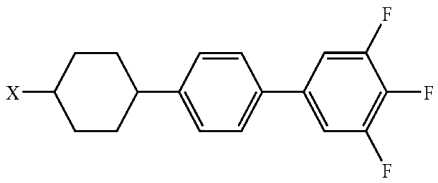
| | | Liquid Crystal ("LC") Composition | | | | |
|---|---|---|---|---|---|---|
| Compound | Formula | A | B | C | D | E |
| 1 |  | 1.5 | 41 | 42 | 21.5 | 12 |
| 2 |  | 15 | 13 | 12.5 | 10 | 5.5 |
| 3 |  | 10 | 8.5 | 10.5 | 7 | 10 |
| 4 |  | 7 | 6.5 | 7 | 5 | — |
| 5 |  | 18.5 | — | 3.5 | 27 | 35 |
| 6 |  | — | — | 6.5 | 10 | — |

TABLE 1-continued

| Compound | Formula | Liquid Crystal ("LC") Composition A | B | C | D | E |
|---|---|---|---|---|---|---|
| 7 |  | 12 | 12 | 10 | 13.5 | 14 |
| 8 |  | — | 8 | — | — | — |
| 9 |  | — | 6 | — | — | — |
| 10 |  | 6 | 5 | 8 | 2 | — |
| 11 |  | — | | | 4 | — |
| 12 |  | — | — | — | — | 5 |
| 13 |  | — | — | — | — | 8.5 |
| 14 |  | — | — | — | — | 10.0 |

In an embodiment, X and Y may be independently one of an alkyl group, an alkynyl group, an alkoxy group, and the like.

**[0081]** As shown in FIG. **11**A, in a first frame F**1** in which the data voltage is changed from 2.5 V to 5 V, the luminance is not less than 10 percent ("%"). However, not until the second frame F**2** is the luminance decreased to the minimum value.

**[0082]** In the first frame F**1**, the luminance rapidly decreases, but the rate of decrease is gradually reduced, and at the end of frame F**1**, the luminance stays at a point over 10%. If a data voltage is no longer applied, the luminance is maintained in the last state. More specifically, since the response speed of the liquid crystal layer **3** is low, it takes a time for complete rearrangement of the liquid crystal molecules **31** to **33** in response to the intensity change of the electric field when the intensity of the electric field varies rapidly. However, a time while a data voltage is applied to a liquid crystal capacitor Clc can be too short to complete such a rearrangement. Therefore, even after the application of a data voltage is terminated and the voltage of the pixel electrodes **191**, which are each one terminal of each of the liquid crystal capacitors Clc and the storage capacitors Cst, are floated, the liquid crystal molecules **31** to **33** are still in a rearrangement process. The dielectric constant of the liquid crystal layer **3** varies in accordance with the rearrangement of the liquid crystal molecules **31** to **33**, and accordingly, the voltage of the pixel electrodes **191** varies and a voltage across the liquid crystal capacitors Clc also varies. Consequently, even after the rearrangement of the liquid crystal molecules **31** to **33** is complete, the luminance does not reach the desired value.

**[0083]** In the second frame F**2**, when the same data voltage as the first frame F**1** is applied, the luminance of the pixel decreases rapidly to obtain a minimum luminance, as desired.

**[0084]** Therefore, a pointed cusp Pc is generated in a luminance curve.

**[0085]** Surprisingly, it has been observed that the pointed cusp Pc can be located below a luminance of 10% by selection of a response time of approximately 16 milliseconds ("ms") or less. In addition, it has been observed that the capacitance ratio influences the location of the pointed cusp Pc.

**[0086]** First, the dielectric anisotropy of the liquid crystal layer **3** is selected to be high so the liquid crystal display can be driven at a low voltage, as small as approximately 2.5 V, thus selection of a liquid crystal material having high dielectric anisotropy can be desirable. The dielectric anisotropy of the liquid crystal composition A is 17.3, and the rotational viscosity of the liquid crystal composition A is 103. In a condition in which the capacitance ratio is set to approximately 0.4, the response time and the luminance were measured while the thickness d (refer to FIG. **3**) of the liquid crystal layer **3**, i.e., the cell gap, was varied.

**[0087]** Table 2 shows the response time and the pointed cusp position in exemplary embodiments in which the cell gap is 3.0 μm, 3.3 μm, and 4.0 μm, respectively. FIG. **8**A, FIG. **8**B, and FIG. **8**C show the luminance in exemplary embodiments in which the cell gap is 3.0 μm, 3.6 μm, and 4.0 μm, respectively.

TABLE 2

| Capacitance | Response time (ms) | | | |
|---|---|---|---|---|
| Ratio | Tr | Tf | Tt | Cusp position (%) |
| 3.0 | 9.08 | 8.18 | 17.26 | 8.88 |
| 3.3 | 10.66 | 9.07 | 19.73 | 8.95 |

TABLE 2-continued

| Capacitance | Response time (ms) | | | |
|---|---|---|---|---|
| Ratio | Tr | Tf | Tt | Cusp position (%) |
| 3.6 | 12.59 | 9.67 | 22.26 | 10.00 |
| 4.0 | 14.2 | 10.19 | 24.39 | 10.97 |

Herein, Tr, Tf, and Tt represent a rising time, a falling time, and a total time, which is a sum of the rising time and the falling time, respectively.

**[0088]** As shown in Table 2 and FIG. **8**A to FIG. **8**C, as the cell gap is reduced, the cusp position is lowered, and in an embodiment in which the cell gap is approximately 3.6 μm or less, the cusp Pc is located at a luminance of equal to or less than 10%. In all embodiments in which the cell gap is approximately 3.0 μm or more, the response time was observed to exceed approximately 17 ms.

**[0089]** Next, in an exemplary embodiment in which the cell gap is fixed at 3.6 μm, the response time and the luminance were measured while varying the liquid crystal material and the capacitance ratio. The liquid crystal composition B and the liquid crystal composition C were selected as the liquid crystal material, in addition to the above-described liquid crystal composition A. The dielectric anisotropy and the rotational viscosity of the liquid crystal composition B are 15.1 and 89, respectively. The dielectric anisotropy and the rotational viscosity of the liquid crystal composition C are 12.9 and 76, respectively.

**[0090]** Table 3 illustrates the response time and the cusp position measured when varying the capacitance ratios in liquid crystal displays comprising the liquid crystal compositions A, B, and C. FIG. **9**A, FIG. **9**B, and FIG. **9**C illustrate luminances of the liquid crystal displays comprising the liquid crystal compositions C, B, and A, respectively, in a state in which the capacitance ratio is fixed to 0.5.

TABLE 3

| LC | Capacitance | Response time (ms) | | | Cusp |
|---|---|---|---|---|---|
| Composition | Ratio | Tr | Tf | Tt | position (%) |
| C | 0.51 | 15.05 | 6.32 | 21.37 | 13.1 |
| B | 0.45 | 14.94 | 7.96 | 22.9 | 10.0 |
| A | 0.4 | 12.59 | 9.67 | 22.26 | 10.00 |

**[0091]** As shown in Table 3 and FIG. **9**A to FIG. **9**C, as the dielectric anisotropy is lowered, the cusp position is raised. In Table 3, it can be observed that there is almost no change in the total response time Tt since the falling time Tf becomes short while the rising time Tr becomes long as the dielectric constant is lowered.

**[0092]** FIG. **10** illustrates voltage-luminance curves for liquid crystal displays comprising the liquid crystal composition A and the liquid crystal composition C. The luminance curve for the liquid crystal display comprising the liquid crystal composition A, having a high dielectric constant, has a steeper slope than that for the liquid crystal display comprising the liquid crystal composition C. The luminance and the voltage of a pixel at the cusp position for the liquid crystal A is lower than for the liquid crystal C. Thus a final luminance of a pixel in the first frame F**1** is reduced as the dielectric constant is increased, so that the position of the cusp Pc is

lower. A final voltage of the pixel is approximately 1.6V. As the dielectric constant is increased, the final voltage of the pixel is slightly reduced.

**[0093]** Next, in a state in which the cell gap is set to a fixed value, the response speed and the luminance for a liquid crystal display comprising the liquid crystal A was measured while the capacitance ratio was varied.

**[0094]** Table 4 shows the response time and the cusp position in an embodiment in which the capacitance ratio is 0.232, 0.4, 0.6, or 0.8 when the cell gap is 3.6 μm. FIG. **11**A, FIG. **11**B, and FIG. **11**C show a luminance curves for capacitance ratios of 0.232, 0.4, and 0.6 in an embodiment in which the cell gap is fixed to 3.6 μm.

TABLE 4

| Capacitance | Response time (ms) | | | |
|---|---|---|---|---|
| Ratio | Tr | Tf | Tt | Cusp position (%) |
| 0.232 | 15.38 | 10.29 | 25.67 | 18.77 |
| 0.4 | 12.59 | 9.67 | 22.26 | 10.00 |
| 0.6 | 6.62 | 9.33 | 15.95 | 3.70 |
| 0.8 | 5.11 | 9.13 | 14.24 | 2.48 |

**[0095]** As shown in Table 4 and FIG. **11**A to FIG. **11**C, in an embodiment in which the capacitance ratio is 0.4 or more, the cusp position is equal to or less than 10%, while in an embodiment in which the capacitance ratio is 0.6 or more, the response time is also below 16 ms.

**[0096]** Table 5 shows the response time and the cusp position for each of the capacitance ratios 0.4, 0.5, 0.55, and 0.6 in an embodiment in which the cell gap is fixed at 3.3 μm. FIG. **12**A, FIG. **12**B, and FIG. **12**C show luminance curves for capacitance ratios of 0.5, 0.55, and 0.6 in an embodiment in which the cell gap is fixed at 3.0 μm, respectively.

TABLE 5

| Capacitance | Response time (ms) | | | |
|---|---|---|---|---|
| Ratio | Tr | Tf | Tt | Cusp position (%) |
| 0.4 | 10.66 | 9.07 | 19.73 | 8.9 |
| 0.5 | 7.33 | 9.41 | 16.74 | 4.9 |
| 0.55 | 5.7 | 8.67 | 14.37 | 4.7 |
| 0.6 | 5.19 | 8.68 | 13.87 | 3.4 |

**[0097]** As shown in Table 5 and FIG. **12**A to FIG. **12**C, in an embodiment in which the capacitance ratio is 0.4 or more, the cusp position is below 10%, while in an embodiment in which the capacitance ratio is 0.5 or more, the response time is below 16 ms.

**[0098]** In a state in which the capacitance is set to a fixed value, the response time and the luminance with respect to each of the liquid crystal compositions A, B, and C were measured.

**[0099]** Table 6 shows the response time and the cusp position with respect to the liquid crystal compositions A, B, and C in a state in which the capacitance ratio is fixed at 0.5. FIG. **13**A, FIG. **13**B, and FIG. **13**C show the luminance of liquid crystal displays comprising the liquid crystal compositions C, B, and A, respectively, under the same conditions.

TABLE 6

| LC | Capacitance | Response time (ms) | | | Cusp |
|---|---|---|---|---|---|
| Composition | Ratio | Tr | Tf | Tt | position (%) |
| C | 0.5 | 14.52 | 9.03 | 23.55 | 12.0 |
| B | 0.5 | 9.66 | 7.89 | 17.55 | 8.3 |
| A | 0.5 | 8.27 | 9.5 | 17.77 | 5.7 |

**[0100]** Table 7 shows the response time and the cusp position with respect to the liquid crystals A, B, and C in a state in which the capacitance is fixed to 0.6. FIG. **14**A, FIG. **14**B, and FIG. **14**C show the luminance of liquid crystal displays comprising the liquid crystal compositions C, B, and A, respectively, under the same conditions.

TABLE 7

| LC | Capacitance | Response time (ms) | | | Cusp |
|---|---|---|---|---|---|
| Composition | Ratio | Tr | Tf | Tt | position (%) |
| C | 0.6 | 14.28 | 8.93 | 23.21 | 10.1 |
| B | 0.6 | 7.2 | 7.79 | 14.99 | 5.5 |
| A | 0.6 | 6.62 | 9.33 | 15.95 | 3.70 |

**[0101]** As shown in Table 6, Table 7, and FIG. **13**A to FIG. **14**C, as the dielectric anisotropy is increased, the cusp position is lowered. As shown in Table 6 and Table 7, the total response time Tt is approximately 16 ms in the exemplary embodiment comprising the liquid crystal compositions B and A, but in the exemplary embodiment comprising the liquid crystal composition C, which has a low dielectric anisotropy, the cusp position is over 10% and the total response time Tt is over 20 ms even though the capacitance ratio is set to 0.6. From this result, it can be observed that the dielectric anisotropy is desirably selected to be approximately 14 or more.

**[0102]** The response time and the cusp position were measured using the liquid crystal compositions D and E, which have almost the same dielectric anisotropy and rotational viscosity as the other liquid crystals, but have different elastic coefficients. The dielectric anisotropy, the rotational viscosity, and the effective elastic coefficient Keff of the liquid crystal composition D are 15.2, 100, and 12.5 (splay elastic coefficient K11=12.9 and band elastic coefficient K33=11.4), respectively. The dielectric anisotropy, the rotational viscosity, and the effective elastic coefficient Keff of the liquid crystal composition E are 15.7, 100, and 9.6 (K11=8.9 and K33=11.8), respectively.

**[0103]** Table 8 shows the response time and the cusp position for the liquid crystal compositions D and E when the capacitance ratios are 0.232 and 0.6. FIG. **15**A and FIG. **15**B show the luminance of liquid crystal displays comprising the liquid crystal compositions D and E in a state in which the capacitance is set to 0.6.

TABLE 8

| LC | Capacitance | Response time (ms) | | | Cusp |
|---|---|---|---|---|---|
| Composition | Ratio | Tr | Tf | Tt | position (%) |
| D | 0.232 | 15.57 | 8.9 | 24.47 | 20.1 |
| | 0.6 | 9.33 | 8.41 | 17.24 | 7.5 |
| E | 0.232 | 14.86 | 12.19 | 27.05 | 12.16 |
| | 0.6 | 5.51 | 11.02 | 16.53 | 2.7 |

**[0104]** As shown in Table 8, FIG. **15**A, and FIG. **15**B, as the effective elastic coefficient is reduced, the cusp position is lowered. When the effective elastic coefficient is 10 or less, the cusp position is below 10% and the total response time Tt is approximately 16 ms when the capacitance ratio is equal to 0.6.

**[0105]** To determine an influence of the pitch of liquid crystal layer **3** on the response time and the cusp position, an experiment was performed in a state in which the pitch of the liquid crystal A was varied.

**[0106]** Table 9 shows the response time and the cusp position measured when the pitch of a liquid crystal display comprising the liquid crystal composition A was set to 40, 70, 100, or 140 with the capacitance ratios of 0.4 and 0.6, respectively. FIG. **16**A, FIG. **16**B, and FIG. **16**C show the luminance of liquid displays having pitches of 70, 100, or 130 in a state in which the capacitance ratio is set to 0.6.

TABLE 9

| | Capacitance | Response time (ms) | | | Cusp |
|---|---|---|---|---|---|
| Pitch | Ratio | Tr | Tf | Tt | position (%) |
| 40 | 0.4 | 14.95 | 9.28 | 24.23 | 11.29 |
| | 0.6 | 7.43 | 9.01 | 16.44 | 6.1 |
| 70 | 0.4 | 12.59 | 9.67 | 22.26 | 10.00 |
| | 0.6 | 6.62 | 9.33 | 15.95 | 4.9 |
| 100 | 0.4 | 11.08 | 9.83 | 20.91 | 8.64 |
| | 0.6 | 6.4 | 9.5 | 15.9 | 4.6 |
| 130 | 0.4 | 10.52 | 9.93 | 20.45 | 8.24 |
| | 0.6 | 6.27 | 9.56 | 15.85 | 3.5 |

**[0107]** As shown in Table 9 and FIG. **16**A to FIG. **16**C, as the pitch is increased, the rising time Tr and the total response time Tt become shorter, and the cusp position is lowered. Accordingly, it has been observed that a pitch set to 100 or more is desirable for low voltage driving since the cusp position is below approximately 10% when the capacitance ratio is approximately 0.4, and the response time is below approximately 16 ms for a capacitance of 0.6 when the pitch is set to 100 or more.

**[0108]** Although exemplary embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present invention should not be limited to the disclosed embodiments and that various other changes and modifications may be made by those skilled in the art without departing from the scope or spirit of the invention.

What is claimed is:

**1**. A liquid crystal display, comprising:

a thin film transistor;

a liquid crystal capacitor, which is electrically connected to the thin film transistor and comprises a liquid crystal layer; and

a storage capacitor, which is electrically connected to the thin film transistor in parallel to the liquid crystal capacitor,

wherein the liquid crystal layer has a positive dielectric anisotropy and is disposed in a twisted nematic mode, and

a capacitance ratio of a capacitance of the storage capacitor to a capacitance of the liquid crystal capacitor is approximately 0.4 or more.

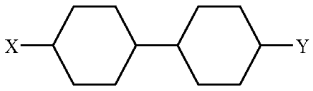
**2**. The liquid crystal display of claim **1**, wherein the capacitance ratio is approximately 0.7 or less.

**3**. The liquid crystal display of claim **2**, wherein a dielectric anisotropy of the liquid crystal layer is approximately 14 or more.

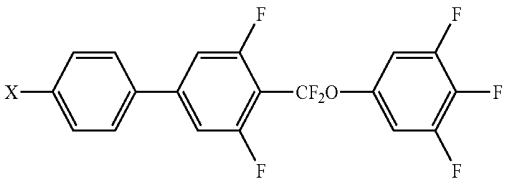
**4**. The liquid crystal display of claim **3**, wherein the dielectric anisotropy of the liquid crystal layer is in a range of approximately 15 to approximately 18.

**5**. The liquid crystal display of claim **4**, wherein the dielectric anisotropy of the liquid crystal layer is in a range of approximately 15.1 to approximately 17.3.

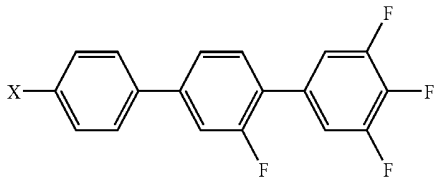
**6**. The liquid crystal display of claim **1**, wherein the liquid crystal layer comprises a liquid crystal composition selected from groups each consisting of liquid crystal compositions I to IV, wherein the liquid crystal composition I comprises compounds of formulas



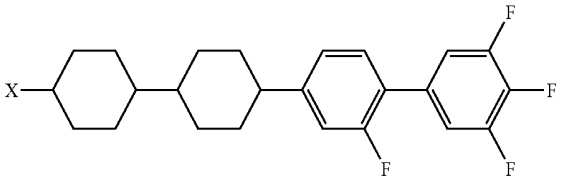

in an amount of approximately 31.5 weight percent,



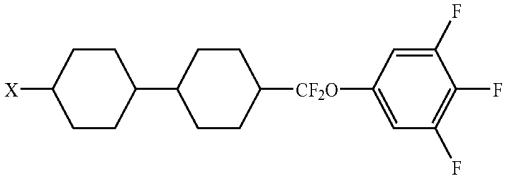

in an amount of approximately 15 weight percent,



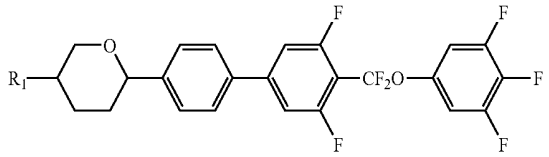

in an amount of approximately 10 weight percent,



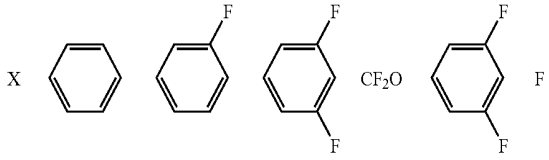

in an amount of approximately 7 weight percent,



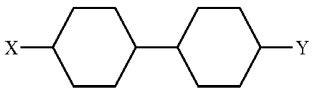

in an amount of approximately 18.5 weight percent,



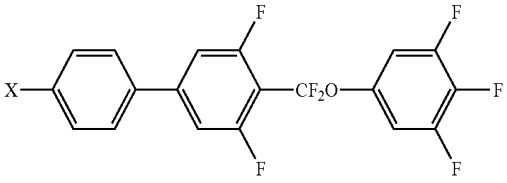
in an amount of approximately 12 weight percent,



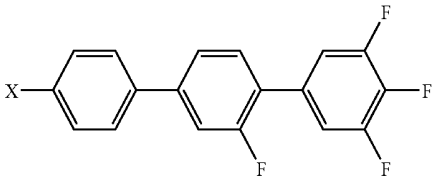
in an amount of approximately 6 weight percent, the liquid crystal composition II comprises compounds of the formulas



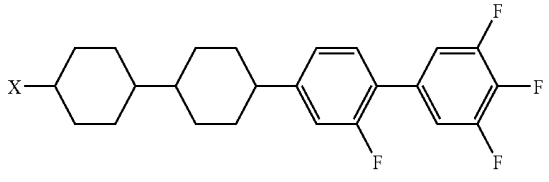
in an amount of approximately 41 weight percent,



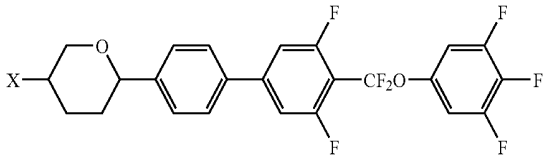
in an amount of approximately 13 weight percent,



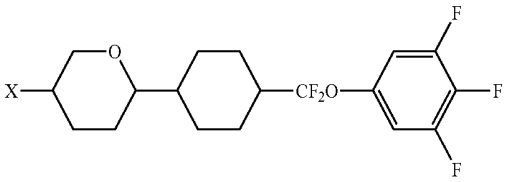
in an amount of approximately 8.5 weight percent,



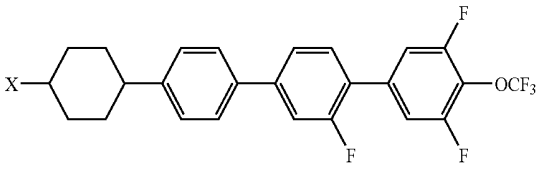
in an amount of approximately 6.5 weight percent,



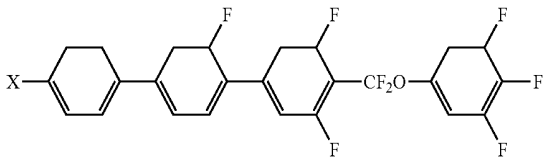
in an amount of approximately 12 weight percent,



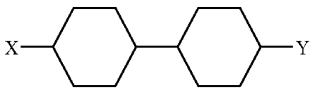
in an amount of 8 weight percent,



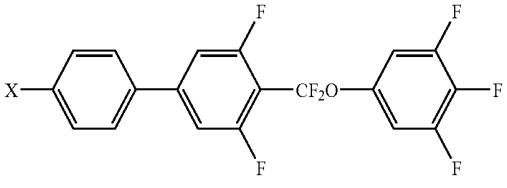
in an amount of approximately 6 weight percent,



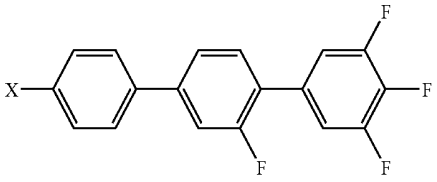
in an amount of approximately 5 weight percent, the liquid crystal composition III comprises compounds of the formulas



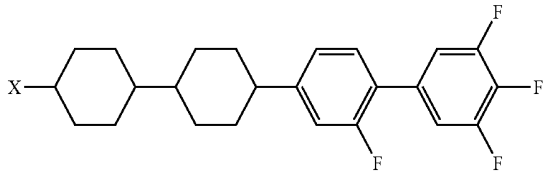
in an amount of approximately 21.5 weight percent,



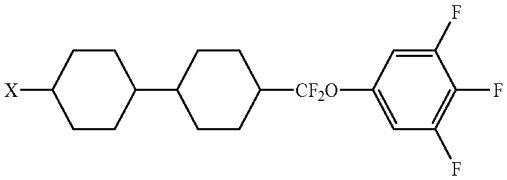
in an amount of approximately 10 weight percent,



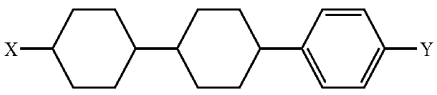
in an amount of approximately 7 weight percent,



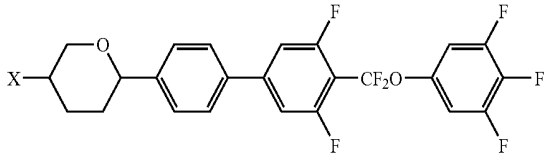
in an amount of approximately 5 weight percent,



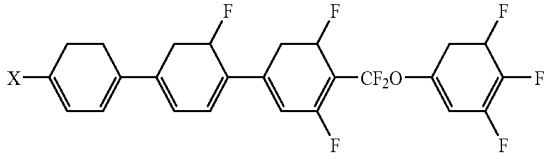
in an amount of approximately 27 weight percent,



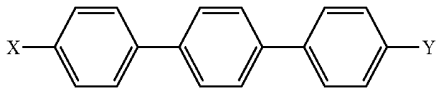
in an amount of approximately 10 weight percent,



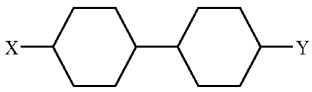
in an amount of approximately 13.5 weight percent,



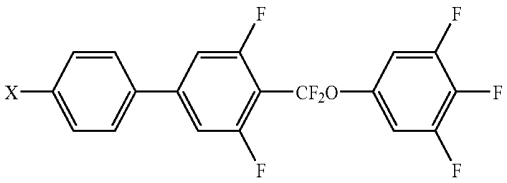
in an amount of approximately 2 weight percent,



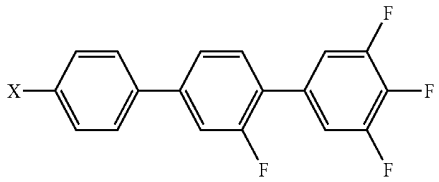
in an amount of approximately 4 weight percent, and the liquid crystal composition IV comprises compounds of the formulas



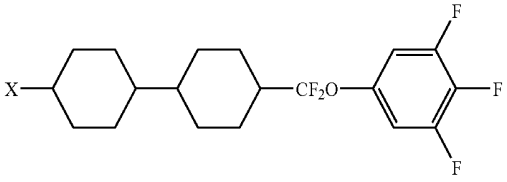
in an amount of approximately 12 weight percent,



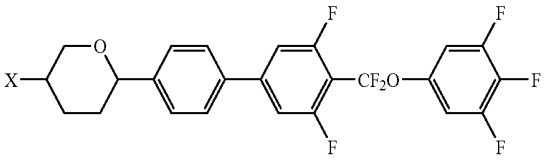
in an amount of approximately 5.5 weight percent,



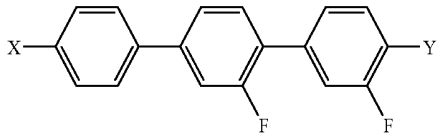
in an amount of approximately 10 weight percent,



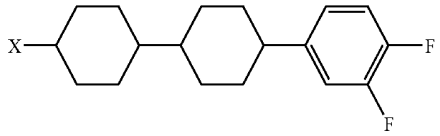
in an amount of approximately 35 weight percent,



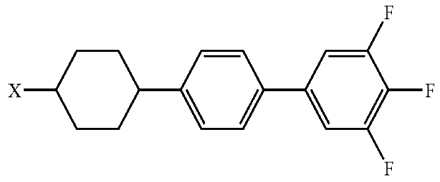
in an amount of approximately 14 weight percent,



in an amount of approximately 5 weight percent,



in an amount of approximately 8.5 weight percent,



in an amount of approximately 10 weight percent, based on a total weight of the liquid crystal composition, and X and Y are independently one of an alkyl group, an alkynyl group and an alkoxy group.

**7**. The liquid crystal display of claim **4**, wherein a thickness of the liquid crystal layer is in a range of approximately 3 micrometers to approximately 4 micrometers.

**8**. The liquid crystal display of claim **7**, wherein the thickness of the liquid crystal layer is in a range of approximately 3.3 micrometers to approximately 3.6 micrometers.

**9**. The liquid crystal display of claim **2**, wherein a thickness of the liquid crystal layer is in a range of approximately 3 micrometers to approximately 4 micrometers.

**10**. The liquid crystal display of claim **9**, wherein the thickness of the liquid crystal layer is in a range of approximately 3 micrometers to approximately 4 micrometers.

**11**. The liquid crystal display of claim **2**, wherein an effective elastic coefficient of the liquid crystal layer is approximately 10 or less.

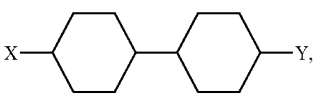
**12**. The liquid crystal display of claim **2**, wherein a pitch of the liquid crystal layer is approximately 100 or more.

**13**. The liquid crystal display of claim **1**, wherein

the liquid crystal display is in a normally white mode, and

a final luminance is approximately 10 percent or less for one frame when a voltage difference between both ends of the liquid crystal capacitor is changed from 0 volts to approximately 2.5 volts.

**14**. The liquid crystal display of claim **1**, wherein the liquid crystal layer comprises a liquid crystal composition comprising at least one compound of the formulas



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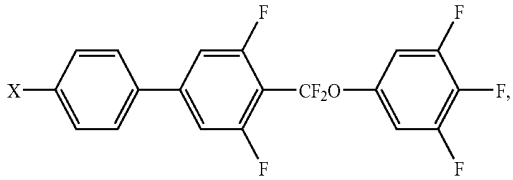

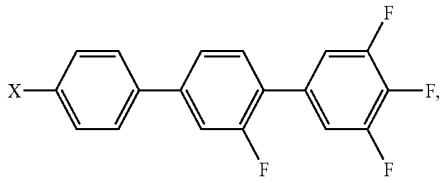

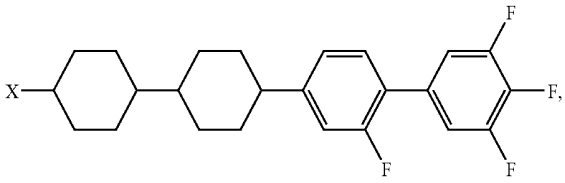

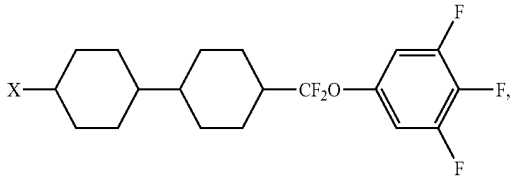

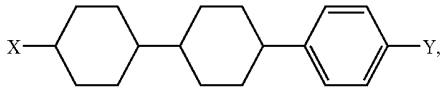

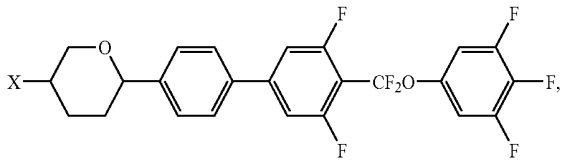

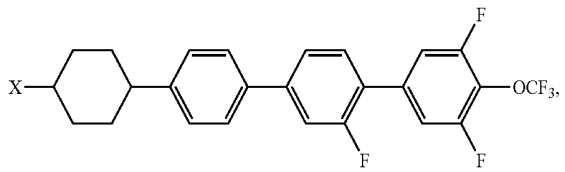

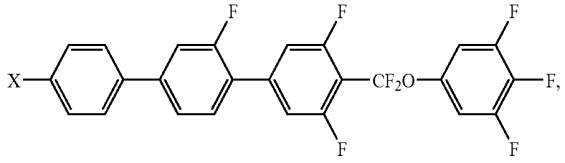

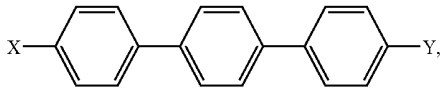

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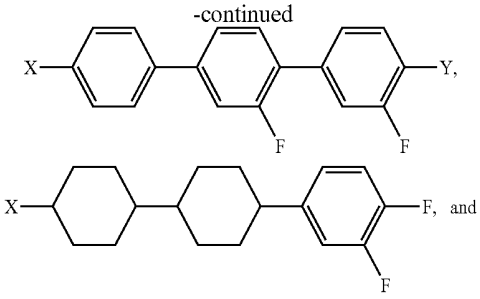


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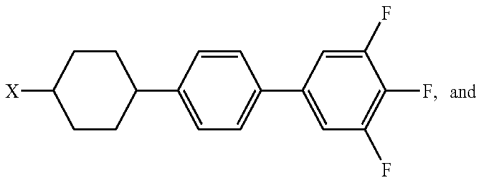


X and Y are independently one of an alkyl group, an alkynyl group and an alkoxy group.

* * * * *

| | | | |
|---|---|---|---|
| 专利名称(译) | 液晶显示器 | | |
| 公开(公告)号 | US20100066932A1 | 公开(公告)日 | 2010-03-18 |
| 申请号 | US12/504266 | 申请日 | 2009-07-16 |
| [标]申请(专利权)人(译) | 三星电子株式会社 | | |
| 申请(专利权)人(译) | SAMSUNG ELECTRONICS CO.，LTD. | | |
| 当前申请(专利权)人(译) | 三星DISPLAY CO.，LTD. | | |
| [标]发明人 | HUH SU JUNG<br>KIM MIN JAE<br>SUH DUCK JONG | | |
| 发明人 | HUH, SU-JUNG<br>KIM, MIN-JAE<br>SUH, DUCK-JONG | | |
| IPC分类号 | G02F1/1343 C09K19/02 | | |
| CPC分类号 | C09K19/3402 C09K19/44 C09K2019/0466 C09K2019/123 G02F2001/13706 C09K2019/3019 C09K2019/3422 G02F1/136213 G02F1/1396 C09K2019/3004 | | |
| 优先权 | 1020080090626 2008-09-16 KR | | |
| 其他公开文献 | US8228450 | | |
| 外部链接 | Espacenet USPTO | | |


摘要(译)

液晶显示器包括薄膜晶体管，液晶电容器，其电连接到薄膜晶体管并包括液晶层，以及存储电容器，其与液体并联地电连接到薄膜晶体管。晶体电容器，其中液晶层具有正介电各向异性并以扭曲向列模式设置，并且存储电容器的电容与液晶电容器的电容的电容比约为0.4或更大。