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(54) LIQUID CRYSTAL DISPLAY AND DRIVING DEVICE THEREOF

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(57) ABSTRACT

The present invention discloses a data driver and a liquid crystal display including the same capable of solving the problems on the liquid crystal display and of decreasing the number of input pins of an external side by generating gamma reference voltages at internal or external side. According to the present invention, a digital gamma storage is provided with digital gamma data for each of R, G and B through predetermined data bus from an external device on the basis of a predetermined gamma load signal, and a gamma reference voltage generator generates gamma reference voltages for gray display, which are used in converting display data into analog data, for each of R, G and B independently, on the basis of the stored digital gamma data for each of R, G and B. A digital-to-analog converter converts image data for each of R, G and B into analog voltages to output them on the basis of the generated gamma reference voltages. As a result, it is possible to solve the problems on image quality of the liquid crystal display as well as to decrease the number of input pins of the external side by generating the gamma reference voltages for each of R, G and B without receiving them from an external device to control so that each of the R, G and B has an independent gamma curve.

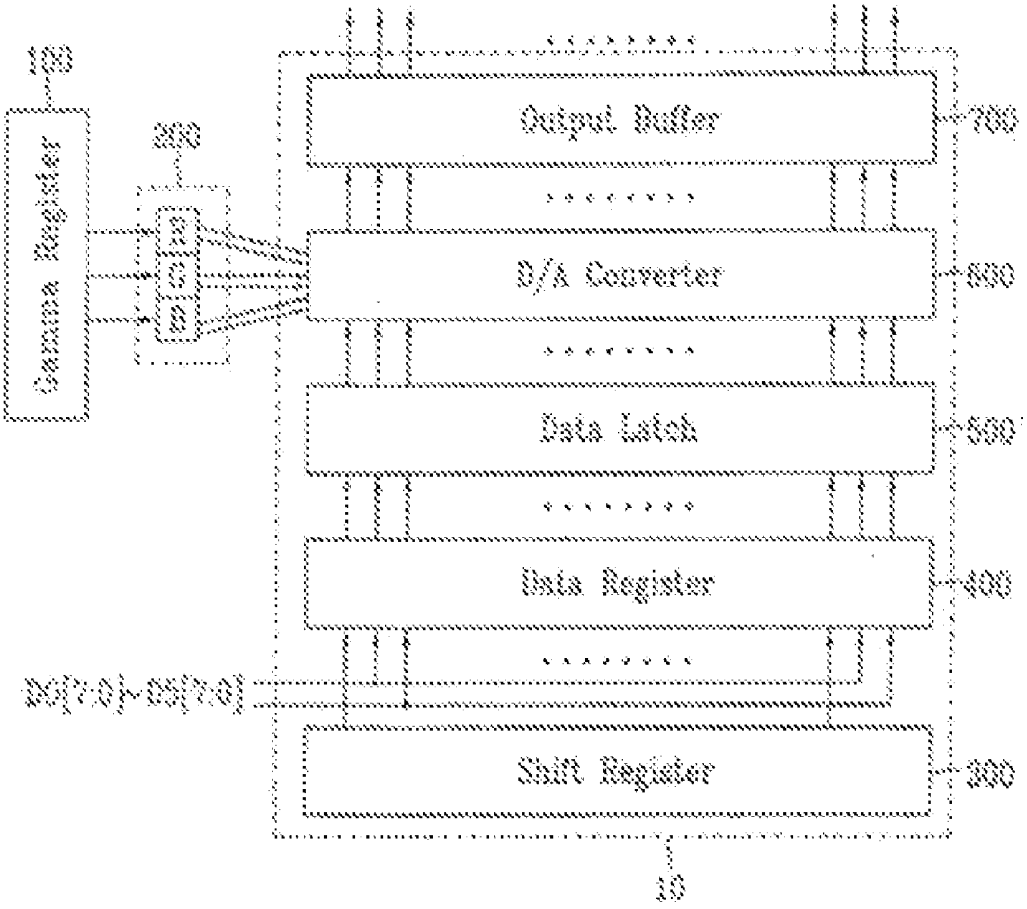


FIG. 1

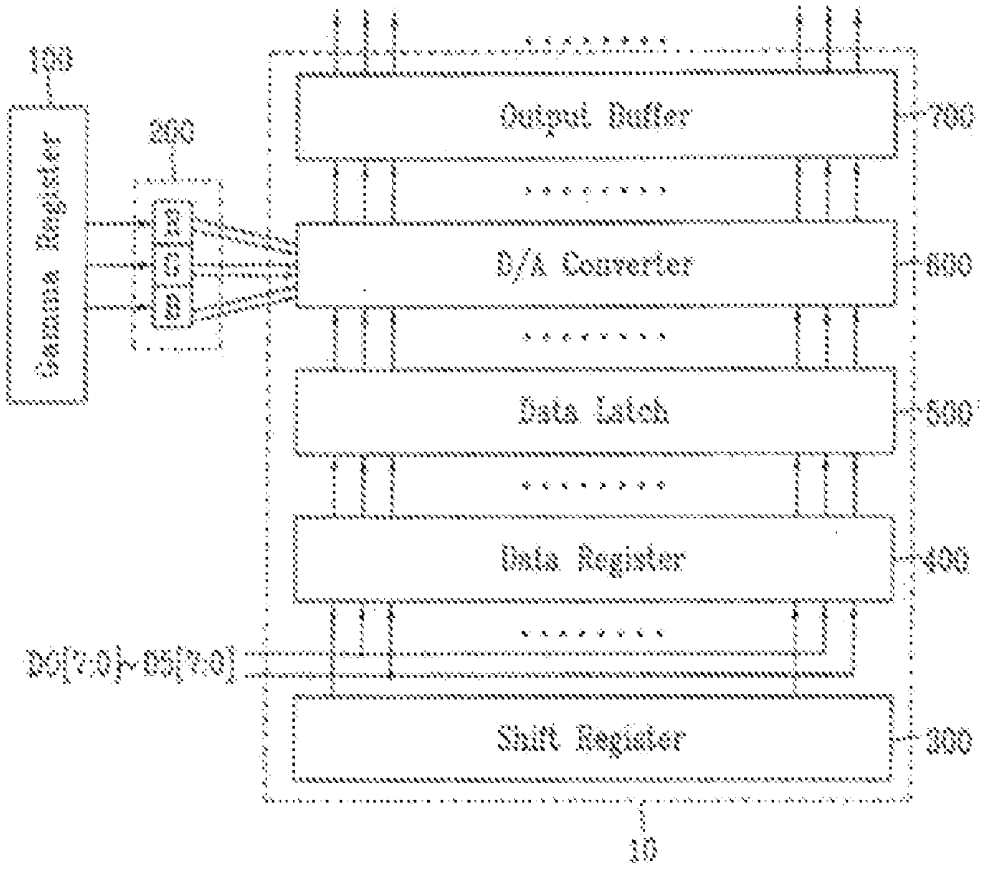

100
Gamma Register
200
R
G
B
Output Buffer
700
D/A Converter
600
Data Latch
500
Data Register
400
Shift Register
300
10
DQ[7:0]~DQ[0:7]

FIG. 2

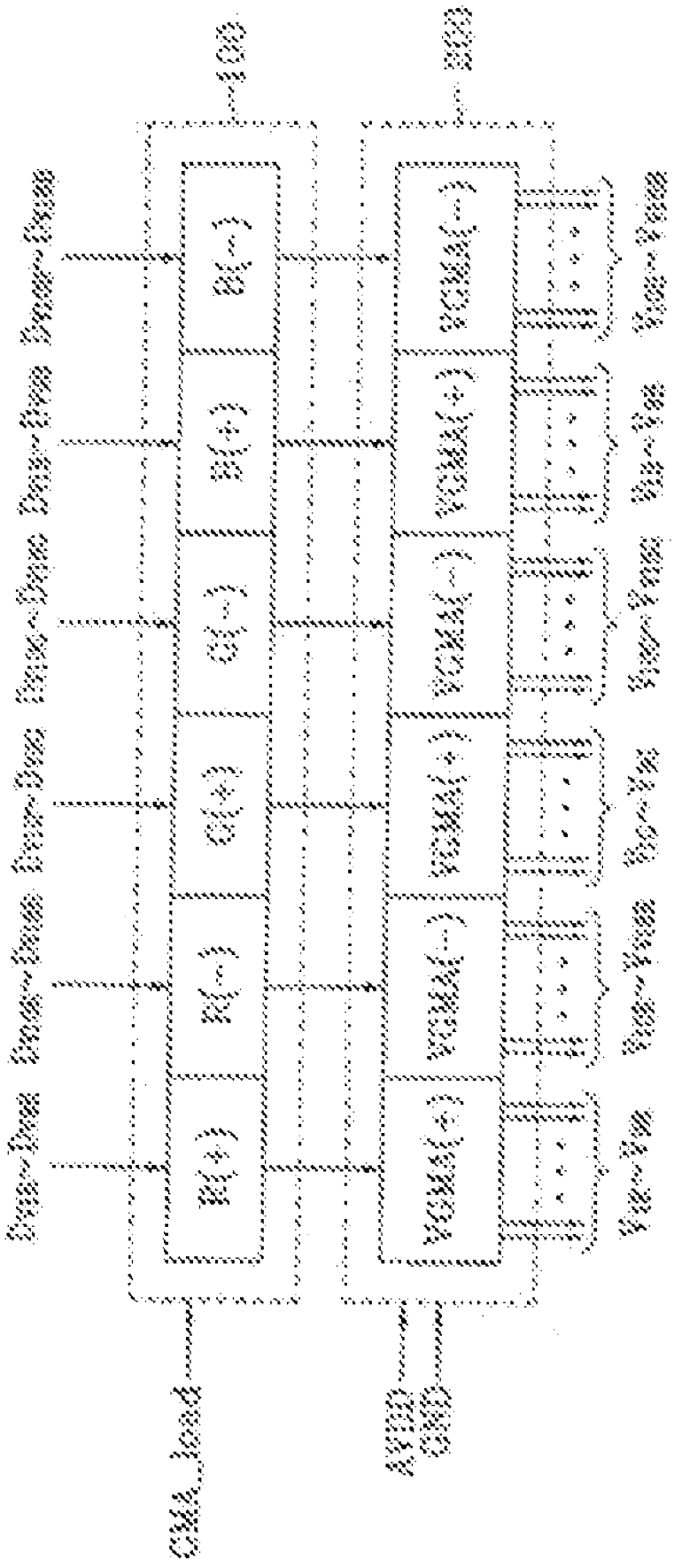
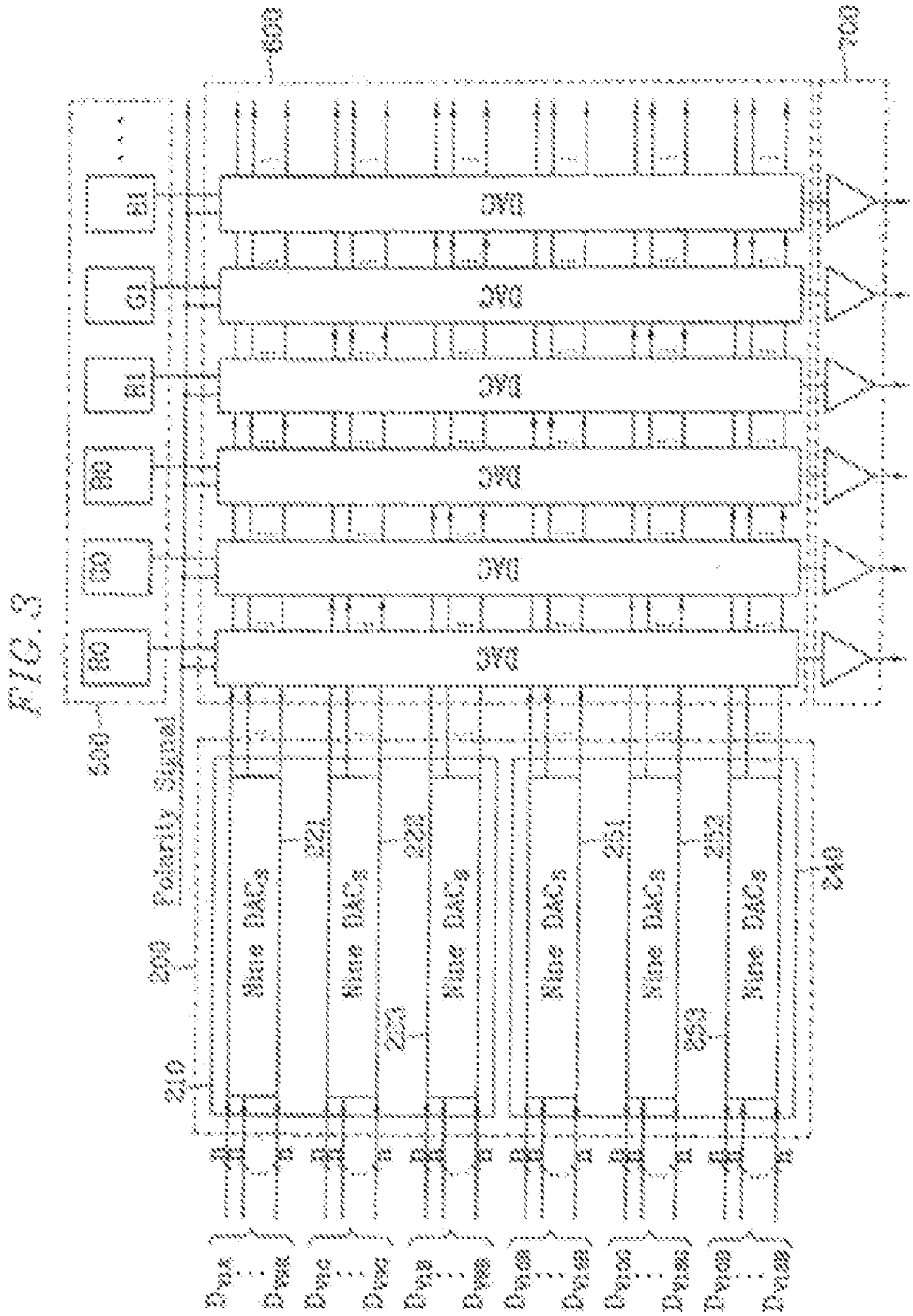


FIG. 3


600
700
500
B0
G0
R0
B1
G1
R1
DAC
DAC
DAC
DAC
DAC
DAC
Polarity Signal
200
210
221
222
223
251
252
253
240
Nine DACs
Nine DACs
Nine DACs
Nine DACs
Nine DACs
Nine DACs

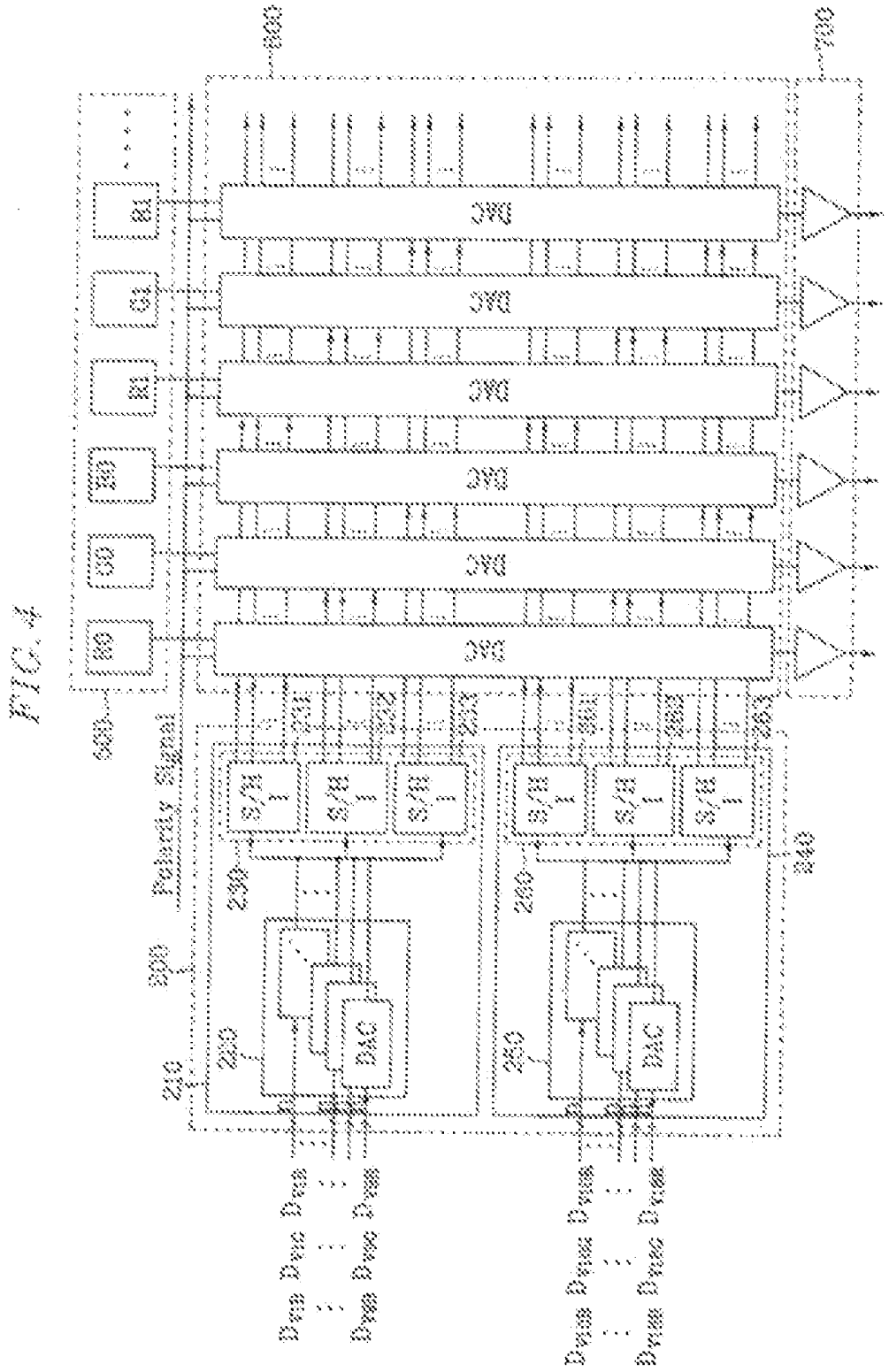


FIG. 4

FIG. 5

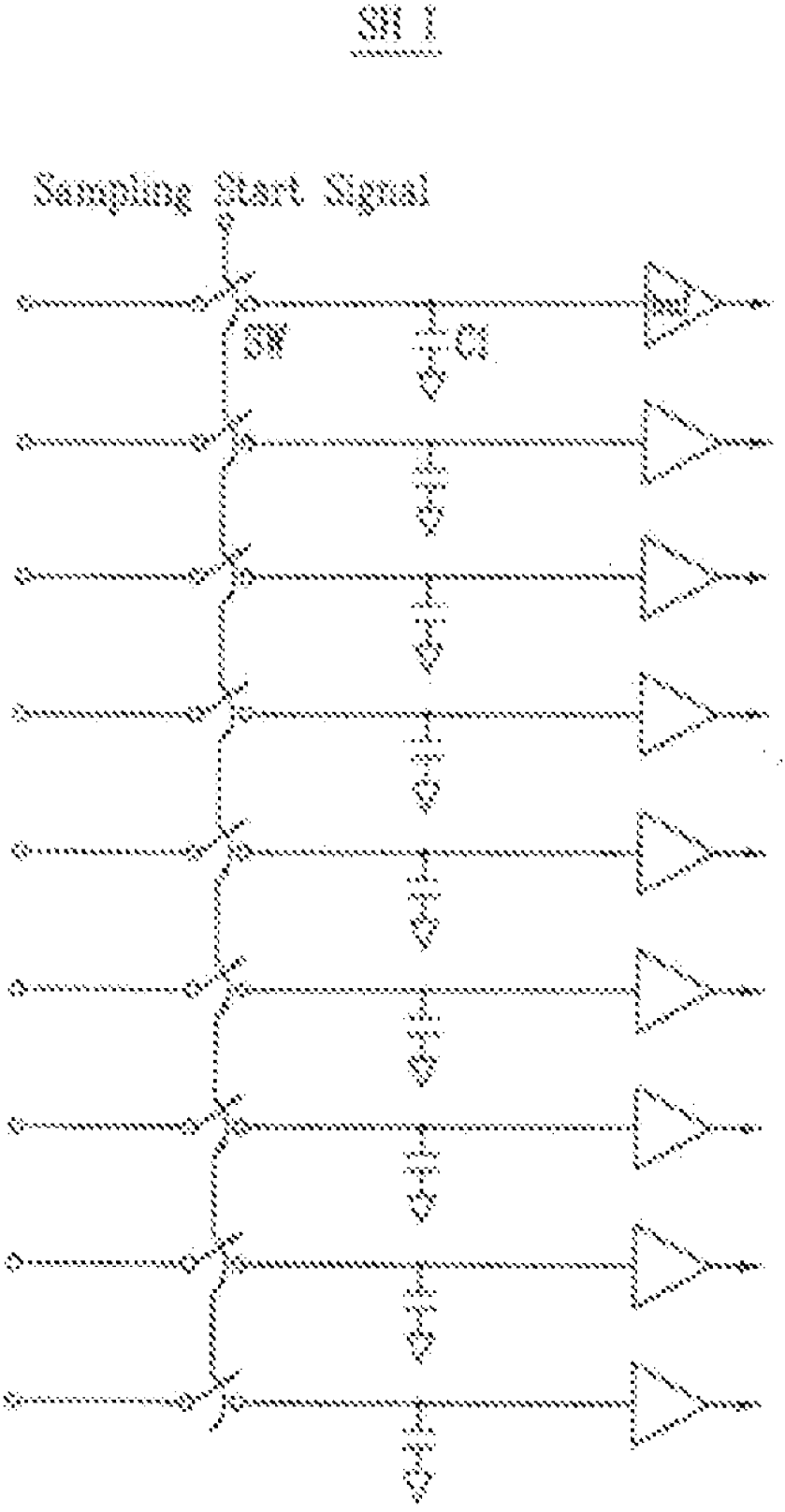

SH 1
Sampling Start Signal
SW
Data
Data
Data
Data
Data
Data
Data
Data

FIG. 6

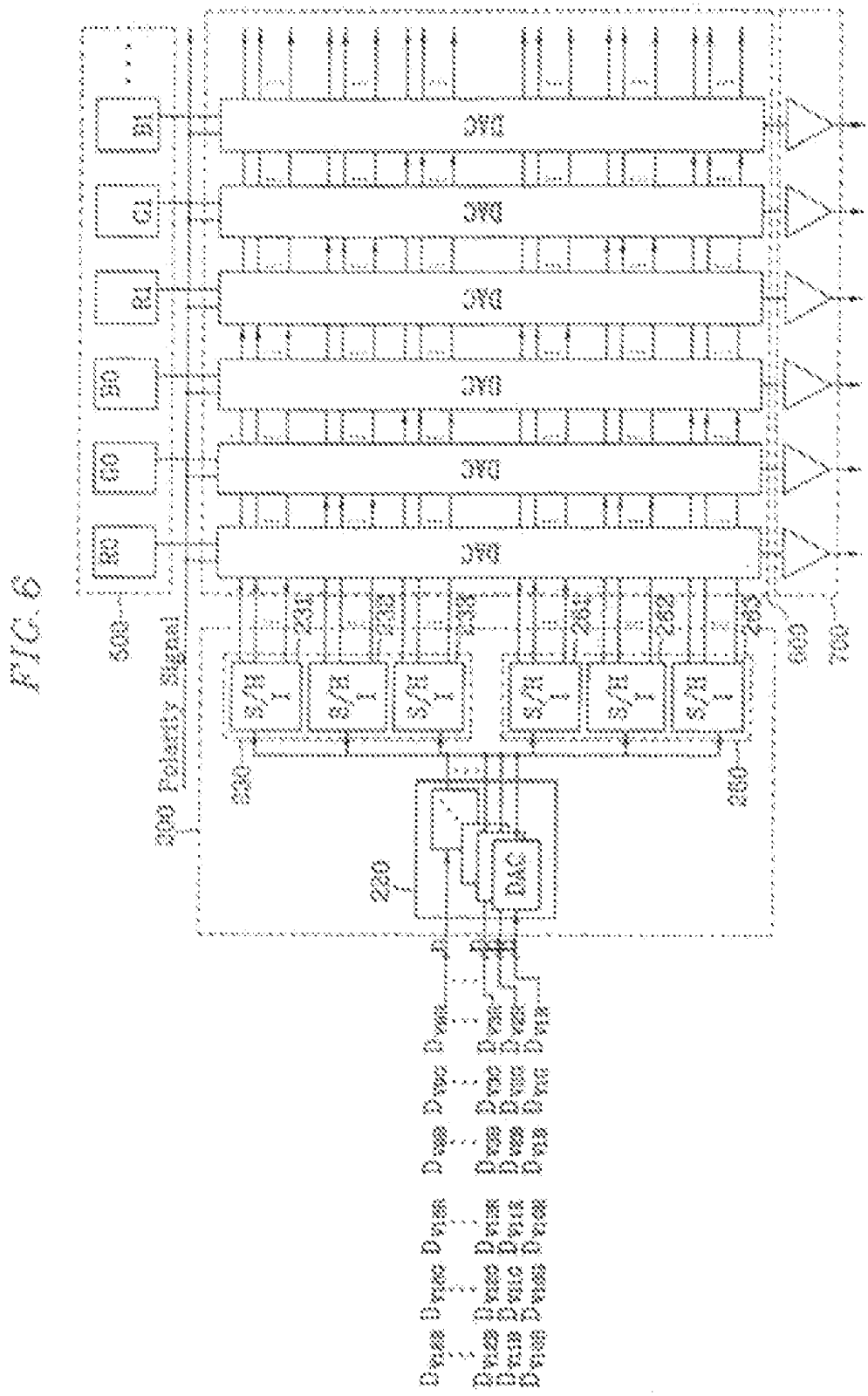


FIG. 7

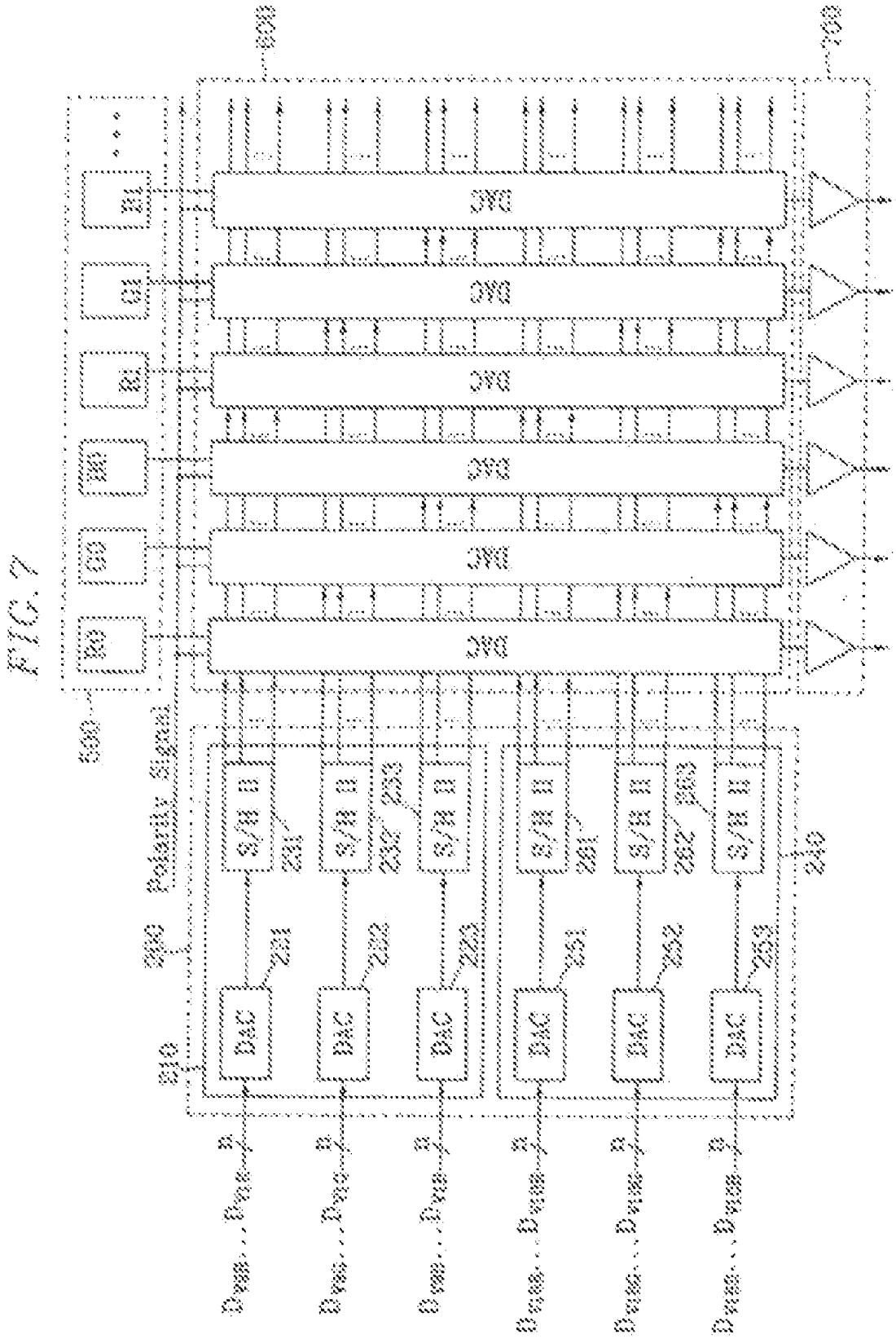

600
700
500
DAC
Polarity Signal
S/H
DAC
231
232
233
251
252
253
240

FIG. 8

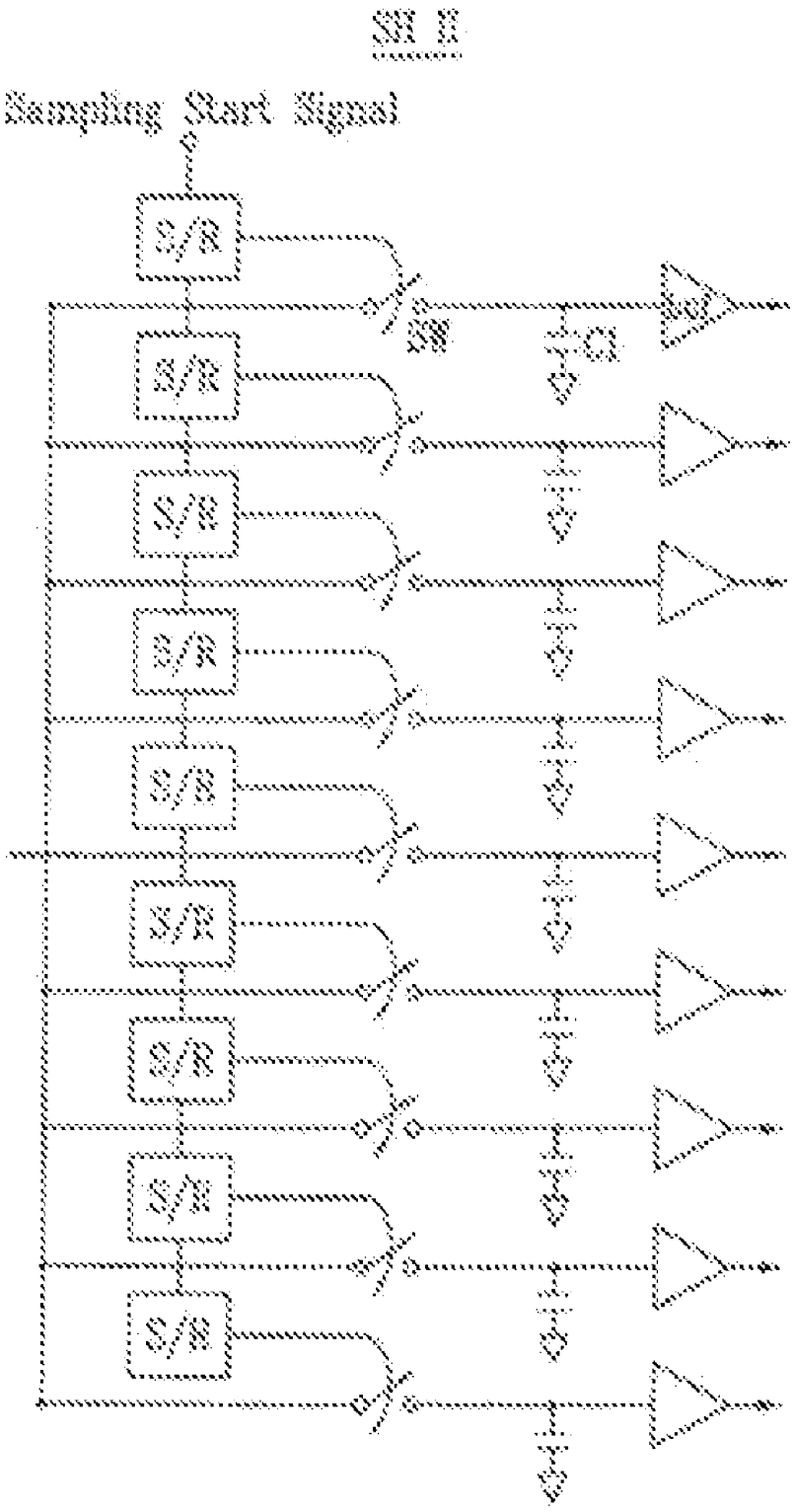


FIG. 9

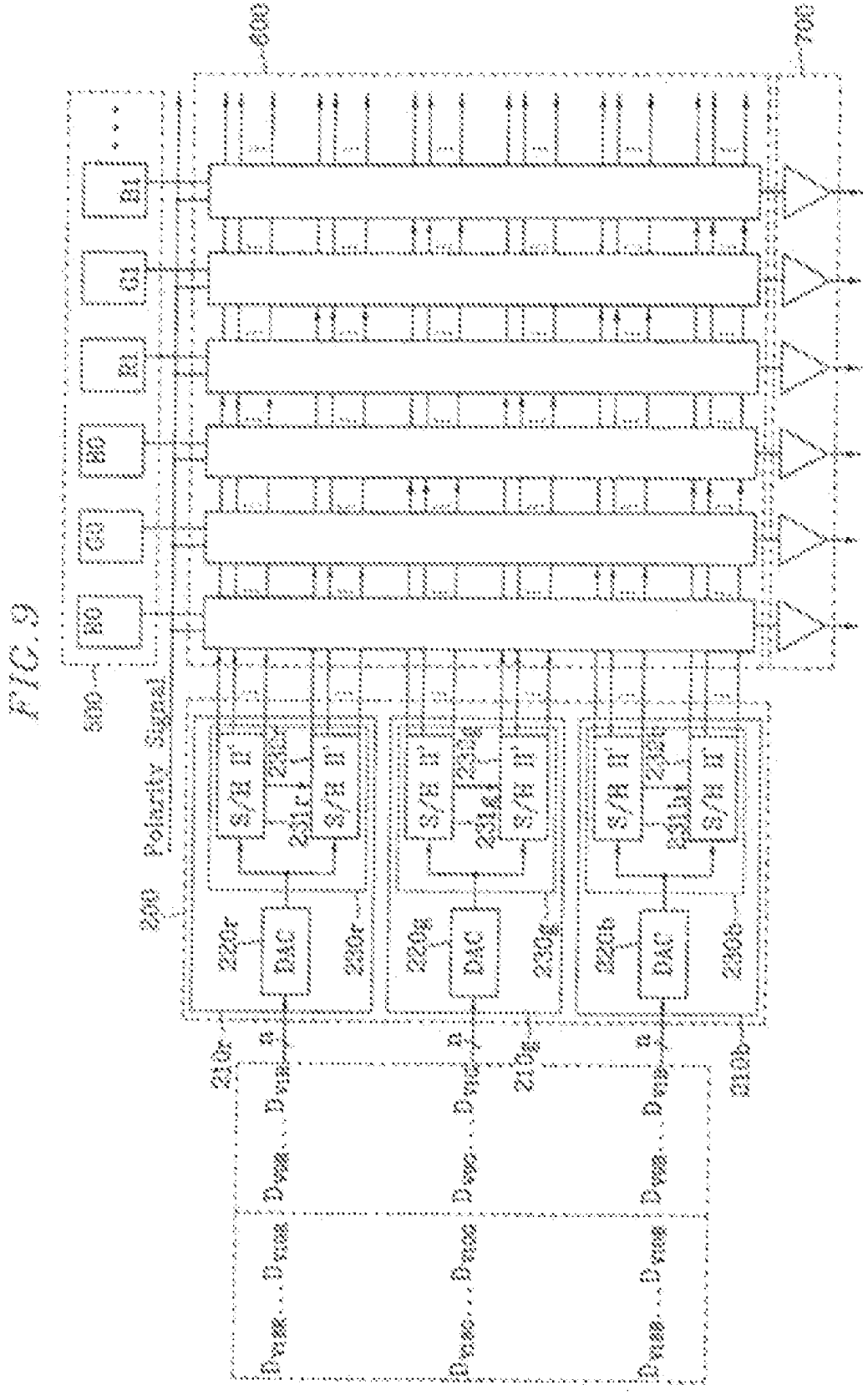

600
700
500
B0
G0
B1
G1
B1
Polarity Signal
200
S/H
DAC
220r
220g
220b
230r
230g
230b
210r
210g
210b

FIG. 10

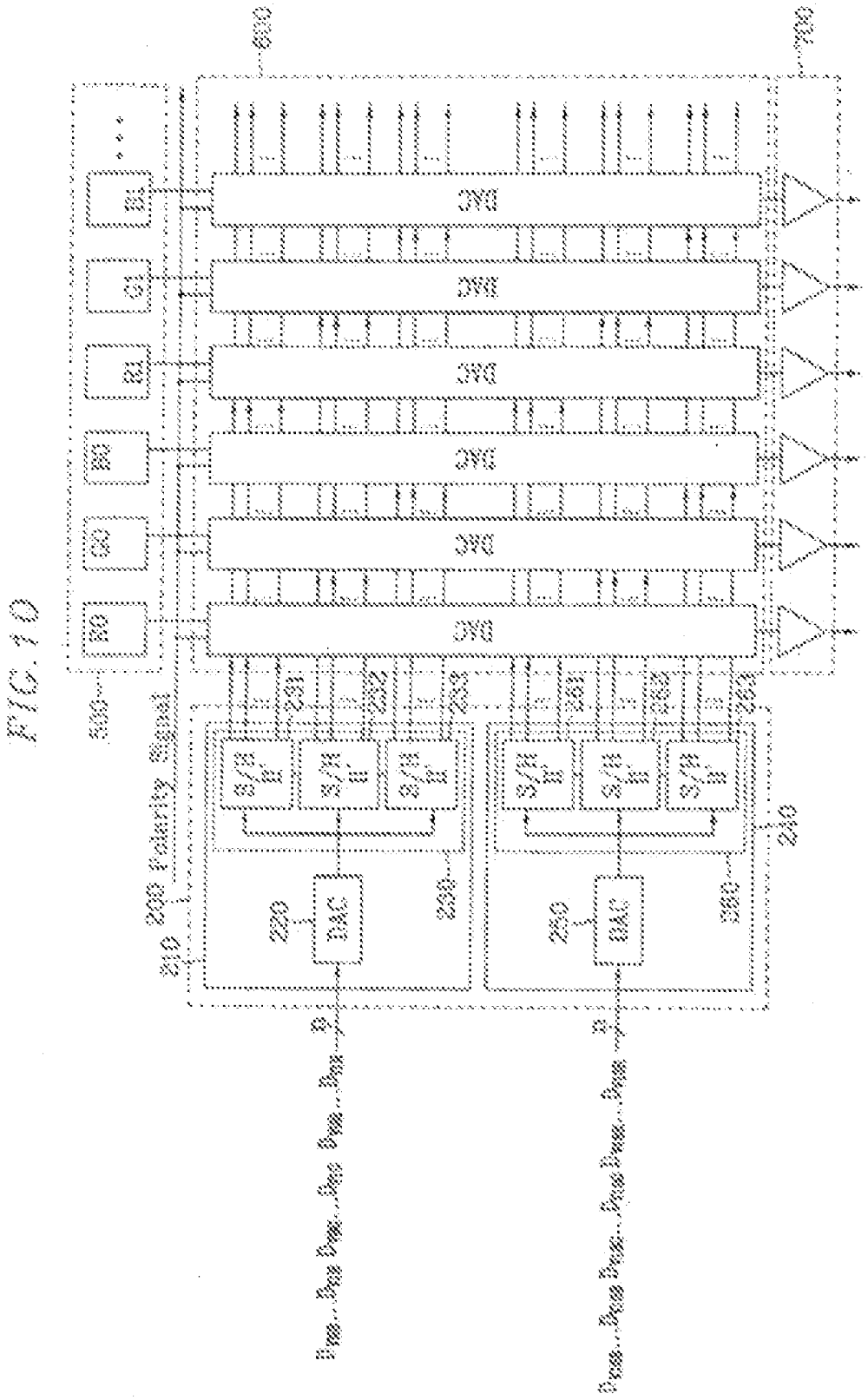

600
700
500
DAC
DAC
DAC
DAC
DAC
DAC
B1
G1
R1
B0
G0
R0
200 Polarity Signal
210
220
DAC
230
240
250
DAC
260
S/H
S/H
S/H
S/H
S/H
S/H
231
232
233
261
262
263

FIG. 11

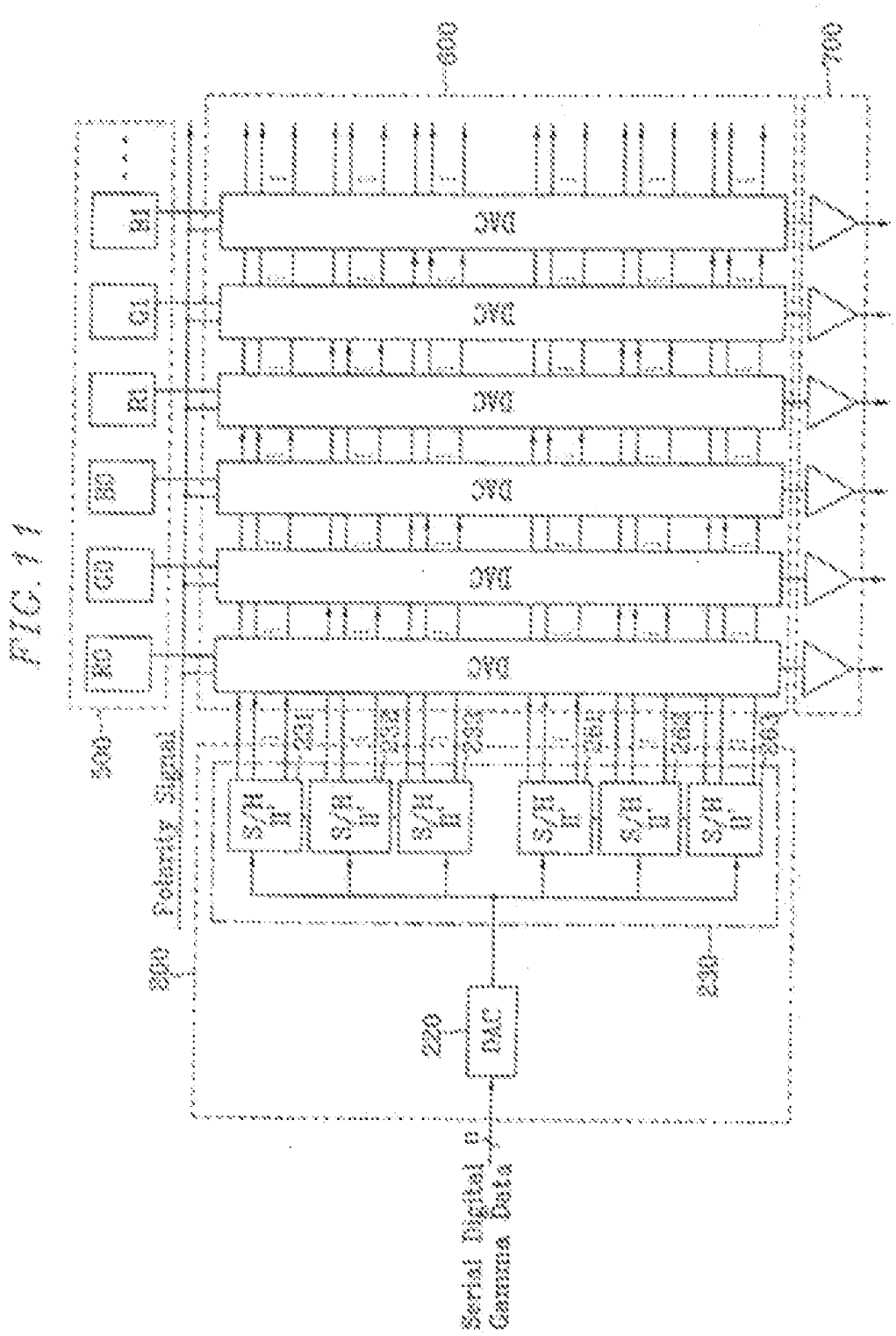

600
700
500
800
230
220
DAC
Polarity Signal
Serial Digital Gamma Data

FIG. 12

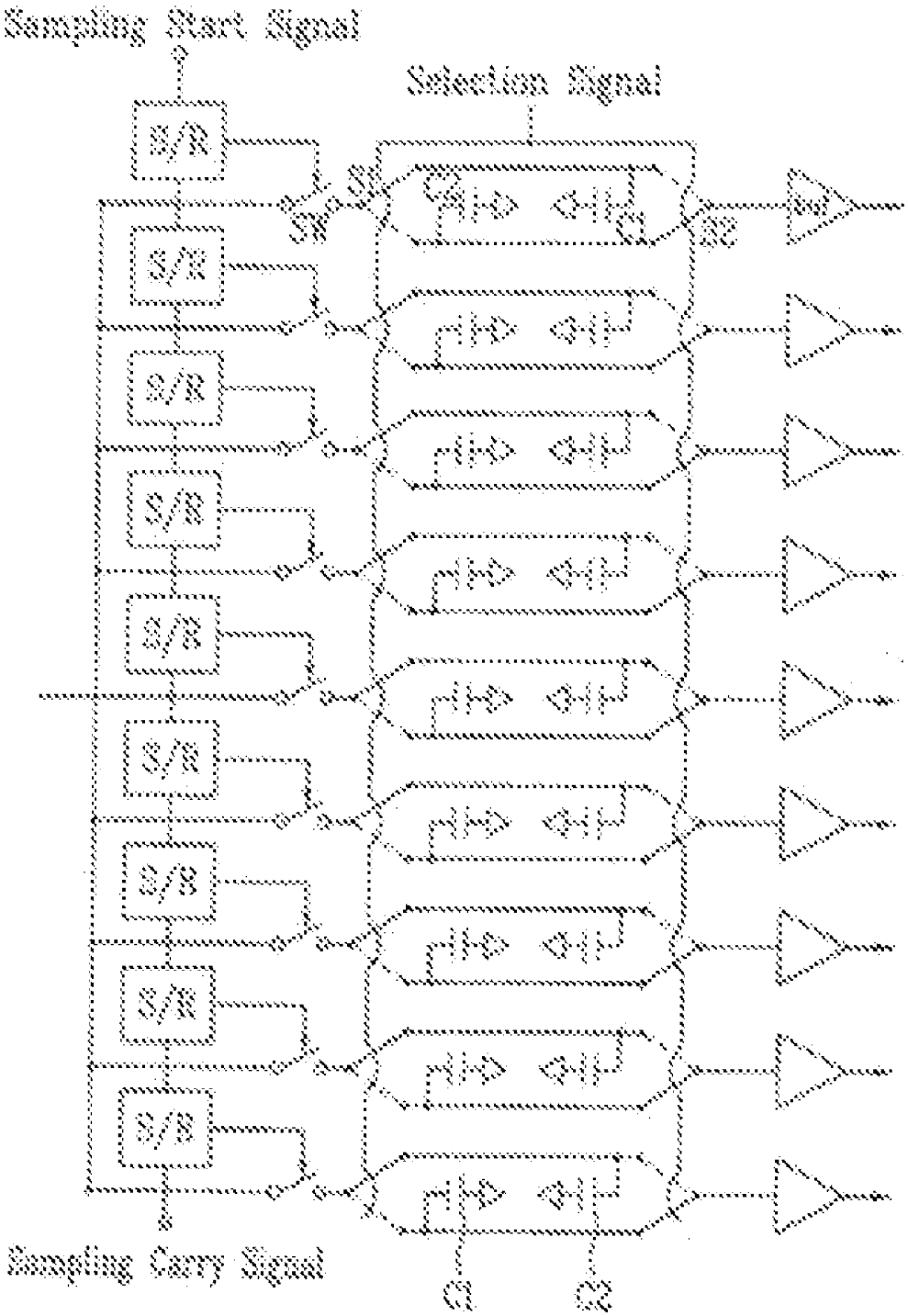
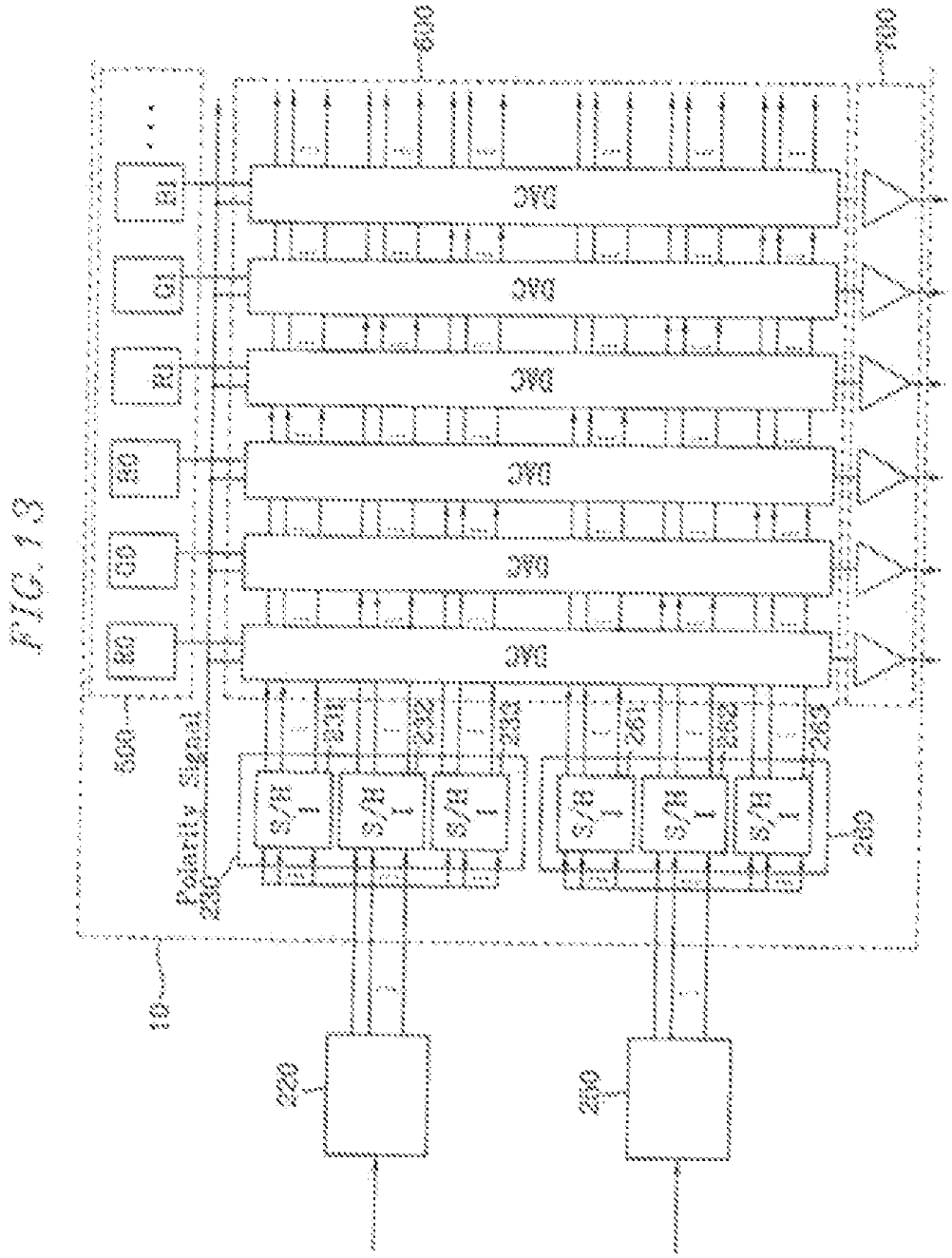

Sampling Start Signal
Selection Signal
S/R
Sampling Carry Signal
C1
C2

FIG. 13


600
700
DAC
DAC
DAC
DAC
DAC
DAC
500
Polarity Signal
230
S/H
S/H
S/H
S/H
S/H
S/H
10
220
250

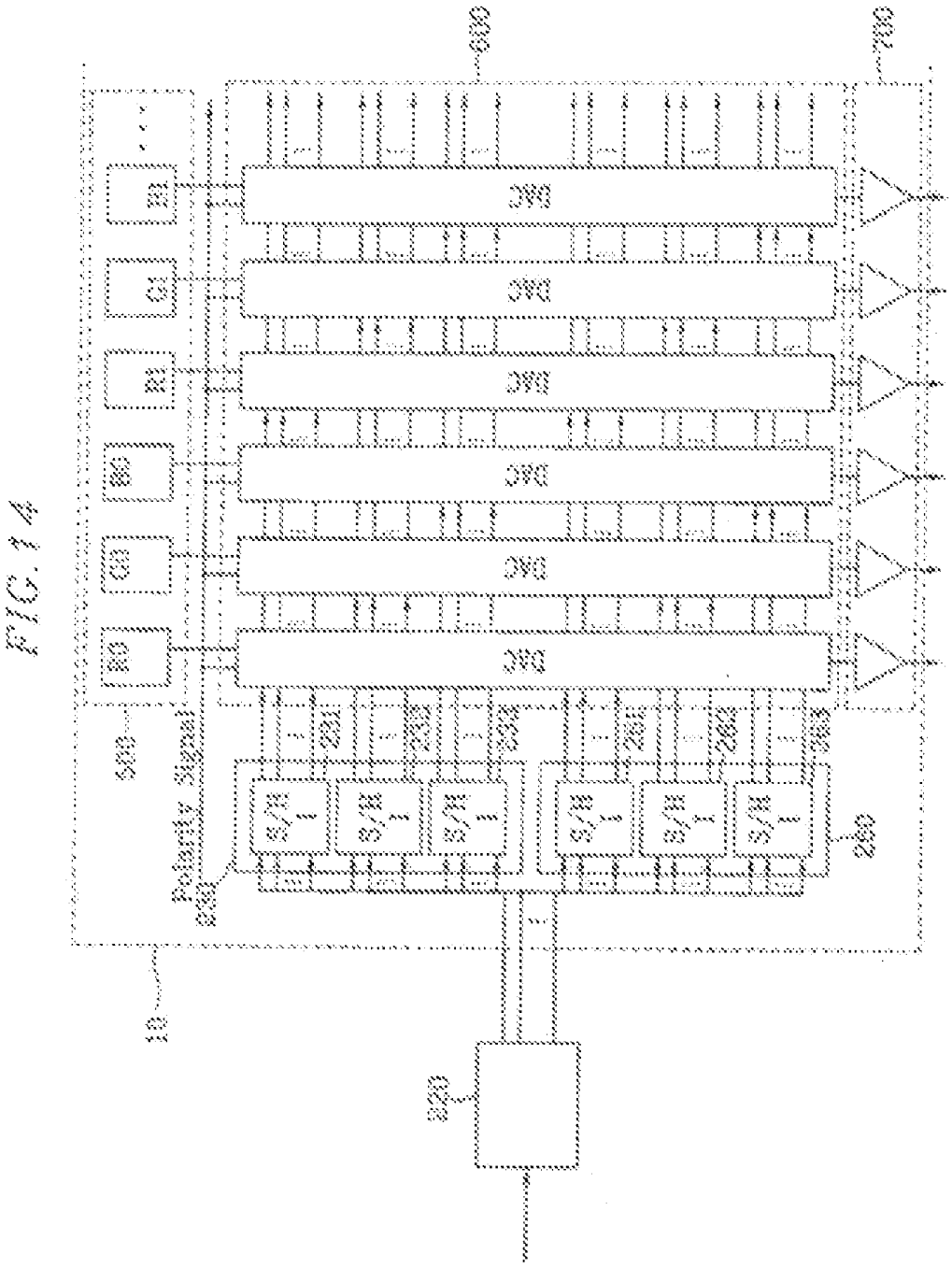


FIG. 14

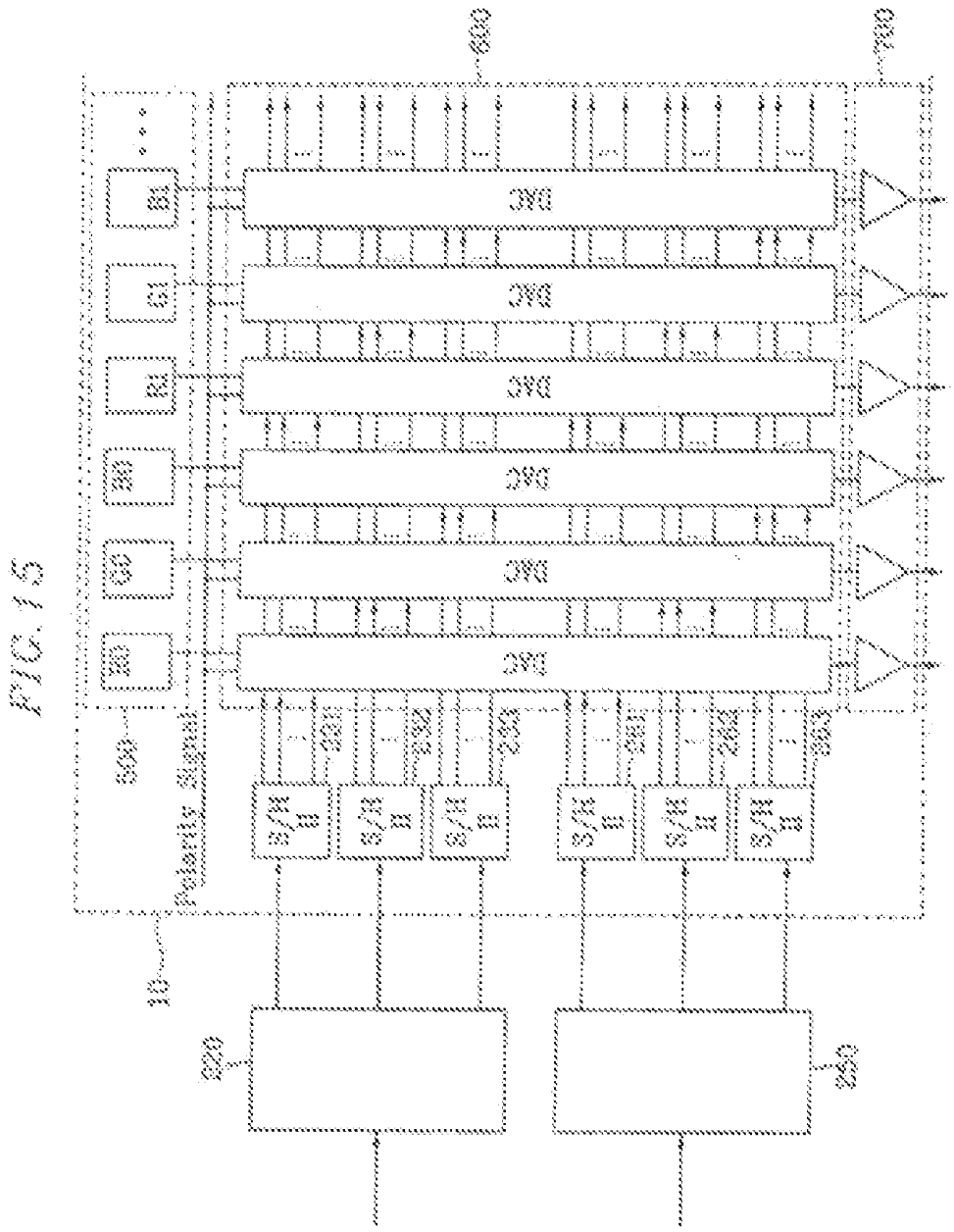


FIG. 15

FIG. 16

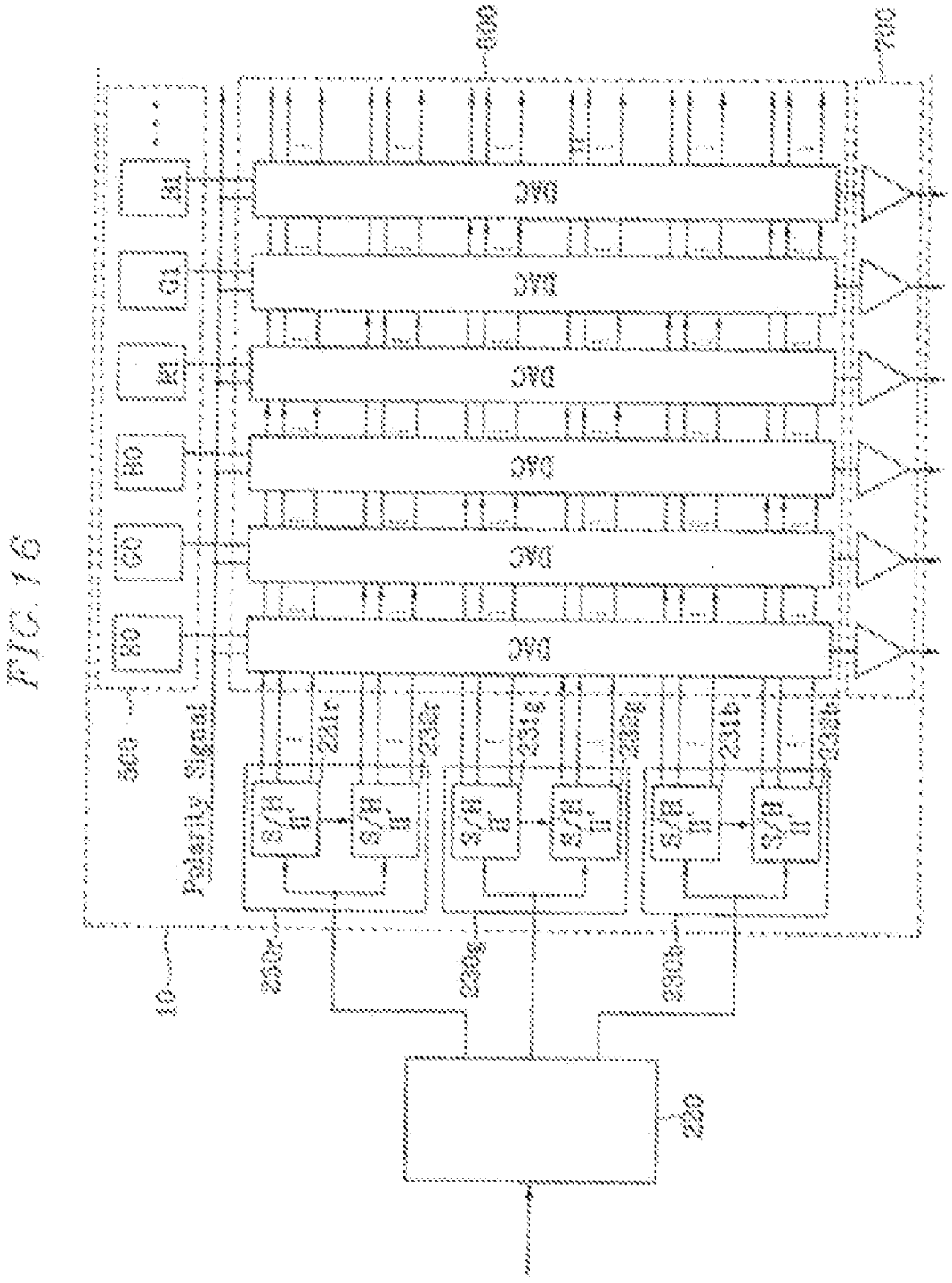


FIG. 17

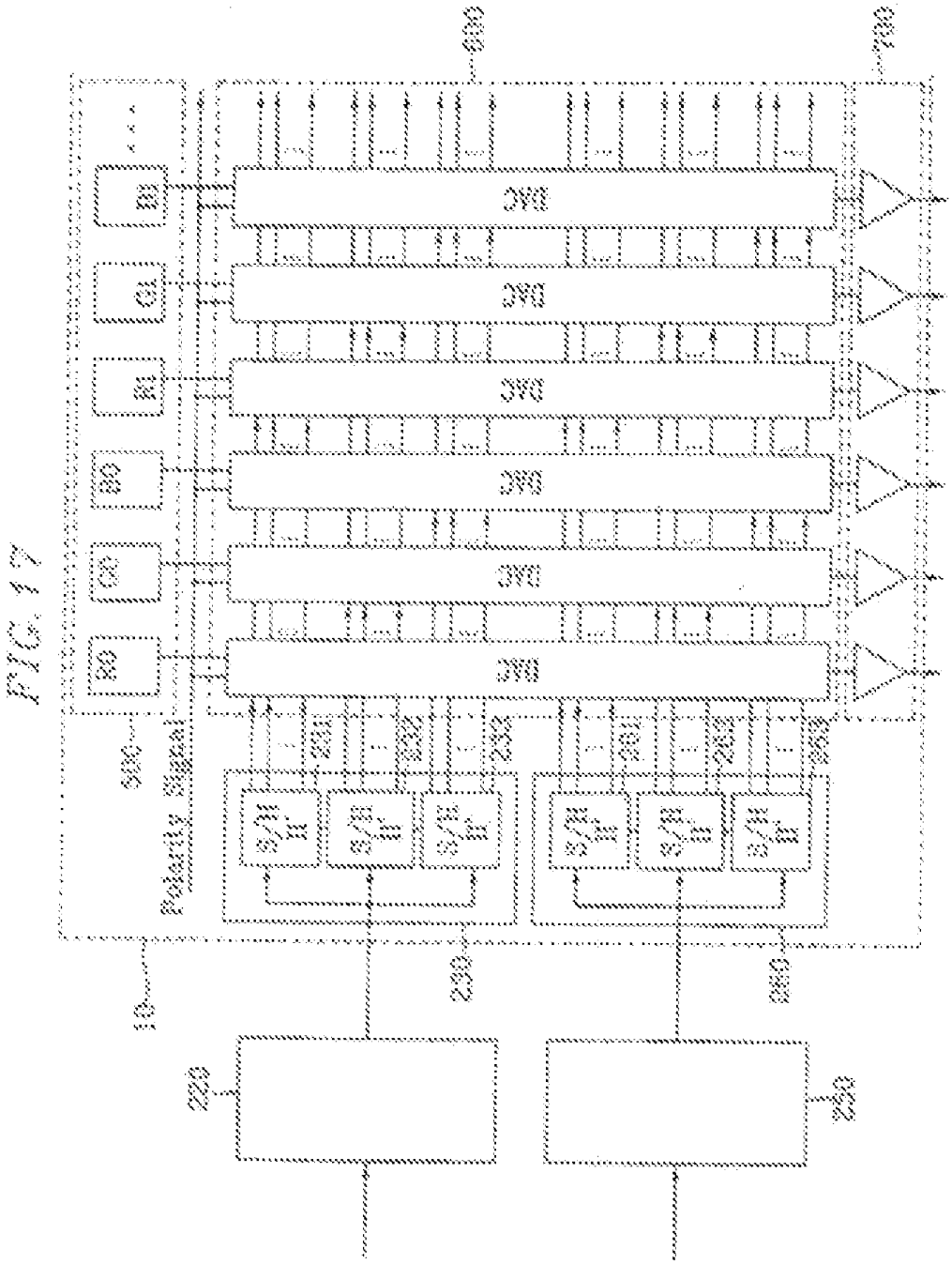
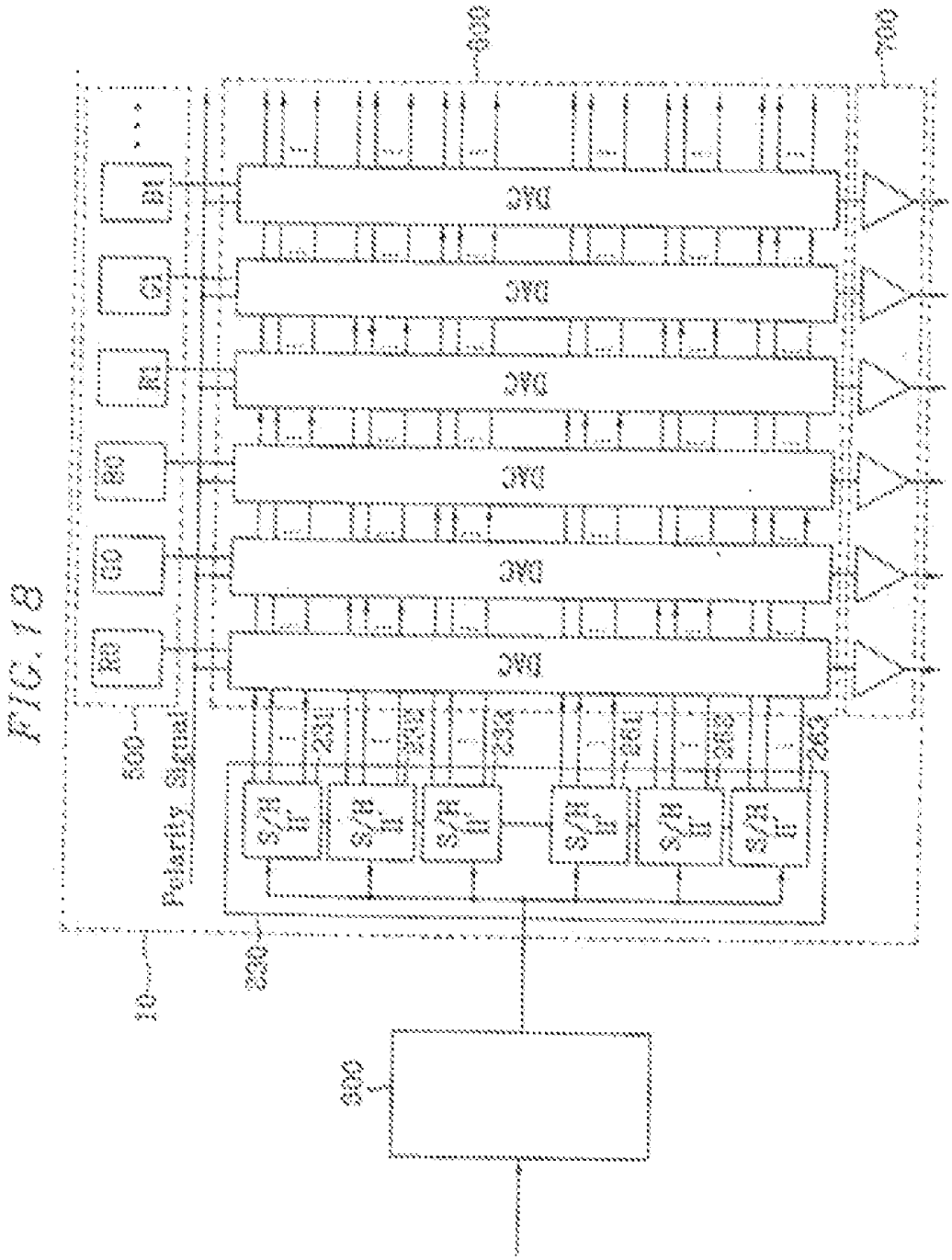

600
700
DAC
DAC
DAC
DAC
DAC
DAC
Polarity Signal
500
10
230
260
220
250

FIG. 18


DAC
DAC
DAC
DAC
DAC
DAC
Polarity Signal
S/H
S/H
S/H
S/H
S/H
S/H
10
220
500
700
900

LIQUID CRYSTAL DISPLAY AND DRIVING DEVICE THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 10/287,916 filed on Nov. 5, 2002, which claims priority to Korean Patent Application Nos. 2001-0068457 filed on Nov. 5, 2001, and 2002-0024781 filed on May 6, 2002, the disclosures of which are incorporated by reference herein in their entirety.

BACKGROUND OF THE INVENTION

[0002] (a) Field of the Invention

[0003] The present invention relates to a liquid crystal display and a driving device thereof.

[0004] (b) Description of the Related Art

[0005] A typical liquid crystal display ("LCD") includes an upper panel provided with a common electrode and an array of color filters and a lower panel provided with a plurality of thin film transistors ("TFTs) and a plurality of pixel electrodes. The two panels have respective alignment films coated thereon and a liquid crystal layer is interposed therebetween. The pixel electrodes and the common electrode are applied with electric voltages and the voltage difference therebetween causes electric field. The variation of the electric field changes the orientations of liquid crystal molecules in the liquid crystal layer and in turn the transmittance of light passing through the liquid crystal layer, thereby obtaining desired images.

[0006] A typical data driver of an LCD includes a shift register, a data register, a data latch, a digital-to-analogue ("D/A") converter and an output buffer. The data driver latches red ("R"), green ("G") and blue ("B") data sequentially inputted in synchronization with a dot clock from a timing controller and alters the timing system from a dot-sequential scheme into a line-sequential scheme in to output data voltages to data lines of a liquid crystal panel assembly. The D/A converter converts the RGB data from the data latch into the respective analog voltages on the basis of gamma reference voltages VGMA1 to VGMA18 provided from an external device.

[0007] A normal LCD uses identical signals for R, G and B pixels assuming that their optical characteristics are the same, which are different in practice. As a result, there is a problem that the impression of colors for respective grays is not balanced or excessively biased.

[0008] To solve this problem, it is suggested to provide different sets of gamma reference voltages for respective R, G and B colors. However, this increases the number of pins of the data driver by thirty-six relative to the previous one and thus the size of the data driver. In addition, the unit for generating the gamma reference voltages has the increased number of blocks, i.e., three blocks for respectively generating corresponding sets of the gamma reference voltages for R, G and B colors. There is a problem that the increase of external circuits as well as the increase of the mounting area for the data driver in a printed circuit board ("PCB") raises the production cost of the LCD.

SUMMARY OF THE INVENTION

[0009] An object of the present invention is to improve image quality of an LCD by generating separate sets of gamma reference voltages for respective R, G and B colors.

[0010] To accomplish the object, an LCD according to a first aspect of the present invention includes a timing controller outputting digital gamma data for each of R, G and B and a data driver. The data driver includes a digital gamma storage, a gamma reference voltage generator and a digital-to-analog converter. The digital gamma storage stores digital gamma data from the timing controller, and the gamma reference voltage generator generates gamma reference voltages, which are used in converting image data into analog voltages, for each of R, G and B independently, on the basis of the stored digital gamma data. The digital-to-analog converter converts the image data for each of R, G and B into analog voltages to output them, on the basis of the generated gamma reference voltages.

[0011] Herein, the gamma reference voltage generator preferably includes a plurality of DACs receiving and converting digital gamma data for each of R, G and B into analog data.

[0012] An LCD according to a second aspect of the present invention includes a timing controller, a gamma reference voltage generator and a data driver. The timing controller outputs digital gamma data for each of R, G and B, and the gamma reference voltage generator converts the digital gamma data from the timing controller into analog data to output them. The data driver includes a sample/hold unit outputting sampled gamma reference voltages after performing sample/hold treatment of the gamma reference voltages from the gamma reference voltage generator, and a digital-to-analog converter converting image data for each of R, G and B into analog voltages to output them on the basis of the sampled gamma reference voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other objects and advantages of the present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

[0014] FIG. **1** is a schematic diagram of a data driver according to an embodiment of the present invention;

[0015] FIG. **2** is a diagram illustrating a gamma reference voltage generator shown in FIG. **1**;

[0016] FIGS. **3** and **4** partially show exemplary data drivers according to first and second embodiments of the present invention, respectively;

[0017] FIG. **5** is a diagram of an exemplary sample/hold circuit of the gamma reference voltage generator according to the second embodiment of the present invention;

[0018] FIGS. **6** and **7** partially show exemplary data drivers according to third and fourth embodiments of the present invention, respectively;

[0019] FIG. **8** is a diagram of an exemplary sample/hold circuit of the gamma reference voltage generator according to the fourth embodiment of the present invention;

[0020] FIGS. **9** and **11** partially show exemplary data drivers according to fifth to seventh embodiments of the present invention;

[0021] FIG. **12** is a diagram illustrating an exemplary sample/hold a gamma reference voltage generator according to an embodiment of the present invention; and

[0022] FIGS. **13** to **18** partially illustrate exemplary data drivers according to eight to thirteenth embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0023] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like numerals refer to like elements throughout.

[0024] Now, LCDs and driving devices thereof according to embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0025] Referring to FIGS. **1** and **2**, a data driver and a gamma reference voltage generator according to an embodiment of the present invention will be described in detail.

[0026] FIG. **1** is a schematic diagram of an exemplary data driver according to an embodiment of the present invention, and FIG. **2** illustrates a configuration of an exemplary gamma reference voltage generator shown in FIG. **1**.

[0027] As shown in FIG. **1**, the data driver **10** according to an embodiment of the present invention includes a gamma register **100**, a gamma reference voltage generator **200**, a shift register **300**, a data register **400**, a data latch **500**, a D/A converter **600**, and an output buffer **700**. The shift register **300** shifts R, G and B data (D0[7:0]-D5[7:0]) from a timing controller (not shown) and stores the data in the data register **400**. The D/A converter **600** receives the data stored in the data register **400** from the data latch **500** and converts the data into analogue gray voltages. The output buffer **700** stores the analogue gray voltages from the D/A converter **600** and applies the analogue gray voltages to a plurality of data lines upon receipt of a load signal. The gamma register **100** stores digital gamma data for respective R, G and B colors, and the gamma reference voltage generator **200** generates a plurality of sets of gamma reference voltages of respective R, G and B colors on the basis of the values stored in the gamma register **100** to provide for the D/A converter **600**.

[0028] As shown in FIG. **2**, the gamma register **100** receives the digital gamma data through a plurality of data buses from a timing controller (not shown) and stores the digital gamma data in response to the gamma load signal GMA_load. The gamma reference voltage generator **200** is connected to two external voltage sources AVDD and GND and converts the digital gamma data for each color and for each polarity into analog values to provide as positive/negative reference voltages for the D/A converter **600**.

[0029] Gamma reference voltage generators according to embodiments of the present invention will be described in detail. In the embodiments of the present invention, the description will be made assuming that the number of the sets of the digital gamma data provided for the gamma reference voltage generator **200** is equal to 9×2×3, i.e., positive R, G and B digital gamma data D_{V1R}-D_{V9R}, $D_{V1G}D_{V9G}$, D_{V1B}-D_{V9B} and negative R, G and B digital gamma data D_{V10R}-D_{V18R}, $D_{V10G}D_{V18G}$, D_{V10B}-D_{V18B}. However, the present invention is not limited to this but properly applied for any number of the sets of the digital gamma data.

[0030] First, a gamma reference voltage generator according to a first embodiment of the present invention will be described with reference to FIG. **3**.

[0031] FIG. **3** is a diagram illustrating an exemplary gamma reference voltage generator according to the first embodiment of the present invention.

[0032] As shown in FIG. **3**, a gamma reference voltage generator **200** according to the first embodiment of the present invention includes a positive gamma reference voltage generator **210** and a negative gamma reference voltage generator **240** for positive and negative gamma voltages, respectively.

[0033] In this embodiment, the gamma reference voltage generator **200** receives digital gamma data for respective R, G and B colors from a gamma register **100** at the same time, and respective D/A converters ("DACs") **221-223** and **251-253** generate corresponding gamma reference voltages. In order for the gamma reference voltage generator **200** to generate all the R, G and B gamma reference voltages, the number of the DACs **221-223** and **251-253** provided in the gamma reference voltage generator **200** corresponds to the number of the R, G and B digital gamma data. For example, the gamma reference voltage generator **200** according to the first embodiment of the present invention preferably includes 9×2×3 DACs.

[0034] In detail, the positive gamma reference voltage generator **210** includes nine DACs **221-223** for each R, G and B color, each analogue-converting the corresponding positive R, G and B digital gamma data DV1R-DV9R, DV9G-DV9G and DV1B-DV9B to generate positive R, G and B gamma reference voltages V1R-V9R, V9G-V9G and V1B-V9B. Also, the negative gamma reference voltage generator **240** includes nine DACs **251-253** for each R, G and B color, each analogue-converting the corresponding positive R, G and B digital gamma data DV10R-DV18R, DV10G-DV18G and DV10B-DV18B into negative R, G and B gamma reference voltages V10R-V18R, V10G-V18G and V10B-V18B.

[0035] The D/A converter **600** converts the R, G and B image data R0, G0, B0, R1, G1, B1, . . . into analog voltages based on the positive and the negative gamma references voltages V1R-V9R, V1R-V9R, V1B-V9B, V10R-V18R, V10G-V18G and V10B-V18B provided from the DACs **221-223** and **252-253**.

[0036] Meanwhile, the number of the DACs in the gamma reference voltage generator **200** can be decreased relative to the first embodiment of the present invention, and, hereafter, such embodiments will be described with reference to FIGS. **4** to **12**.

[0037] First, a gamma reference voltage generator according to a second embodiment of the present invention will be described with reference to FIGS. **4** and **5**.

[0038] FIG. **4** is a diagram illustrating an exemplary gamma reference voltage generator according to the second embodiment of the present invention, and FIG. **5** is a circuit diagram showing an exemplary sample/hod circuit included in the gamma reference voltage generator according to the second embodiment of the present invention.

[0039] As shown in FIG. **4**, a gamma reference voltage generator **200** according to the second embodiment of the present invention also includes positive and negative gamma reference voltage generators **210** and **240** includes a DAC unit **220** and **250** and a sample/hold unit **230** and **260**.

[0040] The DAC unit **220** includes nine DACs analogue-converting the positive digital gamma data DV1R-DV9R, DV9G-DV9G and DV1B-DV9B inputted in time-divisional scheme for each R, G and B color to generate positive R, G and B gamma reference voltages V1R-V9R, V9G-V9G and V1B-V9B. The sample/hold unit **230** includes a plurality of sample/hold circuit units (S/HI) **231-233** for sampling the positive R, G and b gamma reference voltages V1R-V9R, V9G-V9G and V1B-V9B from the DAC unit **220**. likewise, the DAC unit **250** includes nine DACs analogue-converting negative digital gamma data DV10R-DV18R, DV10G-DV18G and DV10B-DV18B inputted in time-divisional scheme for each R, G and B color to generate negative R, G and B gamma reference voltages V10R-V18R, V10G-V18G and V10B-V18G. The sample/hold unit **260** includes a plurality of sample/hold circuit units (S/HI) **261-263** for sampling the negative gamma reference voltages V10R-V18R, V10G-V18G and V10B-DV18G from the DAC unit **250**.

[0041] In detail, the R sample/hold circuit **231** samples the positive R gamma reference voltages V1R-V9R to provide for the D/A converter **600**. The D/A converter **600** converts R image data R0, R1, . . . the data latch **500** into analog voltages on the basis of the sampled positive R gamma reference voltages V1R-V9R. In the same way, the G and B sample/hold circuit units **262** and **263** respectively sample the positive G and B gamma reference voltages V9G-V9G and V1B-V9B to supply for the D/A converter **600**. The DAC unit **250** and the sample/hold unit **260** in the negatice gamma reference voltage generator **240** analogue-convert the negative R, G and B digital gamma data to generate the negative R, G and B gamma reference voltages V10R-V18R, V10G-V18G and V10B-V18G and sample to provide for the D/A converter **600**.

[0042] one **231** of the sample/hold circuit units **231-233** and **261-263** of the sample/hold units **230** and **260** will be described in detail with reference to FIG. **5**.

[0043] The sample/hold unit **231** includes nine sample/hold circuits for respectively sampling the positive R gamma reference voltages from the nine DACs of the DAC unit **220**. Each sample/hold circuit includes a switch SW, a capacitor C**1** and a buffer buf. When the switch WW is turned on in response to a sampling start signal, the gamma reference voltage from the DAC is stored in the capacitor C**1** and sampled, and the sampled gamma reference voltage is provided for the D/A converter **600** through the analog buffer.

[0044] The number of the DACs provided in the gamma reference voltage generator **200** according to the second embodiment of the present invention is equal to 9+9=18, and is reduced to one thirds of that according to the first embodiment of the present invention as described above.

[0045] Although the second embodiment of the present invention employs separate DAC units for positive and negative polarities, the DAC capable of supporting both the positive and negative polarities may be used. Hereinafter, such an embodiment will be described with reference to FIG. **6**.

[0046] FIG. **6** is a diagram of an exemplary gamma reference voltage generator according to a third embodiment of the present invention.

[0047] As shown in FIG. **6**, a gamma reference voltage generator **200** according to the third embodiment of the present invention is almost the same as that of the second embodiment except using a single DAC unit **220** for the positive and negative digital gamma data.

[0048] In detail, the DAC unit **220** includes nine DACs, and analogue-converts positive R, G and B digital gamma data DV1R-DV9R, DV9G-DV9G and DV1B-DV9B and negative R, G and B digital gamma data DV10R-DV18R, DV10G-DV18G and DV10B-DV18B sequentially inputted in time-divisional scheme for respective R, G and B colors and polarities to generate the positive and the negative R, G and B gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G and V10B-V18B. In addition, the DAC unit **220** provides the positive and the negative R, G and B gamma reference voltages for two sample/hold units **230** and **260**, respectively. The sample/hold units **230** and **260** are substantially the same as those described in the second embodiment of the present invention.

[0049] The number of the DACs provided in the gamma reference voltage generator **200** according to the third embodiment of the present invention is nine, which is decreased to one sixths of that according to the first embodiment of the present invention.

[0050] According to the second and the third embodiments of the present invention, since the timing controller (not shown) sequentially inputs the R, G and B digital gamma data in time-divisional scheme for respective R, G and B colors, the DACs provided in the DAC unit has a relation with the digital gamma data in one to one correspondence. However, eighteen digital gamma data for each R, G and B color can be inputted sequentially. Such an embodiment will now be described in detail with reference to drawings.

[0051] First, a gamma reference voltage generator according to a fourth embodiment of the present invention will be described with reference to FIGS. **7** and **8**.

[0052] FIG. **7** is a diagram of an exemplary gamma reference voltage generator according to the fourth embodiment of the present invention, and FIG. **8** illustrates an exemplary sample/hold circuit unit provided in the gamma reference voltage generator according to the fourth embodiment of the present invention.

[0053] As shown in FIG. **7**, a gamma reference voltage generator **200** also includes positive and negative gamma reference voltage generators **210** and **240** like the first embodiment. The positive gamma reference voltage generator **210** includes three DACs **221-223** corresponding to respective positive R, G and B digital gamma data DV1R-

DV9R, DV9G-DV9G and DV1B-DV9B and three sample/hold units **231-233** connected to the respective DACs **221-233**. In the same way, the negative gamma reference voltage generator **240** includes three DACs **251-253** corresponding to respective R, G and B digital gamma data DV10R-DV18R, DV10G-DV18G and DV10B-DV18B and three sample/hold unit **261-263**.

[**0054**] As shown in FIG. **7**, the positive and the negative R, G and B digital gamma data DV1R--DV9R, DV9G-DV9G, DV1B-DV9B DV10R-DV18R, DV10G-DV18G and DV10B-DV18B from the timing controller are serially input for respective R, G and B colors and respective polarities to the DACs **221-223** and **252-253**. The DACs **221-223** and **251-253** analogue-convert these digital gamma data and serially output the analog-converted positive and negative gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G and V10B-V18B to the respective sample/hold circuit units **231-233** and **261-263**. The sample/hold circuit units **231-233** and **261-263** respectively sample the positive and the negative gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G and V10B-V18B to provide for the D/A converter **600**.

[**0055**] Although each sample/hold circuit unit **231-233** and **261-263** according to the second and the third embodiments of the present invention described in FIG. **5** simultaneously sample and output the nine gamma reference voltages, the sample/hold circuit units **231-233** and **261-263** according to the fourth embodiment of the present invention sequentially sample and output the serially entered gamma reference voltages. For example, as shown in FIG. **8**, one sample/hold circuit unit **231** includes nine sample/hold circuits connected to the output of the DAC **221**. The sample/hold circuit includes a switch SW for switching the gamma reference voltage from the DAC **221**, a capacitor C**1** storing the gamma reference voltage inputted through the switch SW, an analog buffer buf outputting the gamma reference voltage stored in the capacitor C**1** to the D/A converter **600**, and a shift register S/R transmitting a sampling start signal for controlling turning on and off of the switch to a next sample/hold circuit.

[**0056**] The sample/hold circuit unit **231** sequentially outputs the gamma reference voltages from the DAC **221** in response to the shift of the sampling start signal through the shift register S/R.

[**0057**] Since the gamma reference voltage generator **200** employs according to the fourth embodiment of the present invention six DACs respectively for the positive and the negative R, G and B colors, the number of the DACs is decreased to one thirds of that according to the second embodiment.

[**0058**] Although a single DAC has been assigned to each R, G and B color with each polarity in the fourth embodiment of the present invention, the DAC may be irrelevant to the polarity. Such an embodiment will be described with reference to FIG. **9**.

[**0059**] FIG. **9** is a diagram illustrating an exemplary gamma reference voltage generator according to a fifth embodiment of the present invention.

[**0060**] As shown in FIG. **9**, a gamma reference voltage generator **200** according to the fifth embodiment of the present invention includes R, G and B gamma reference voltage generators **210***r*, **210***g* and **210***b* for generating respective R, G and B gamma reference voltages. Each of the R, G and B gamma reference voltage generators **210***r*, **210***g* and **210***b* includes a DAC **220***r*, **220***g* and **220***b* and sample/hold unit **230***r*, **230***g* and **230***b*, and each sample/hold unit **230***r*, **230***g* and **230***b* includes two sample/hold circuit units (S/H II') **231***r* and **232***r*, **231***g* and **231***b*. The DACs **220***r*, **220***g* and **220***b* analogue-convert the R, G and B digital gamma data DV1R-DV18R, DV9G-DV18G and DV1B-DV18B serially received from a timing controller, and outputs the analog-converted R, G and B gamma reference voltages V1R-V18R, V9G-V18G and V1B-V18B to the sample/hold units **230***r*, **230***g* and **230***b*, respectively. In the sample/hold units **230***r*, **230***g* and **230***b*, the sample/hold circuit units **231***r* and **232***r*, **231***g* and **232***g* and **231***b* and **232***b* are the same as those described in FIG. **8** excepting that the outputs of the last shift registers S/R of the sample/hold circuit unit **231***r*, **231***g* and **231***b* is used as the sampling start signal of the sample/hold circuit units **232***r*, **232***g* and **232***b*.

[**0061**] In detail, the sample/hold circuit unit **231***r* sequentially samples the positive R gamma reference voltages V1R-V9R of the R gamma reference voltages V1R-V18R outputted serially from the DAC **220***r* according to the sampling start signal, to output them to the D/A converter **600**, and the sample/hold circuit unit **232***r* sequentially samples the negative R gamma reference voltages V10R-V18R according to the output of the last shift register S/R of the sample/hold circuit unit **231***r* sequentially D/A converter **600**. In the same way, the sample/hold circuit units **231***g* and **231***b* sequentially sample the positive G and B gamma reference voltages V9G-V9G and V1B-V9B, respectively, according to the sampling start signal, and the sample/hold circuit units **232***g* and **232***b* sequentially sample the negative G and B gamma reference voltages V10G-V18G and V10B-V18B, respectively, according to the outputs of the last shift registers S/R of the sample/hold circuit units **231***g* and **231***b*.

[**0062**] According to the fifth embodiment of the present invention the number of the DACs is decreased to a half of the fourth embodiment. Although the fifth embodiment has the DACs for each of R, G and B, the DACs may be used for each polarity. Such an embodiment will be described with reference to FIG. **10** in the following.

[**0063**] FIG. **10** illustrates an exemplary gamma reference voltage generator according to a sixth embodiment of the present invention.

[**0064**] As shown in FIG. **10**, a gamma reference voltage generator according to the sixth embodiment of the present invention includes positive and negative gamma reference voltage generators **210** and **240** like the first embodiment of the present invention. The positive gamma reference voltage generator **210** includes one DAC **220** and sample/hold unit **230** including three sample/hold circuit units **231-233**. The negative gamma reference voltage generator **240** includes one DAC **250** and sample/hold unit **260** including three sample/hold circuit units **262-263**.

[**0065**] The DAC **220** serially receives the positive R, G and B digital gamma data DV1R-DV9R, DV9G-DV9G, DV1B-DV9B to convert them into the gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, to output them to the sample/hold unit **230**. In the same way, the DAC **250**

serially receives the negative R, G and B digital gamma data DV10R-DV18R, DV10G-DV18G, DV10B-DV18B to convert them into the gamma reference voltages V10R-V18R, V10G-V18G, V10B-V18B to output them to the sample/hold unit **260**.

[**0066**] The sample/hold circuit units **231-233** of the sample/hold unit **230** sample the positive R, G and B gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, respectively, which are the same as the sample/hold circuit units described FIG. **8**, excepting that the outputs of the last shift registers S/R of the sample/hold circuit units **231** and **232** become the sampling start signal of the sample/hold circuit units **232** and **233**, respectively, as described in the fifth embodiment. In the same way, the sample/hold circuit units **261-263** of the sample/hold unit **260** sample the negative R, G and B gamma reference voltages V10R-V18R, V10G-V18G, V10B-V18B, respectively. By the gamma reference voltage generator according to the sixth embodiment of the present invention, just two DACs are used.

[**0067**] Meanwhile, the order to generate gamma reference voltages for each of R, G and B regardless of the polarities of the gamma reference voltages, only one DAC may be used. Such an embodiment will be described with reference to FIG. **11**.

[**0068**] FIG. **11** is a diagram illustrating an exemplary gamma reference voltage generator according to a seventh embodiment of the present invention.

[**0069**] As shown in FIG. **11**, a gamma reference voltage generator **200** according to the seventh embodiment of the present invention includes one DAC **220** and sample/hold unit **230**, and the sample/hold unit **230** includes six sample/hold circuit units **231-233** and **262-263**. The DAC **220** is serially provided with positive and negative R, G and B digital gamma data DV1R-DV9R, DV9G-DV9G, DV1B-DV9B DV10R-DV18R, DV10G-DV18G and DV10B-DV18B to convert them into positive and negative R, G and B gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G and V10B-V18B to output them to the sample/hold unit **230**. The sample/hold circuit units **321-233** of the sample/hold unit **230** sample the positive R, G and B gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, equally as described in the sixth embodiment, and the output of the last shift register of the sample/hold circuit unit **233** become the sampling start signal of the sample/hold circuit unit **261**. Then, the sample/hold circuit units **261-263** sample the negative R, G and B gamma reference voltages V10R-V18R, V10G-V18G, V10B-V18B according to such sampling start signal.

[**0070**] According to the seventh embodiment of the present invention as above, only one DAC can be used in order to generate the gamma reference voltages.

[**0071**] Meanwhile, a time to take to generate the gamma reference voltages of the second and the third embodiments is three times and six times as long as that of the first embodiment, respectively, and a time of take to generate the gamma reference voltages of the fourth and the fifth embodiments is nine times and eighteen times as long as that of the first embodiment. A time to take to generate the gamma reference voltages is fifty four times as long as that of the first embodiment.

[**0072**] Assuming that it takes one DAC **1**μs to generate gamma reference voltages, it takes the DAC of FIG. **51**μs, while it takes the DAC of FIG. **1354**μs. Since such time is shorter than a blank interval with no data between frames, there is no problem in displaying a screen.

[**0073**] However, in case such time causes a problem, it is possible to decrease a time using a sample/hold circuit unit S/H III.

[**0074**] FIG. **12** illustrates an exemplary sample/hold circuit S/H III according to another embodiment of the present invention.

[**0075**] As shown in FIG. **12**, a sample/hold circuit unit S/H according to another embodiment of the present invention is composed of nine sample/hold circuits connected to output terminal of the DAC, and the sample/hold circuit includes a switch SW, a shift register S/R, capacitors C**1** and C**2**, an analog buffer buf, input and output switches S**1** and S**2**. The switch SW operates to transmit the gamma reference voltage from the DAC according to the sampling start signal, and the shift register S/R transmits the sampling start signal to next sample/hold circuit. The capacitors C**1** and C**2** are connected to first and second paths to charge the gamma reference voltage transmitted along the first and the second paths, and the analog buffer buf outputs the gamma reference voltage charged in the capacitors C**1** and C**2** to the D/A converter **600**. In this case, the input switch S**1** connected between the switch SW and the first and the second paths to alternate between the first and the second paths according to a selection signal, and the output switch S**2** is connected between the first and the second paths and the analog buffer to alternate between the first and the second paths and the analog buffer to alternate between the first and the second paths according to the selection signal.

[**0076**] In this sample/hold circuit unit S/H III, the gamma reference voltage inputted from one terminal is sequentially outputted according to transmittance of the sampling start signal through the shift register S/R.

[**0077**] An operation of the sample/hold circuit unit S/H III will be described.

[**0078**] When the present gamma voltage is stored in the capacitor C**2**, a changed gamma reference voltage is stored in the capacitor C**1** to store all the changed gamma reference voltage in a capacitance corresponding to the capacitor C**1**, and thereafter, the gamma reference voltage of the capacitor C**1** is outputted by altering the selection signal. Then, the gamma reference voltage is changed in so short a time. When this state is maintained and the gamma reference voltage is changed, new gamma reference voltage is stored in the capacitor C**2**, and after the storage of the new gamma reference voltage is completed, the gamma reference voltage charged in the capacitor C**2** is only outputted.

[**0079**] This sample/hold circuit S/H III can be used instead of the sample/hold circuits S/H II and S/H II' in the embodiment described above and embodiments described below.

[**0080**] In the above, many embodiments for generating the gamma reference voltages at the internal side of the data driver **10** and decreasing an area occupied with the DACs for generating the gamma reference voltages have been described.

[0081] Meanwhile, the DACs for generating the gamma reference voltages may be implemented remote from the data driver **10**, and such embodiments will be described in simplicity with reference to FIG. **13** to FIG. **18**.

[0082] GIG. **13** is a diagram of an exemplary gamma reference voltage generator according to an eighth embodiment of the present invention.

[0083] Referring to FIG. **13**, the eighth embodiment of the present invention is the same as the second embodiment excepting that positive and negative gamma reference voltage generators **220** and **250** for respectively receiving positive and negative digital gamma data DV1R-DV9R, DV9G-DV9G, DV1B-DV9B DV10R-DV18R, DV10G-DV18G, DV10B-DV18B to generate positive and negative gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G, V10B-V18B are provided at an external side of the data driver **10**.

[0084] The positive and the negative gamma reference voltage generators **220** and **250** are composed of digital-to analog converters of multiple channel system, respectively, and they output the positive and the negative R, G and B gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18B time-divided for each of R, G and B. Sample/hold units **230** and **260**, which respectively receive the positive and the negative R, G and B gamma reference voltages from the positive and the negative gamma reference voltage generators **220** and **250** to sample them, are provided within the data driver **10**. The sample/hold units **230** and **260** are the same as that in the first embodiment.

[0085] Although the eight embodiment of the present invention has the two digital-to-analog converters of multiple channel system that is divided for each polarity, it may have one digital-to analog converter regardless of polarity as shown in FIG. **14**.

[0086] FIG. **14** illustrates an exemplary gamma reference voltage generator according to a ninth embodiment of the present invention.

[0087] As shown in FIG. **14**, the ninth embodiment is the same as the third embodiment excepting that a gamma reference voltage generator **220** for receiving digital gamma data DV1R-DV9R, DV9G-DV9G, DV1B-DV9B DV10R-DV18R, DV10G-DV18G, DV10B-DV18B from a timing controller to generate gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G, V10B-V18B is provided at an external side of a data driver **10**.

[0088] The gamma reference voltage generator **220** is composed of digital-to analog converters and outputs positive and negative R, G and B gamma reference voltages V1R-V9R, V9G-V9G, V1B-V9B, V10R-V18R, V10G-V18G, V10B-V18B time-divided for each of R, G and B to sample/hold circuit units **231-233** and **261-263**. The sample/hold circuit units **231-233** and **261-263** for respectively receiving the positive and the negative R, G and B gamma reference voltages to sample them are provided within the data driver **10**. The sample/hold circuit units **231-233** and **261-263** are the same as that of the second embodiment.

[0089] As shown in FIG. **15**, a tenth embodiment of the present invention is the same as the fourth embodiment except positive and negative gamma reference voltage generators **220** and **250** respectively receiving positive and negative gamma reference voltages through a timing controller and a digital interface to generate positive and negative gamma reference voltages.

[0090] The positive and the negative gamma reference voltage generators **220** and **250** serializes the positive and the negative R, G and B gamma reference voltages for each of R, G and B to provide them to the sample/hold units **230** and **260** in the data driver **10**. The sample/hold units **230** and **260** are the same as that of the fourth embodiment.

[0091] As shown in FIG. **16**, an eleventh embodiment of the present invention is the same as the fifth embodiment except a gamma reference voltage generator **220** receiving digital gamma data through a timing controller and a digital interface to generate gamma reference voltages. The gamma reference voltage generator **220** serializes the gamma reference voltages for each of R, G and B to provide them to the sample/hold units **230***r*, **230***g* and **230***b* in the data driver **10**. These sample/hold units **230***r*, **230***g* and **230***b* are the same as the sample/hold units **230***r*, **230***g* and **230***b* of the fifth embodiment.

[0092] As shown in FIG. **17**, a twelfth embodiment of the present invention is the same as the sixth embodiment except positive and negative gamma reference voltage generators **220** and **250** respectively receiving positive and negative gamma reference voltages through a timing controller and a digital interface to generate positive and negative gamma reference voltages. The positive and the negative gamma reference voltage generators **220** and **250** serializes the positive and the negative R, G and B gamma reference voltages for each of R, G and B to provide them to the sample/hold units **230** and **260** in the data driver **10**. The sample/hold units **230** and **260** respectively include three sample/hold circuit units **231-233** and **261-263** like that of the sixth embodiment.

[0093] As shown in FIG. **18**, a thirteenth embodiment of the present invention is the same as the seventh embodiment except a gamma reference voltage generator **220** receiving digital gamma data through a timing controller and a digital interface to generate gamma reference voltages. The gamma reference voltage generator **220** serializes the gamma reference voltages for each of R, G and B to provide them to the sample/hold unit **230** in the data driver **10**. These sample/hold unit **230** includes six sample/hold units **231-233** and **261-263** like the seventh embodiment.

[0094] As described above, since the data driver can have the gamma reference voltage for each of R, G and B using the gamma reference voltage for each of R, G and B, it is possible to adjust temperature and coordinate of colors as desired.

[0095] In addition, it is possible to more variably implement a color tone that has been limited by the characteristics of the liquid crystal or the color filter.

[0096] Furthermore, it is possible to obtain a dynamic screen even in the moving pictures since new gamma is applicable to each of frames due to receiving digital gamma data from the timing controller. Of course, when the driving IC as above is applied, the timing controller is preferably also altered. That is, when the timing controller is supplied with power, it preferably transmits the gamma value for each of R, G and B to the data driver as digital type, and it

preferably transmits the gamma values so that the gamma values can be adjusted by analyzing inputted data of screen when a dynamic screen desires to be watched.

What is claimed is:

1. A liquid crystal display comprising:

a timing controller outputting digital gamma data for respective R, G and B colors; and

a data driver comprising a digital gamma storage storing the digital gamma data from the timing controller, a gamma reference voltage generator generating gamma reference voltages for respective R, G and B colors, which are used in converting image signals into analog voltages on the basis of the stored digital gamma data, and a digital-to-analog converter converting image data for each of R, G and B into analog voltages to output them on the basis of the generated gamma reference voltages.

2. The liquid crystal display of claim 1, wherein the gamma reference voltage generator comprises a plurality of DACs receiving the digital gamma data for each of R, G and B to convert them into analog data.

3. The liquid crystal display of claim 1, wherein the gamma reference voltage comprises:

a first polarity gamma reference voltage generator converting first polarity digital gamma data sequentially inputted for each of R, G and B into analog data to generate gamma reference voltages for each of R, G and B with first polarities; and

a second polarity gamma reference voltage generator converting polarity digital gamma data sequentially inputted for each of R, G and B into analog data to generate gamma reference voltages for each of R, G and B with second polarities.

4. The liquid crystal display of claim 3, wherein the first polarity gamma reference voltage generator comprises a plurality of DACs converting the first polarity digital gamma data sequentially inputted for each of R, G and B into analog data to generate gamma reference voltages; and

a first polarity sample/hold unit performing sample/hold treatment of each of the analog-converted R, G and B gamma reference voltages to generate sampled R, G and B gamma reference voltages,

wherein the second polarity gamma reference voltage generator comprises:

a plurality of DACs converting the second polarity digital gamma data sequentially inputted for each of R, G and B into analog data to generate gamma reference voltages; and

a second polarity sample/hold unit performing sample/hold treatment of each of the analog-converted R, G and B gamma reference voltages to generate sampled R, G and B gamma reference voltages.

5. The liquid crystal display of claim 1, wherein the gamma reference voltage generator comprises a plurality of DACs converting a first and a second polarity digital gamma data sequentially inputted for each of R, G and B into analog data to generate gamma reference voltages;

a first polarity sample/hold unit performing sample/hold treatment of each of the analog-converted R, G and B gamma reference voltages to generate sampled R, G and B gamma reference voltages; and

a second polarity sample/hold unit performing sample/hold treatment of each of the analog-converted R, G and B gamma reference voltages to generate sampled R, G and B gamma reference voltages.

6. The liquid crystal display of claim 4, wherein each of the first and the second polarity sample/hold unit comprises three sample/hold circuit unit provided for each of R, G and B, and the sample/hold circuit unit is composed of a plurality of sample/hold circuits connected to the output terminals of the plurality of DACs, wherein the sample/hold circuits comprises switches controlling ON/OFF of outputs of gamma reference voltages in response to predetermined sampling start signals, capacitors storing the gamma reference voltages inputted through the switches, and buffers outputting sampled gamma reference voltages stored in the capacitors.

7. The liquid crystal display of claim 1, wherein the gamma reference voltage generator comprises:

a plurality of DACs sequentially outputting each of gamma reference voltages, which are generated by receiving and converting serialized digital gamma data with a first and a second polarities into analog data, through one output line, and provided for each of R, G and B and have a multi-to-one method;

and a plurality of sample/hold circuit unit corresponding to the plurality of DACs, respectively, and outputting sampled gamma reference voltages for each of R, G and B after performing sample/hold treatment of the gamma reference voltages sequentially outputted from the DACs and having a one-to-multi method.

8. The liquid crystal display of claim 1, wherein the gamma reference voltage generator comprises:

an R gamma reference voltage generator outputting sampled R gamma reference voltage after performing sample/hold treatment of gamma reference voltage generated by sequentially receiving and converting serialized R gamma data with a first polarity and serialized R gamma data with a second polarity into analog data;

a G gamma reference voltage generator outputting sampled G gamma reference voltage after performing sample/hold treatment of gamma reference voltage generated by sequentially receiving and converting serialized G gamma data with a first polarity and serialized G gamma data with a second polarity into analog data; and

a B gamma reference voltage generator outputting sampled B gamma reference voltage after performing sample/hold treatment of gamma reference voltage generated by sequentially receiving and converting serialized B gamma data with a first polarity and serialized R gamma data with a second polarity into analog data.

9. The liquid crystal display of claim 8, each of the R, G and B gamma reference voltage generator comprises:

a DAC sequentially receiving and converting serialized digital gamma data with a first and second polarities

corresponding to each of R, G and B into analog data and then outputting them, and having a multi-to-one method;

a first polarity sample/hold circuit unit sequentially performing sample/hold treatment of the first polarity gamma reference voltage outputted from the DAC and outputting them; and

a second polarity sample/hold circuit unit, after completion of the sample/hold treatment in the first polarity sample/hold circuit unit and receiving sampling start signal from the first polarity sample/hold circuit unit, sequentially performing sample/hold treatment of the second polarity gamma reference voltage outputted from the DAC.

10. The liquid crystal display of claim 1, wherein the gamma reference voltage generator comprises:

a DAC having a multi-to-one method and outputting gamma reference voltage, which are generated by sequentially receiving and converting serialized digital gamma data into analog data, through one line;

a first sample/hold unit sequentially performing sample/hold treatment of analog gamma reference voltage with first polarity of analog gamma reference voltages outputted from the DAC and then outputting them for each of R, G and B; and

a second sample/hold unit, after completion of the sample/hold treatment in the first polarity sample/hold circuit unit and receiving sampling start signal from the first polarity sample/hold circuit unit, sequentially performing sample/hold treatment of analog gamma reference voltage with the second polarity of analog gamma reference voltages outputted from the DAC.

11. The liquid crystal display of claim 10, wherein each of the first and the second polarity sample/hold units comprises three sample/hold units corresponding to each of R, G and B, and any one sample/hold unit starts sample/hold treatment by sampling start signal, and, after completion of the sample/hold treatment, the sampling start signal is sent to another sample/hold circuit unit.

12. The liquid crystal display of claim 7, wherein the sample/hold circuit unit comprises a plurality of sample/hold circuits in parallel connected to output terminal of the DAC,

wherein the sample/hold circuit comprises:

a shift register transmitting sampling start signal to an adjacent sample/hold circuit;

a switch controlling ON/Off of output of gamma reference voltage in response to the sampling start signal;

a capacitor storing gamma reference voltage inputted through the switch; and

a buffer outputting the sampled gamma reference voltage in the capacitor.

13. The liquid crystal display of claim 7, wherein the sample/hold circuit unit comprises a plurality of sample/hold circuits in parallel connected to output terminal of the DAC,

wherein the sample/hold circuit comprises:

a shift register transmitting sampling start signal to an adjacent sample/hold circuit;

a switch controlling ON/OFF of output of gamma reference voltage in response to the sampling start signal;

first and second capacitors storing the gamma reference voltages;

an input switch connected to the switch and transmitting the gamma reference voltages having passed the switch to the first and the second capacitors;

a buffer outputting the gamma reference voltages stored in the first and the second capacitors; and

an output switch connected to the first and the second capacitors and transmitting the gamma reference voltages stored in the first and the second capacitors to the buffer.

14. A liquid crystal display comprising:

a timing controller outputting digital gamma data for each of R, G and B;

a gamma reference voltage generator converting the digital gamma data from the timing controller into analog data generate gamma reference voltages; and

a data driver comprising a sample/hold unit outputting sampled gamma reference voltages for respective R, G and B colors after performing sample/hold treatment of the gamma reference voltage from the gamma reference voltage generator and a digital-to-analog converter converting image data for each of R, G and B into analog voltages on the basis of the sampled gamma reference voltages to output them.

15. The liquid crystal display of claim 14, wherein the gamma reference voltage generator comprises a first and a second polarity gamma reference voltage generator sequentially outputting a first and a second polarity gamma reference voltages for each of R, G and B through a plurality of output terminals,

wherein the sample/hold unit comprises a first polarity sample/hold unit performing sample/hold treatment of the first gamma reference voltage to output sampled gamma reference voltage with a first polarity to the digital-to analog converter, and a second polarity sample/hold unit performing sample/hold treatment of the second gamma reference voltage to output sampled gamma reference voltage with a second polarity to the digital-to-analog converter.

16. The liquid crystal display of claim 14, wherein the gamma reference voltage generator sequentially outputting a first and a second gamma reference voltages through a plurality of output terminals,

wherein the sample/hold unit comprises a first polarity sample/hold unit performing sample/hold treatment of a first polarity gamma reference voltage from the gamma reference voltage generator to output sampled gamma reference voltage with a first polarity for R, G and B to the digital-to analog converter, and a second polarity sample/hold unit performing sample/hold treatment of a second polarity gamma reference voltage from the gamma reference voltage generator to output sampled gamma reference voltage with a second polarity for R, G and B to the digital-to-analog converter.

17. The liquid crystal display of claim 15, wherein each of the first and the second sample/hold unit comprises three sample/hold circuits provided for each R, G and B, and the

sample/hold circuit unit comprises a plurality of sample/hold circuits connected respectively to a plurality of output terminals of the gamma reference voltage generator,

wherein the sample/hold circuit comprises:

a switch controlling ON/OFF of output of gamma reference voltage in response to a predetermined sampling start signal;

a capacitor storing the gamma reference voltage inputted through the switch; and

a buffer outputting sampled gamma reference voltage stored in the capacitor.

18. The liquid crystal display of claim 14, wherein the gamma reference voltage comprises a first polarity gamma reference voltage generator serializing a first polarity gamma reference voltage for each of R, G and B to output each of R, G and B through each of output terminals and a second polarity gamma reference voltage generator serializing a second polarity gamma reference voltage for each of R, G and B to output each of R, G and B through each of output terminals,

wherein the sample/hold unit comprises a first polarity sample/hold unit performing sample/hold treatment for each of the serialized R, G and B gamma reference voltage with a first polarity to output sampled gamma reference voltage for each of R, G and B with a first polarity to the digital-to-analog converter and a second polarity sample/hold unit performing sample/hold treatment for each of the serialized R, G and B gamma reference voltage with a second polarity to output sampled gamma reference voltage for each of R, G and B with a second polarity to the digital-to-analog converter,

wherein each of the first and a second polarity sample/hold unit comprises three sample/hold circuit units performing sample/hold treatment for each of R, G and B gamma reference voltage.

19. The liquid crystal display of claim 14, wherein the gamma reference voltage generator serializing for each of R, G and B of a first and a second polarity gamma reference voltages to output each of R, G and B through each of output terminals,

wherein the sample/hold unit comprises R, g and B sample/hold unit performing sample/hold treatment for each of R, G and B of the serialized gamma reference voltage to output each of sampled first and second polarity gamma reference voltage to the digital-to-analog converter,

wherein each of the R, G and B sample/hold units comprises a first polarity sample/hold circuit sequentially performing sample/hold treatment of a firs polarity gamma reference voltage to output it, and a second polarity sample/hold circuit unit, after completion of the sample/hold treatment in the first polarity, receiving sampling start signal from the first polarity sample/hold circuit unit and sequentially performing sample/hold treatment of a second polarity gamma reference voltage to output them.

20. The liquid crystal display of claim 14, wherein the gamma reference voltage generator serializes first and second R, G and B gamma reference voltages to output them through one output terminal,

wherein the sample/hold unit comprises a first polarity sample/hold unit sequentially performing sample/hold treatment first polarity R, G and B gamma reference voltages of the serialized first and second polarity gamma reference voltages to output sampled first polarity R, G and B gamma reference voltages and a second polarity sample/hold unit, after completion of the sample/hold treatment in the first sample/hold unit, receiving sampling start signal from the first sample/hold unit and sequentially performing sample/hold treatment first polarity R, G and B gamma reference voltages of the serialized first and second polarity gamma reference voltages to output sampled first polarity R, G and B gamma reference voltages,

wherein each of the first and the second polarity sample/hold comprises three sample/hold circuits corresponding to each of R, G and B, and any one of the sample/hold circuit units starts sample/hold treatment by sampling start signal and the sampling start signal is transmitted to another sample/hold circuit unit after completion of the sample/hold treatment.

21. The liquid crystal display of claim 19, wherein the sample/hold circuit unit comprises a plurality of sample/hold circuits in parallel connected to one output terminal to the gamma reference voltage generator,

wherein the sample/hold circuit comprises:

a shift register transmitting sampling start signal to an adjacent sample/hold circuit;

a switch controlling ON/OFF of output of gamma reference voltage in response to the sampling start signal;

a capacitor storing gamma reference voltages inputted through the switch; and

a buffer outputting sample gamma reference voltages stored in the capacitor.

22. The liquid crystal display of claim 19, wherein the sample/hold circuit unit comprises a plurality of sample/hold circuits in parallel connected to one output terminal to the gamma reference voltage generator,

wherein the sample/hold circuit comprises:

a shift register transmitting sampling start signal to an adjacent sample/hold circuit;

a switch controlling ON/Off of gamma reference voltages in response to the sampling start signal;

first and second capacitors storing the gamma reference voltages;

an input switch connected to the switch and transmitting the gamma reference voltages having passed the switch to the first or the second capacitor in response to selection signal from an external device;

a buffer outputting gamma reference voltages stored in the first or the second capacitor; and

an output switch connected to the first and the second capacitors and transmitting gamma reference voltages stored in the first or the second capacitor to the buffer.

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专利名称(译)	液晶显示器及其驱动装置		
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[标]申请(专利权)人(译)	李承WOO		
申请(专利权)人(译)	李承WOO		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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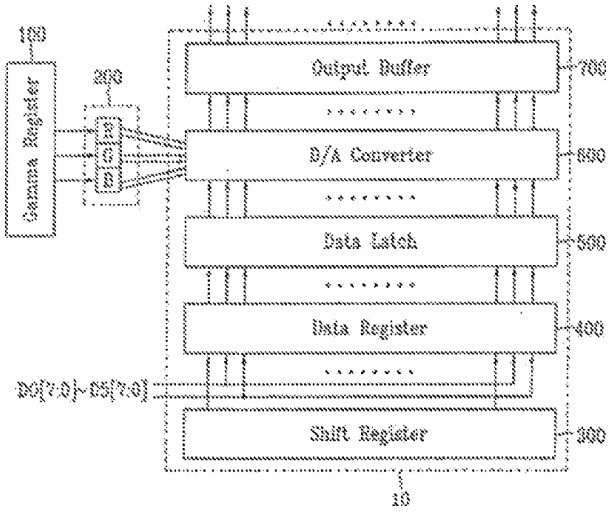
摘要(译)

本发明公开了一种数据驱动器和包括该数据驱动器的液晶显示器，其能够通过在内部或外部产生伽马参考电压来解决液晶显示器上的问题和减少外侧的输入引脚的数量。根据本发明，基于预定的伽马负载信号，通过来自外部设备的预定数据总线为R，G和B中的每一个提供数字伽玛数据，并且伽马参考电压发生器产生伽马。灰度显示的参考电压，用于根据存储的R，G和B中每一个的数字伽玛数据，独立地为R，G和B中的每一个将显示数据转换为模拟数据。模拟转换器将R，G和B中的每一个的图像数据转换为模拟电压，以根据产生的伽马参考电压输出它们。结果，通过为R，G和B中的每一个产生伽马参考电压而不接收它们，可以解决液晶显示器的图像质量问题以及减少外部输入引脚的数量。从外部设备进行控制，使R，G和B中的每一个都具有独立的伽马曲线。