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(54) STACKED STORAGE CAPACITOR STRUCTURE FOR A THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAY

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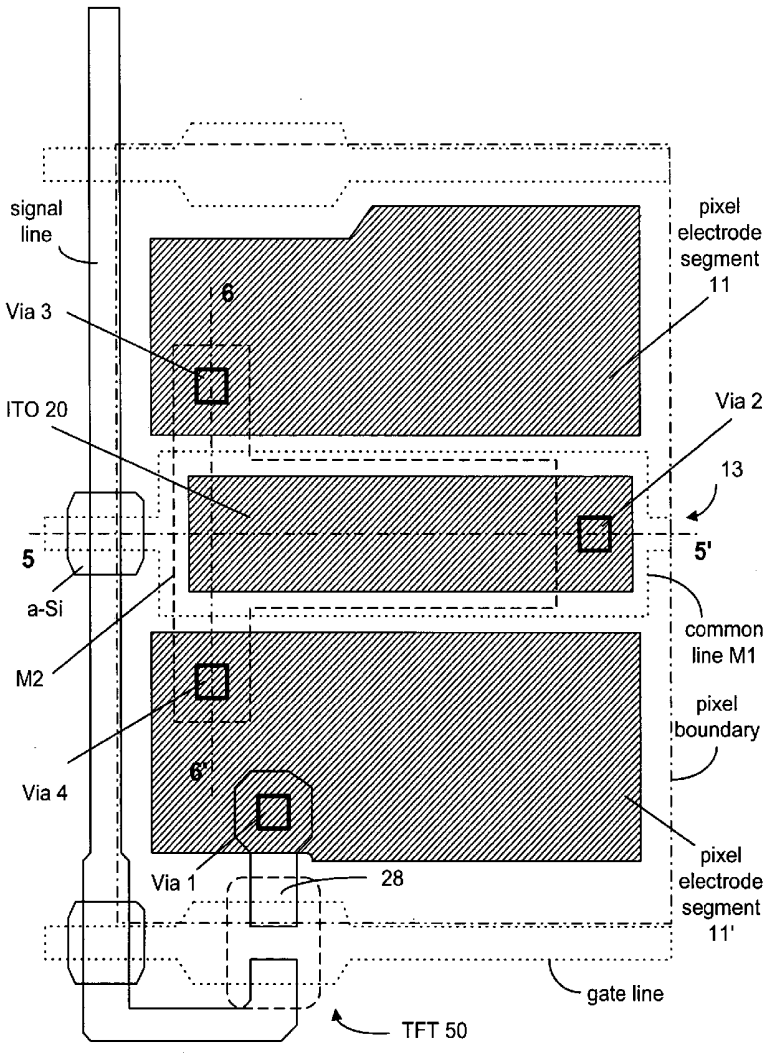
(57) **ABSTRACT**

A stacked storage capacitor structure for use in each pixel of a TFT-LCD, wherein a first storage capacitor is formed by a first metal layer, a gate insulator layer and a second metal layer. The second capacitor is formed by the second metal layer, a passivation insulator layer and an ITO layer. The first metal layer and the ITO layer are joined together through a via hole which is etched in one insulator etching step during the overall fabrication process through both the gate insulator and the passivation insulator layers. As such, the two capacitors are connected in parallel in a stacked configuration. With the stacked storage capacitor structure, the charge storage capacity is increased without significantly affecting the aperture ratio of a pixel. The ITO and the pixel electrode can be different parts of an indium tine oxide layer deposited on the passivation insulator layer.



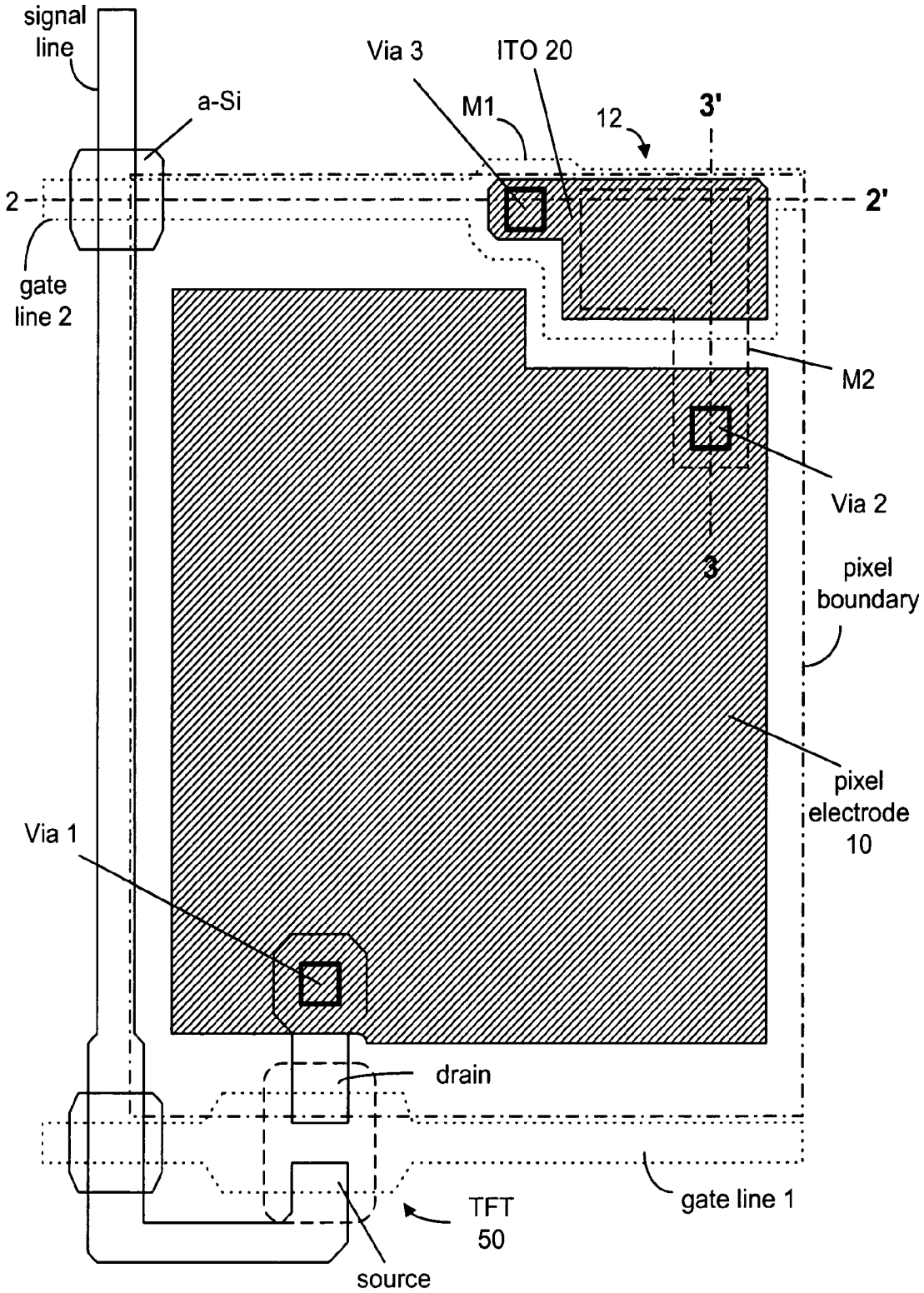

signal line
a-Si
Via 3
ITO 20
M1
12
3'
2
2'
gate line 2
M2
Via 2
3
pixel boundary
pixel electrode 10
Via 1
drain
gate line 1
TFT 50
source

FIG. 1

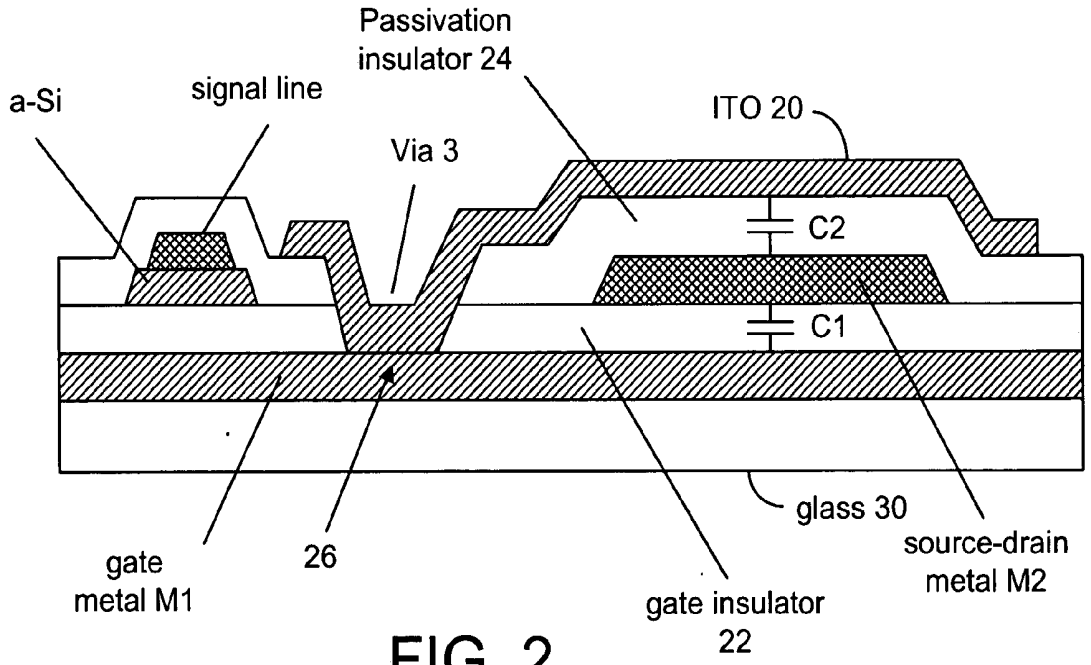

Passivation
insulator 24
a-Si
signal line
ITO 20
Via 3
C2
C1
glass 30
gate
metal M1
26
gate insulator
22
source-drain
metal M2

FIG. 2

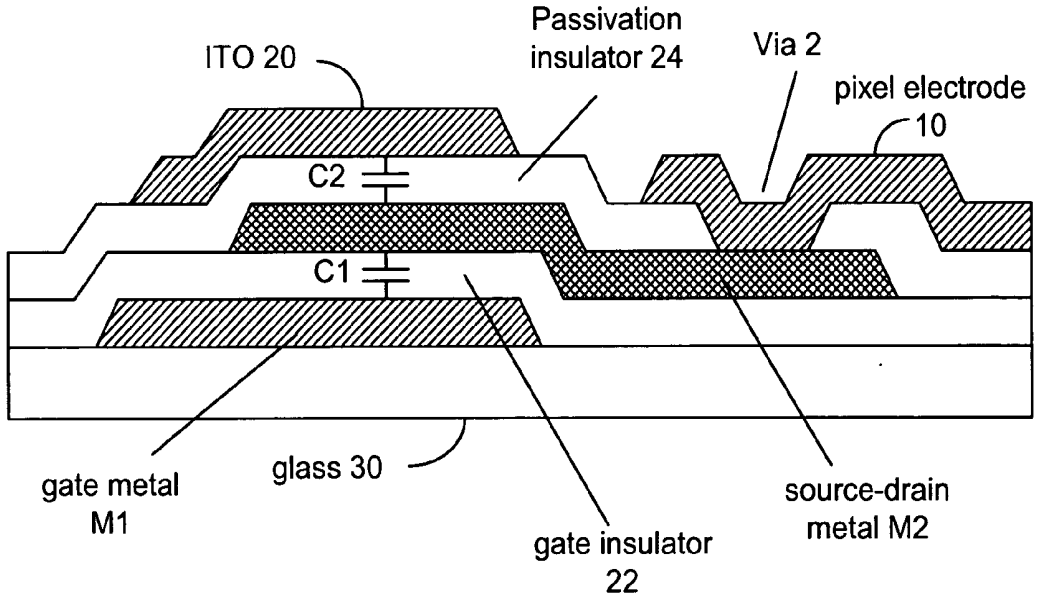

ITO 20
Passivation
insulator 24
Via 2
pixel electrode
10
C2
C1
gate metal
M1
glass 30
gate insulator
22
source-drain
metal M2

FIG. 3

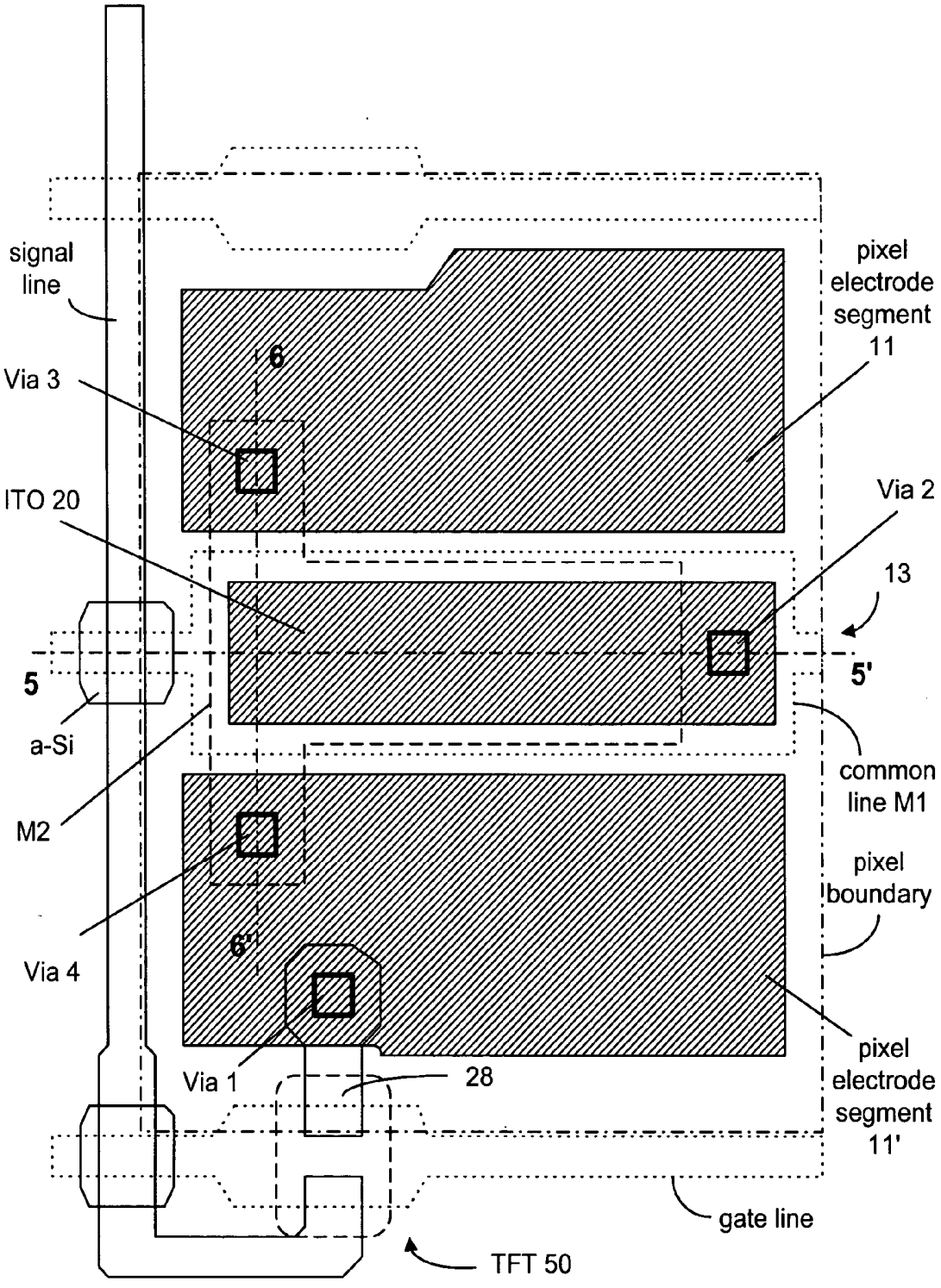

signal line
pixel electrode segment 11
6
Via 3
ITO 20
Via 2
13
5
5'
a-Si
common line M1
M2
pixel boundary
6'
Via 4
Via 1
28
pixel electrode segment 11'
gate line
TFT 50

FIG. 4

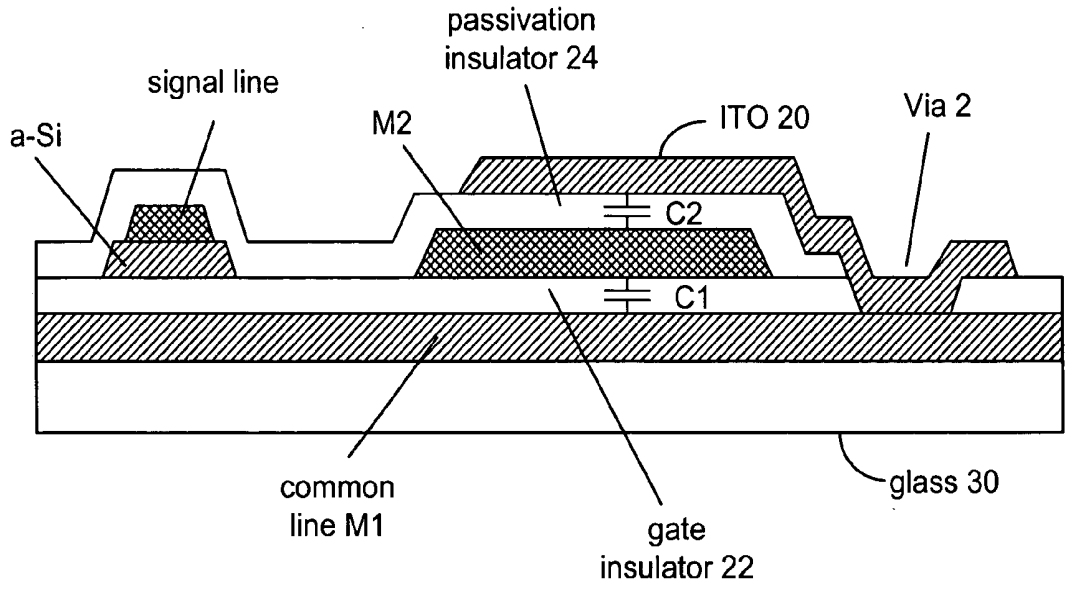

passivation
insulator 24
signal line
a-Si
M2
ITO 20
Via 2
C2
C1
common
line M1
gate
insulator 22
glass 30

FIG. 5

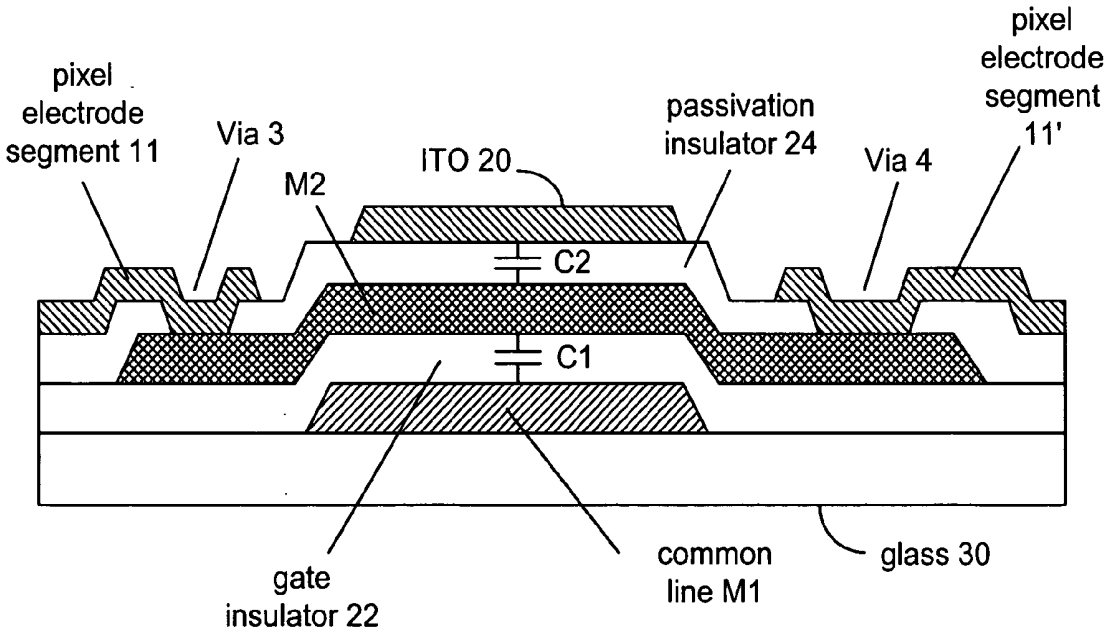

pixel
electrode
segment 11
Via 3
M2
ITO 20
passivation
insulator 24
Via 4
pixel
electrode
segment
11'
C2
C1
gate
insulator 22
common
line M1
glass 30

FIG. 6

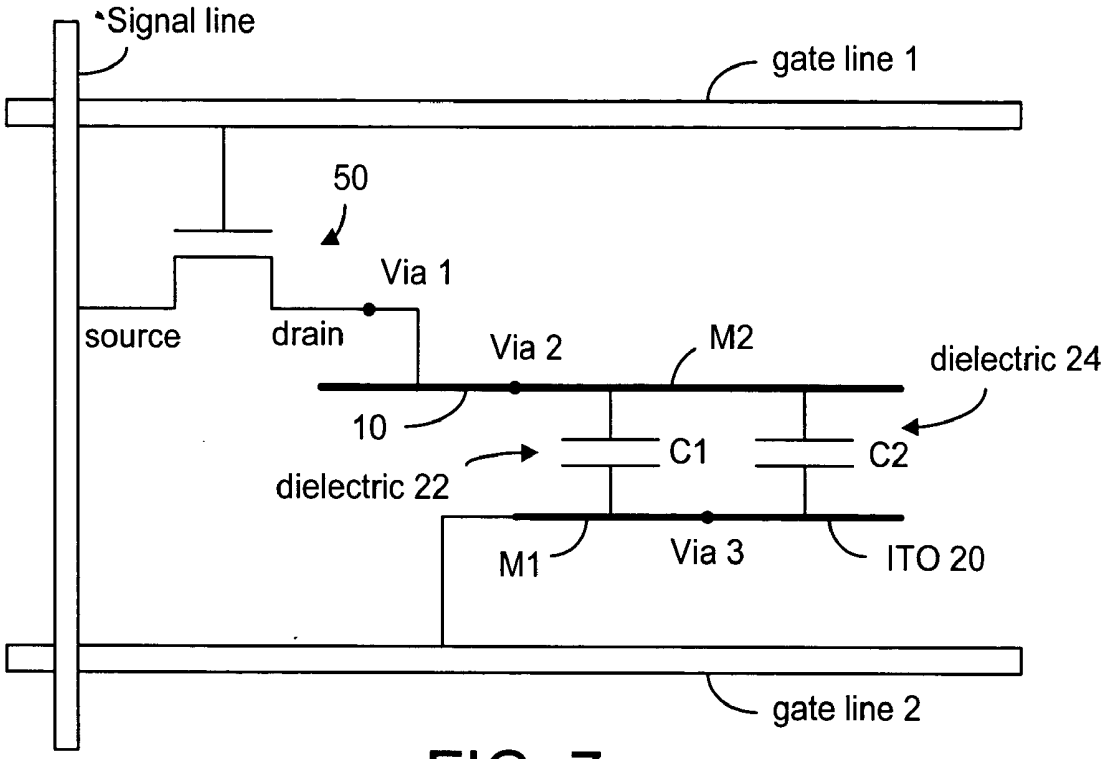

Signal line
gate line 1
50
Via 1
source
drain
Via 2
M2
dielectric 24
10
C1
C2
dielectric 22
M1
Via 3
ITO 20
gate line 2

FIG. 7

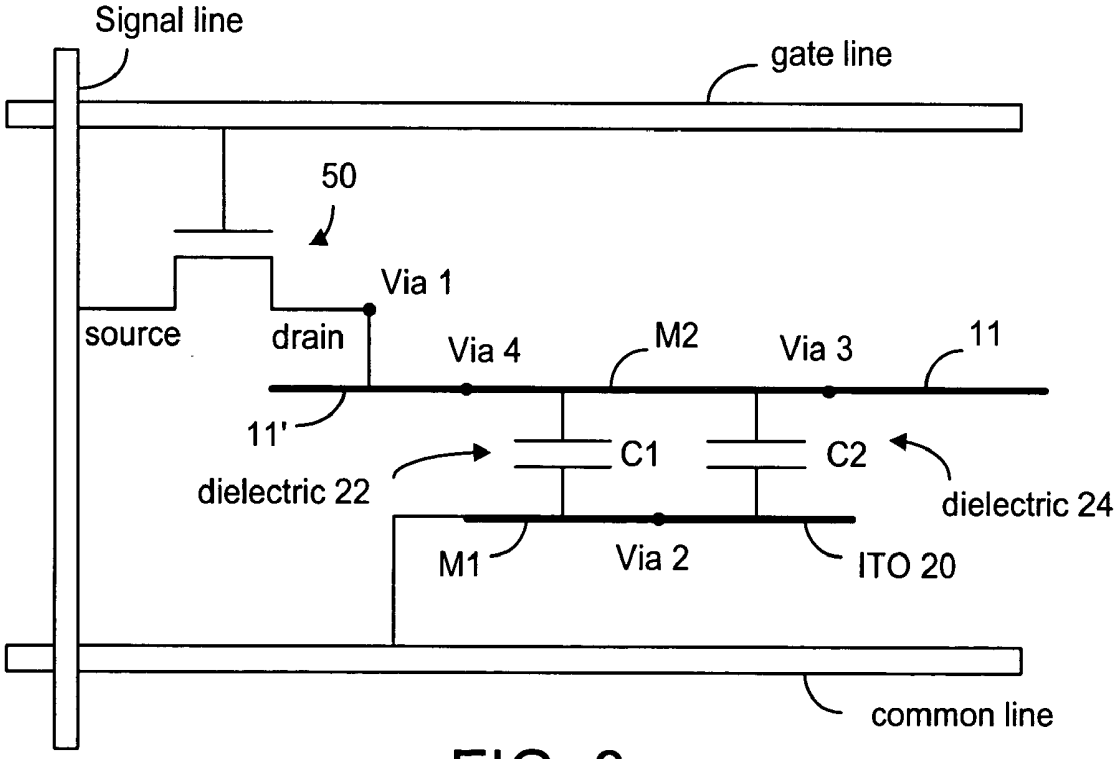

Signal line
gate line
50
Via 1
source
drain
Via 4
M2
Via 3
11
11'
C1
C2
dielectric 22
dielectric 24
M1
Via 2
ITO 20
common line

FIG. 8

STACKED STORAGE CAPACITOR STRUCTURE FOR A THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAY

TECHNICAL FIELD

[0001] The present invention relates to a storage capacitor structure for use in a thin film transistor liquid crystal display particularly an amorphous silicon thin film transistor liquid crystal display.

BACKGROUND OF THE INVENTION

[0002] It is known in the art that thin film transistor liquid crystal displays (commonly referred to as TFT-LCD) seek to minimize the area needed for the storage capacitor used in such displays especially as the resolution of the display increases and therefore the pixel size decreases. The increase in display resolution is especially important for amorphous silicon TFT-LCD displays (a-Si TFT-LCDs). In particular, it is well known that as the display resolution increases, the area available on each pixel of such displays for the fabrication of the storage capacitor is diminished due to aperture ratio considerations. What this means is that for a given pixel it is desired that as the overall size of the pixel decreases, that the maximum amount of the pixel area be devoted to the pixel electrode rather than the storage capacitor associated with the pixel. As a result, as the resolution of a-Si TFT-LCD's has increased, the size of the storage capacitor is reduced to a point that the charge storage capacity significantly affects the performance of the overall LCD display in terms of artifacts such as flicker, image retention and cross-talk. It is therefore important that the storage capacitance and, particularly the area ratio of pixel electrode to the storage capacitance, be increased without adversely affecting the aperture ratio of the pixel.

[0003] In a conventional a-Si TFT-LCD fabrication process, the storage capacitor is either a metal-insulator-metal (MIM) structure or a metal-insulation-ITO (MII) structure. In the MIM structure, the first capacitor plate is the gate metal and the second capacitor plate is the source drain metal separated by the gate insulator layer. In the MII structure, the first capacitor plate is the gate metal and the second capacitor plate is the ITO (indium-tin oxide) electrode separated by both the gate insulator layer and the passivation insulator layer. However, when the resolution is increased, the area available for the storage capacitor is difficult to maintain without sacrificing the aperture ratio.

[0004] In order to increase charge storage capacity without sacrificing the aperture ratio of the pixel, or to maintain the charge storage capacity while increasing the aperture ratio of the pixel in an a-Si TFT-LCD display, it would be desirable to better utilize all layers of conductors and insulators for purposes of increasing the capacitance of the storage capacitor.

SUMMARY OF THE INVENTION

[0005] It is a primary objective of the present invention to increase the charge storage capacity without significantly affecting the aperture ratio in a pixel. The present invention is directed to better utilization of all layers of conductors and insulators for the fabrication of a storage capacitor in an associated pixel of an a-Si TFT-LCD array without changing the currently used fabrication processes for such a-Si TFT-LCD's. To accomplish this result, the source drain metal (M2) is used as a shared capacitor plate in a stacked capacitor structure comprising an MIM structure and a modified MII structure connected in parallel. In particular, the gate metal (M1) and the source-drain metal (M2) sandwich the gate insulator layer so as to form a first capacitor, and the second metal (M2) and the indium titanium oxide (ITO) electrode sandwich a passivation insulator layer so as to form a second capacitor. The two storage capacitors are stacked substantially on top of each other and are interconnected so as to be electrically in parallel with each other, thereby raising the overall capacitance of the storage capacitor while maintaining approximately the same area on the pixel as would be used in conventional storage capacitor fabrication.

[0006] More particularly, in an a-Si TFT-LCD display a stacked storage capacitor structure is described herein wherein a first storage capacitor is formed by the first metal layer acting as a first plate and the second metal layer acting as a second plate, with the gate insulator layer sandwiched in between acting as the insulator for the first storage capacitor. The second capacitor is formed by use of the second metal electrode (M2) acting as the second plate and the ITO electrode acting as the first plate of the second capacitor, with the passivation insulator layer acting as the insulator for the second storage capacitor. The second metal electrode (M2) is shared by both capacitors and the second capacitor is stacked on top of the first capacitor. The first metal electrode (M1) and the ITO electrode are joined together through a via hole and this via hole is etched in one insulator etching step during the overall fabrication process through both the gate insulator and the passivation insulator layers. The middle electrode for the stacked structure is therefore the second metal which is connected to the pixel electrode through via holes in the passivation insulator layer. The ITO electrode is connected to the first metal electrode (M1) through a via hole which is etched through the gate insulator and the passivation insulator. The pixel electrode is connected to the drain of the TFT through another via hole in the passivation insulator.

[0007] Thus, the first aspect of the present invention provides a stacked storage capacitor structure for a thin film transistor liquid crystal display having a plurality of pixels, each pixel having a pixel area, wherein at least some of the pixels have a storage capacitor formed substantially within the pixel area and associated with a stacked storage capacitor structure. The stacked storage capacitor structure comprises:

[0008] a first storage capacitor having a first plate formed by a first electrically conductive layer, a second plate formed by a second electrically conductive layer and a dielectric formed by a first insulator layer positioned between the first electrically conductive layer and the second electrically conductive layer; and

[0009] a second storage capacitor having a first plate formed by a third electrically conductive layer, a second plate formed by the second electrically conductive layer and a dielectric formed by a second insulator layer positioned between the first and second plates, wherein the first electrically conductive layer and the third electrically conductive layer are electrically connected to each other so that the first and second storage capacitors are electrically connected in

parallel, and wherein the second electrically conductive layer is positioned between the first electrically conductive layer and the third electrically conductive layer.

[0010] According to the present invention, each of said at least some of the pixels has a gate line disposed at one edge section of the pixel area for controlling electric charges in the storage capacitor, and the storage capacitor is formed substantially in said one edge section.

[0011] According to the present invention, each of said at least some of the pixels has a semiconductor switching element and a pixel electrode electrically connected to the switching element, and the pixel electrode is located within the pixel area adjacent to said one edge section in a non-overlapping manner.

[0012] According to the present invention, the switching element has a first switching end, a second switching end and a switching control terminal, the first switching end operatively connected to a signal line, the second end operatively connected to the pixel electrode, and each of said at least some of the pixels further comprises a further gate line operatively connected to the switching control terminal of the switch element for causing the opening and closing between the first and second switching ends.

[0013] According to the present invention, the second electrically conductive layer (M2) is operatively connected to the second switching end of the switching element via the pixel electrode and the first electrically conductive layer (M1) is operatively connected to the gate line.

[0014] According to the present invention, the first switching end is a source terminal, the second switching end is a drain terminal, and the switching control terminal is a gate terminal of a transistor, wherein the first electrically conductive layer is a gate metal layer, the first insulator layer is a gate insulator layer and second electrically conductive layer is a source-drain metal layer, and the third electrically conductive layer is made substantially of indium-tin oxide, and the second insulator layer is a passivation insulator layer.

[0015] According to the present invention, part of the passivation insulator layer is disposed adjacent to part of the gate insulator layer, and the pixel electrode is made substantially of indium-tin oxide, and at least part of the pixel electrode and part of the third electrically conductor layer are disposed on different sections of the passivation insulator layer.

[0016] Alternatively, each of said at least some of the pixels comprises

[0017] a semiconductor switching element;

[0018] a gate line disposed at one edge section of the pixel area for controlling the switching element; and

[0019] a common line disposed in a pixel section spaced from the gate line for controlling electric charges in the storage capacitor, and wherein the storage capacitor is formed substantially in said pixel section.

[0020] According to the present invention, each of said at least some of the pixels has a first pixel electrode segment and a second pixel electrode segment located within the pixel area and separated by said pixel section in a non-overlapping manner.

[0021] According to the present invention, the common line is substantially parallel to the gate line.

[0022] According to the present invention, the switching element has a first switching end, a second switching end and a switching control terminal, the first switching end operatively connected to a signal line, the second end operatively connected to the first pixel electrode segment, wherein each of said at least some of the pixels further comprises a gate line operatively connected to the switching control terminal of the switch element for causing the opening and closing between the first and second switching ends.

[0023] According to the present invention, the second electrically conductive layer (M2) is operatively connected to the second switching end of the switching element via the pixel electrode and the first electrically conductive layer (M1) is operatively connected to the common line.

[0024] According to the present invention, the first switching end is a source terminal, the second switching end is a drain terminal, and the switching control terminal is a gate terminal of a transistor, wherein the first electrically conductive layer is a gate metal layer, the first insulator layer is a gate insulator layer and second electrically conductive layer is a source-drain metal layer, and the third electrically conductive layer is made substantially of indium-tin oxide, and the second insulator layer is a passivation insulator layer.

[0025] According to the present invention, part of the passivation insulator layer is disposed adjacent to part of the gate insulator layer, and the first and second pixel electrode segment are made substantially of indium-tin oxide, wherein at least part of the first and second pixel electrode segments and part of the third electrically conductor layer are disposed on different sections of the passivation insulator layer.

[0026] The second aspect of the present invention provides a method of increasing charge storage capacity in a thin film transistor liquid crystal display having a plurality of pixels, each pixel having a pixel area and a pixel electrode located within the pixel area, wherein at least some of the pixels have a storage capacitor structure formed at a section of the pixel area substantially within the pixel area for storing electric charges associated with the pixel electrode, and wherein the section is adjacent to the pixel electrode in a non-overlapping manner. The method comprising the steps of:

[0027] forming a first storage capacitor having a first plate formed by a first electrically conductive layer, a second plate formed by a second electrically conductive layer and a dielectric formed by a first insulator layer positioned between the first electrically conductive layer and the second electrically conductive layer; and

[0028] forming a second storage capacitor having a first plate formed by a third electrically conductive layer, a second plate formed by the second electrically conductive layer and a dielectric formed by a second insulator layer positioned between the first and second plates; and

[0029] electrically connecting the first electrically conductive layer to the third electrically conductive layer so that the first and second storage capacitors are electrically connected in parallel for forming the storage capacitor structure, and

wherein the second electrically conductive layer is positioned between the first electrically conductive layer and the third electrically conductive layer.

[0030] The third aspect of the present invention provides a thin film transistor liquid crystal display, comprising:

[0031] a plurality of pixels arranged in rows and columns, each pixel having a pixel area, a plurality of signal lines disposed between the pixel columns; and

[0032] a plurality of gate lines disposed between the pixel rows, wherein at least some of the pixels have a storage capacitor formed substantially within the pixel area, the storage capacitor comprising:

[0033] a first storage capacitor having a first plate formed by a first electrically conductive layer, a second plate formed by a second electrically conductive layer and a dielectric formed by a first insulator layer positioned between the first electrically conductive layer and the second electrically conductive layer; and

[0034] a second storage capacitor having a first plate formed by a third electrically conductive layer, a second plate formed by the second electrically conductive layer and a dielectric formed by a second insulator layer positioned between the first and second plates, wherein the first electrically conductive layer and the third electrically conductive layer are electrically connected to each other so that the first and second storage capacitors are electrically connected in parallel, and wherein the second electrically conductive layer is positioned between the first electrically conductive layer and the third electrically conductive layer.

[0035] According to the present invention, each of said at least some of the pixels has a further gate line disposed at one edge section of the pixel area for controlling electric charges in the storage capacitor, and the storage capacitor is formed substantially in said one edge section.

[0036] According to the present invention, each of said at least some of the pixels has a semiconductor switching element and a pixel electrode electrically connected to the switching element, and the pixel electrode is located within the pixel area adjacent to said one edge section in a non-overlapping manner.

[0037] According to the present invention, the switching element has a first switching end, a second switching end and a switching control terminal, the first switching end operatively connected to one of said plurality of signal lines, the second end operatively connected to the pixel electrode, and wherein the switching control terminal of the switch element is operatively connected to one of said plurality of gate lines for causing the opening and closing between the first and second switching ends.

[0038] Alternatively, each of said at least some of the pixels comprises

[0039] a semiconductor switching element operatively connected to the gate line; and

[0040] a common line disposed in a pixel section spaced from the gate line for controlling electric charges in the storage capacitor, and wherein the storage capacitor is formed substantially in said pixel section.

[0041] According to the present invention, each of said at least some of the pixels has a first pixel electrode segment and a second pixel electrode segment located within the pixel area and separated by said pixel section in a non-overlapping manner, and the common line is disposed between two adjacent gate lines.

[0042] According to the present invention, the switching element has a first switching end, a second switching end and a switching control terminal, wherein the first switching end is operatively connected to one of said plurality of signal lines, the second end is operatively connected to the first pixel electrode segment, and the switching control terminal of the switch element is operatively connected to one of the gate lines for causing the opening and closing between the first and second switching ends.

[0043] The present invention will become apparent upon reading the description taken in conjunction with **FIGS. 1-8**.

BRIEF DESCRIPTION OF THE DRAWINGS

[0044] For a better understanding of the nature of the present invention, reference is made to the following figures in which:

[0045] **FIG. 1** is a plan view of a pixel where the storage capacitor is fabricated as a storage capacitor-on-gate (Cs-on-gate) design;

[0046] **FIG. 2** is a cross-sectional view taken along line **2-2'** of the pixel of **FIG. 1**;

[0047] **FIG. 3** is a cross-sectional view taken along line **3-3'** of the pixel of **FIG. 1**;

[0048] **FIG. 4** is a plan view of a pixel where the storage capacitor is fabricated as a storage capacitor-on-common (Cs-on-com) design;

[0049] **FIG. 5** is a cross-sectional view taken along line **5-5'** of the pixel of **FIG. 4**;

[0050] **FIG. 6** is a cross-sectional view taken along line **6-6'** of the pixel of **FIG. 4**;

[0051] **FIG. 7** shows an equivalent circuit of the pixel of **FIG. 1**; and

[0052] **FIG. 8** shows an equivalent circuit of the pixel of **FIG. 2**.

DETAILED DESCRIPTION OF THE INVENTION

[0053] As best seen in **FIGS. 1, 2** and **3**, a pixel according to the present invention which typically forms part of a pixel array comprises two general areas, one associated with the pixel electrode **10** and another associated with the control and storage capacitor area **12**. The pixel fabrication technique shown in **FIGS. 1, 2** and **3** is known in the art as a storage capacitor-on-gate design (Cs-on-gate). The fabrication technique in general is with regard to an amorphous silicon thin film transistor liquid crystal display (a-Si TFT-LCD) although the principles described could be used for other types of TFT-LCD displays, and as a p-Si TFT-LCD display.

[0054] As seen in **FIGS. 1, 2** and **3**, a storage capacitor for use in maintaining the state of the pixel electrode and thus of the LCD pixel between scans, comprises two storage

capacitors shown diagrammatically as C1 and C2. The first capacitor C1 is formed between a first metal layer M1 (gate electrode) and a second metal layer M2. The second capacitor C2 is also shown diagrammatically in **FIGS. 2 and 3** and is formed between the second metal layer M2 and an indium tin oxide (ITO) layer **20**. For capacitor C1, metal layer M1 forms the first plate of the capacitor and metal layer M2 forms the second plate of the capacitor and the dielectric material therebetween is the gate insulator **22**. For capacitor C2, the second plate is fabricated by the same metal layer M2 and the first plate is formed by the ITO layer **20**. The dielectric between these two plates is the passivation insulator layer **24**.

[**0055**] Capacitors C1 and C2 therefore share one plate, namely the metal layer M2, and the two capacitors are electrically connected in parallel to each other by the ITO layer **20** making contact with the metal layer M1 by means of Via **3** at region **26**.

[**0056**] For fabricating such an a-Si TFT-LCD a five-mask process is typically used. Such a process is well known in the art. First, the gate metal M1 is deposited on a glass substrate **30**. This gate metal is then patterned to the particular design needed for the pixels. A nitride layer is then deposited. Part of the nitride layer is the gate insulator layer **22**. This is followed by the forming of an amorphous silicon (a-Si) and n+ doped amorphous silicon layer (n+ a-Si) by a plasma-enhanced chemical vapor deposition (PECVD) process. In addition, n+ a-Si and a-Si islands are formed on the nitride layer. Then a metal layer is deposited and patterned so as to form the source-drain electrode and the shared capacitor plate M2. After the etching of n+ a-Si to form the conducting channel for the thin film transistor (TFT) **50**, a passivation insulator layer **24** is deposited. Via holes Via **1**, Via **2** and Via **3** are then created by selective etching. Via **1** is used for the drain contact, and Via **2** is used for providing a contact point on the shared capacitor plate M2. Via **3** is for providing a contact point on the gate metal layer M1 (gate electrode). Via **1** and Vail **2** are created by etching the passivation insulator layer **24**, while Via **3** is created by etching both the passivation insulator layer **24** and the gate insulator layer **22**. An ITO layer is then deposited on top of the etched layers and patterned. After etching, part of the ITO layer forms the pixel electrode **10**, which contacts the source-drain metal or the shared capacitor plate M2 through Via **2**. The pixel electrode **10** is also connected to the drain contact through Via **1**. As such, the shared capacitor plate M2 is electrically connected to the drain of the TFT **50** through the pixel electrode **10**. The part of the ITO layer that forms the ITO layer **20** and serves as the top capacitor plate for storage capacitor C2 is connected to the gate electrode (gate metal) M1 through Via **3** (see **FIG. 7**). In this manner, a stacked storage capacitor structure comprising capacitors C1 and C2 is formed.

[**0057**] As can be seen in **FIGS. 2 and 3**, this stacked storage capacitor structure effectively uses the same general area **12** (see **FIG. 1**) that would otherwise be used for a storage capacitor comprising only a single pair of plates; but by the design of the present invention, the stacked storage capacitor effectively obtains a second pair of plates to form capacitor C2, thereby nearly doubling the total capacitance of the storage capacitor while maintaining approximately the same area that would otherwise be used to form a storage capacitor with only a single pair of plates. The equivalent circuit of the pixel structure of **FIG. 1** is shown in **FIG. 7**.

[**0058**] **FIGS. 4, 5** and **6** show another technique used to form an a-Si TFT-LCD display known as storage capacitor-on-common (Cs-on-com) design. As seen in **FIG. 4**, two pixel electrode segments **11** and **11'** are separated by a region **13** having a common line M1. It is in this region that the stacked storage capacitor structure according to the present invention is formed.

[**0059**] **FIGS. 5 and 6** show the cross-sectional views taken along lines **5-5'** and **6-6'** respectively. In this fabrication design, capacitor C1 has a first plate formed by the metal layer M1 (common line) and a second plate formed by the source-drain metal M2. The gate insulator layer **22** forms the dielectric for capacitor C1. The second capacitor C2 has a first plate formed by the ITO layer **20** and a second plate formed by the source-drain metal M2. The passivation insulator layer **24** is the dielectric for capacitor C2. Thus, C1 and C2 have a shared capacitor plate M2. The pixel electrode **11'** is connected to the drain electrode **28** of the TFT **50** by Via **1** (see **FIG. 4**). The pixel electrode segment **11'** is also connected to the shared capacitor plate M2 through Via **4**. Similarly, the pixel electrode segment **11** is connected to the shared capacitor plate M2 through Via **3**. The ITO layer **20** for capacitor C2 is connected to the common line M1 through Via **2** see **FIG. 8**). In this manner, a stacked storage capacitor structure is formed. The equivalent circuit for the pixel structure of **FIG. 4** is shown in **FIG. 8**. As with the fabrication process as described in conjunction with **FIGS. 2 and 3**, a five-mask process can be used.

[**0060**] As can be seen in the equivalent circuits shown in **FIGS. 7 and 8**, the source-drain metal layer M2 is a shared capacitor plate for the storage capacitors C1 and C2 and these two capacitors are connected at Via **3** in parallel so as to increase the charge storage capacity associated with the pixel electrode **10** (**FIG. 7**) or with the pixel electrode segments **11**, **11'** (**FIG. 8**). In both embodiments, M1 and ITO **20** are separately used for two capacitor plates of the stacked capacitor structure, and insulator layers **22** and **24** are separately used as the dielectric for C1 and the dielectric for C2. The difference between the two embodiments is where M1 is connected to. All the electrically conductive layers M1, M2, ITO **20** and the insulator layers **22**, **24** are generally required in the five-mask fabricating process for most TFT-LCD displays. It is therefore apparent from the present description that a stacked storage capacitor structure, according to the present invention, can be fabricated for a-Si TFT-LCD display without additional material layers or masks. According to the present invention, the amount of pixel real estate associated with the storage capacitor is thereby minimized, which in turn maximizes the aperture ratio of the pixel, providing better performance as the resolution of the pixel increases.

[**0061**] It will be apparent to those skilled in the art that various modifications and variations can be made in the structure and method of the present invention without departing from the scope of the present invention. As a result, it is intended that the present invention covers such modifications and variations provided that they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A stacked storage capacitor structure for a thin film transistor liquid crystal display having a plurality of pixels, each pixel having a pixel area, wherein at least some of the pixels have a storage capacitor formed substantially within the pixel area and associated with a stacked storage capacitor structure, the stacked storage capacitor structure comprising:

a first storage capacitor having a first plate formed by a first electrically conductive layer, a second plate formed by a second electrically conductive layer and a dielectric formed by a first insulator layer positioned between the first electrically conductive layer and the second electrically conductive layer; and

a second storage capacitor having a first plate formed by a third electrically conductive layer, a second plate formed by the second electrically conductive layer and a dielectric formed by a second insulator layer positioned between the first and second plates, wherein the first electrically conductive layer and the third electrically conductive layer are electrically connected to each other so that the first and second storage capacitors are electrically connected in parallel, and wherein the second electrically conductive layer is positioned between the first electrically conductive layer and the third electrically conductive layer.

2. A stacked storage capacitor structure as defined in claim 1 wherein each of said at least some of the pixels has a gate line disposed at one edge section of the pixel area for controlling electric charges in the storage capacitor, and wherein the storage capacitor is formed substantially in said one edge section.

3. A stacked storage capacitor structure as defined in claim 2, wherein each of said at least some of the pixels has a semiconductor switching element and a pixel electrode electrically connected to the switching element, and wherein the pixel electrode is located within the pixel area adjacent to said one edge section in a non-overlapping manner.

4. A stacked storage capacitor structure as defined in claim 3, wherein the switching element has a first switching end, a second switching end and a switching control terminal, the first switching end operatively connected to a signal line, the second end operatively connected to the pixel electrode, and wherein each of said at least some of the pixels further comprises a further gate line operatively connected to the switching control terminal of the switch element for causing the opening and closing between the first and second switching ends.

5. A stacked storage capacitor structure as defined in claim 4, wherein the second electrically conductive layer (M2) is operatively connected to the second switching end of the switching element via the pixel electrode and the first electrically conductive layer (M1) is operatively connected to the gate line.

6. A stacked storage capacitor structure as defined in claim 5, wherein the first switching end is a source terminal, the second switching end is a drain terminal, and the switching control terminal is a gate terminal of a transistor, and wherein the first electrically conductive layer is a gate metal layer, the first insulator layer is a gate insulator layer and second electrically conductive layer is a source-drain metal layer.

7. A stacked storage capacitor structure as defined in claim 6, wherein the third electrically conductive layer is made substantially of indium-tin oxide, and the second insulator layer is a passivation insulator layer.

8. A stacked storage capacitor structure as defined in claim 7, wherein part of the passivation insulator layer is disposed adjacent to part of the gate insulator layer, and the pixel electrode is made substantially of indium-tin oxide, and wherein at least part of the pixel electrode and part of the third electrically conductor layer are disposed on different sections of the passivation insulator layer.

9. A stacked storage capacitor structure as defined in claim 1, wherein each of said at least some of the pixels comprises

a semiconductor switching element;

a gate line disposed at one edge section of the pixel area for controlling the switching element; and

a common line disposed in a pixel section spaced from the gate line for controlling electric charges in the storage capacitor, and wherein the storage capacitor is formed substantially in said pixel section.

10. A stacked storage capacitor structure as defined in claim 9, wherein each of said at least some of the pixels has a first pixel electrode segment and a second pixel electrode segment located within the pixel area and separated by said pixel section in a non-overlapping manner.

11. A stacked storage capacitor structure as defined in claim 9, wherein the common line is substantially parallel to the gate line.

12. A stacked storage capacitor structure as defined in claim 10, wherein the switching element has a first switching end, a second switching end and a switching control terminal, the first switching end operatively connected to a signal line, the second end operatively connected to the first pixel electrode segment, and wherein each of said at least some of the pixels further comprises a gate line operatively connected to the switching control terminal of the switch element for causing the opening and closing between the first and second switching ends.

13. A stacked storage capacitor structure as defined in claim 12, wherein the second electrically conductive layer (M2) is operatively connected to the second switching end of the switching element via the pixel electrode and the first electrically conductive layer (M1) is operatively connected to the common line.

14. A stacked storage capacitor structure as defined in claim 13, wherein the first switching end is a source terminal, the second switching end is a drain terminal, and the switching control terminal is a gate terminal of a transistor, and wherein the first electrically conductive layer is a gate metal layer, the first insulator layer is a gate insulator layer and second electrically conductive layer is a source-drain metal layer.

15. A stacked storage capacitor structure as defined in claim 14, wherein the third electrically conductive layer is made substantially of indium-tin oxide, and the second insulator layer is a passivation insulator layer.

16. A stacked storage capacitor structure as defined in claim 15, wherein part of the passivation insulator layer is disposed adjacent to part of the gate insulator layer, and the first and second pixel electrode segment are made substantially of indium-tin oxide, and wherein at least part of the first and second pixel electrode segments and part of the

third electrically conductor layer are disposed on different sections of the passivation insulator layer.

17. A method of increasing charge storage capacity in a thin film transistor liquid crystal display having a plurality of pixels, each pixel having a pixel area and a pixel electrode located within the pixel area, wherein at least some of the pixels have a storage capacitor structure formed at a section of the pixel area substantially within the pixel area for storing electric charges associated with the pixel electrode, and wherein the section is adjacent to the pixel electrode in a non-overlapping manner, said method comprising the steps of:

forming a first storage capacitor having a first plate formed by a first electrically conductive layer, a second plate formed by a second electrically conductive layer and a dielectric formed by a first insulator layer positioned between the first electrically conductive layer and the second electrically conductive layer; and

forming a second storage capacitor having a first plate formed by a third electrically conductive layer, a second plate formed by the second electrically conductive layer and a dielectric formed by a second insulator layer positioned between the first and second plates; and

electrically connecting the first electrically conductive layer to the third electrically conductive layer so that the first and second storage capacitors are electrically connected in parallel for forming the storage capacitor structure, and wherein the second electrically conductive layer is positioned between the first electrically conductive layer and the third electrically conductive layer.

18. A thin film transistor liquid crystal display comprising:

a plurality of pixels arranged in rows and columns, each pixel having a pixel area,

a plurality of signal lines disposed between the pixel columns; and

a plurality of gate lines disposed between the pixel rows, wherein at least some of the pixels have a storage capacitor formed substantially within the pixel area, the storage capacitor comprising:

a first storage capacitor having a first plate formed by a first electrically conductive layer, a second plate formed by a second electrically conductive layer and a dielectric formed by a first insulator layer positioned between the first electrically conductive layer and the second electrically conductive layer; and

a second storage capacitor having a first plate formed by a third electrically conductive layer, a second plate formed by the second electrically conductive layer and a dielectric formed by a second insulator layer positioned between the first and second plates, wherein the first electrically conductive layer and the third electrically conductive layer are electrically connected to each other so that the first and second storage capacitors are electrically connected in parallel, and wherein the second electrically conductive layer is positioned between the first electrically conductive layer and the third electrically conductive layer.

19. A thin-film liquid crystal display as defined in claim 18, wherein each of said at least some of the pixels has a further gate line disposed at one edge section of the pixel area for controlling electric charges in the storage capacitor, and wherein the storage capacitor is formed substantially in said one edge section.

20. A thin-film liquid crystal display as defined in claim 18, wherein each of said at least some of the pixels has a semiconductor switching element and a pixel electrode electrically connected to the switching element, and wherein the pixel electrode is located within the pixel area adjacent to said one edge section in a non-overlapping manner.

21. A thin-film liquid crystal display as defined in claim 20, wherein the switching element has a first switching end, a second switching end and a switching control terminal, the first switching end operatively connected to one of said plurality of signal lines, the second end operatively connected to the pixel electrode, and wherein the switching control terminal of the switch element is operatively connected to one of said plurality of gate lines for causing the opening and closing between the first and second switching ends.

22. A thin-film liquid crystal display as defined in claim 18, wherein each of said at least some of the pixels comprises

a semiconductor switching element operatively connected to the gate line

a common line disposed in a pixel section spaced from the gate line for controlling electric charges in the storage capacitor, and wherein the storage capacitor is formed substantially in said pixel section.

23. A thin-film liquid crystal display as defined in claim 18, wherein each of said at least some of the pixels has a first pixel electrode segment and a second pixel electrode segment located within the pixel area and separated by said pixel section in a non-overlapping manner.

24. A thin-film liquid crystal display as defined in claim 23, wherein the common line is disposed between two adjacent gate lines.

25. A thin-film liquid crystal display as defined in claim 23, wherein the switching element has a first switching end, a second switching end and a switching control terminal, wherein the first switching end is operatively connected to one of said plurality of signal lines, the second end is operatively connected to the first pixel electrode segment, and the switching control terminal of the switch element is operatively connected to one of the gate lines for causing the opening and closing between the first and second switching ends.

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专利名称(译)	用于薄膜晶体管液晶显示器的堆叠存储电容器结构		
公开(公告)号	US20060119753A1	公开(公告)日	2006-06-08
申请号	US11/004389	申请日	2004-12-03
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电股份有限公司		
当前申请(专利权)人(译)	友达光电股份有限公司		
[标]发明人	LUO FANG CHEN LO CHANG CHENG		
发明人	LUO, FANG-CHEN LO, CHANG-CHENG		
IPC分类号	G02F1/1343 G02F1/133 G02F1/136 G02F1/1362 H01L21/027 H01L27/12 H01L29/786		
CPC分类号	G02F1/136213 H01L27/12		
其他公开文献	US7675582		
外部链接	Espacenet USPTO		

摘要(译)

一种用于TFT-LCD的每个像素的堆叠存储电容器结构，其中第一存储电容器由第一金属层，栅极绝缘层和第二金属层形成。第二电容器由第二金属层，钝化绝缘层和ITO层形成。第一金属层和ITO层通过通孔连接在一起，通孔在整个制造过程中通过栅绝缘体和钝化绝缘层在一个绝缘体蚀刻步骤中被蚀刻。这样，两个电容器以堆叠配置并联连接。利用堆叠的存储电容器结构，电荷存储容量增加而不会显着影响像素的孔径比。ITO和像素电极可以是沉积在钝化绝缘层上的铟锡氧化物层的不同部分。