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(54) LIQUID CRYSTAL DSPLAY

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(57) **ABSTRACT**

A liquid crystal display includes an insulating substrate, gate and data lines formed on the substrate to define pixel areas, or collectively a display area. Gate signal interconnection wires are formed at a corner portion of the substrate outside the display area to transmit gate electrical signals, and provided with gate signal interconnection lines and first and second gate signal interconnection pads connected to both ends of the gate signal interconnection lines. A gate insulating layer, and a protective layer are further formed on the substrate, and provided with first and second contact holes exposing the first and second gate signal interconnection pads. Gate and data signal transmission films are attached to the substrate, and provided with first and second gate signal leads and first and second gate signal wires. The first and second gate signal leads are connected to the first and second gate signal interconnection pads through the first and second contact holes. The first or the second gate signal lead completely covers the first or the second contact hole at least in the longitudinal direction of the lead.

Fig. 1

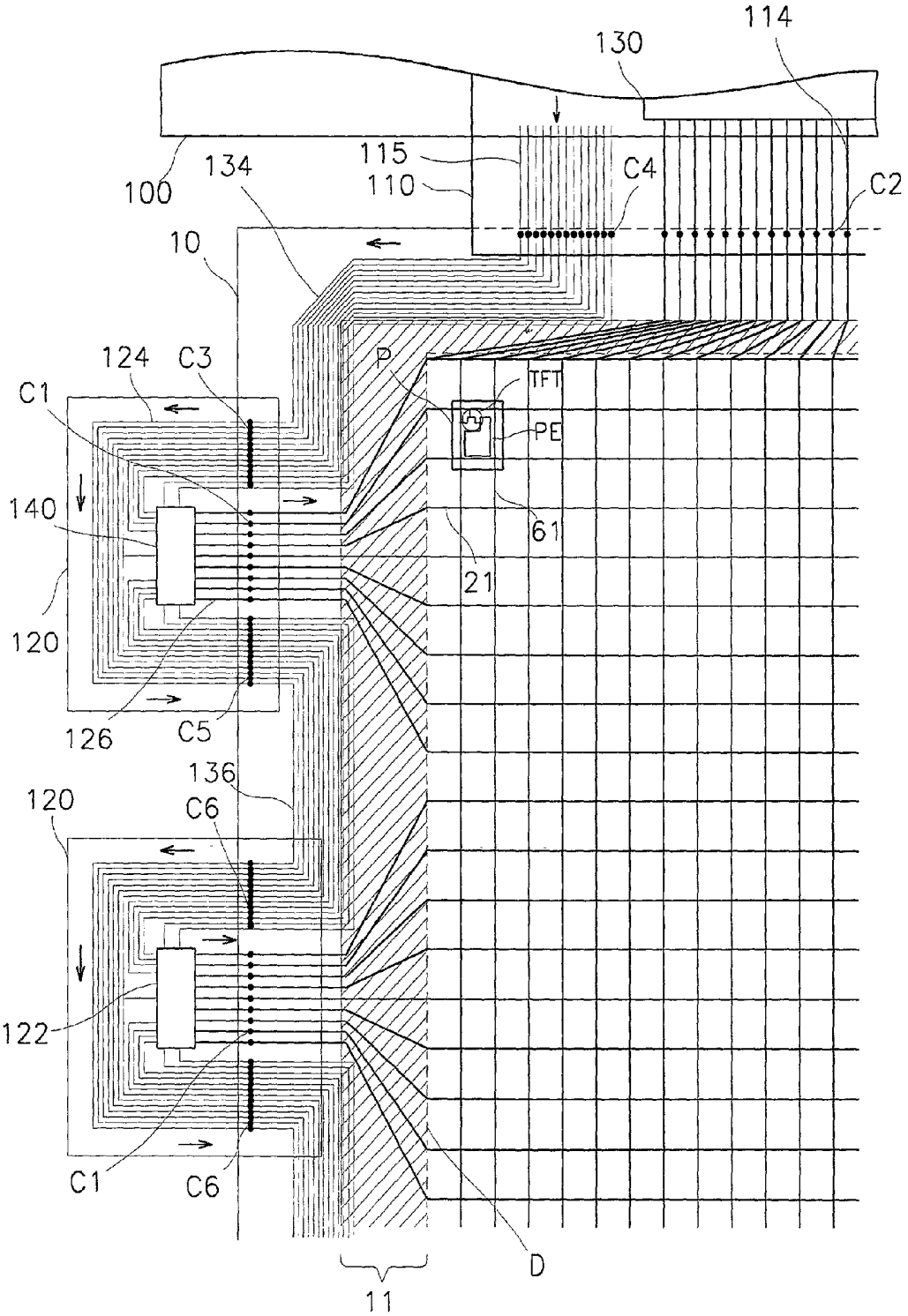

114
130
115
134
100
110
C4
C2
10
124
C3
P
TFT
C1
PE
140
61
21
120
126
C5
136
120
C6
122
C1
C6
D
11

Fig.2

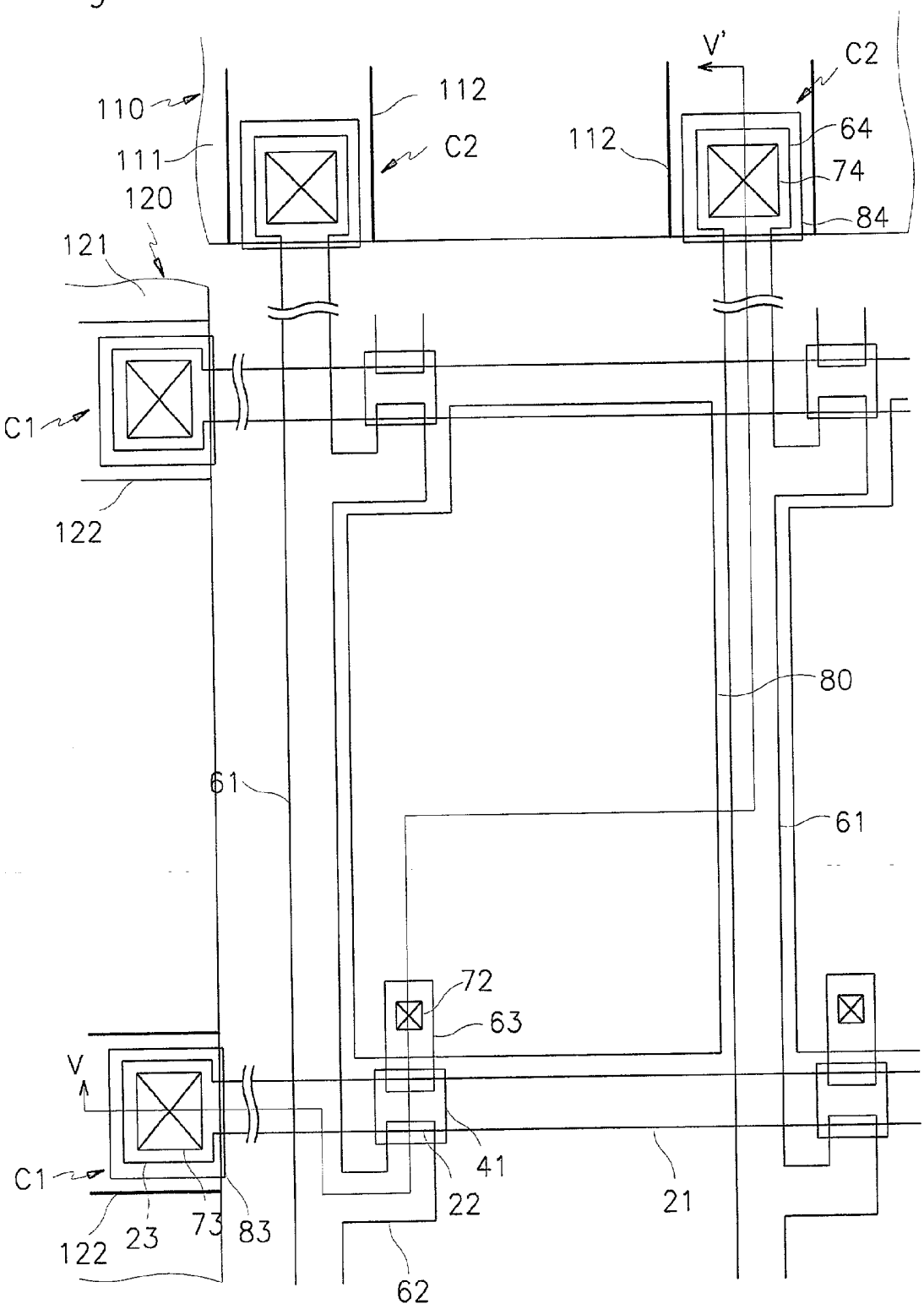

110
111
120
121
112
C2
V'
C2
112
64
74
84
C1
122
80
61
61
72
63
V
C1
122
23
73
83
41
22
21
62

Fig.3

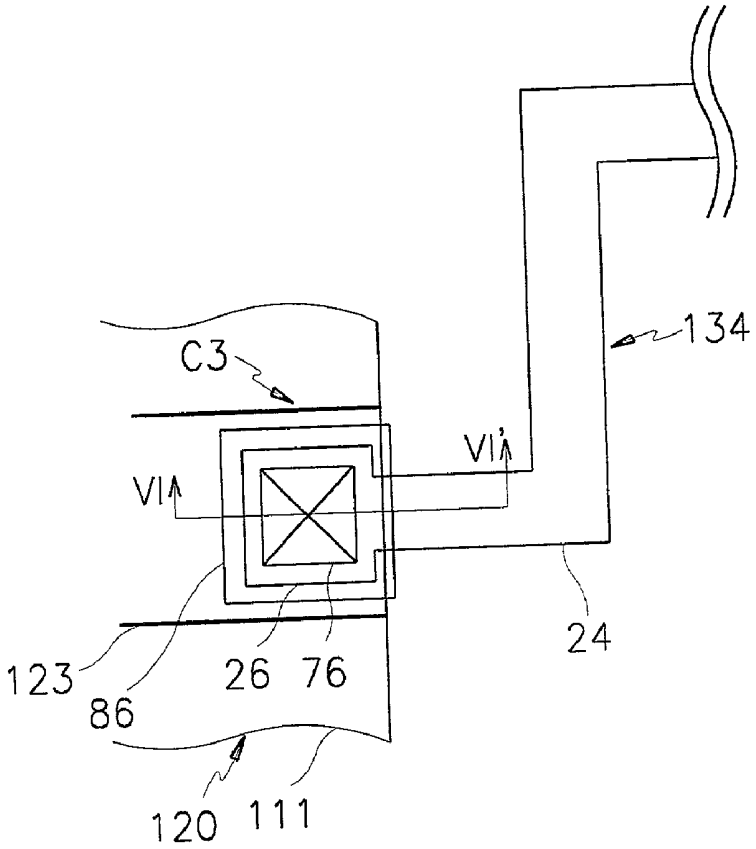


Fig.4

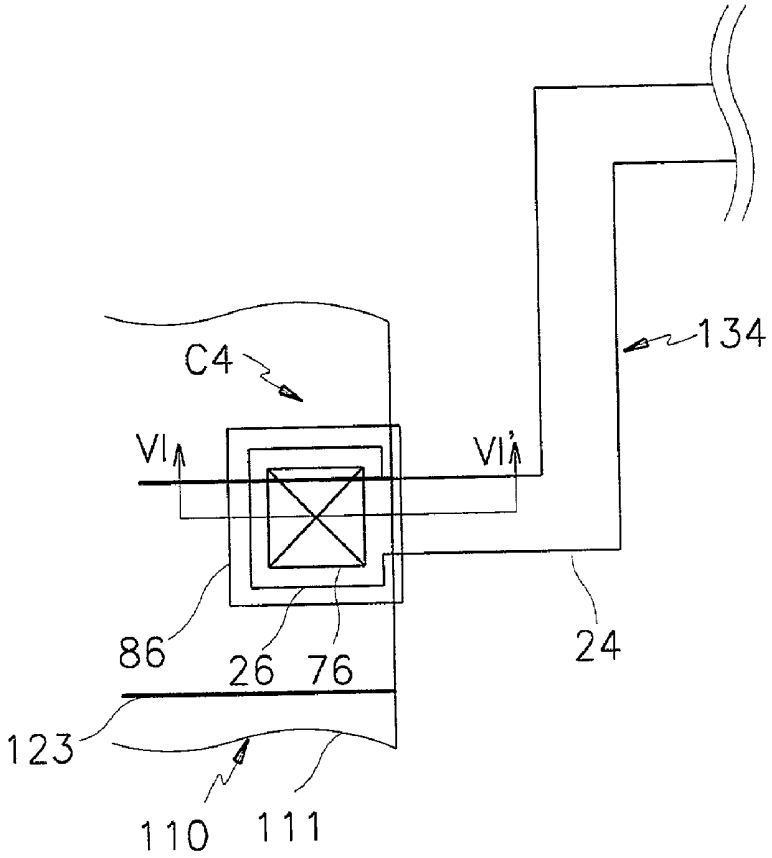
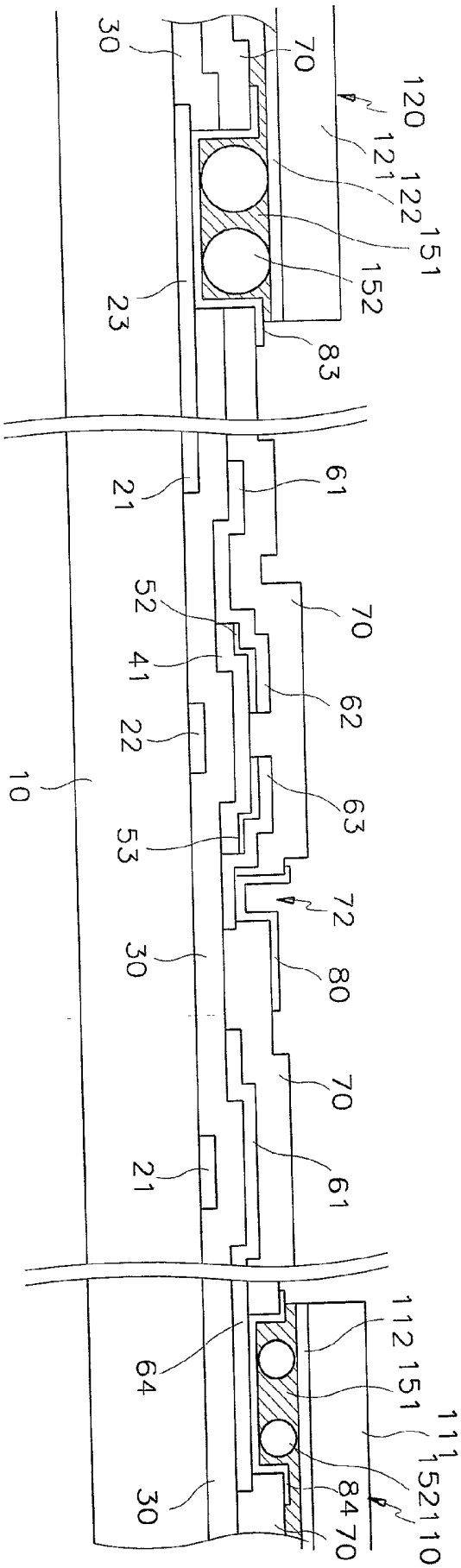


Fig.5


30
70
120
121
122
151
152
23
83
21
61
52
70
41
62
22
10
63
53
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80
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21
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152
84
70
30
10

Fig.6

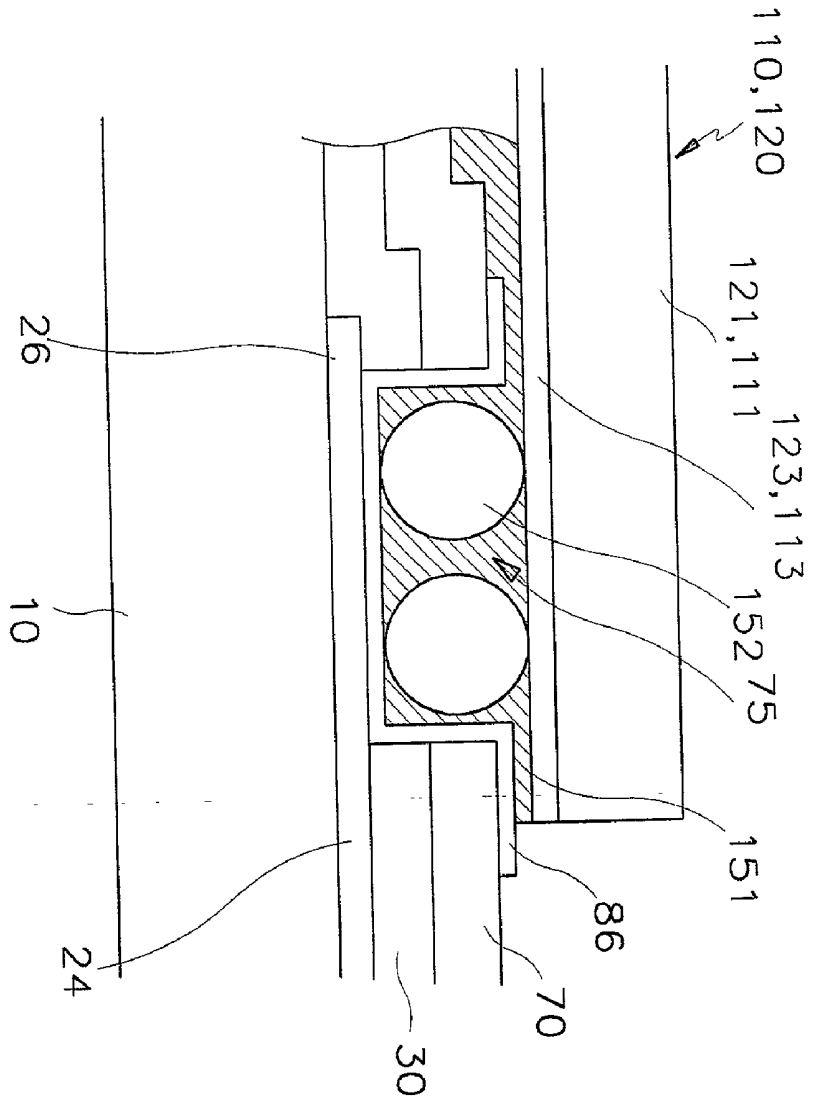


Fig.7a

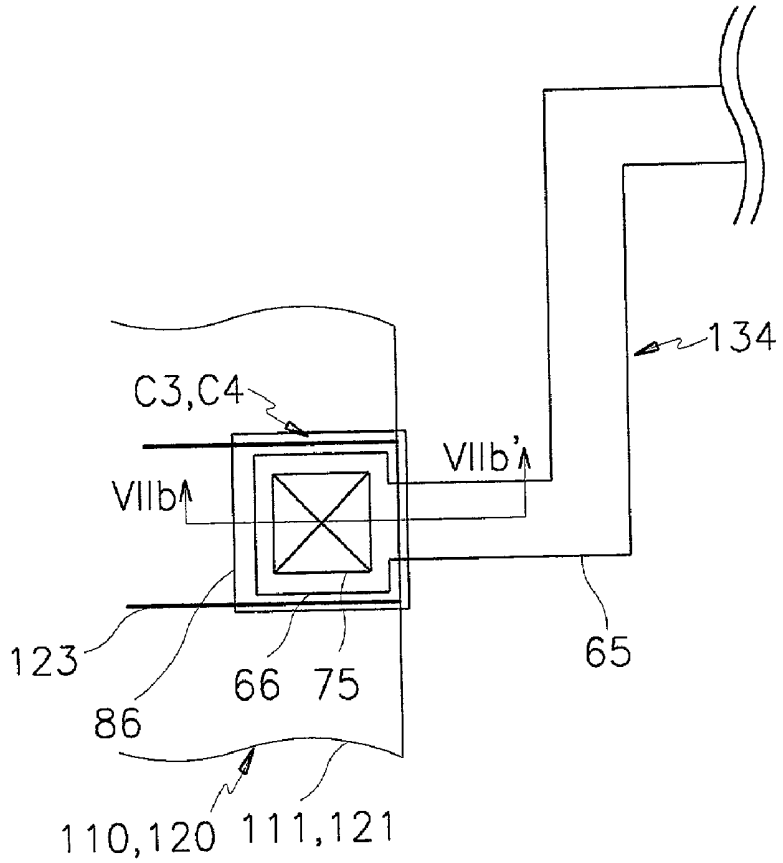


Fig.7b

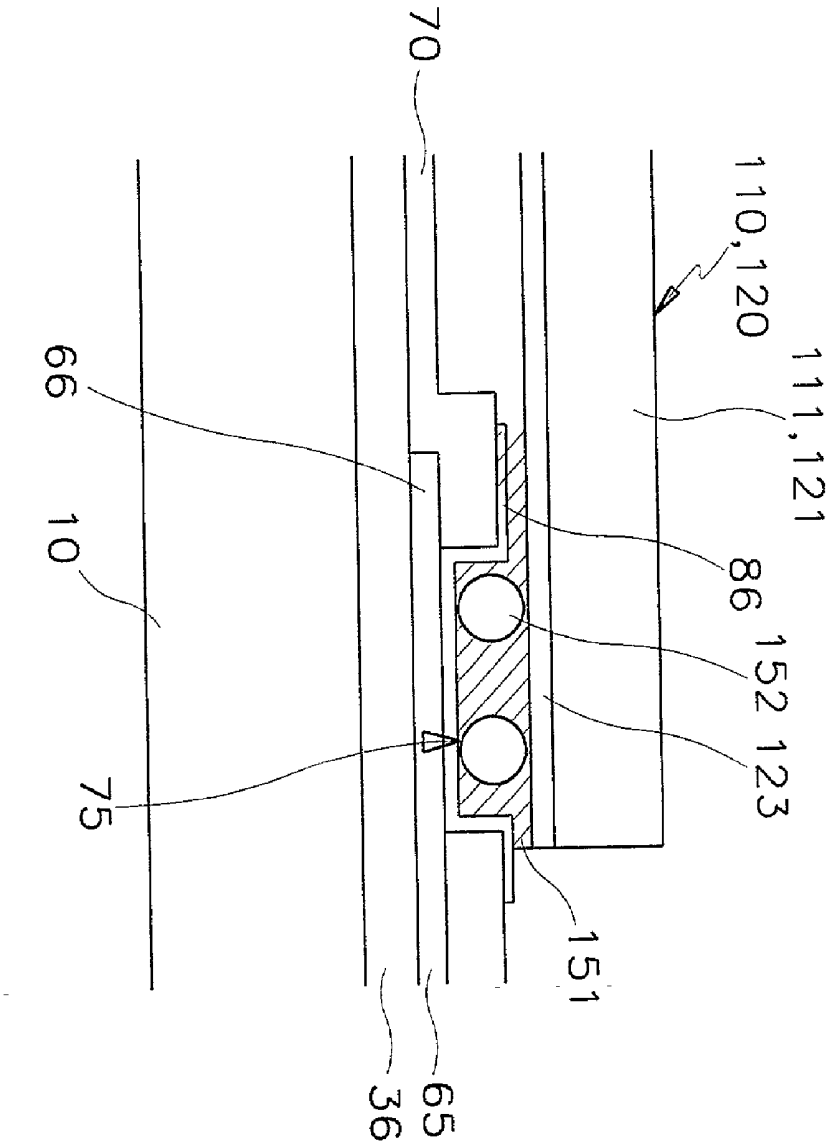


Fig.8a

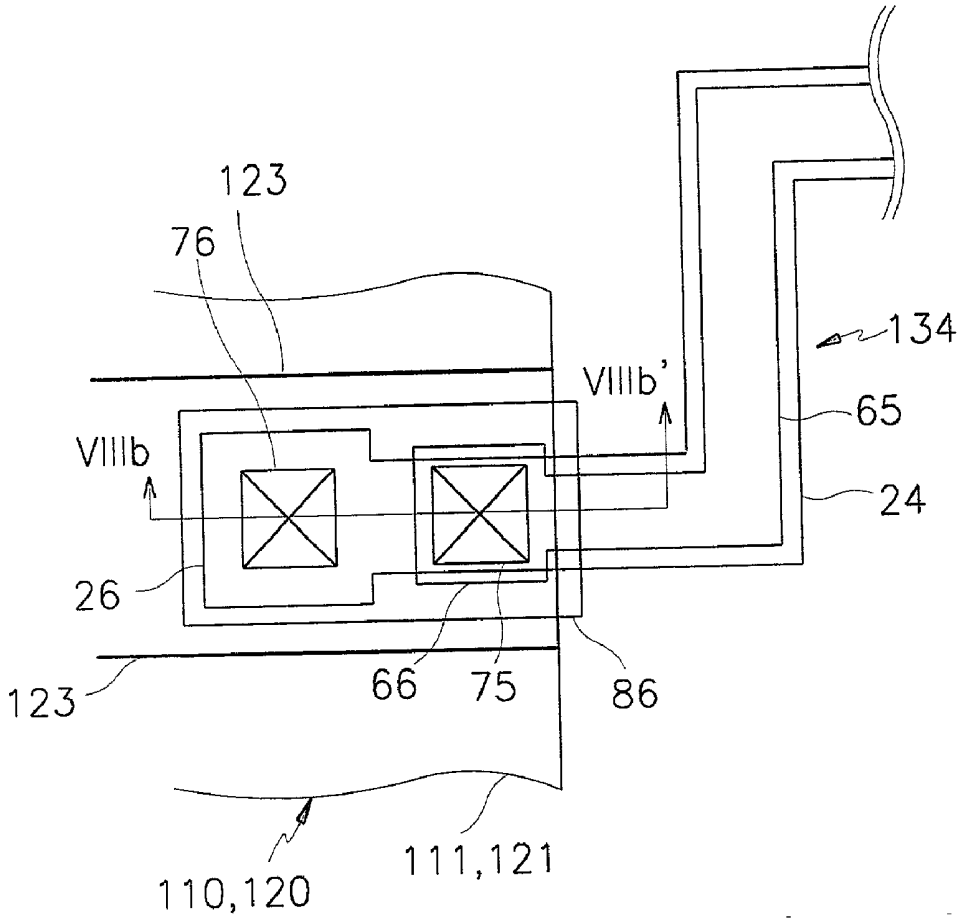
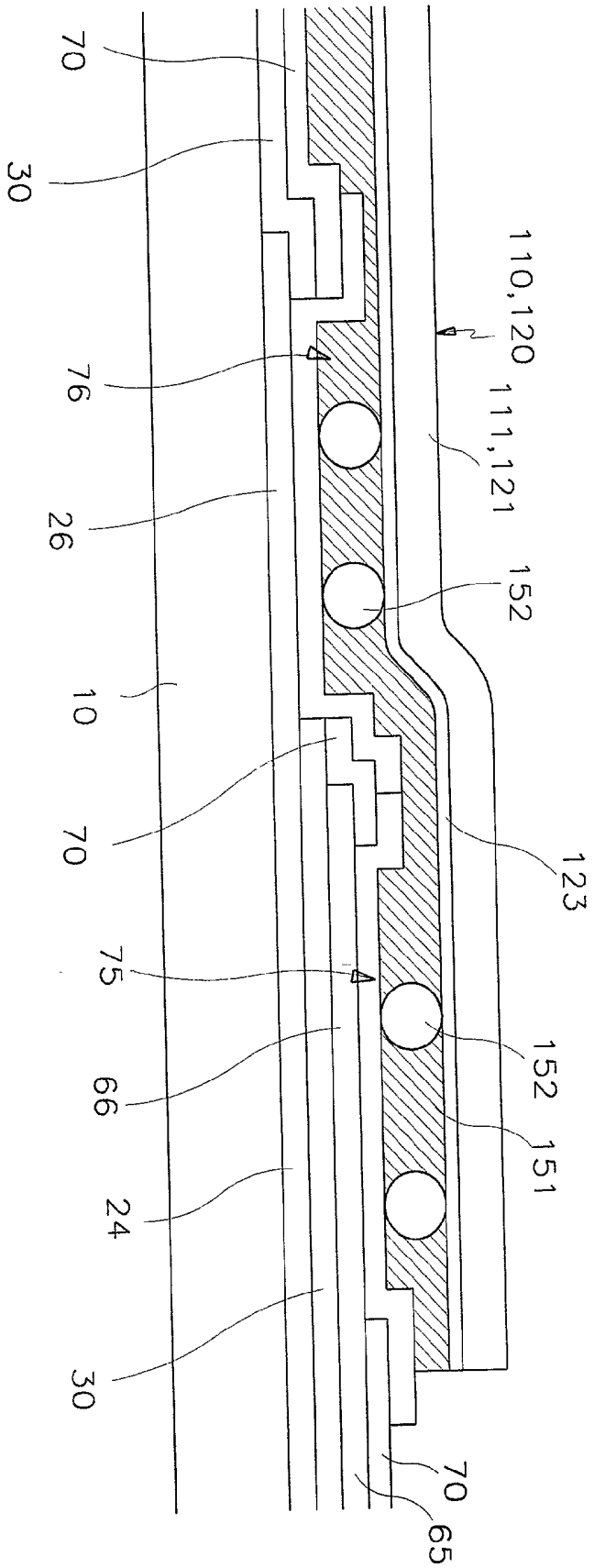


Fig.8b



LIQUID CRYSTAL DSPLAY

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to a liquid crystal display and a method for fabricating the same and, more particularly, to a liquid crystal display showing good performance characteristics.

[0003] (b) Description of the Related Art

[0004] A liquid crystal display is one of the flat panel displays that have been currently used in a most extensive manner. Such a liquid crystal display basically has two glass substrates with electrodes for generating electric fields, a liquid crystal layer sandwiched between the substrates, and polarizing plates externally attached to the substrates. When voltage is applied to the electrodes, the liquid crystal molecules are re-oriented to thereby control light transmission.

[0005] One of the substrates is provided with an array of thin film transistors (TFTs) for switching voltages applied to the electrodes.

[0006] The TFT array substrate has a plurality of gate and data lines proceeding in the horizontal and vertical directions, respectively. The data lines cross over the gate lines to thereby define pixel areas, and pixel electrodes are formed at the pixel areas. The TFTs control picture signals transmitted thereto through the data lines in accordance with scanning signals transmitted thereto through the gate lines, and sends the picture signals to the pixel electrodes. The display area may be outlined by the set of the pixel areas surrounded by the wiring lines. A plurality of gate and data pads are formed at the TFT array substrate external to the display area while being connected to the gate and data lines. The gate and data pads are directly connected to external driving ICs to receive scanning signals and picture signals from the outside, and transmit the singals to the relevant signal lines.

[0007] A gate printed circuit board, and a data printed circuit board are provided external to the TFT array substrate to transmit relevant signals thereto. A data singal transmission film interconnects the TFT array substrate with the data printed circuit board, and a data driving IC is mounted on the data signal transmission film to convert electrical signals into data signals, and send the data signals to the data pads and the data lines. Furthermore, gate signal transmission films connect the TFT array substrate with the gate printed circuit board, and gate driving ICs are mounted on the gate signal transmission films to convert electrical signals into gate signals, and send the gate signals to the gate pads and the gate lines.

[0008] Gate signal pads, and data signal pads are aligned with the gate and data pads in a one to one correspondence, and connected thereto through thermal compression process using an anisotropic conductive film (ACF).

[0009] Meanwhile, the gate printed circuit board may be omitted. In this case, the data printed circuit board generates gate signals, and sends the signals to the gate singal transmission film. Gate signal wires for transmitting the gate signals are formed at the data signal transmission film connected to the data printed circuit board. Gate signal interconnection wires are formed at the TFT array substrate to connect the gate signal lines of the gate signal transmission films with the gate signal wires. The gate signal wires, and the gate signal interconnection wires are connected to each other to receive gate signals from the data printed circuit board, and transmit the signals to the gate driving ICs.

[0010] However, in the above structure, corrosion should not occur at both pad portions of the gate signal interconnection wires interconnecting the gate signal lines and the gate signal wires to obtain good contact characteristics, and the thermal compression process using the ACF should be performed in a stable manner.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to provide a liquid crystal display which involves good contact characteristics.

[0012] It is another object of the present invention to provide a liquid crystal display where gate signal interconnection pads are covered by leads of gate and data signal transmission films, or stepped difference at the contact poritons is minimized.

[0013] These and other objects may be achieved by a liquid crystal display with an insulating substrate. The substrate is overlaied with a plurality of gate lines, and a plurality of data lines crossing over the gate lines to define pixel areas. A gate signal interconnection line assembly is formed at the substrate. The gate signal interconnection line assembly is provided with gate signal interconnection lines, and first and second gate signal interconnection pads connected to both ends of the gate signal interconnection lines to relay gate electrical signals to the gate lines. Insulating layers are formed on the substrate while bearing first and second contact holes exposing the first and second gate signal interconnection pads. Gate signal transmission films are attached to the substrate while each mounting a gate driving integrated circuit thereon to receive gate electrical signals and send gate signals to the gate lines. Each gate transmission film has first gate signal wires, and first gate signal leads connected to the first gate signal interconnection pads through the first contact holes. Data signal transmission films are attached to the substrate with second gate signal wires, and second gate signal leads connected to the second gate signal interconnection pads through the second contact holes. The first or the second gate signal lead completely covers the first or the second contact hole at least in the longitudinal direction of the lead.

[0014] The liquid crystal display further includes a printed circuit board connected to the data signal transmission films to send the gate and data electrical signals to the gate driving integrated circuits and the data driving integrated circuit.

[0015] Pixel electrodes are formed on the insulating layer at the pixel areas. First and second subsidiary gate signal interconnection pads are formed at the same plane as the pixel electrodes while covering the first and second contact holes. The first and second subsidiary gate signal interconnection pads are positioned between the first and second gate signal interconnection pads and the first and second gate signal leads, respectively.

[0016] The insulating layers are formed with a gate insulating layer covering the gate lines, and a protective layer covering the data lines over the gate insulating layer. The

first or the second gate signal lead completely covers at least one side of each contact hole in the longitudinal direction. The gate signal interconnection line assembly may be formed at the same plane as the gate lines or the data lines, and provided with first gate signal interconnection lines placed at the same plane as the gate lines, and second gate signal interconnection lines placed at the same plane as the data lines. The first and the second gate signal interconnection lines are connected to each other via the first and second subsidiary gate signal interconnection pads.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

[0018] **FIG. 1** is a plan view of a TFT array substrate for a liquid crystal display according to a first preferred embodiment of the present invention;

[0019] **FIG. 2** is a partial amplified view of the TFT array substrate shown in **FIG. 1** where the pixel area and the pad area are illustrated;

[0020] **FIGS. 3 and 4** are partial amplified views of the TFT array substrate shown in **FIG. 1** where gate signal wiring structures and contact or pad portions are specifically illustrated;

[0021] **FIG. 5** is a cross sectional view of the TFT array substrate taken along the V-V' line of **FIG. 2**;

[0022] **FIG. 6** is a cross sectional view of the TFT array substrate taken along the VI-VI' line of **FIG. 3** or **4**;

[0023] **FIGS. 7A and 7B** are plan views of a TFT array substrate for a liquid crystal display according to a second preferred embodiment where a gate signal interconnection wire is illustrated; and

[0024] **FIGS. 8A and 8B** are plan views of a TFT array substrate for a liquid crystal display according to a third preferred embodiment where a gate signal interconnection wire is illustrated.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

[0026] **FIG. 1** schematically illustrates a TFT array substrate for a liquid crystal display according to a first preferred embodiment of the present invention.

[0027] As shown in **FIG. 1, a** plurality of gate lines **21** are formed on an insulating substrate **10** in the horizontal direction, and a plurality of data lines **61** proceed in the vertical direction while being electrically insulated from the gate lines **21**.

[0028] The data lines **61** cross over the gate lines **21** to thereby define pixel areas P, and the pixel areas P collectively form a display area D. A thin film transistor TFT is formed at each pixel area P while being connected to the gate lines **21** and the data lines **61**. A pixel electrode PE is also provided at each pixel area while being connected to the TFT. A black matrix **11** is formed at the substrate **10** outside the display area D to preventlight leakage.

[0029] A printed circuit board **100** is positioned outside of the substrate **10** in the horizontal direction to output gate and data electrical signals for driving the device. The printed circuit board **100**, and the substrate **10** are electrically connected to each other via data signal transmission films **110**. A data driving IC **130** is mounted on each data signal transmission film **110** to provide picture signals. The data signal transmission film **110** is also provided with a plurality of data signal lines **114**, and a plurality of first gate signal wires **115**. The data signal lines **114** are connected to the data lines **61** at contact portions C**2** to relay the picture signals issued from the data driving IC **130** to the data lines **61**.

[0030] A plurality of gate signal transmission films **120** are arranged at the left side of the substrate **10** in the vertical direction while being electrically connected thereto. A gate driving IC **140** is mounted on each gate signal transmission film **120** to issue scanning signals or gate signals. Each gate signal transmission film **120** is also provided with a plurality of second gate signal wires **124**, and gate signal lines **126** connected to the gate lines **21** at connection or contact portions C**1** to relay the gate signals issued from the gate driving IC **140** to the gate lines **21**.

[0031] Gate signal interconnection wires **134** are arranged at the left top corner portion of the substrate **10** external to the display area D. The gate signal interconnection wires **134** connect the first gate signal wires **115** of the data signal transmission film **110** with the second gate signal wires **124** of the gate signal transmission film **120** at contact portions C**4** and C**3**.

[0032] Third gate signal wires **136** are formed at the left side of the substrate **10** external to the display area D. The third gate signal wires **136** interconnect the second gate signal wires **124** of the neighboring gate signal transmission films **120** at the contact or pad portions C**5** and C**6**.

[0033] The substrate **10**, and the plurality of signal lines or wires **114**, **115**, **61**, **134**, **124**, **126** and **136** are provided with pads at the pad or contact portions C**1** through C**6**, and connected to each other via the pads using an anisotropic conductive film.

[0034] In the above-structured liquid crystal display, the gate electrical signals issued from the printed circuit board **100** are transmitted to the gate signal interconnection wires **134** via the first gate signal wires **115**. The gate electrical signals are then sent to the gate driving IC **140** via the second gate signal wires **124**, or transmitted to the third gate signal wires **136**. Thereafter, the gate electrical signals are partially converted into gate signals at the gate driving IC **140**, and the gate signals are sent to the gate lines **21** through the gate signal lines **126**. That is, the gate electrical signals issued from the printed circuit board **100** are partially sent to the gate lines **21** via the first to third gate signal wires **115**, **124** and **136**, and the gate signal interconnection wires **134**.

[0035] Meanwhile, in addition to the data signal transmission films **110**, separate signal transmission films may be provided to connect the printed circuit board **100** to the substrate **10**. In this structure, the first gate signal wires **115** would be formed at the separate signal transmission films.

[0036] The main structure of the TFT array substrate according to the first preferred embodiment will be now described with reference to FIGS. **2** to **6**.

[0037] **FIG. 2** is a partial amplified view of the TFT array substrate shown in **FIG. 1** where the pixel area P and the pad portions C1 and C2 are specifically illustrated. **FIGS. 3 and 4** are partial amplified views of the TFT array substrate shown in **FIG. 1** where the gate signal wiring structure and the contact or pad portions C3 and C4 are specifically illustrated. **FIG. 5** is a cross sectional view of the TFT array substrate taken along the V-V' line of **FIG. 2**, and **FIG. 6** is a cross sectional view of the TFT array substrate taken along the VI-VI' line of **FIG. 3** or **4**. Since the contact portions C3 and C4 bear the same structure, only one contact portion is illustrated in **FIG. 6**.

[0038] The pixel area P, the contact portions C1 to C4, and the gate signal interconnection wires **134** will be first introduced while omitting detailed description of the third gate signal wires **136**, and the contact portions C5 and C6 because they have the same structure as the gate signal interconnection wires **134**, and the contact portions C3 and C4.

[0039] As shown in **FIG. 2, a** gate line assembly is formed on the insulating substrate **10** at the same plane as the gate signal interconnection wires **134** with a metallic or conductive material such as Al or Al alloy, Mo or MoW alloy, Cr, and Ta.

[0040] The gate line assembly includes a plurality of gate lines **21**, gate electrodes **22** part of the gate lines **21**, and gate pads **23** connected to the end portions of the gate lines **21** to receive scanning signals from the outside and transmit them to the gate lines **21**. Each gate signal interconnection wire **134** is provided with a gate signal interconnection line **24**, and gate signal interconnection pads **26** connected to both ends of the gate signal interconnection line **24**.

[0041] The gate line assembly, and the gate signal interconnection wires **134** may have a single-layered structure, or a multiple-layered structure. In the case of a double-layered structure, one layer is formed with a material bearing a lower resistance, and the other layer is formed with a material bearing good contact characteristics with other materials. For example, the double-layered structure may be formed with a chrome-based layer and an aluminum alloy-based layer, or a molybdenum or molybdenum-based layer and an aluminum-based layer.

[0042] A gate insulating layer **30** is formed on the substrate **10** with silicon nitride while covering the gate line assembly and the gate signal interconnection wires **134**.

[0043] A semiconductor pattern **41** is formed on the gate insulating layer **30** over each gate electrode **22** with amorphous silicon. Ohmic contact patterns **52** and **53** are formed on the semiconductor pattern **41** with amorphous silicon doped with n-type impurities such as P, and separated from each other around the gate electrode **22**.

[0044] A data line assembly is formed on the ohmic contact patterns **52** and **53**, and the gate insulating layer **30** with a metallic or conductive material such as Al or Al alloy, Mo or MoW alloy, Cr, and Ta.

[0045] The data line assembly includes a plurality of data lines **61**, source electrodes **62** branched from the data lines **61**, drain electrodes **63** separated from the source electrodes **62** while interposing the gate electrodes **21** between them, and data pads **64** connected to the data lines **61** to receive picture signals from the outside and transmit them to the data lines **61**.

[0046] The data line assembly may have a single-layered structure, or a multiple-layered structure. In the case of a double-layered structure, one layer is formed with a material bearing a lower resistance, and the other layer is formed with a material bearing good contact characteristics with other materials.

[0047] Each TFT is formed with the gate electrode **22**, the semiconductor pattern **41**, and source and drain electrodes **62** and **63**.

[0048] A protective layer **70** is formed on the data line assembly and the gate insulating layer **30** exposed through the data line assembly with silicon nitride or organic insulating material. The protective layer **70** has contact holes **73** exposing the gate pads **23** together with the gate insulating layer **30** at the contact portions C1, contact holes **74** exposing the data pads **64** at the contact portions C2, and contact holes **72** exposing the drain electrodes **63** at the pixel areas P. Furthermore, the protective layer **70** further has contact holes **76** exposing the gate signal interconnection pads **26** together with the gate insulating layer **30** at the contact portions C3 and C4.

[0049] Pixel electrodes **80**, subsidiary gate pads **83**, subsidiary data pads **84**, and subsidiary gate signal interconnection pads **86** are formed on the protective layer **70** with a transparent conductive material such as indium tin oxide (ITO), or indium zinc oxide (IZO).

[0050] The pixel electrodes **80** are connected to the drain electrodes **63** through the contact holes **72** to receive picture signals. The subsidiary gate and data pads **83** and **84** are connected to the gate and data pads **64** through the contact holes **73** and **74** to protect them, and enhance adhesion thereof to external circuits.

[0051] The subsidiary gate signal interconnection pads **86** are connected to the gate signal interconnection pads **26** through the contact holes **76**.

[0052] In the meantime, the gate signal transmission film **120** has gate signal leads **122** overlaid with an insulating resin layer **121**. Each gate signal lead **122** is physico-electrically connected to the subsidiary gate pad **83** via an anisotropic conductive film **151**, with conductive particles **152** and adhesives **151**. The gate signal lead **122** completely covers the contact hole **73** in the longitudinal direction as well as in the direction of width. The gate signal lead **122** may or may not completely cover the contact hole **73** or the subsidiary gate pad **83**.

[0053] The data signal transmission film **110** has a data signal lead **112** overlaid with an insulating resin layer **111**. The data signal lead **122** is physico-electrically connected to the subsidiary data pad **84** via an anisotropic conductive film with conductive particles **152** and adhesives **151**. The data signal lead **112** may or may not completely cover the contact hole **74** or the subsidiary data pad **84**.

[0054] In the gate and data signal transmission films **110** and **120** at the contact portions C3 and C4, gate signal interconnection leads **123** are formed under the insulating

resin layers **111** and **121**. The gate signal interconnection leads **123** are connected to the subsidiary gate signal interconnection pads **86** via an anisotropic conductive film with conductive particles **152** and adhesives **151**, thereby electrically interconnecting the first and second gate signal wires **115** and **124**. The gate signal interconnection lead **123** completely covers the contact hole **76** of the protective layer **70** and the gate insulating layer **30** in the longitudinal direction as well as in the direction of width. As shown in **FIG. 4**, the gate signal interconnection lead **123** may cover at least one longitudinal side of the contact hole **76** or the subsidiary gate signal pad **86**. The gate signal interconnection lead **123** may or may not completely cover the subsidiary gate signal pad **86**.

[**0055**] In the above structure, the gate signal interconnection leads **123** or the anisotropic conductive films of the gate and data signal transmission films **110** and **120** completely cover the contact hole **76** over the subsidiary gate signal interconnection pads **86** so that corrosion does not occur at the pad portions C**3** and C**4**, and adhesion can be strengthened at those portions.

[**0056**] In order to further enhance contact characteristics at the contact portions C**3** and C**4**, it may be controlled that stepped difference at the contact hole **86** should be minimized. For this purpose, the interconnection line of the gate signal interconnection wire **134** may be formed at the same plane as the data line assembly.

[**0057**] **FIGS. 7A and 7B** illustrate the wiring structure of a TFT array substrate according to a second preferred embodiment of the present invention.

[**0058**] In this preferred embodiment, other components and structures of the TFT array substrate are the same as those related to the first preferred embodiment except that gate signal interconnection lines **65** and gate signal interconnection pads **66** of the gate signal interconnection wires **134** are placed at the same plane as the data line assembly on the gate insulating layer **30**, and contact holes **75** exposing the gate signal interconnection pads **66** are only formed at the protective layer **70**. The contact holes **75** are preferably formed to be smaller than the gate signal interconnection pads **66**.

[**0059**] **FIGS. 8A and 8B** illustrate the wiring structure of a TFT array substrate according to a third preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the TFT array substrate are the same as those related to the first preferred embodiment except for the following features.

[**0060**] As shown in **FIGS. 8A and 8B**, each gate signal interconnection wire **134** has double-structured gate signal interconnection lines **24** and **65** with gate signal interconnection pads **26** and **66** that are placed at the same plane as the gate line assembly and the data line assembly, respectively. The gate insulating layer **30** and the protective layer **70** together have contact holes **76** exposing the gate signal interconnection pads **26**, and the protective layer **70** only has contact holes **75** exposing the gate signal interconnection pads **66**. The subsidiary gate signal interconnection pads **86** are connected to the gate signal interconnection pads **26** and **66** through the contact holes **75** and **76**, thereby electrophysically interconnecting the gate signal interconnection lines **24** and **65**. In this structure, the contact failure due to the stepped difference is reduced while compensating for short circuits of the gate signal interconnection lines **24** and **65** and minimizing the wiring resistance. The overlying gate signal interconnection pads **66** may be extended toward the underlying gate signal interconnection pads **66**. In this case, the aforementioned effects can be obtained, and further, it can be prevented that the moisture content is introduced into the pad portions C**3** and C**4**.

[**0061**] The reinforcement of the pad portions C**3** and C**4** based on the double-structured pads **26** and **66** may be applied to other pad portions C**1**, C**2**, C**5** and C**6** in the same manner. The structures illustrated in **FIGS. 7A** to **8**B may be selectively applied to the plurality of gate signal interconnection wires **134**.

[**0062**] A method for fabricating a TFT array substrate will be now described with reference to FIGS. **2** to **8**B.

[**0063**] A conductive layer is formed on an insulating substrate **10**, and patterned to form a gate line assembly **21**, **22** and **23**, and a gate signal interconnection line assembly **24** and **26**. Then, a gate insulating layer **30**, an amorphous silicon-based layer, and a doped amorphous silicon-based layer are sequentially deposited onto the substrate **10**. The amorphous silicon-based layer, and the doped amorphous silicon-based layer are patterned to thereby form a semiconductor pattern **41** and an ohmic contact pattern **51** over each gate electrode **22**. At this time, the semiconductor pattern may be left over the gate signal interconnection line **24**. Thereafter, a conductive layer is deposited, and patterned to thereby form a data line assembly **61** to **64**. At this time, as shown in **FIGS. 7A** to **8**B, a gate signal interconnection assembly **65** and **66** may be formed together at the same plane as the data line assembly **61** to **64**. The portion of the ohmic contact pattern **51** exposed between the source and drain electrodes **62** and **63** is removed, thereby separating it into two patterns **52** and **53** while exposing the semiconductor pattern **41**. A protective layer **70** is deposited onto the substrate **10**, and patterned to thereby form contact holes **72** to **76**. Thereafter, a transparent conductive material is deposited, and patterned to thereby form pixel electrodes **80**, subsidiary gate pads **83**, subsidiary data pads **84**, and subsidiary gate signal interconnection pads **86**.

[**0064**] Although the semiconductor pattern **41**, and the data line assembly **61** to **64** are formed through different processing steps, they may be formed through one etching process. In such a process, a mask partially differentiated in light transmission is used to form photoresist patterns having different thickness. The semiconductor layer **41**, and the data line assembly **61** to **64** are patterned together using the above mask as etching mask. In the patterning process, the photoresist pattern of a middle thickness is positioned over the channel portion between the source and drain electrodes **62** and **63**, and the photoresist pattern with a large thickness positioned over the area where the data line assembly **61** to **64** are formed. In the resulting structure, ohmic contact patterns and semiconductor patterns are formed under the data line assembly **61** through **64**, and the gate signal interconnection line assembly **65** and **66**. The ohmic contact patterns **52** and **53** are formed along the shape of the data line assembly **61** to **64**, and the gate signal interconnection line assembly **65** and **66**. The semiconductor pattern **41** is also formed along the shape of the data line assembly **61** to

64, and the gate signal interconnection line assembly **65** and **66** except for the channel portion between the source and drain electrodes **62** and **63**.

[**0065**] As described above, the contact portions are covered by leads, and the stepped difference at the contact portions is minimized. The gate signal interconnection line assembly is established to have a double-lined structure. This prevents short circuits of the wiring lines while keeping a moisture-free state, thereby obtaining good contact characteristics.

[**0066**] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A liquid crystal display, comprising:

an insulating substrate having a plurality of gate lines, a plurality of data lines crossing over the gate lines to define pixel areas, a gate signal interconnection line assembly with gate signal interconnection lines and first and second gate signal interconnection pads connected to both ends of the gate signal interconnection lines to relay gate electrical signals to the gate lines, and insulating layers with first and second contact holes exposing the first and second gate signal interconnection pads;

gate signal transmission films attached to the substrate while each mounting a gate driving integrated circuit thereon to receive gate electrical signals and send gate signals to the gate lines, each gate transmission film having first gate signal wires, and first gate signal leads connected to the first gate signal interconnection pads through the first contact holes; and

signal transmission films attached to the substrate with second gate signal wires, and second gate signal leads connected to the second gate signal interconnection pads through the second contact holes;

wherein the first or the second gate signal lead completely covers the first or the second contact hole at least in the longitudinal direction of the lead.

2. The liquid crystal display of claim 1, further comprising pixel electrodes formed on the insulating layer at the pixel areas.

3. The liquid crystal display of claim 2, further comprising first and second subsidiary gate signal interconnection pads formed at the same plane as the pixel electrodes while covering the first and second contact holes, the first and second subsidiary gate signal interconnection pads positioned between the first and second gate signal interconnection pads and the first and second gate signal leads, respectively.

4. The liquid crystal display of claim 1, wherein the insulating layers comprise a gate insulating layer covering the gate lines, and a protective layer covering the data lines over the gate insulating layer.

5. The liquid crystal display of claim 1, wherein the first or the second gate signal lead completely covers at least one side of each contact hole in the longitudinal direction.

6. The liquid crystal display of claim 4, wherein the gate signal interconnection line assembly is formed at the same plane as the gate lines, and the first and second contact holes are formed at both of the gate insulating layer and the protective layer.

7. The liquid crystal display of claim 4, wherein the gate signal interconnection line assembly is formed at the same plane as the data lines, and the first and second contact holes are formed only at the protective layer.

8. The liquid crystal display of claim 3, wherein the gate signal interconnection line assembly comprises first gate signal interconnection lines formed at the same plane as the gate lines, and second gate signal interconnection lines formed at the same plane as the data lines.

9. The liquid crystal display of claim 8, wherein the first and the second gate signal interconnection lines are connected to each other via the first and second subsidiary gate signal interconnection pads.

10. The liquid crystal display of claim 1, wherein the signal transmission films are data signal transmission films each mounted with a data driving integrated circuit to receive data electrical signals and send data signals to the data lines.

11. The liquid crystal display of claim 10, further comprising a printed circuit board connected to the data signal transmission films to send the gate and data electrical signals to the gate driving integrated circuits and the data driving integrated circuit.

12. A liquid crystal display, comprising:

an insulating substrate having a plurality of gate lines, a plurality of data lines crossing over the gate lines to define pixel areas, a gate signal interconnection line assembly with gate signal interconnection lines and first and second gate signal interconnection pads formed at both ends of the gate interconnection lines, and insulating layers with first and second contact holes exposing the first and second gate signal interconnection pads;

wherein the first and second gate signal interconnection pads are formed at the same plane as the data lines.

13. The liquid crystal display of claim 12, further comprising pixel electrodes formed on the insulating layer at the pixel areas.

14. The liquid crystal display of claim 13, further comprising first and second subsidiary gate signal interconnection pads formed at the same plane as the pixel electrodes while covering the first and second contact holes, the first and second subsidiary gate signal interconnection pads being positioned between the first and second gate signal interconnection pads and the first and second gate signal leads, respectively.

15. The liquid crystal display of claim 12, wherein the insulating layers comprise a gate insulating layer covering the gate lines, and a protective layer comprising the data lines over the gate insulating layer.

16. The liquid crystal display of claim 12, further comprising gate signal transmission films attached to the substrate while each mounting a gate driving integrated circuit to receive gate electrical signals and send gate signals to the gate lines, each gate signal transmission film having first gate signal wires, and first gate signal leads connected to the first gate signal interconnection pads through the first contact holes.

17. The liquid crystal display of claim 12, further comprising data signal transmission films attached to the substrate while each mounting a data driving integrated circuit to receive data electrical signals and send data signals to the data lines, the data signal transmission film having second gate signal wires, and second gate signal leads connected to the second gate signal interconnection pads through the second contact holes.

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专利名称(译)	液晶显示器		
公开(公告)号	US20020012079A1	公开(公告)日	2002-01-31
申请号	US09/901127	申请日	2001-07-10
[标]申请(专利权)人(译)	金东GYU 金相SOO 李相旭		
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IPC分类号	G02F1/1333 G02F1/13 G02F1/1343 G02F1/1345 G02F1/136 G02F1/1362 G09F9/30		
CPC分类号	G02F1/1345 G02F1/136286 G02F1/13458 G02F1/13452		
优先权	1020000043508 2000-07-27 KR		
其他公开文献	US6636288		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示器包括绝缘基板，形成在基板上以限定像素区域的栅极和数据线，或者统称为显示区域。栅极信号互连线形成在显示区域外部的基板的拐角部分处以传输栅极电信号，并且设置有栅极信号互连线以及连接到栅极信号互连线的两端的第一和第二栅极信号互连焊盘。栅极绝缘层和保护层还形成在基板上，并设置有暴露第一和第二栅极信号互连焊盘的第一和第二接触孔。栅极和数据信号传输膜附着在基板上，并设有第一和第二栅极信号引线以及第一和第二栅极信号线。第一和第二栅极信号引线通过第一和第二接触孔连接到第一和第二栅极信号互连焊盘。第一或第二栅极信号引线至少在引线的纵向方向上完全覆盖第一或第二接触孔。