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**Lai**

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(54) **LIQUID CRYSTAL DISPLAYS**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] ..... **G02F 1/1343**
(52) **U.S. Cl.** ..... **349/139**; 349/143
(58) **Field of Search** ..... 349/139–143

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,063,653 A 5/2000 Lin et al. ..... 438/160
6,429,909 B1 * 8/2002 Kim et al. ..... 349/54
2002/0191124 A1 * 12/2002 Nakata ..... 349/43
2003/0122983 A1 * 7/2003 Kim et al. ..... 349/43

* cited by examiner

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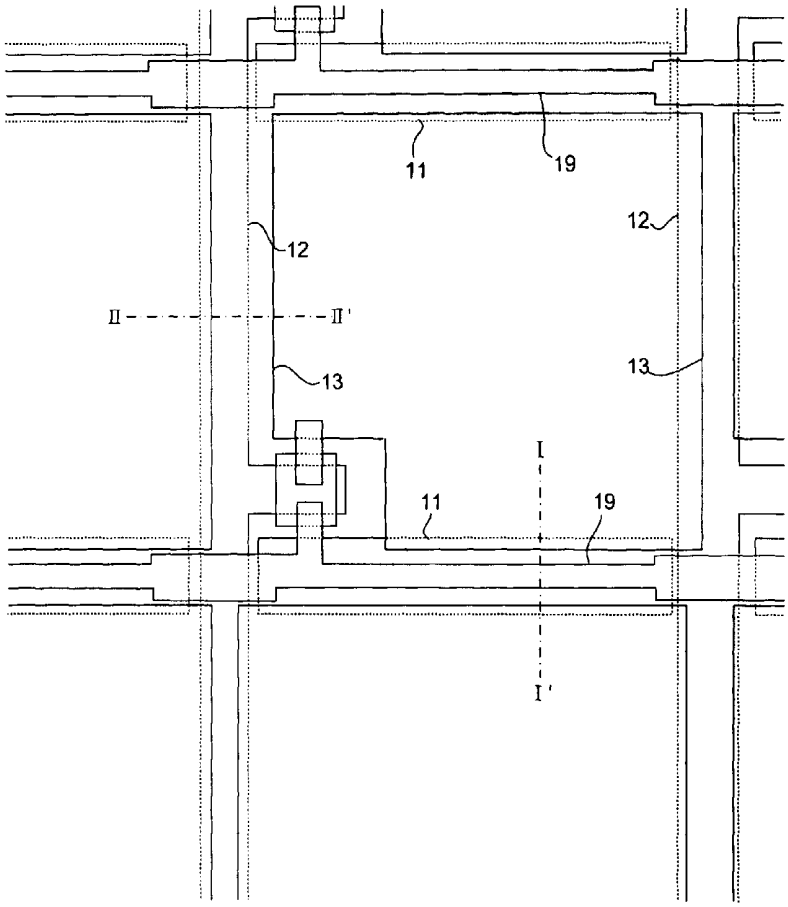
(57) **ABSTRACT**

The present invention provides a liquid crystal display including a substrate, a first gate line, a second gate line, an insulation layer, a data line, a passivation layer, a low dielectric constant layer, and a pixel electrode. The first gate line intersects with and is insulated from the second gate line. The pixel electrode overlaps a portion of the first gate line and a portion of the second gate line. The data line overlaps a portion of the first gate line. The portion of the first gate line overlapped by the pixel electrode is different from the portion of the first gate line overlapped by the data line. Therefore, the capacitance effect between the pixel electrode and the data line is reduced.

**17 Claims, 6 Drawing Sheets**



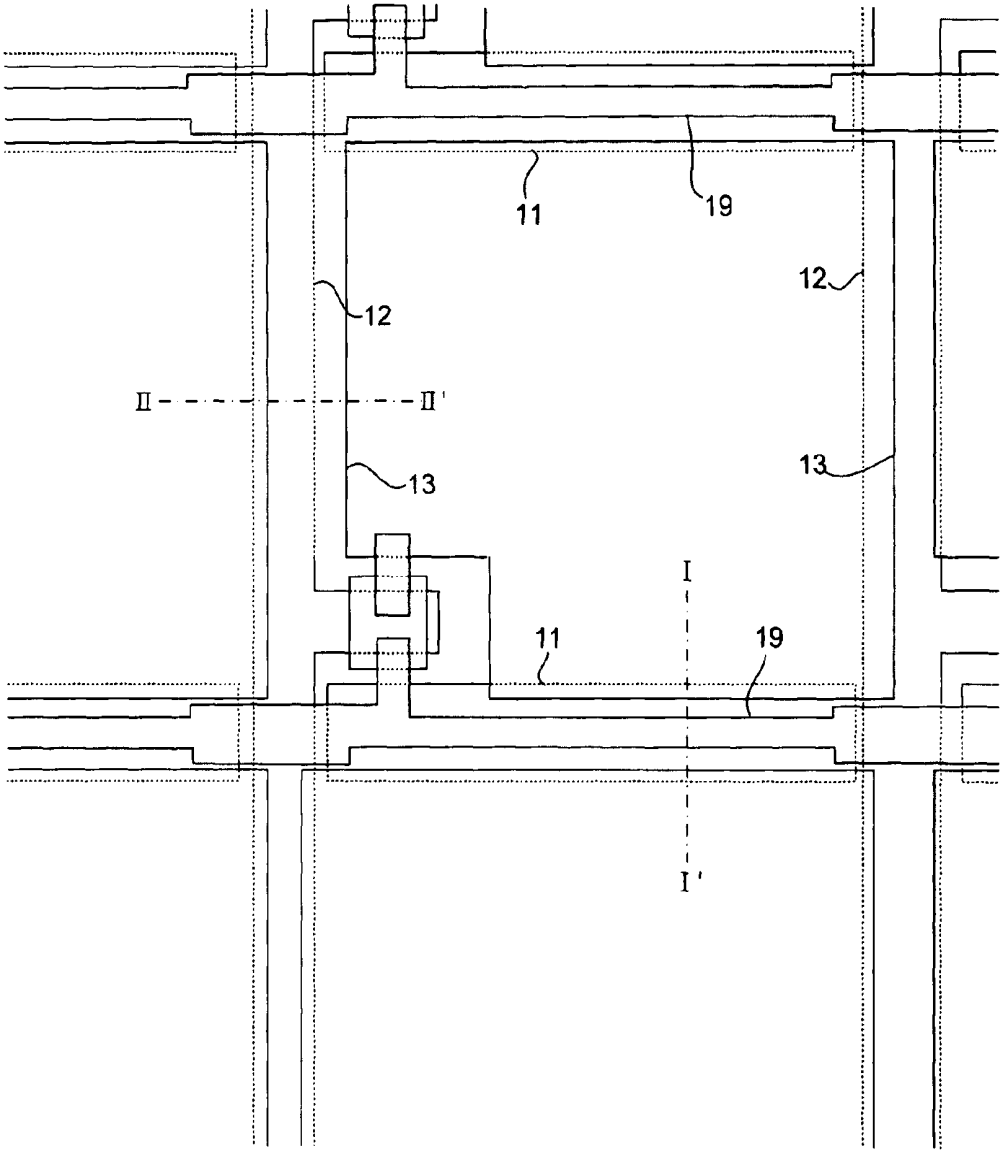



Fig.1a

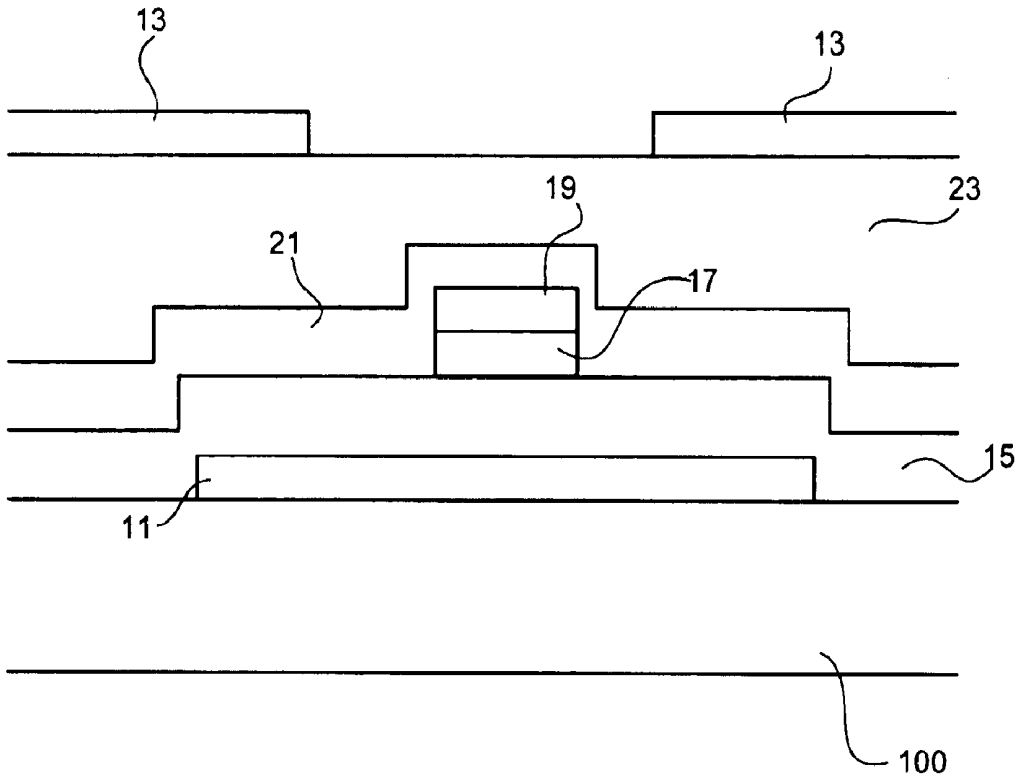



Fig.1b

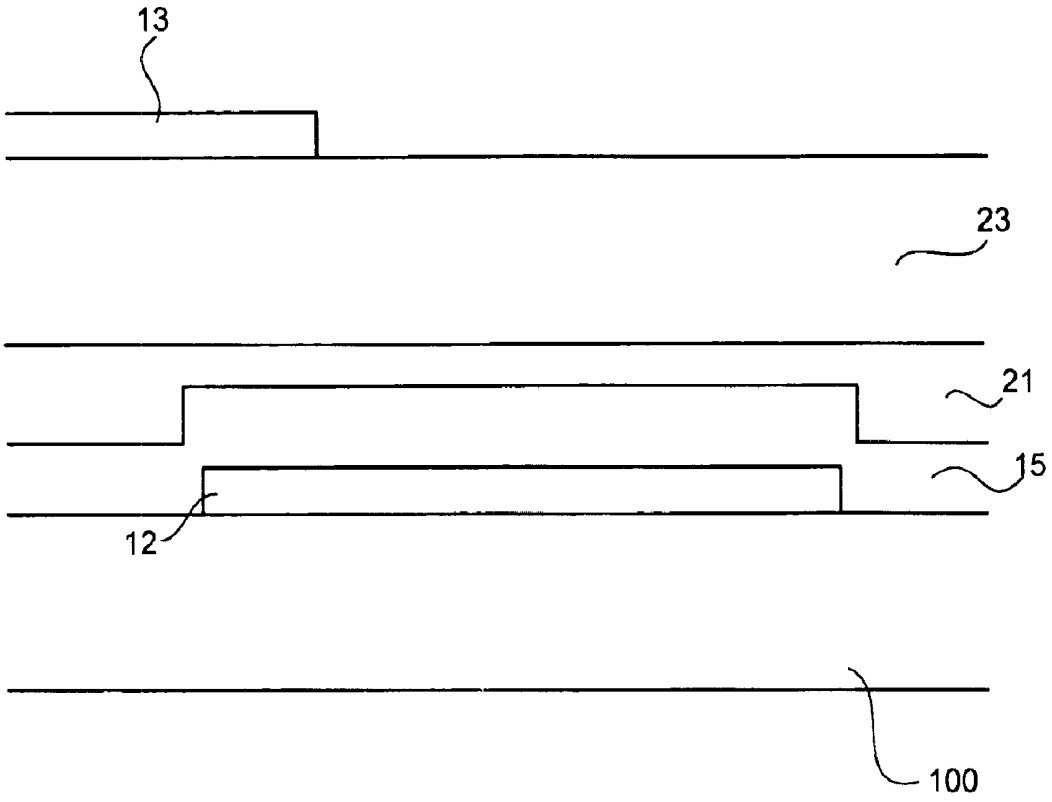



Fig.1c

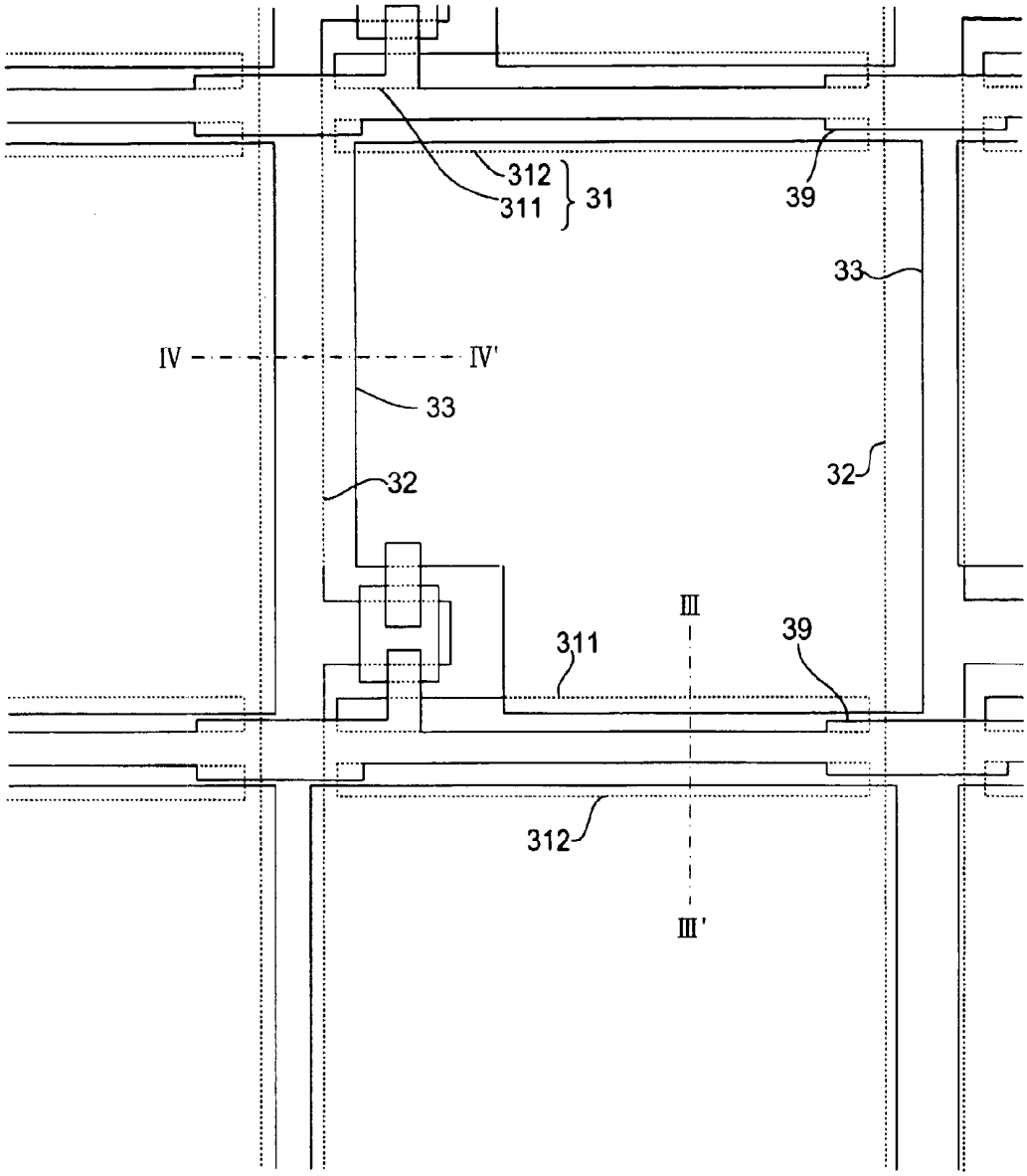



Fig.2a

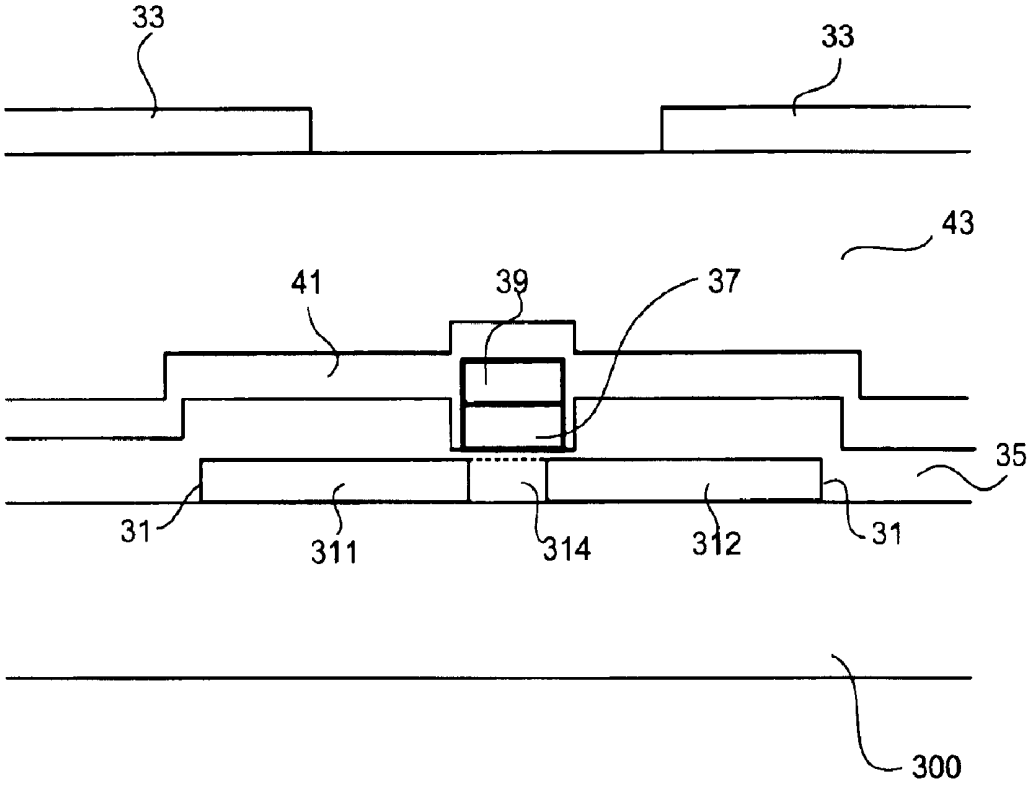



Fig.2b

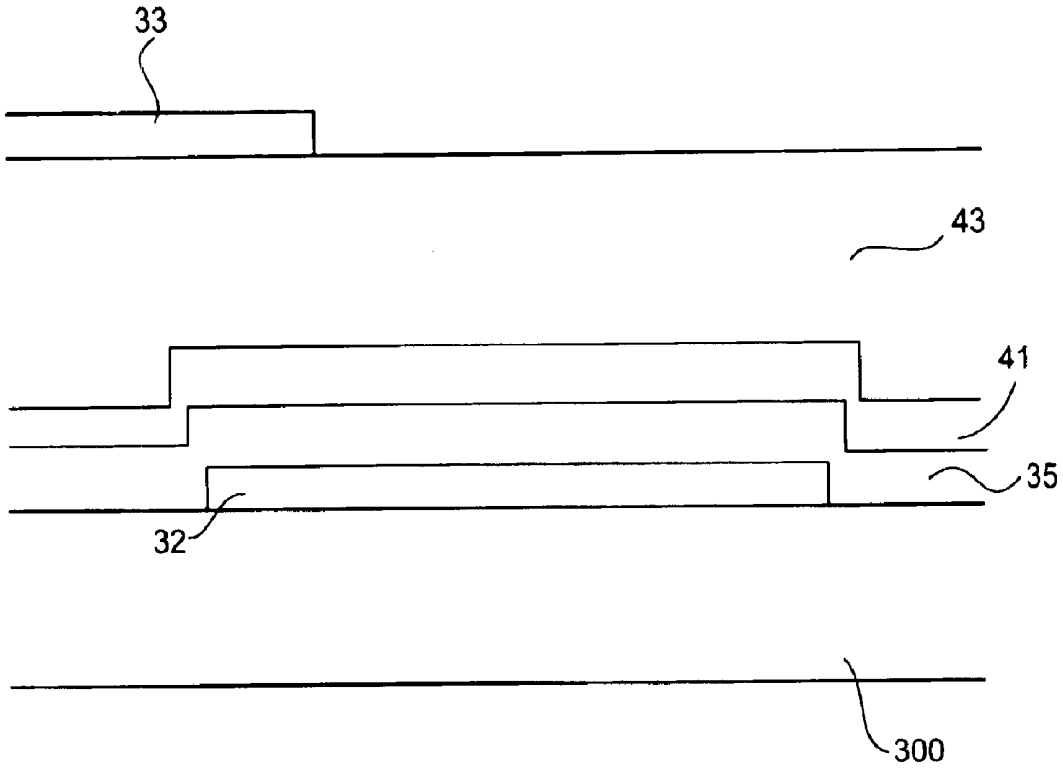



Fig.2c

# LIQUID CRYSTAL DISPLAYS

## CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority of Taiwan Patent Application Serial No. 091124962 filed on Oct. 25, 2002.

## FIELD OF INVENTION

The present invention relates to an LCD (Liquid Crystal Display) and its method of manufacture.

## BACKGROUND OF THE INVENTION

Compared with a CRT (cathode ray tube) display, the LCD has the advantages of less weight, smaller volume, and lower radiation. Hence, we can expect that the LCD will substitute the CRT display as popular display in the future.

Conventional LCDs include a liquid crystal panel and a back light device. The liquid crystal panel includes a top substrate, a bottom substrate and a liquid crystal layer formed between the top substrate and the bottom substrate. The top substrate has a CF (Color Filter). The bottom substrate has a TFT (thin film transistor). Beside, a top polarizer is disposed on the top substrate and a bottom polarizer is disposed between the bottom polarizer and the back light device.

A Black Matrix may be plated on a CF to increase contrast and prevent mixture of colors and leakage of light. Hence, the LCD is better than the CRT display in resolution. However, if the resolution is enhanced without narrowing the pitch of the pixels, the aperture ratio of pixels will be reduced and the brightness of the LCD will decrease. Hence, narrowing of the Black Matrix or other alternatives to improve the brightness is an important issue.

## SUMMARY OF THE INVENTION

One aspect of the present invention is to provide an LCD with better aperture ratio and a method for manufacturing the LCD.

Another aspect of the present invention is to reduce the disconnection caused by a signal line.

Still another aspect of the present invention is to avoid the light leakage of the LCD.

The other aspect of the present invention is to reduce the capacitance effect between a signal line and a pixel electrode.

In the present invention, a first gate line and a second gate are formed on a substrate. The first gate line and the second gate line are insulated from each other and are non-parallel to each other. After that, an insulation layer, a semiconductor layer, a data line, a passivation layer, a low dielectric constant layer and a pixel electrode are formed sequentially. The data line overlaps the first gate line. A dielectric constant layer is a low dielectric constant layer. The pixel electrode overlaps with a portion of the first gate line and a portion of the second gate line. The data line overlaps with a portion of the first gate line. The portion of the first gate line overlapped by the pixel electrode is different from the portion of the first gate line overlapped by the data line. Therefore, the capacitance effect between the pixel electrode and the data line is avoided. In the second embodiment of the present invention, another kind of LCD is disclosed. The first gate line is replaced by a gate line including a pair of gate lines that are parallel to each other and separated by a gap.



The advantages and spirit of the present invention may be further comprehended through the following detailed description and drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. **1***a* is a schematic diagram of the first embodiment of the present invention;

FIG. **1***b* is a cross-sectional diagram along the line I–I' of FIG. **1***a;*

FIG. **1***c* is a cross-sectional diagram along the line II–II' of FIG. **1***a;*

FIG. **2***a* is a schematic diagram of the second embodiment of the present invention;

FIG. **2***b* is a cross-sectional diagram along the line III–III' in FIG. **2***a;*

FIG. **2***c* is a cross-sectional diagram along the line IV–IV' of FIG. **2***a.*

## DETAILED DESCRIPTION

FIG. **1***a* is a schematic diagram of the first embodiment of the present invention. The LCD of the present invention includes a plurality of first gate lines **11**, a plurality of second gate lines **12**, a plurality of data lines **19** and a plurality of pixel electrodes **13**. Only one of the pixels is illustrated in FIG. **1***a*. The first gate line **11** and the second gate line **12** are insulated from each other and are non-parallel to each other. The data line **19** overlaps a portion of the first gate line **11**. The pixel electrode **13** also overlaps a portion of the first gate line **11** and a portion of the second gate line **12**. However, in the first gate line **11**, the overlapping portion of the data line **19** is different from the overlapping portion of the pixel electrode **13**.

FIG. **1***b* is a cross-sectional diagram along the line I–I'of FIG. **1***a*. On a substrate, such as a glass substrate, the first gate line **11**, an insulation layer **15**, a semiconductor layer **17**, a data line **19**, a passivation layer **21**, a low dielectric constant layer **23** and a pixel electrode **13** are formed sequentially. Obviously, the portion that the data line **19** overlapping the first gate line **11** is different from the portion of the pixel electrode **13** overlapping the first gate line **11**.

FIG. **1***c* is a cross-sectional diagram along the line II–II' of FIG. **1***a*. In the present invention, the second gate line **12** and the insulation layer **15** are formed sequentially on the substrate **100**. Thus, after the semiconductor layer **17** and the data line **19** are formed as illustrated in FIG. **1***b,* the passivation layer **21**, the low dielectric constant layer **23** and the pixel electrode **13** are formed sequentially. As shown in FIG. **1***c,* the pixel electrode **13** overlaps a portion of the second gate line **12**.

In the present invention, the material of the insulation layer **15** includes an $Si_3N_4$ layer depositing above the first gate line **11**, the second gate line **12** and the substrate **100**. The material of the semiconductor layer **17** includes an undoped Si amorphous layer and a doped Si amorphous layer. The material of passivation layer **21** includes $Si_3N_4$. The low dielectric constant layer **23** is a transparent material with low dielectric constant, such as the acrylic. The material of the pixel electrode **13** includes ITO (Indium Tin Oxide).

FIG. **2***a* is a schematic diagram of the second embodiment of the present invention. In the present invention, an LCD

includes a plurality of gate line pairs **31**, a plurality of gate lines **32**, a plurality of data lines **39** and a plurality of pixel electrodes **33**. Only one pixel is illustrated in FIG. **2***a*. The gate line pair **31** and the gate line **32** are insulated from each other and are non-parallel to each other. The gate line pair **31** includes a first gate line **311** and a second gate line **312**. The first gate line **311** parallels the second gate line **312** with a gap **314** therebetween. The data line **39** overlaps a portion of the gate line pair **31** and the gap **314**. Besides, the pixel electrode **33** also overlaps a portion of the gate line pair **31**. However, in the gate line pair **31**, the overlapping portion of the data line **39** is different from the overlapping portion of the pixel electrode **33**. Likewise, the pixel electrode **33** also overlaps a portion of the gate line **32**.

In the second embodiment, as shown in FIG. **2***a*, the data line **39** overlaps the gap **314** of the gate line pair **31** and a portion of the gate line pair **31**. The pixel electrode **33** overlaps a portion of the second gate line **312**. The pixel electrode **33** overlaps a portion of the first gate line **311**.

FIG. **2***b* is a cross-sectional diagram along the line III–III'of FIG. **2***a*. On a substrate, such as a glass substrate, the gate line pair **31**, an insulation layer **35**, a semiconductor layer **37**, a data line **39**, a passivation layer **41**, a low dielectric constant layer **43** and a pixel electrode **33** are formed sequentially. Obviously, the portion that the data line **39** overlaps the gate line pair **31** is different from the portion of the pixel electrode **33** overlapping the gate line pair **31**.

FIG. **2***c* is a cross-sectional diagram along the line IV–IV' of FIG. **2***a*. In the present invention, the gate line **32** and the insulation layer **35** are formed sequentially on the substrate **300**. Thus, after the semiconductor layer **37** and the data line **39** are formed as illustrated in FIG. **2***b*, the passivation layer **41**, the low dielectric constant layer **43** and the pixel electrode **33** are formed sequentially. As shown in FIG. **2***c*, the pixel electrode **33** overlaps a portion of the gate line **32**.

In the present invention, the material of the insulation layer **35** includes an $Si_3N_4$ layer depositing above the gate line pair **31**, the gate line **32** and the substrate **300**. The material of the semiconductor layer **37** includes an undoped Si amorphous layer and a doped Si amorphous layer. The material of passivation layer **41** includes $Si_3N_4$. The low dielectric constant layer **43** is a transparent material with low dielectric constant, such as the acrylic. The material of the pixel electrode **33** includes ITO (Indium Tin Oxide).

The structure of an LCD proposed in the present invention may effectively increase the aperture ratio and avoid the leakage of light. Moreover, it may reduce the disconnection caused by a signal line to reduce the capacitance effect between a signal line and a pixel electrode.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention as claimed.

What is claimed is:

**1**. A liquid crystal display, comprising:

a substrate;

a first gate line, comprising a first portion and a second portion;

a second gate line, said first gate line and said second gate line being disposed on said substrate and being insulated from each other, said first gate line being non-parallel to said second gate line;

an insulation layer disposed above said first gate line and said second gate line;

a data line, said data line and said first portion overlapping, said insulation layer being disposed between said data line and said first portion; and

a pixel electrode disposed above said data line, said pixel electrode and said second portion overlapping.

**2**. The liquid crystal display according to claim **1**, wherein said first portion is different from said second portion.

**3**. The liquid crystal display according to claim **1**, wherein said pixel electrode and said second gate line overlap.

**4**. The liquid crystal display according to claim **1**, wherein said liquid crystal display further comprises a semiconductor layer disposed above said insulation layer, said semiconductor layer comprises an undoped amorphous silicon layer and a doped amorphous silicon layer.

**5**. The liquid crystal display according to claim **1**, wherein said liquid crystal display further comprises a passivation layer disposed above said data line.

**6**. The liquid crystal display according to claim **1**, wherein said liquid crystal display further comprises a low-dielectric-constant layer disposed above said passivation layer.

**7**. The liquid crystal display according to claim **1**, wherein said first gate line comprises a pair of gate lines, said pair of gate lines are parallel to each other and separated by a gap.

**8**. The liquid crystal display according to claim **7**, wherein said data line, said gap and a part of said pair of gate lines overlap.

**9**. A liquid crystal display, comprising:

a substrate;

a first gate line, comprising a first portion and a second portion;

a second gate line, said first gate line and said second gate line being disposed on said substrate and being insulated from each other, said first gate line being non-parallel to said second gate line;

an insulation layer disposed above said first gate line and said second gate line;

a data line, said data line and said first portion overlapping, said insulation layer being disposed between said data line and said first portion; and

a pixel electrode disposed above said data line, said pixel electrode and said second portion overlapping;

wherein said first portion is different from said second portion.

**10**. The liquid crystal display according to claim **9**, wherein said pixel electrode and said second gate line overlap.

**11**. The liquid crystal display according to claim **9**, wherein said liquid crystal display further comprises a semiconductor layer disposed above said insulation layer, said semiconductor layer comprises an undoped amorphous silicon layer and a doped amorphous silicon layer.

**12**. The liquid crystal display according to claim **9**, wherein said liquid crystal display further comprises a passivation layer disposed above said data line.

**13**. The liquid crystal display according to claim **9**, wherein said liquid crystal display further comprises a low-dielectric-constant layer disposed above said passivation layer.

**14**. The liquid crystal display according to claim **9**, wherein said first gate line comprises a pair of gate lines, said pair of gate lines are parallel to each other and separated by a gap.

**15**. The liquid crystal display according to claim **14**, wherein said data line, said gap and a part of said pair of gate lines overlap.

16. A manufacture method of a liquid crystal display, said method comprising:

providing a substrate;

forming a first gate line and a second gate line, said first gate line and said second gate line being disposed on said substrate and being insulated from each other, said first gate line being non-parallel to said second gate line;

forming an insulation layer disposed above said first gate line and said second gate line;

forming a data line, said data line and a first portion of said first gate line overlapping, said insulation layer being disposed between said data line and said first portion;

forming a passivation layer disposed above said data line;

forming a low-dielectric-constant layer disposed above said passivation layer; and

forming a pixel electrode disposed above said low-dielectric-constant layer, said pixel electrode and a second portion of said first gate line overlapping;

wherein said first portion is different from said second portion.

17. The liquid crystal display according to claim 16, wherein said liquid crystal display further comprises a semiconductor layer disposed above said insulation layer, said semiconductor layer comprises an undoped amorphous silicon layer and a doped amorphous silicon layer.

* * * * *

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|---|---|---|---|
| 专利名称(译) | 液晶显示器 | | |
| 公开(公告)号 | US6961109 | 公开(公告)日 | 2005-11-01 |
| 申请号 | US10/645703 | 申请日 | 2003-08-22 |
| [标]申请(专利权)人(译) | 赖汉钟离 | | |
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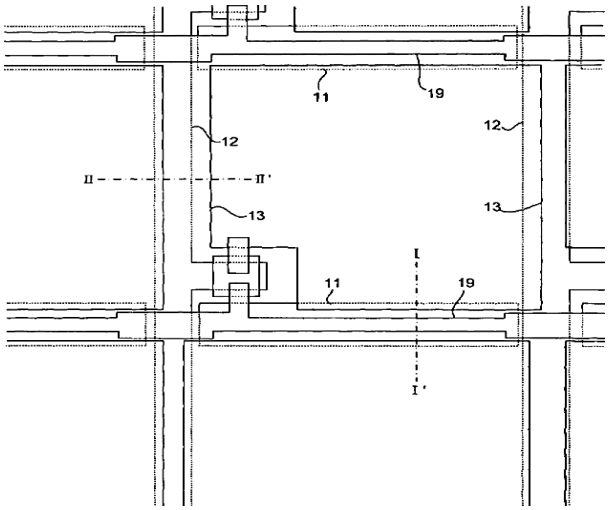
| IPC分类号 | G02F1/1343 G02F1/1362 G02F1/13 | | |
| CPC分类号 | G02F1/134336 G02F1/136286 | | |
| 审查员(译) | NGUYEN，龚便T. | | |
| 优先权 | 091124962 2002-10-25 TW | | |
| 其他公开文献 | US20040090563A1 | | |
| 外部链接 | Espacenet USPTO | | |


摘要(译)

本发明提供一种液晶显示器，包括基板，第一栅极线，第二栅极线，绝缘层，数据线，钝化层，低介电常数层和像素电极。第一栅极线与第二栅极线相交并与第二栅极线绝缘。像素电极与第一栅极线的一部分和第二栅极线的一部分重叠。数据线与第一栅极线的一部分重叠。与像素电极重叠的第一栅极线的部分与由数据线重叠的第一栅极线的部分不同。因此，减小了像素电极和数据线之间的电容效应。