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(54) **LIQUID CRYSTAL DISPLAY DEVICE**

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(57) **ABSTRACT**

An LCD with reduced power consumption is described. The LCD includes a liquid crystal panel having a plurality of gate lines and data lines, a data driver supplying a data voltage to the plurality of data lines, a controller generating a current control signal to control an output terminal of the data driver so that the output terminal operates during a first period in which data is outputted from the data driver, and the output terminal does not operate during a second period in which data is not outputted from the data driver, and a gate driver that supplies a scan signal to the plurality of the gate lines.

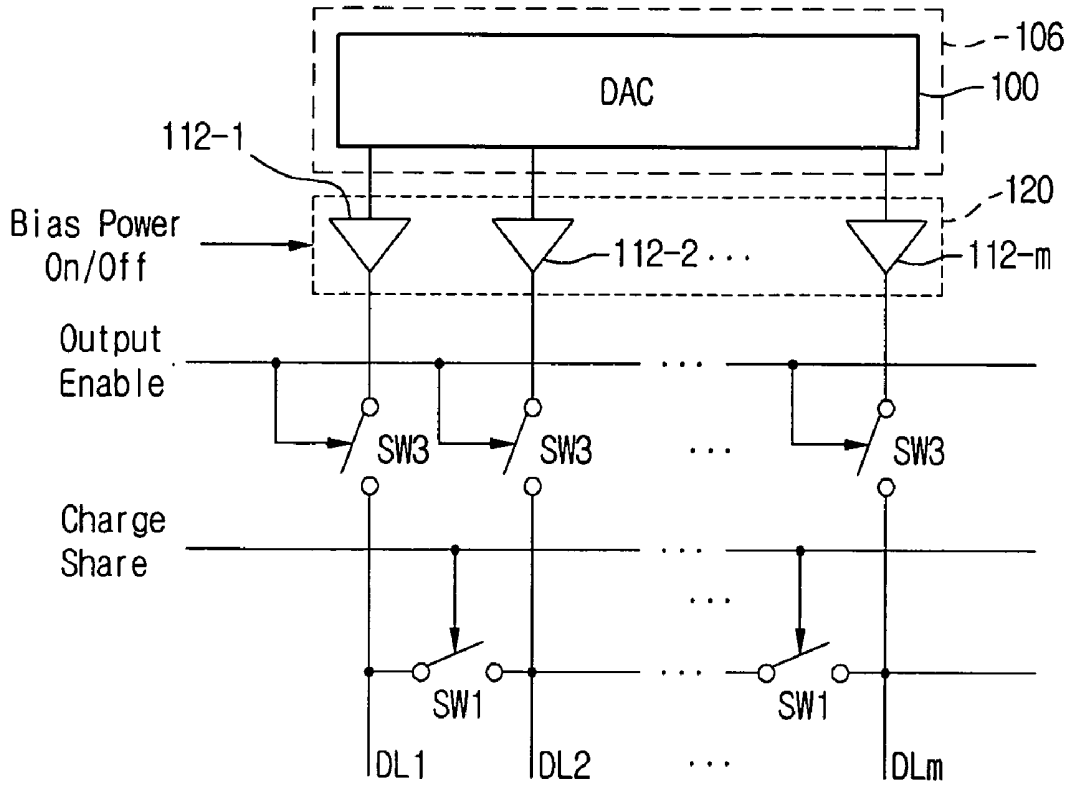


Fig.1 (Related Art)

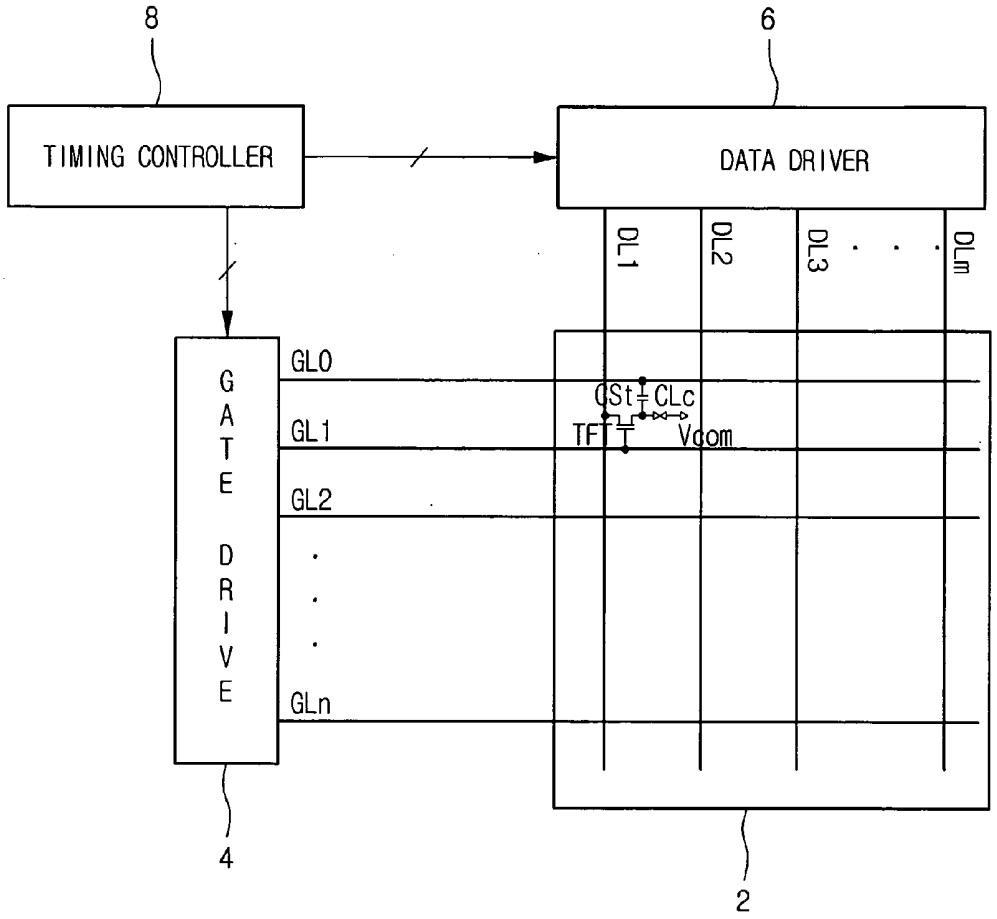


Fig.2

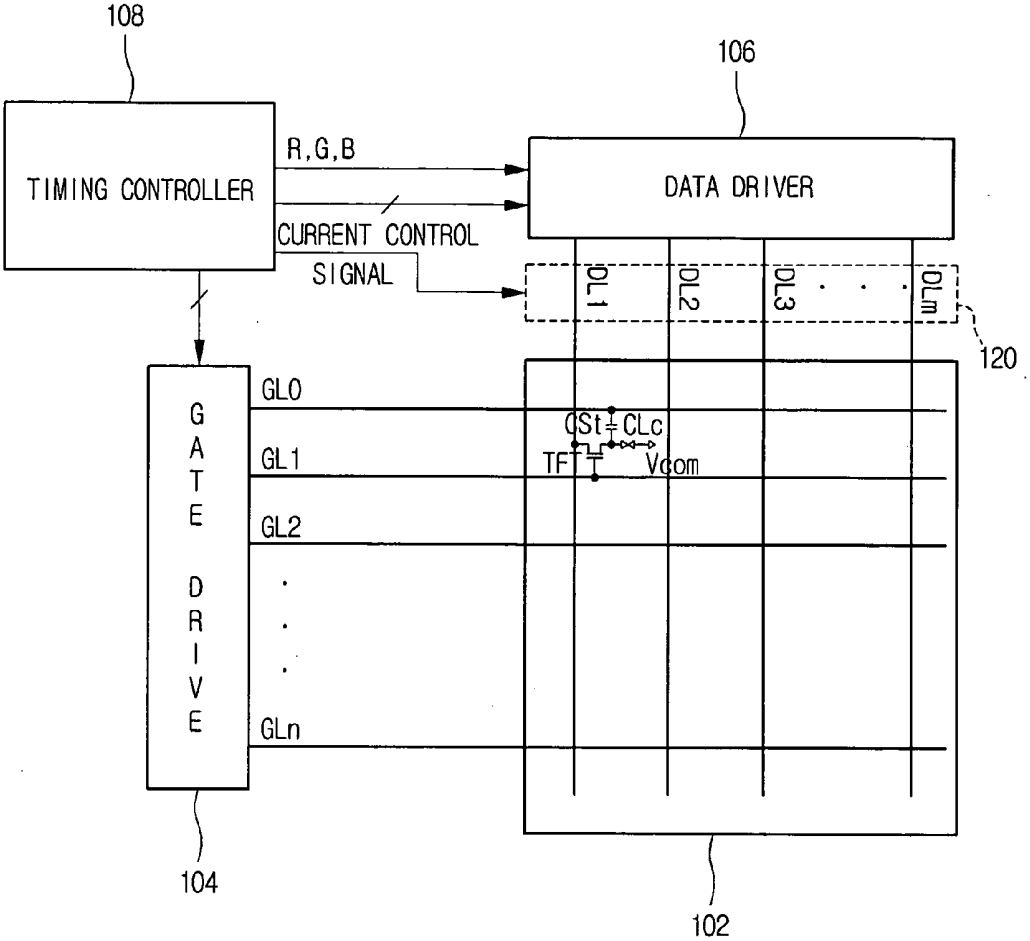

108
106
TIMING CONTROLLER
R,G,B
CURRENT CONTROL
SIGNAL
DATA DRIVER
DL1
DL2
DL3
DLm
120
GATE DRIVE
GL0
GL1
GL2
GLn
CSt
CLc
TFT
Vcom
104
102

Fig.3A

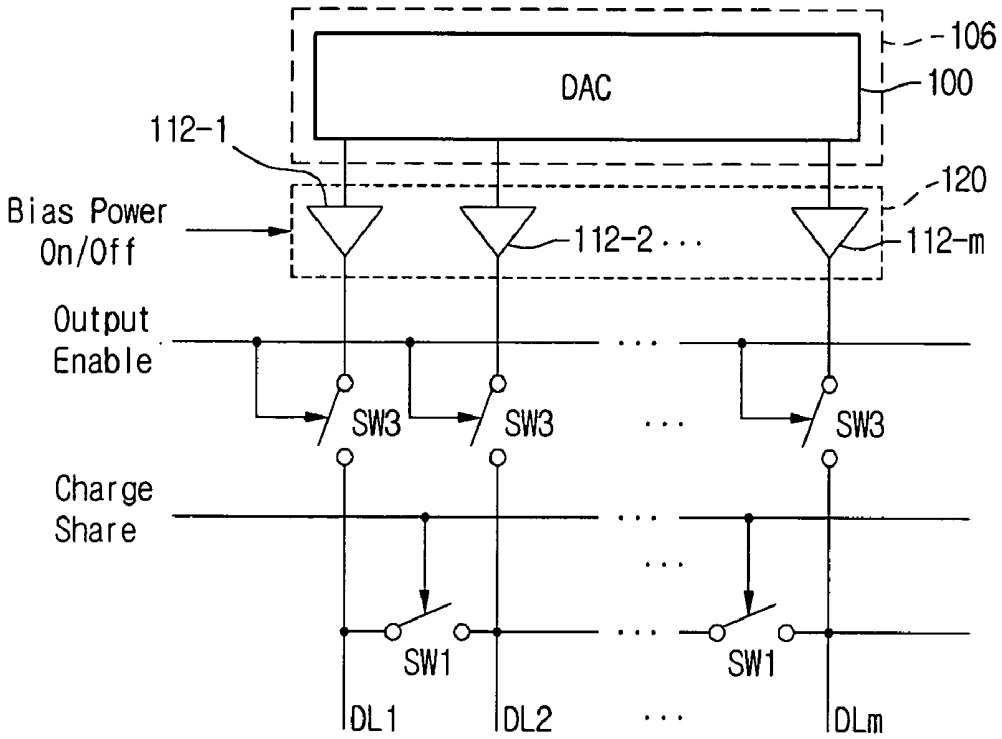

106
DAC
100
112-1
120
Bias Power
On/Off
112-2 · · ·
112-m
Output
Enable
SW3
SW3
SW3
Charge
Share
SW1
SW1
DL1
DL2
DLm

Fig.3B

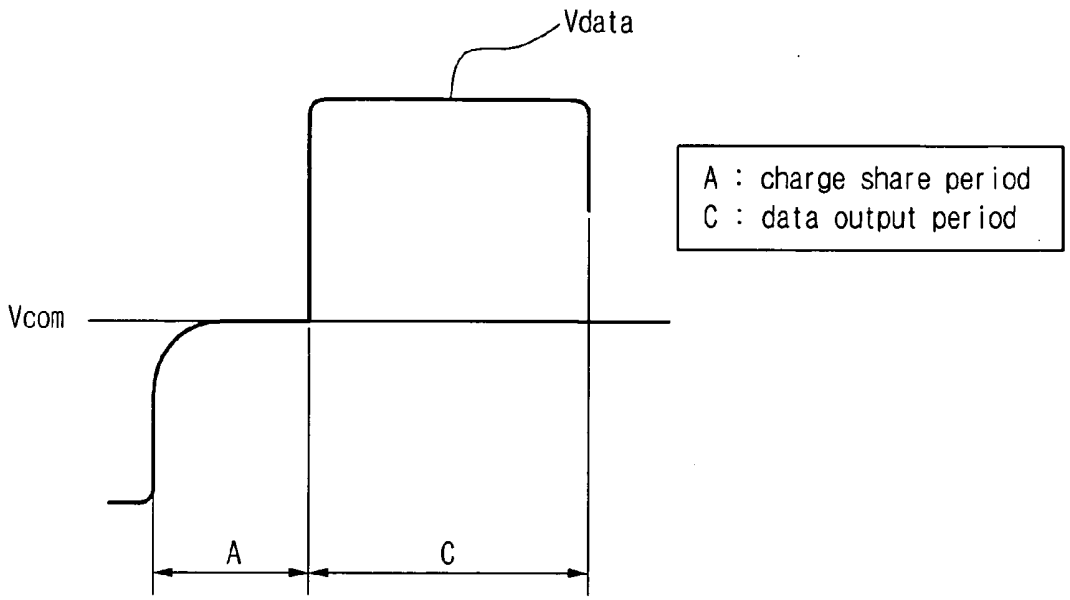


Fig.4A

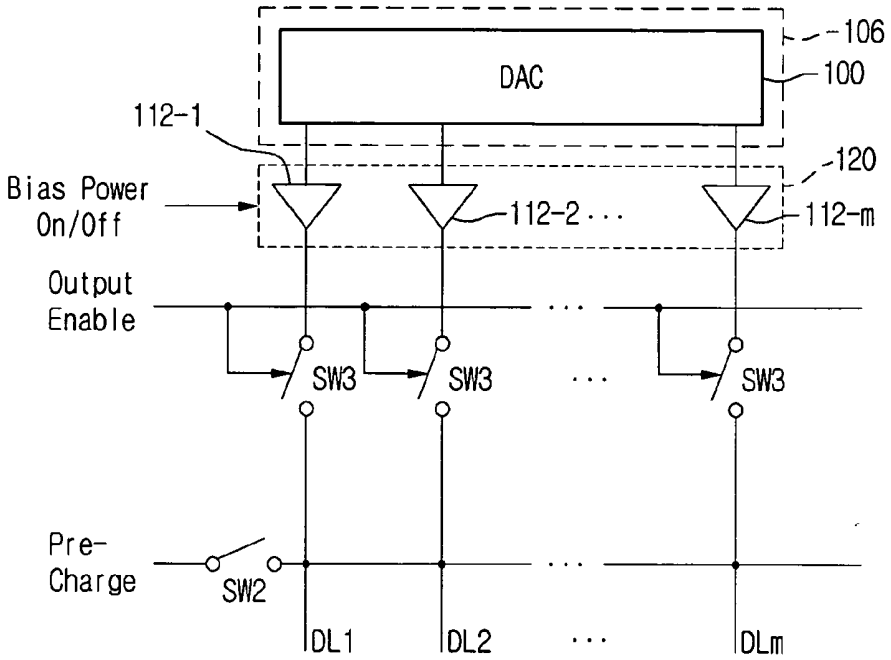

106
DAC
100
112-1
120
Bias Power
On/Off
112-2 · · ·
112-m
Output
Enable
SW3
SW3
SW3
Pre-
Charge
SW2
DL1
DL2
DLm

Fig.4B

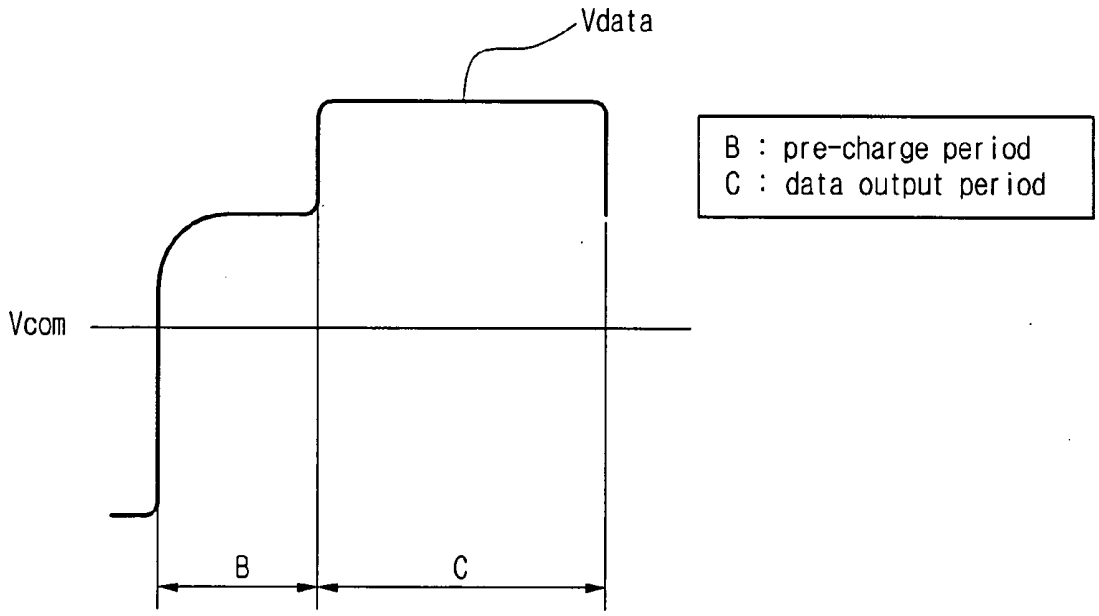

Vdata
B : pre-charge period
C : data output period
Vcom
B
C

Fig.5A

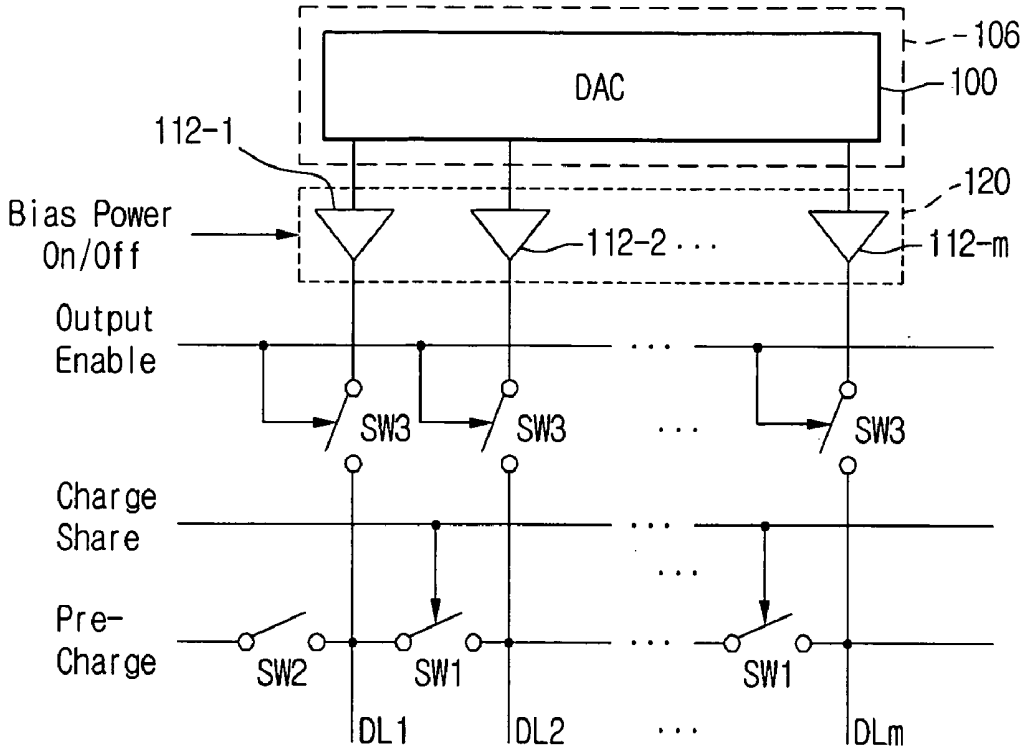

106
DAC
100
112-1
120
Bias Power
On/Off
112-2 · · ·
112-m
Output
Enable
SW3
SW3
SW3
Charge
Share
Pre-
Charge
SW2
SW1
SW1
DL1
DL2
DLm

Fig.5B

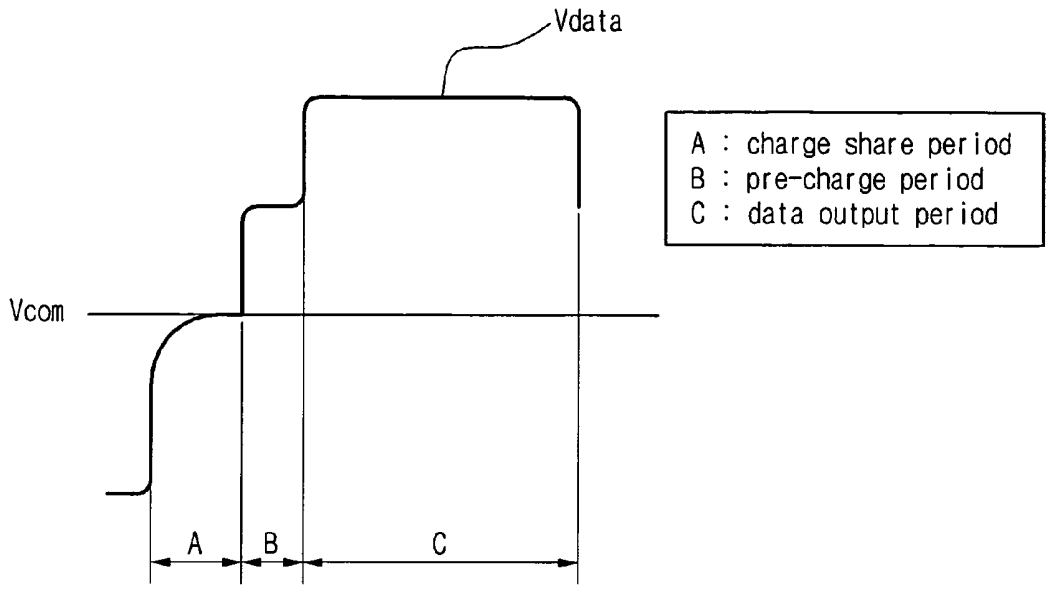

Vdata
Vcom
A
B
C
A : charge share period
B : pre-charge period
C : data output period

Fig.6

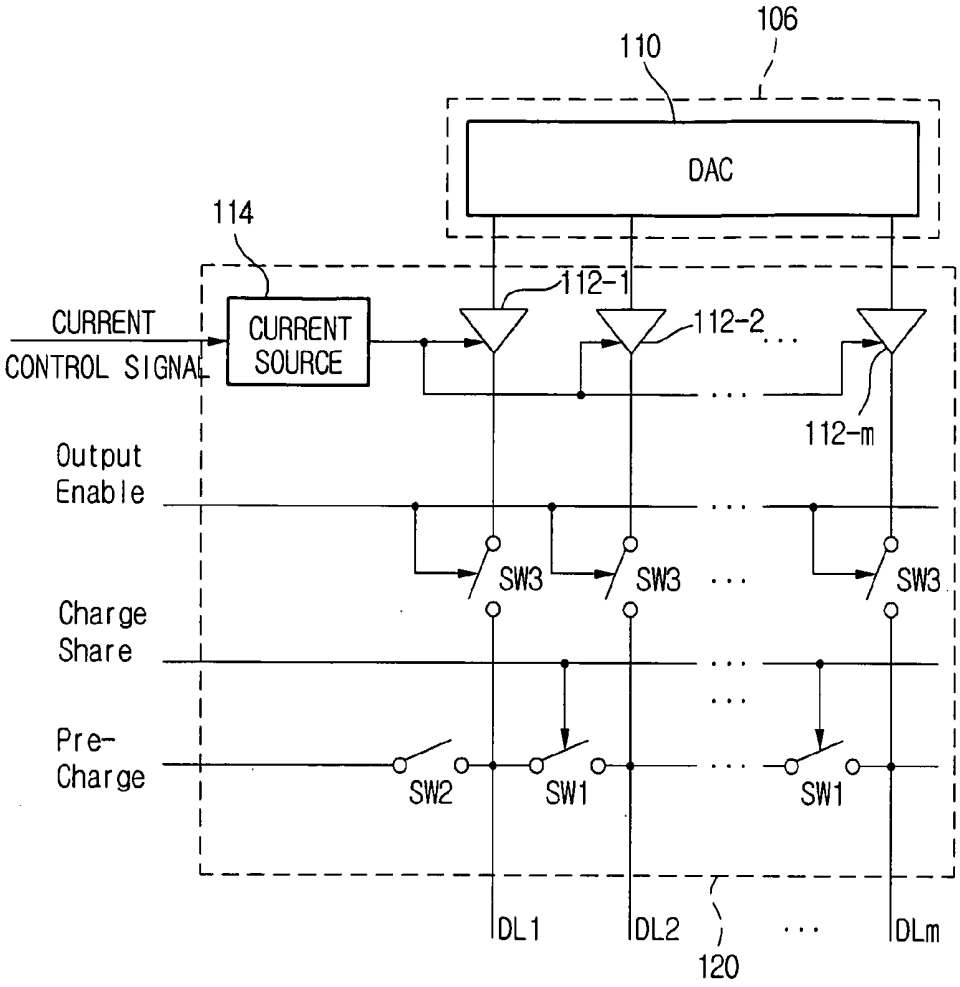

106
110
DAC
114
112-1
112-2
CURRENT
CONTROL SIGNAL
CURRENT
SOURCE
112-m
Output
Enable
SW3
SW3
SW3
Charge
Share
Pre-
Charge
SW2
SW1
SW1
DL1
DL2
DLm
120

Fig.7

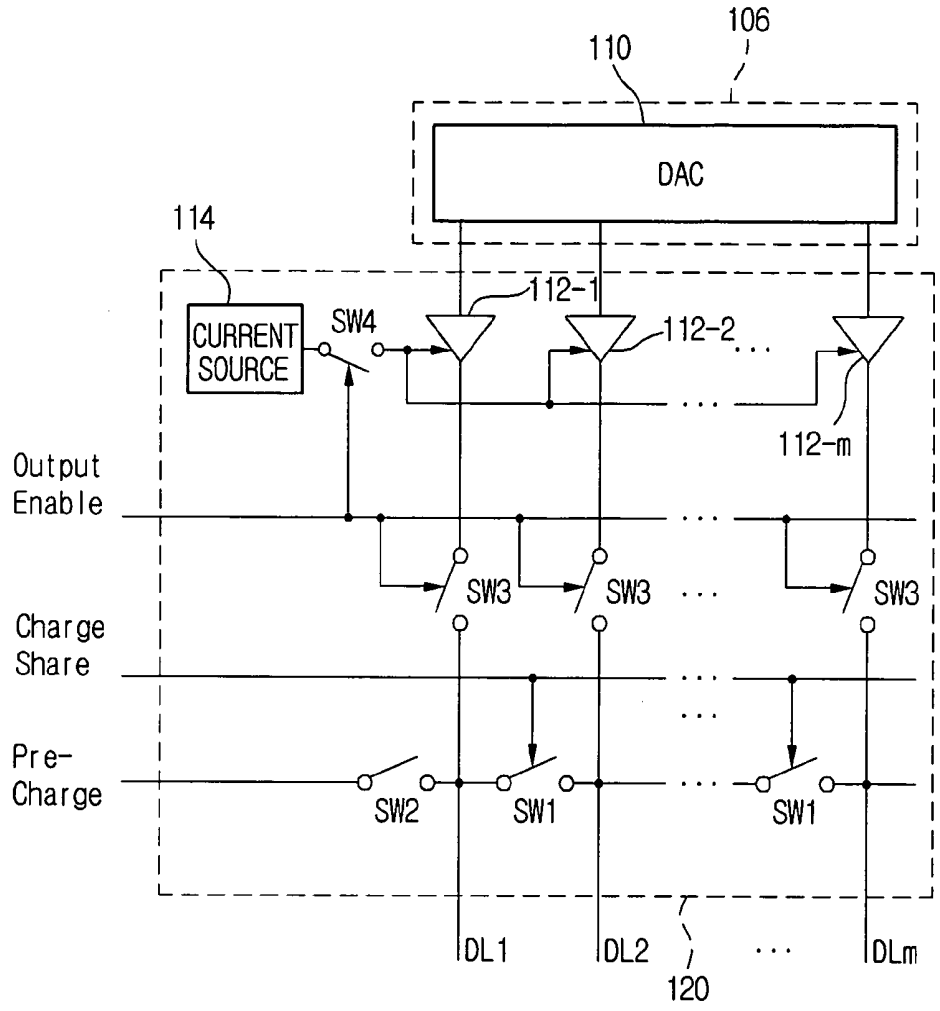

106
110
DAC
114
CURRENT SOURCE
SW4
112-1
112-2
112-m
Output Enable
Charge Share
Pre-Charge
SW3
SW2
SW1
DL1
DL2
DLm
120

Fig.8

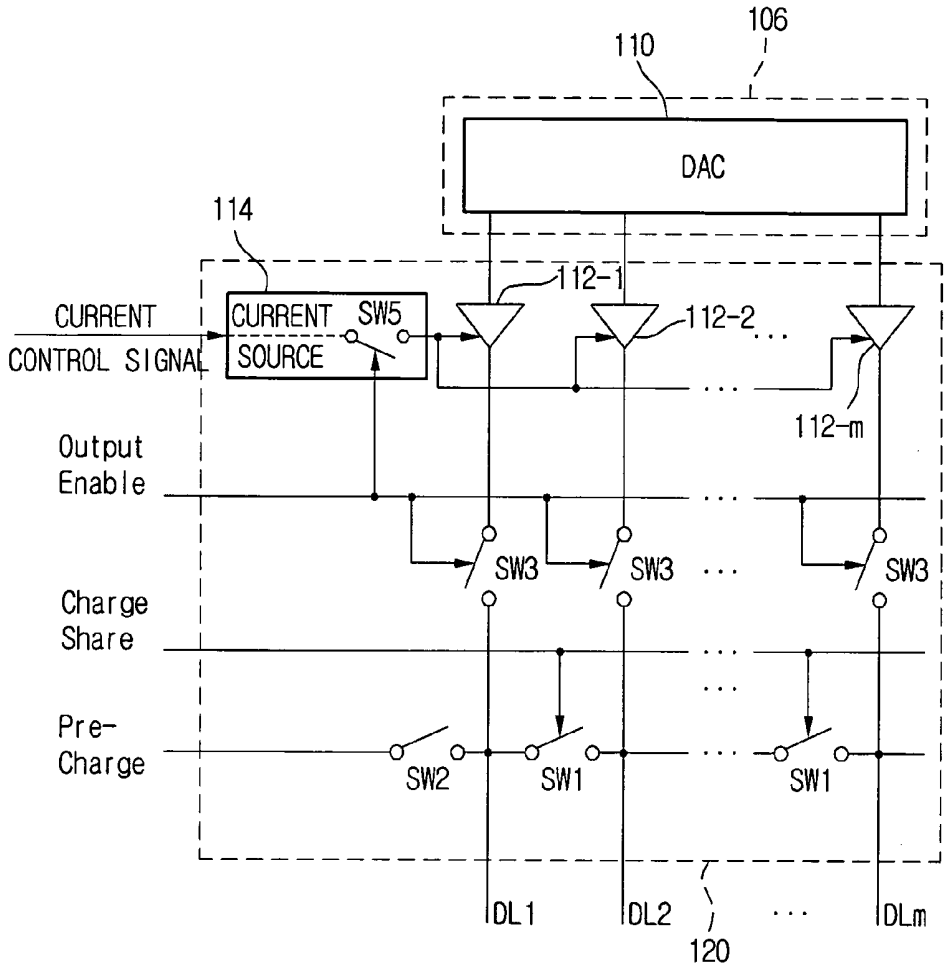

106
110
DAC
114
112-1
112-2
112-m
CURRENT
CONTROL SIGNAL
CURRENT SOURCE
SW5
Output Enable
Charge Share
Pre-Charge
SW3
SW2
SW1
DL1
DL2
DLm
120

Fig.9

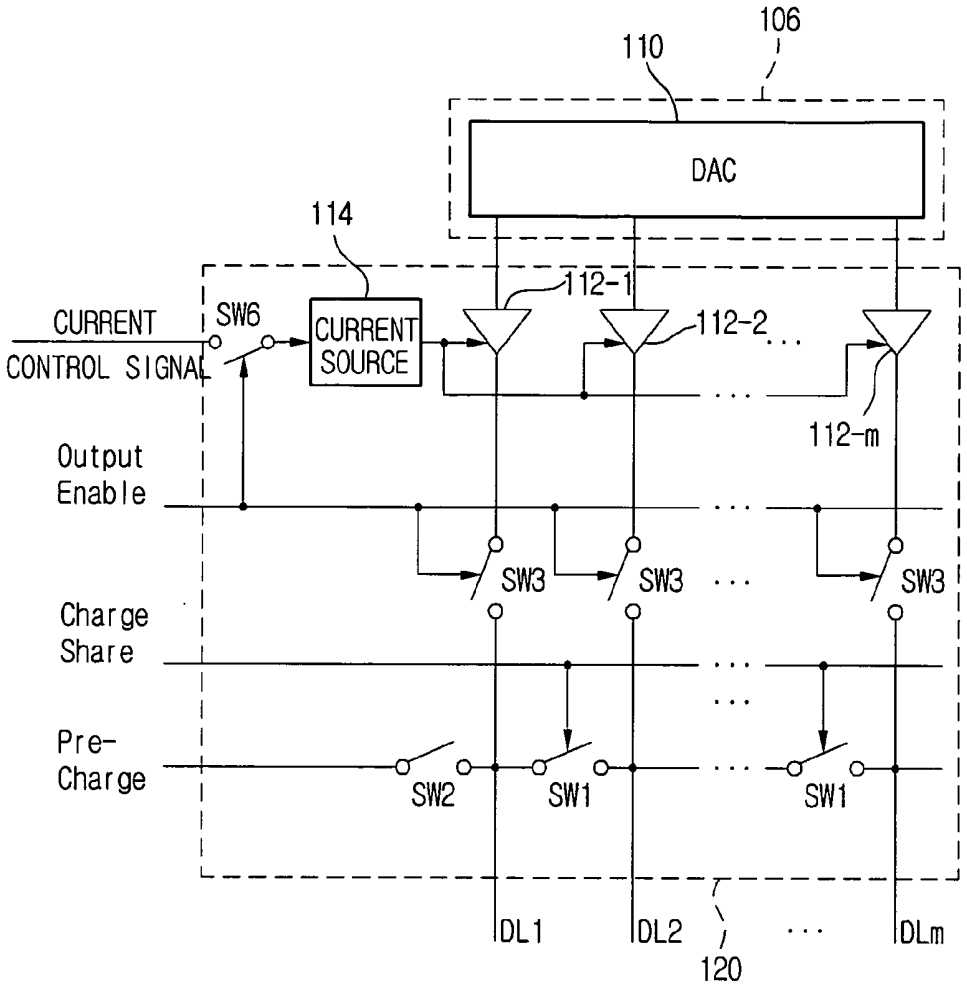

106
110
DAC
114
112-1
112-2
112-m
CURRENT
CONTROL SIGNAL
SW6
CURRENT
SOURCE
Output
Enable
SW3
SW3
SW3
Charge
Share
Pre-
Charge
SW2
SW1
SW1
DL1
DL2
DLm
120

Fig.10

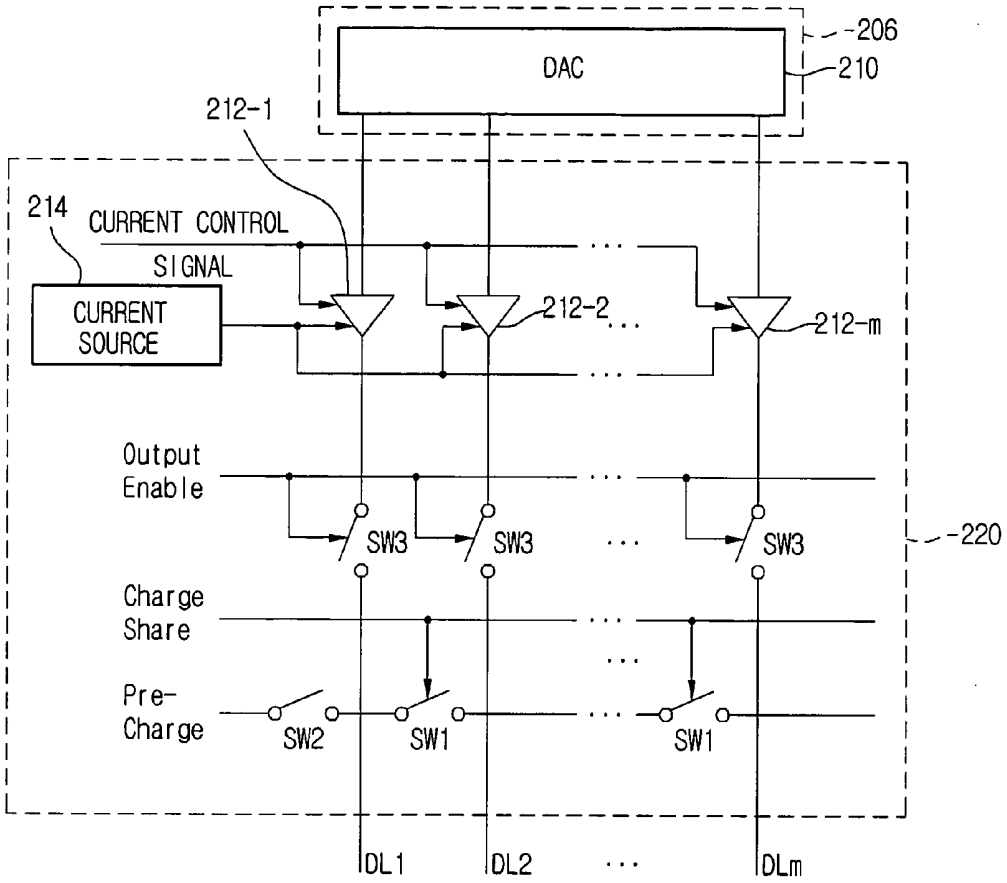

206
DAC
210
212-1
214
CURRENT CONTROL
SIGNAL
CURRENT SOURCE
212-2
212-m
Output Enable
SW3
SW3
SW3
220
Charge Share
Pre-Charge
SW2
SW1
SW1
DL1
DL2
DLm

Fig.11

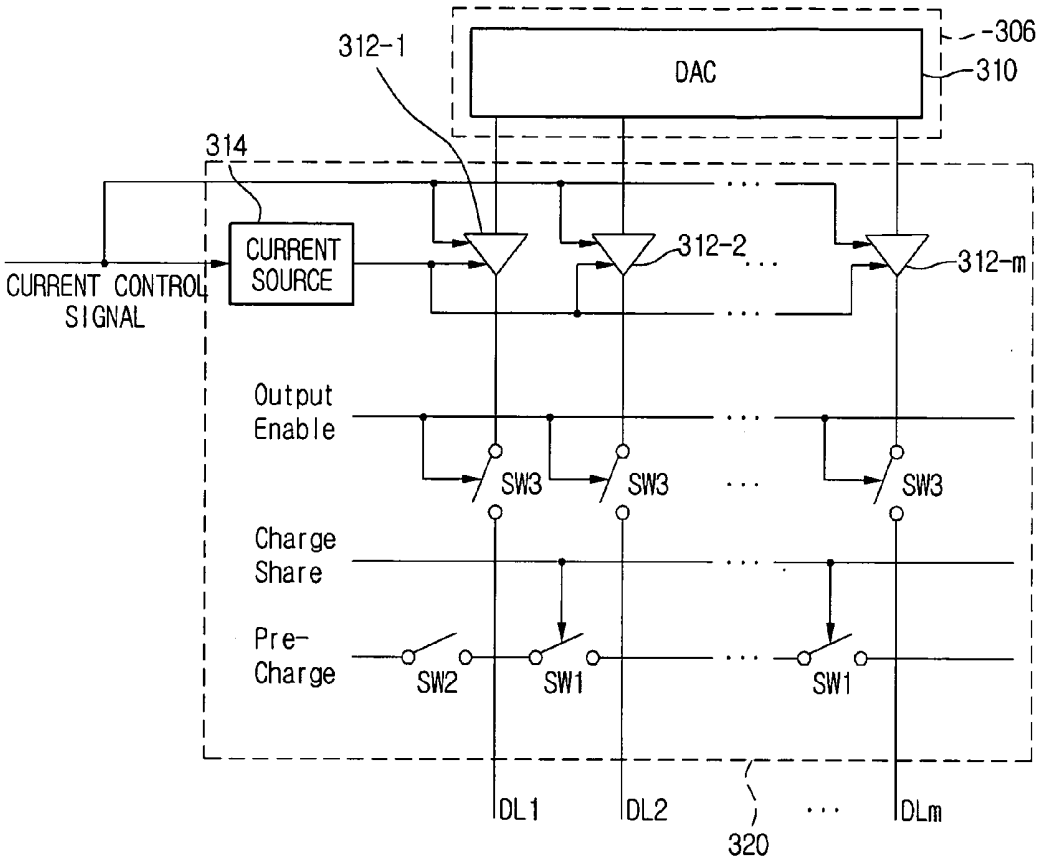

312-1
DAC
306
310
314
CURRENT SOURCE
CURRENT CONTROL SIGNAL
312-2
312-m
Output Enable
SW3
SW3
SW3
Charge Share
Pre-Charge
SW2
SW1
SW1
DL1
DL2
DLm
320

Fig.12A

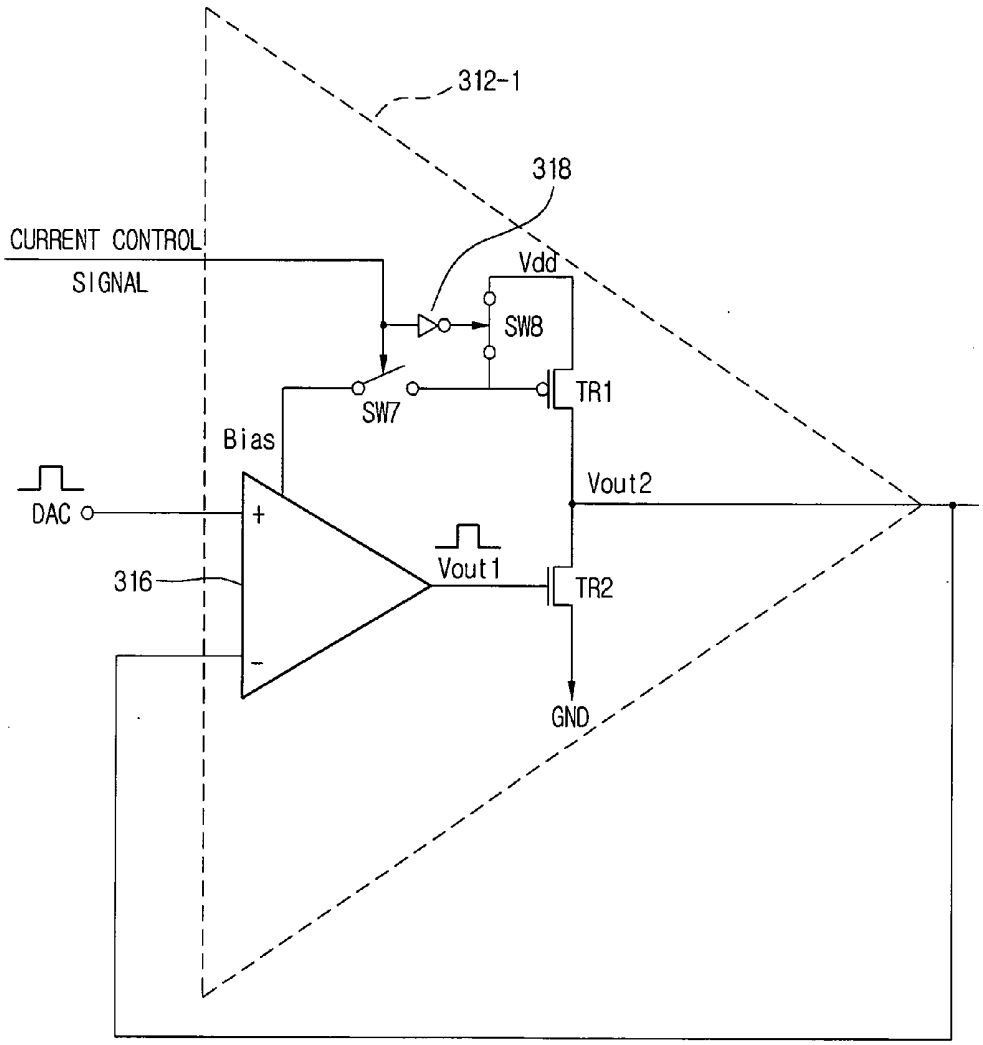
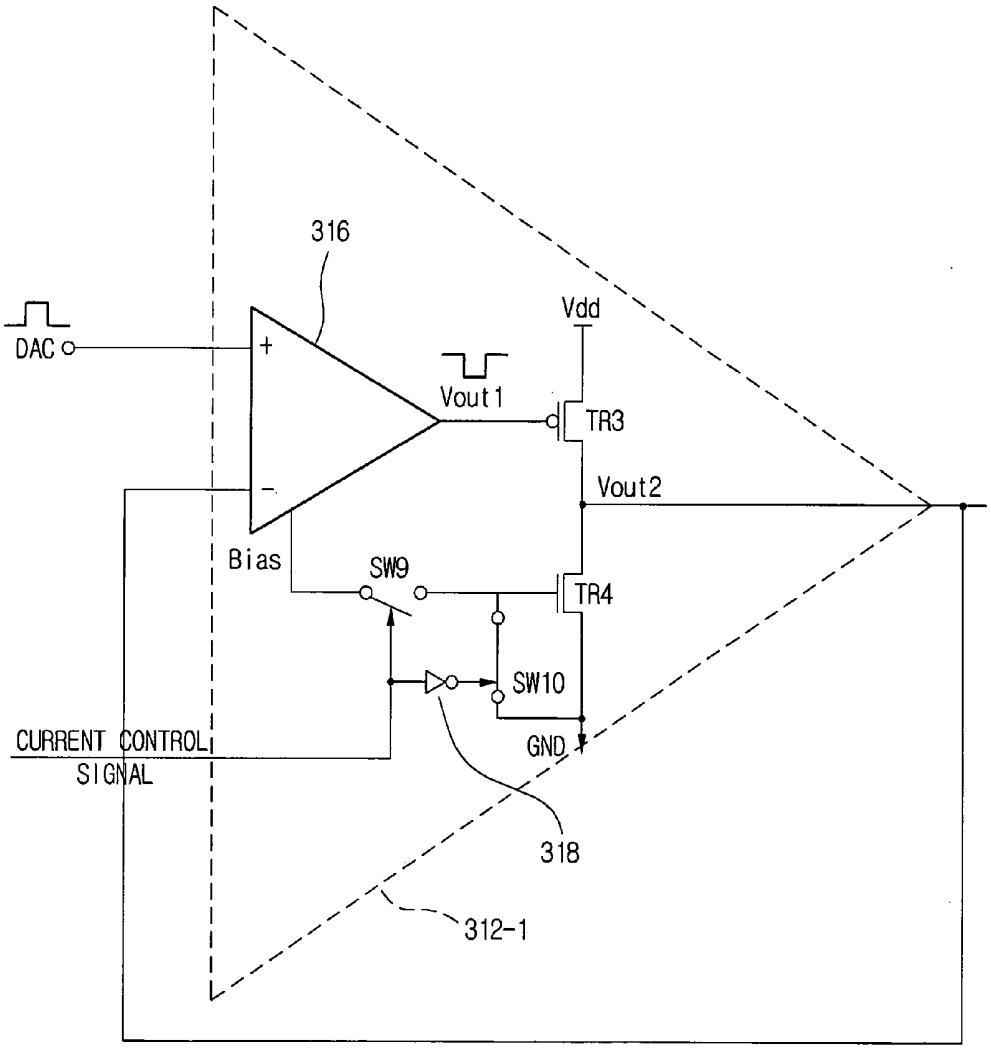

312-1
318
CURRENT CONTROL
SIGNAL
Vdd
SW8
SW7
TR1
Bias
DAC
Vout2
316
Vout1
TR2
GND

Fig.12B


316
DAC
+
-
Vout1
Vdd
TR3
Vout2
Bias
SW9
TR4
SW10
GND
CURRENT CONTROL SIGNAL
318
312-1

LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of priority to Korean patent application 131214/2005, filed on Dec. 28, 2005, which is incorporated by reference herein.

TECHNICAL FIELD

[0002] The present application relates to a liquid crystal display device (LCD), and more particularly, to an LCD capable of reducing power consumption.

BACKGROUND

[0003] A liquid crystal display (LCD) using an active matrix driving method can display a moving picture image using thin film transistors (TFTs) serving as a switching element. LCDs are widely used in computers (e.g., personal computers and notebook computers, etc.), office automation equipment (a copier, etc.), and portable devices (e.g., mobile phones, beepers, etc.) because of its thinness and lightness.

[0004] A liquid crystal panel includes a plurality of pixels arranged in a matrix, and a plurality of TFTs switching a data signal to be applied to each of the pixels. An image is displayed on a screen when the liquid crystal panel controls an amount of transmitted light supplied from a backlight.

[0005] The LCD includes a liquid crystal panel displaying an image and a driving unit driving the liquid crystal panel.

[0006] The related art LCD shown in FIG. **1** includes a liquid crystal panel **2** having a plurality of gate lines GL**0** to GL n and data lines DL**1** to DLm arranged to display a predetermined image, a gate driver **4** driving the gate lines GL**0** to GLn, a data driver **6** driving the data lines DL**1** to DLm, and a timing controller **8** controlling the gate driver **4** and the data driver **6**.

[0007] TFT switching devices are formed at the intersections of the gate lines GL**0** to GLn and the data lines DL**1** to DLm, arranged on the liquid crystal panel **2**. The TFT is connected to a pixel electrode (not shown), which is overlapped with the gate lines GL**0** to GLn to form a storage capacitor Cst.

[0008] The gate driver **4** sequentially applies a scan signal (i.e., gate high voltage VGH) to the gate lines GL**0** to GLn according to a control signal generated by the timing controller **8**.

[0009] The data driver **6** supplies a data voltage to the data lines DL**1** to DLm according to a control signal generated by the timing controller **8**. The data driver **6** includes output buffers (not shown) corresponding to the data lines DL**1** to DLm in the liquid crystal panel **2**.

[0010] Since the output buffers operate during a non-operation period in which data is not being applied to the liquid crystal panel **2**, a current is consumed because of driving the output buffers during the non-operation periods. Thus, power consumption is increased. Heat generated from the data driver **6** is maximized. Therefore, malfunctions of the liquid crystal panel **2** can occur due to the heat generating effect.

SUMMARY

[0011] A liquid crystal display (LCD) including a liquid crystal panel having a plurality of gate lines and data lines, a data driver supplying a data voltage to the plurality of data lines, a controller generating a current control signal to control an output terminal of the data driver so that the output terminal operates during a first period in which data is outputted from the data driver, and the output terminal does not operate during a second period in which data is not outputted from the data driver, and a gate driver supplying a scan signal to the plurality of the gate lines. Therefore, a current consumption is minimized and thus power consumption is reduced. Additionally, heat generated from the elements can be minimized.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a view of a related art LCD;

[0013] FIG. **2** is a view of an LCD of an embodiment;

[0014] FIG. **3**A is a view of an output terminal in a data driver of an embodiment;

[0015] FIG. **3**B is a view of an output voltage in a data driver of an embodiment;

[0016] FIG. **4**A is a view of another output terminal in a data driver of an embodiment;

[0017] FIG. **4**B is a view of another output voltage in a data driver of an embodiment;

[0018] FIG. **5**A is a view of another output terminal in a data driver of an embodiment;

[0019] FIG. **5**B is a view of another output voltage in a data driver of an embodiment;

[0020] FIG. **6** is a view of an output terminal in a data driver according to a first example;

[0021] FIG. **7** is a view of an output terminal in a data driver according to a second example;

[0022] FIG. **8** is a view of an output terminal in a data driver according to a third example;

[0023] FIG. **9** is a view of an output terminal in a data driver according to a fourth example;

[0024] FIG. **10** is a view of an output terminal in a data driver according to a fifth example;

[0025] FIG. **11** is a view of an output terminal in a data driver according to a sixth example;

[0026] FIG. **12**A is a view of an output buffer in the data driver of FIG. **11**; and

[0027] FIG. **12**B is a view of another output buffer in the data driver of FIG. **11**.

DETAILED DESCRIPTION

[0028] Exemplary embodiments may be better understood with reference to the drawings, but these examples are not intended to be of a limiting nature. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts

[0029] FIG. **2** shows an embodiment where the LCD includes a liquid crystal panel **102** to display a image, including a plurality of gate lines GL**0** to GLn and data lines DL**1** to DLm, a gate driver **104** for driving the plurality of gate lines GL**0** to GLn, a data driver **106** for driving the plurality of data lines DL**1** to DLm, and a timing controller **108** controlling the gate driver **104** and the data driver **106**.

[0030] Thin film transistors (TFT) are formed at intersections of the gate lines GL**0** to GLn and the data lines DL**1** to DLm on the liquid crystal panel **102**. The TFTs are connected to pixel electrodes (not shown), which are overlapped with the gate lines GL**0** to GLn to form a capacitor Cst.

[0031] The gate driver **104** supplies scan signals (i.e., a gate high voltage VGH or a gate low voltage VGL) to the gate lines GL**0** to GLn according to a gate control signal supplied from the timing controller **108**.

[0032] The data driver **106** supplies a data voltage (an analog voltage) to the data lines DL**1** to DLm according to a control signal supplied form the timing controller **108**. An output terminal **120** of the data driver **106** (hereinafter, referred to as an output terminal) includes a plurality of output buffers (not shown) corresponding to the data lines DL**1** to DLm.

[0033] The output terminal **120** is controlled by a current control signal supplied from the timing controller **108**. For example, when the current control signal is a high state, the output terminal **120** does not operate, and when the current control signal is a low state, the output terminal **120** operates. The timing controller **108** generates a gate control signal, a data control signal, and a current control signal using a Vsync/Hsync signal, a data enable (DE) signal, and a clock signal.

[0034] The timing controller **108** generates and supplies a low state current control signal to the output terminal **120** during a period in which a data is not outputted from the data driver **106**. A current source for driving the output terminal **120** thus is turned on and supplies a driving current to the output buffers **112-1** to **112-***m*. Therefore, the output buffers **112-1** to **112-***m* operate during the period in which the data is not outputted from the data driver **106**.

[0035] As shown in FIGS. **3** to **5**, the data driver **106** includes a digital-to-analog converter (DAC) **110** converting a digital data signal supplied from the timing controller **108** into an analog data voltage. The DAC **110** is connected to output buffers **112-1** to **112-***m* corresponding to the data lines DL**1** to DLm, respectively.

[0036] The data lines DL**1** to DLm can be supplied with a charge share voltage or a pre-charge voltage during a charge share period or a pre-charge period, respectively. Also, the data lines DL**1** to DLm can be supplied with both of the charge share voltage and the pre-charge voltage during the charge share period and the pre-charge period.

[0037] The output buffers **112-1** to **112-***m* are turned on/off by a current from a current source (not shown) that is controlled by a current control signal supplied from the timing controller **108**.

[0038] The output buffers **112-1** to **112-***m* operate using a current supplied from a current source.

[0039] The current control signal generated from the timing controller **108** is supplied to the current source.

[0040] During the charge share period and the pre-charge period in which data is not outputted from the data driver **106**, the output buffers **112-1** to **112-***m* do not operate because the current source **114** does not supply a driving current. Since the output buffers **112-1** to **112-***m* do not operate during the charge share period and the pre-charge period, power consumption may be reduced. Additionally, since the output buffers **112-1** to **112-***m* do not operate during the charge share and pre-charge periods, heat which is generated from elements located inside the output buffers **112-1** to **112***m* may be reduced.

[0041] During the data output period in which the data is outputted from the data driver **106**, the output buffers **112-1** to **112-***m* receive data voltages from the DAC **110** and supply the data voltages to the corresponding data lines DL**1** to DLm. During the data output period, the output buffers **112-1** to **112-***m* are electrically connected to the data lines DL**1** to DLm through the third switch SW**3**.

[0042] The third switch SW**3** is turned on when a high output enable (OE) signal is supplied during the data output period. During the data output period, the output buffers **112-1** to **112-***m* are thus connected to data lines DL**1** to DLm, and data voltages are supplied to corresponding to the data lines DL**1** to DLm, so that an image corresponding to the data voltages is displayed on the liquid crystal panel **102**.

[0043] During the charge share and pre-charge periods, the current source **114** is turned off, and a driving current is not supplied to the output buffers **112-1** to **112-***m* when the high state current control signal from the timing controller **108** is supplied to the current source **114**.

[0044] During the data output period, the current source **114** is turned on, and a driving current is supplied to the output buffers **112-1** to **112-***m* when the low state current control signal from the timing controller **108** is supplied to the current source **114**. Therefore, the output buffers **112-1** and **112-***m* are connected to data lines DL**1** to DLm, and operate during the third operation period.

[0045] Whether the output buffers **112-1** to **112-***m* operate or not is determined by the state of the current control signal.

[0046] For example, when a low state current control signal is supplied to the output buffers **112-1** to **112-***m*, the output buffers **112-1** to **112-***m* do not operate. When a high state current control signal is supplied to the output buffers **112-1** to **112-***m*, the output buffers **112-1** to **112-***m* operate, the output buffers **112-1** to **112-***m* receive a driving current from the current source **114**.

[0047] As shown FIGS. **3**A and **3**B, the data driver **106** operates during two operation periods. A first operation period is a charge share period A. A second operation period is a data output period C.

[0048] During the charge share period A, a charge share control signal is applied to the first switch SW**1**, and the first switch SW**1** is turned on when a high state charge share control signal is applied to the first switch SW**1**. The first switch SW**1** is arranged in a direction intersecting the data lines DL**1** to DLm to connect data lines DL**1** to DLm each other through the first switch, and. A voltage corresponding to the common voltage Vcom is supplied to the data lines DL**1** to DLm.

[0049] During the data output period C, an image corresponding to a data voltage is displayed on the liquid crystal panel **102** of FIG. **2** when a required data voltage is supplied to the data lines DL**1** to DLm.

[0050] During the first period, the output buffers **112-1** to **112-***m* do not operate (OFF state); during the second period, the output buffers **112-1** to **112-***m* operate (ON state).

[0051] As shown FIGS. **4**A and **4**B, the data driver **106** operates during two operation periods. A first operation period is a pre-charge period B. A second operation period is a data output period C.

[0052] In the pre-charge period, a voltage lower than a required data voltage is charged before the required data voltage is supplied to the data lines DL**1** to DLm. Thus, power consumption associated with charging the required data voltage can be reduced.

[0053] A pre-charge voltage is supplied to the data lines DL**1** to DLm. During the pre-charge period B, a voltage higher than the common voltage Vcom is supplied to the data lines DL**1** to DLm.

[0054] The output buffers **112-1** to **112-***m* do not operate during the pre-charge period B; the output buffers **112-1** to **112-***m* operate during the data output period C.

[0055] As shown FIGS. **5**A and **5**B, the data driver **106** can operate during three operation periods. A first operation

period is a charge share period A. A second operation period is a pre-charge period B. A third operation period is a data output period C.

[0056] The data driver **106** includes a digital-to-analog converter (DAC) **110**. An output terminal **120** of the DAC **110** includes a plurality of output buffers **112-1** to **112-***m* corresponding to the data lines DL**1** to DLm arranged on the liquid crystal panel **102**. The LCD with the data driver **106** performs pre-charging through charge sharing. The output buffers **112-1** to **112-***m* are connected through the data lines DL**1** to DLm and switches SW**1** and SW**2**.

[0057] A third period is a data output period, and an image corresponding to a data voltage is displayed on the liquid crystal panel **102** of FIG. **2** when a required data voltage is supplied to the data lines DL**1** to DLm.

[0058] During the first operation period, a charge share control signal is applied to the first switch SW**1**, and the first switch SW**1** is turned on when a high state charge share control signal is applied to the first switch SW**1**. The first switch SW**1** is arranged in a direction intersecting the data lines DL**1** to DLm to connect data lines DL**1** to DLm each other through the first switch, and. A voltage corresponding to the common voltage Vcom is supplied to the data lines DL**1** to DLm.

[0059] A second switch SW**2** is turned on in the second operation period, and a pre-charge voltage is supplied to the data lines DL**1** to DLm. Therefore, a voltage higher than the common voltage Vcom is supplied to the data lines DL**1** to DLm. The output buffers **112-1** to **112-***m* are not connected to the data lines DL**1** to DLm during the first and second operation periods; and, output buffers **112-1** to **112** do not operate during the first and second operation periods.

[0060] During the third operation period, a third switch SW**3** disposed between output buffers **112-1** to **112-***m* and data lines DL**1** to DLm is closed. The third switch SW**3** is controlled by an output enable (OE) signal. During the third operation period, an OE high signal is applied to the third switch SW**3** to electrically connect the output buffers **112-1** to **112-***m* and data lines DL**1** to DLm.

[0061] The output buffers **112-1** to **112-***m* thus supply a data voltage from the DAC **110** to the data lines DL**1** to DLm through the third switch SW**3**; and, output buffers **112-1** to **112-***m* do not operate during the third operation period.

[0062] That is, the output buffers **112-1** to **112-***m* operate by receiving a converted data voltage from the DAC **110** through a non-inverting input terminal. The output buffers **112-1** to **112-***m* operate during the first and second operation periods. The output buffers **112-1** to **112-***m* are connected to the data lines DL**1** to DLm and supply a data voltage from the DAC **110** to the data lines DL**1** to DLm during the third operation period.

[0063] During the first and second operation periods, the output buffers **112-1** to **112-***m* do not operate (OFF state); and, during the third operation period, the output buffers **112-1** to **112-***m* operate (ON state). The output buffers **112-1** to **112-***m* are controlled by the current control signal from the timing controller.

[0064] The timing controller generates the current control signal to control output buffers **112-1** to **112-***m* of the data driver **106** so that the output terminal **120** operates during the third operation period, in which data is outputted from the data driver, and the output terminal **120** does not operate during at least one of the charge-share period and the pre-charge period, in which data is not outputted from the data driver.

[0065] FIG. **6** is a view of an output terminal in a data driver according to a first example. During the first and second operation periods, the timing controller **108** generates and supplies a high state current control signal to the current source **114** and the current source **114** is turned off, and does not supply a driving current to the output buffers **112-1** to **112-***m*. Therefore, the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods and output buffers **112-1** to **112-***m* are not connected to the data lines DL**1** to DLm during the first and second operation periods.

[0066] During the first and second operation periods, first and second switches SW**1** and SW**2** are turned on and a voltage is supplied to the data lines DL**1** to DLm. The first and second switches SW**1** and SW**2** are turned on when an "on" state charge share control signal and a pre-charge voltage are supplied during the first and second operation periods.

[0067] The timing controller **108** generates and supplies a low state current control signal to the current source **114** during the third operation period. The current source **114** thus is turned on and supplies a driving current to the output buffers **112-1** to **112-***m*. Therefore, the output buffers **112-1** to **112-***m* operate during the third operation period.

[0068] During the third operation period, the output buffers **112-1** to **112-***m* receive data voltages from the DAC **110** and supply the data voltages to the corresponding data lines DL**1** to DLm; and, the output buffers **112-1** to **112-***m* are electrically connected to the data lines DL**1** to DLm through the third switch SW**3**.

[0069] The third switch SW**3** is turned on when a high state output enable (OE) signal is supplied during the third operation period. The output buffers **112-1** to **112-***m* are thus connected to data lines DL**1** to DLm, and data voltages are supplied to corresponding data lines DL**1** to DLm, so that an image corresponding to the data voltages is displayed on the liquid crystal panel **102**.

[0070] During the first and second operation periods in which data is not output from the data driver, the output buffers **112-1** to **112-***m* do not operate because the current source **114** does not supply a driving current. Since the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods, power consumption may be reduced. Additionally, since the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods, heat which is generated from elements located inside the output buffers **112-1** to **112***m* may be reduced.

[0071] FIG. **7** is a view of an output terminal in a data driver according to a second example. The current source is connected to the output buffers **112-1** to **112-***m* through a forth switch SW**4**. The third switch SW**3** and the forth switch SW**4** are turned on when a high output enable (OE) signal is supplied during the third operation period.

[0072] The output buffers **112-1** to **112-***m* are electrically connected to the data lines DL**1** to DLm through the third switch SW**3** and the current source **114** is electrically connected to the output buffers **112-1** to **112-***m* through the forth switch SW**4**.

[0073] Therefore, the output buffers **112-1** to **112-***m* operate during the third operation period, and the output buffers **112-1** third and fifth switches SW**3** and SW**5** are turned off and, the output buffers **112-1** to **112-***m* do not operate because

the output buffers **112-1** to **112-***m* do not receive a driving current from the current source **114**.

[0074] During the third operation period, the output buffers **112-1** to **112-***m* are electrically connected to the data lines DL**1** to DLm through the third switch SW**3** and the current source **114** operates and supplies the driving current to the output buffers **112-1** to **112-***m* by the fifth switch SW**5**. At the same time, the first and second switches SW**1** and SW**2** are turned off.

[0075] Therefore, the output buffers **112-1** to **112-***m* operate during the third operation period because the output buffers **112-1** to **112-***m* receive the driving current from the current source **114**.

[0076] During the first and second operation period, the output buffers **112-1** to **112-***m* do not operate because the current source **114** does not supply a driving current. Since the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods, power consumption may be reduced. Additionally, since the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods, heat which is generated from elements located inside the output buffers **112-1** to **112***m* may be reduced.

[0077] FIG. **9** is a view of an output terminal in a data driver according to a forth example.

[0078] The current source is connected to the output buffers **112-1** to **112-***m*. and the current source **114** receives a current control signal from the timing controller (not shown) through a sixth switch SW**6**. The third and sixth switches SW**3** and SW**6** are turned on when a high state output enable (OE) signal is supplied during the third operation period.

[0079] During the third operation period, the output buffers **112-1** to **112-***m* are electrically connected to the data lines DL**1** to DLm through the third switch SW**3** and the current source **114** receives the current control signal from the timing controller through the sixth switch SW**6**. The current source is electrically connected to the output buffers **112-1** to **112-***m* through the current control signal.

[0080] Therefore, the output buffers **112-1** to **112-***m* operate during the third operation period, and the output buffers **112-1** to **112-***m* do not operate during the first and second operation period.

[0081] During the first and second operation period, the output buffers **112-1** to **112-***m* do not operate because the current source **114** does not supply a driving current. Since the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods, power consumption may be reduced. Additionally, since the output buffers **112-1** to **112-***m* do not operate during the first and second operation periods, heat which is generated from elements located inside the output buffers **112-1** to **112***m* may be reduced.

[0082] It will be understood by persons of skill in the art that the switches described herein may be shown as contact closures for clarity of illustration of function, and may be implemented by any means performing the switching function. For example, the switches may be at least one of a NMOS transistor, a PMOS transistor, a CMOS transistor, a diode, a bipolar transistor, or the like.

[0083] FIG. **10** is a view of an output terminal in a data driver according to a fifth example.

[0084] The data driver **206** supplies a data voltage (an analog voltage) to the data lines DL**1** to DLm according to a control signal supplied form the timing controller. An output terminal **220** of the data driver **206** (hereinafter, referred to as an output terminal) includes a plurality of output buffers **212-1** to **212-***m* corresponding to the data lines DL**1** to DLm. The output buffers **212-1** to **212-***m* are supplied with a driving current from a current source **214**.

[0085] The output buffers **212-1** to **212-***m* are controlled by the current control signal supplied from the timing controller. For example, when the current control signal is a high state during the first and second operation period, the output buffers **212-1** to **212-***m* do not operate, and when the current control signal is a low state during the third operation period, the output buffers **212-1** to **212-***m* operate.

[0086] FIG. **11** is a view of an output terminal in a data driver according to a sixth example. The current source **314** and the output buffers **312-1** to **312-***m* receive a current control signal generated from the timing controller.

[0087] During the first and second operation periods, the timing controller generates and supplies a high state current control signal to the current source **314** and the output buffers **312-1** to **312-***m*. And the current source **314** is turned off, and the output buffers **312-1** to **312-***m* do not operate during the first and second operation periods.

[0088] During the third operation period, the timing controller generates and supplies a low state current control signal to the current source **314** and the output buffers **312-1** to **312-***m*. The current source **314** is turned on, and the output buffers **312-1** to **312-***m* operate during the third operation period.

[0089] During the third operation period, the output buffers **312-1** to **312-***m* receive data voltages from the DAC **310** and supply the data voltages to the corresponding data lines DL**1** to DLm.

[0090] The output buffers **312-1** to **312-***m* do not operate during the first and second operation periods, power consumption may be reduced. Additionally, since the output buffers **312-1** to **312-***m* do not operate during the first and second operation periods, heat which is generated from elements located inside the output buffers **312-1** to **312***m* may be reduced.

[0091] FIG. **12***a* is a view of an output buffer in the data driver of FIG. **11**.

[0092] A first output buffer **312-1** shown in FIG. **12***a* includes an operational amplifier **316**, two transistors TR**1** and TR**2**, two switches SW**7** and SW**8**, and an inverter **318**.

[0093] During the first and second operation periods, the low state current control signal is supplied to the seventh switch SW**7** and the inverter **318**. The low state current control signal is converted into a low signal through the inverter **318** and then supplied into the eighth switch SW**8**.

[0094] The seventh switch SW**7** is turned off by the low state current control signal, and the eighth switch SW**8** is turned on by the high state current control signal.

[0095] When the eighth switch SW**8** is turned on, a power supply voltage Vdd is supplied to a gate terminal of the first transistor TR**1**. Simultaneously, the power supply voltage Vdd is supplied to a source terminal of the first transistor TR**1**.

[0096] Therefore, a voltage Vg supplied to the gate terminal of the first transistor TR**1** and a voltage Vs supplied to the source terminal of the first transistor TR**1** become equal. A current does not flow between the source and drain terminals when the voltage Vg supplied to the gate terminal of the first transistor TR**1** and a voltage Vs supplied to the source terminal of the first transistor TR**1** are equal. Consequently, the first output buffer **212-1** does not operate during the first and second operation periods.

[0097] A high state current control signal generated by the timing controller and supplied to the seventh switch SW**7** and the inverter **318** during the third operation period. The high state current control signal supplied to the inverter **318** is converted into a low signal, and supplied to the eighth switch SW**8**. The seventh switch SW**7** is tuned on by the high state current control signal, and the eighth switch SW**8** is turned off by the high state current control signal.

[0098] When the seventh switch SW**7** is turned on, a bias voltage supplied by the operational amplifier **316** is supplied to the gate terminal of the first transistor TR**1** through the seventh switch SW**7**. The bias voltage differs from that of the power supply voltage Vdd, and the power supply voltage Vdd is supplied from the source terminal to the drain terminal in the first transistor TR**1**.

[0099] Since a voltage Vg supplied to the gate terminal of the first transistor TR**1** is the bias voltage, and a voltage Vs supplied to the source terminal is the power supply voltage Vdd, a current flows from the source terminal to the drain terminal of the first transistor TR**1**. Since a current flows from the source to and drain terminal in the first transistor TR**1**, the first output buffer **312-1** operates in response to the high state current control signal supplied from the timing controller during the third operation period.

[0100] FIG. **12***b* is a view of another output buffer in the data driver of FIG. **11**. A first output buffer **312-1** includes an operational amplifier **316**, two transistors TR**3** and TR**4**, two switches SW**9** and SW**10**, and an inverter **318**.

[0101] During the first and second operation periods, the timing controller supplies a low state current control signal to the ninth switch SW**9** and the inverter **318**. The low state current control signal supplied to the inverter **318** is converted into a high signal, and supplied to the tenth switch SW**10**.

[0102] Accordingly, the ninth switch SW**9** is turned off by the low state current control signal, and the tenth switch SW**10** is turned on by the high state current control signal.

[0103] When the tenth switch SW**10** is turned on, a ground voltage GND is supplied to a gate terminal of the fourth transistor TR**4**. The ground voltage GND is also supplied to a source terminal of the fourth transistor TR**4**. A voltage Vg supplied to the gate terminal of the fourth transistor TR**4** and a voltage Vs supplied to the source terminal of the fourth transistor TR**4** become equal as the ground voltage GND.

[0104] Due to characteristics of the fourth transistor TR**4**, when a voltage Vg supplied to the gate terminal of the fourth transistor TR**4** and a voltage Vs supplied to the source terminal of the fourth transistor TR**2** become equal, a current does not flow between the source and drain terminals in the fourth transistor TR**4**. Therefore, the first output buffer **312-1** does not operate during the first and second operation periods.

[0105] The timing controller supplies a high state current control signal to the ninth switch SW**9** and the inverter **318** during the third operation period. The high state current control signal supplied to the inverter **318** is converted into a low signal, and then supplied to the tenth switch SW**10**.

[0106] Accordingly, the ninth switch SW**9** is turned on by the high state current control signal, and the tenth switch SW**10** is turned off by the low state current control signal.

[0107] When the ninth switch SW**9** is turned on, a bias voltage is supplied to the gate terminal of the fourth transistor TR**4**. A ground voltage GND is supplied to the source terminal of the fourth transistor TR**4**. The bias voltage is different from the ground voltage GND.

[0108] A voltage Vg supplied to the gate terminal of the fourth transistor TR**4** is the bias voltage, and a voltage Vs supplied to the source terminal is the ground voltage GND.

[0109] Consequently, since the voltage Vg supplied to the gate terminal of the fourth transistor TR**4** is different from the voltage Vs supplied to the source terminal of the fourth transistor TR**4**, a current flows between the source and drain terminals in the fourth transistor TR**4**.

[0110] Thus, when the low state current control signal is supplied from the timing controller to the output buffers during the first and second operation periods, the output buffers do not operate.

[0111] When the high state current control signal supplied from the timing controller to the output buffers, the output buffers operate during the third operation period. Since output buffers do not operate during the first and second operation periods, power consumption decreases and less heat is generated by elements inside the output buffers.

[0112] As described above, the LCD does not operate an output terminal of a data driver using a current control signal during at least one period of a charge share period and a pre-charge period, and operates the output terminal of the data driver only during a data output period. Thus, current consumption is minimized and also power consumption can be reduced, and heat generated from elements in the data driver can be reduced.

[0113] The LCD operates an output terminal of the data driver only when displaying of an actual image. Therefore, a current consumption is reduced and thus power consumption is reduced and a heat generated from the elements can be reduced.

[0114] Although the present invention has been explained by way of the examples described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the examples, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display device comprising:

a liquid crystal panel having a plurality of gate lines and data lines;

a data driver supplying a data voltage to the plurality of data lines;

a controller generating a current control signal to control an output terminal of the data driver so that the output terminal operates during a first period in which data is outputted from the data driver, and the output terminal does not operate during a second period in which data is not outputted from the data driver; and

a gate driver supplying a scan signal to the plurality of the gate lines.

2. The liquid crystal display device according to claim **1**, wherein the output terminal comprises:

a plurality of output buffers corresponding to the plurality of data lines.

3. The liquid crystal display device according to claim **2**, wherein the output terminal comprises:

a current source supplying a driving current to drive the plurality of output buffers.

4. The liquid crystal display device according to claim **1**, further comprising a current source supplying a driving current to drive the plurality of output buffers.

5. The liquid crystal display device according to claim 3, wherein the current control signal is supplied to the current source.

6. The liquid crystal display device according to claim 3, wherein the current source is turned on when the current control signal is a first current control signal in which data is output from the data driver, and the current source is turned off when the current control signal is a second current control signal in which data is not output from the data driver.

7. The liquid crystal display device according to claim 1, wherein the second period includes at least one of a charge-share period and a pre-charge period.

8. The liquid crystal display device according to claim 3, wherein the current source is supplied a current control signal controlling the current source.

9. A liquid crystal display device comprising:

a liquid crystal panel having a plurality of gate lines and data lines;

a data driver supplying a data voltage to the plurality of data lines;

a controller generating a current control signal to control a current source of the data driver so that the current source operates during a first period in which data is outputted from the data driver, and the current source does not operate during a second period in which data is not outputted from the data driver; and

a gate driver supplying a scan signal to the plurality of gate lines.

10. The liquid crystal display device according to claim 9, wherein the data driver comprises:

a plurality of output buffers corresponding to the plurality of data lines.

11. The liquid crystal display device according to claim 9, wherein the current source supplies a driving current to drive the plurality of output buffers.

12. The liquid crystal display device according to claim 10, wherein the current control signal is supplied to the output buffers.

13. The liquid crystal display device according to claim 10, wherein a switching element is disposed between the current source and the output buffer.

14. The liquid crystal display device according to claim 10, wherein a switching element is disposed between the current source and the controller.

15. The liquid crystal display device according to claim 10, wherein the current source includes a switching element.

16. The liquid crystal display device according to any one of claims 11-13, wherein the switching element controls the operation of the out buffers.

17. The liquid crystal display device according to any one of claims 11-13, wherein the switching element includes at least one of a switch, a NMOS transistor, a PMOS transistor, a CMOS transistor, a diode, or a Bipolar transistor.

18. The liquid crystal display device according to claim 16, wherein the switching element is turned on during the first period, and the switching element is turned off during the second period.

19. The liquid crystal display device according to claim 9, wherein the second period includes at least one of a charge-share period and a pre-charge period.

20. The liquid crystal display device according to claim 10, wherein the output buffers are electrically connected to the data lines when the driving current is supplied to the output buffers, and the output buffers are not connected to the data lines when the driving current is not supplied to the output buffers.

21. The liquid crystal display device according to claim 10, wherein the output buffers operate when the current control signal is a first current control signal and data is output from the data driver, and the output buffers does not operate when the current control signal is a second current control signal and data is not output from the data driver.

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申请(专利权)人(译)	LG飞利浦LCD CO.，LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO.，LTD.		
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摘要(译)

描述了具有降低的功耗的LCD。 LCD包括具有多条栅极线和数据线的液晶面板，向多条数据线提供数据电压的数据驱动器，产生电流控制信号的控制器，以控制数据驱动器的输出端子，使得输出端子在数据从数据驱动器输出的第一时段期间操作，并且输出端子在没有从数据驱动器输出数据的第二时段期间不操作，并且栅极驱动器向其提供扫描信号。多条栅极线。