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(19) **United States**(12) **Patent Application Publication**
Yamato(10) **Pub. No.: US 2012/0242646 A1**(43) **Pub. Date: Sep. 27, 2012**(54) **DISPLAY PANEL, LIQUID CRYSTAL
DISPLAY, AND DRIVING METHOD****Publication Classification**(51) **Int. Cl.**
G09G 3/36 (2006.01)
G06F 3/038 (2006.01)
(52) **U.S. Cl.** **345/212; 345/87**(75) **Inventor:** **Asahi Yamato**, Osaka-shi (JP)(73) **Assignee:** **SHARP KABUSHIKI KAISHA**,
Osaka-shi, Osaka (JP)(21) **Appl. No.:** **13/514,082**(22) **PCT Filed:** **Sep. 22, 2010**(86) **PCT No.:** **PCT/JP2010/066453**§ 371 (c)(1),
(2), (4) Date: **Jun. 6, 2012**(57) **ABSTRACT**

A display panel includes: a gate driver (13), which supplies gate signals to a plurality of gate bus lines (GL_1 to GL_N); a source driver (12), which supplies source signals to a plurality of source bus lines (SL_1 to SL_M); a plurality of auxiliary capacitor bus lines (CSL_1 to CSL_N); and an auxiliary capacitor driver (14) which, in a single scanning period (T_p) from a point in time where the gate driver (13) supplies a gate bus line (GL_n) with a conducting signal to a point in time where the gate driver (13) supplies the conducting signal next, supplies an auxiliary capacitor bus line (CSL_n) with a rectangular voltage signal ($\#CSL_n$) in synchronization with the conducting signal, the rectangular voltage signal ($\#CSL_n$) being composed of at least a first voltage level (V_{CS1}) and a second voltage level (V_{CS2}) that is different from the first voltage level. This allows the display panel to suppress the phenomenon of blurring of moving images while suppressing increase in manufacturing cost and in power consumption.

(30) **Foreign Application Priority Data**

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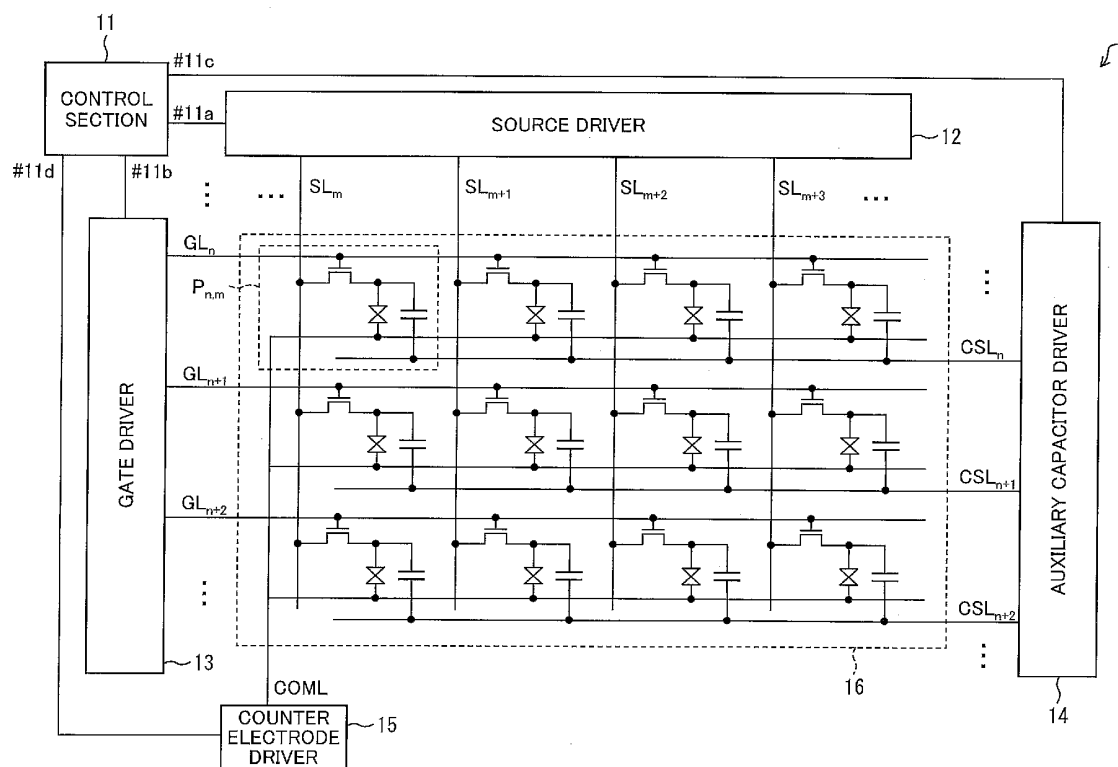


FIG. 1

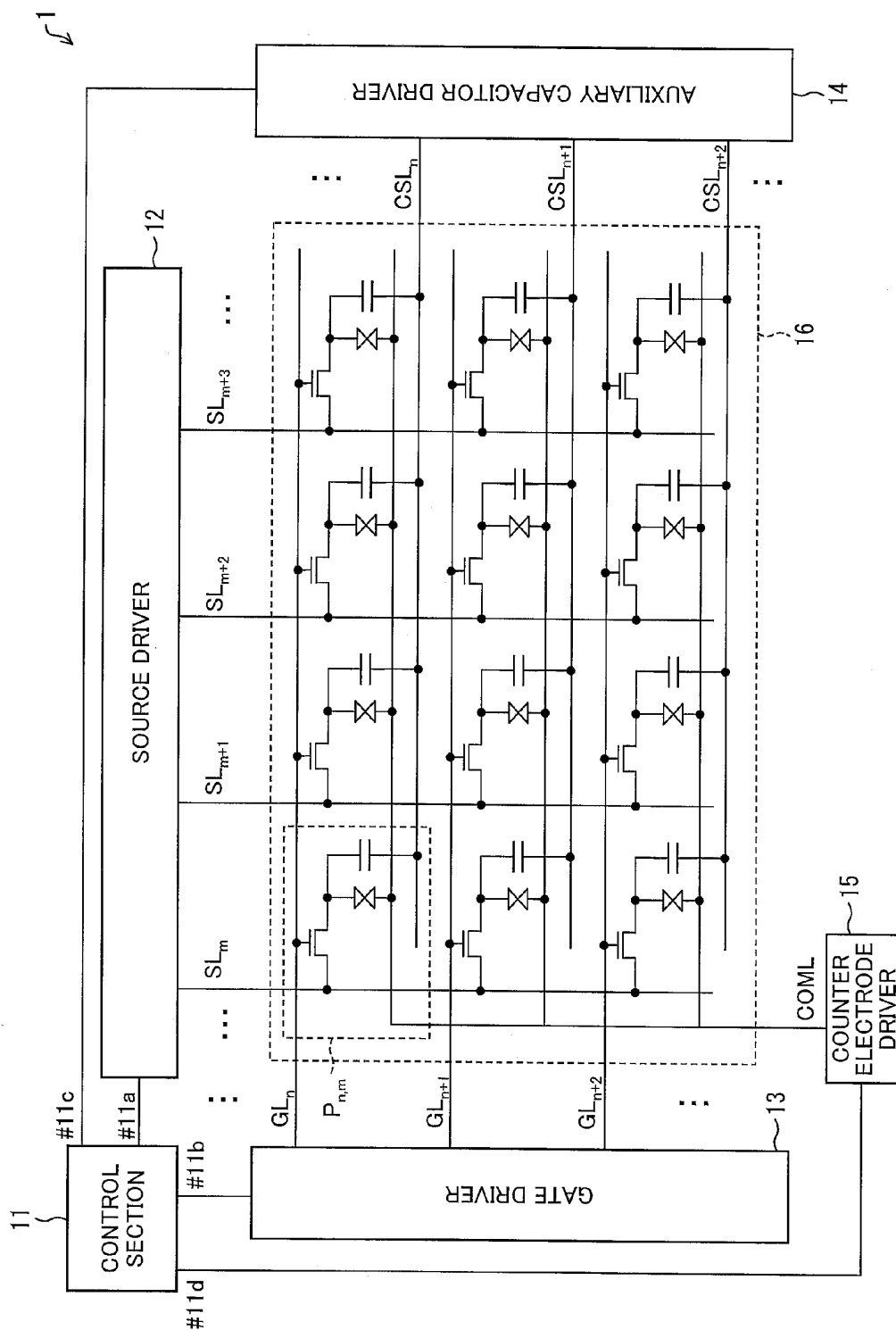


FIG. 2

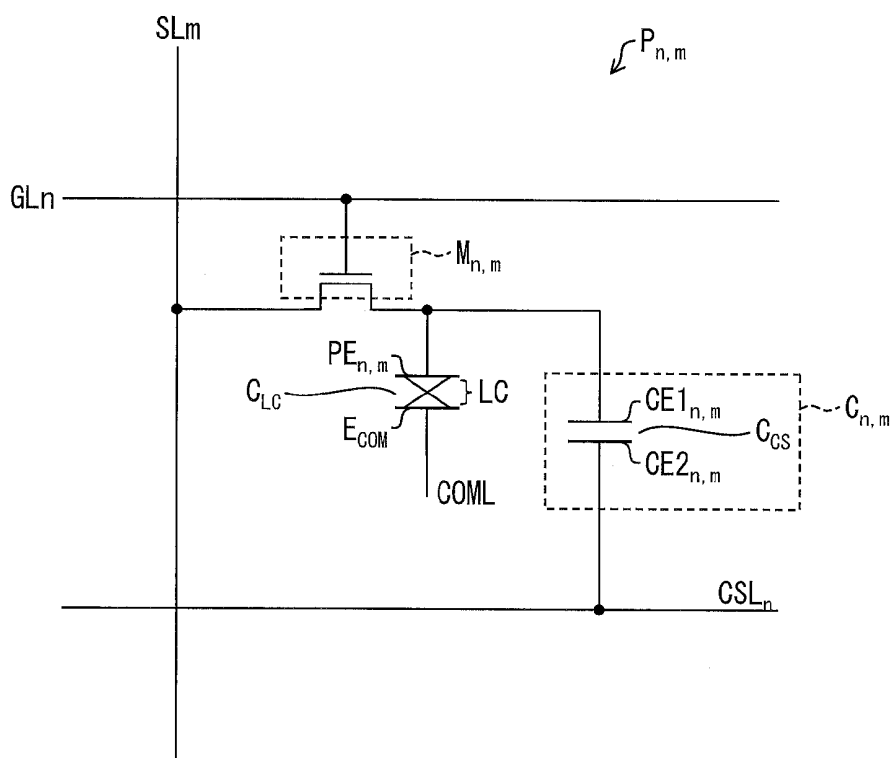


FIG. 3

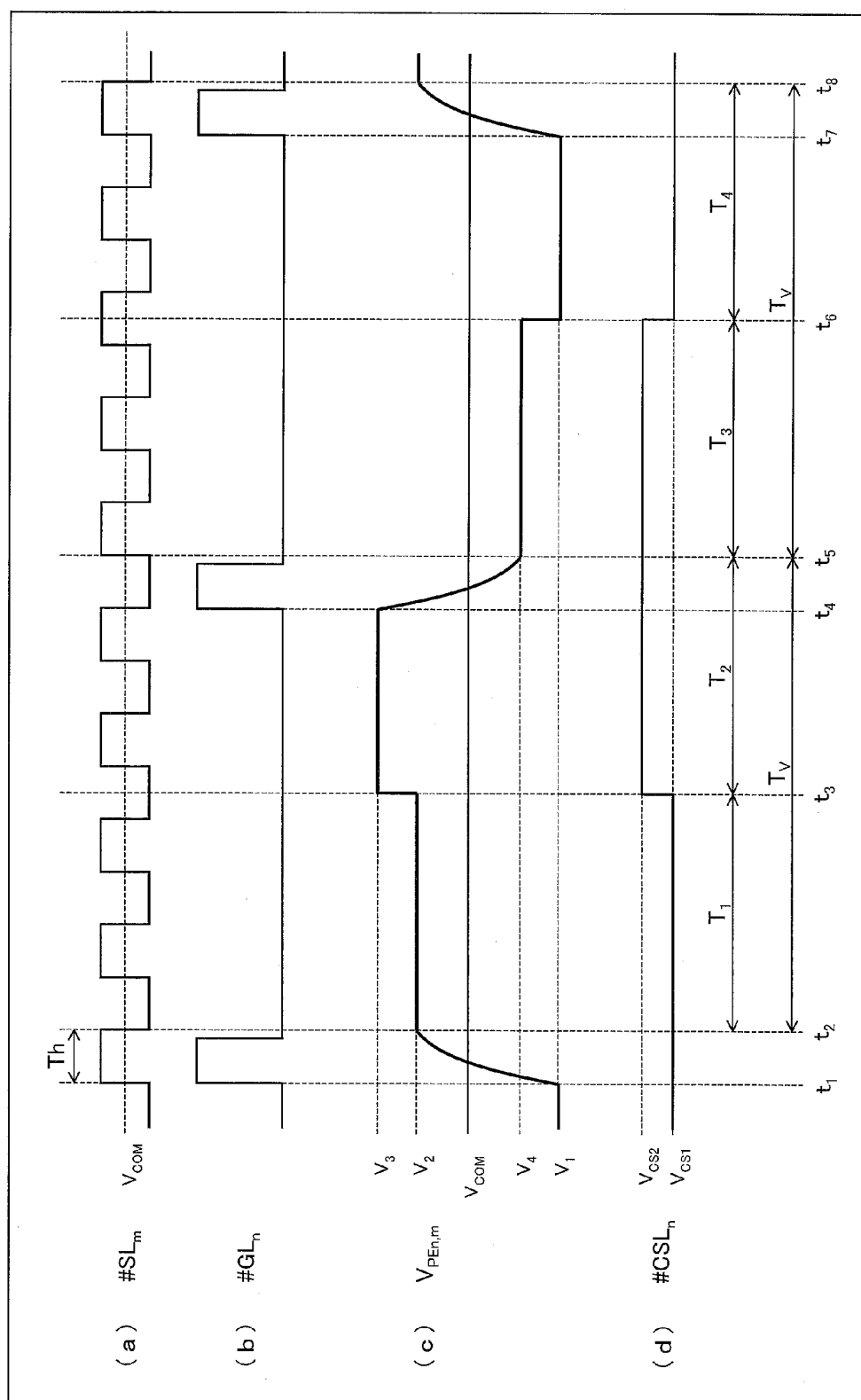


FIG. 4

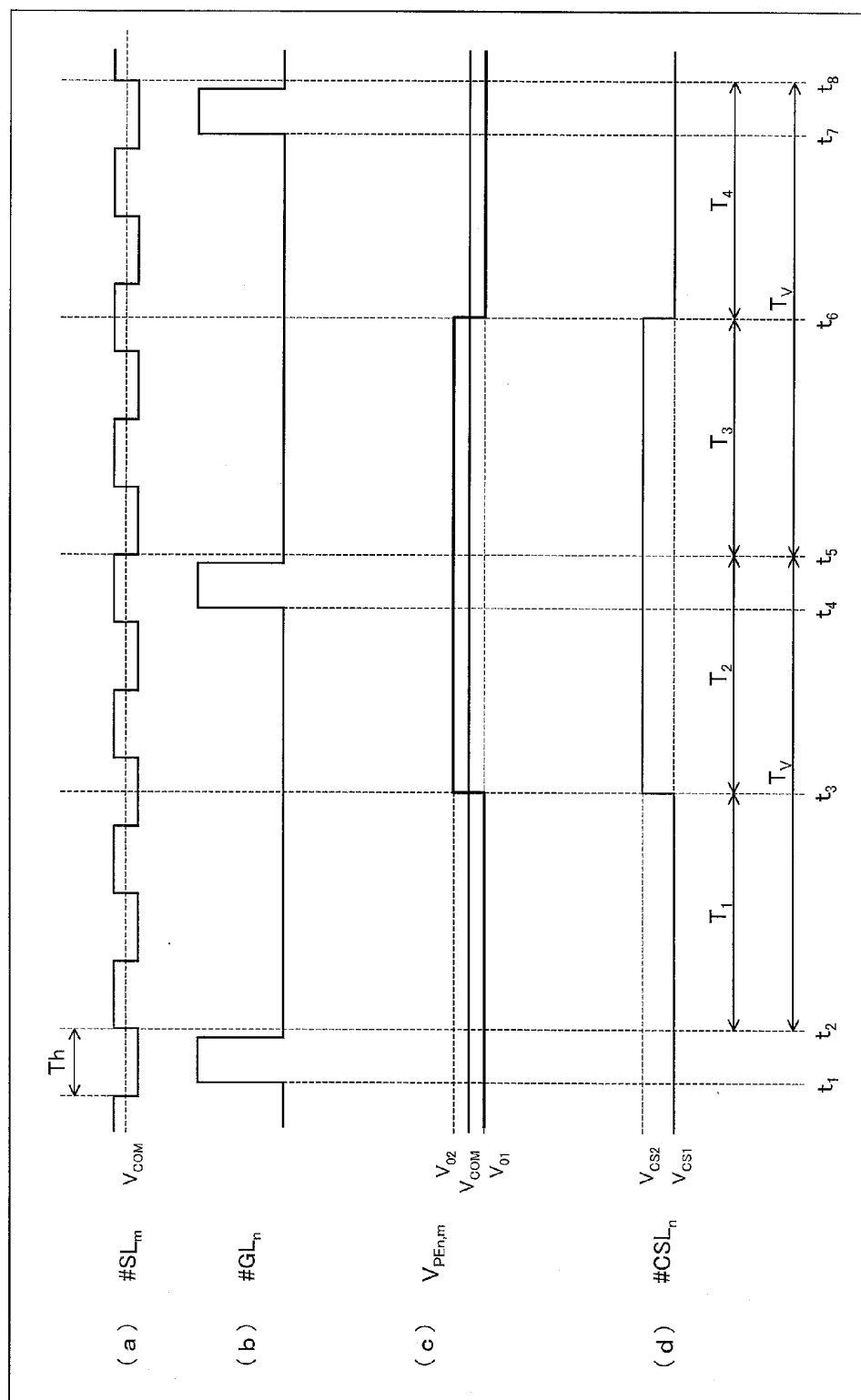


FIG. 5

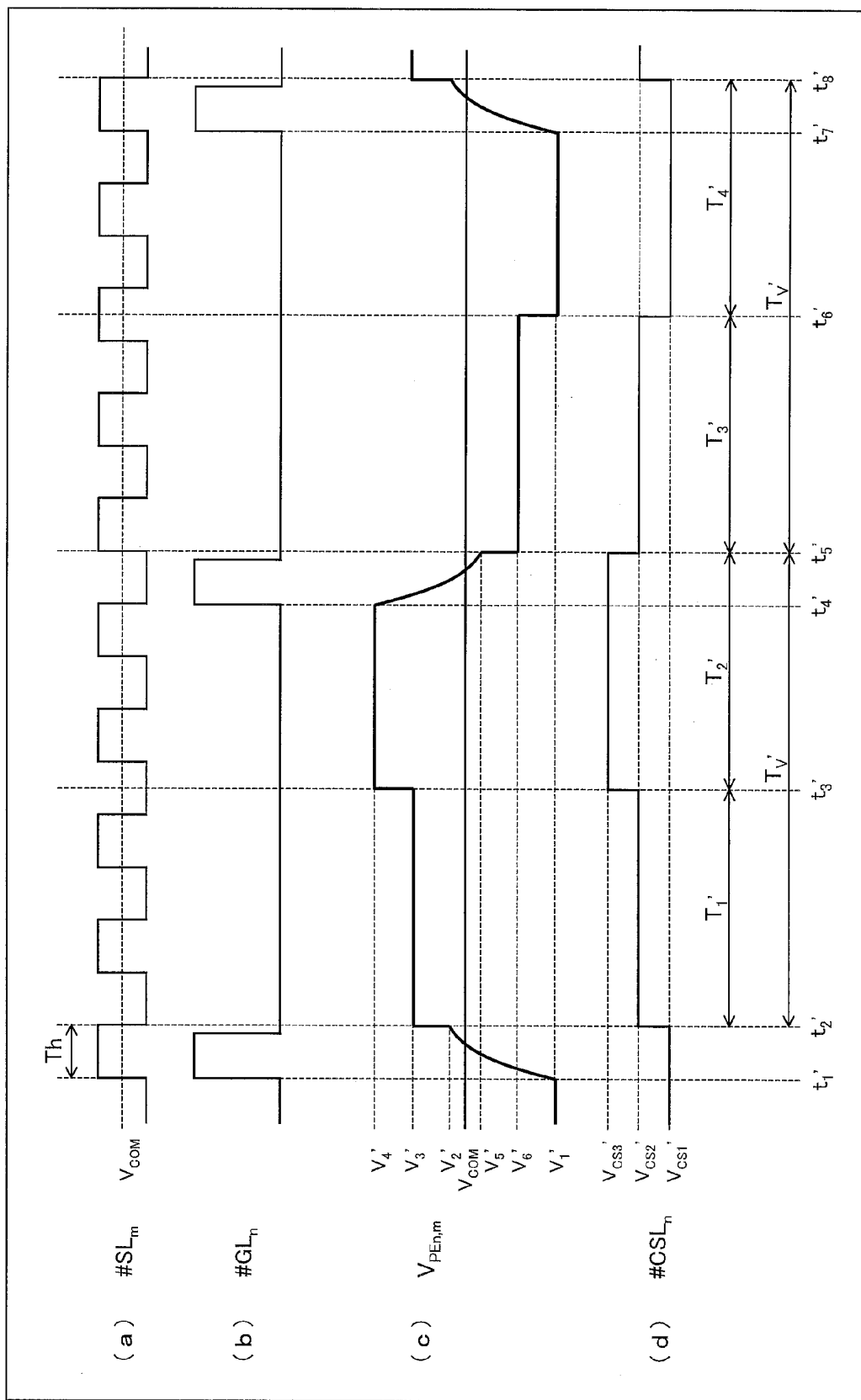


FIG. 6

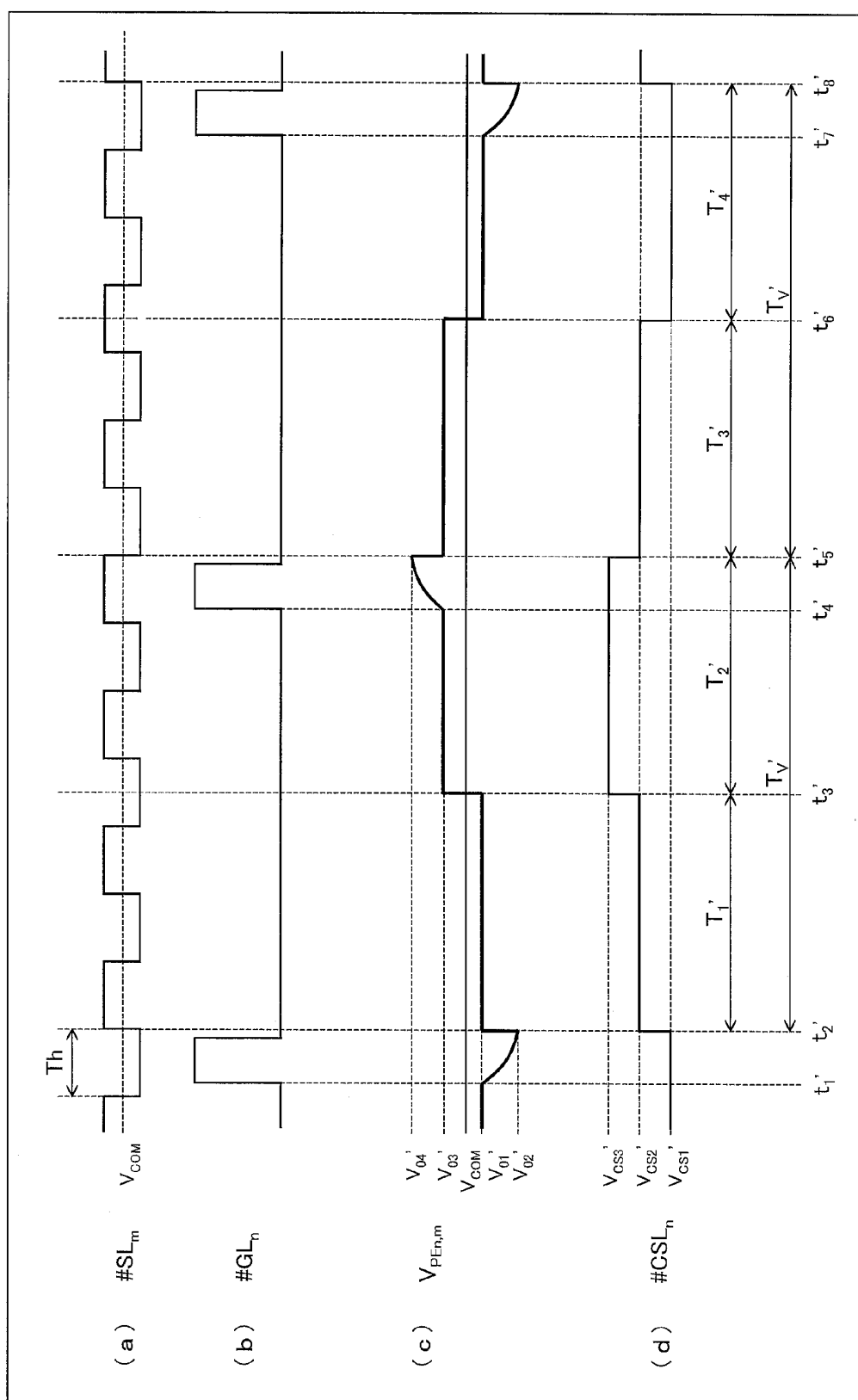


FIG. 7

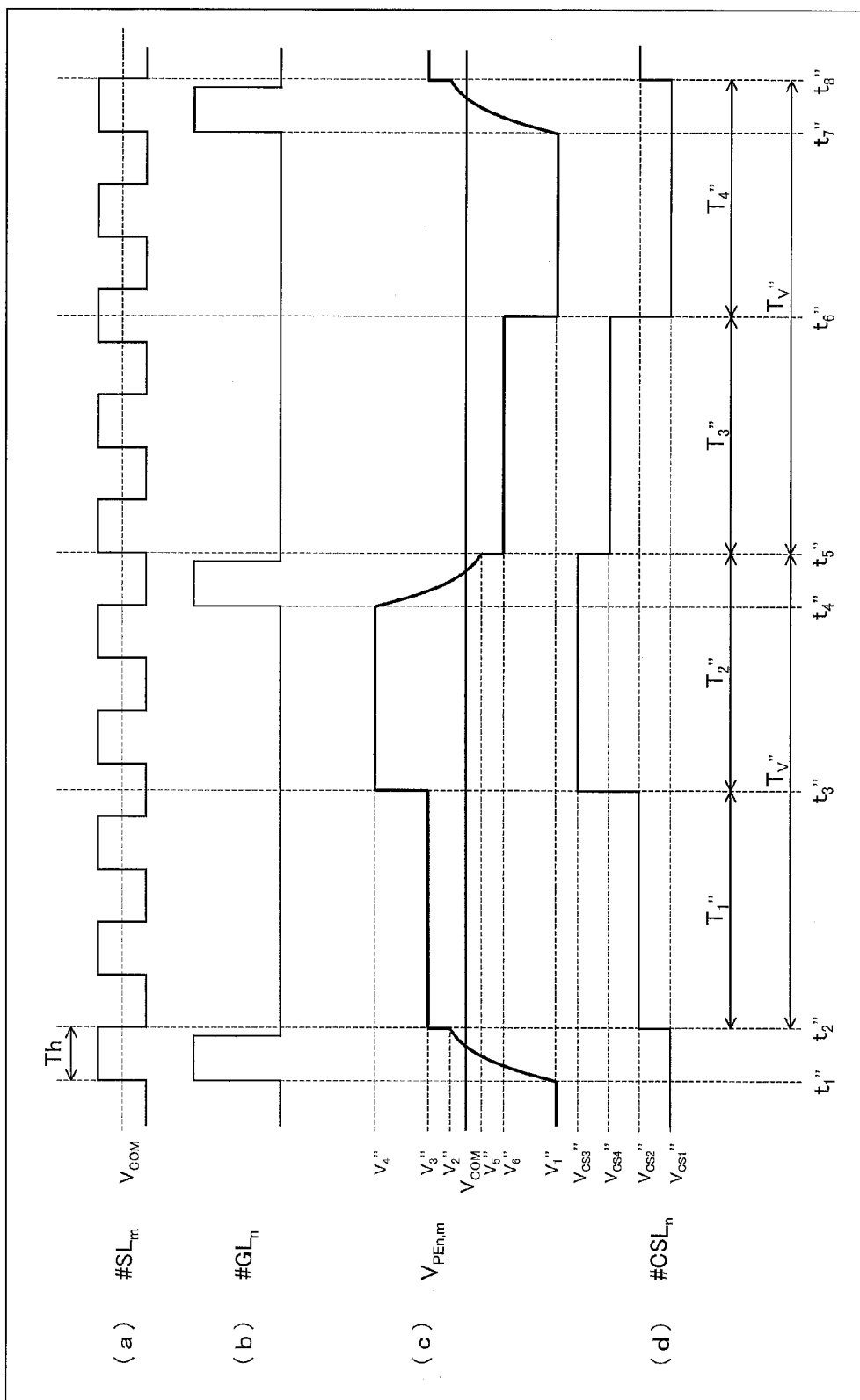


FIG. 8

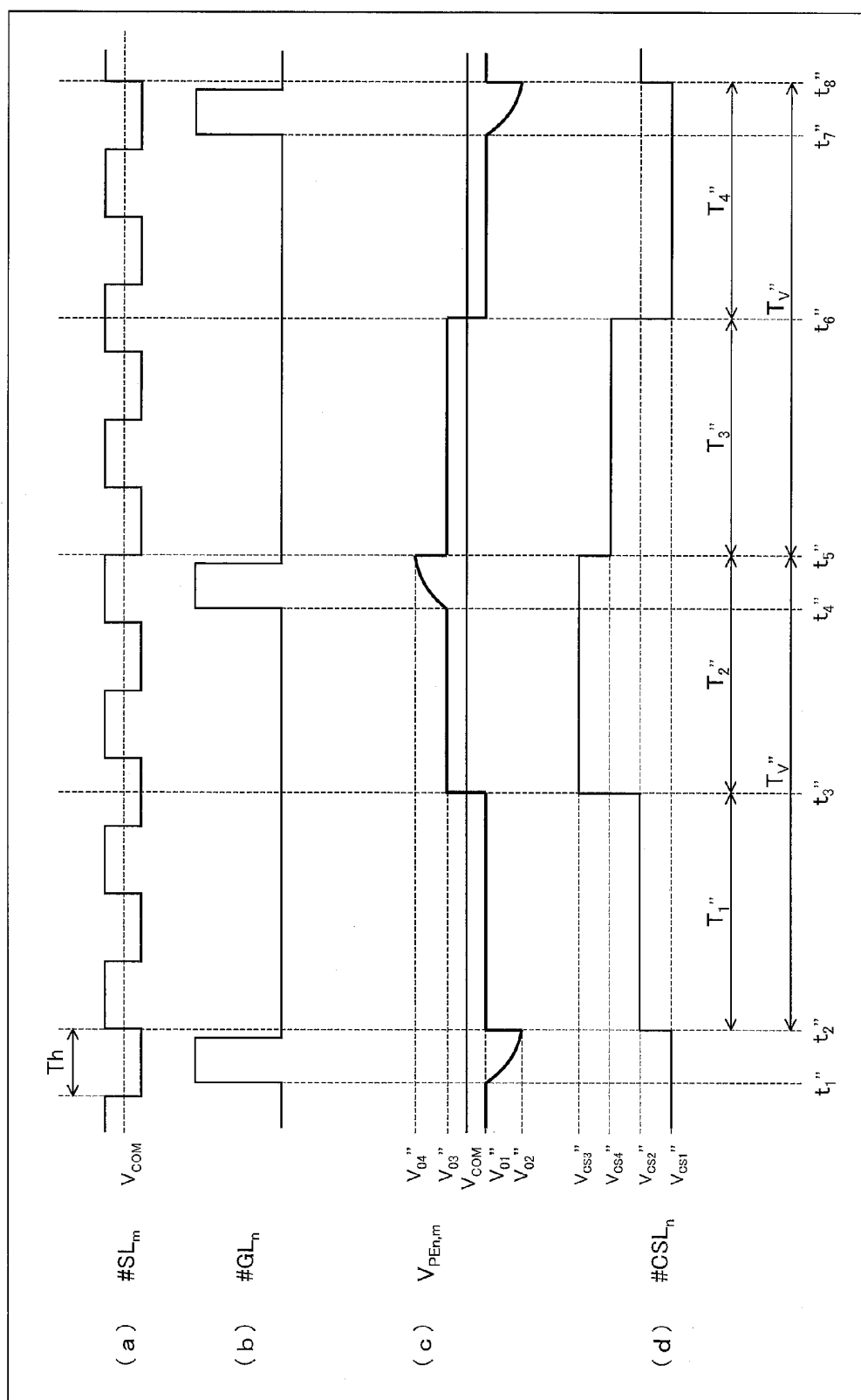


FIG. 9

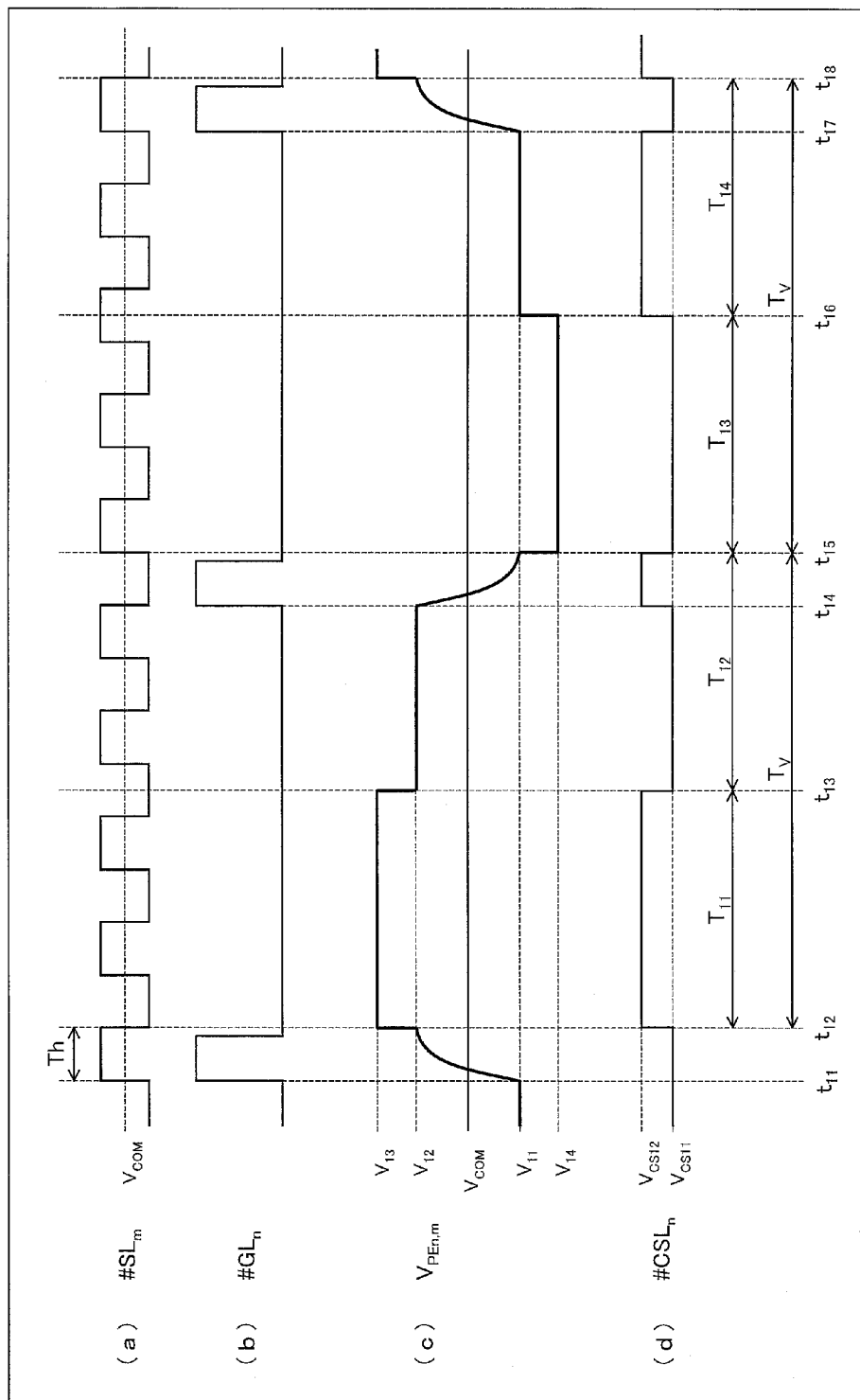


FIG. 10

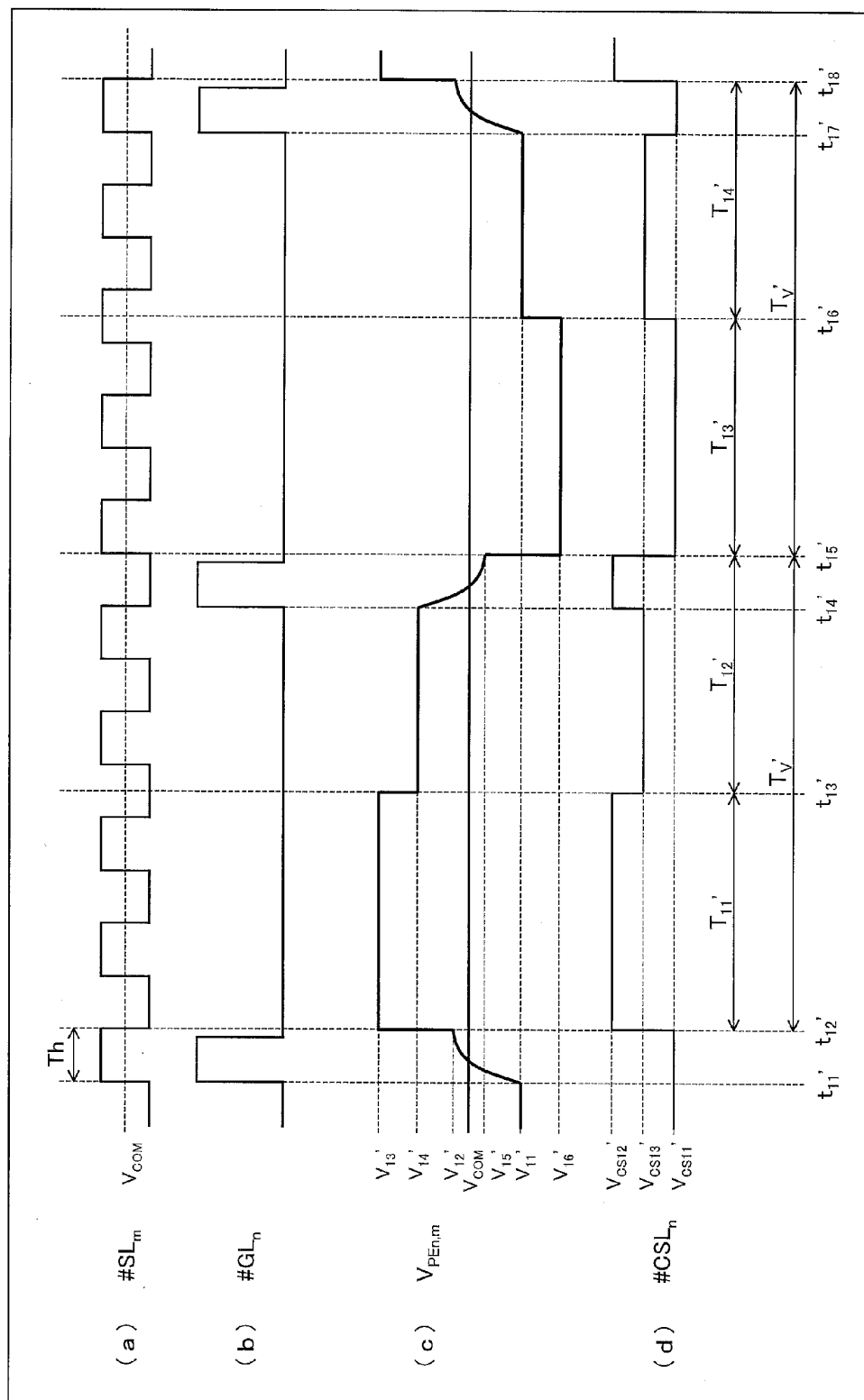


FIG. 11

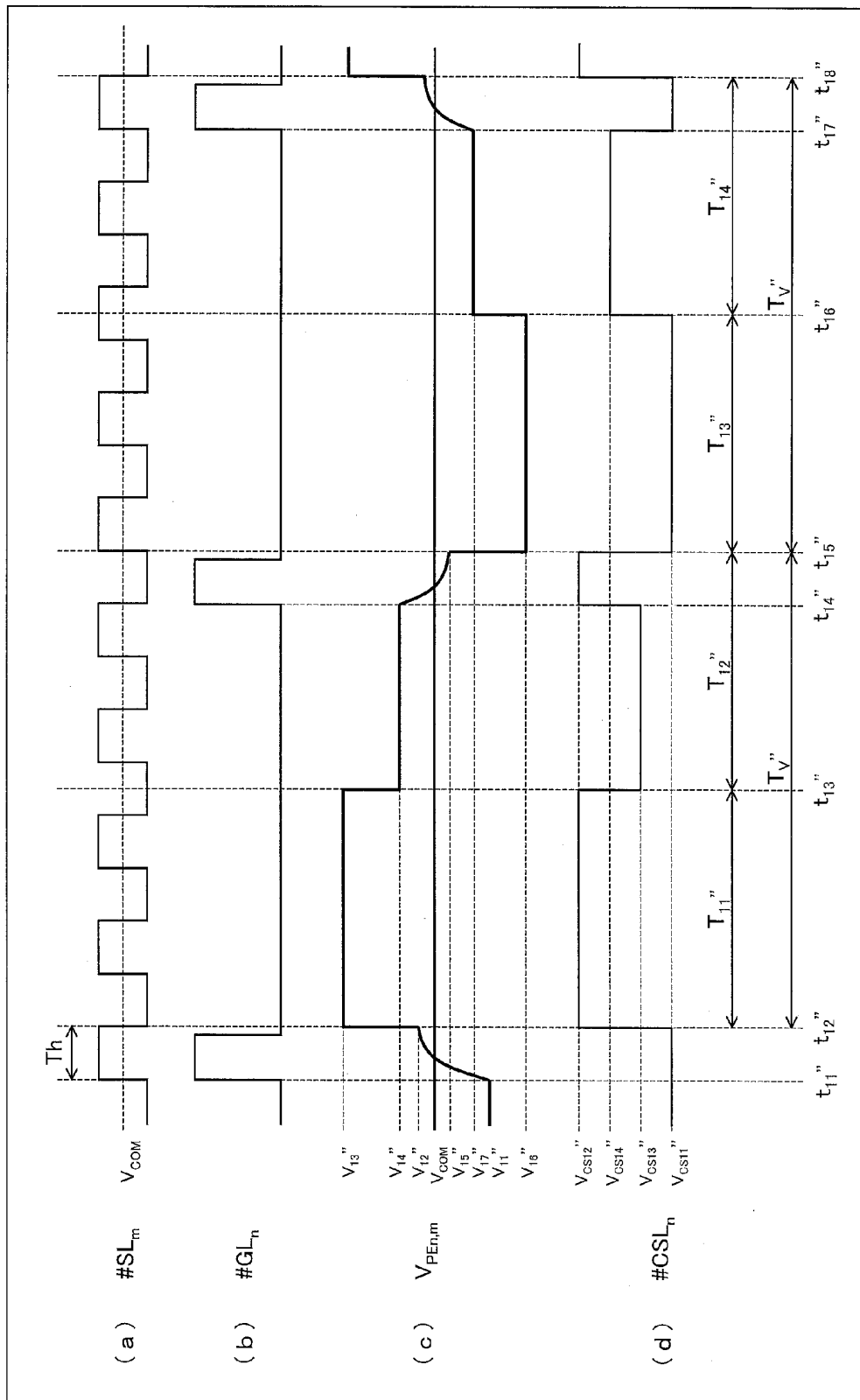


FIG. 12

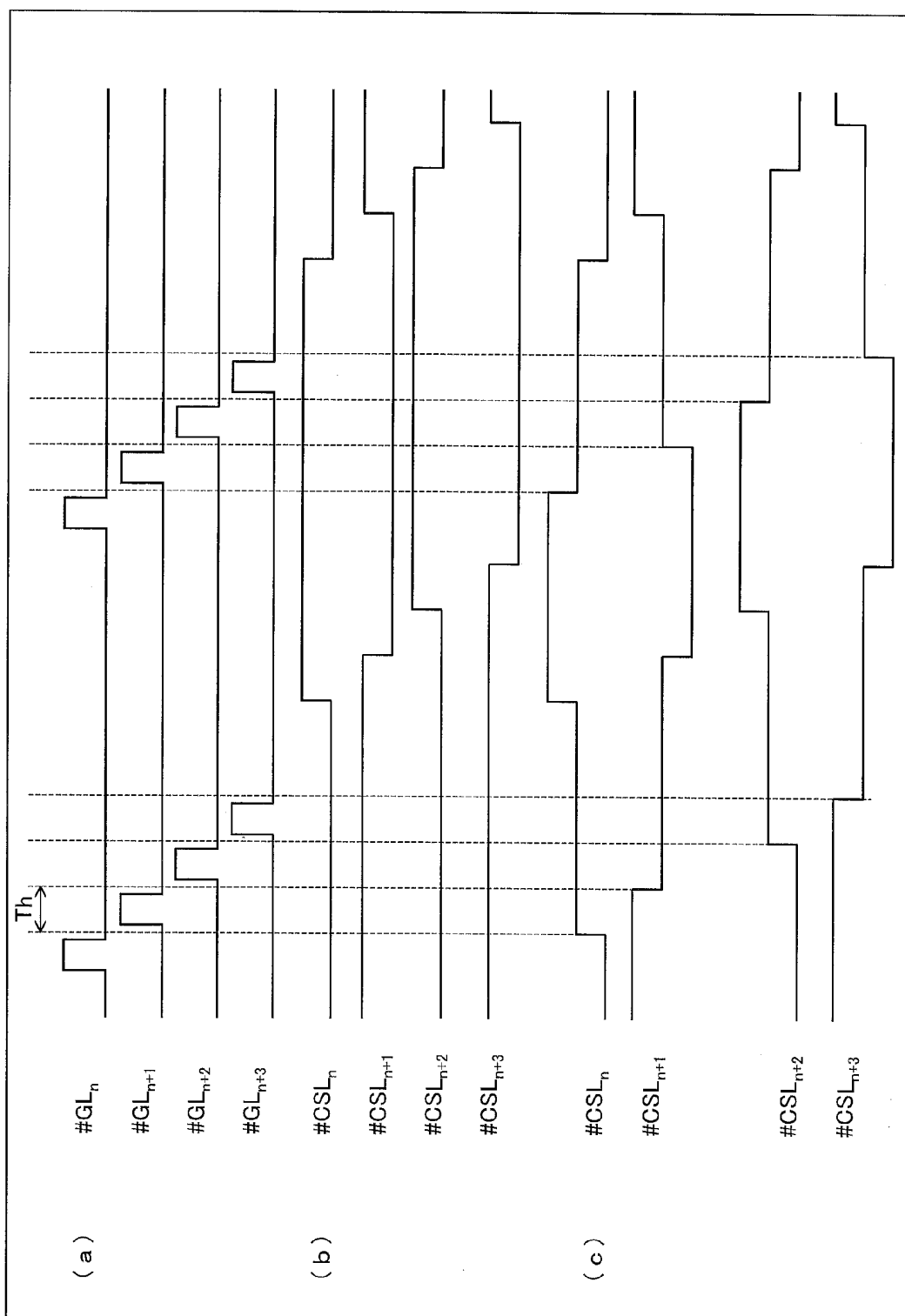


FIG. 13

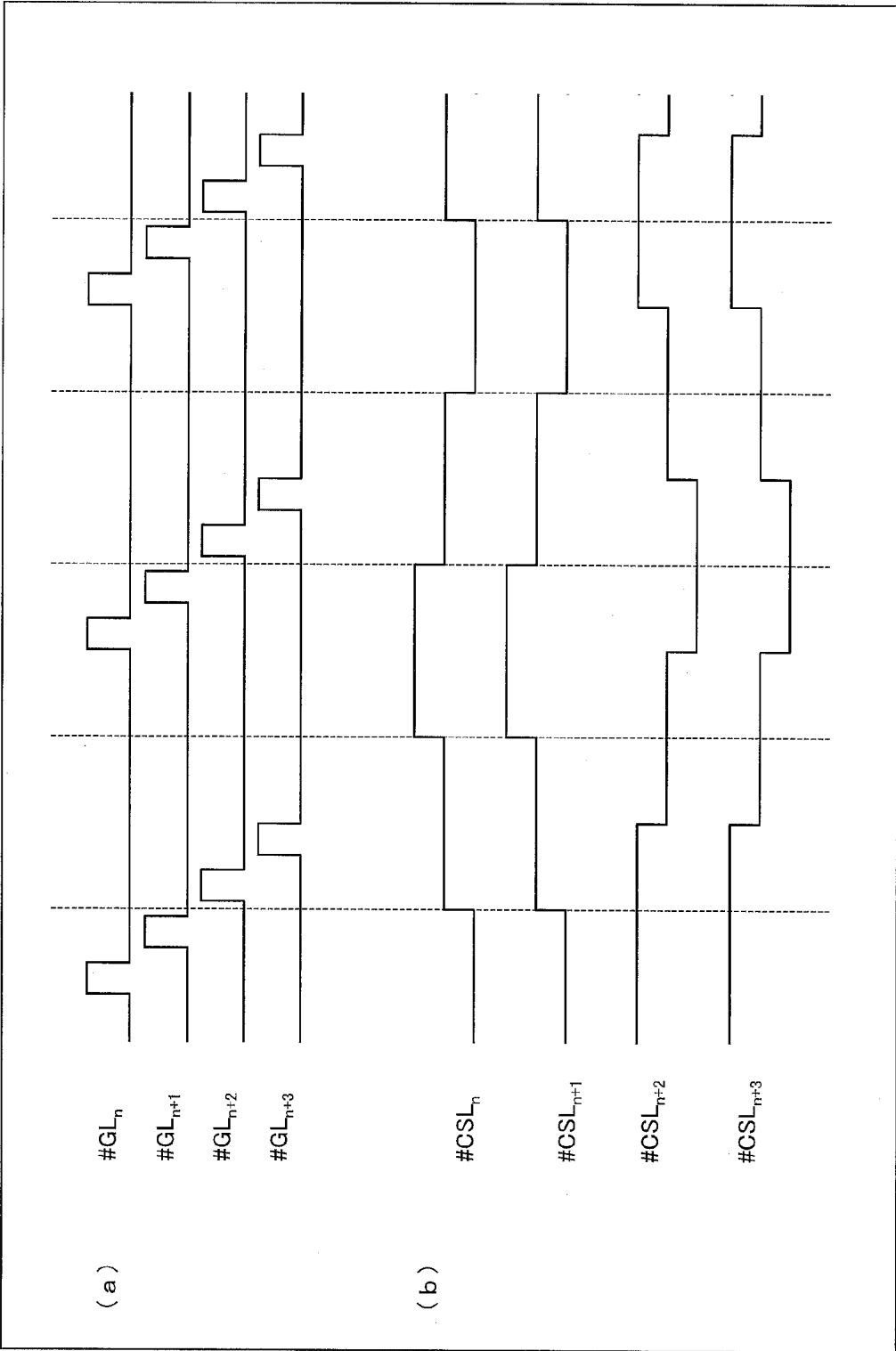


FIG. 14

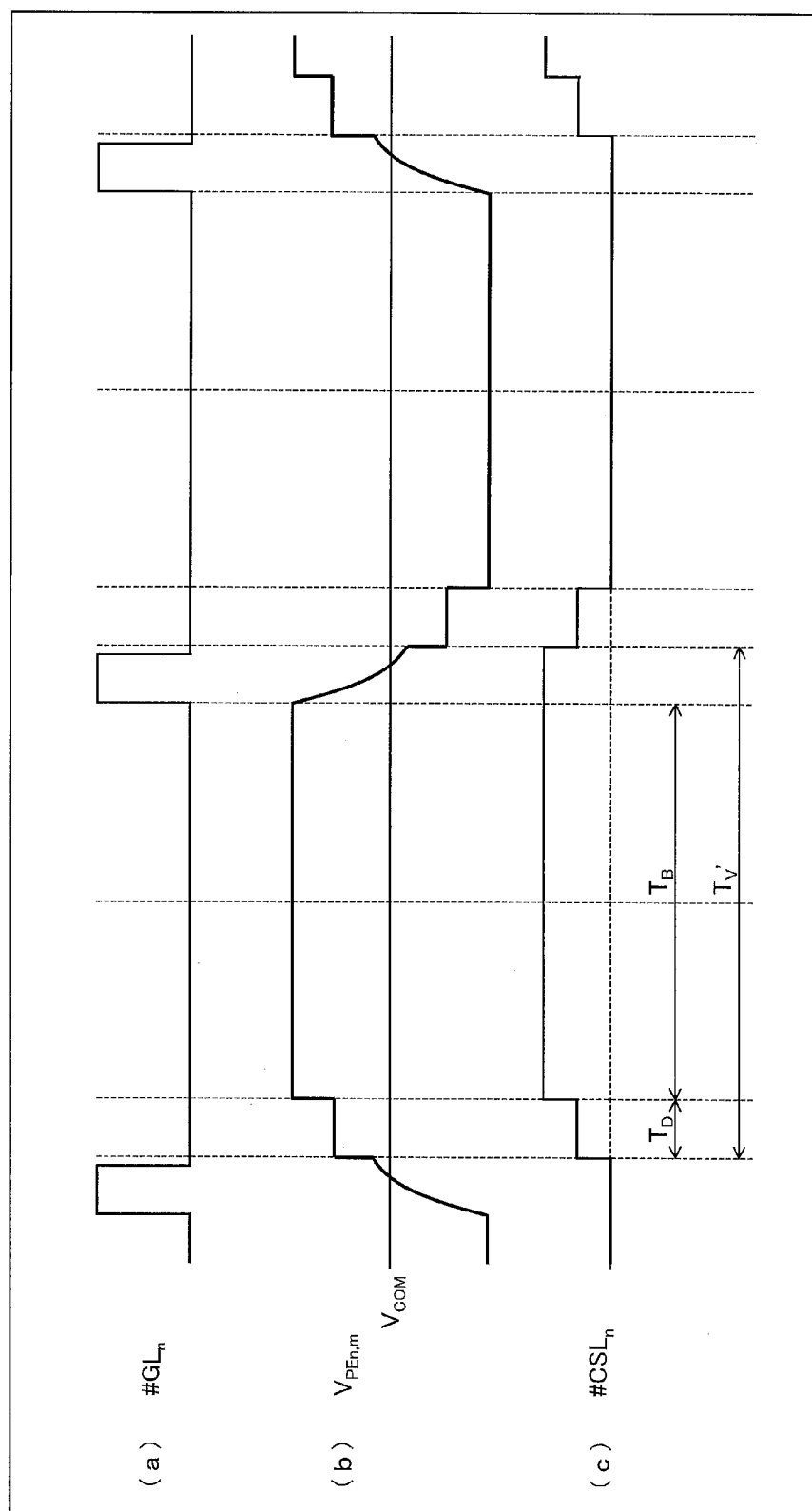


FIG. 15

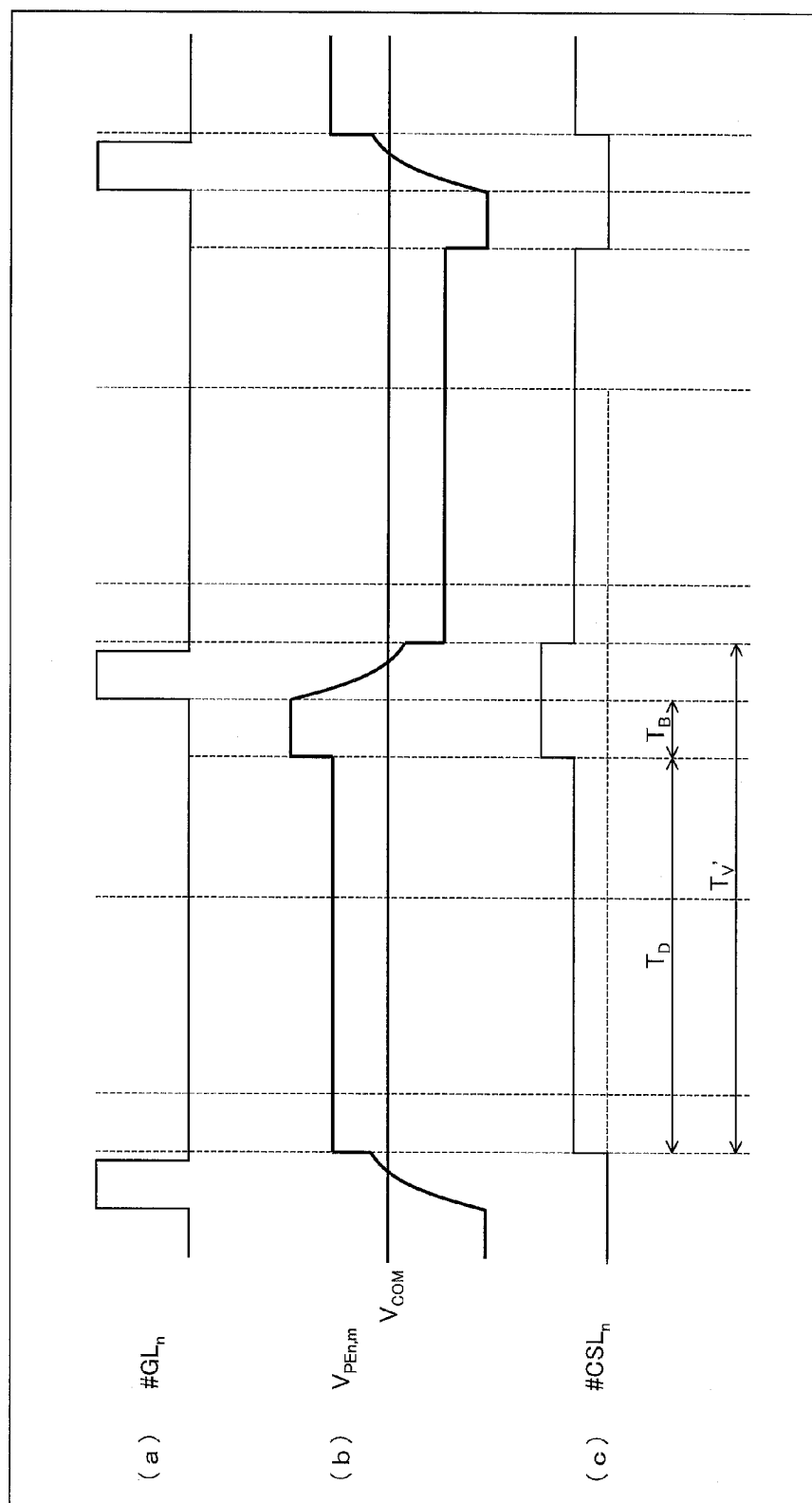


FIG. 16

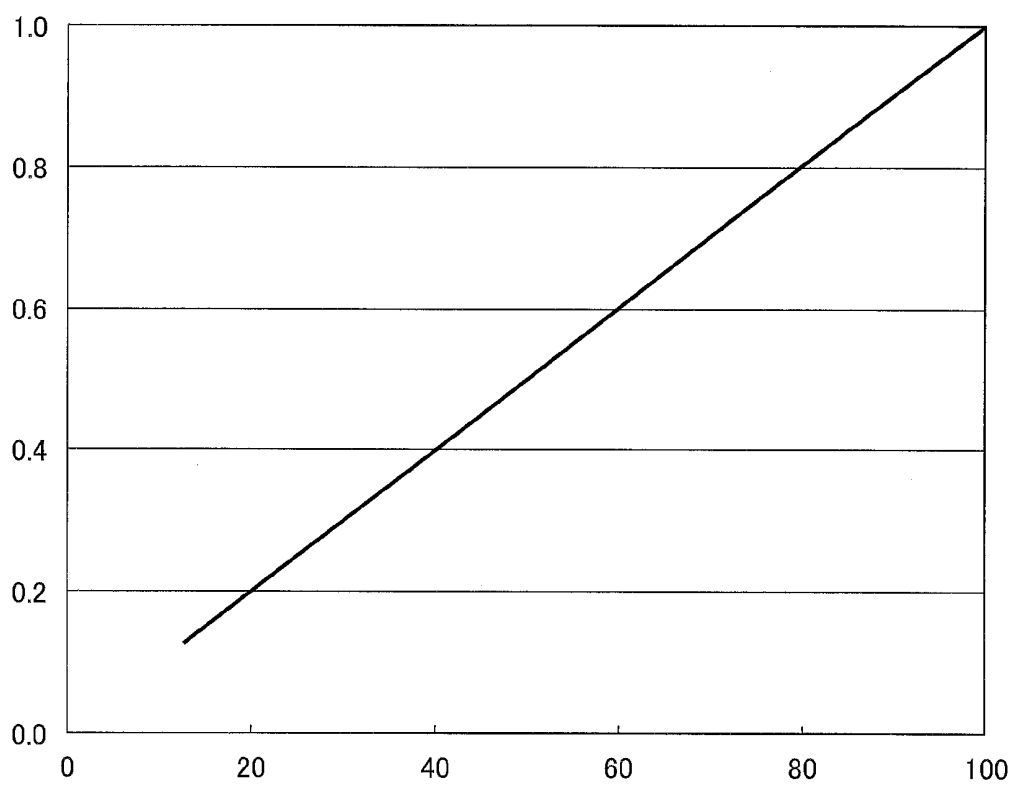


FIG. 17

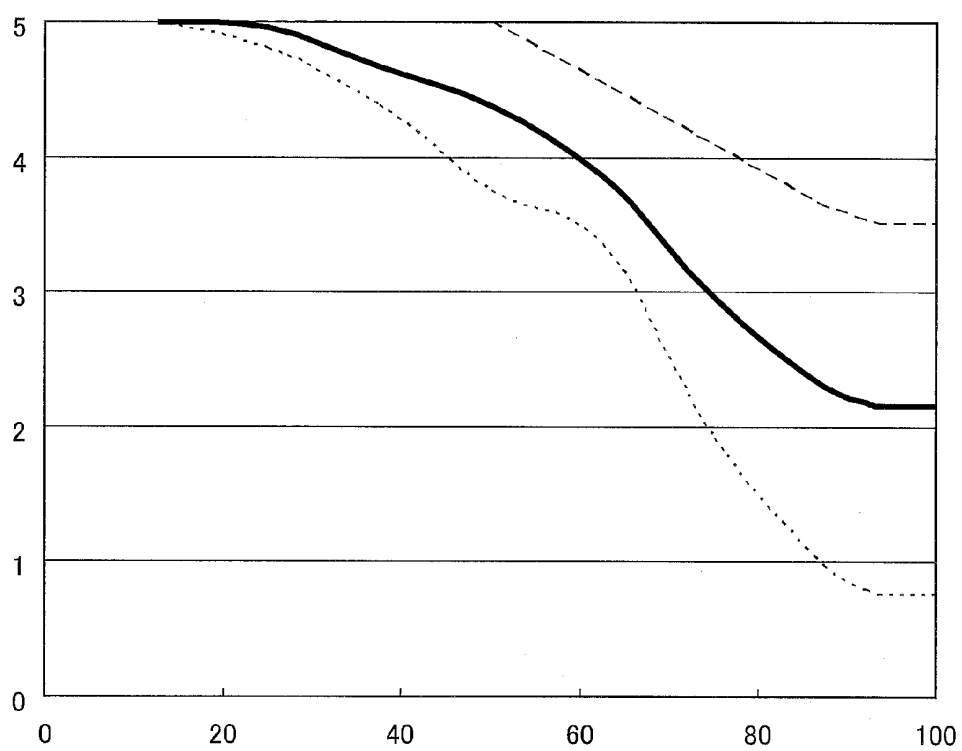


FIG. 18

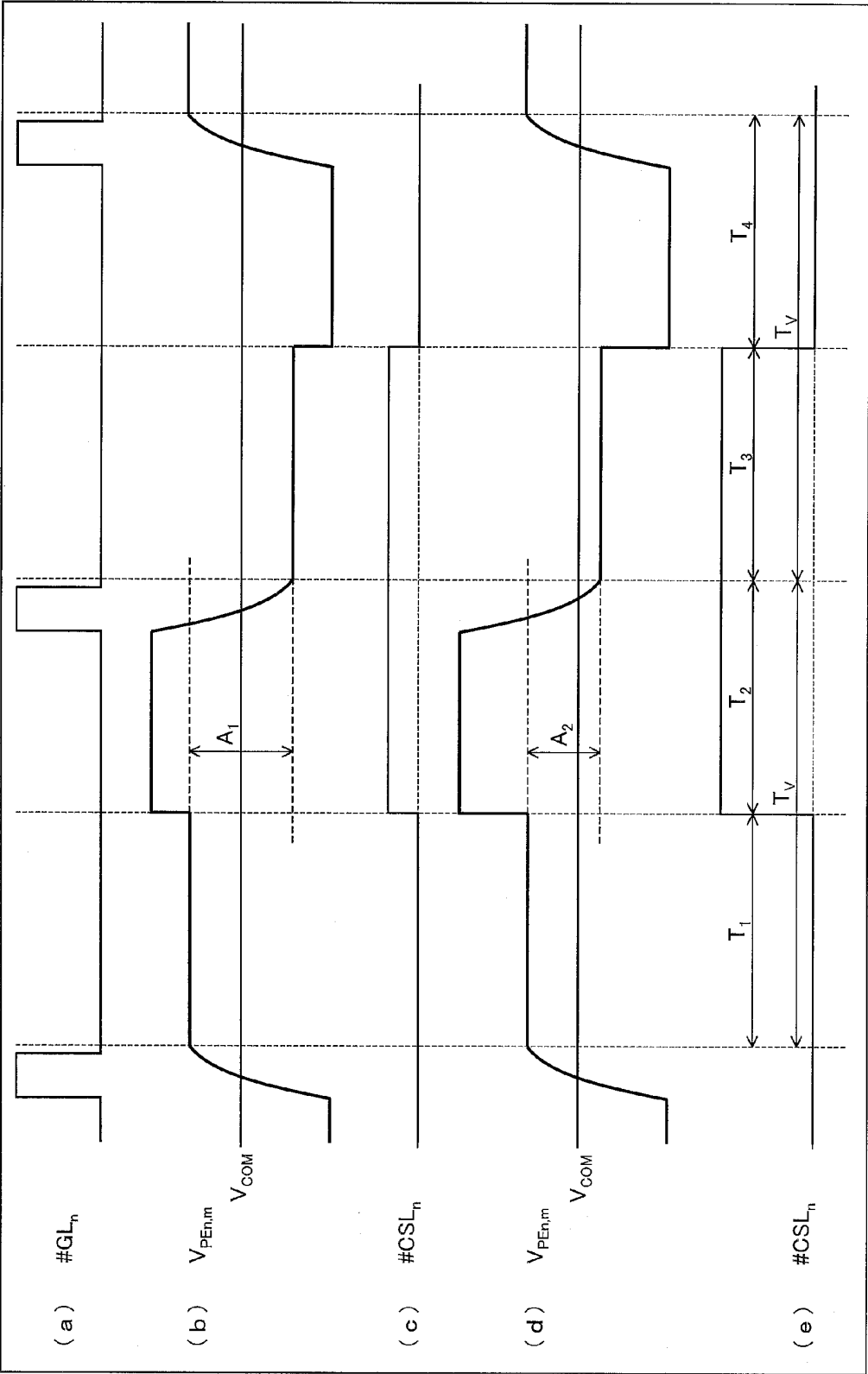


FIG. 19

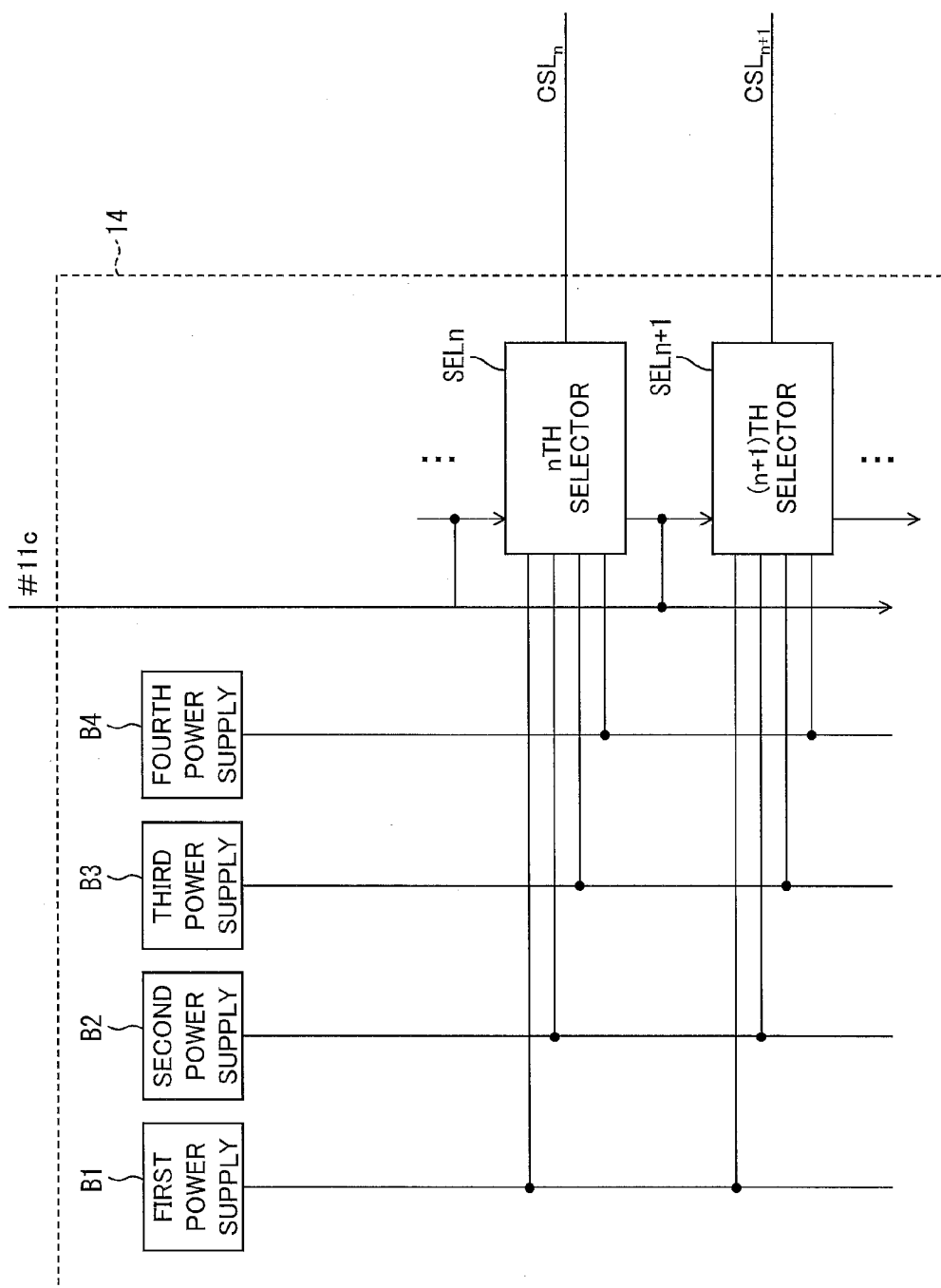


FIG. 20

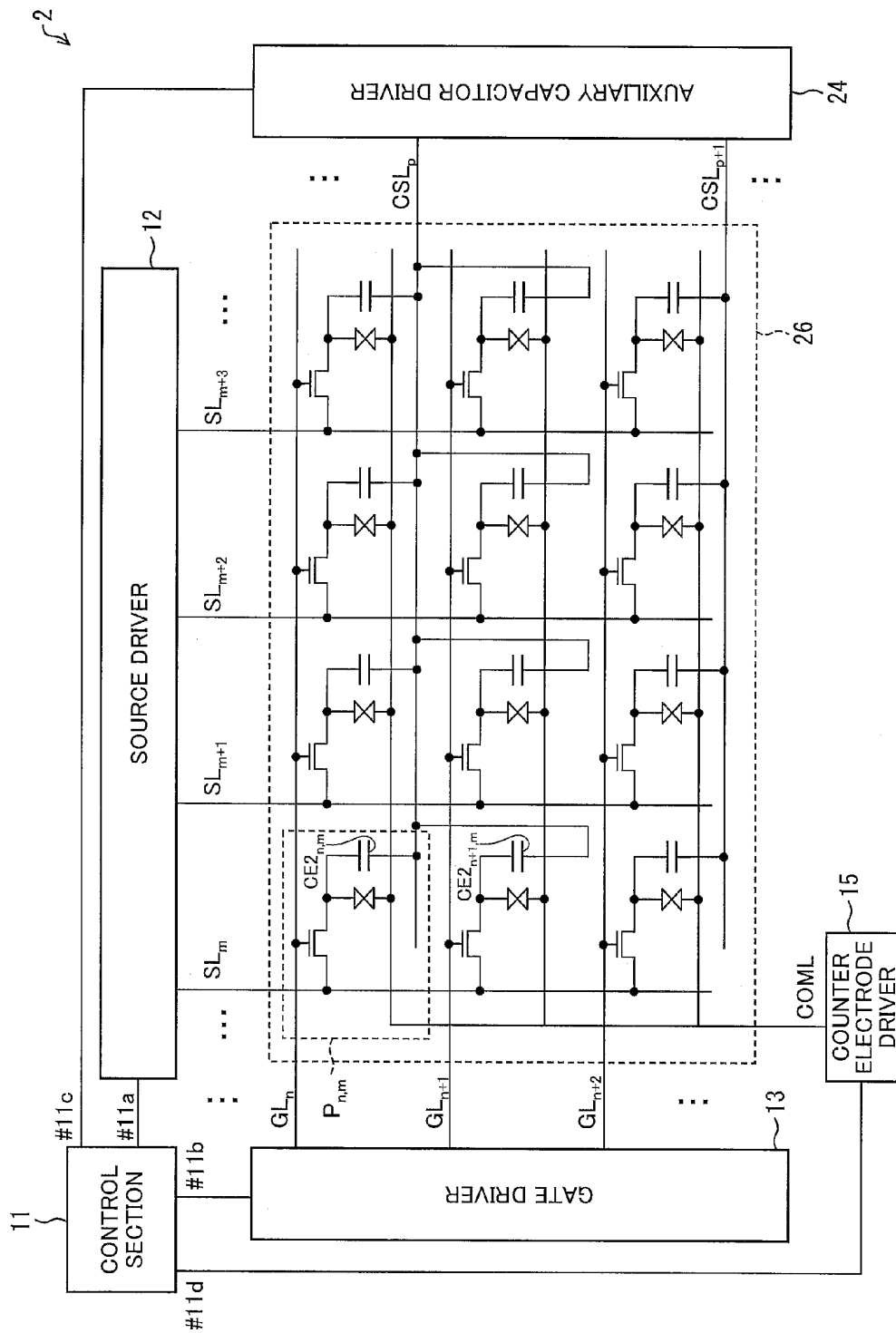
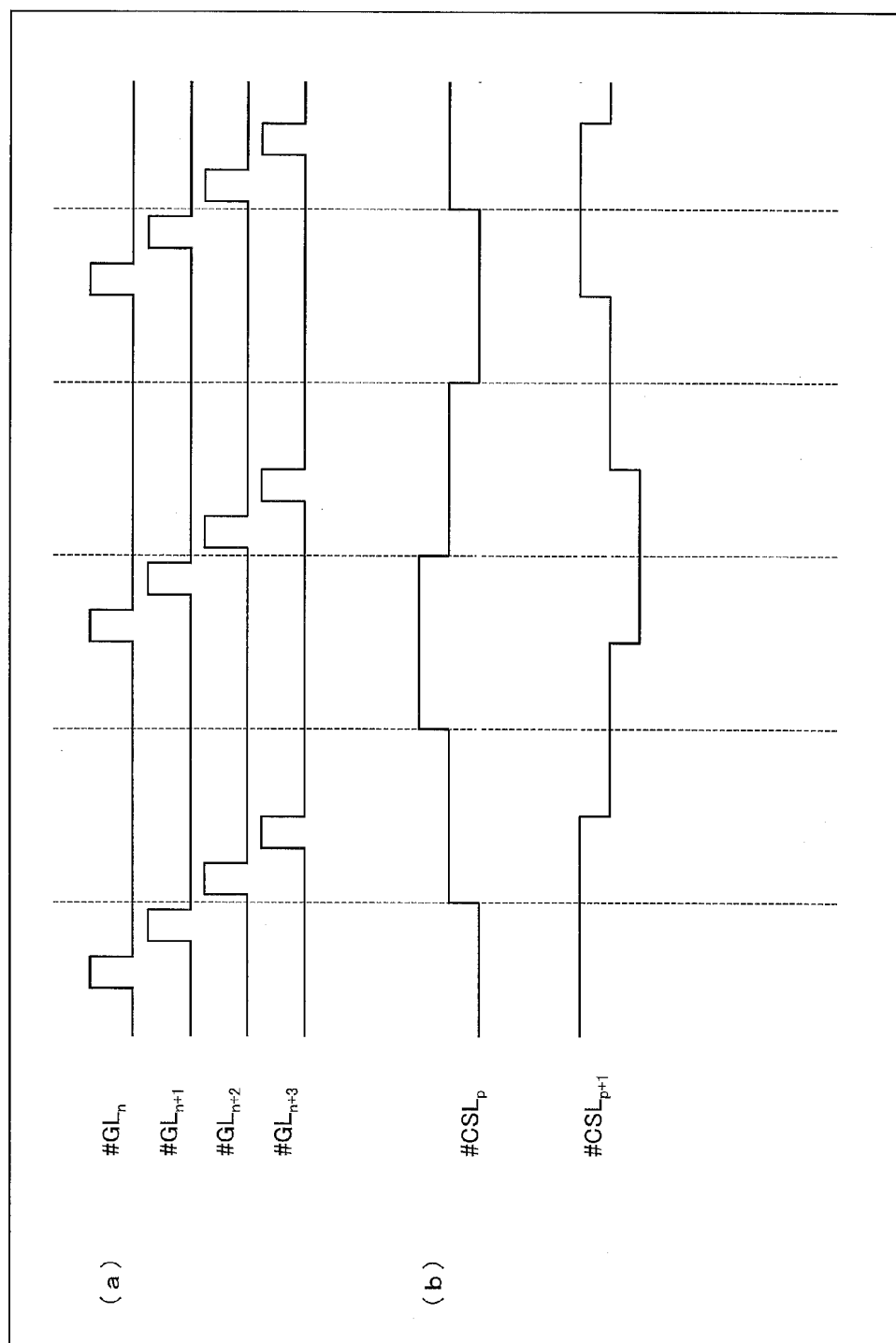


FIG. 21



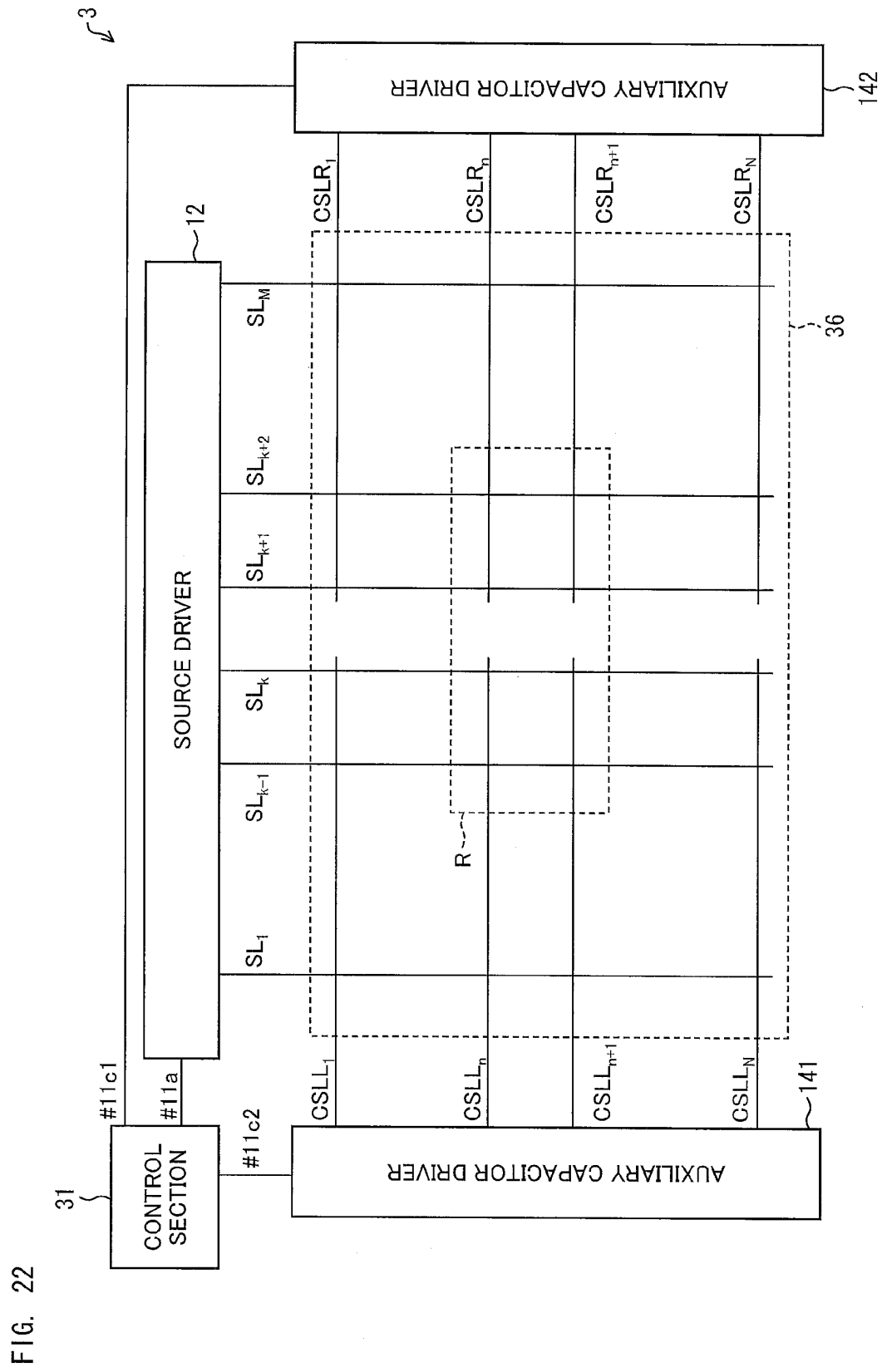


FIG. 23

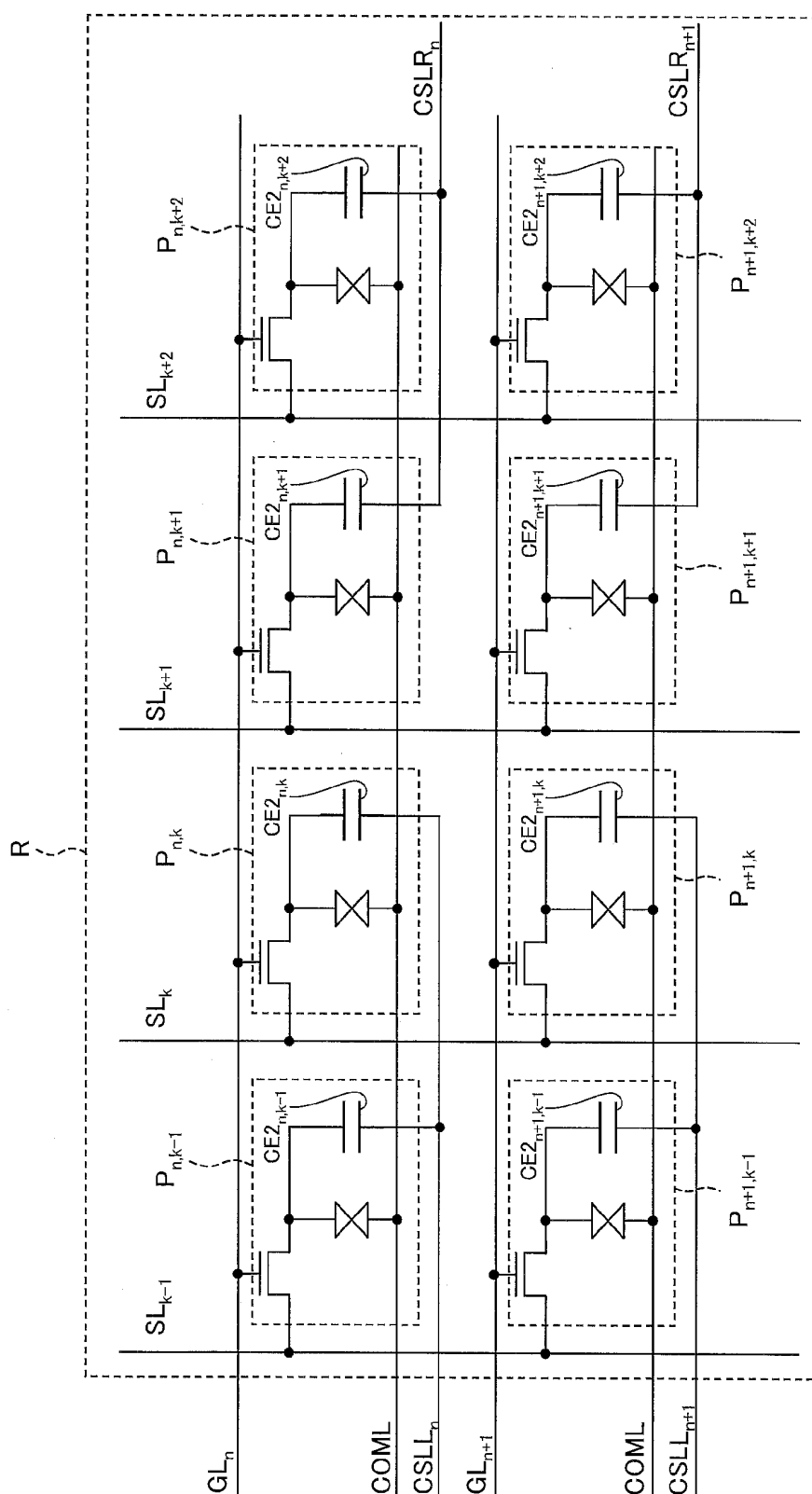


FIG. 24

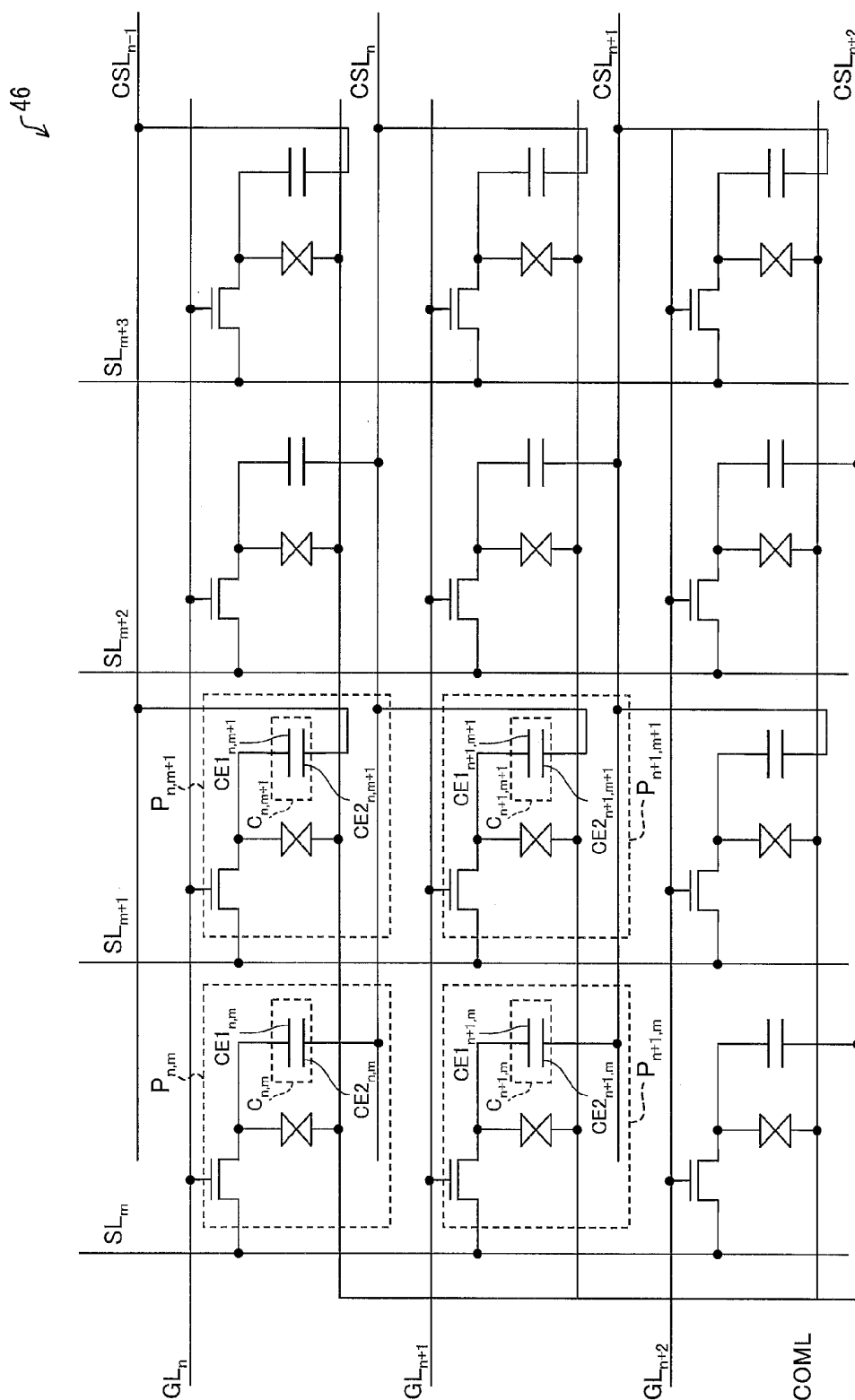


FIG. 25

$P_{n,m}$ +	$P_{n,m+1}$ —	+	—
$P_{n+1,m}$ —	$P_{n+1,m+1}$ +	—	+
+	—	+	—

DISPLAY PANEL, LIQUID CRYSTAL DISPLAY, AND DRIVING METHOD

TECHNICAL FIELD

[0001] The present invention relates to a display panel that displays an image by using liquid crystals, and also relates to a liquid crystal display device including such a display panel.

BACKGROUND ART

[0002] Conventionally, image display devices for displaying images have been classified broadly into impulse-type image display devices such as CRT (cathode-ray tubes) and hold-type image display devices such as liquid crystal display devices.

[0003] In an impulse-type image display device, a lighting period during which an image is displayed and an extinction period during which no image is displayed are alternately repeated. In a typical hold-type image display device, on the other hand, no extinction period is provided.

[0004] Therefore, the hold-type image display devices are more likely to suffer from blurring of moving images than the impulse-type image display devices.

[0005] A reason for this is for example as follows: Although, in changing from displaying one frame to displaying the next frame, a hold-type image display device displays a moving object as if the moving object were staying in one position, the observer transfers his/her gaze on the screen in chase of the moving object even in a period of time during which the moving object is being displayed as if it were staying in one position; therefore, the contours of the moving object appear to be blurred.

[0006] Patent Literature 1 discloses an image display device which divides one frame period into two subframes, namely a first-half subframe and a second-half subframe, and which supplies the two subframes with image signals having different gray-scale levels. According to the technology described in Patent Literature 1, such the phenomenon of blurring of moving images can be suppressed by making the brightness of an image in the first-half subframe and the brightness of an image in the second-half subframe different.

CITATION LIST

Patent Literature 1

[0007] Japanese Patent Application Publication, Tokukai, No. 2005-173573 (Jun. 30, 2005)

SUMMARY OF INVENTION

Technical Problem

[0008] However, the technology described in Patent Literature 1 requires a frame memory in which to temporarily store the input image signals, thus undesirably bringing about increase in manufacturing cost. Moreover, the technology described in Patent Literature 1 requires access to the frame memory every time a frame is displayed, thus undesirably bringing about increase in power consumption.

[0009] The present invention has been made in view of the foregoing problems, and it is an object of the present invention to realize a display panel capable of suppressing the

phenomenon of blurring of moving images while suppressing increase in manufacturing cost and in power consumption.

Solution to Problem

[0010] In order to solve the foregoing problems, a display panel according to the present invention is a display panel including: a plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the display panel including an auxiliary capacitor driver which, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

[0011] Although, in changing from displaying one frame to displaying the next frame, a hold-type image display device such as a liquid crystal display device displays a moving object as if the moving object were staying in one position, the observer transfers his/her gaze on the screen in chase of the moving object even in a period of time during which the moving object is being displayed as if it were staying in one position; therefore, there occurs a phenomenon of blurring of moving images where the contours of the moving object appear to be blurred.

[0012] As described above, a display panel according to the present invention is a display panel including: a plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines,

which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal layer; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the display panel including an auxiliary capacitor driver which, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level. Therefore, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, a first voltage level and a second voltage level that is different from the first voltage level can be applied to the pixel electrode connected via the transistor to the given gate bus line.

[0013] Further, in the display panel according to the present invention, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level are each longer than a response time of the liquid crystal. The response time of the liquid crystal here means the amount of time required for the orientation of the liquid crystal to start to change after application of an electric field to the liquid crystal. Generally, the amount of time required is 1 ms or more.

[0014] Therefore, the foregoing configuration can cause the brightness of an image in the pixel region in which the pixel electrode has been formed to switch between two values in the single scanning period.

[0015] This brings about an effect of making it possible to suppress the phenomenon of blurring of moving images.

[0016] Further, the auxiliary capacitor driver of the display panel according to the present invention can supply, in synchronization with the conducting signal, the rectangular voltage signal composed of the first voltage level and the second voltage level. Therefore, the voltage level of the rectangular voltage signal changes after a certain period of time has elapsed since the conducting signal was supplied.

[0017] Therefore, unlike in a case where a voltage signal is supplied out of synchronization with the conducting signal, the switching between bright and dark can be carried out in every pixel region on the screen after a certain period of time has elapsed since an update of image data.

[0018] Further, in the display panel according to the present invention, the blurring of moving images can be suppressed without using a frame memory in which to temporarily store image signals. Therefore, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, the display panel according to the present invention brings about an effect of making it possible to reduce manufacturing cost. Further, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, the display panel according to the present invention brings about an effect of making it possible to reduce power consumption.

[0019] Further, a driving method according to the present invention is a method for driving a display panel including: a

plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the method including a voltage signal supplying step of, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplying the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

[0020] The foregoing method brings about the same effects as the foregoing display panel according to the present invention.

Advantageous Effects of Invention

[0021] As described above, a display panel according to the present invention is a display panel including: a plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the display panel including an auxiliary capacitor driver which, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor

bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

[0022] Therefore, in the display panel according to the present invention, the blurring of moving images can be suppressed without using a frame memory in which to temporarily store image signals. Therefore, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, manufacturing cost can be reduced. Further, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, power consumption can be reduced.

BRIEF DESCRIPTION OF DRAWINGS

[0023] FIG. 1 is a block diagram showing a configuration of a display panel according to a first embodiment of the present invention.

[0024] FIG. 2 is a circuit diagram showing a configuration of a pixel region of the display panel according to the first embodiment of the present invention.

[0025] FIG. 3 serves to explain a first example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal corresponding to a high tone, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0026] FIG. 4 serves to explain the first example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal corresponding to a low tone, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0027] FIG. 5 serves to explain a second example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal corresponding to a high tone, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0028] FIG. 6 serves to explain the second example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal corresponding to a low tone, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0029] FIG. 7 serves to explain a third example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal corresponding to a high tone, (b) being a timing chart showing a waveform of a gate signal, (c) being

a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0030] FIG. 8 serves to explain the third example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal corresponding to a low tone, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0031] FIG. 9 serves to explain a fourth example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0032] FIG. 10 serves to explain a fifth example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0033] FIG. 11 serves to explain a sixth example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a source signal, (b) being a timing chart showing a waveform of a gate signal, (c) being a timing chart showing a common potential and a potential of a pixel electrode, (d) being a timing chart showing a waveform of an auxiliary capacitor signal.

[0034] FIG. 12 serves to explain an example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing waveforms of gate signals, (b) being a timing chart showing examples of waveforms of auxiliary capacitor signals, (c) being a timing chart showing other examples of waveforms of auxiliary capacitor signals.

[0035] FIG. 13 serves to explain a seventh example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing waveforms of gate signals, (b) being a timing chart showing waveforms of auxiliary capacitor signals.

[0036] FIG. 14 serves to explain an example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a gate signal, (b) being a timing chart showing a common potential and a potential of a pixel electrode, (c) being a timing chart showing a waveform of an auxiliary capacitor signal having a duty ratio.

[0037] FIG. 15 serves to explain an example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a gate signal, (b) being a timing chart showing a common potential and a potential of a pixel electrode, (c) being a timing chart showing a waveform of an auxiliary capacitor signal having another duty ratio.

[0038] FIG. 16, which serves to explain an effect of the display panel according to the first embodiment of the present invention, is a graph representing a relationship between duty ratio and brightness.

[0039] FIG. 17, which serves to explain an effect of the display panel according to the first embodiment of the present invention, is a graph representing a relationship between duty ratio and visibility.

[0040] FIG. 18 serves to explain an example of operation of the display panel according to the first embodiment of the present invention, (a) being a timing chart showing a waveform of a gate signal, (b) being a timing chart showing a common potential and an example of a potential of a pixel electrode, (c) being a timing chart showing an example of a waveform of an auxiliary capacitor signal, (d) being a timing chart showing a common potential and another example of a potential of a pixel electrode, (e) being a timing chart showing another example of a waveform of an auxiliary capacitor signal.

[0041] FIG. 19 is a block diagram showing a configuration of an auxiliary capacitor driver in the display panel according to the first embodiment of the present invention.

[0042] FIG. 20 is a block diagram showing a configuration of a display panel according to a second embodiment of the present invention.

[0043] FIG. 21 serves to explain an example of operation of the display panel according to the second embodiment of the present invention, (a) being a timing chart showing waveforms of gate signals, (b) being a timing chart showing waveforms of auxiliary capacitor signals.

[0044] FIG. 22 is a block diagram showing a configuration of a display panel according to a third embodiment of the present invention.

[0045] FIG. 23 is a circuit diagram showing a configuration of a display section in the display panel according to the third embodiment.

[0046] FIG. 24 is a circuit diagram showing a configuration of a display section in a display panel according to a fourth embodiment of the present invention.

[0047] FIG. 25, which is a diagram showing an example of operation of the display panel according to the fourth embodiment of the present invention, is a diagram showing the polarities of potentials that are applied to the display section of the display panel.

DESCRIPTION OF EMBODIMENTS

Embodiment 1

[0048] A configuration of a display panel according to a first embodiment of the present invention is described with reference to FIGS. 1 and 2. FIG. 1 is a block diagram showing a configuration of a display panel 1 according to the present embodiment. The display panel 1 is an active-matrix liquid crystal display panel.

[0049] As shown in FIG. 1, the display panel 1 includes a control section 11, a source driver 12, a gate driver 13, an auxiliary capacitor driver 14, a counter electrode driver 15, and a display section 16.

[0050] The control section 11 outputs a control signal #11a to control the source driver 12, a control signal #11b to control the gate driver 13, a control signal #11c to control the auxiliary capacitor driver 14, and a control signal #11d to control the counter electrode driver 15.

[0051] In the display section 16, N gate bus lines GL_1 to GL_N and M source bus lines SL_1 to SL_M are formed in such a reticular pattern as to intersect one another. Further, in the display section 16, N auxiliary capacitor bus lines CSL_1 to CSL_N are formed substantially in parallel with the N gate bus lines GL_1 to GL_N . Further, in the display section 16, a counter electrode wire COML is formed. In the following, as shown in FIG. 1, the nth gate bus line, the mth source bus line, and the nth auxiliary capacitor bus line are represented as "gate bus line GL_n ", "source bus line SL_m ", and "auxiliary capacitor bus line CSL_n ", respectively.

[0052] Further, as shown in FIG. 1, the display section 16 includes a pixel region $P_{n,m}$ defined by the gate bus line GL_n ($1 \leq n \leq N$) and the source bus line SL_m ($1 \leq m \leq M$).

[0053] As shown in FIG. 1, the M source bus lines SL_1 to SL_M have their terminals connected to the source driver 12. The source driver 12 supplies the M source bus lines SL_1 to SL_M with source signals # SL_1 to # SL_M , respectively.

[0054] Further, the N gate bus lines GL_1 to GL_N have their terminals connected to the gate driver 13. The gate driver 13 supplies the N gate bus lines GL_1 to GL_N with gate signals # GL_1 to # GL_N , respectively.

[0055] Further, the N auxiliary capacitor bus lines CSL_1 to CSL_N have their terminals connected to the auxiliary capacitor driver 14. The auxiliary capacitor driver 14 supplies the N auxiliary capacitor bus lines CSL_1 to CSL_N with auxiliary capacitor signals # CSL_1 to # CSL_N , respectively.

[0056] Further, the counter electrode wire COML has its terminal connected to the counter electrode driver 15. The counter electrode driver 15 supplies the counter electrode wire COML with a common potential V_{COM} .

[0057] FIG. 2 is a circuit diagram showing a configuration of the display panel 1 in the pixel region $P_{n,m}$. As shown in FIG. 2, the display panel 1 includes, in the pixel region $P_{n,m}$, a transistor $M_{n,m}$ having its gate connected to the gate bus line GL_n and its source connected to the source bus line SL_m . The transistor $M_{n,m}$ is, for example, a thin-film transistor (TFT), but, in the present invention, is not to be limited to a specific type of transistor. Further, in the present embodiment, the transistor $M_{n,m}$ is described by taking, as an example, a transistor that switches into a conducting state when a high-level potential is applied to the gate and switches into a cutoff state when a low-level potential is applied to the gate. However, the present invention is not to be limited to such an example. Even a transistor that switches into a conducting state when a low-level potential is applied to the gate and switches into a cutoff state when a high-level potential is applied to the gate can be applied to the present invention.

[0058] Further, as shown in FIG. 2, the transistor $M_{n,m}$ has its drain connected to a pixel electrode $PE_{n,m}$. Further, the display panel 1 includes, in the pixel region $P_{n,m}$, a counter electrode E_{COM} opposed to the pixel electrode $PE_{n,m}$, and the counter electrode E_{COM} is connected to the counter electrode wire COML. Further, the display panel 1 includes a liquid crystal LC between the pixel electrode $PE_{n,m}$ and the counter electrode E_{COM} , with a pixel capacitor C_{LC} formed between the pixel electrode $PE_{n,m}$ and the counter electrode E_{COM} .

[0059] An electric field corresponding to charge stored in the pixel electrode $PE_{n,m}$ is induced between the pixel electrode $PE_{n,m}$ and the counter electrode E_{COM} , and the orientation of the liquid crystal LC is determined according to the magnitude of the electric field. In other words, the orientation of the liquid crystal LC is determined according to the absolute value of a potential difference between the pixel electrode

$PE_{n,m}$ and the counter electrode E_{COM} . Further, the transmittance of the liquid crystal LC is determined according to the orientation. The present embodiment is described by taking, as an example, a case of normally black in which as the absolute value of the potential difference becomes larger, the transmittance of the liquid crystal LC becomes higher. However, the present invention is not to be limited to such an example. The present invention can be applied even in a case of normally white in which as the absolute value of the potential difference becomes larger, the transmittance of the liquid crystal LC becomes lower. Further, the higher the transmittance of the liquid crystal LC becomes, the higher the brightness of the pixel region $P_{n,m}$, which includes the liquid crystal LC, becomes.

[0060] Further, the transistor $M_{n,m}$ has its drain connected to a first auxiliary capacitor electrode $CE1_{n,m}$ parallel to the pixel electrode $PE_{n,m}$. Further, the pixel region $P_{n,m}$ includes a second auxiliary capacitor electrode $CE2_{n,m}$ opposed to the first auxiliary capacitor electrode $CE1_{n,m}$ and connected to the auxiliary capacitor bus line CSL_n , with an auxiliary capacitor C_{CS} formed between the first auxiliary capacitor electrode $CE1_{n,m}$ and the second auxiliary capacitor electrode $CE2_{n,m}$ in parallel with the pixel capacitor C_{LC} . In other words, the first auxiliary capacitor electrode $CE1_{n,m}$ and the second auxiliary capacitor electrode $CE2_{n,m}$ constitute a capacitor $C_{n,m}$ having the auxiliary capacitor C_{CS} .

[0061] (Example 1 of Operation of the Display Panel 1)

[0062] A first example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) through (d) of FIG. 3 and (a) through (d) of FIG. 4.

[0063] First, a case where the source driver 12 supplies the source bus line SL_m with a source signal $\#SL_m$ corresponding to a high tone is described with reference to (a) through (d) of FIG. 3.

[0064] (a) of FIG. 3 is a timing chart showing an example of a waveform of the source signal $\#SL_m$, which is supplied to the source bus line SL_m .

[0065] (b) of FIG. 3 is a timing chart showing an example of a waveform of the gate signal $\#GL_n$, which is supplied to the gate bus line GL_n .

[0066] (c) of FIG. 3 is a timing chart showing the common potential V_{COM} , which is supplied to the counter electrode wire COM , and a potential $V_{PEN,m}$ that is applied to the pixel electrode $PE_{n,m}$.

[0067] (d) of FIG. 3 is a timing chart showing a waveform of the auxiliary capacitor signal $\#CSL_n$, which is supplied to the auxiliary capacitor bus line CSL_n . As shown in (d) of FIG. 3, the auxiliary capacitor signal $\#CSL_n$ is a signal that alternately takes on a potential V_{CS1} and a potential V_{CS2} in a single cycle composed of two consecutive vertical scanning periods T_V . More specifically, as shown in (d) of FIG. 3, the auxiliary capacitor signal $\#CSL_n$ takes on the potential V_{CS1} during a period T_1 in a single vertical scanning period T_V , and takes on the potential V_{CS2} during a period T_2 . Further, the auxiliary capacitor signal $\#CSL_n$ takes on the potential V_{CS2} during a period T_3 in the ensuing vertical scanning period T_V , and takes on the potential V_{CS1} during a period T_4 . It is assumed that as shown in (d) of FIG. 3, specific values of the potentials V_{CS1} and V_{CS2} satisfy $V_{CS1} < V_{CS2}$.

[0068] As shown in (c) and (d) of FIG. 3, when the auxiliary capacitor signal $\#CSL_n$ is at the lowest potential (potential V_{CS1}) and the gate signal $\#GL_n$ is at a high level, the voltage that is applied to the liquid crystal LC changes into a positive

polarity; and when the auxiliary capacitor signal $\#CSL_n$ is at the highest potential (potential V_{CS2}) and the gate signal $\#GL_n$ is at a high level, the voltage that is applied to the liquid crystal LC changes into a negative polarity.

[0069] The “voltage that is applied to the liquid crystal LC” here means a potential difference between the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, and the potential V_{COM} , which is applied to the counter electrode E_{COM} (same applies below).

[0070] Further, in the present embodiment, a case is described where the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, has the same polarity as a potential $V_{PEN,t}$ ($t \neq m, 1 \leq t \leq M$) that is applied to a pixel electrode $PE_{n,t}$.

[0071] It should be noted that each single vertical scanning period T_V is defined as including a boundary time at a point in time where the period starts, but not including a boundary time at a point in time where the period ends. That is, in (d) of FIG. 3, each single vertical period T_V is defined as a set of times t that satisfy $t_2 \leq t < t_5$ or as a set of times t that satisfy $t_5 \leq t < t_8$ (same applies below).

[0072] The following describes the operation of each of the components in the pixel region $P_{n,m}$ of the display panel 1.

[0073] First, as shown in (b) of FIG. 3, the gate signal $\#GL_n$ rises from a low level to a high level at the time t_1 and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal $\#GL_n$ is at a high level, the transistor $M_{n,m}$ is in a conducting state. When the transistor $M_{n,m}$ is in a conducting state, the source signal $\#SL_m$ is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$. As shown in (c) of FIG. 3, in a period from the time t_1 to the time t_2 , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, rises from a potential V_1 to a potential V_2 (which is positive).

[0074] Then, the auxiliary capacitor signal $\#CSL_n$ rises from the potential V_{CS1} to the potential V_{CS2} at the time t_3 . Since the gate signal $\#GL_n$ is at a low level at this point in time, the transistor $M_{n,m}$ is in a cutoff state. Therefore, a sum of the charge stored in the pixel electrode $PE_{n,m}$ and the charge stored in the first auxiliary capacitor electrode $CE1_{n,m}$ is invariable. Meanwhile, when the value of the auxiliary capacitor signal $\#CSL_n$ changes, the charge stored in the pixel electrode $PE_{n,m}$ and the charge stored in the first auxiliary capacitor electrode $CE1_{n,m}$ change. Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_2 to a potential V_3 . It should be noted here that a specific value of the potential V_3 is defined as:

$$V_3 = (V_{CS2} - V_{CS1}) \times C_{CS} / \Sigma C + V_2.$$

Further, ΣC is the sum of the capacitors connected to the drain of the transistor $M_{n,m}$ in parallel with each other and, in the present embodiment, specifically, $\Sigma C = C_{LC} + C_{CS}$. Since $V_{CS1} < V_{CS2}$ as mentioned above, the potential V_3 is greater than the potential V_2 .

[0075] Further, as shown in (c) of FIG. 3, the potential difference between the potential V_3 and the common potential V_{COM} is greater than the potential difference between the potential V_2 and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_3 to the time t_4 is greater than the transmittance of the liquid crystal LC in a period from the time t_2 to the time t_3 . That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_3 to the time t_4 is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_2 to the time t_3 .

[0076] Then, the gate signal #GL_n rises from a low level to a high level at the time t₄ and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor M_{n,m} is in a conducting state, so that the source signal #SL_m is supplied to the pixel electrode PE_{n,m} and the first auxiliary capacitor electrode CE1_{n,m}.

[0077] As shown in (c) of FIG. 3, in a period from the time t₄ to the time t₅, the potential V_{PE_{n,m}}, which is applied to the pixel electrode PE_{n,m}, falls from the potential V₃ to a potential V₄ (which is negative).

[0078] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS2} to the potential V_{CS1} at the time t₆. Since the gate signal #GL_n is at a low level at this point in time, the transistor M_{n,m} is in a cutoff state. Therefore, a sum of the charge stored in the pixel electrode PE_{n,m} and the charge stored in the first auxiliary capacitor electrode CE1_{n,m} is invariable. Meanwhile, when the value of the auxiliary capacitor signal #CSL_n changes, the charge stored in the pixel electrode PE_{n,m} and the charge stored in the first auxiliary capacitor electrode CE1_{n,m} change. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₄ to the potential V₁. It should be noted here that a specific value of the potential V₁ is defined as:

$$V_1 = (V_{CS1} - V_{CS2}) \times C_{CS} / \Sigma C + V_4$$

Further, since V_{CS1} < V_{CS2} as mentioned above, the potential V₁ is smaller than the potential V₄.

[0079] Further, as shown in (c) of FIG. 3, the potential difference between the potential V₁ and the common potential V_{COM} is greater than the potential difference between the potential V₄ and the common potential V_{COM}. That is, the transmittance of the liquid crystal LC in a period from the time t₆ to the time t₇ is greater than the transmittance of the liquid crystal LC in a period from the time t₅ to the time t₆. That is, the brightness of the pixel region P_{n,m} in the period from the time t₆ to the time t₇ is greater than the brightness of the pixel region P_{n,m} in the period from the time t₅ to the time t₆.

[0080] The operation at the time t₇ and later is the same as the operation at the time t₁ and later.

[0081] Although the foregoing description has assumed that $\Sigma C = C_{LC} + C_{CS}$, the present invention is not to be limited thereby. For example, in such a case where a capacitor (parasitic capacitor) Cgd exists between the drain of the transistor M_{n,m} and the gate bus line GL_n and a capacitor (parasitic capacitor) Csd exists between the drain of the transistor M_{n,m} and the source bus line SL_m, $\Sigma C = C_{LC} + C_{CS} + C_{gd} + C_{sd}$. Alternatively, in such a case where in addition to these capacitors, a further capacitor Cext exists in parallel with the liquid crystal capacitor C_{LC}, $\Sigma C = C_{LC} + C_{CS} + C_{gd} + C_{sd} + C_{ext}$. As for the definition of ΣC , the same applies to the following description.

[0082] Further, in actuality, a period of time during which the gate signal #GL_n shown in (b) of FIG. 3 is at a high level is sufficiently shorter than a single vertical scanning period T_V.

[0083] As described above, the display panel 1 according to the present embodiment is a display panel including: a plurality of gate bus lines GL₁ to GL_N; a plurality of source bus lines SL₁ to SL_M; a plurality of auxiliary capacitor bus lines CSL₁ to CSL_N; a transistor M_{n,m} including a gate connected to a given gate bus line GL_n of the plurality of gate bus lines and a source connected to a given source bus line SL_m of the

plurality of source bus lines; a pixel electrode PE_{n,m} connected to a drain of the transistor; a capacitor C_{n,m}, one end (first auxiliary capacitor electrode CE1_{n,m}) of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end (second auxiliary capacitor electrode CE2_{n,m}) of which is connected to a given auxiliary capacitor bus line CSL_n of the plurality of auxiliary capacitor bus lines; a source driver 12, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver 13, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode E_{COM} opposed to the pixel electrode via a liquid crystal layer (liquid crystal LC); a counter electrode wire COML connected to the counter electrode; and a counter electrode driver 15, which supplies the counter electrode wire with a common potential V_{COM}, the display panel 1 including an auxiliary capacitor driver which, in a single scanning period (single vertical scanning period T_V) from a point in time where the gate driver supplies the given gate bus line with the conducting signal (high-level interval of a gate signal #GL_n) to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor bus line CSL_n with a rectangular voltage signal (auxiliary capacitor signal #CSL_n) in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level (i.e., at least a potential V_{CS1} and a potential V_{CS2}). Further, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level, i.e., a time T₁ and a time T₂, are each longer than a response time of the liquid crystal.

[0084] Therefore, in the single scanning period, the display panel 1 can apply a two-valued voltage level to the pixel electrode connected via the transistor to the given gate bus line. That is, the display panel 1 can cause the brightness of an image in the pixel region P_{n,m}, in which the pixel electrode PE_{n,m} has been formed, to switch between two values in the single scanning period.

[0085] This makes it possible to suppress the aforementioned phenomenon of blurring of moving images.

[0086] The auxiliary capacitor driver 14 of the display panel 1 according to the present invention can supply the rectangular voltage signal (auxiliary capacitor signal #CSL_n) in synchronization with the conducting signal. Therefore, unlike in a case where a voltage signal is supplied out of synchronization with the conducting signal, a proportion between a period of display at a high brightness and a period of display at a low brightness can be made substantially equal in any place on the screen, so that blurring of moving images can be effectively suppressed.

[0087] Further, in the display panel 1 according to the present invention, the blurring of moving images can be suppressed without using a frame memory in which to temporarily store image signals. Therefore, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, manufacturing cost can be reduced. Further, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, power consumption can be reduced.

[0088] Further, according to this example of operation, the rectangular voltage signal (auxiliary capacitor signal #CSL_n) takes on either one of the first and second voltage levels (i.e., either one of the potentials V_{CS1} and V_{CS2}) in an at least 10% continuous period of time of the single scanning period.

[0089] Therefore, the phenomenon of blurring of moving images can be effectively suppressed.

[0090] Further, according to this example of operation, the rectangular voltage signal (auxiliary capacitor signal #CSL_n) takes on either one (potential V_{CS1}) of the first and second voltage levels in a period of time from a point in time at which the single scanning period (single vertical scanning period T_v) starts to a point in time where substantially 10% of the single scanning period elapses, and takes on the other one (potential V_{CS2}) of the first and second voltage levels in a period of time from a point in time where substantially 90% of the single scanning period elapses to a point in time at which the single scanning period ends.

[0091] Generally, in the case of switching between a display at a high brightness and a display at a low brightness, no improvement in blurring of moving images is felt when the percentage of the display at the high brightness is 90% or higher, more improvement in blurring of moving images is felt at a lower percentage between 90% to 10%, and satisfactory improvement in blurring of moving images is felt at a percentage of approximately 10%.

[0092] Therefore, according to the foregoing configuration, the phenomenon of blurring of moving images can be effectively suppressed.

[0093] Next, a case where the source driver 12 supplies the source bus line SL_m with a source signal #SL_m corresponding to a low tone is described with reference to (a) through (d) of FIG. 4. It should be noted that overlaps with the foregoing description are not described below.

[0094] (a) of FIG. 4 is a timing chart showing an example of a waveform of the source signal #SL_m which is supplied to the source bus line SL_m. In the following, as shown in (a) of FIG. 4, a case where the potential of the source signal #SL_m when the conducting signal #GL_n is at a high level and the auxiliary capacitor bus line #CSL_n is at a low level is lower than the potential of the waveform shown in (a) of FIG. 3 under the same conditions or a case where the potential of the source signal #SL_m when the conducting signal #GL_n is at a high level and the auxiliary capacitor bus line #CSL_n is at a high level is higher than the potential of the waveform shown in (a) of FIG. 3 under the same conditions is described.

[0095] (b) of FIG. 4 is a timing chart showing an example of a waveform of the gate signal #GL_n, which is supplied to the gate bus line GL_n. The waveform shown in (b) of FIG. 4 is the same as that shown in (b) of FIG. 3.

[0096] (c) of FIG. 4 is a timing chart showing the common potential V_{COM} which is supplied to the counter electrode wire COML, and a potential V_{PE_{n,m}} that is applied to the pixel electrode PE_{n,m}.

[0097] (d) of FIG. 4 is a timing chart showing a waveform of the auxiliary capacitor signal #CSL_n, which is supplied to the auxiliary capacitor bus line CSL_n. The waveform shown in (d) of FIG. 4 is the same as that shown in (d) of FIG. 3.

[0098] First, as shown in (b) of FIG. 4, the gate signal #GL_n rises from a low level to a high level at the time t₁ and, after a certain period of time has elapsed, falls to a low level. In a case where, as shown in (a) of FIG. 4, the potential of the source signal #SL_m relative to the common potential V_{COM} is substantially equal to the potential of the pixel electrode PE_{n,m}

during a period from the time t₁ to the time t₂, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} stays substantially constant at a potential V₀₁.

[0099] Then, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS1} to the potential V_{CS2} at the time t₃. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₀₁ to a potential V₀₂. It should be noted here that a specific value of the potential V₀₂ is defined as:

$$V_{02} = (V_{CS2} - V_{CS1}) \times C_{CS} / \Sigma C + V_{01}.$$

Since V_{CS1} < V_{CS2} as mentioned above, the potential V₀₂ is greater than the potential V₀₁.

[0100] Then, the gate signal #GL_n rises from a low level to a high level at the time t₄ and, after a certain period of time has elapsed, falls to a low level. In a case where, as shown in (a) of FIG. 4, the potential of the source signal #SL_m relative to the common potential V_{COM} is substantially equal to the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} during a period from the time t₄ to the time t₅, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} stays substantially constant at the potential V₀₂.

[0101] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS2} to the potential V_{CS1} at the time t₆. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes for example from the potential V₀₂ to the potential V₀₁.

[0102] The operation at the time t₇ and later is the same as the operation at the time t₁ and later.

[0103] As shown in (c) of FIG. 4, the absolute value of the potential difference between the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} and the common potential V_{COM} is always kept substantially constant throughout all the periods. That is, in a case where the source signal #SL_m corresponding to a low tone is supplied, the transmittance of the liquid crystal LC of the pixel region P_{n,m} can be kept substantially constant even in a case where the value of the auxiliary capacitor signal #CSL_n is changed as shown in (d) of FIG. 4.

[0104] According to this example of operation, as described above, in the single scanning period (single vertical scanning period T_v), the polarity of a voltage that is applied to the liquid crystal when the rectangular voltage signal (auxiliary capacitor signal #CSL_n) is at the first voltage level and the polarity of a voltage that is applied to the liquid crystal when the rectangular voltage signal is at the second voltage level are polarities that are different from each other. That is, a voltage that is applied to the liquid crystal as represented by a difference between the potential V₀₁ of the pixel electrode PE_{n,m} and the potential V_{COM} of the counter electrode when the auxiliary capacitor signal #CSL_n is at the potential V_{CS1} and a voltage that is applied to the liquid crystal as represented by a difference between the potential V₀₂ of the pixel electrode PE_{n,m} and the potential V_{COM} of the counter electrode when the auxiliary capacitor signal #CSL_n is at the potential V_{CS2} are opposite in polarity to each other.

[0105] According to the foregoing configuration, regardless of whether the rectangular voltage signal is at the first or second voltage level, the absolute value of the voltage that is applied to the liquid crystal can be made sufficiently small.

[0106] Therefore, according to the foregoing configuration, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, a black display can be carried

out at a sufficiently low brightness, regardless of whether the rectangular voltage signal is at the first or second voltage level.

[0107] Further, according to this example of operation, it is preferable that the absolute value of the potential difference between the first voltage level and the second voltage level be twice or less as great as the threshold voltage of the liquid crystal. That is, it is preferable that the absolute value of the potential difference between the potential V_{CS1} and the potential V_{CS2} be twice or less as great as the threshold voltage of the liquid crystal.

[0108] Generally, the orientation of a liquid crystal is not affected even when a voltage that is equal to or lower than the threshold voltage is applied to the liquid crystal. In other words, the threshold voltage means a voltage at which the orientation of a liquid crystal starts to be affected (same applies below). The threshold voltage can be defined, for example, as a voltage $1/100$ times as great as a saturation voltage at which the transmittance of the liquid crystal gets saturated.

[0109] Assuming that the voltage difference between the voltage that is applied to the liquid crystal as represented by the difference between the potential of the pixel electrode $PE_{n,m}$ and the potential V_{COM} of the counter electrode in a case where the auxiliary capacitor signal $\#CSL_n$ is at the potential V_{CS1} and the voltage that is applied to the liquid crystal as represented by the difference between the potential of the pixel electrode $PE_{n,m}$ and the potential V_{COM} of the counter electrode in a case where the auxiliary capacitor signal $\#CSL_n$ is at the potential V_{CS2} is represented as ΔV_{LC} , ΔV_{LC} satisfies:

$$\Delta V_{LC} = (V_{CS2} - V_{CS1}) \times C_{CS} / \Sigma C.$$

It should be noted here that since $C_{CS} / \Sigma C < 1$, $\Delta V_{LC} < (V_{CS2} - V_{CS1})$ is derived.

[0110] Further, assuming that the voltage that is applied to the liquid crystal as represented by the difference between the potential of the pixel electrode $PE_{n,m}$ and the potential V_{COM} of the counter electrode is expressed as V_{LC} , it is desirable that in a case where the potential of the auxiliary capacitor signal $\#CSL_n$ is the potential V_{CS1} , V_{LC} be set as $V_{LC} = -\Delta V_{LC}/2$, and that in a case where the potential of the auxiliary capacitor signal $\#CSL_n$ is the potential V_{CS2} , V_{LC} be set as $V_{LC} = \Delta V_{LC}/2$. It should be noted here that as long as $\Delta V_{LC}/2$ is equal to or less than the threshold voltage V_{LCth} , i.e., $\Delta V_{LC}/2 \leq V_{LCth}$, a black display can be carried out regardless of whether the potential of the auxiliary capacitor signal $\#CSL_n$ is the potential V_{CS1} or the potential V_{CS2} . Therefore, as long as $V_{CS2} - V_{CS1} \leq 2 \times V_{LCth}$, a black display can be carried out regardless of whether the potential of the auxiliary capacitor signal $\#CSL_n$ is the potential V_{CS1} or the potential V_{CS2} .

[0111] According to the foregoing configuration, as described above, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, a black display can be carried out regardless of whether the voltage level of the rectangular voltage signal is the first or second voltage level.

[0112] It should be noted that the above method of derivation can be applied in substantially the same manner to the examples of operation to be described later.

[0113] (Example 2 of Operation of the Display Panel 1)

[0114] A second example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) through (d) of FIG. 5 and (a) through (d) of FIG. 6.

[0115] First, a case where the source driver 12 supplies the source bus line SL_m with a source signal $\#SL_m$ corresponding to a high tone is described with reference to (a) through (d) of FIG. 5.

[0116] (a) of FIG. 5 is a timing chart showing an example of a waveform of the source signal $\#SL_m$, which is supplied to the source bus line SL_m . This waveform is the same as the waveform of the source signal $\#SL_m$ shown in (a) of FIG. 3.

[0117] (b) of FIG. 5 is a timing chart showing a waveform of the gate signal $\#GL_n$, which is supplied to the gate bus line GL_n . As shown in (b) of FIG. 5, the waveform of the gate signal $\#GL_n$ in this example of operation is described as being the same as the waveform of the gate signal $\#GL_n$ shown in (b) of FIG. 3.

[0118] (c) of FIG. 5 is a timing chart showing the common potential V_{COM} , which is supplied to the counter electrode wire COM_L , and a potential $V_{PEN,m}$ that is applied to the pixel electrode $PE_{n,m}$.

[0119] (d) of FIG. 5 is a timing chart showing a waveform of the auxiliary capacitor signal $\#CSL_n$, which is supplied to the auxiliary capacitor bus line CSL_n . As shown in (d) of FIG. 5, the auxiliary capacitor signal $\#CSL_n$ in this example of operation is a signal that takes on a potential V_{CS1}' , a potential V_{CS2}' , and a potential V_{CS3}' in a single cycle composed of two consecutive vertical scanning periods T_V' . More specifically, as shown in (d) of FIG. 5, the auxiliary capacitor signal $\#CSL_n$ takes on the potential V_{CS2}' during a period T_1' in a single vertical scanning period T_V' , and takes on the potential V_{CS3}' during a period T_2' . Further, the auxiliary capacitor signal $\#CSL_n$ takes on the potential V_{CS2}' during a period T_3' in the ensuing vertical scanning period T_V' , and takes on the potential V_{CS1}' during a period T_4' . It is assumed that as shown in (d) of FIG. 5, specific values of the potentials V_{CS1}' , V_{CS2}' , and V_{CS3}' satisfy $V_{CS1}' < V_{CS2}' < V_{CS3}'$.

[0120] As shown in (c) and (d) of FIG. 5, when the auxiliary capacitor signal $\#CSL_n$ is at the lowest potential (potential V_{CS1}') and the gate signal $\#GL_n$ is at a high level, the voltage that is applied to the liquid crystal LC changes into a positive polarity; and when the auxiliary capacitor signal $\#CSL_n$ is at the highest potential (potential V_{CS3}') and the gate signal $\#GL_n$ is at a high level, the voltage that is applied to the liquid crystal LC changes into a negative polarity.

[0121] The following describes the operation of each of the components in the pixel region $P_{n,m}$ of the display panel 1 in this example of operation.

[0122] First, as shown in (b) of FIG. 5, the gate signal $\#GL_n$ rises from a low level to a high level at the time t_1' and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal $\#GL_n$ is at a high level, the transistor $M_{n,m}$ is in a conducting state. When the transistor $M_{n,m}$ is in a conducting state, the source signal $\#SL_m$ is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$. As shown in (c) of FIG. 5, in a period from the time t_1' to the time t_2' , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, rises from a potential V_1' to a potential V_2' (which is positive).

[0123] Further, the auxiliary capacitor signal $\#CSL_n$ rises from the potential V_{CS1}' to the potential V_{CS2}' at the time t_2' . Since the gate signal $\#GL_n$ is at a low level at this point in

time, the transistor $M_{n,m}$ is in a cutoff state. Therefore, a sum of the charge stored in the pixel electrode $PE_{n,m}$ and the charge stored in the first auxiliary capacitor electrode $CE1_{n,m}$ is invariable. Meanwhile, when the value of the auxiliary capacitor signal $\#CSL_n$ changes, the charge stored in the pixel electrode $PE_{n,m}$ and the charge stored in the first auxiliary capacitor electrode $CE1_{n,m}$ change. Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_2' to a potential V_3' . It should be noted here that a specific value of the potential V_3' is defined as:

$$V_3' = (V_{CS2}' - V_{CS1}') \times C_{CS}' \Sigma_C + V_2'.$$

Since $V_{CS1}' < V_{CS2}'$ as mentioned above, the potential V_3' is greater than the potential V_2' .

[0124] Then, the auxiliary capacitor signal $\#CSL_n$ rises from the potential V_{CS2}' to the potential V_{CS3}' at the time t_3' . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_3' to a potential V_4' . It should be noted here that a specific value of the potential V_4' is defined as:

$$V_4' = (V_{CS3}' - V_{CS2}') \times C_{CS}' \Sigma_C + V_3'.$$

Since $V_{CS2}' < V_{CS3}'$ as mentioned above, the potential V_4' is greater than the potential V_3' .

[0125] Further, as shown in (c) of FIG. 5, the potential difference between the potential V_4' and the common potential V_{COM} is greater than the potential difference between the potential V_3' and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_3' to the time t_4' is greater than the transmittance of the liquid crystal LC in a period from the time t_2' to the time t_3' . That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_3' to the time t_4' is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_2' to the time t_3' .

[0126] Then, the gate signal $\#GL_n$ rises from a low level to a high level at the time t_4' and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal $\#GL_n$ is at a high level, the transistor $M_{n,m}$ is in a conducting state, so that the source signal $\#SL_m$ is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$.

[0127] As shown in (c) of FIG. 5, in a period from the time t_4' to the time t_5' , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, falls from the potential V_4' to a potential V_5' (which is negative).

[0128] Further, the auxiliary capacitor signal $\#CSL_n$ falls from the potential V_{CS3}' to the potential V_{CS2}' at the time t_5' . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_5' to a potential V_6' . It should be noted here that a specific value of the potential V_6' is defined as:

$$V_6' = (V_{CS2}' - V_{CS3}') \times C_{CS}' \Sigma_C + V_5'.$$

Since $V_{CS2}' < V_{CS3}'$ as mentioned above, the potential V_6' is smaller than the potential V_5' .

[0129] Then, the auxiliary capacitor signal $\#CSL_n$ falls from the potential V_{CS2}' to the potential V_{CS1}' at the time t_6' . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_6' to the potential V_1' . It should be noted here that a specific value of the potential V_1' is defined as:

$$V_1' = (V_{CS1}' - V_{CS2}') \times C_{CS}' \Sigma_C + V_6'.$$

Since $V_{CS1}' < V_{CS2}'$ as mentioned above, the potential V_1' is smaller than the potential V_6' .

[0130] Further, as shown in (c) of FIG. 5, the potential difference between the potential V_1' and the common potential V_{COM} is greater than the potential difference between the potential V_6' and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_6' to the time t_7' is greater than the transmittance of the liquid crystal LC in a period from the time t_5' to the time t_6' . That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_6' to the time t_7' is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_5' to the time t_6' .

[0131] The operation at the time t_7' and later is the same as the operation at the time t_1' and later.

[0132] The above example of operation has described a case where the auxiliary capacitor signal $\#CSL_n$ rises from the potential V_{CS1}' to the potential V_{CS2}' at the time t_2' and the auxiliary capacitor signal $\#CSL_n$ falls from the potential V_{CS3}' to the potential V_{CS2}' at the time t_5' . However, more generally, the auxiliary capacitor signal $\#CSL_n$ rises from the potential V_{CS1}' to the potential V_{CS2}' before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t_2' and the auxiliary capacitor signal $\#CSL_n$ falls from the potential V_{CS3}' to the potential V_{CS2}' before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t_5' .

[0133] Further, according to this example of operation, in the single scanning period (single vertical scanning period T_V'), the auxiliary capacitor driver 14 supplies the given auxiliary capacitor bus line with a rectangular voltage signal (auxiliary capacitor signal $\#CSL_n$) in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels.

[0134] That is, according to this example of operation, in the single scanning period (single vertical scanning period T_V'), the auxiliary capacitor driver 14 supplies a rectangular voltage signal (auxiliary capacitor signal $\#CSL_n$) composed of the potential V_{CS1}' , the potential V_{CS2}' , and the potential V_{CS3}' .

[0135] Therefore, according to this example of operation, in the single scanning period, the level of voltage that is applied to the given auxiliary capacitor bus line switches among three values. In other words, in the single scanning period, the level of voltage that is applied to the auxiliary capacitor bus line makes two transitions. The first transition between the voltage levels in the single scanning period causes a voltage that is applied to the liquid crystal after the first transitions between the voltage levels to be suitable for a display after the first transition between the voltage levels, and the second transition between the voltage levels allows switching between a high brightness and a low brightness.

[0136] That is, this example of operation makes a display at a higher brightness possible while effectively suppressing the phenomenon of blurring of moving images.

[0137] Further, according to this example of operation, in a case where when the gate driver 13 supplies the given gate bus line GL_n with the conducting signal (high-level interval of the gate signal $\#GL_n$), the given auxiliary capacitor bus line CSL_n is supplied with the lowest voltage level among the voltage levels, the auxiliary capacitor driver 14 supplies the given

auxiliary capacitor bus line CSL_n with the rectangular voltage signal $\#CSL_n$ in the single scanning period (single vertical scanning period T_v), the rectangular voltage signal $\#CSL_n$ having its voltage levels arranged in an ascending order.

[0138] That is, as mentioned above, in a case where in the period from the time t_1' to the time t_2' , the auxiliary capacitor bus line CSL_n is supplied with the lowest voltage level $V_{CS1'}$ among the voltage levels $V_{CS1'}$, $V_{CS2'}$, and $V_{CS3'}$, the auxiliary capacitor driver 14 supplies the auxiliary capacitor bus line CSL_n with an auxiliary capacitor signal $\#CSL_n$ in a single scanning period from the time t_2' to the time t_5' (single vertical scanning period T_v), the auxiliary capacitor signal $\#CSL_n$ taking on the voltage level $V_{CS2'}$ in a period T_1' from the time t_2' to the time t_3' and taking on the voltage level $V_{CS3'}$ ($V_{CS2'} < V_{CS3'}$) in a period T_2' from the time t_3' to the time t_5' .

[0139] Generally, in a normally black type in which a black display is carried out in a case where no voltage is applied to the pixel electrode, a phenomenon of insufficient rising from a low brightness to a high brightness occurs due to finite lengths of time of response of the liquid crystal. In other words, there is such a characteristic that the amount of time required to change from a low brightness to a high brightness is larger than the amount of time required to change from a high brightness to a low brightness. In a case where a signal that is applied to the pixel electrode has a positive polarity, such a phenomenon can occur at a timing when the potential of the pixel electrode changes to a high voltage.

[0140] According to the foregoing configuration, in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the lowest voltage level among the voltage levels, the pixel electrode can be supplied with a voltage signal at a lower voltage and then with a voltage signal at a higher voltage level in the single scanning period.

[0141] This allows the potential that is applied to the pixel electrode to gradually change to a high voltage. This makes it possible to suppress the phenomenon of insufficient rising from a low brightness to a high brightness that can occur in a normally black type.

[0142] Further, according to this example of operation, in a case where when the gate driver 13 supplies the given gate bus line GL_n with the conducting signal (high-level interval of the gate signal $\#GL_n$), the given auxiliary capacitor bus line CSL_n is supplied with the highest voltage level among the voltage levels, the auxiliary capacitor driver 14 supplies the given auxiliary capacitor bus line CSL_n with the rectangular voltage signal in the single scanning period, the rectangular voltage signal having its voltage levels arranged in a descending order.

[0143] That is, as mentioned above, in a case where in the period from the time t_4' to the time t_5' , the auxiliary capacitor bus line CSL_n is supplied with the highest voltage level $V_{CS3'}$ among the voltage levels $V_{CS1'}$, $V_{CS2'}$, and $V_{CS3'}$, the auxiliary capacitor driver 14 supplies the auxiliary capacitor bus line CSL_n with a rectangular voltage signal $\#CSL_n$ in a single scanning period (single vertical scanning period T_v) from the time t_5' to the time t_8' , the rectangular voltage signal $\#CSL_n$ taking on the voltage level $V_{CS2'}$ in a period T_3' from the time t_5' to the time t_6' and taking on the voltage level $V_{CS1'}$ ($V_{CS1'} < V_{CS2'}$) in a period T_4' from the time t_6' to the time t_8' .

[0144] Generally, in a normally black type in which a black display is carried out in a case where no voltage is applied to the pixel electrode, a phenomenon of insufficient rising from a low brightness to a high brightness occurs due to finite

lengths of time of response of the liquid crystal. In other words, there is such a characteristic that the amount of time required to change from a low brightness to a high brightness is larger than the amount of time required to change from a high brightness to a low brightness. In a case where a signal that is applied to the pixel electrode has a negative polarity, such a phenomenon can occur at a timing when the potential of the pixel electrode changes to a low voltage.

[0145] According to the foregoing configuration, in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the highest voltage level among the voltage levels, the pixel electrode can be supplied with a voltage signal at a higher voltage and then with a voltage signal at a lower voltage level in the single scanning period.

[0146] This allows the potential that is applied to the pixel electrode to gradually change to a low voltage. This makes it possible to suppress the phenomenon of insufficient rising from a low brightness to a high brightness that can occur in a normally black type.

[0147] Next, a case where the source driver 12 supplies the source bus line SL_m with a source signal $\#SL_m$ corresponding to a low tone is described with reference to (a) through (d) of FIG. 6. It should be noted that overlaps with the foregoing description are not described below.

[0148] (a) of FIG. 6 is a timing chart showing an example of a waveform of the source signal $\#SL_m$, which is supplied to the source bus line SL_m . In the following, as shown in (a) of FIG. 6, a case where the potential of the source signal $\#SL_m$ when the conducting signal $\#GL_n$ is at a high level and the auxiliary capacitor bus line $\#CSL_n$ is at a low level is lower than the potential of the waveform shown in (a) of FIG. 3 under the same conditions or a case where the potential of the source signal $\#SL_m$ when the conducting signal $\#GL_n$ is at a high level and the auxiliary capacitor bus line $\#CSL_n$ is at a high level is higher than the potential of the waveform shown in (a) of FIG. 3 under the same conditions is described.

[0149] (b) of FIG. 6 is a timing chart showing a waveform of the gate signal $\#GL_n$, which is supplied to the gate bus line GL_n . The waveform shown in (b) of FIG. 6 is the same as that shown in (b) of FIG. 3.

[0150] (c) of FIG. 6 is a timing chart showing the common potential V_{COM} , which is supplied to the counter electrode wire COML, and a potential $V_{PEN,m}$ that is applied to the pixel electrode $PE_{n,m}$.

[0151] (d) of FIG. 6 is a timing chart showing a waveform of the auxiliary capacitor signal $\#CSL_n$, which is supplied to the auxiliary capacitor bus line CSL_n . The waveform shown in (d) of FIG. 6 is the same as that shown in (d) of FIG. 5.

[0152] First, as shown in (b) of FIG. 6, the gate signal $\#GL_n$ rises from a low level to a high level at the time t_1' and, after a certain period of time has elapsed, falls to a low level. As shown in (c) of FIG. 6, in the period from the time t_1' to the time t_2' , the potential $V_{PEN,m}$ that is applied to the pixel electrode $PE_{n,m}$, falls, for example, from a potential $V_{O1'}$ to a potential $V_{O2'}$.

[0153] Further, the auxiliary capacitor signal $\#CSL_n$ rises from the potential $V_{CS1'}$ to the potential $V_{CS2'}$ at the time t_2' . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential $V_{O2'}$, for example, to the potential $V_{O1'}$.

[0154] Then, the auxiliary capacitor signal $\#CSL_n$ rises from the potential $V_{CS2'}$ to the potential $V_{CS3'}$ at the time t_3' . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$

changes from the potential V_{01}' to a potential V_{03}' . It should be noted here that a specific value of the potential V_{03}' is defined as:

$$V_{03}' = (V_{CS3}' - V_{CS2}') \times C_{CS} / \Sigma C + V_0.$$

Since $V_{CS2}' < V_{CS3}'$ as mentioned above, the potential V_{03}' is greater than the potential V_{01}' .

[0155] Then, the gate signal #GL_n rises from a low level to a high level at the time t_4' and, after a certain period of time has elapsed, falls to a low level. As shown in (c) of FIG. 6, in the period from the time t_4' to the time t_5' , the potential $V_{PEN,m}'$, which is applied to the pixel electrode PE_{n,m}, rises from the potential V_{01}' to a potential V_{04}' .

[0156] Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS3}' to the potential V_{CS2}' at the time t_5' . Accordingly, the potential $V_{PEN,m}'$ of the pixel electrode PE_{n,m} changes from the potential V_{04}' , for example, to the potential V_{03}' .

[0157] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS2}' to the potential V_{CS1}' at the time t_6' . Accordingly, the potential $V_{PEN,m}'$ of the pixel electrode PE_{n,m} changes from the potential V_{03}' to the potential V_{01}' .

[0158] The operation at the time t_7' and later is the same as the operation at the time t_1' and later.

[0159] As shown in (c) of FIG. 6, the absolute value of the potential difference between the potential $V_{PEN,m}'$ of the pixel electrode PE_{n,m} and the common potential V_{COM} is always kept substantially constant throughout all the periods. That is, the transmittance of the liquid crystal LC of the pixel region P_{n,m} can be kept substantially constant even in a case where the value of the auxiliary capacitor signal #CSL_n is changed as shown in (d) of FIG. 6.

[0160] Further, according to this example of operation, in the single scanning period (single vertical scanning period T_{V'}), a polarity of a voltage that is applied to the liquid crystal after a first transition between the voltage levels and a polarity of a voltage that is applied to the liquid crystal after a next transition between the voltage levels are polarities that are different from each other. A voltage that is applied to the liquid crystal as represented by a difference between the potential V_{01}' of the pixel electrode PE_{n,m} and the potential V_{COM} of the counter electrode when the auxiliary capacitor signal #CSL_n is at the potential V_{CS2}' and a voltage that is applied to the liquid crystal as represented by a difference between the potential V_{03}' of the pixel electrode PE_{n,m} and the potential V_{COM} of the counter electrode when the auxiliary capacitor signal #CSL_n is at the potential V_{CS3}' are opposite in polarity to each other.

[0161] According to the foregoing configuration, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period, the absolute value of the voltage that is applied to the liquid crystal can be made sufficiently small.

[0162] Therefore, according to the foregoing configuration, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, a black display can be carried out at a sufficiently low brightness, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period.

[0163] Further, according to this example of operation, it is preferable that an absolute value of a potential difference

between the middle voltage level among the first to third voltage levels and the highest voltage level among the first to third voltage levels be twice or less as great as a threshold voltage of the liquid crystal. That is, according to this example of operation, it is preferable that the absolute value of the potential difference between the middle potential V_{CS2}' among the potentials V_{CS1}' , V_{CS2}' , and V_{CS3}' and the highest potential V_{CS3}' among the potentials V_{CS1}' , V_{CS2}' , and V_{CS3}' be twice or less as great as the threshold voltage of the liquid crystal.

[0164] According to the foregoing configuration, the absolute value of the potential difference between the middle voltage level among the first to third voltage levels and the highest voltage level among the first to third voltage levels is twice or less as great as the threshold voltage of the liquid crystal; that is, in this example, the absolute value of the potential difference between the middle potential V_{CS2}' among the potentials V_{CS1}' , V_{CS2}' , and V_{CS3}' and the highest potential V_{CS3}' among the potentials V_{CS1}' , V_{CS2}' , and V_{CS3}' is twice or less as great as the threshold voltage of the liquid crystal. This makes it possible to prevent the orientation of the liquid crystal from being affected, regardless of which of the first to third voltage levels the rectangular voltage signal takes on.

[0165] Therefore, according to the foregoing configuration, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, a black display can be carried out regardless of which of the first to third voltage levels the rectangular voltage signal takes on.

[0166] (Example 3 of Operation of the Display Panel 1)

[0167] A third example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) through (d) of FIG. 7 and (a) through (d) of FIG. 8.

[0168] First, a case where the source driver 12 supplies the source bus line SL_m with a source signal #SL_m corresponding to a high tone is described with reference to (a) through (d) of FIG. 7.

[0169] (a) of FIG. 7 is a timing chart showing an example of a waveform of the source signal #SL_m, which is supplied to the source bus line SL_m. As shown in (a) of FIG. 7, the waveform of the source signal #SL_m in this example of operation is described as being the same as the waveform of the source signal #SL_m shown in (a) of FIG. 3.

[0170] (b) of FIG. 7 is a timing chart showing a waveform of the gate signal #GL_n, which is supplied to the gate bus line GL_n. As shown in (b) of FIG. 7 the waveform of the gate signal #GL_n in this example of operation is described as being the same as the waveform of the gate signal #GL_n shown in (b) of FIG. 3.

[0171] (c) of FIG. 7 is a timing chart showing the common potential V_{COM} , which is supplied to the counter electrode wire COM_L, and a potential $V_{PEN,m}$ that is applied to the pixel electrode PE_{n,m}.

[0172] (d) of FIG. 7 is a timing chart showing a waveform of the auxiliary capacitor signal #CSL_n, which is supplied to the auxiliary capacitor bus line CSL_n. As shown in (d) of FIG. 7, the auxiliary capacitor signal #CSL_n in this example of operation is a signal that takes on a potential V_{CS1}' , a potential V_{CS2}' , a potential V_{CS3}' , and a potential V_{CS4}' in a single cycle composed of two consecutive vertical scanning periods T_{V''}. More specifically, as shown in (d) of FIG. 7, the auxiliary capacitor signal #CSL_n takes on the potential V_{CS2}' during a

period T_1 " in a single vertical scanning period T_V ", and takes on the potential V_{CS3} " during a period T_2 ". Further, the auxiliary capacitor signal #CSL_n takes on the potential V_{CS4} " during a period T_3 " in the ensuing vertical scanning period T_V ", and takes on the potential V_{CS1} " during a period T_4 ". It is assumed that as shown in (d) of FIG. 7, specific values of the potentials V_{CS1} ", V_{CS2} ", V_{CS3} ", and V_{CS4} " satisfy $V_{CS1}" < V_{CS2}" < V_{CS4}" < V_{CS3}"$ and $V_{CS2}" - V_{CS1}" < V_{CS3}" - V_{CS2}"$, as well as $V_{CS3}" - V_{CS4}" < V_{CS4}" - V_{CS1}"$.

[0173] As shown in (c) and (d) of FIG. 7, when the auxiliary capacitor signal #CSL_n is at the lowest potential (potential V_{CS1} "") and the gate signal #GL_n is at a high level, the voltage that is applied to the liquid crystal LC changes into a positive polarity; and when the auxiliary capacitor signal #CSL_n is at the highest potential (potential V_{CS3} "") and the gate signal #GL_n is at a high level, the voltage that is applied to the liquid crystal LC changes into a negative polarity.

[0174] The following describes the operation of each of the components in the pixel region $P_{n,m}$ of the display panel 1 in this example of operation.

[0175] First, as shown in (b) of FIG. 7, the gate signal #GL_n rises from a low level to a high level at the time t_1 " and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor $M_{n,m}$ is in a conducting state. When the transistor $M_{n,m}$ is in a conducting state, the source signal #SL_m is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$. As shown in (c) of FIG. 7, in a period from the time t_1 " to the time t_2 ", the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, rises from a potential V_1 " to a potential V_2 " (which is positive).

[0176] Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS1} " to the potential V_{CS2} " at the time t_2 ". Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_2 " to a potential V_3 ". It should be noted here that a specific value of the potential V_3 " is defined as:

$$V_3 = (V_{CS2} - V_{CS1}) \times C_{CS} / \Sigma C + V_2.$$

Since $V_{CS1}" < V_{CS2}"$ as mentioned above, the potential V_3 " is greater than the potential V_2 ".

[0177] Then, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS2} " to the potential V_{CS3} " at the time t_3 ". Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_3 " to a potential V_4 ". It should be noted here that a specific value of the potential V_4 " is defined as:

$$V_4 = (V_{CS3} - V_{CS2}) \times C_{CS} / \Sigma C + V_3.$$

Since $V_{CS2}" < V_{CS3}"$ as mentioned above, the potential V_4 " is greater than the potential V_3 ".

[0178] Further, as shown in (c) of FIG. 7, the potential difference between the potential V_4 " and the common potential V_{COM} is greater than the potential difference between the potential V_3 " and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_3 " to the time t_4 " is greater than the transmittance of the liquid crystal LC in a period from the time t_2 " to the time t_3 ". That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_3 " to the time t_4 " is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_2 " to the time t_3 ".

[0179] Then, the gate signal #GL_n rises from a low level to a high level at the time t_4 " and, after a certain period of time has elapsed, falls to a low level. In a period of time during

which the gate signal #GL_n is at a high level, the transistor $M_{n,m}$ is in a conducting state, so that the source signal #SL_m is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$.

[0180] As shown in (a) of FIG. 7, in a period from the time t_4 " to the time t_5 ", the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, falls from the potential V_4 " to a potential V_5 " (which is negative).

[0181] Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS3} " to the potential V_{CS4} " at the time t_5 ". Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_5 " to a potential V_6 ". It should be noted here that a specific value of the potential V_6 " is defined as:

$$V_6 = (V_{CS4} - V_{CS3}) \times C_{CS} / \Sigma C + V_5.$$

Since $V_{CS4}" < V_{CS3}"$ as mentioned above, the potential V_6 " is smaller than the potential V_5 ".

[0182] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS4} " to the potential V_{CS1} " at the time t_6 ". Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_6 " to the potential V_1 ". It should be noted here that a specific value of the potential V_1 " is defined as:

$$V_1 = (V_{CS1} - V_{CS4}) \times C_{CS} / \Sigma C + V_6.$$

Since $V_{CS1}" < V_{CS4}"$ as mentioned above, the potential V_1 " is smaller than the potential V_6 ".

[0183] Further, as shown in (c) of FIG. 7, the potential difference between the potential V_1 " and the common potential V_{COM} is greater than the potential difference between the potential V_6 " and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_6 " to the time t_7 " is greater than the transmittance of the liquid crystal LC in a period from the time t_5 " to the time t_6 ". That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_6 " to the time t_7 " is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_5 " to the time t_6 ".

[0184] The operation at the time t_7 " and later is the same as the operation at the time t_1 " and later.

[0185] The above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS1} " to the potential V_{CS2} " at the time t_2 " and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS3} " to the potential V_{CS4} " at the time t_5 ". However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS1} " to the potential V_{CS4} " before several horizontal periods (period multiple times as long as a horizontal period T_h) have elapsed since the time t_2 " and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS3} " to the potential V_{CS2} " before several horizontal periods (period multiple times as long as a horizontal period T_h) have elapsed since the time t_5 ".

[0186] Further, according to this example of operation, in the single scanning period (single vertical scanning period T_V "), the auxiliary capacitor driver 14 supplies the given auxiliary capacitor bus line CSL_n with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels, and in a single scanning period subsequent to the single scanning period (single vertical scanning period T_V "), the auxiliary capacitor driver 14 supplies the given auxiliary capacitor bus

line CSL_n with a rectangular voltage signal (auxiliary capacitor signal # CSL_n) in synchronization with the conducting signal, the rectangular voltage signal being composed of any two of the first to third voltage levels and a fourth voltage level that is different from the first to third voltage levels.

[0187] That is, according to this example of operation, in the two consecutive vertical scanning periods, the auxiliary capacitor driver 14 supplies a rectangular voltage signal (auxiliary capacitor signal # CSL_n) composed of the potential V_{CS1} , the potential V_{CS2} , the potential V_{CS3} , and the potential V_{CS4} .

[0188] Therefore, according to this example of operation, in the single scanning period, the auxiliary capacitor driver 14 can supply the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels. Therefore, in the single scanning period, the level of voltage that is applied to the given auxiliary capacitor bus line switches among three values. In other words, in the single scanning period, the level of voltage that is applied to the auxiliary capacitor bus line makes two transitions. The first transition between the voltage levels in the single scanning period causes a voltage that is applied to the liquid crystal after the first transition between the voltage levels to be suitable for a display after the first transition between the voltage levels, and the second transition between the voltage levels allows switching between a high brightness and a low brightness.

[0189] Therefore, the foregoing configuration makes a display at a higher brightness possible while effectively suppressing the phenomenon of blurring of moving images.

[0190] Furthermore, the foregoing configuration makes it possible, in a single scanning period subsequent to the single scanning period, to supply a rectangular voltage signal composed of any two of the first to third voltage levels and a fourth voltage level that is different from the first to third voltage levels. Therefore, as compared with a case where a rectangular voltage signal composed of the first to third voltage levels is supplied in a single scanning period subsequent to the single scanning period, the adjustment of brightness levels between a high brightness and a low brightness can be more flexibly carried out.

[0191] Therefore, the foregoing configuration makes a display at a high brightness possible while further effectively suppressing the phenomenon of blurring of moving images.

[0192] Further, in the display panel according to the present invention, the absolute value $|V_{CS2} - V_{CS1}|$ of the potential difference between the voltage level before a first transition between the voltage levels in the single scanning period (single vertical scanning period T_V) and the voltage level after the first transition is smaller than the absolute value $|V_{CS3} - V_{CS2}|$ of the potential difference between the voltage level before a next transition between the voltage levels in the single scanning period and the voltage level after the next transition. It is assumed here that the symbol $|a|$ represents the absolute value of a .

[0193] Therefore, in this example of operation, a change in brightness of the pixel region $P_{n,m}$ along with a transition between the voltage levels of the auxiliary capacitor signal # CSL_n at the time t_3 can be made larger while maintaining the effect of enhancing the brightness.

[0194] Therefore, in this example of operation, the phenomenon of blurring of moving images can be more effectively suppressed. The same applies to the single vertical scanning period T_V from the time t_5 to the time t_8 .

[0195] Next, a case where the source driver 12 supplies the source bus line SL_m with a source signal # SL_m corresponding to a low tone is described with reference to (a) through (d) of FIG. 8. It should be noted that overlaps with the foregoing description are not described below.

[0196] (a) of FIG. 8 is a timing chart showing an example of a waveform of the source signal # SL_m , which is supplied to the source bus line SL_m . This waveform is the same as the waveform of the source signal # SL_m shown in (a) of FIG. 6.

[0197] (b) of FIG. 8 is a timing chart showing a waveform of the gate signal # GL_n , which is supplied to the gate bus line GL_n . As shown in (b) of FIG. 8, the waveform of the gate signal # GL_n in this example of operation is described as being the same as the waveform of the gate signal # GL_n shown in (b) of FIG. 3.

[0198] (c) of FIG. 8 is a timing chart showing the common potential V_{COM} , which is supplied to the counter electrode wire COML, and a potential $V_{PEN,m}$ that is applied to the pixel electrode $PE_{n,m}$.

[0199] (d) of FIG. 8 is a timing chart showing a waveform of the auxiliary capacitor signal # CSL_n , which is supplied to the auxiliary capacitor bus line CSL_n . The waveform shown in (d) of FIG. 8 is the same as that shown in (d) of FIG. 6.

[0200] First, as shown in (b) of FIG. 8, the gate signal # GL_n rises from a low level to a high level at the time t_1 and, after a certain period of time has elapsed, falls to a low level. As shown in (a) of FIG. 8, in the period from the time t_1 to the time t_2 , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, falls from a potential V_{01} to a potential V_{02} .

[0201] Further, the auxiliary capacitor signal # CSL_n rises from the potential V_{CS1} to the potential V_{CS2} at the time t_2 . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{02} , for example, to the potential V_{01} .

[0202] Then, the auxiliary capacitor signal # CSL_n rises from the potential V_{CS2} to the potential V_{CS3} at the time t_3 . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{01} to a potential V_{03} . It should be noted here that a specific value of the potential V_{03} is defined as:

$$V_{03} = (V_{CS3} - V_{CS2}) \times C_{CS} / \Sigma C + V_0.$$

Since $V_{CS2} < V_{CS3}$ as mentioned above, the potential V_{03} is greater than the potential V_{01} .

[0203] Then, the gate signal # GL_n rises from a low level to a high level at the time t_4 and, after a certain period of time has elapsed, falls to a low level. As shown in (c) of FIG. 8, in the period from the time t_4 to the time t_5 , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, rises from the potential V_{03} to a potential V_{04} .

[0204] Further, the auxiliary capacitor signal # CSL_n falls from the potential V_{CS3} to the potential V_{CS4} at the time t_5 . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{04} , for example, to the potential V_{03} .

[0205] Then, the auxiliary capacitor signal # CSL_n falls from the potential V_{CS4} to the potential V_{CS1} at the time t_6 .

Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{03} , for example, to the potential V_{01} .

[0206] The operation at the time t_7 and later is the same as the operation at the time t_1 and later.

[0207] As shown in (c) of FIG. 8, the absolute value of the potential difference between the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ and the common potential V_{COM} is always kept substantially constant throughout all the periods. That is, the transmittance of the liquid crystal LC of the pixel region $P_{n,m}$ can be kept substantially constant even in a case where the value of the auxiliary capacitor signal $\#CSL_n$ is changed as shown in (d) of FIG. 8.

[0208] Each of the above examples 1 to 3 of operation has described a case where the brightness of the pixel region $P_{n,m}$ in the second half of a single vertical scanning period is greater than the brightness of the pixel region $P_{n,m}$ in the first half of the single vertical scanning period. However, the present invention is not to be limited to these examples. In the following, examples 4 to 6 of operation, where the brightness of the pixel region $P_{n,m}$ in the second half of a single vertical scanning period is smaller than the brightness of the pixel region $P_{n,m}$ in the first half of the single vertical scanning period, are described with reference to FIGS. 9 through 11.

[0209] According to this example of operation, in the single scanning period single vertical scanning period T_V , a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode after a first transition between the voltage levels and a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and the potential of the counter electrode after a next transition between the voltage levels are polarities that are different from each other. That is, a voltage that is applied to the liquid crystal as represented by a difference between the potential V_{01} of the pixel electrode $PE_{n,m}$ and the potential V_{COM} of the counter electrode when the auxiliary capacitor signal $\#CSL_n$ is at the potential V_{CS2} and a voltage that is applied to the liquid crystal as represented by a difference between the potential V_{03} of the pixel electrode $PE_{n,m}$ and the potential V_{COM} of the counter electrode when the auxiliary capacitor signal $\#CSL_n$ is at the potential V_{CS3} are opposite in polarity to each other.

[0210] According to the foregoing configuration, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period, the absolute value of the voltage that is applied to the liquid crystal can be made sufficiently small.

[0211] Therefore, according to the foregoing configuration, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, a black display can be carried out at a sufficiently low brightness, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period.

[0212] Further, according to this example of operation, it is preferable that an absolute value of a potential difference between the second lowest voltage level among the first to fourth voltage levels and the highest voltage level among the first to fourth voltage levels be twice or less as great as a threshold voltage of the liquid crystal. That is, according to

this example of operation, it is preferable that the absolute value of the potential difference between the second lowest potential V_{CS2} among the potentials V_{CS1} , V_{CS2} , V_{CS3} , and V_{CS4} and the highest potential V_{CS3} among the potentials V_{CS1} , V_{CS2} , V_{CS3} , and V_{CS4} be twice or less as great as the threshold voltage of the liquid crystal.

[0213] According to the foregoing configuration, it is preferable that the absolute value of the potential difference between the second lowest voltage level among the first to fourth voltage levels and the highest voltage level among the first to fourth voltage levels be twice or less as great as the threshold voltage of the liquid crystal. That is, according to this example of operation, the absolute value of the potential difference between the second lowest potential V_{CS2} among the potentials V_{CS1} , V_{CS2} , V_{CS3} , and V_{CS4} and the highest potential V_{CS3} among the potentials V_{CS1} , V_{CS2} , V_{CS3} , and V_{CS4} is twice or less as great as the threshold voltage of the liquid crystal. This makes it possible to prevent the orientation of the liquid crystal from being affected, regardless of which of the third and fourth voltage levels the rectangular voltage signal takes on.

[0214] Therefore, according to the foregoing configuration, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, a black display can be carried out regardless of which of the first to fourth voltage levels the rectangular voltage signal takes on.

[0215] (Example 4 of Operation of the Display Panel 1)

[0216] A fourth example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) through (d) of FIG. 9.

[0217] (a) of FIG. 9 is a timing chart showing an example of a waveform of the source signal $\#SL_m$, which is supplied to the source bus line SL_m . As shown in (a) of FIG. 9, the waveform of the source signal $\#SL_m$ in this example of operation is described as being substantially the same as the waveform of the source signal $\#SL_m$ shown in (a) of FIG. 3.

[0218] (b) of FIG. 9 is a timing chart showing a waveform of the gate signal $\#GL_n$, which is supplied to the gate bus line GL_n . As shown in (b) of FIG. 9, the waveform of the gate signal $\#GL_n$ in this example of operation is described as being the same as the waveform of the gate signal $\#GL_n$ shown in (b) of FIG. 3.

[0219] (c) of FIG. 9 is a timing chart showing the common potential V_{COM} , which is supplied to the counter electrode wire COM_L , and a potential $V_{PEN,m}$ that is applied to the pixel electrode $PE_{n,m}$.

[0220] (d) of FIG. 9 is a timing chart showing a waveform of the auxiliary capacitor signal $\#CSL_n$, which is supplied to the auxiliary capacitor bus line CSL_n . As shown in (d) of FIG. 9, the auxiliary capacitor signal $\#CSL_n$ in this example of operation is a signal that takes on a potential V_{CS11} and a potential V_{CS12} in a single cycle composed of two consecutive vertical scanning periods T_V . More specifically, as shown in (d) of FIG. 9, the auxiliary capacitor signal $\#CSL_n$ takes on the potential V_{CS12} during a period T_{11} in a single vertical scanning period T_V , takes on the potential V_{CS11} from a time t_{13} to a time t_{14} in a period T_{12} , and takes on the potential V_{CS12} from the time t_{14} to a time t_{15} in the period T_{12} . Further, the auxiliary capacitor signal $\#CSL_n$ takes on the potential V_{CS11} during a period T_{13} in the ensuing vertical scanning period T_V , takes on the potential V_{CS12} from a time t_{16} to a time t_{17} in a period T_{14} , and takes on the potential V_{CS11} from the time t_{17} to a time t_{18} in the period T_{14} . It is assumed that as

shown in (d) of FIG. 9, specific values of the potentials V_{CS11} and V_{CS12} satisfy $V_{CS11} < V_{CS12}$.

[0221] The following describes the operation of each of the components in the pixel region $P_{n,m}$ of the display panel 1 in this example of operation.

[0222] First, as shown in (b) of FIG. 9, the gate signal #GL_n rises from a low level to a high level at the time t_{11} and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor $M_{n,m}$ is in a conducting state. When the transistor $M_{n,m}$ is in a conducting state, the source signal #SL_m is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$. As shown in (c) of FIG. 9, in a period from the time t_{11} to the time t_{12} , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, rises from a potential V_{11} to a potential V_{12} (which is positive).

[0223] Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t_{12} . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{12} to a potential V_{13} . It should be noted here that a specific value of the potential V_{13} is defined as:

$$V_{13} = (V_{CS12} - V_{CS11}) \times C_{CS} / \Sigma C + V_{12}.$$

Since $V_{CS11} < V_{CS12}$ as mentioned above, the potential V_{13} is greater than the potential V_{12} .

[0224] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} at the time t_{13} . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{13} to the potential V_{12} .

[0225] Further, as shown in (c) of FIG. 9, the potential difference between the potential V_{13} and the common potential V_{COM} is greater than the potential difference between the potential V_{12} and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_{12} to the time t_{13} is greater than the transmittance of the liquid crystal LC in a period from the time t_{13} to the time t_{14} . That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_{12} to the time t_{13} is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_{13} to the time t_{14} .

[0226] Then, the gate signal #GL_n rises from a low level to a high level at the time t_{14} and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor $M_{n,m}$ is in a conducting state, and the source signal #SL_m is supplied to the pixel electrode $PE_{n,m}$ and the first auxiliary capacitor electrode $CE1_{n,m}$. Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t_{14} .

[0227] As shown in (a) of FIG. 9, in the period from the time t_{14} to the time t_{15} , the potential $V_{PEN,m}$, which is applied to the pixel electrode $PE_{n,m}$, falls from the potential V_{12} , for example, to the potential V_{11} .

[0228] Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} at the time t_{15} . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{11} to a potential V_{14} . It should be noted here that a specific value of the potential V_{14} is defined as:

$$V_{14} = (V_{CS11} - V_{CS12}) \times C_{CS} / \Sigma C + V_{11}.$$

Since $V_{CS11} < V_{CS12}$ as mentioned above, the potential V_{14} is smaller than the potential V_{11} .

[0229] Then, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t_{16} . Accordingly, the potential $V_{PEN,m}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{14} to the potential V_{11} .

[0230] As shown in (c) of FIG. 9, the potential difference between the potential V_{14} and the common potential V_{COM} is greater than the potential difference between the potential V_{11} and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_{15} to the time t_{16} is greater than the transmittance of the liquid crystal LC in a period from the time t_{16} to the time t_{17} . That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_{15} to the time t_{16} is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_{16} to the time t_{17} .

[0231] Then, the gate signal #GL_n rises from a low level to a high level at the time t_{17} and, after a certain period of time has elapsed, falls to a low level. Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} . The operation at the time t_{17} and later is the same as the operation at the time t_{11} and later.

[0232] The above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t_{12} and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} at the time t_{15} . However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t_{12} and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t_{15} .

[0233] Further, the above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t_{14} . However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} in a period from the time t_{13} to the time t_{15} .

[0234] As in this example of operation, the display panel 1 according to the present invention can also cause a change in brightness of the pixel region $P_{n,m}$ in a single vertical scanning period by supplying the auxiliary capacitor signal #CSL_n in such a way that the brightness of the pixel region $P_{n,m}$ in the second half of a single vertical scanning period is smaller than the brightness of the pixel region $P_{n,m}$ in the first half of the single vertical scanning period.

[0235] Therefore, in this example of operation, too, the phenomenon of blurring of moving images can be suppressed.

[0236] (Example 5 of Operation of the Display Panel 1)

[0237] A fifth example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) through (d) of FIG. 10.

[0238] (a) of FIG. 10 is a timing chart showing an example of a waveform of the source signal #SL_m, which is supplied to the source bus line SL_m. As shown in (a) of FIG. 10, the waveform of the source signal #SL_m in this example of operation is described as being substantially the same as the waveform of the source signal #SL_m shown in (a) of FIG. 3.

[0239] (b) of FIG. 10 is a timing chart showing a waveform of the gate signal #GL_n, which is supplied to the gate bus line GL_n. As shown in (b) of FIG. 10, the waveform of the gate

signal #GL_n in this example of operation is described as being substantially the same as the waveform of the gate signal #GL_n shown in (b) of FIG. 3.

[0240] (c) of FIG. 10 is a timing chart showing the common potential V_{COM}, which is supplied to the counter electrode wire COML, and a potential V_{PE_{n,m}} that is applied to the pixel electrode PE_{n,m}.

[0241] (d) of FIG. 10 is a timing chart showing a waveform of the auxiliary capacitor signal #CSL_n, which is supplied to the auxiliary capacitor bus line CSL_n. As shown in (d) of FIG. 10, the auxiliary capacitor signal #CSL_n in this example of operation is a signal that takes on a potential V_{CS11}, a potential V_{CS12}, and a potential V_{CS13} in a single cycle composed of two consecutive vertical scanning periods T_v. More specifically, as shown in (d) of FIG. 10, the auxiliary capacitor signal #CSL_n takes on the potential V_{CS12} during a period T₁₁ in a single vertical scanning period T_v, takes on the potential V_{CS13} from a time t₁₃ to a time t₁₄ in a period T₁₂, and takes on the potential V_{CS12} from the time t₁₄ to a time t₁₅ in the period T₁₂. Further, the auxiliary capacitor signal #CSL_n takes on the potential V_{CS11} during a period T₁₃ in the ensuing vertical scanning period T_v, takes on the potential V_{CS13} from a time t₁₆ to a time t₁₇ in a period T₁₄, and takes on the potential V_{CS11} from the time t₁₇ to a time t₁₈ in the period T₁₄. It is assumed that as shown in (d) of FIG. 10, specific values of the potentials V_{CS11}, V_{CS12}, and V_{CS13} satisfy V_{CS11} < V_{CS13} < V_{CS12}.

[0242] The following describes the operation of each of the components in the pixel region P_{n,m} of the display panel 1 in this example of operation.

[0243] First, as shown in (b) of FIG. 10, the gate signal #GL_n rises from a low level to a high level at the time t₁₁ and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor M_{n,m} is in a conducting state. When the transistor M_{n,m} is in a conducting state, the source signal #SL_m is supplied to the pixel electrode PE_{n,m} and the first auxiliary capacitor electrode CE1_{n,m}. As shown in (a) of FIG. 10, in a period from the time t₁₁ to the time t₁₂, the potential V_{PE_{n,m}}, which is applied to the pixel electrode PE_{n,m}, rises from a potential V₁₁ to a potential V₁₂ (which is positive).

[0244] Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t₁₂. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₁₂ to a potential V₁₃. It should be noted here that a specific value of the potential V₁₃ is defined as:

$$V_{13} = (V_{CS12} - V_{CS11}) \times C_{CS} / \Sigma C + V_{12}.$$

Since V_{CS11} < V_{CS12} as mentioned above, the potential V₁₃ is greater than the potential V₁₂.

[0245] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS13} at the time t₁₃. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₁₃ to a potential V₁₄. It should be noted here that a specific value of the potential V₁₄ is defined as:

$$V_{14} = (V_{CS13} - V_{CS12}) \times C_{CS} / \Sigma C + V_{13}.$$

Since V_{CS13} < V_{CS12} as mentioned above, the potential V₁₄ is smaller than the potential V₁₃.

[0246] As shown in (c) of FIG. 10, the potential difference between the potential V₁₃ and the common potential V_{COM} is greater than the potential difference between the potential V₁₄ and the common potential V_{COM}. That is, the transmittance of the liquid crystal LC in a period from the time t₁₂ to the time t₁₃ is greater than the transmittance of the liquid crystal LC in a period from the time t₁₃ to the time t₁₄. That is, the brightness of the pixel region P_{n,m} in the period from the time t₁₂ to the time t₁₃ is greater than the brightness of the pixel region P_{n,m} in the period from the time t₁₃ to the time t₁₄.

Then, the gate signal #GL_n rises from a low level to a high level at the time t₁₄ and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor M_{n,m} is in a conducting state, and the source signal #SL_m is supplied to the pixel electrode PE_{n,m} and the first auxiliary capacitor electrode CE1_{n,m}. Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS13} to the potential V_{CS12} at the time t₁₄.

[0247] As shown in (c) of FIG. 10, in the period from the time t₁₄ to the time t₁₅, the potential V_{PE_{n,m}}, which is applied to the pixel electrode PE_{n,m}, falls from the potential V₁₄ to a potential V₁₅ (which is negative).

[0249] Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} at the time t₁₅. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₁₅ to a potential V₁₆. It should be noted here that a specific value of the potential V₁₆ is defined as:

$$V_{16} = (V_{CS11} - V_{CS12}) \times C_{CS} / \Sigma C + V_{15}.$$

Since V_{CS11} < V_{CS12} as mentioned above, the potential V₁₆ is smaller than the potential V₁₅.

[0250] Then, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS13} at the time t₁₆. Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₁₆ to the potential V₁₁.

[0251] As shown in (c) of FIG. 10, the potential difference between the potential V₁₆ and the common potential V_{COM} is greater than the potential difference between the potential V₁₁ and the common potential V_{COM}. That is, the transmittance of the liquid crystal LC in a period from the time t₁₅ to the time t₁₆ is greater than the transmittance of the liquid crystal LC in a period from the time t₁₆ to the time t₁₇. That is, the brightness of the pixel region P_{n,m} in the period from the time t₁₅ to the time t₁₆ is greater than the brightness of the pixel region P_{n,m} in the period from the time t₁₆ to the time t₁₇.

[0252] Then, the gate signal #GL_n rises from a low level to a high level at the time t₁₇ and, after a certain period of time has elapsed, falls to a low level. Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11}. The operation at the time t₁₇ and later is the same as the operation at the time t₁₁ and later.

[0253] The above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t₁₂ and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} at the time t₁₅. However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t₁₂ and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t₁₅.

[0254] Further, the above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS13}' to the potential V_{CS12}' at the time t₁₄'. However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS13}' to the potential V_{CS12}' in a period from the time t₁₃' to the time t₁₅'.

[0255] As in this example of operation, the display panel 1 according to the present invention can also cause a change in brightness of the pixel region P_{n,m} in a single vertical scanning period by supplying the auxiliary capacitor signal #CSL_n in such a way that the brightness of the pixel region P_{n,m} in the second half of a single vertical scanning period is smaller than the brightness of the pixel region P_{n,m} in the first half of the single vertical scanning period.

[0256] Therefore, in this example of operation, too, the phenomenon of blurring of moving images can be suppressed. Further, in this example of operation, the auxiliary capacitor signal #CSL_n takes on a three-valued voltage level. Therefore, as compared with the example 4 of operation described above, a display at a high brightness can be carried out while maintaining the effect of suppressing the phenomenon of blurring of moving images.

[0257] (Example 6 of Operation of the Display Panel 1)

[0258] A sixth example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) through (d) of FIG. 11.

[0259] (a) of FIG. 11 is a timing chart showing an example of a waveform of the source signal #SL_m, which is supplied to the source bus line SL_m. As shown in (a) of FIG. 11, the waveform of the source signal #SL_m in this example of operation is described as being substantially the same as the waveform of the source signal #SL_m shown in (a) of FIG. 3.

[0260] (b) of FIG. 11 is a timing chart showing a waveform of the gate signal #GL_n, which is supplied to the gate bus line GL_n. As shown in (b) of FIG. 11, the waveform of the gate signal #GL_n in this example of operation is described as being substantially the same as the waveform of the gate signal #GL_n shown in (b) of FIG. 3.

[0261] (c) of FIG. 11 is a timing chart showing the common potential V_{COM}, which is supplied to the counter electrode wire COML, and a potential V_{PE_{n,m}} that is applied to the pixel electrode PE_{n,m}.

[0262] (d) of FIG. 11 is a timing chart showing a waveform of the auxiliary capacitor signal #CSL_n, which is supplied to the auxiliary capacitor bus line CSL_n. As shown in (d) of FIG. 11, the auxiliary capacitor signal #CSL_n in this example of operation is a signal that takes on a potential V_{CS11}", a potential V_{CS12}", a potential V_{CS13}", and a potential V_{CS14}" in a single cycle composed of two consecutive vertical scanning periods T_v". More specifically, as shown in (d) of FIG. 11, the auxiliary capacitor signal #CSL_n takes on the potential V_{CS12}" during a period T₁₁" in a single vertical scanning period T_v", takes on the potential V_{CS13}" from a time t₁₃" to a time t₁₄" in a period T₁₂", and takes on the potential V_{CS12}" from the time t₁₄" to a time t₁₅" in the period T₁₂". Further, the auxiliary capacitor signal #CSL_n takes on the potential V_{CS11}" during a period T₁₃" in the ensuing vertical scanning period T_v", takes on the potential V_{CS14}" from a time t₁₆" to a time t₁₇" in a period T₁₄", and takes on the potential V_{CS11}" from the time t₁₇" to a time t₁₈" in the period T₁₄". It is assumed that as shown in (d) of FIG. 11, specific values of the potentials V_{CS11}", V_{CS12}", V_{CS13}", and V_{CS14}" satisfy V_{CS11}" < V_{CS13}" < V_{CS14}" < V_{CS12}".

[0263] The following describes the operation of each of the components in the pixel region P_{n,m} of the display panel 1 in this example of operation.

[0264] First, as shown in (b) of FIG. 11, the gate signal #GL_n rises from a low level to a high level at the time t₁₁" and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor M_{n,m} is in a conducting state. When the transistor M_{n,m} is in a conducting state, the source signal #SL_m is supplied to the pixel electrode PE_{n,m} and the first auxiliary capacitor electrode CE1_{n,m}. As shown in (c) of FIG. 11, in a period from the time t₁₁" to the time t₁₂", the potential V_{PE_{n,m}}, which is applied to the pixel electrode PE_{n,m}, rises from a potential V₁₁" to a potential V₁₂" (which is positive).

[0265] Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11}" to the potential V_{CS12}" at the time t₁₂". Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₁₂" to a potential V₁₃". It should be noted here that a specific value of the potential V₁₃" is defined as:

$$V_{13} = (V_{CS12} - V_{CS11}) \times C_{CS} / \Sigma C + V_{12}.$$

Since V_{CS11}" < V_{CS12}" as mentioned above, the potential V₁₃" is greater than the potential V₁₂".

[0266] Then, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12}" to the potential V_{CS13}" at the time t₁₃". Accordingly, the potential V_{PE_{n,m}} of the pixel electrode PE_{n,m} changes from the potential V₁₃" to a potential V₁₄". It should be noted here that a specific value of the potential V₁₄" is defined as:

$$V_{14} = (V_{CS13} - V_{CS12}) \times C_{CS} / \Sigma C + V_{13}.$$

Since V_{CS13}" < V_{CS12}" as mentioned above, the potential V₁₄" is smaller than the potential V₁₃".

[0267] As shown in (c) of FIG. 11, the potential difference between the potential V₁₃" and the common potential V_{COM} is greater than the potential difference between the potential V₁₄" and the common potential V_{COM}. That is, the transmittance of the liquid crystal LC in a period from the time t₁₂" to the time t₁₃" is greater than the transmittance of the liquid crystal LC in a period from the time t₁₃" to the time t₁₄". That is, the brightness of the pixel region P_{n,m} in the period from the time t₁₂" to the time t₁₃" is greater than the brightness of the pixel region P_{n,m} in the period from the time t₁₃" to the time t₁₄".

[0268] Then, the gate signal #GL_n rises from a low level to a high level at the time t₁₄" and, after a certain period of time has elapsed, falls to a low level. In a period of time during which the gate signal #GL_n is at a high level, the transistor M_{n,m} is in a conducting state, and the source signal #SL_m is supplied to the pixel electrode PE_{n,m} and the first auxiliary capacitor electrode CE1_{n,m}. Further, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS13}" to the potential V_{CS12}" at the time t₁₄".

[0269] As shown in (a) of FIG. 11, in the period from the time t₁₄" to the time t₁₅", the potential V_{PE_{n,m}}, which is applied to the pixel electrode PE_{n,m}, falls from the potential V₁₄" to a potential V₁₅" (which is negative).

[0270] Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12}" to the potential V_{CS11}" at the time t₁₅". Accordingly, the potential V_{PE_{n,m}} of the pixel electrode

$PE_{n,m}$ changes from the potential V_{15} to a potential V_{16} . It should be noted here that a specific value of the potential V_{16} is defined as:

$$V_{16} = (V_{CS11} - V_{CS12}) \times C_{CS} \Sigma C + V_{15}.$$

Since $V_{CS11} < V_{CS12}$ as mentioned above, the potential V_{16} is smaller than the potential V_{15} .

[0271] Then, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS14} at the time t_{16} . Accordingly, the potential $V_{PE_{n,m}}$ of the pixel electrode $PE_{n,m}$ changes from the potential V_{16} to a potential V_{17} . It should be noted here that a specific value of the potential V_{17} is defined as:

$$V_{17} = (V_{CS14} - V_{CS11}) \times C_{CS} \Sigma C + V_{16}.$$

Since $V_{CS11} < V_{CS14}$ as mentioned above, the potential V_{17} is greater than the potential V_{16} .

[0272] As shown in (c) of FIG. 11, the potential difference between the potential V_{16} and the common potential V_{COM} is greater than the potential difference between the potential V_{17} and the common potential V_{COM} . That is, the transmittance of the liquid crystal LC in a period from the time t_{15} to the time t_{16} is greater than the transmittance of the liquid crystal LC in a period from the time t_{16} to the time t_{17} . That is, the brightness of the pixel region $P_{n,m}$ in the period from the time t_{15} to the time t_{16} is greater than the brightness of the pixel region $P_{n,m}$ in the period from the time t_{16} to the time t_{17} .

[0273] Then, the gate signal #GL_n rises from a low level to a high level at the time t_{17} and, after a certain period of time has elapsed, falls to a low level. Further, the auxiliary capacitor signal #CSL_n falls from the potential V_{CS14} to the potential V_{CS11} . The operation at the time t_{17} and later is the same as the operation at the time t_{11} and later.

[0274] The above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} at the time t_{12} and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} at the time t_{15} . However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS11} to the potential V_{CS12} before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t_{12} and the auxiliary capacitor signal #CSL_n falls from the potential V_{CS12} to the potential V_{CS11} before several horizontal periods (period multiple times as long as a horizontal period Th) have elapsed since the time t_{15} .

[0275] Further, the above example of operation has described a case where the auxiliary capacitor signal #CSL_n rises from the potential V_{CS13} to the potential V_{CS12} at the time t_{14} . However, more generally, the auxiliary capacitor signal #CSL_n rises from the potential V_{CS13} to the potential V_{CS12} in a period from the time t_{13} to the time t_{15} .

[0276] As in this example of operation, the display panel 1 according to the present invention can also cause a change in brightness of the pixel region $P_{n,m}$ in a single vertical scanning period by supplying the auxiliary capacitor signal #CSL_n in such a way that the brightness of the pixel region $P_{n,m}$ in the second half of a single vertical scanning period is smaller than the brightness of the pixel region $P_{n,m}$ in the first half of the single vertical scanning period.

[0277] Therefore, in this example of operation, too, the phenomenon of blurring of moving images can be suppressed. Further, in this example of operation, the auxiliary capacitor signal #CSL_n takes on a four-valued voltage level.

Therefore, as compared with the examples 4 and 5 of operation, a display at a higher brightness can be carried out, and the phenomenon of blurring of moving images can be more effectively suppressed.

[0278] The above examples 1 to 6 of operation have been described by taking, as an example, the gate signal #GL_n that is supplied to the nth gate bus line GL_n and the auxiliary capacitor signal #CSL_n that is supplied to the nth auxiliary capacitor bus line CSL_n. However, the same applies to a gate signal #GL_p that is supplied to a gate bus line GL_p (p≠n) other than the nth gate bus line and a auxiliary capacitor signal #CSL_p that is supplied to an auxiliary capacitor bus line CSL_p (p≠n) other than the nth auxiliary capacitor bus line.

[0279] Further, the auxiliary capacitor driver 14 in the display panel 1 according to the present invention supplies the nth auxiliary capacitor bus line CSL_n with the auxiliary capacitor signal #CSL_n in synchronization with the gate signal #GL_n.

[0280] Furthermore, in a case where such a polarity reversal signal as that mentioned above is applied to the pixel electrode $PE_{n,m}$, i.e., in a case where the potential $V_{PE_{n,m}}$ of the pixel electrode $PE_{n,m}$ reverses its polarity with respect to the voltage V_{COM} of the counter electrode every single horizontal scanning period, the auxiliary capacitor driver 14 supplies an auxiliary capacitor signal #CSL_{n+1} in such a way that the auxiliary capacitor signal #CSL_{n+1} has its polarity reversed with respect to the polarity of the auxiliary capacitor signal #CSL_n.

[0281] (a) of FIG. 12 is a timing chart showing examples of waveforms of gate signals #GL_n to #GL_{n+3} that are supplied to the gate bus lines GL_n to GL_{n+3}, respectively. (b) of FIG. 12 is a timing chart showing examples of waveforms of auxiliary capacitor signals #CSL_n to #CSL_{n+3} that are supplied to the auxiliary capacitor bus lines CSL_n to CSL_{n+3}, respectively, in the example 1 of operation described above. (c) of FIG. 12 is a timing chart showing examples of waveforms of auxiliary capacitor signals #CSL_n to #CSL_{n+3} that are supplied to the auxiliary capacitor bus lines CSL_n to CSL_{n+3}, respectively, in the example 2 of operation described above.

[0282] In a case where as in the example 1 of operation, the potential level of an auxiliary capacitor signal during a selection period switches between the highest and lowest potential levels among a plurality of potential levels every single horizontal line period, i.e., in the case of line reversal driving, as shown in (b) and (c) of FIG. 12, the auxiliary capacitor driver 14 supplies the auxiliary capacitor signal #CSL_{n+1} in such a way that the auxiliary capacitor signal #CSL_{n+1} has its polarity reversed with respect to the polarity of the auxiliary capacitor signal #CSL_n.

[0283] Further, as shown in (b) and (c) of FIG. 12, the auxiliary capacitor driver 14 supplies the auxiliary capacitor bus line CSL_n with the auxiliary capacitor signals #CSL_n to #CSL_{n+3} in synchronization with the gate signals #GL_n to #GL_{n+3}, respectively.

[0284] Further, the same applies to the other gate signal #GL_q (q≦n-1, q≦n+4) and the other auxiliary capacitor signal #CSL_q (q≦n-1, q≦n+4).

[0285] In a case where the potential level of an auxiliary capacitor signal during a selection period switches between the highest and lowest potential levels among a plurality of potential levels every plural horizontal line periods, it is preferable the auxiliary capacitor driver 14 be configured to supply an auxiliary capacitor signal having its polarity reversed every plural auxiliary capacitor bus lines.

[0286] (Example 7 of Operation of the Display Panel 1)

[0287] The examples 1 to 6 of operation described above have been described by taking, as an example, a case where the auxiliary capacitor driver 14 supplies the plurality of auxiliary capacitor bus lines CSL_1 to CSL_N with the auxiliary capacitor signals $\#CSL_1$ to $\#CSL_N$, respectively, in sequence every horizontal scanning period Th , i.e., a case where there is a phase difference corresponding to the length of a horizontal scanning period Th between the auxiliary capacitor signal $\#CSL_n$ and the auxiliary capacitor signal $\#CSL_{n+1}$. However, the present invention is not to be limited to such an example.

[0288] A seventh example of operation of the display panel 1 according to the present embodiment is described below with reference to (a) and (b) of FIG. 13. Further, this example of operation is described by taking, as an example, a case where the potential level of an auxiliary capacitor signal during a selection period switches between the highest and lowest potential levels among a plurality of potential levels every two horizontal line periods.

[0289] (a) of FIG. 13 is a timing chart showing examples of waveforms of gate signals $\#GL_n$ to $\#GL_{n+3}$ that are supplied to the gate bus lines GL_n to GL_{n+3} , respectively. (b) of FIG. 13 is a timing chart showing examples of waveforms of auxiliary capacitor signals $\#CSL_n$ to $\#CSL_{n+3}$ that are supplied to the auxiliary capacitor bus lines CSL_n to CSL_{n+3} , respectively, in this example of operation.

[0290] As shown in (b) FIG. 13, the auxiliary capacitor driver supplies the auxiliary capacitor bus lines CSL_n and CSL_{n+1} with the auxiliary capacitor signals $\#CSL_n$ and $\#CSL_{n+1}$, which are in phase with each other. In other words, the auxiliary capacitor driver 14 supplies a pair of two adjacent auxiliary capacitor bus lines with a common auxiliary capacitor signal.

[0291] Thus, in this example of operation, the auxiliary capacitor driver 14 synchronously supplies the rectangular voltage signal (auxiliary capacitor signals $\#CSL_n$ and $\#CSL_{n+1}$) to the auxiliary capacitor bus line CSL_n connected via the transistor $M_{n,m}$ and the capacitor $C_{n,m}$ to the n th gate bus line GL_n of the plurality of gate bus lines GL_1 to GL_N , and to the auxiliary capacitor bus line CSL_{n+1} connected via the transistor $M_{n+1,m}$ and the capacitor $C_{n+1,m}$ to the $(n+1)$ th gate bus line GL_{n+1} of the plurality of gate bus lines GL_1 to GL_N .

[0292] As a configuration to supply a pair of auxiliary capacitor bus lines with a common auxiliary capacitor signal, for example, it is only necessary to generate the auxiliary capacitor signals $\#CSL_n$ and $\#CSL_{n+1}$ by using identical signal generating means in the auxiliary capacitor driver 14, and to supply the auxiliary capacitor signals $\#CSL_n$ and $\#CSL_{n+1}$ to the auxiliary capacitor bus lines CSL_n and CSL_{n+1} , respectively.

[0293] Therefore, in this example of operation, the phenomenon of blurring of moving images can be suppressed by the auxiliary capacitor driver 14 of a simpler configuration.

[0294] Further, the display panel according to the present invention may be configured such that the auxiliary capacitor driver 14 synchronously supplies the rectangular voltage signal (auxiliary capacitor signals $\#CSL_n$ and $\#CSL_{n+2}$) to the auxiliary capacitor bus line CSL_n connected via the transistor $M_{n,m}$ and the capacitor $C_{n,m}$ to the n th gate bus line GL_n of the plurality of gate bus lines GL_1 to GL_N , and to the auxiliary capacitor bus line CSL_{n+2} connected via the transistor $M_{n+2,m}$ and the capacitor $C_{n+2,m}$ to the $(n+2)$ th gate bus line GL_{n+2} of the plurality of gate bus lines GL_1 to GL_N .

[0295] According to the foregoing configuration, the auxiliary capacitor driver 14 of a simpler configuration brings about a further effect of making it possible to suppress the phenomenon of blurring of moving images while suppressing the occurrence of flickers and streaks corresponding to polarity reversal.

[0296] Further, the auxiliary capacitor driver 14 may be configured to supply a set of three or more adjacent auxiliary capacitor bus lines with a common auxiliary capacitor signal.

[0297] As described above in the examples 1 to 7 of operation, in a single vertical scanning period, the display panel 1 according to the present invention supplies the auxiliary capacitor bus lines CSL_1 to CSL_N with the rectangular auxiliary capacitor signals $\#CSL_1$ to $\#CSL_N$ each composed of a plurality of voltage levels, thereby making it possible to set up, in the single vertical scanning period, a period during which the brightness of the pixel region $P_{n,m}$ is relatively high (such a period being hereinafter referred to as "bright period") and a period during which the brightness of the pixel region $P_{n,m}$ is relatively low (such a period being hereinafter referred to as "dark period").

[0298] Further, the existence of such bright and dark periods in a single vertical scanning period can suppress blurring of images that are displayed on the display panel 1.

[0299] Further, the length of such a bright period and the length of such a dark period in a single vertical scanning period can be adjusted by changing the duty ratio of an auxiliary capacitor signal $\#CSL_n$ that is supplied by the auxiliary capacitor driver 14.

[0300] It should be noted here that in a single vertical scanning period immediately after the potential level of an auxiliary capacitor signal $\#CSL_n$ during a selection period takes on the lowest potential level among a plurality of potential levels, the duty ratio of the auxiliary capacitor signal $\#CSL_n$ means the proportion of a period during which the voltage level of the auxiliary capacitor signal $\#CSL_n$ takes on the highest voltage level among the plurality of voltage levels in the single vertical scanning period, and that in a single vertical scanning period immediately after the potential level of an auxiliary capacitor signal $\#CSL_n$ during a selection period takes on the highest potential level among a plurality of potential levels, the duty ratio of the auxiliary capacitor signal $\#CSL_n$ means the proportion of a period during which the voltage level of the auxiliary capacitor signal $\#CSL_n$ takes on the lowest voltage level among the plurality of voltage levels in the single vertical scanning period.

[0301] (c) of FIG. 14 shows a waveform of the auxiliary capacitor signal $\#CSL_n$ shown in (d) of FIG. 5, the auxiliary capacitor signal $\#CSL_n$ being set so that the duty ratio is approximately 90%.

[0302] As shown in (c) of FIG. 14, a period TD during which the voltage level of the auxiliary capacitor signal $\#CSL_n$ is relatively low occupies approximately 10% of a single vertical scanning period T_V , and a period T_B during which the voltage level of the auxiliary capacitor signal $\#CSL_n$ is relatively high occupies approximately 90% of the single vertical scanning period T_V . Further, the single vertical scanning period T_V shown in (c) of FIG. 14 is a vertical scanning period immediately after a potential of a positive polarity has been applied to the pixel electrode $PE_{n,m}$. Therefore, the duty ratio of the auxiliary capacitor signal $\#CSL_n$ is approximately 90%.

[0303] As shown in (b) of FIG. 14, the potential difference between the potential $V_{PE_{n,m}}$ of the pixel electrode $PE_{n,m}$ and

the supply potential V_{COM} during the period TD is smaller than the potential difference between the potential $V_{PE_{n,m}}$ of the pixel electrode $PE_{n,m}$ and the supply potential V_{COM} during the period T_B . Therefore, the period TD corresponds to a dark period, and the period T_B corresponds to a bright period. In other words, the supply of the auxiliary capacitor signal #CSL_n set so that the duty ratio is approximately 90% causes approximately 90% of a single vertical scanning period to be a bright period and the rest 10% to be a dark period.

[0304] (c) of FIG. 15 shows a waveform of the auxiliary capacitor signal #CSL_n shown in (d) of FIG. 5, the auxiliary capacitor signal #CSL_n being set so that the duty ratio is approximately 10%.

[0305] As shown in (c) of FIG. 15, a period TD during which the voltage level of the auxiliary capacitor signal #CSL_n is relatively low occupies approximately 90% of a single vertical scanning period T_V' , and a period T_B during which the voltage level of the auxiliary capacitor signal #CSL_n is relatively high occupies approximately 10% of the single vertical scanning period T_V' . Further, the single vertical scanning period T_V' shown in (c) of FIG. 15 is a vertical scanning period immediately after a potential of a positive polarity has been applied to the pixel electrode $PE_{n,m}$. Therefore, the duty ratio of the auxiliary capacitor signal #CSL_n is approximately 10%.

[0306] As shown in (b) of FIG. 15, the potential difference between the potential $V_{PE_{n,m}}$ of the pixel electrode $PE_{n,m}$ and the supply potential V_{COM} during the period TD is smaller than the potential difference between the potential $V_{PE_{n,m}}$ of the pixel electrode $PE_{n,m}$ and the supply potential V_{COM} during the period T_B . Therefore, the period TD corresponds to a dark period, and the period T_B corresponds to a bright period. In other words, the supply of the auxiliary capacitor signal #CSL_n set so that the duty ratio is approximately 10% causes approximately 10% of a single vertical scanning period to be a bright period and the rest 90% to be a dark period.

[0307] FIG. 16 is a graph showing a relationship between the duty ratio and brightness. In FIG. 16, the vertical axis represents the relative brightness with the lowest brightness at 0.0 and the highest brightness at 1.0, and the horizontal axis represents the duty ratio.

[0308] As shown in FIG. 16, the greater the duty ratio is, the higher the relative brightness is.

[0309] FIG. 17 is a graph of experimental data showing a relationship between the duty ratio and the visibility of moving images that are displayed on the display panel 1.

[0310] The vertical axis of FIG. 17 represents, on a scale of 1 to 5, the visibility felt by a viewer looking at a moving image being displayed on the display panel 1. The higher the visibility is, the more clearly the moving image looks to the viewer, i.e., the less blurred the moving image looks to the viewer. The horizontal axis of FIG. 17 represents the aforementioned duty ratio.

[0311] In FIG. 17, the dotted line represents the lowest evaluations among evaluations of visibility given by a plurality of viewers, respectively, the broken line representing the highest evaluations among the evaluations of visibility given by the plurality of viewers, respectively, the solid line representing the average of the evaluations of visibility given by the plurality of viewers, respectively.

[0312] As shown in FIG. 17, at a duty ratio of approximately 10% or less, all of the viewers gave the highest evaluation

of visibility. Meanwhile, at a duty ratio of approximately 90% or greater, most of the viewers cannot sense a change in visibility.

[0313] The experimental data shown in FIG. 17 shows that it is preferable that the aforementioned duty ratio be set within a range of approximately 10% to approximately 90%.

[0314] Further, the display panel 1 according to the present embodiment is preferably configured such that the source driver 12 sets the size of amplitude of the source signals #SL₁ to #SL_M in accordance with the size of amplitude of the auxiliary capacitor signals #CSL₁ to #CSL_N that are supplied by the auxiliary capacitor driver 14.

[0315] (a) of FIG. 18 is a timing chart showing a waveform of the gate signal #GL_n. (b) of FIG. 18 is a timing chart showing the common potential V_{COM} and a waveform of the potential $V_{PE_{n,m}}$ as applied to the pixel electrode $PE_{n,m}$ in a case where the amplitude of the source signal #SL_m is larger, and (c) of FIG. 18 is a timing chart showing a waveform of the auxiliary capacitor signal #CSL_n as supplied to the auxiliary capacitor bus line CSL_n in a case where the amplitude of the source signal #SL_m is larger.

[0316] Further, (d) of FIG. 18 is a timing chart showing the common potential V_{COM} and a waveform of the potential $V_{PE_{n,m}}$ as applied to the pixel electrode $PE_{n,m}$ in a case where the amplitude of the source signal #SL_m is smaller, and (e) of FIG. 18 is a timing chart showing a waveform of the auxiliary capacitor signal CSL_n as supplied to the auxiliary capacitor bus line CSL_n in a case where the amplitude of the source signal #SL_m is smaller.

[0317] The amplitude A1 shown in (b) of FIG. 18 and the amplitude A2 shown in (d) of FIG. 18 represent the amplitude of the source signal #SL_m.

[0318] As shown in (b) through (e) of FIG. 18, the auxiliary capacitor driver 14 supplies the auxiliary capacitor signal #CSL_n of smaller amplitude in a case where the amplitude of the source signal #SL_m is larger, and supplies the auxiliary capacitor signal #CSL_n of larger amplitude in a case where the amplitude of the source signal #SL_m is smaller. Thus, in a case where the auxiliary capacitor driver 14 supplies the auxiliary capacitor signal #CSL_n of smaller amplitude, the source driver 12 supplies the source signal #SL_m of larger amplitude, and in a case where the auxiliary capacitor driver 14 supplies the auxiliary capacitor signal #CSL_n of larger amplitude, the source driver 12 supplies the source signal #SL_m of smaller amplitude, whereby the average brightness of the pixel region $P_{n,m}$ during a single vertical scanning period T_V can be held substantially constant regardless of whether the auxiliary capacitor signal #CSL_n is of larger amplitude or smaller amplitude.

[0319] Further, a specific configuration, such as that described above, for supplying the auxiliary capacitor bus lines CSL₁ to CSL_N with the rectangular auxiliary capacitor signals #CSL₁ to #CSL_N each composed of a plurality of voltage levels can be realized, for example, by the auxiliary capacitor driver 14 including a plurality of power supplies for supplying the plurality of voltage levels and a selector for selecting any one of the voltage levels supplied from the plurality of power supplies.

[0320] FIG. 19 is a block diagram showing a configuration of the auxiliary capacitor driver 14 for supplying the auxiliary capacitor signals #CSL₁ to #CSL_N each composed of a four-valued voltage level.

[0321] As shown in FIG. 19, the auxiliary capacitor driver 14 includes a first power supply B1, a second power supply

B2, a third power supply **B3**, and a fourth power supply **B4**. Further, as shown in FIG. 19, the auxiliary capacitor driver **14** includes an n th selector SEL_n ($1 \leq n \leq N$) connected to the auxiliary capacitor bus line CSL_n ($1 \leq n \leq N$).

[0322] Further, as shown in FIG. 19, the n th selector SEL_n is supplied with the control signal #11c that is outputted from the control section 11.

[0323] As shown in FIG. 19, a first potential that is outputted from the first power supply **B1**, a second potential that is outputted from the second power supply **B2**, a third potential that is outputted from the third power supply **B3**, and a fourth potential that is outputted from the fourth power supply **B4** are supplied to the n th selector SEL_n ($1 \leq n \leq N$). The n th selector SEL_n selects any one of the first to fourth potentials in accordance with the control signal #11c and supplies the selected potential to the auxiliary capacitor bus line CSL_n .

[0324] Although the present invention is not to be limited by a specific configuration of the first to fourth power supplies, DACs (digital-analog converters) to which digital values respectively corresponding to the first to fourth potentials are inputted may be used, for example, or another configuration may be used.

[0325] As described above, the display panel 1 according to the present invention is preferably configured such that the auxiliary capacitor driver 14 includes amplitude changing means for changing size of amplitude of the rectangular voltage signal (auxiliary capacitor signal # CSL_n).

[0326] By the auxiliary capacitor driver 14 thus including amplitude changing means for changing size of amplitude of the rectangular voltage signal, the phenomenon of blurring of moving images can be more effectively suppressed.

[0327] Further, the display panel 1 according to the present invention is configured such that the source driver 12 supplies the source signal # SL_m of larger amplitude in a case where the amplitude of the rectangular voltage signal (auxiliary capacitor signal # CSL_n) is smaller, and supplies the source signal # SL_m of smaller amplitude in a case where the amplitude of the rectangular voltage signal (auxiliary capacitor signal # CSL_n) is larger.

[0328] The foregoing configuration allows the source driver to supply the source signal of larger amplitude in a case where the amplitude of the rectangular voltage signal is smaller, and to supply the source signal of smaller amplitude in a case where the amplitude of the rectangular voltage signal is larger, thus bringing about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images, regardless of whether the rectangular voltage signal is of larger amplitude or smaller amplitude.

[0329] It should be noted the amplitude of the source signal is defined as being obtained by subtracting the potential of the source signal at the time of negative polarity writing from the potential of the source signal at the time of positive polarity writing (same applies below). Further, the time of positive polarity writing refers to the time of supply of the conducting signal during which the rectangular voltage signal is at the lowest voltage level, and the time of negative polarity writing refers to the time of supply of the conducting signal during which the rectangular voltage signal is at the highest voltage level (same applies below).

Embodiment 2

[0330] In Embodiment 1, the display device 1 has been described as being configured to include N gate bus lines GL_1

to GL_N and N auxiliary capacitor bus lines CSL_1 to CSL_N . However, the present invention is not to be limited to this configuration.

[0331] A display panel 2 according to a second embodiment of the present invention is described below with reference to FIGS. 20 and 21. It should be noted those parts which have already been described are given the same reference signs, and as such, will not be described below.

[0332] FIG. 20 is a block diagram showing a configuration of the display panel 2 according to the present embodiment. As shown in FIG. 20, the display panel 2 includes an auxiliary capacitor driver 24, instead of the auxiliary capacitor driver 14 in the display panel 1, and a display section 26, instead of the display section 16 in the display panel 1.

[0333] As shown in FIG. 20, in addition to the N gate bus lines GL_1 to GL_N (it is assumed in the present embodiment that N is an even number) and the M source bus lines SL_1 to SL_M , the display section 26 includes $N/2$ auxiliary capacitor bus lines CSL_1 to $CSL_{N/2}$.

[0334] Further, as shown in FIG. 20, a second auxiliary capacitor electrode $CE2_{n,m}$ formed in the pixel region $P_{n,m}$ defined by a gate bus line GL_n (n is an odd number) and a second auxiliary capacitor electrode $CE2_{n+1,m}$ formed in the pixel region $P_{n+1,m}$ defined by a gate bus line GL_{n+1} are both connected to an auxiliary capacitor bus line CSL_p ($p=(n+1)/2$).

[0335] The auxiliary capacitor driver 24 supplies the $N/2$ auxiliary capacitor bus lines CSL_1 to $CSL_{N/2}$ with auxiliary capacitor signals # CSL_1 to # $CSL_{N/2}$, respectively.

[0336] Further, in the present embodiment, the source driver 12 is described as one which supplies the source bus line SL_m with a source signal that reverses its polarity every two consecutive horizontal scanning periods.

[0337] The other components of the display panel 2 are the same as those of the display panel 1.

[0338] (a) of FIG. 21 is a timing chart showing examples of waveforms of gate signals # GL_n to # GL_{n+3} that are supplied to the gate bus lines GL_n to GL_{n+3} , respectively, by the gate driver 13 in the display panel 2, and (b) of FIG. 21 is a timing chart showing examples of waveforms of auxiliary capacitor signals # CSL_p ($p=(n+1)/2$) and # CSL_{p+1} that are supplied to the auxiliary capacitor bus lines CSL_p and CSL_{p+1} , respectively, by the auxiliary capacitor driver 24 in the display panel 2.

[0339] As shown in (a) and (b) of FIG. 21, the auxiliary capacitor driver 24 supplies the auxiliary capacitor bus line CSL_p ($p=(n+1)/2$) with the auxiliary capacitor signal # CSL_p ($p=(n+1)/2$) in synchronization with the gate signals # GL_n and # GL_{n+1} , and supplies the auxiliary capacitor bus line CSL_{p+1} ($p=(n+1)/2$) with the auxiliary capacitor signal # CSL_{p+1} ($p=(n+1)/2$) in synchronization with the gate signals # GL_{n+2} and # GL_{n+3} .

[0340] Thus, the display panel 2 according to the present embodiment is configured such that: the number of the plurality of gate bus lines GL_1 to GL_N is an even number; the number of the plurality of auxiliary capacitor bus lines is a half (i.e., $N/2$) of the number of the plurality of gate bus lines; and the other end (second auxiliary capacitor electrode $CE2_{2k-1,m}$) of the capacitor $C_{2k-1,m}$ connected via the transistor $M_{2k-1,m}$ to the $(2k-1)$ th (k is a natural number) gate bus line GL_{2k-1} of the plurality of gate bus lines and the other end (second auxiliary capacitor electrode $CE2_{2k}$) of the capacitor $C_{2k,m}$ connected via the transistor $M_{2k,m}$ to the $2k$ th gate bus

line $GL_{2k,m}$ of the plurality of gate bus lines are connected to the k th auxiliary capacitor bus line CSL_k of the plurality of auxiliary capacitor bus lines.

[0341] The display panel 2 according to the present embodiment can reduce the number of auxiliary capacitor bus lines to half as compared with the display panel 1 in Embodiment 1. Therefore, the configuration of the display section 26 in the display panel 2 can be made simpler than the configuration of the display section 16 in the display panel 1. Further, since the auxiliary capacitor driver 24 in the display panel 2 needs only supply the $N/2$ auxiliary capacitor bus lines CSL_1 to $CSL_{N/2}$ with the auxiliary capacitor signals $\#CSL_1$ to $\#CSL_{N/2}$, respectively, the auxiliary capacitor driver 24 can be made simpler in configuration than the auxiliary capacitor driver 14, in the display panel 1, which supplies the N auxiliary capacitor bus lines CSL_1 to CSL_N with the auxiliary capacitor signals $\#CSL_1$ to $\#CSL_N$, respectively. That is, the display panel 2 according to the present embodiment can suppress the phenomenon of blurring of moving images with a simpler configuration than the display panel 1 in Embodiment 1.

Embodiment 3

[0342] A display panel 3 according to a third embodiment of the present invention is described below with reference to FIGS. 22 and 23.

[0343] FIG. 22 is a block diagram showing a configuration of the display panel 3 according to the present embodiment. As shown in FIG. 22, the display panel 3 includes a control section 31, a source driver 12, an auxiliary capacitor driver 141, an auxiliary capacitor driver 142, and a display section 36. Further, the display panel 3 includes a gate driver (not illustrated) and a counter electrode driver (not illustrated). It should be noted here that the gate driver (not illustrated) and the counter electrode driver (not illustrated) are identical in configuration to the gate driver 13 and the counter electrode driver 15 in the display panel 1, respectively.

[0344] As shown in FIG. 22, the display section 36 has the auxiliary capacitor drivers 141 and 142 disposed on both sides thereof, respectively. Further, the auxiliary capacitor driver 141 is supplied with a control signal $\#11c2$ from the control section 31, and the auxiliary capacitor driver 142 is supplied with a control signal $\#11c1$ from the control section 31.

[0345] The display section 36 is provided with M source bus lines SL_1 to SL_M and N gate bus lines (not illustrated). It should be noted that the N gate bus lines (not illustrated) are identical in configuration to the N gate bus lines GL_1 to GL_N in the display panel 1. Further, the display section 36 is provided with a counter electrode wire (not illustrated) identical to the counter electrode wire COM1 in the display panel 1.

[0346] Further, as shown in FIG. 22, the display section 36 has N auxiliary capacitor bus lines $CSLL_1$ to $CSLL_N$ formed on a left half surface thereof substantially perpendicularly to the source bus lines SL_1 to SL_M , and has N auxiliary capacitor bus lines $CSLR_1$ to $CSLR_N$ formed on a right half surface thereof substantially perpendicularly to the source bus lines SL_1 to SL_M . Further, the N auxiliary capacitor bus lines $CSLL_1$ to $CSLL_N$ and the N auxiliary capacitor bus lines $CSLR_1$ to $CSLR_N$ are insulated from each other. Further, as shown in FIG. 22, the auxiliary capacitor bus line $CSLL_n$ and the auxiliary capacitor bus line $CSLR_n$ are disposed collinearly. Therefore, in other words, in the present embodiment, the auxiliary capacitor bus line CSL_n in the display

panel 1 is constituted by the two auxiliary capacitor bus lines $CSLL_n$ and $CSLR_n$ formed collinearly via an insulating section.

[0347] Further, each of the N auxiliary capacitor bus lines $CSLL_1$ to $CSLL_N$ has an end connected to the auxiliary capacitor driver 141, and each of the N auxiliary capacitor bus lines $CSLR_1$ to $CSLR_N$ has an end connected to the auxiliary capacitor driver 142.

[0348] It should be noted that the auxiliary capacitor bus lines $CSLL_1$ to $CSLL_N$ and the auxiliary capacitor bus lines $CSLR_1$ to $CSLR_N$ are insulated from each other.

[0349] The auxiliary capacitor driver 141 supplies the auxiliary capacitor bus lines $CSLL_1$ to $CSLL_N$ with auxiliary capacitor signals $\#CSLL_1$ to $\#CSLL_N$, respectively, and the auxiliary capacitor driver 142 supplies the auxiliary capacitor bus lines $CSLR_1$ to $CSLR_N$ with auxiliary capacitor signals $\#CSLR_1$ to $\#CSLR_N$, respectively.

[0350] FIG. 23 is a circuit diagram showing a configuration of the display section 36 in a region R shown in FIG. 22. As shown in FIG. 23, second auxiliary capacitor electrodes $CE2_{n,1}$ to $CE2_{n,k}$ formed in the pixel regions $P_{n,1}$ to $P_{n,k}$ defined by source bus lines SL_1 to SL_k are connected to the auxiliary capacitor bus line $CSLL_n$, and second auxiliary capacitor electrodes $CE2_{n,k+1}$ to $CE2_{n,M}$ formed in the pixel regions $P_{n,k+1}$ to $P_{n,M}$ defined by source bus lines SL_{k+1} to SL_M are connected to the auxiliary capacitor bus line $CSLR_n$. The same applies to the pixel regions $P_{s,1}$ to $P_{s,k}$ ($s \neq n$, $1 \leq s \leq N$) and the pixel regions $P_{s,k+1}$ to $P_{s,M}$ ($s \neq n$, $1 \leq s \leq N$).

[0351] It should be noted here that it is preferable that the k take on a value of approximately $M/2$, where M is the number of source bus lines. Further, it is preferable that the value of k fall within a range of approximately $0.45 \times M$ to $0.55 \times M$.

[0352] The auxiliary capacitor drivers 141 and 142 may be configured to carry out the same operation as the auxiliary capacitor driver 14 described in Embodiment 1, or may be configured to supply different auxiliary capacitor signals from each other. For example, the auxiliary capacitor driver 141 may supply auxiliary capacitor signals $\#CSLL_1$ to $\#CSLL_N$ such as those of the example 2 of operation of Embodiment 1, and the auxiliary capacitor driver 142 may supply auxiliary capacitor signals $\#CSLR_1$ to $\#CSLR_N$ such as those of the example 5 of operation of Embodiment 1. Further, the auxiliary capacitor drivers 141 and 142 may be configured to output auxiliary capacitor signals $\#CSLL_1$ to $\#CSLL_N$ and auxiliary capacitor signals $\#CSLR_1$ to $\#CSLR_N$, respectively, that are different in duty ratio from each other.

[0353] Further, it is preferable that in a case where the source driver 12 supplies the source bus lines SL_1 to SL_k with source signals $\#SL_1$ to $\#SL_k$ of larger amplitude such as those shown in (b) of FIG. 18 and supplies the source bus lines SL_{k+1} to SL_M with source signals $\#SL_{k+1}$ to $\#SL_M$ of smaller amplitude such as those shown in (d) of FIG. 18, the auxiliary capacitor driver 141 supply the auxiliary capacitor bus lines $CSLL_1$ to $CSLL_N$ with auxiliary capacitor signals $\#CSLL_1$ to $\#CSLL_N$ of smaller amplitude such as those shown in (c) of FIG. 18 and the auxiliary capacitor driver 142 supply the auxiliary capacitor bus lines $CSLR_1$ to $CSLR_N$ with auxiliary capacitor signals $\#CSLR_1$ to $\#CSLR_N$ of larger amplitude such as those shown in (e) of FIG. 18.

[0354] Further, the display panel 3 according to the present embodiment is configured such that: the auxiliary capacitor driver comprises two auxiliary capacitor drivers (auxiliary capacitor drivers 141 and 142); the given auxiliary capacitor bus line (auxiliary capacitor bus line CSL_n) is constituted by

two auxiliary capacitor bus lines (auxiliary capacitor bus lines CSL_{L,n} and CSL_{R,n}) formed collinearly via an insulating section; in the single scanning period (single vertical scanning period), either one (auxiliary capacitor driver 141) of the two auxiliary capacitor drivers supplies either one (auxiliary capacitor bus line CSL_{L,n}) of the two auxiliary capacitor bus lines with the rectangular voltage signal (auxiliary capacitor signal #CSLL_n) in synchronization with the conducting signal (high-level interval of the gate signal GL_n), the rectangular voltage signal (auxiliary capacitor signal #CSLL_n) being composed of the first voltage level and the second voltage level that is different from the first voltage level; and in the single scanning period, the other one (auxiliary capacitor driver 142) of the two auxiliary capacitor drivers supplies the other one (auxiliary capacitor bus line CSL_{R,n}) of the two auxiliary capacitor bus lines with the rectangular voltage signal (auxiliary capacitor signal #CSLR_n) in synchronization with the conducting signal, the rectangular voltage signal (auxiliary capacitor signal #CSLR_n) being composed of the first voltage level and the second voltage level that is different from the first voltage level.

[0355] The display panel 3 according to the present embodiment can supply a pixel electrode connected to the one auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{L,n}) and a pixel electrode connected to the other auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{R,n}) with the rectangular voltage signals (auxiliary capacitor signals #CSLL_n and #CSLR_n) independently from each other.

[0356] Therefore, the foregoing configuration allows a pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and a pixel region including the pixel electrode connected to the other auxiliary capacitor bus line to display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be made to more effectively claim users' attention. That is, the improvement effect of the present invention on the blurring of moving images can be made more effectively appealing to users.

[0357] Further, as mentioned above, the source driver 12 may supply source signals of different amplitudes to the source bus line SL_m connected via the capacitor C_{n,m} (m ≤ k) and the transistor M_{n,m} to the one auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{L,n}) and to the source bus line SL_r connected via the capacitor C_{n,r} (r ≥ k+1) and the transistor M_{n,r} to the other auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{R,n}).

[0358] Therefore, in this example of operation, the pixel electrode PE_{n,m} (m ≤ k) connected to the one auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{L,n}) and the pixel electrode PE_{n,m} (m = k+1) connected to the other auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{R,n}) are supplied with the rectangular voltage signals (auxiliary capacitor signals #CSLL_n and #CSLR_n) independently from each other, whereby while uniforming the visibility of images except for the phenomenon of blurring of moving images, the pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and the pixel region including the pixel electrode connected to the other auxiliary capacitor bus line can display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be made to more effectively claim users' attention. That is, the improvement effect

of the present invention on the blurring of moving images can be made more effectively appealing to users.

[0359] Further, the one auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{L,n}) has a length that is substantially 45% to substantially 55% of that of the given auxiliary capacitor bus line (auxiliary capacitor bus line CSL_n in the display panel 1), and the other auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{R,n}) has a length that is substantially equal to a length obtained by subtracting the length of the one auxiliary capacitor bus line (auxiliary capacitor bus line CSL_{L,n}) from the length of the given auxiliary capacitor bus line (auxiliary capacitor bus line CSL_n in the display panel 1).

[0360] Therefore, according to the display panel 3 configured as described above, the brightness of the pixel region including the pixel electrode PE_{n,m} (n ≤ k) disposed on one half surface of the display section 36 and the brightness of the pixel region including the pixel electrode PE_{n,m} (n ≥ k+1) disposed on the other half surface can be each independently controlled in the single scanning period. Therefore, according to the foregoing configuration, the phenomenon of blurring of moving images can be more effectively suppressed.

[0361] Further, since the one auxiliary capacitor bus line and the other auxiliary capacitor bus line can be made substantially identical in load characteristic to each other, the auxiliary capacitor driver connected to the one auxiliary capacitor bus line and the auxiliary capacitor driver connected to the other auxiliary capacitor bus line can be made substantially identical in configuration to each other.

[0362] Therefore, according to the foregoing configuration, the improvement effect of the present invention on the blurring of moving images can be made effectively appealing to users by a configuration that is easy to design and fabricate.

[0363] Further, the display panel 3 according to the present embodiment is configured such that the one auxiliary capacitor driver (auxiliary capacitor driver 141) includes first amplitude changing means (configured in the same manner as that shown in FIG. 19) for changing size of amplitude of the rectangular voltage signal, and the other auxiliary capacitor driver (auxiliary capacitor driver 142) includes second amplitude changing means (configured in the same manner as that shown in FIG. 19) for changing size of amplitude of the rectangular voltage signal.

[0364] Therefore, according to the foregoing configuration, the one auxiliary capacitor driver and the other auxiliary capacitor driver supply the rectangular voltage signal of different amplitudes, whereby the pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and the pixel region including the pixel electrode connected to the other auxiliary capacitor bus line can display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be made to more effectively claim users' attention. That is, the improvement effect of the present invention on the blurring of moving images can be made more effectively appealing to users.

[0365] Further, it is preferable that in a case where the one auxiliary capacitor driver (auxiliary capacitor driver 141) supplies the one auxiliary capacitor bus line CSL_{L,n} with the rectangular voltage signal (auxiliary capacitor signal #CSLL_n) of smaller amplitude, the source driver 12 supplies the source signal #SL_m of larger amplitude to the source bus line SL_m connected via the capacitor C_{n,m} (m ≤ k) and the

transistor $M_{n,m}$ to the one auxiliary capacitor bus line $CSLL_n$, that in a case where the one auxiliary capacitor driver (auxiliary capacitor driver 141) supplies the one auxiliary capacitor bus line $CSLL_n$ with the rectangular voltage signal (auxiliary capacitor signal # $CSLL_n$) of larger amplitude, the source driver 12 supplies the source signal # SL_m of smaller amplitude to the source bus line SL_m connected via the capacitor $C_{n,m}$ and the transistor $M_{n,m}$ to the one auxiliary capacitor bus line $CSLL_n$, that in a case where the other auxiliary capacitor driver (auxiliary capacitor driver 142) supplies the other auxiliary capacitor bus line $CSLR_n$ with the rectangular voltage signal (auxiliary capacitor signal # $CSLR_n$) of smaller amplitude, the source driver 12 supplies the source signal # SL_m of larger amplitude to the source bus line SL_m connected via the capacitor $C_{n,m}$ and the transistor $M_{n,m}$ to the other auxiliary capacitor bus line, and that in a case where the other auxiliary capacitor driver (auxiliary capacitor driver 142) supplies the other auxiliary capacitor bus line $CSLR_n$ with the rectangular voltage signal (auxiliary capacitor signal # $CSLR_n$) of larger amplitude, the source driver 12 supplies the source signal # SL_m of smaller amplitude to the source bus line SL_m connected via the capacitor $C_{n,m}$ and the transistor $M_{n,m}$ to the other auxiliary capacitor bus line $CSLR_n$.

[0366] According to the foregoing configuration, the amplitude of the source signal that the source driver supplies to the source bus line connected via the capacitor and the transistor to the one auxiliary capacitor bus line is controlled in accordance with the amplitude of the rectangular voltage signal that the one auxiliary capacitor driver supplies to the one auxiliary capacitor bus line, and the amplitude of the source signal that the source driver supplies to the source bus line connected via the capacitor and the transistor to the other auxiliary capacitor bus line is controlled in accordance with the amplitude of the rectangular voltage signal that the other auxiliary capacitor driver supplies to the other auxiliary capacitor bus line, whereby while uniforming the visibility of images except for the phenomenon of blurring of moving images, the pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and the pixel region including the pixel electrode connected to the other auxiliary capacitor bus line can display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be more effectively appealing to users.

Embodiment 4

[0367] In Embodiments 1 to 3, the applications of the present invention to a line reversal driving system have mainly been described. However, the present invention is not to be limited to a line reversal driving system. In the following, the application of the present invention to a dot reversal driving system in which adjacent pixel electrodes are supplied with potentials that are opposite in polarity to each other is described with reference to FIGS. 24 and 25.

[0368] FIG. 24 is a circuit diagram showing a configuration of a display section 46 in a display panel according to the present embodiment. Another configuration of the display panel according to the present embodiment is identical to the configuration of the display panel 1 in Embodiment 1.

[0369] FIG. 25 is a diagram showing the polarities of potentials that are applied to the respective pixel electrodes of the display section 46. In the present embodiment, as shown in

FIG. 25, pixel electrodes that are adjacent to each other are supplied with potentials of opposite polarities. For such dot reversal driving, the source driver in the present embodiment needs only be configured, for example, to supply, at a given timing, such source signals # SL_1 to # SL_M that the polarity of the source signal # SL_m and the polarity of the source signal # SL_{m+1} are opposite polarities.

[0370] As shown in FIG. 24, in the display section 46, the second auxiliary capacitor electrode $CE2_{n,m}$ formed in the pixel region $P_{n,m}$ is connected to the auxiliary capacitor bus line CSL_n , and the second auxiliary capacitor electrode $CE2_{n,m+1}$ formed in the pixel region $P_{n,m+1}$ is connected to the auxiliary capacitor bus line CSL_{n-1} .

[0371] Further, the second auxiliary capacitor electrode $CE2_{n+1,m}$ formed in the pixel region $P_{n+1,m}$ is connected to the auxiliary capacitor bus line CSL_{n+1} , and the second auxiliary capacitor electrode $CE2_{n+1,m+1}$ formed in the pixel region $P_{n+1,m+1}$ is connected to the auxiliary capacitor bus line CSL_n .

[0372] Further, the auxiliary capacitor driver in the present embodiment supplies such auxiliary capacitor signals # CSL_1 to # CSL_N that the polarity of the auxiliary capacitor signal # CSL_n and the polarity of the auxiliary capacitor signal # CSL_{n+1} are opposite polarities. This can be realized, for example, by configuring the auxiliary capacitor driver in the present embodiment in the same manner as the auxiliary capacitor driver 14 in Embodiment 1.

[0373] Thus, the display panel according to the present embodiment is configured such that: in a case where the one end (first auxiliary capacitor electrode $CE1_{n,m}$) of the capacitor $C_{n,m}$ is connected to the transistor $M_{n,m}$ connected to the n th gate bus line GL_n of the plurality of gate bus lines and the m th source bus line SL_m of the plurality of source bus lines, the other end (first auxiliary capacitor electrode $CE2_{n,m}$) of the capacitor $C_{n,m}$ is connected to the n th auxiliary capacitor bus line CSL_n of the plurality of auxiliary capacitor bus lines; and in a case where the one end (first auxiliary capacitor electrode $CE1_{n,m+1}$) of the capacitor $C_{n,m+1}$ is connected to the transistor $M_{n,m+1}$ connected to the n th gate bus line GL_n of the plurality of gate bus lines and the $(m+1)$ th source bus line SL_{m+1} of the plurality of source bus lines, the other end (second auxiliary capacitor electrode $CE2_{n,m+1}$) of the capacitor $C_{n,m+1}$ is connected to the $(n-1)$ th auxiliary capacitor bus line CSL_{n-1} of the plurality of auxiliary capacitor bus lines.

[0374] According to the display panel thus configured, by carrying out dot reversal driving in which potentials that are applied to pixel electrodes that are adjacent to each other are opposite in polarity to each other, the phenomenon of blurring of moving images can be suppressed while flickers, cross-talks, etc. are being suppressed.

[0375] (Summary)

[0376] As described above, a display panel according to the present invention is a display panel including: a plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the

given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the display panel including an auxiliary capacitor driver which, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

[0377] Although, in changing from displaying one frame to displaying the next frame, a hold-type image display device such as a liquid crystal display device displays an moving object as if the moving object were staying in one position, the observer transfers his/her gaze on the screen in chase of the moving object even in a period of time during which the moving object is being displayed as if it were staying in one position; therefore, there occurs a phenomenon of blurring of moving images where the contours of the moving object appear to be blurred.

[0378] As described above, the display panel according to the present invention is a display panel including: a plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal layer; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the display panel including an auxiliary capacitor driver which, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level. Therefore, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the

conducting signal to a point in time where the gate driver supplies the conducting signal next, a first voltage level and a second voltage level that is different from the first voltage level can be applied to the pixel electrode connected via the transistor to the given gate bus line.

[0379] Further, in the display panel according to the present invention, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level are each longer than a response time of the liquid crystal. The response time of the liquid crystal here means the amount of time required for the orientation of the liquid crystal to start to change after application of an electric field to the liquid crystal. Generally, the amount of time required is 1 ms or more.

[0380] Therefore, the foregoing configuration can cause the brightness of an image in the pixel region in which the pixel electrode has been formed to switch between two values in the single scanning period.

[0381] This brings about an effect of making it possible to suppress the phenomenon of blurring of moving images.

[0382] Further, the auxiliary capacitor driver of the display panel according to the present invention can supply, in synchronization with the conducting signal, the rectangular voltage signal composed of the first voltage level and the second voltage level. Therefore, the voltage level of the rectangular voltage signal changes after a certain period of time has elapsed since the conducting signal was supplied.

[0383] Therefore, unlike in a case where a voltage signal is supplied out of synchronization with the conducting signal, the switching between bright and dark can be carried out in every pixel region on the screen after a certain period of time has elapsed since an update of image data.

[0384] Further, in the display panel according to the present invention, the blurring of moving images can be suppressed without using a frame memory in which to temporarily store image signals. Therefore, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, the display panel according to the present invention brings about an effect of making it possible to reduce manufacturing cost. Further, as compared with a conventional configuration that uses a frame memory in which to temporarily store image signals, the display panel according to the present invention brings about an effect of making it possible to reduce power consumption.

[0385] Further, the display panel according to the present invention is preferably configured such that the rectangular voltage signal takes on either one of the first and second voltage levels in an at least 10% continuous period of time of the single scanning period.

[0386] According to the foregoing configuration, the rectangular voltage signal takes on either one of the first and second voltage levels in an at least 10% continuous period of time of the single scanning period. This brings about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images.

[0387] Further, the display panel according to the present invention is preferably configured such that the rectangular voltage signal takes on either one of the first and second voltage levels in a period of time from a point in time at which the single scanning period starts to a point in time where substantially 10% of the single scanning period elapses, and takes on the other one of the first and second voltage levels in a period of time from a point in time where substantially 90%

of the single scanning period elapses to a point in time at which the single scanning period ends.

[0388] Generally, in the case of switching between a display at a high brightness and a display at a low brightness, the viewer feels no improvement in blurring of moving images when the percentage of the display at the high brightness is 90% or higher, feels more improvement in blurring of moving images at a lower percentage between 90% to 10%, and feels satisfactory improvement in blurring of moving images at a percentage of approximately 10%.

[0389] Therefore, the foregoing configuration brings about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images.

[0390] Further, the display panel according to the present invention is preferably configured such that in the single scanning period, a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode when the rectangular voltage signal is at the first voltage level and a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and the potential of the counter electrode when the rectangular voltage signal is at the second voltage level are polarities that are different from each other.

[0391] According to the foregoing configuration, regardless of whether the rectangular voltage signal is at the first or second voltage level, the absolute value of the voltage that is applied to the liquid crystal can be made sufficiently small.

[0392] Therefore, the foregoing configuration brings about a further effect of making it possible, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, to carry out a black display at a sufficiently low brightness, regardless of whether the rectangular voltage signal is at the first or second voltage level.

[0393] Further, the display panel according to the present invention is preferably configured such that an absolute value of a potential difference between the first voltage level and the second voltage level is twice or less as great as a threshold voltage of the liquid crystal.

[0394] Generally, the orientation of a liquid crystal is not affected even when a voltage that is lower than the threshold value is applied to the liquid crystal. In other words, the threshold voltage means a voltage at which the orientation of a liquid crystal starts to be affected (same applies below).

[0395] According to the foregoing configuration, the absolute value of the potential difference between the first voltage level and the second voltage level is twice or less as great as the threshold voltage of the liquid crystal. This makes it possible to prevent the orientation of the liquid crystal from being affected, regardless of whether the rectangular voltage signal is at the first or second voltage level.

[0396] Therefore, the foregoing configuration brings about a further effect of making it possible, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, to carry out a black display regardless of whether the rectangular voltage signal is at the first or second voltage level.

[0397] Further, the display panel according to the present invention is preferably configured such that in the single scanning period, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the

rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels.

[0398] According to the foregoing configuration, in the single scanning period, the auxiliary capacitor driver can supply the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels. Therefore, in the single scanning period, the level of voltage that is applied to the given auxiliary capacitor bus line switches among three values. In other words, in the single scanning period, the level of voltage that is applied to the auxiliary capacitor bus line makes two transitions. The first transition between the voltage levels in the single scanning period causes a voltage that is applied to the liquid crystal after the first transitions between the voltage levels to be suitable for a display after the first transition between the voltage levels, and the second transition between the voltage levels allows switching between a high brightness and a low brightness.

[0399] That is, the foregoing configuration brings about a further effect of making a display at a higher brightness possible while effectively suppressing the phenomenon of blurring of moving images.

[0400] Further, the display panel according to the present invention is preferably configured such that the rectangular voltage signal takes on any one of the first to third voltage levels in an at least 10% period of time of the single scanning period.

[0401] According to the foregoing configuration, the rectangular voltage signal takes on any one of the first to third voltage levels in an at least 10% period of time of the single scanning period. This brings about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images.

[0402] Further, the display panel according to the present invention is preferably configured such that the rectangular voltage signal takes on any one of the first to third voltage levels in a period of time from a point in time at which the single scanning period starts to a point in time where substantially 10% of the single scanning period elapses, and takes on another one of the first to third voltage levels in a period of time from a point in time where substantially 90% of the single scanning period elapses to a point in time at which the single scanning period ends.

[0403] Generally, in the case of switching between a display at a high brightness and a display at a low brightness, the viewer feels no improvement in blurring of moving images when the percentage of the display at the high brightness is 90% or higher, feels more improvement in blurring of moving images at a lower percentage between 90% to 10%, and feels satisfactory improvement in blurring of moving images at a percentage of approximately 10%.

[0404] Therefore, the foregoing configuration brings about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images.

[0405] Further, the display panel according to the present invention is preferably configured such that in the single scanning period, a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode after a first transition between the voltage levels and a

polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and the potential of the counter electrode after a next transition between the voltage levels are polarities that are different from each other.

[0406] According to the foregoing configuration, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period, the absolute value of the voltage that is applied to the liquid crystal can be made sufficiently small.

[0407] Therefore, the foregoing configuration brings about a further effect of making it possible, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, to carry out a black display at a sufficiently low brightness, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period.

[0408] Further, the display panel according to the present invention is preferably configured such that an absolute value of a potential difference between the highest voltage level among the first to third voltage levels and the middle voltage level among the first to third voltage levels is twice or less as great as a threshold voltage of the liquid crystal.

[0409] According to the foregoing configuration, the absolute value of the potential difference between the highest voltage level among the first to third voltage levels and the middle voltage level among the first to third voltage levels is twice or less as great as the threshold voltage of the liquid crystal. This makes it possible to prevent the orientation of the liquid crystal from being affected, regardless of which of the first to third voltage levels the rectangular voltage signal takes on.

[0410] Therefore, the foregoing configuration brings about a further effect of making it possible, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, to carry out a black display regardless of which of the first to third voltage levels the rectangular voltage signal takes on.

[0411] Further, the display panel according to the present invention is preferably configured such that in the single scanning period, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels, and in a single scanning period subsequent to the single scanning period, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of any two of the first to third voltage levels and a fourth voltage level that is different from the first to third voltage levels.

[0412] According to the foregoing configuration, in the single scanning period, the auxiliary capacitor driver can supply the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels. Therefore, in the single scanning period, the level of voltage

that is applied to the given auxiliary capacitor bus line switches among three values. In other words, in the single scanning period, the level of voltage that is applied to the auxiliary capacitor bus line makes two transitions. The first transition between the voltage levels in the single scanning period causes a voltage that is applied to the liquid crystal after the first transitions between the voltage levels to be suitable for a display after the first transition between the voltage levels, and the second transition between the voltage levels allows switching between a high brightness and a low brightness.

[0413] Therefore, the foregoing configuration brings about a further effect of making a display at a higher brightness possible while effectively suppressing the phenomenon of blurring of moving images.

[0414] Furthermore, the foregoing configuration makes it possible, in a single scanning period subsequent to the single scanning period, to supply a rectangular voltage signal composed of any two of the first to third voltage levels and a fourth voltage level that is different from the first to third voltage levels. Therefore, as compared with a case where a rectangular voltage signal composed of the first to third voltage levels is supplied in a single scanning period subsequent to the single scanning period, the adjustment of brightness levels between a high brightness and a low brightness can be more flexibly carried out.

[0415] Therefore, the foregoing configuration brings about a further effect of making a display at a high brightness possible while further effectively suppressing the phenomenon of blurring of moving images.

[0416] Further, the display panel according to the present invention is preferably configured such that an absolute value of a potential difference between the voltage level before a first transition between the voltage levels in the single scanning period and the voltage level after the first transition is smaller than an absolute value of a potential difference between the voltage level before a next transition between the voltage levels in the single scanning period and the voltage level after the next transition.

[0417] According to the foregoing configuration, the absolute value of the potential difference between the voltage level before the first transition between the voltage levels in the single scanning period and the voltage level after the first transition is smaller than the absolute value of the potential difference between the voltage level before the next transition between the voltage levels in the single scanning period and the voltage level after the next transition. Therefore, the difference between the brightness before the next transition and the brightness after the next transition can be made greater than the difference between the brightness before the first transition and the brightness after the first transition. Therefore, the foregoing configuration brings about a further effect of making it possible to more effectively suppress the phenomenon of blurring of moving images.

[0418] Further, the display panel according to the present invention is preferably configured such that the rectangular voltage signal takes on any one of the first to fourth voltage levels in an at least 10% period of time of the single scanning period.

[0419] According to the foregoing configuration, the rectangular voltage signal takes on any one of the first to fourth voltage levels in an at least 10% period of time of the single

scanning period. This brings about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images.

[0420] Further, the display panel according to the present invention is preferably configured such that the rectangular voltage signal takes on any one of the first to fourth voltage levels in a period of time from a point in time at which the single scanning period starts to a point in time where substantially 10% of the single scanning period elapses, and takes on another one of the first to fourth voltage levels in a period of time from a point in time where substantially 90% of the single scanning period elapses to a point in time at which the single scanning period ends.

[0421] Generally, in the case of switching between a display at a high brightness and a display at a low brightness, the viewer feels no improvement in blurring of moving images when the percentage of the display at the high brightness is 90% or higher, feels more improvement in blurring of moving images at a lower percentage between 90% to 10%, and feels satisfactory improvement in blurring of moving images at a percentage of approximately 10%.

[0422] Therefore, the foregoing configuration brings about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images.

[0423] Further, the display panel according to the present invention is preferably configured such that in the single scanning period, a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode after a first transition between the voltage levels and a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and the potential of the counter electrode after a next transition between the voltage levels are polarities that are different from each other.

[0424] According to the foregoing configuration, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period, the absolute value of the voltage that is applied to the liquid crystal can be made sufficiently small.

[0425] Therefore, the foregoing configuration brings about a further effect of making it possible, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, to carry out a black display at a sufficiently low brightness, regardless of whether after the first transition between the voltage levels or after the next transition between the voltage levels in the single scanning period.

[0426] Further, the display panel according to the present invention is preferably configured such that an absolute value of a potential difference between the second lowest voltage level among the first to fourth voltage levels and the highest voltage level among the first to fourth voltage levels is twice or less as great as a threshold voltage of the liquid crystal.

[0427] According to the foregoing configuration, the absolute value of the potential difference between the second lowest voltage level among the first to fourth voltage levels and the highest voltage level among the first to fourth voltage levels is twice or less as great as the threshold voltage of the liquid crystal. This makes it possible to prevent the orientation of the liquid crystal from being affected, regardless of which of the first to fourth voltage levels the rectangular voltage signal takes on.

[0428] Therefore, the foregoing configuration brings about a further effect of making it possible, in a normally black type in which the brightness is lower in a case where the absolute value of a voltage that is applied to the liquid crystal is smaller, to carry out a black display regardless of which of the first to fourth voltage levels the rectangular voltage signal takes on.

[0429] Further, the display panel according to the present invention is preferably configured such that in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the lowest voltage level among the voltage levels, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with the rectangular voltage signal in the single scanning period, the rectangular voltage signal having its voltage levels arranged in an ascending order.

[0430] Generally, in a normally black type in which a black display is carried out in a case where no voltage is applied to the pixel electrode, a phenomenon of insufficient rising from a low brightness to a high brightness occurs due to finite lengths of time of response of the liquid crystal. In other words, there is such a characteristic that the amount of time required to change from a low brightness to a high brightness is larger than the amount of time required to change from a high brightness to a low brightness. In a case where a signal that is applied to the pixel electrode has a positive polarity, such a phenomenon can occur at a timing when the potential of the pixel electrode changes to a high voltage.

[0431] According to the foregoing configuration, in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the lowest voltage level among the voltage levels, the pixel electrode can be supplied with a voltage signal at a lower voltage level and then with a voltage signal at a higher voltage level in the single scanning period.

[0432] This allows the potential that is applied to the pixel electrode to gradually change to a high voltage. This brings about a further effect of making it possible to suppress the phenomenon of insufficient rising from a low brightness to a high brightness that can occur in a normally black type.

[0433] Further, the display panel according to the present invention is preferably configured such that in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the highest voltage level among the voltage levels, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with the rectangular voltage signal in the single scanning period, the rectangular voltage signal having its voltage levels arranged in a descending order.

[0434] Generally, in a normally black type in which a black display is carried out in a case where no voltage is applied to the pixel electrode, a phenomenon of insufficient rising from a low brightness to a high brightness occurs due to finite lengths of time of response of the liquid crystal. In other words, there is such a characteristic that the amount of time required to change from a low brightness to a high brightness is larger than the amount of time required to change from a high brightness to a low brightness. In a case where a signal that is applied to the pixel electrode has a positive polarity, such a phenomenon can occur at a timing when the potential of the pixel electrode changes to a low voltage.

[0435] According to the foregoing configuration, in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus

line is supplied with the highest voltage level among the voltage levels, the pixel electrode can be supplied with a voltage signal at a higher voltage and then with a voltage signal at a lower voltage level in the single scanning period.

[0436] This allows the potential that is applied to the pixel electrode to gradually change to a low voltage. This brings about a further effect of making it possible to suppress the phenomenon of insufficient rising from a low brightness to a high brightness that can occur in a normally black type.

[0437] Further, the display panel according to the present invention is preferably configured such that the auxiliary capacitor driver synchronously supplies the rectangular voltage signal to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the n th gate bus line of the plurality of gate bus lines and to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the $(n+1)$ th gate bus line of the plurality of gate bus lines.

[0438] The foregoing configuration makes it possible to synchronously supply the rectangular voltage signal to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the n th gate bus line of the plurality of gate bus lines and to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the $(n+1)$ th gate bus line of the plurality of gate bus lines. Therefore the auxiliary capacitor driver of a simpler configuration brings about a further effect of making it possible to suppress the phenomenon of blurring of moving images.

[0439] Further, the display panel according to the present invention is preferably configured such that the auxiliary capacitor driver synchronously supplies the rectangular voltage signal to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the n th gate bus line of the plurality of gate bus lines and to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the $(n+2)$ th gate bus line of the plurality of gate bus lines.

[0440] The foregoing configuration allows the auxiliary capacitor driver to synchronously supply the rectangular voltage signal to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the n th gate bus line of the plurality of gate bus lines and to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the $(n+2)$ th gate bus line of the plurality of gate bus lines. Therefore, the auxiliary capacitor driver of a simpler configuration brings about a further effect of making it possible to suppress the phenomenon of blurring of moving images while suppressing the occurrence of flickers and streaks corresponding to polarity reversal.

[0441] Further, the display panel according to the present invention is preferably configured such that: the number of the plurality of gate bus lines is an even number; the number of the plurality of auxiliary capacitor bus lines is a half of the number of the plurality of gate bus lines; and the other end of the capacitor connected via the transistor to the $(2k-1)$ th (k is a natural number) gate bus line of the plurality of gate bus lines and the other end of the capacitor connected via the transistor to the $2k$ th gate bus line of the plurality of gate bus lines are connected to the k th auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines.

[0442] According to the foregoing configuration, the number of auxiliary capacitor bus lines to be formed on the display panel can be reduced to half of the number of the plurality of

gate bus lines. Therefore, the display panel of a simpler configuration brings about a further effect of making it possible to suppress the phenomenon of blurring of moving images.

[0443] Further, the display panel according to the present invention is preferably configured such that the auxiliary capacitor driver includes amplitude changing means for changing size of amplitude of the rectangular voltage signal.

[0444] According to the foregoing configuration, the auxiliary capacitor driver includes amplitude changing means for changing size of amplitude of the rectangular voltage signal. This brings about a further effect of making it possible to more effectively suppress the phenomenon of blurring of moving images.

[0445] Further, the display panel according to the present invention is preferably configured such that the source driver supplies the source signal of larger amplitude in a case where the amplitude of the rectangular voltage signal is smaller, and supplies the source signal of smaller amplitude in a case where the amplitude of the rectangular voltage signal is larger.

[0446] The foregoing configuration allows the source driver to supply the source signal of larger amplitude in a case where the amplitude of the rectangular voltage signal is smaller, and to supply the source signal of smaller amplitude in a case where the amplitude of the rectangular voltage signal is larger, thus bringing about a further effect of making it possible to effectively suppress the phenomenon of blurring of moving images, regardless of whether the rectangular voltage signal is of larger amplitude or smaller amplitude.

[0447] It should be noted the amplitude of the source signal is defined as being obtained by subtracting the voltage level of the source signal at the time of negative polarity writing from the voltage level of the source signal at the time of positive polarity writing (same applies below). Further, the time of positive polarity writing refers to the time of supply of the conducting signal during which the rectangular voltage signal is at the lowest voltage level, and the time of negative polarity writing refers to the time of supply of the conducting signal during which the rectangular voltage signal is at the highest voltage level (same applies below).

[0448] Further, the display panel according to the present invention may be configured such that: the auxiliary capacitor driver comprises two auxiliary capacitor drivers; the given auxiliary capacitor bus line is constituted by two auxiliary capacitor bus lines formed collinearly via an insulating section; in the single scanning period, either one of the two auxiliary capacitor drivers supplies either one of the two auxiliary capacitor bus lines with the rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level and the second voltage level that is different from the first voltage level; and in the single scanning period, the other one of the two auxiliary capacitor drivers supplies the other one of the two auxiliary capacitor bus lines with the rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level and the second voltage level that is different from the first voltage level.

[0449] According to the foregoing configuration, the one auxiliary capacitor driver supplies the rectangular voltage signal to either one of the two auxiliary capacitor bus lines formed collinearly via the insulating section, and the other auxiliary capacitor driver supplies the rectangular voltage signal to the other auxiliary capacitor bus line.

[0450] Therefore, according to the foregoing configuration, the pixel electrode connected to the one auxiliary capacitor bus line and the pixel electrode connected to the other auxiliary capacitor bus line can be supplied with the rectangular voltage signal independently from each other.

[0451] Therefore, the foregoing configuration allows a pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and a pixel region including the pixel electrode connected to the other auxiliary capacitor bus line to display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be made to more effectively claim users' attention. That is, such a further effect can be brought about that the improvement effect of the present invention on the blurring of moving images can be made more effectively appealing to users.

[0452] Further, the display panel according to the present invention is preferably configured such that the source driver supplies source signals of different amplitudes to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line and to that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line.

[0453] According to the foregoing configuration, the source driver can supply source signals of different amplitudes to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line and to that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line. Therefore, the pixel electrode connected to the one auxiliary capacitor bus line and the pixel electrode connected to the other auxiliary capacitor bus line can be supplied with the rectangular voltage signal independently from each other, whereby while uniforming the visibility of images except for the phenomenon of blurring of moving images, the pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and the pixel region including the pixel electrode connected to the other auxiliary capacitor bus line can display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be made to more effectively claim users' attention. That is, such a further effect can be brought about that the improvement effect of the present invention on the blurring of moving images can be made more effectively appealing to users.

[0454] Further, the display panel according to the present invention is preferably configured such that the one auxiliary capacitor bus line has a length that is substantially 45% to substantially 55% of that of the given auxiliary capacitor bus line, and the other auxiliary capacitor bus line has a length that is substantially equal to a length obtained by subtracting the length of the one auxiliary capacitor bus line from the length of the given auxiliary capacitor bus line.

[0455] According to the foregoing configuration, the given auxiliary capacitor bus line is electrically separated into the one auxiliary capacitor bus line and the other auxiliary capacitor bus line within a range of $\pm 5\%$ from the center line dividing the display section, which displays an image in the display panel, into two equal parts in parallel with the source bus lines.

[0456] Therefore, according to the foregoing configuration, the brightness of the pixel region including the pixel

electrode disposed on one half surface of the display section and the brightness of the pixel region including the pixel electrode disposed on the other half surface can be each independently controlled in the single scanning period. Further, since the one auxiliary capacitor bus line and the other auxiliary capacitor bus line can be made substantially identical in load characteristic to each other, the auxiliary capacitor driver connected to the one auxiliary capacitor bus line and the auxiliary capacitor driver connected to the other auxiliary capacitor bus line can be made substantially identical in configuration to each other.

[0457] Therefore, the foregoing configuration brings about such a further effect that the improvement effect of the present invention on the blurring of moving images can be made effectively appealing to users by a configuration that is easy to design and fabricate.

[0458] Further, the display panel according to the present invention is preferably configured such that the one auxiliary capacitor driver includes first amplitude changing means for changing size of amplitude of the rectangular voltage signal, and the other auxiliary capacitor driver includes second amplitude changing means for changing size of amplitude of the rectangular voltage signal.

[0459] According to the foregoing configuration, the one auxiliary capacitor driver includes first amplitude changing means for changing size of amplitude of the rectangular voltage signal, and the other auxiliary capacitor driver includes second amplitude changing means for changing size of amplitude of the rectangular voltage signal. Therefore, the one auxiliary capacitor driver and the other auxiliary capacitor driver can supply the rectangular voltage signal of different amplitudes.

[0460] Therefore, according to the foregoing configuration, the one auxiliary capacitor driver and the other auxiliary capacitor driver supply the rectangular voltage signal of different amplitudes, whereby the pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and the pixel region including the pixel electrode connected to the other auxiliary capacitor bus line can display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, the improvement effect of the present invention on the blurring of moving images can be made to more effectively claim users' attention. That is, such a further effect can be brought about that the improvement effect of the present invention on the blurring of moving images can be made more effectively appealing to users.

[0461] Further, the display panel according to the present invention is preferably configured such that: in a case where the one auxiliary capacitor driver supplies the one auxiliary capacitor bus line with the rectangular voltage signal of smaller amplitude, the source driver supplies the source signal of larger amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line; in a case where the one auxiliary capacitor driver supplies the one auxiliary capacitor bus line with the rectangular voltage signal of larger amplitude, the source driver supplies the source signal of smaller amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line; in a case where the other auxiliary capacitor driver supplies the other auxiliary capacitor bus line with the rectangular voltage signal of smaller amplitude, the source driver supplies the source signal of larger amplitude to

that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line; and in a case where the other auxiliary capacitor driver supplies the other auxiliary capacitor bus line with the rectangular voltage signal of larger amplitude, the source driver supplies the source signal of smaller amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line.

[0462] According to the foregoing configuration, the amplitude of the source signal that the source driver supplies to the source bus line connected via the capacitor and the transistor to the one auxiliary capacitor bus line is controlled in accordance with the amplitude of the rectangular voltage signal that the one auxiliary capacitor driver supplies to the one auxiliary capacitor bus line, and the amplitude of the source signal that the source driver supplies to the source bus line connected via the capacitor and the transistor to the other auxiliary capacitor bus line is controlled in accordance with the amplitude of the rectangular voltage signal that the other auxiliary capacitor driver supplies to the other auxiliary capacitor bus line, whereby while uniforming the visibility of images except for the phenomenon of blurring of moving images, the pixel region including the pixel electrode connected to the one auxiliary capacitor bus line and the pixel region including the pixel electrode connected to the other auxiliary capacitor bus line can display images that are different in improvement effect on the phenomenon of blurring of moving images. Therefore, such a further effect can be brought about that the improvement effect of the present invention on the blurring of moving images can be more effectively appealing to users.

[0463] Further, the display panel according to the present invention is preferably configured such that: in a case where the one end of the capacitor is connected to the transistor connected to the n th gate bus line of the plurality of gate bus lines and the m th source bus line of the plurality of source bus lines, the other end of the capacitor is connected to the n th auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; and in a case where the one end of the capacitor is connected to the transistor connected to the n th gate bus line of the plurality of gate bus lines and the $(m+1)$ th source bus line of the plurality of source bus lines, the other end of the capacitor is connected to the $(n-1)$ th auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines.

[0464] The display panel thus configured brings about such a further effect that by carrying out dot reversal driving in which source signals that are applied to pixel electrodes that are adjacent to each other are opposite in polarity to each other, the phenomenon of blurring of moving images can be suppressed while flickers, cross-talks, etc. are being suppressed.

[0465] Further, a liquid crystal display device including a display panel thus configured is also encompassed in the scope of the present invention.

[0466] Further, a driving method according to the present invention is a method for driving a display panel including: a plurality of gate bus lines; a plurality of source bus lines; a plurality of auxiliary capacitor bus lines; a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus

line of the plurality of source bus lines; a pixel electrode connected to a drain of the transistor; a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal; a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting; a counter electrode opposed to the pixel electrode via a liquid crystal; a counter electrode wire connected to the counter electrode; and a counter electrode driver, which supplies the counter electrode wire with a common potential, the method including a voltage signal supplying step of, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplying the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level, in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

[0467] The foregoing method brings about the same effects as the foregoing display panel according to the present invention.

[0468] The present invention is not limited to the description of the embodiments above, but may be altered by a skilled person within the scope of the claims. An embodiment based on a proper combination of technical means disclosed in different embodiments is encompassed in the technical scope of the present invention.

[0469] Further, a liquid crystal display device including a display panel described in any one of the embodiments is also encompassed in the present invention.

INDUSTRIAL APPLICABILITY

[0470] The present invention can be suitably applied to a display panel that displays an image by using liquid crystals.

REFERENCE SIGNS LIST

- [0471] 1 Display panel
- [0472] 11 Control section
- [0473] 12 Source driver
- [0474] 13 Gate driver
- [0475] 14 Auxiliary capacitor driver
- [0476] 15 Counter electrode driver
- [0477] 16 Display section
- [0478] SL_m Source bus line
- [0479] GL_n Gate bus line
- [0480] CSL_n Auxiliary capacitor bus line
- [0481] $COML$ Counter electrode wire
- [0482] $P_{n,m}$ Pixel region
- [0483] $PE_{n,m}$ Pixel electrode
- [0484] $M_{n,m}$ Transistor
- [0485] E_{COM} Counter electrode
- [0486] $C_{n,m}$ Capacitor

[0487] CE1_{n,m} First auxiliary capacitor electrode

[0488] CE2_{n,m} Second auxiliary capacitor electrode

1. A display panel including:

a plurality of gate bus lines;

a plurality of source bus lines;

a plurality of auxiliary capacitor bus lines;

a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines;

a pixel electrode connected to a drain of the transistor;

a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines;

a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal;

a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting;

a counter electrode opposed to the pixel electrode via a liquid crystal;

a counter electrode wire connected to the counter electrode; and

a counter electrode driver, which supplies the counter electrode wire with a common potential,

the display panel comprising an auxiliary capacitor driver which, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level,

in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

2. The display panel as set forth in claim 1, wherein the rectangular voltage signal takes on either one of the first and second voltage levels in an at least 10% continuous period of time of the single scanning period.

3. The display panel as set forth in claim 1, wherein the rectangular voltage signal takes on either one of the first and second voltage levels in a period of time from a point in time at which the single scanning period starts to a point in time where substantially 10% of the single scanning period elapses, and takes on the other one of the first and second voltage levels in a period of time from a point in time where substantially 90% of the single scanning period elapses to a point in time at which the single scanning period ends.

4. The display panel as set forth in claim 1, wherein in the single scanning period, a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode when the rectangular voltage signal is at the first voltage level and a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a poten-

tial of the pixel electrode and the potential of the counter electrode when the rectangular voltage signal is at the second voltage level are polarities that are different from each other.

5. The display panel as set forth in claim 1, wherein an absolute value of a potential difference between the first voltage level and the second voltage level is twice or less as great as a threshold voltage of the liquid crystal.

6. The display panel as set forth in claim 1, wherein in the single scanning period, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels.

7. The display panel as set forth in claim 6, wherein the rectangular voltage signal takes on any one of the first to third voltage levels in an at least 10% period of time of the single scanning period.

8. The display panel as set forth in claim 6, wherein the rectangular voltage signal takes on any one of the first to third voltage levels in a period of time from a point in time at which the single scanning period starts to a point in time where substantially 10% of the single scanning period elapses, and takes on another one of the first to third voltage levels in a period of time from a point in time where substantially 90% of the single scanning period elapses to a point in time at which the single scanning period ends.

9. The display panel as set forth in claim 6, wherein in the single scanning period, a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode after a first transition between the voltage levels and a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and the potential of the counter electrode after a next transition between the voltage levels are polarities that are different from each other.

10. The display panel as set forth in claim 6, wherein an absolute value of a potential difference between the highest voltage level among the first to third voltage levels and the middle voltage level among the first to third voltage levels is twice or less as great as a threshold voltage of the liquid crystal.

11. The display panel as set forth in claim 1, wherein in the single scanning period, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level, the second voltage level, and a third voltage level that is different from the first and second voltage levels, and in a single scanning period subsequent to the single scanning period, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of any two of the first to third voltage levels and a fourth voltage level that is different from the first to third voltage levels.

12. The display panel as set forth in claim 11, wherein an absolute value of a potential difference between the voltage level before a first transition between the voltage levels in the single scanning period and the voltage level after the first transition is smaller than an absolute value of a potential difference between the voltage level before a next transition

between the voltage levels in the single scanning period and the voltage level after the next transition.

13. The display panel as set forth in claim **11**, wherein the rectangular voltage signal takes on any one of the first to fourth voltage levels in an at least 10% period of time of the single scanning period.

14. The display panel as set forth in claim **11**, wherein the rectangular voltage signal takes on any one of the first to fourth voltage levels in a period of time from a point in time at which the single scanning period starts to a point in time where substantially 10% of the single scanning period elapses, and takes on another one of the first to fourth voltage levels in a period of time from a point in time where substantially 90% of the single scanning period elapses to a point in time at which the single scanning period ends.

15. The display panel as set forth in claim **11**, wherein in the single scanning period, a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and a potential of the counter electrode after a first transition between the voltage levels and a polarity of a voltage that is applied to the liquid crystal as represented by a difference between a potential of the pixel electrode and the potential of the counter electrode after a next transition between the voltage levels are polarities that are different from each other.

16. The display panel as set forth in claim **11**, wherein an absolute value of a potential difference between the second lowest voltage level among the first to fourth voltage levels and the highest voltage level among the first to fourth voltage levels is twice or less as great as a threshold voltage of the liquid crystal.

17. The display panel as set forth in claim **1**, wherein in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the lowest voltage level among the voltage levels, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with the rectangular voltage signal in the single scanning period, the rectangular voltage signal having its voltage levels arranged in an ascending order.

18. The display panel as set forth in claim **1**, wherein in a case where when the gate driver supplies the given gate bus line with the conducting signal, the given auxiliary capacitor bus line is supplied with the highest voltage level among the voltage levels, the auxiliary capacitor driver supplies the given auxiliary capacitor bus line with the rectangular voltage signal in the single scanning period, the rectangular voltage signal having its voltage levels arranged in a descending order.

19. The display panel as set forth in claim **1**, wherein the auxiliary capacitor driver synchronously supplies the rectangular voltage signal to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the n th gate bus line of the plurality of gate bus lines and to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the $(n+1)$ th gate bus line of the plurality of gate bus lines.

20. The display panel as set forth in claim **1**, wherein the auxiliary capacitor driver synchronously supplies the rectangular voltage signal to that one of the auxiliary capacitor bus lines which is connected via the transistor and the capacitor to the n th gate bus line of the plurality of gate bus lines and to that one of the auxiliary capacitor bus lines which is con-

nected via the transistor and the capacitor to the $(n+2)$ th gate bus line of the plurality of gate bus lines.

21. The display panel as set forth in claim **1**, wherein: the number of the plurality of gate bus lines is an even number;

the number of the plurality of auxiliary capacitor bus lines is a half of the number of the plurality of gate bus lines; and

the other end of the capacitor connected via the transistor to the $(2k-1)$ th (k is a natural number) gate bus line of the plurality of gate bus lines and the other end of the capacitor connected via the transistor to the $2k$ th gate bus line of the plurality of gate bus lines are connected to the k th auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines.

22. The display panel as set forth in claim **1**, wherein the auxiliary capacitor driver includes amplitude changing means for changing size of amplitude of the rectangular voltage signal.

23. The display panel as set forth in claim **22**, wherein the source driver supplies the source signal of larger amplitude in a case where the amplitude of the rectangular voltage signal is smaller, and supplies the source signal of smaller amplitude in a case where the amplitude of the rectangular voltage signal is larger.

24. The display panel as set forth in claim **1**, wherein: the auxiliary capacitor driver comprises two auxiliary capacitor drivers;

the given auxiliary capacitor bus line is constituted by two auxiliary capacitor bus lines formed collinearly via an insulating section;

in the single scanning period, either one of the two auxiliary capacitor drivers supplies either one of the two auxiliary capacitor bus lines with the rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level and the second voltage level that is different from the first voltage level; and

in the single scanning period, the other one of the two auxiliary capacitor drivers supplies the other one of the two auxiliary capacitor bus lines with the rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of the first voltage level and the second voltage level that is different from the first voltage level.

25. The display panel as set forth in claim **24**, wherein the source driver supplies source signals of different amplitudes to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line and to that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line.

26. The display panel as set forth in claim **24**, wherein the one auxiliary capacitor bus line has a length that is substantially 45% to substantially 55% of that of the given auxiliary capacitor bus line, and the other auxiliary capacitor bus line has a length that is substantially equal to a length obtained by subtracting the length of the one auxiliary capacitor bus line from the length of the given auxiliary capacitor bus line.

27. The display panel as set forth in claim **24**, wherein the one auxiliary capacitor driver includes first amplitude changing means for changing size of amplitude of the rectangular voltage signal, and the other auxiliary capacitor driver

includes second amplitude changing means for changing size of amplitude of the rectangular voltage signal.

28. The display panel as set forth in claim **27**, wherein:

in a case where the one auxiliary capacitor driver supplies the one auxiliary capacitor bus line with the rectangular voltage signal of smaller amplitude, the source driver supplies the source signal of larger amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line;

in a case where the one auxiliary capacitor driver supplies the one auxiliary capacitor bus line with the rectangular voltage signal of larger amplitude, the source driver supplies the source signal of smaller amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the one auxiliary capacitor bus line,

in a case where the other auxiliary capacitor driver supplies the other auxiliary capacitor bus line with the rectangular voltage signal of smaller amplitude, the source driver supplies the source signal of larger amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line; and

in a case where the other auxiliary capacitor driver supplies the other auxiliary capacitor bus line with the rectangular voltage signal of larger amplitude, the source driver supplies the source signal of smaller amplitude to that one of the source bus lines which is connected via the capacitor and the transistor to the other auxiliary capacitor bus line.

29. The display panel as set forth in claim **1**, wherein:

in a case where the one end of the capacitor is connected to the transistor connected to the *n*th gate bus line of the plurality of gate bus lines and the *m*th source bus line of the plurality of source bus lines, the other end of the capacitor is connected to the *n*th auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines; and

in a case where the one end of the capacitor is connected to the transistor connected to the *n*th gate bus line of the plurality of gate bus lines and the (*m*+1)th source bus line of the plurality of source bus lines, the other end of the capacitor is connected to the (*n*-1)th auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines.

30. A liquid crystal display device comprising a display panel as set forth in claims **1**.

31. A method for driving a display panel including:

a plurality of gate bus lines;

a plurality of source bus lines;

a plurality of auxiliary capacitor bus lines;

a transistor including a gate connected to a given gate bus line of the plurality of gate bus lines and a source connected to a given source bus line of the plurality of source bus lines;

a pixel electrode connected to a drain of the transistor;

a capacitor, one end of which is connected to the drain of the transistor in parallel with the pixel electrode, and the other end of which is connected to a given auxiliary capacitor bus line of the plurality of auxiliary capacitor bus lines;

a source driver, connected to one end of each of the plurality of source bus lines, which supplies the given source bus line with a source signal;

a gate driver, connected to one end of each of the plurality of gate bus lines, which sequentially supplies the given gate bus line with a conducting signal that renders the transistor conducting;

a counter electrode opposed to the pixel electrode via a liquid crystal;

a counter electrode wire connected to the counter electrode; and

a counter electrode driver, which supplies the counter electrode wire with a common potential,

the method comprising a voltage signal supplying step of, in a single scanning period from a point in time where the gate driver supplies the given gate bus line with the conducting signal to a point in time where the gate driver supplies the conducting signal next, supplying the given auxiliary capacitor bus line with a rectangular voltage signal in synchronization with the conducting signal, the rectangular voltage signal being composed of at least a first voltage level and a second voltage level that is different from the first voltage level,

in the single scanning period, a period of time during which the rectangular voltage signal is at the first voltage level and a period of time during which the rectangular voltage signal is at the second voltage level being each longer than a response time of the liquid crystal.

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专利名称(译)	显示面板，液晶显示器和驱动方法		
公开(公告)号	US20120242646A1	公开(公告)日	2012-09-27
申请号	US13/514082	申请日	2010-09-22
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	YAMATO ASAHI		
发明人	YAMATO, ASAHI		
IPC分类号	G09G3/36 G06F3/038		
CPC分类号	G02F1/136213 G02F2001/133397 G09G3/3614 G09G2320/0247 G09G3/3655 G09G2300/0876 G09G2320/0219 G09G3/3648		
优先权	2009282187 2009-12-11 JP		
外部链接	Espacenet USPTO		

摘要(译)

一种显示面板，包括：栅极驱动器（13），其向多条栅极总线（GL1至GLN）提供栅极信号；源极驱动器（12），其向多个源极总线（SL1至SLM）提供源极信号；多个辅助电容总线（CSL1至CSLN）；以及辅助电容驱动器（14），其在单个扫描周期（TV）中从栅极驱动器（13）向栅极总线（GLn）提供导通信号的时间点到栅极的时间点驱动器（13）接下来提供导通信号，与导通信号同步地提供具有矩形电压信号（#CSLn）的辅助电容总线（CSLn），矩形电压信号（#CSLn）至少由第一个组成电压电平（VCS1）和不同于第一电压电平的第二电压电平（VCS2）。这允许显示面板抑制运动图像模糊的现象，同时抑制制造成本和功耗的增加。

