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(54) APPARATUS AND METHOD FOR DRIVING LIQUID CRYSTAL DISPLAY DEVICE

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(57) **ABSTRACT**

An apparatus and method for driving a liquid crystal display device are disclosed. The apparatus includes a liquid crystal panel with pixels defined by data and gate lines. A gate driver provides different gate pulses to the odd-column pixels than to the even-column pixels. The gate pulses have different voltages and/or widths. Data drivers provide data voltages having a positive or negative polarity to the data lines. A timing controller controls the gate and data drivers and supplies gate clock pulses that have different voltages and/or widths to the gate driver.

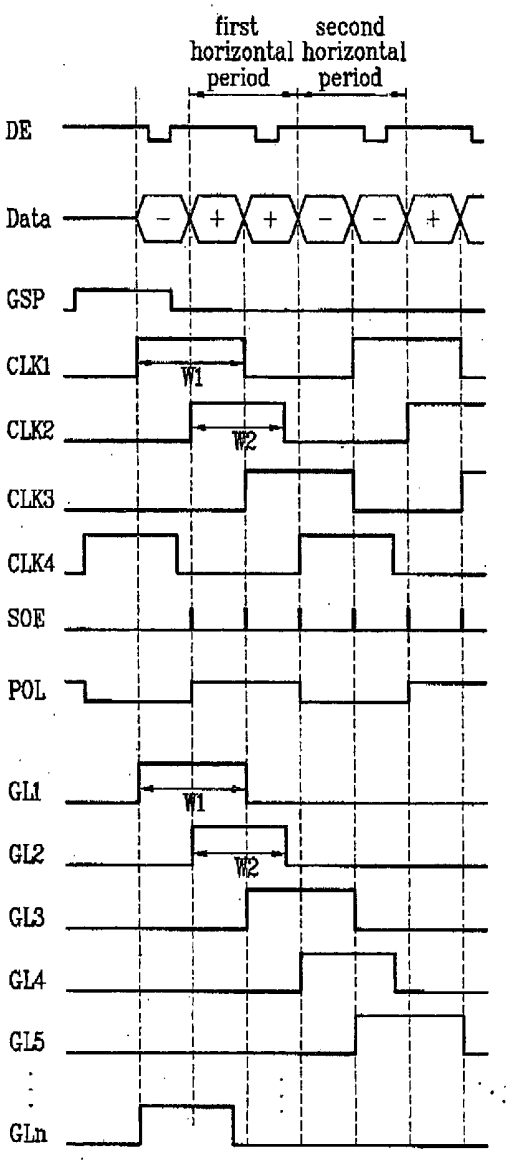


FIG. 1A
Related Art

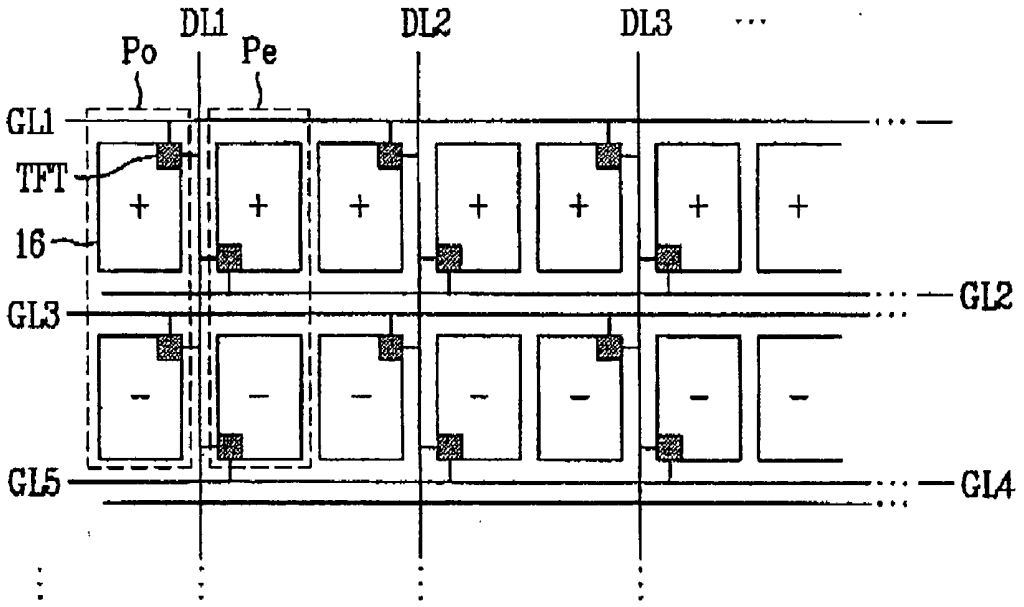


FIG. 1B
Related Art

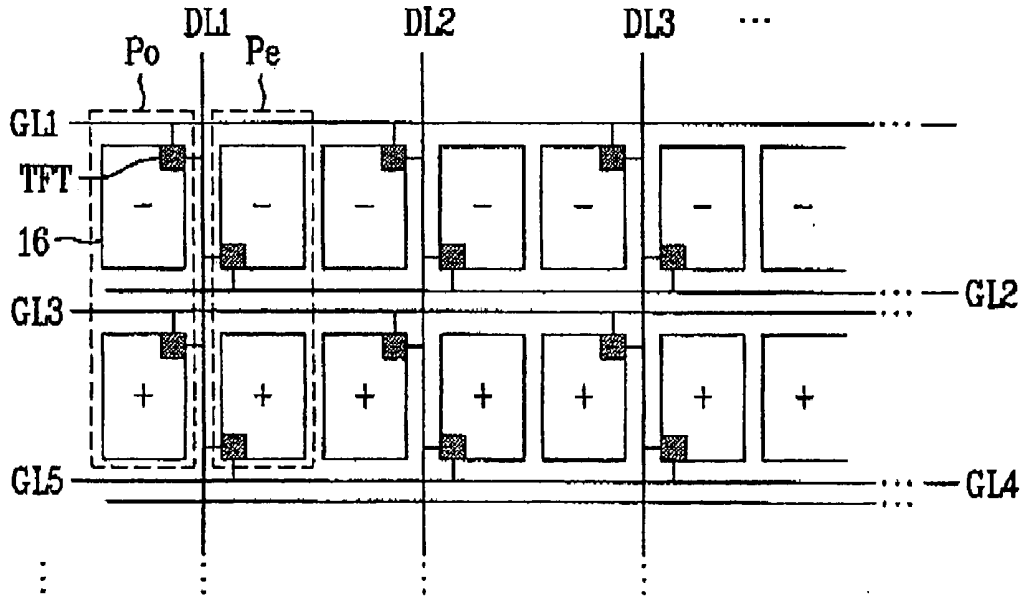


FIG. 2
Related Art

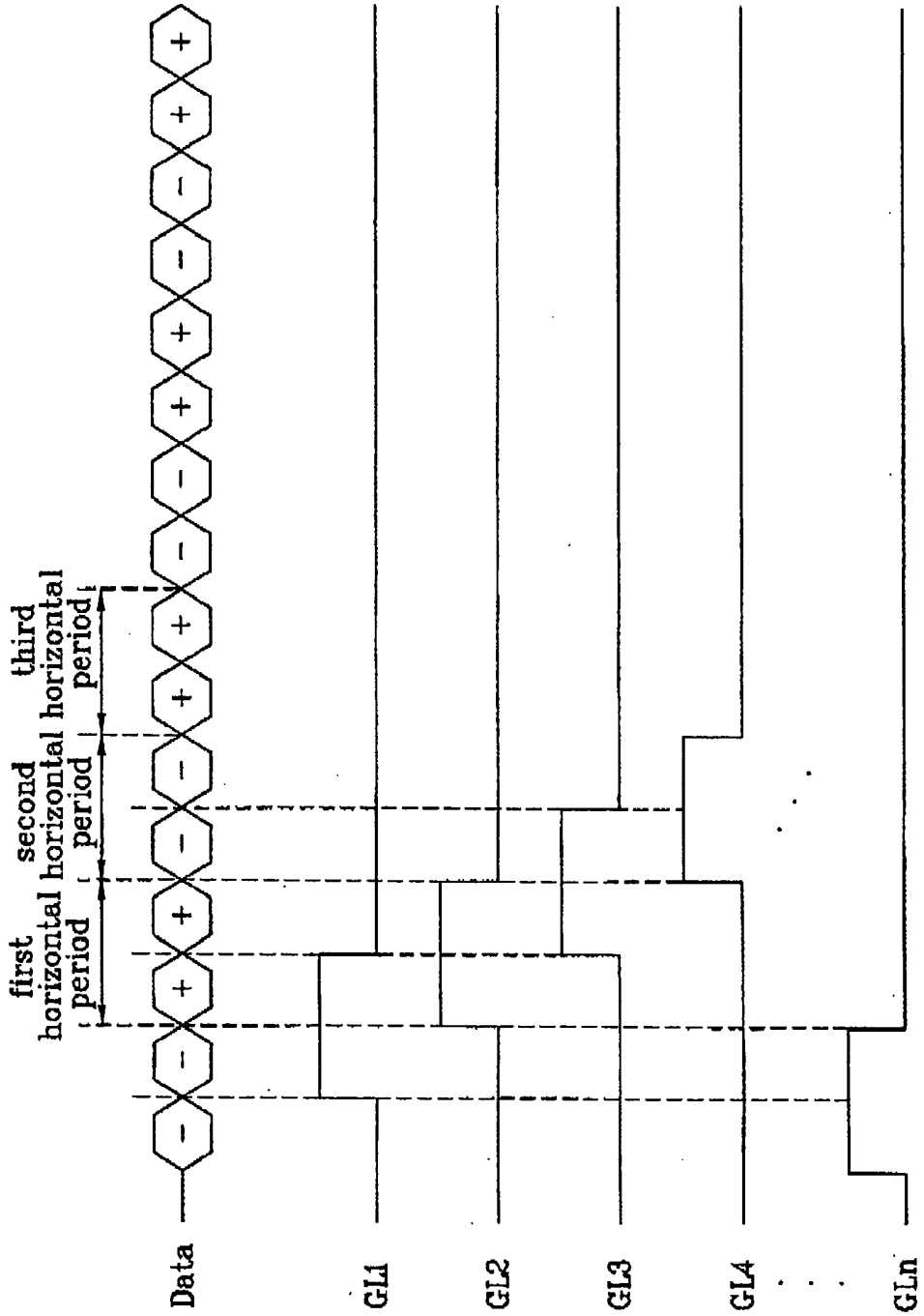


FIG. 3

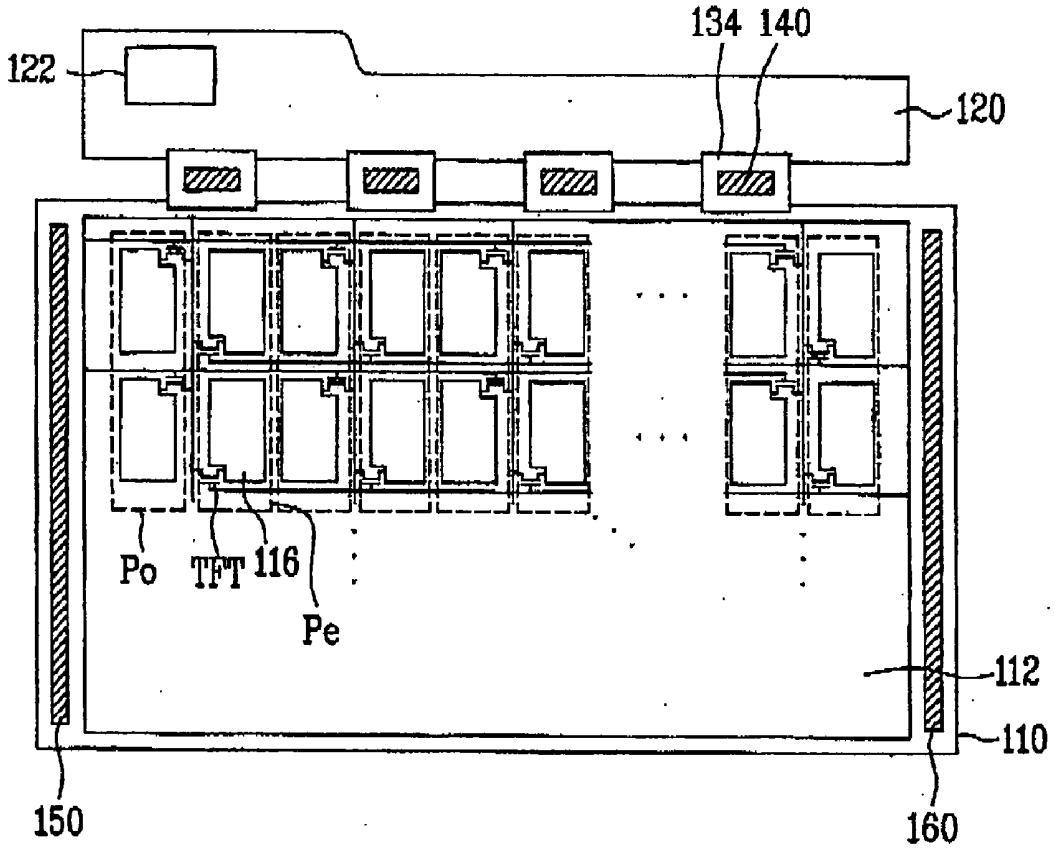


FIG. 4

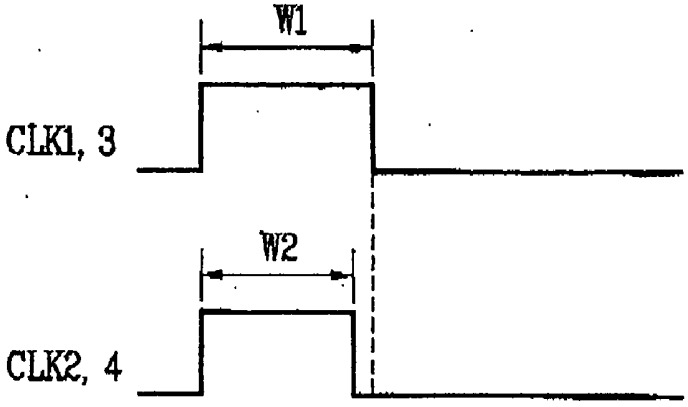


FIG. 5

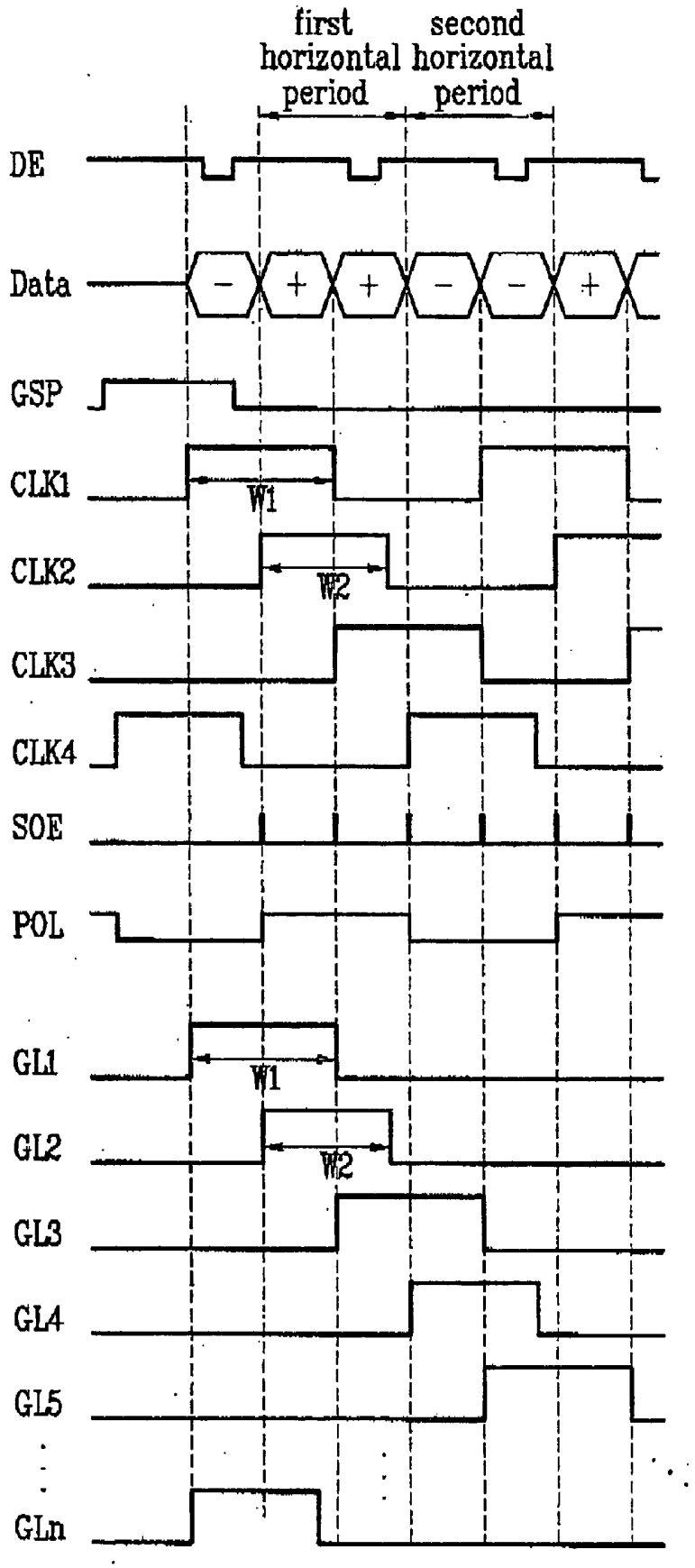

first horizontal period
second horizontal period
DE
Data
GSP
CLK1
CLK2
CLK3
CLK4
SOE
POL
GL1
GL2
GL3
GL4
GL5
GLn
W1
W2
W1
W2

FIG. 6

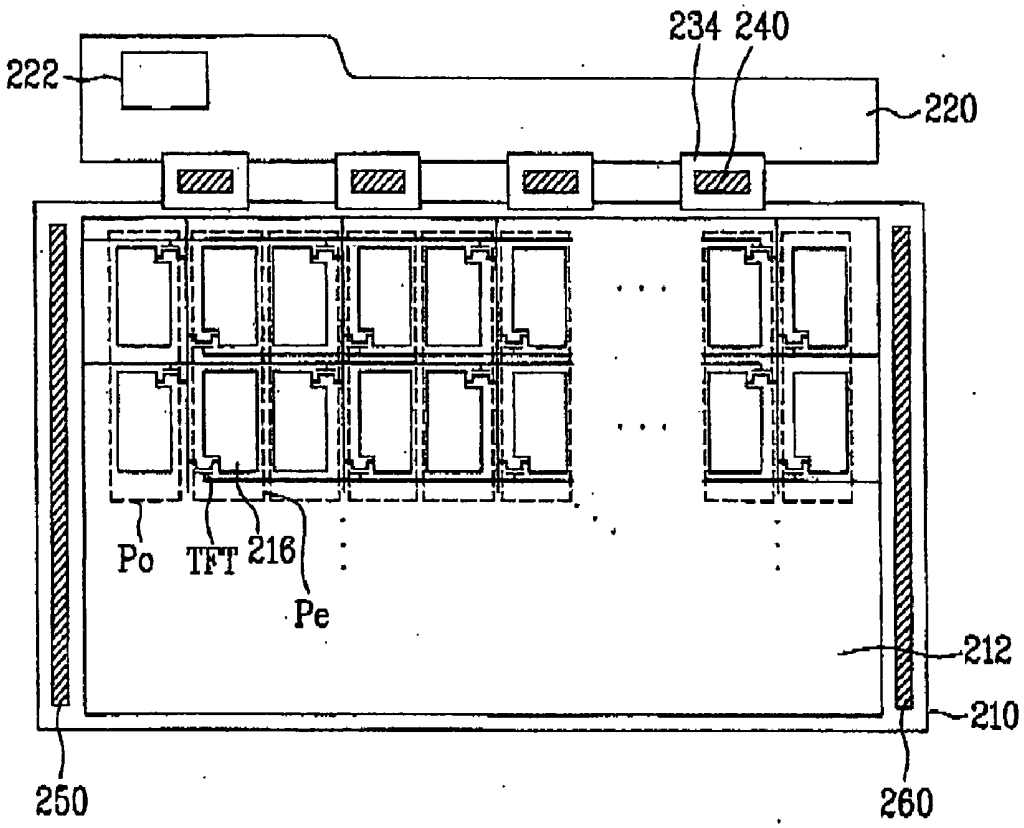


FIG. 7

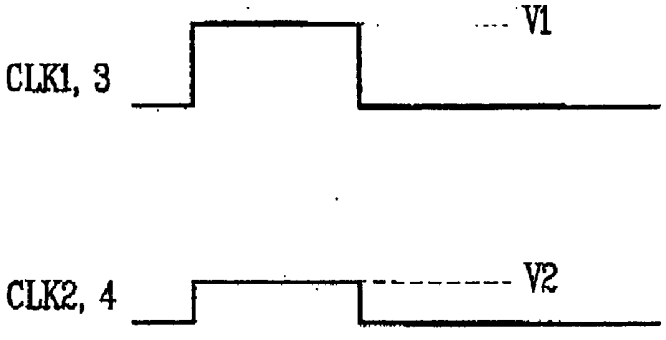


FIG. 8

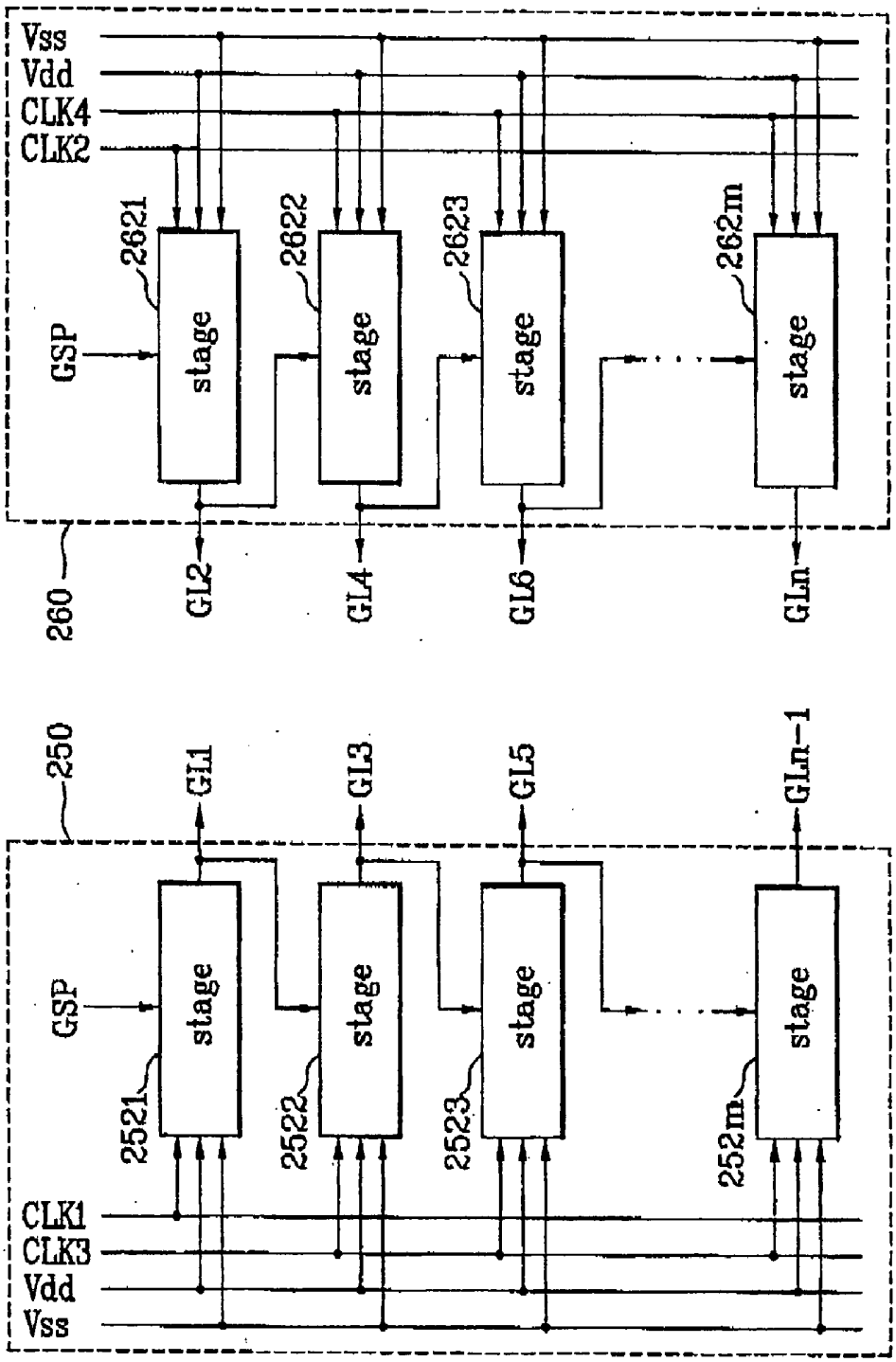

Vss
Vdd
CLK4
CLK2
2621
2622
2623
262m
GSP
stage
stage
stage
stage
260
GL2
GL4
GL6
GLn
250
GL1
GL3
GL5
GLn-1
GSP
stage
stage
stage
stage
2521
2522
2523
252m
CLK1
CLK3
Vdd
Vss

FIG. 9

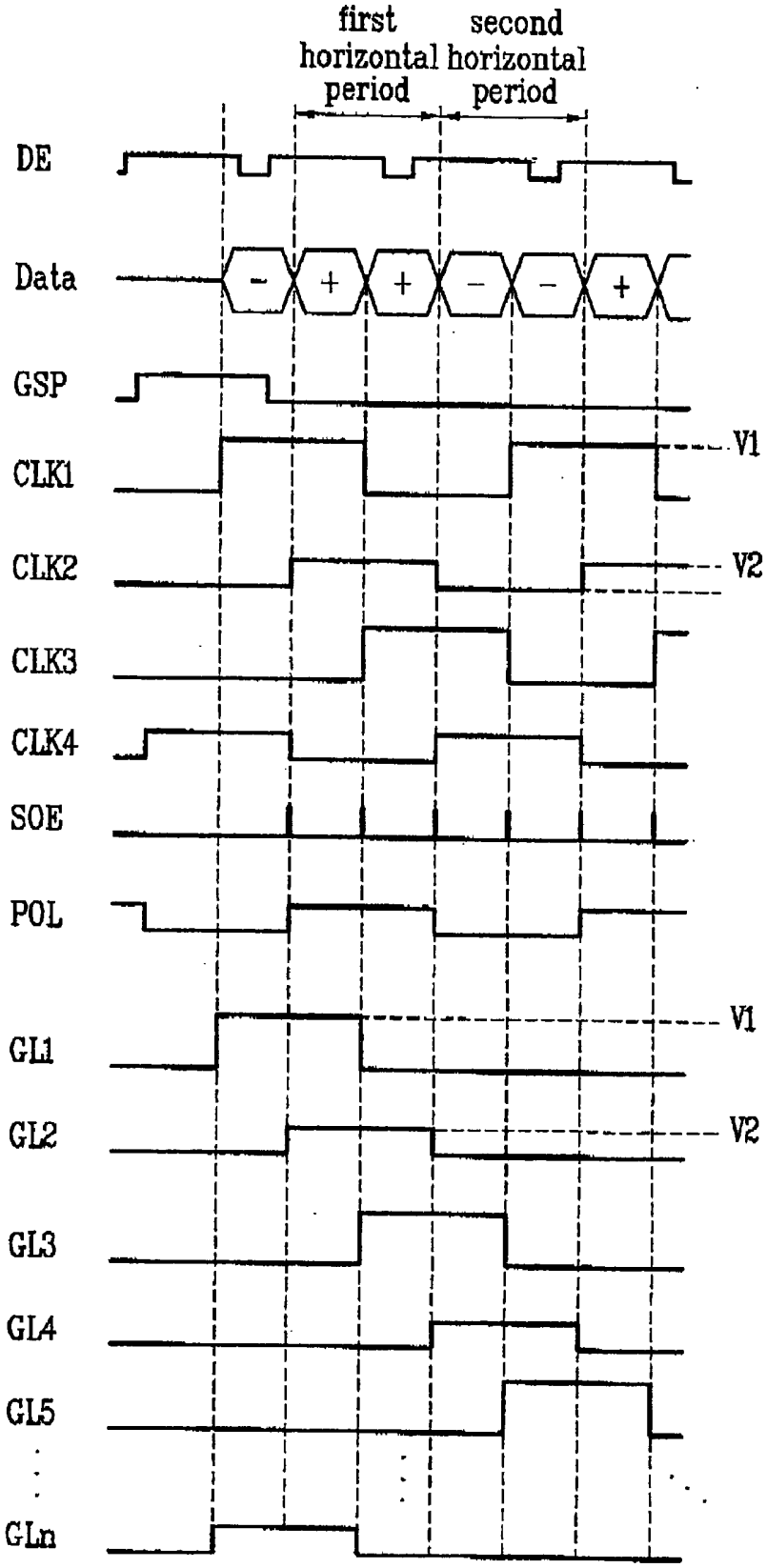

first horizontal period
second horizontal period
DE
Data
GSP
CLK1
CLK2
CLK3
CLK4
SOE
POL
GL1
GL2
GL3
GL4
GL5
GLn
V1
V2
V1
V2

FIG. 10

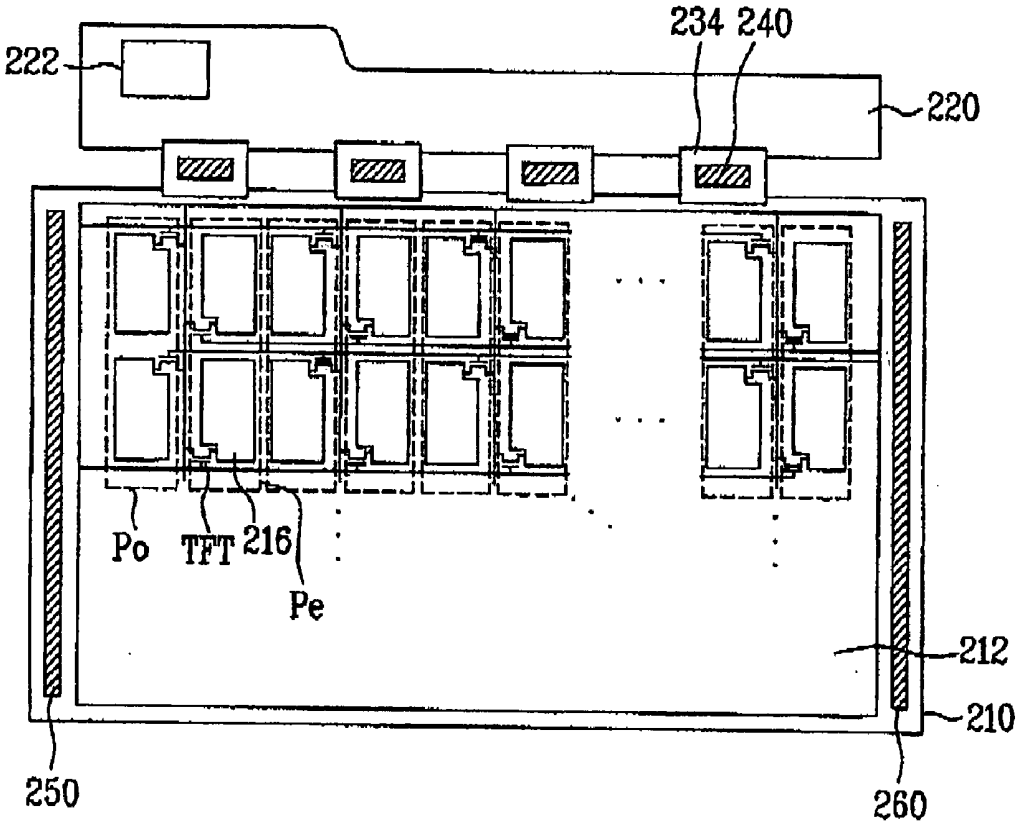


FIG. 11

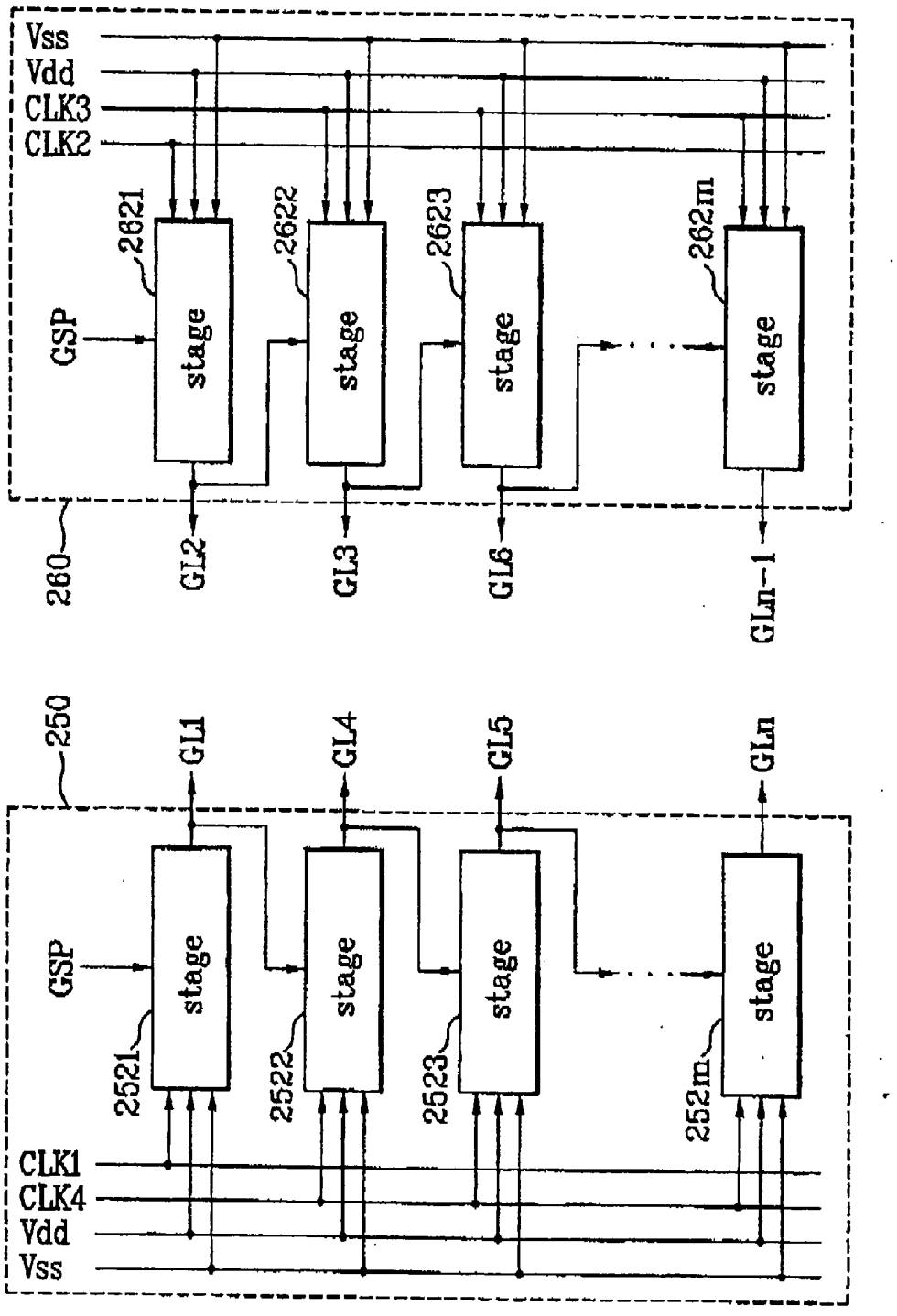

Vss
Vdd
CLK3
CLK2
2621
2622
2623
262m
GSP
stage
stage
stage
stage
260
GL2
GL3
GL6
GLn-1
250
GL1
GL4
GL5
GLn
GSP
stage
stage
stage
stage
2521
2522
2523
252m
CLK1
CLK4
Vdd
Vss

FIG. 12

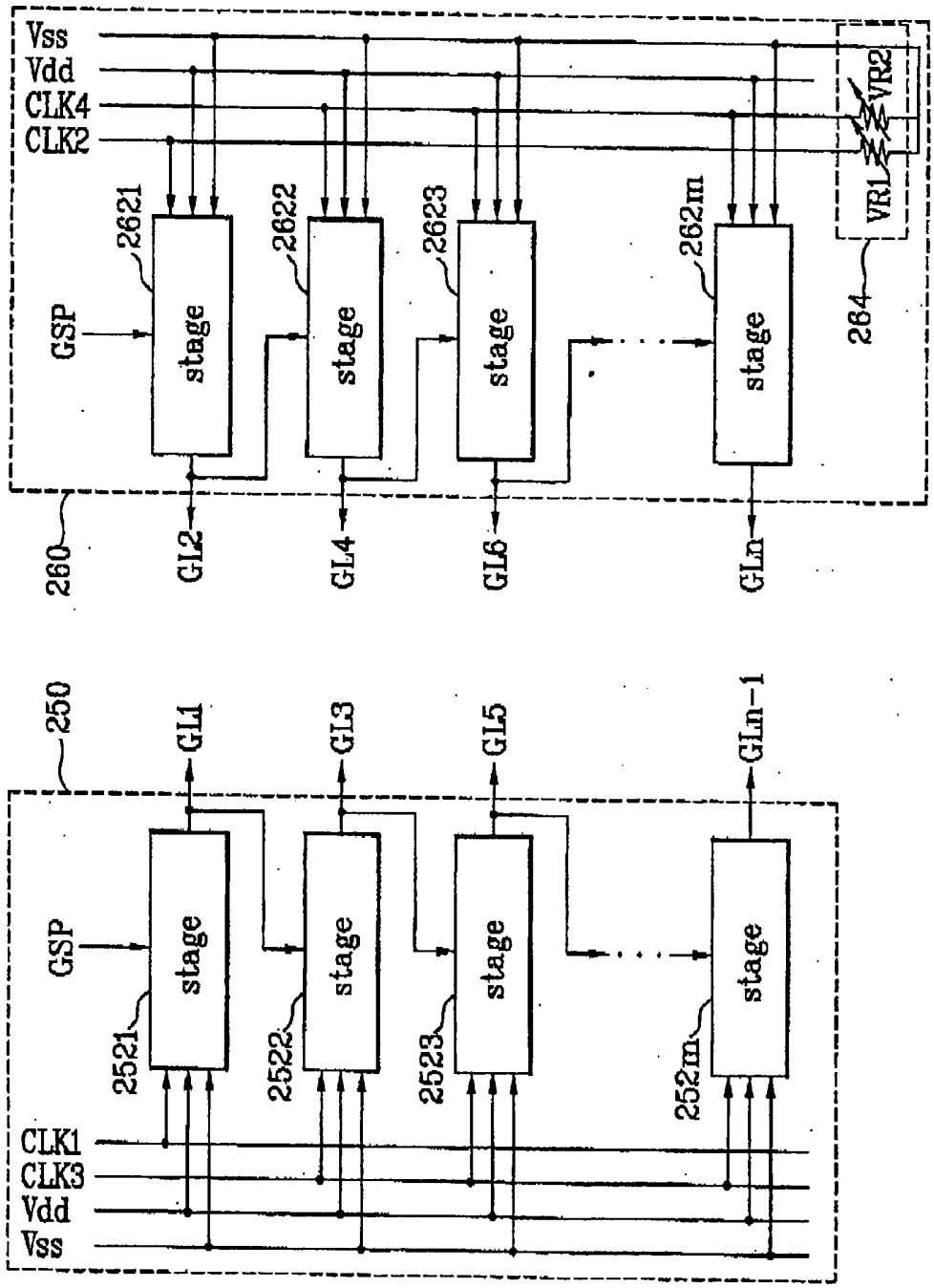

Vss
Vdd
CLK4
CLK2
VR2
VR1
264
2621
2622
2623
262m
GSP
stage
260
GL2
GL4
GL6
GLn
250
GL1
GL3
GL5
GLn-1
2521
2522
2523
252m
CLK1
CLK3
Vdd
Vss

FIG. 13

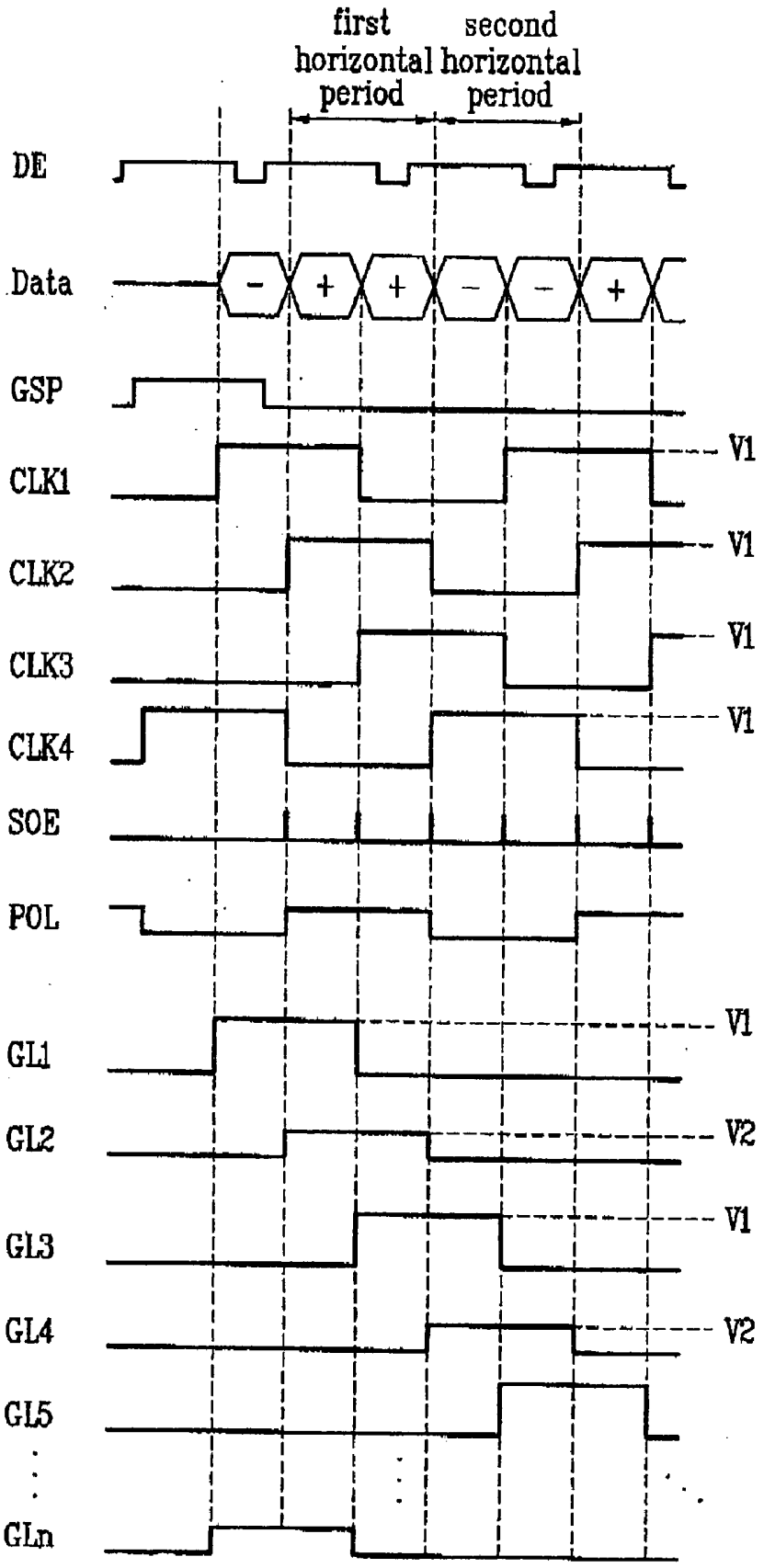
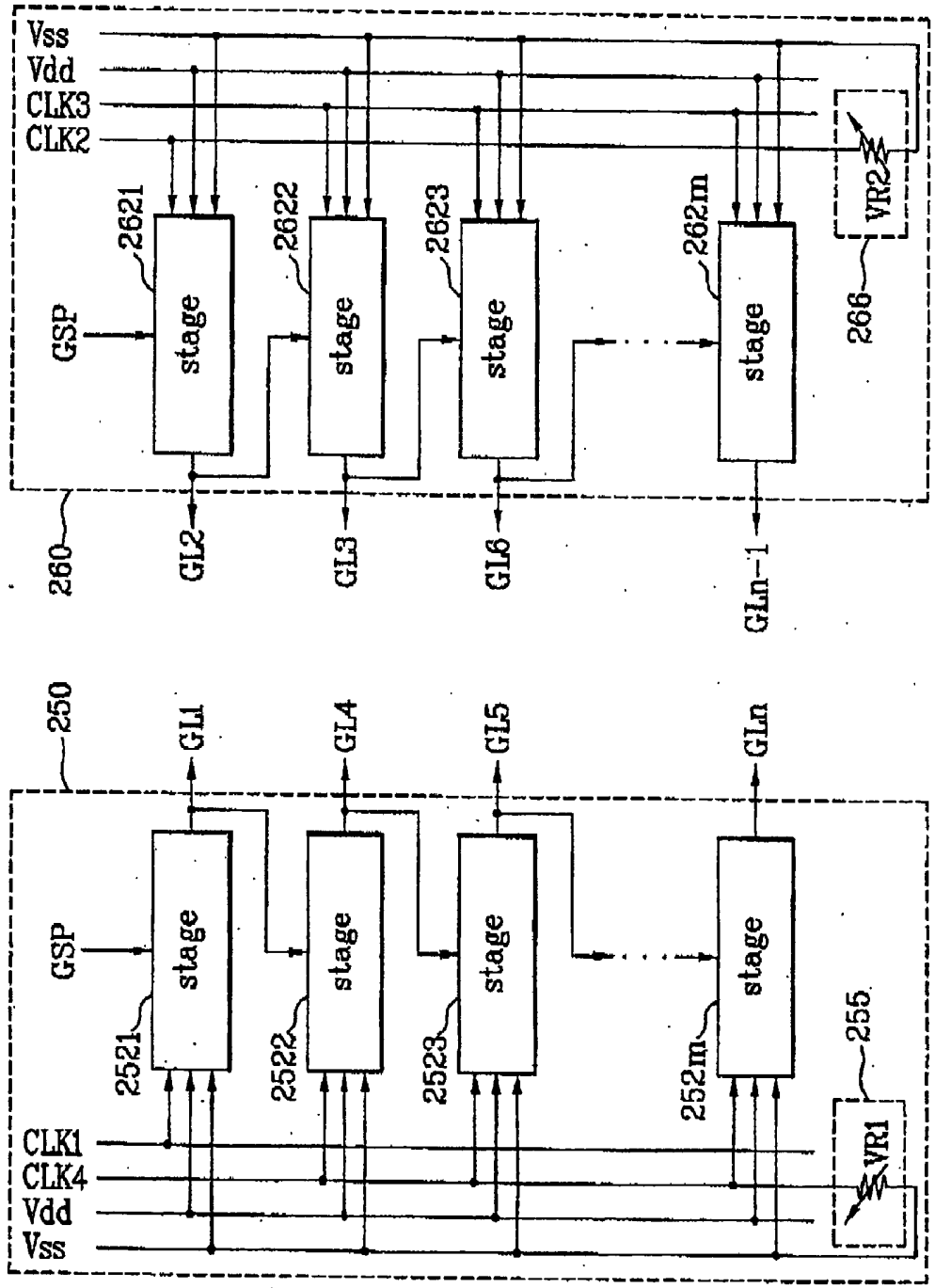

first horizontal period
second horizontal period
DE
Data
GSP
CLK1
CLK2
CLK3
CLK4
SOE
POL
GL1
GL2
GL3
GL4
GL5
GLn
V1
V2

FIG. 14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Vdd
CLK3
CLK2
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2623
262m
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GSP
stage
stage
stage
stage
266
260
GL2
GL3
GL6
GLn-1
250
GL1
GL4
GL5
GLn
GSP
stage
stage
stage
stage
255
2521
2522
2523
252m
VR1
CLK1
CLK4
Vdd
Vss

FIG. 15

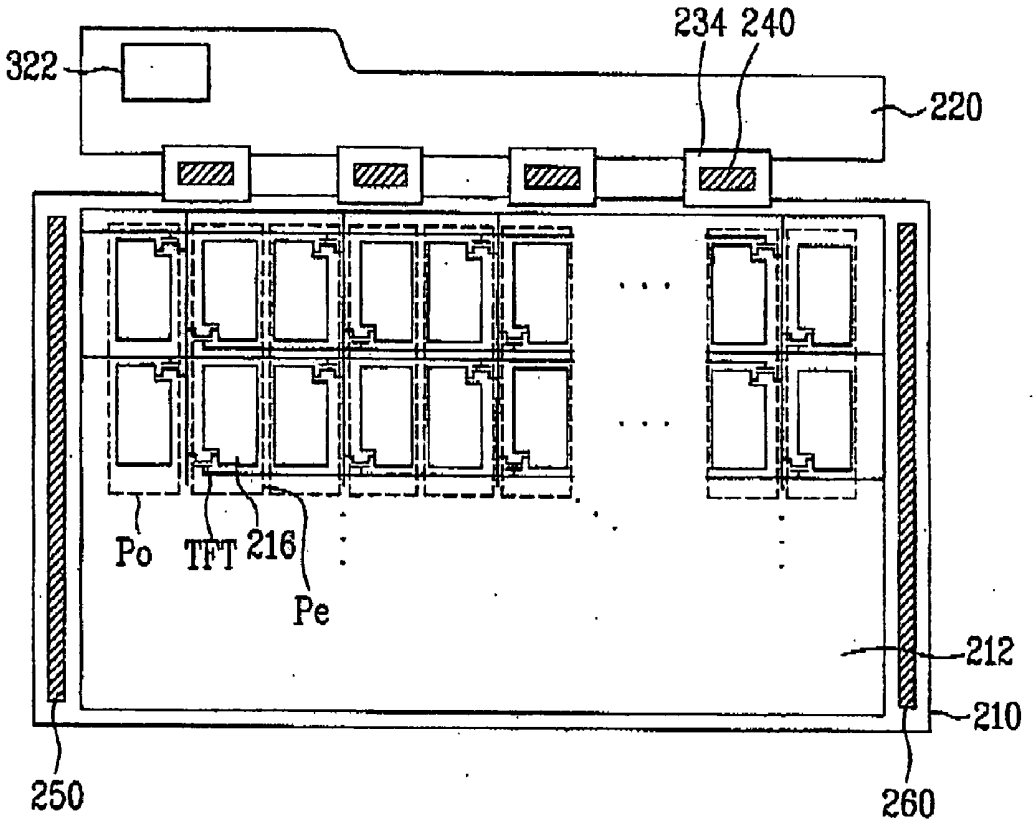

234 240
322
220
Po
TFT
216
Pe
212
210
250
260

FIG. 16

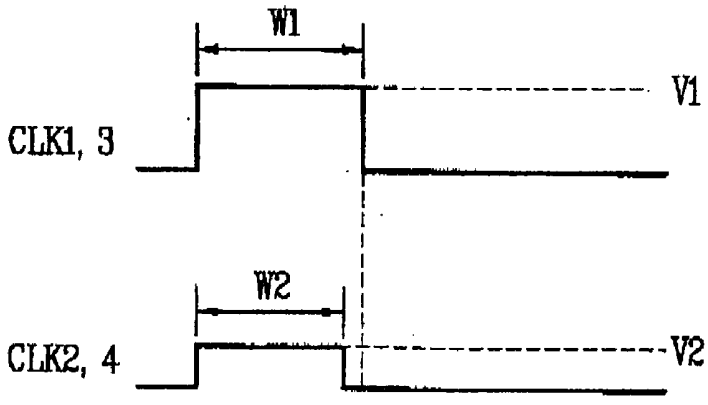

W1
V1
CLK1, 3
W2
CLK2, 4
V2

FIG. 17

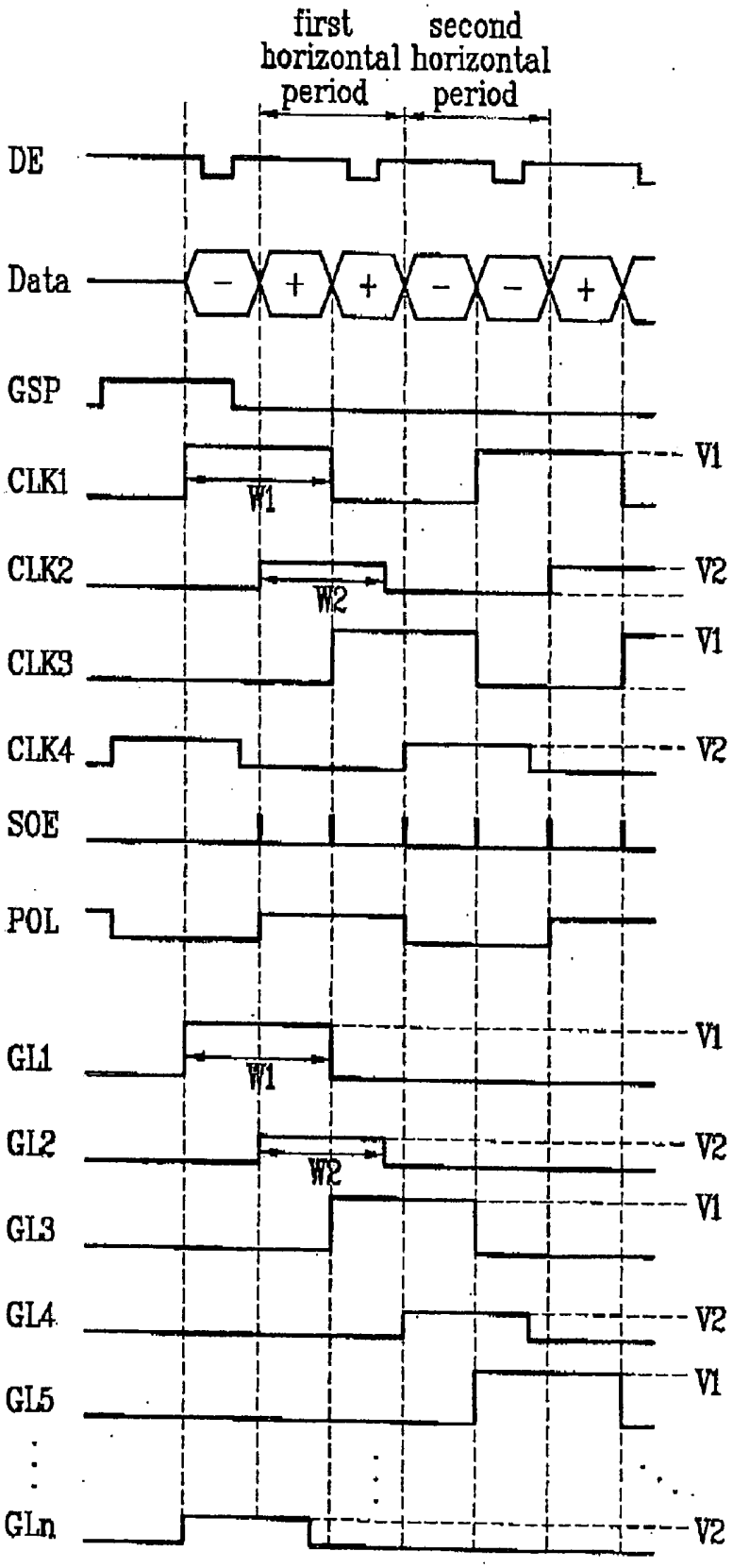

first horizontal period
second horizontal period
DE
Data
GSP
CLK1
CLK2
CLK3
CLK4
SOE
POL
GL1
GL2
GL3
GL4
GL5
GLn
W1
W2
V1
V2

FIG. 18

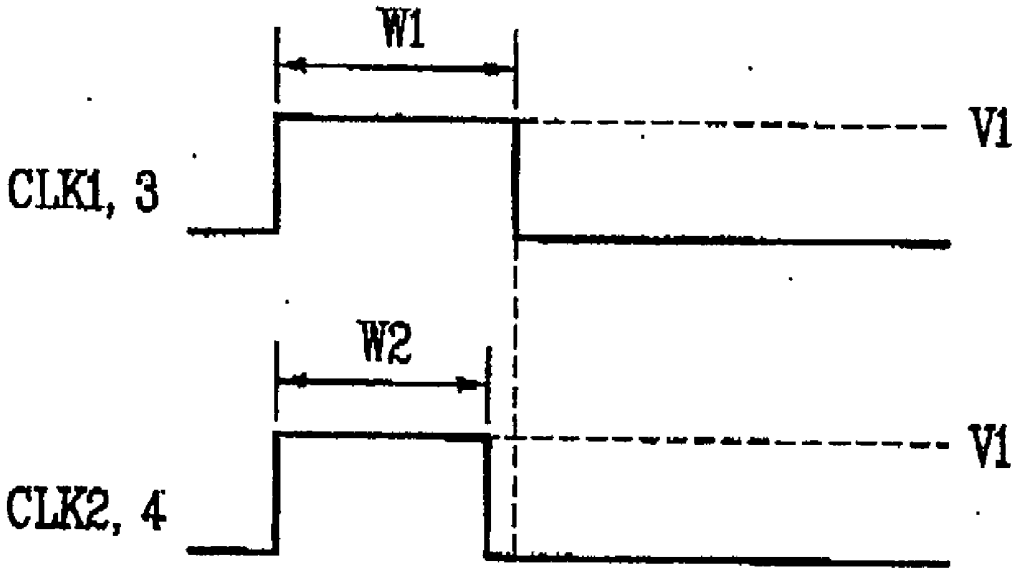
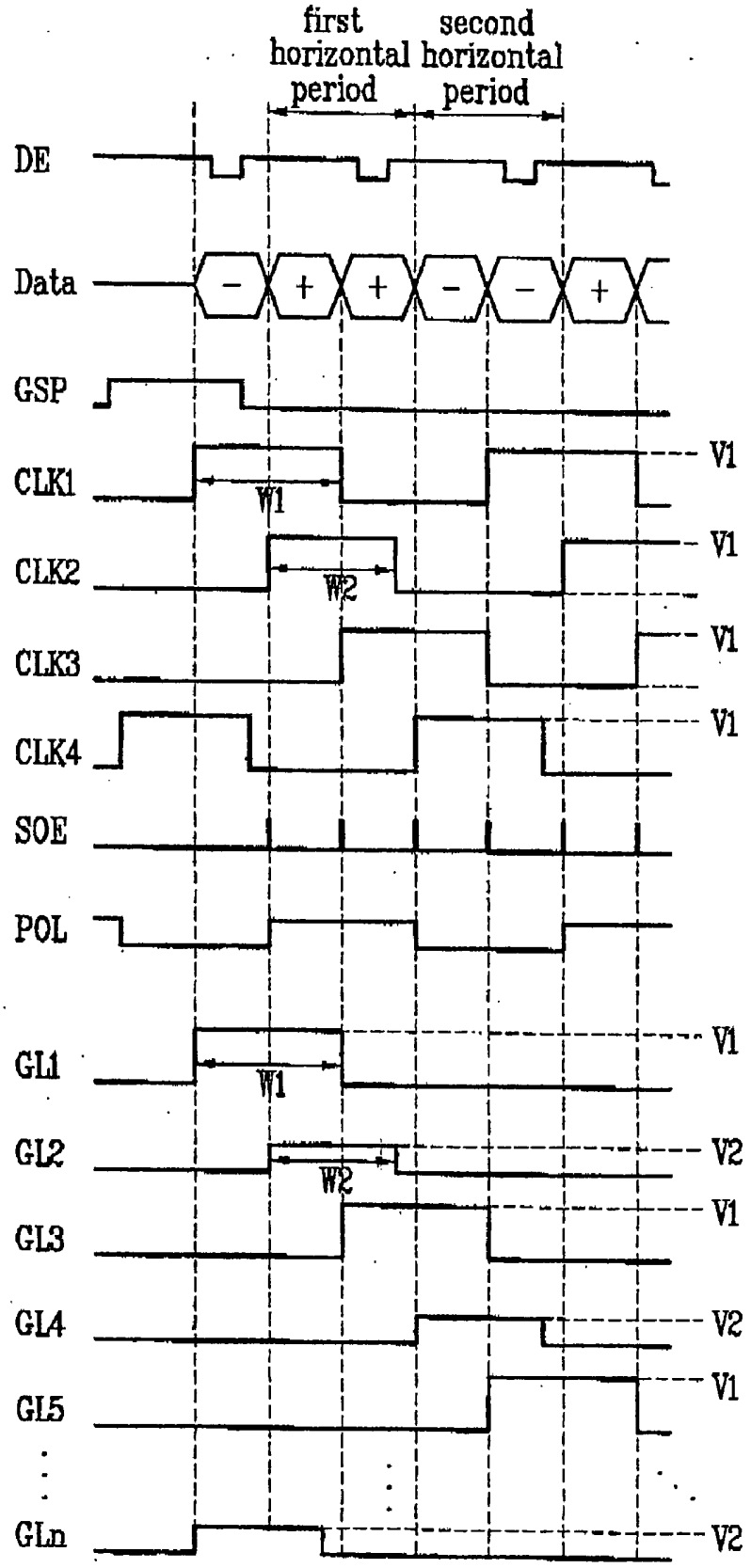


FIG. 19


first horizontal period
second horizontal period
DE
Data
GSP
CLK1
CLK2
CLK3
CLK4
SOE
POL
GL1
GL2
GL3
GL4
GL5
GLn
W1
W2
V1
V2

APPARATUS AND METHOD FOR DRIVING LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of Korean Patent Application Nos. P2005-51395 filed on Jun. 15, 2005, P2005-57002 filed on Jun. 29, 2005, which are hereby incorporated by reference as if fully set forth herein.

FIELD OF THE INVENTION

[0002] The present invention relates to a liquid crystal display device, and more particularly, to an apparatus and method for driving a liquid crystal display device, in which vertical dimming is minimized to improve picture quality.

DISCUSSION OF THE RELATED ART

[0003] In recent years, various flat panel display devices, which have advantages over cathode ray tubes in terms of weight and size, conventional weaknesses of cathode ray tubes, have entered into widespread use. These flat panel display devices include liquid crystal displays, field emission displays, plasma display panels, and light emitting displays.

[0004] Among these flat panel display devices displays, a liquid crystal displays (LCD) device an image by controlling light transmittance of a liquid crystal.

[0005] To this end, an active matrix type LCD is known which uses a thin film transistor (TFT) as a switching element. The active matrix type LCD comprises a TFT array substrate, a facing substrate placed a predetermined distance therefrom, and a liquid crystal material sealed between the two substrates. In the TFT array substrate, gate lines and data lines are formed in a matrix array, and TFTs are arranged at intersections of the gate lines and data lines. A voltage applied to the liquid crystal material is controlled by the TFTs to display images using electro optical effects of the liquid crystal material.

[0006] As the number of pixels increases owing to a high definition display of the active matrix type LCD, the number of the gate lines and data lines has become very large. Accordingly, the number of driving integrated circuits (driving ICs) also increases, raising costs. In addition, a pad pitch for bonding in the driving ICs and the array substrate decreases, hence bonding yield decreases owing to the difficulty of bonding between the driving ICs and the array substrate.

[0007] To solve these problems simultaneously, an LCD device and driving method thereof have been proposed in Korean Patent Publication No. 2005-0000105 (published Jan. 3, 2005), in which a voltage from one data line is supplied to two adjacent pixels in a time-divided fashion to reduce the number of data driving ICs and costs.

[0008] In the LCD device and driving method thereof proposed in Korean Patent Publication No. 2005-0000105, the polarity of data voltage is reversed on a frame-by-frame, line-by-line, or dot-by-dot basis. Gate pulses are supplied to associated gate lines such that they overlap with one another for a ½ horizontal period during each horizontal period.

[0009] **FIG. 2** is a waveform diagram illustrating polarities of data voltages and gate pulses supplied to pixels shown in **FIGS. 1A and 1B**.

[0010] Firstly, data voltage is supplied such that its polarity is reversed for every horizontal line. Gate pulses are supplied to associated gate lines such that the gate pulse supplied to one gate line overlaps with that of the previous gate line for a ½ horizontal period. Here, the gate pulses supplied to the gate lines have the same pulse width.

[0011] Consequently, in every horizontal period, each pixel **16** (shown in **FIGS. 1A and 1B**) is precharged with data voltage during a first period, for which the gate pulse supplied to the associated gate line overlaps with that of the previous gate line, and is charged with data voltage during the remaining second period.

[0012] Hereinafter, this operation will be described in detail with reference to **FIG. 2** and **FIGS. 1A and 1B**.

[0013] Firstly, during a period just before the first period of a first horizontal period, the odd pixels **16** connected to a first gate line GL**1** are precharged with data voltage having a negative (−) polarity supplied from the data lines DL to the pixels **16** of the last horizontal line, respectively, by a gate pulse overlapped with a gate pulse supplied to an Nth gate line.

[0014] Next, during the first period of the first horizontal period, each odd pixel **16** connected to the first gate line GL**1** and precharged with the negative-polarity data voltage is charged with data voltage having a positive (+) polarity for odd pixels provided from the associated data line DL, by the gate pulse provided to the first gate line GL**1**.

[0015] Also, during the first period of the first horizontal period, each even pixel **16** connected to a second gate line GL**2** is precharged with data voltage having a positive (+) polarity for odd pixels provided from the associated data line DL, by the gate pulse provided to the second gate line GL**2** to overlap with the gate pulse supplied to the first gate line.

[0016] Next, during a second period of the first horizontal period, each odd pixel **16** connected to the second gate line GL**2** precharged with the positive-polarity data voltage for odd pixels is charged with data voltage having a positive (+) polarity for even pixels provided from each of the associated data lines DL, by the gate pulse provided to the second gate line GL**2**.

[0017] Also, during the second period of the first horizontal period, each odd pixel **16** connected to a third gate line GL**3** is precharged with data voltage having a positive (+) polarity for even pixels provided from the associated data line DL, by the gate pulse provided to the third gate line GL**3** to overlap with the gate pulse supplied to the second gate line.

[0018] Consequently, during the first horizontal period, the associated odd and even pixels **16** respectively connected to the left and the right of each data line DL are charged with the positive-polarity data voltage.

[0019] Next, during a first period of a second horizontal period, each odd pixel **16** connected to a third gate line GL**3** precharged with the positive-polarity data voltage is charged with data voltage having a negative (−) polarity for odd pixels provided from the associated data line DL, by the gate pulse provided to the third gate line GL**3**.

[0020] Also, during the first period of the second horizontal period, each even pixel **16** connected to a fourth gate line

GL**4** is precharged with data voltage having a negative (−) polarity for odd pixels provided from the associated data line DL, by the gate pulse provided to the fourth gate line GL**4** to overlap with the gate pulse supplied to the third gate line.

[**0021**] Next, during a second period of the second horizontal period, each even pixel **16** connected to the fourth gate line GL**4** precharged with the negative-polarity data voltage for odd pixels is charged with data voltage having negative (−) polarity for odd pixels provided from the associated data line DL, by the gate pulse provided to the fourth gate line GL**4**.

[**0022**] Also, during the second period of the second horizontal period, each odd pixel **16** connected to a fifth gate line GL**5** is precharged with data voltage having a negative (−) polarity for even pixels provided from the associated data line DL, by the gate pulse provided to the fifth gate line GL**5** to overlap with the gate pulse supplied to the fourth gate line.

[**0023**] Consequently, during the second horizontal period, the associated odd and even pixels **16** respectively connected to the left and the right of each data line DL are charged with the negative-polarity data voltage.

[**0024**] During a third to Nth horizontal periods, in the same way as the first and the second horizontal periods, gate pulses having the same pulse width are supplied to the gate lines connected with the odd and even pixels **16** associated with each data line, respectively, and positive and negative polarity data voltages are supplied to each data line.

[**0025**] In sum, the driving method proposed in Korean Patent Publication No. 2005-0000105, drives the LCD device using a line inversion scheme.

[**0026**] However, in the LCD device and the driving method thereof proposed in Korean Patent Publication No. 2005-0000105, because gate pulses having the same pulse width and pulse height are sequentially supplied to the gate lines, there exists a problem in that vertical dimming occurs owing to a brightness difference between odd-column pixels Po connected to one side of each one of the data lines and odd gate lines GL**1**, GL**3**, . . . , GLn−1 and even-column pixels Pe connected to the other side of each one of the data lines and even gate lines GL**2**, GL**4**, . . . , GLn.

[**0027**] Specifically, while the polarity of the precharged data voltage is opposite to the polarity of the charged data voltage in the odd-column pixels Po, the polarity of the precharged data voltage is equal to the polarity of the charged data voltage in the even-column pixels Pe. Namely, the odd-column pixels Po are either charged with the positive-polarity data voltage after being precharged with the negative-polarity voltage or are charged with the negative-polarity data voltage after being precharged with the positive-polarity voltage. To the contrary, the even-column pixels Pe are either charged with the negative-polarity data voltage after being precharged with the negative-polarity voltage or charged with the positive-polarity data voltage after being precharged with the positive-polarity voltage. Thus, the data voltages for precharge respectively applied to the odd-column pixels Po and the even-column pixels Pe have different polarities.

[**0028**] Accordingly, in the LCD device and the driving method thereof proposed in Korean Patent Publication No. 2005-0000105, there is a problem in that picture quality is degraded owing to the vertical dimming caused by a difference between the data voltage charged at each of the odd-column pixels Po and the data voltage charged at each of the even-column pixels Pe.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0029**] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[**0030**] **FIGS. 1A and 1B** illustrate arrangements of pixels in conventional line inversion scheme;

[**0031**] **FIG. 2** is a waveform diagram illustrating polarities of data voltages and gate pulses supplied to the pixels of **FIGS. 1A and 1B**;

[**0032**] **FIG. 3** illustrates an apparatus for driving a liquid crystal display device according to the first embodiment of the present invention;

[**0033**] **FIG. 4** is a waveform diagram illustrating a first to fourth gate shift clocks generated from a timing controller of **FIG. 3**;

[**0034**] **FIG. 5** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the first embodiment of the present invention;

[**0035**] **FIG. 6** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the second embodiment of the present invention;

[**0036**] **FIG. 7** is a waveform diagram illustrating a first to fourth gate shift clocks generated from a timing controller of **FIG. 6**;

[**0037**] **FIG. 8** illustrates a gate driver of **FIG. 7**;

[**0038**] **FIG. 9** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the second embodiment of the present invention;

[**0039**] **FIG. 10** illustrates an apparatus for driving a liquid crystal display device according to the third embodiment of the present invention;

[**0040**] **FIG. 11** illustrates a gate driver of **FIG. 10**;

[**0041**] **FIG. 12** illustrates a gate driver in an apparatus for driving a liquid crystal display device according to the fourth embodiment of the present invention;

[**0042**] **FIG. 13** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the fourth embodiment of the present invention; and

[**0043**] **FIG. 14** illustrates a gate driver in an apparatus for driving a liquid crystal display device according to the fifth embodiment of the present invention.

[**0044**] **FIG. 15** illustrates an apparatus for driving a liquid crystal display device according to the sixth embodiment of the present invention;

[**0045**] **FIG. 16** is a waveform diagram illustrating a first to fourth gate shift clocks generated from a timing controller of **FIG. 15**;

[0046] **FIG. 17** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the sixth embodiment of the present invention;

[0047] **FIG. 18** is a waveform diagram illustrating a first to fourth gate shift clocks according to the seventh embodiment of the present invention generated from a timing controller of **FIG. 15**; and

[0048] **FIG. 19** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the seventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0049] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0050] **FIG. 3** illustrates an apparatus for driving a liquid crystal display device according to the first embodiment of the present invention.

[0051] Referring to **FIG. 3**, the apparatus for driving a liquid crystal display device comprises a liquid crystal panel **110**. The liquid crystal panel **110** comprises an image display **112** including a plurality of data lines DL and a plurality of gate lines GL. The image display **112** also includes odd-column pixels Po each of which is connected to a first side of one of the data lines DL and connected to one of the odd gate lines GL**1**, GL**3**, . . . , GLn−1, and even-column pixels Pe each of which is connected to a second side of one of the data lines and connected to one of the even gate lines GL**2**, GL**4**, . . . , GLn. The driving apparatus also comprises a gate driver for providing first and second gate pulses having different widths to the odd gate lines GL**1**, GL**3**, . . . , GL n−1 and the even gate lines GL**2**, GL**4**, . . . , GLn, respectively, and a plurality of data integrated circuits **140** for providing data voltages having a positive or negative polarity to the data lines DL, respectively. The driving apparatus further comprises a timing controller **122** for performing supply and control of data signals to provide the data voltages to the data lines DL, and for controlling the gate driver.

[0052] The apparatus for driving a liquid crystal display according to the first embodiment of the present invention further comprises a printed circuit board **120**, on which a power circuit (not shown) is mounted together with the timing controller **122**, and a plurality of tape carrier packages (hereinafter, referred to as "TCPs") **134**, which are connected between the printed circuit board **120** and the liquid crystal panel **110**. The data integrated circuits **140** are mounted in the TCPs **134**, respectively.

[0053] The gate driver of the liquid crystal display driving apparatus includes a first gate driver circuit **150** for providing gate pulses having a first width to the odd gate lines GL**1**, GL**3**, . . . , GLn−1, and a second gate driver circuit **160** for providing gate pulses having a second width different from the first width to the even gate lines GL**2**, GL**4**, . . . , GLn.

[0054] The image display **112** displays an image by controlling light transmittance of the pixels according to gate pulses supplied to the gate lines GL and data voltages supplied to the column pixels Po and Pe.

[0055] Each of the TCPs **134** is electrically connected to the printed circuit board **120** and to the liquid crystal panel **110** using tape automated bonding (TAB). Input pads of each TCP **134** are electrically connected to the printed circuit board **120**, and output pads are electrically connected to the liquid crystal panel **110**.

[0056] The timing controller **122** adequately arranges source data provided from an external driving system for driving the liquid crystal panel **110** and supplies the arranged source data to the data integrated circuits **140** according to vertical and horizontal synchronous signals, and a data enable signal provided from the external driving system.

[0057] The timing controller **122** controls driving timing of the data integrated circuits **140** using the vertical and horizontal synchronous signals and the data enable signal provided from the driving system. To this end, the timing controller **122** generates data control signals including a source start pulse (SSP), source shift clock (SSC), a polarity control signal (POL), and a source output enable signal (SOE), and supplies the generated data control signals to the data integrated circuits **140**. The timing controller **122** generates a polarity control signal such that the polarity pattern of an image supplied to the image display **112** can be reversed for every horizontal line, namely, can be line-inverted.

[0058] Using the vertical and horizontal synchronous signals and the data enable signal provided from the driving system, the timing controller **122** generates gate control signals including a gate start pulse (GSP) for controlling driving timing of the first and second gate driver circuits **150** and **160**, a plurality of gate shift clocks (GSC), and a gate output enable (GOE) signal, and supplies the generated gate control signals to the first and second gate driver circuits **150** and **160**.

[0059] The timing controller **122** generates a plurality of gate shift clocks (GSC) in accordance with the number of the gate shift clocks used to drive shift registers constituting the first and second gate driver circuits **150** and **160**. In this description, it is assumed that each of the first and second gate driver circuits **150** and **160** uses two gate shift clocks to generate gate pulses.

[0060] Hence, using the vertical and horizontal synchronous signals and the data enable signal, the timing controller **122** generates first and third gate shift clocks CLK**1** and CLK**3** having a first width W**1** and second and fourth gate shift clocks CLK**2** and CLK**4** having a second width W**2**, as shown in **FIG. 4**. The first width W**1** is set to be wider than the second width W**2**. Preferably, the ratio of the first width W**1** to the second width W**2** is set to be at least about 4:3 and/or at most about 2:1. In one example, the ratio is about 10:7.

[0061] Especially, the timing controller **122** generates the first and third gate shift clocks CLK**1** and CLK**3** having the first width W**1** and the second and fourth gate shift clocks CLK**2** and CLK**4** having the second width W**2** by using a data enable signal and first and second masking signals different from each other. That is, the timing controller **122** generates a reference clock by dividing the data enable signal into two, and counting the divided data enable signal. Then, the timing controller **122** controls the falling time of the reference clock according to the generated reference

clock and the first masking signal, thereby generating the first and third gate shift clocks CLK1 and CLK3 having the first width W1. Also, the timing controller **122** controls the falling time of the reference clock according to the reference clock and the second masking signal, thereby generating the second and fourth gate shift clocks CLK2 and CLK4 having the second width.

[0062] The timing controller **122** delays the phases of the first to fourth gate shift clocks CLK1 to CLK4 in sequence so as to overlap for a half horizontal period, and supplies the phase-delayed gate shift clocks CLK1 to CLK4 to the first and second gate driver circuits **150** and **160**. The first and third gate shift clocks CLK1 and CLK3 having the first width W1 are supplied to the first gate driver circuit **150**. The second and fourth gate shift clocks CLK2 and CLK4 having the second width W2 are supplied to the second gate driver circuit **160**.

[0063] Each of the data integrated circuits **140** converts a data signal from the timing controller **122** to analog data voltage and supplies the analog data voltage to the associated data line DL of the liquid crystal panel **110** through the output pads of the associated TCP **134**, according to data control signals inputted through the input pads of the TCP **134**. Each of the data integrated circuits **140** generates data voltage having a positive (+) or negative (−) polarity according to the polarity control signal (POL), and supplies the data voltage to the associated data line DL according to a source output enable signal (SOE) from the timing controller **122**.

[0064] The first gate driver circuit **150** is formed at one side of the liquid crystal panel **110** and electrically connected with the odd gate lines GL1, GL3, . . . , GLn−1 of the image display **112**. The first gate driver circuit **150** is driven by the gate start pulse GSP from the timing controller **122**, generates gate pulses having the first width W1 which are sequentially phase-delayed by one horizontal period according to the first and third gate shift clocks CLK1 and CLK3 from the timing controller **122**, and sequentially supplies the gate pulses having the first width W1 to the odd gate lines GL1, GL3, . . . , GLn−1 according to the gate output enable signal GOE.

[0065] The second gate driver circuit **160** is formed at the other side of the liquid crystal panel **110** and electrically connected with the even gate lines GL2, GL4, . . . , GLn of the image display **112**. The second gate driver circuit **160** is driven by the gate start pulse GSP from the timing controller **122**, generates gate pulses having the second width W2 which are sequentially phase-delayed by one horizontal period according to the second and fourth gate shift clocks CLK2 and CLK4 from the timing controller **122**, sequentially supplies the gate pulses having the second width W2 to the even gate lines GL2, GL4, . . . , GLn according to the gate output enable signal GOE.

[0066] Consequently, the first and second gate driver circuits **150** and **160** sequentially supply, to the gate lines GL of the image display **112**, the gate pulses each overlapping with one another for the half horizontal period.

[0067] **FIG. 5** is a waveform diagram illustrating a driving method for the liquid crystal display device according to an embodiment of the present invention.

[0068] Firstly, the polarity of the data voltage is reversed for every horizontal line (1 horizontal period). Gate pulses, overlapped with one another for the half horizontal period, having the first width W1 and the second width W2 are sequentially supplied to the odd gate lines GL1, GL3, . . . , GLn−1 and the even gate lines GL2, GL4, . . . , GLn, respectively.

[0069] In every horizontal period, each pixel **116** is precharged with data voltage during a first period, for which the gate pulse supplied to the associated gate line GL overlaps with that of the previous gate line GL, and is charged with data voltage during the remaining second period. The data voltage charge time in odd-column pixels Po by the gate pulses having the first width W1 is longer than the data voltage charge time in even-column pixels Pe by the gate pulses having the second width W2.

[0070] Hereinafter, the driving method for the liquid crystal display device according to the first embodiment of the present invention is explained with reference to **FIGS. 3 and 5**.

[0071] Firstly, during a period before a first horizontal period, it is assumed that each of the odd pixels **116** connected to a first gate line GL1 is precharged with a data voltage having a negative (−) polarity by a gate pulse having the first width W1 provided from the first gate driver circuit **150** so as to overlap with a gate pulse having the second width W2 provided to an nth gate line GLn.

[0072] Next, during the first horizontal period, the second gate driver circuit **160** supplies a gate pulse having the second width W2 to a second gate line GL2 such that the gate pulse is overlapped with the gate pulse having the first width W1 supplied by the first gate driver circuit **150** to the first gate line GL1.

[0073] Hence, during a first period of the first horizontal period, for which the gate pulse having the first width W1 supplied to the first gate line GL1 and the gate pulse having the second width W2 supplied to the second gate line GL2 overlap, each odd pixel **116** connected to the first gate line GL1 precharged with a data voltage having a negative (−) polarity is charged with data voltage having a positive (+) polarity for odd pixels from the associated data line DL by a gate pulse having the first width W1. In the same period, each even pixel **116** connected to the second gate line GL2 is precharged with a positive (+) polarity data voltage for odd pixels supplied from the associated data line DL by the gate pulse having the second width W2.

[0074] Next, the first gate driver circuit **150** supplies a gate pulse having the first width W1 to a third gate line GL3 such that the gate pulse is overlapped with the gate pulse having the second width W2 supplied by the second gate driver circuit **160** to the second gate line GL2. Hence, during a second period of the first horizontal period, for which the gate pulse having the second width W2 supplied to the second gate line GL2 and the gate pulse having the first width W1 supplied to the third gate line GL3 overlap, each even pixel **116** connected to the second gate line GL2 and precharged with a data voltage having a positive (+) polarity is charged with an even data voltage having a positive (+) polarity supplied from the associated data line DL by a gate pulse having the second width W2. Each odd pixel **116** connected to the third gate line GL3 is precharged with a positive (+) polarity data voltage for even pixels supplied from the associated data line DL by the gate pulse having the first width W1.

[0075] Consequently, during the first horizontal period, the associated odd and even pixels **116** respectively connected to the left and right of each data line DL, are charged with the positive-polarity data voltages. The time that the even pixel **116** precharged with the positive-polarity data voltage is charged with the positive-polarity data voltage is shorter than the time that the odd pixel **116** precharged with the negative-polarity data voltage by the gate pulse having the second width W**2** charged with the positive-polarity data voltage.

[0076] Next, during the second horizontal period, the second gate driver circuit **160** supplies a gate pulse having the second width W**2** to the fourth gate line GL**4** such that the gate pulse is overlapped with the gate pulse having the first width W**1** supplied by the first gate driver circuit **150** to the third gate line GL**3**.

[0077] Hence, during a first period of the second horizontal period, for which the gate pulse having the first width W**1** supplied to the third gate line GL**3** and the gate pulse having the second width W**2** supplied to the fourth gate line GL**4** overlap, each odd pixel **116** connected to the third gate line GL**3** and precharged with a data voltage having a positive polarity is charged with an odd data voltage having a negative polarity supplied from the associated data line DL by a gate pulse having the first width W**1**. Each of the even pixels **116** connected to the fourth gate line GL**4** is precharged with a negative polarity data voltage for odd pixels supplied from the associated data line DL by the gate pulse having the second width W**2**.

[0078] Next, the first gate driver circuit **150** supplies a gate pulse having the first width W**1** to the fifth gate line GL**5** such that the gate pulse is overlapped with the gate pulse having the second width W**2** supplied by the second gate driver circuit **160** to the fourth gate line GL**4**. Hence, during a second period of the second horizontal period, for which the gate pulse having the second width W**2** supplied to the fourth gate line GL**4** and the gate pulse having the first width W**1** supplied to the fifth gate line GL**5** overlap, each of the even pixels **116** connected to the fourth gate line GL**4** and precharged with a data voltage having a negative polarity is charged with an even data voltage having a negative polarity from the associated data line DL by a gate pulse having the second width W**2**. Each of the odd pixels **116** connected to the fifth gate line GL**5** is precharged with a negative polarity data voltage for even pixels supplied from the associated data line DL by the gate pulse having the first width W**1**.

[0079] Consequently, during the second horizontal period, the associated odd and even pixels **116** respectively connected to the left and the right of each data line DL are charged with the negative-polarity data voltage. The time that the even pixel **116** precharged with the negative-polarity data voltage is charged with the negative-polarity data voltage is shorter than the time that the odd pixel **116** precharged with the positive-polarity data voltage by the gate pulse having the second width W**2** is charged with the negative-polarity data voltage.

[0080] In the same way as the first and the second horizontal periods, during a third to Nth horizontal periods, the gate pulse having the first width W**1** and the gate pulse having the second width W**2** are supplied to the odd gate lines GL**1**, GL**3**, . . . , GLn−1 and the even gate lines GL**2**, GL**4**, GLn, respectively, such that the two gate pulses overlap for ½ of the horizontal period, and positive and negative polarity data voltages are supplied to the data lines.

[0081] In the apparatus and method for driving a liquid crystal display device according to the present invention, vertical dimming caused by a brightness difference between odd-column pixels Po and even-column pixels Pe can be minimized. One gate pulse having a first width is supplied to the odd-column pixels Po and another gate pulse having a second width is supplied to the even-column pixels Pe, making the charge time of the odd-column pixels Po different from that of the even-column pixels Pe.

[0082] Specifically, while the polarity of the precharged data voltages is opposite to the polarity of the charged data voltages in the odd-column pixels Po, the polarity of the precharged data voltages is equal to the polarity of the charged data voltages in the even-column pixels Pe. Namely, the odd-column pixels Po are either charged with the positive-polarity data voltages after being precharged with the negative-polarity voltage or are charged with the negative-polarity data voltages after being precharged with the positive-polarity voltage. To the contrary, the even-column pixels Pe are either charged with the negative-polarity data voltages after being precharged with the negative-polarity voltage or are charged with the positive-polarity data voltages after being precharged with the positive-polarity voltage.

[0083] According to the present invention, the odd-column pixels Po are charged with data voltage using a gate pulse having a first width W**1**, and the even-column pixels Pe are charged with data voltage using a gate pulse having a second width W**2** narrower than the first width W**1**. Namely, in the odd-column pixels Po, the polarity of the precharged data voltages is opposite to the polarity of the charged data voltages, hence, effective data voltage charge time is increased using the first width W**1**. In the even-column pixels Pe, the polarity of the precharged data voltages is equal to the polarity of the charged data voltages, hence, effective data voltage charge time is reduced using the second width W**2**.

[0084] In the apparatus and method for driving a liquid crystal display device according to the first embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **112**, can be minimized by supplying gate pulses having different widths W**1** and W**2** to the odd-column pixels Po and the even-column pixels Pe, respectively.

[0085] **FIG. 6** illustrates an apparatus for driving a liquid crystal display device according to the second embodiment of the present invention.

[0086] Referring to **FIG. 6**, the apparatus for driving a liquid crystal display device comprises a liquid crystal panel **210**. The liquid crystal panel **210** comprises an image display **212** including a plurality of data lines DL and 'n' gate lines GL. The image display **212** also includes odd-column pixels Po each of which is connected to a first side of one of the data lines DL and connected to one of the odd gate lines GL**1**, GL**3**, . . . , GLn−1, and even-column pixels Pe each of which is connected to a second side of one of the data lines and connected to one of the even gate lines GL**2**, GL**4**, . . . , GLn. The driving apparatus also comprises a gate driver for providing first and second gate pulses having

different voltages to the odd gate lines GL**1**, GL**3**, . . . , GLn−1 and the even gate lines GL**2**, GL**4**, . . . , GLn, respectively, and a plurality of data integrated circuits **240** for providing data voltages having a positive or negative polarity to the data lines DL, respectively. The driving apparatus further comprises a timing controller **222** for performing supply and control of data signals to provide the data voltages to the data lines DL, and for controlling the gate driver.

[**0087**] The apparatus for driving a liquid crystal display according to the second embodiment of the present invention further comprises a printed circuit board **220**, on which a power circuit (not shown) is mounted together with the timing controller **222**, and a plurality of tape carrier packages (hereinafter, referred to as "TCPs") **234**, which are connected between the printed circuit board **220** and the liquid crystal panel **210**. The data integrated circuits **240** are mounted in the TCPs **234**, respectively.

[**0088**] The gate driver of the liquid crystal display driving apparatus according to the second embodiment of the present invention includes a first gate driver circuit **250** for providing gate pulses having a first voltage to the odd gate lines GL**1**, GL**3**, . . . , GLn−1, and a second gate driver circuit **260** for providing gate pulses having a second voltage different from the first voltage to the even gate lines GL**2**, GL**4**, . . . , GLn.

[**0089**] The image display **212** displays an image by controlling light transmittance of the pixels according to gate pulses supplied to the gate lines GL and data voltages supplied to the column pixels Po and Pe.

[**0090**] Each of the TCPs **234** is electrically connected to the printed circuit board **220** and to the liquid crystal panel **110** using tape automated bonding (TAB). Input pads of each TCP **234** are electrically connected to the printed circuit board **220**, and output pads are electrically connected to the liquid crystal panel **210**.

[**0091**] The timing controller **222** arranges source data provided from an external driving system for driving the liquid crystal panel **210** and supplies the arranged source data to the data integrated circuits **240** according to vertical and horizontal synchronous signals, and a data enable signal provided from the external driving system.

[**0092**] The timing controller **222** controls driving timing of the data integrated circuits **240** using the vertical and horizontal synchronous signals and the data enable signal provided from the driving system. To this end, the timing controller **222** generates data control signals including a source start pulse (SSP), source shift clock (SSC), a polarity control signal (POL), and a source output enable signal (SOE), and supplies the generated data control signals to the data integrated circuits **240**. The timing controller **222** generates a polarity control signal such that the polarity pattern of an image supplied to the image display **212** can be reversed for every horizontal line, namely, can be line-inverted.

[**0093**] Using the vertical and horizontal synchronous signals and the data enable signal provided from the driving system, the timing controller **222** generates gate control signals including a gate start pulse (GSP) for controlling driving timing of the first and second gate driver circuits **250** and **260**, a plurality of gate shift clocks (GSC), and a gate output enable (GOE) signal, and supplies the generated gate control signals to the first and second gate driver circuits **250** and **260**.

[**0094**] The timing controller **222** generates a plurality of gate shift clocks (GSC) in accordance with the number of the gate shift clocks used to drive shift registers constituting the first and second gate driver circuits **250** and **260**. In this description, it is assumed that each of the first and second gate driver circuits **250** and **260** uses two gate shift clocks to generate gate pulses.

[**0095**] Hence, using the vertical and horizontal synchronous signals and the data enable signal, the timing controller **222** generates first and third gate shift clocks CLK**1** and CLK**3** having a first voltage V**1** and second and fourth gate shift clocks CLK**2** and CLK**4** having a second voltage V**2**, as shown in **FIG. 7**. The first voltage V**1** is set to be higher than the second voltage V**2**.

[**0096**] The timing controller **222** delays the phases of the first to fourth gate shift clocks CLK**1** to CLK**4** having the first and second voltages V**1** and V**2** in sequence so as to overlap for a half horizontal period, and supplies the phase-delayed gate shift clocks CLK**1** to CLK**4** to the first and second gate driver circuits **250** and **260**. The first and third gate shift clocks CLK**1** and CLK**3** having the first voltage V**1** are supplied to the first gate driver circuit **250**. The second and fourth gate shift clocks CLK**2** and CLK**4** having the second voltage V**2** are supplied to the second gate driver circuit **260**.

[**0097**] Each of the data integrated circuits **240** converts a data signal from the timing controller **222** to analog data voltage and supplies the analog data voltage to the associated data line DL of the liquid crystal panel **110** through the output pads of the associated TCP **234**, according to data control signals inputted through the input pads of the TCP **234**. Each of the data integrated circuits **240** generates data voltage having a positive (+) or negative (−) polarity according to the polarity control signal (POL), and supplies the data voltage to the associated data line DL according to source output enable signal (SOE) from the timing controller **222**.

[**0098**] As shown in **FIG. 8**, the first gate driver circuit **250** is provided with first and third gate shift clock CLK**1** and CLK**3** input lines, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and 'm' stages (m, positive number of n/2) connected with the respective input lines for supplying the gate pulse of the first voltage V**1** to the odd gate lines (GL**1**, GL**3**, . . . , GLn−1). The first gate driver circuit **250** is directly formed on the liquid crystal panel **210**.

[**0099**] As shown in **FIG. 7**, the first and third gate shift clocks CLK**1** and CLK**3** having the first voltage V**1** are sequentially phase-delayed by one horizontal period from the timing controller **222**, and are sequentially supplied to the first and third gate shift clock CLK**1** and CLK**3** input lines.

[**0100**] Except the first stage **2521**, each stage **2521** to **252***m* supplies the clock signal CLK**1** and CLK**3** of the first voltage V**1** provided from one of the first and third gate shift clock input lines to the corresponding odd gate line GL**1**, GL**3**, . . . , GLn−1 according to the output signal of the previous stage **2522** to **252***m*. The first stage **2521** supplies

the first gate shift clock CLK1 of the first voltage V1 provided from the input line of the first gate shift clock CLK1 to the first gate line GL1 according to the gate start pulse GSP from the timing controller **222**.

[0101] The first gate drive circuit **250** is driven by the gate start pulse GSP from the timing controller **222**, generates the gate pulses having the first voltage V1 which are sequentially phase-delayed by one horizontal period according to the first and third gate shift clocks CLK1 and CLK3 from the timing controller **222**, sequentially supplies the gate pulses having the first voltage V1 to the odd gate lines GL1, GL3, . . . , GLn−1 according to the gate output enable signal GOE.

[0102] The second gate driver circuit **260** is provided with second and fourth gate shift clock CLK2 and CLK4 input lines, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and 'm' stages (m, positive number of n/2) connected with the respective input lines for supplying the gate pulse of the second voltage V2 to the even gate lines (GL2, GL4, . . . , GLn). The second gate driver circuit **260** is directly formed on the liquid crystal panel **210**.

[0103] As shown in **FIG. 7**, the second and fourth gate shift clocks CLK2 and CLK4 having the second voltage V2 are sequentially phase-delayed by one horizontal period from the timing controller **222**, and are sequentially supplied to one end of the second and fourth gate shift clock CLK2 and CLK4 input lines.

[0104] Except the first stage **2621**, each stage **2621** to **262***m* supplies the clock signal CLK2 and CLK4 of the second voltage V2 provided from one of the second and fourth gate shift clock input lines to the corresponding even gate line GL2, GL4, . . . , GLn according to the output signal of the previous stage **2622** to **262***m*. The first stage **2621** supplies the second gate shift clock CLK2 of the second voltage V2 provided from the input line of the second gate shift clock CLK2 to the second gate line GL2 according to the gate start pulse GSP from the timing controller **222**.

[0105] The second gate drive circuit **260** is driven by the gate start pulse GSP from the timing controller **222**, generates the gate pulses having the second voltage V2 which are sequentially phase-delayed by one horizontal period according to the second and fourth gate shift clocks CLK2 and CLK4 from the timing controller **222**, sequentially supplies the gate pulses having the second voltage V2 to the even gate lines GL2, GL4, . . . , GLn according to the gate output enable signal GOE.

[0106] Consequently, the first and second gate driver circuits **250** and **260** sequentially supply, to the gate lines GL of the image display **212**, the gate pulses each overlapping with one another for the half horizontal period.

[0107] **FIG. 9** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the second embodiment of the present invention.

[0108] Firstly, the polarity of the data voltage is reversed for every horizontal line (1 horizontal period). Gate pulses, overlapped with one another for the half horizontal period, having the first voltage V1 and the second voltage V2 are sequentially supplied to the odd gate lines GL1, GL3, . . . , GLn−1 and the even gate lines GL2, GL4, GLn, respectively.

[0109] In every horizontal period, each pixel **216** is precharged with data voltage during a first period, for which the gate pulse supplied to the associated gate line GL overlaps with that of the previous gate line GL, and is charged with data voltage during the remaining second period. The data voltage charge time in odd-column pixels Po by the gate pulses having the first voltage V1 is substantially equal to that of the data voltage charge time in even-column pixels Pe by the gate pulses having the second voltage V2.

[0110] Hereinafter, the driving method for the liquid crystal display device according to the second embodiment of the present invention is explained with reference to **FIG. 6**.

[0111] Firstly, during a period before a first horizontal period, it is assumed that each of the odd pixels **216** connected to a first gate line GL1 is precharged with a data voltage having a negative (−) polarity by a gate pulse having the first voltage V1 provided from the first gate driver circuit **250** so as to overlap with a gate pulse having the second voltage V2 provided to an nth gate line GLn.

[0112] Next, during the first horizontal period, the second gate driver circuit **260** supplies a gate pulse having the second voltage V2 to a second gate line GL2 such that the gate pulse is overlapped with the gate pulse having the first voltage V1 supplied by the first gate driver circuit **250** to the first gate line GL1.

[0113] Hence, during a first period of the first horizontal period, for which the gate pulse having the first voltage V1 supplied to the first gate line GL1 and the gate pulse having the second voltage V2 supplied to the second gate line GL2 overlap, each odd pixel **216** connected to the first gate line GL1 precharged with a data voltage having a negative (−) polarity is charged with data voltage having a positive (+) polarity for odd pixels from the associated data line DL by a gate pulse having the first voltage V1. In the same period, each even pixel **216** connected to the second gate line GL2 is precharged with a positive (+) polarity data voltage for odd pixels supplied from the associated data line DL by the gate pulse having the second voltage V2.

[0114] Next, the first gate driver circuit **250** supplies a gate pulse having the first voltage V1 to a third gate line GL3 such that the gate pulse is overlapped with the gate pulse having the second voltage V2 supplied by the second gate driver circuit **260** to the second gate line GL2. Hence, during a second period of the first horizontal period, for which the gate pulse having the second voltage V2 supplied to the second gate line GL2 and the gate pulse having the first voltage V1 supplied to the third gate line GL3 overlap, each even pixel **216** connected to the second gate line GL2 and precharged with a data voltage having a positive (+) polarity is charged with an even data voltage having a positive (+) polarity supplied from the associated data line DL by a gate pulse having the second voltage V2. Each odd pixel **216** connected to the third gate line GL3 is precharged with a positive (+) polarity data voltage for even pixels supplied from the associated data line DL by the gate pulse having the first voltage V1.

[0115] Consequently, during the first horizontal period, the associated odd and even pixels **216** respectively connected to the left and right of each data line DL, are charged with the positive-polarity data voltages. The time that the even pixel **216** precharged with the positive-polarity data voltage

is charged with the positive-polarity data voltage is substantially equal to the time that the odd pixel **216** precharged with the negative-polarity data voltage by the gate pulse having the second voltage V**2** is charged with the positive-polarity data voltage.

[**0116**] Next, during the second horizontal period, the second gate driver circuit **260** supplies a gate pulse having the second voltage V**2** to the fourth gate line GL**4** such that the gate pulse is overlapped with the gate pulse having the first voltage V**1** supplied by the first gate driver circuit **250** to the third gate line GL**3**.

[**0117**] Hence, during a first period of the second horizontal period, for which the gate pulse having the first voltage V**1** supplied to the third gate line GL**3** and the gate pulse having the second voltage V**2** supplied to the fourth gate line GL**4** overlap, each odd pixel **216** connected to the third gate line GL**3** and precharged with a data voltage having a positive polarity is charged with an odd data voltage having a negative polarity supplied from the associated data line DL by a gate pulse having the first voltage V**1**. Each of the even pixels **216** connected to the fourth gate line GL**4** is precharged with a negative polarity data voltage for odd pixels supplied from the associated data line DL by the gate pulse having the second voltage V**2**.

[**0118**] Next, the first gate driver circuit **250** supplies a gate pulse having the first voltage V**1** to the fifth gate line GL**5** such that the gate pulse is overlapped with the gate pulse having the second voltage V**2** supplied by the second gate driver circuit **260** to the fourth gate line GL**4**. Hence, during a second period of the second horizontal period, for which the gate pulse having the second voltage V**2** supplied to the fourth gate line GL**4** and the gate pulse having the first voltage V**1** supplied to the fifth gate line GL**5** overlap, each of the even pixels **216** connected to the fourth gate line GL**4** and precharged with a data voltage having a negative polarity is charged with an even data voltage having a negative polarity from the associated data line DL by a gate pulse having the second voltage V**2**. Each of the odd pixels **216** connected to the fifth gate line GL**5** is precharged with a negative polarity data voltage for even pixels supplied from the associated data line DL by the gate pulse having the first voltage V**1**.

[**0119**] Consequently, during the second horizontal period, the associated odd and even pixels **216** respectively connected to the left and the right of each data line DL are charged with the negative-polarity data voltage. The time that the even pixel **216** precharged with the negative-polarity data voltage is charged with the negative-polarity data voltage is substantially equal to the time that the odd pixel **116** precharged with the positive-polarity data voltage by the gate pulse having the second voltage V**2** is charged with the negative-polarity data voltage. Thus, the even pixel **216** is both charged and precharged by the gate pulse having the second voltage V**2** while the odd pixel **216** is both charged and precharged by the gate pulse having the first voltage V**1**.

[**0120**] In the same way as the first and the second horizontal periods, during a third to Nth horizontal periods, the gate pulse having the first voltage V**1** and the gate pulse having the second voltage V**2** are supplied to the odd gate lines GL**1**, GL**3**, . . . , GLn−1 and the even gate lines GL**2**, GL**4**, . . . , GLn, respectively, such that the two gate pulses overlap for ½ of the horizontal period, and positive and negative polarity data voltages are supplied to the data lines.

[**0121**] In the apparatus and method for driving a liquid crystal display device according to the present invention, vertical dimming caused by a brightness difference between odd-column pixels Po and even-column pixels Pe can be minimized. One gate pulse having a first voltage is supplied to the odd-column pixels Po and another gate pulse having a second voltage is supplied to the even-column pixels Pe, thus substantially equalizing the amount of charge in the odd-column pixels Po and in the even-column pixels Pe.

[**0122**] Specifically, while the polarity of the precharged data voltages is opposite to the polarity of the charged data voltages in the odd-column pixels Po, the polarity of the precharged data voltages is equal to the polarity of the charged data voltages in the even-column pixels Pe. Namely, the odd-column pixels Po are either charged with the positive-polarity data voltages after being precharged with the negative-polarity voltages or are charged with the negative-polarity data voltages after being precharged with the positive-polarity voltages. The even-column pixels Pe, on the other hand, are either charged with the negative-polarity data voltages after being precharged with the negative-polarity voltages or are charged with the positive-polarity data voltages after being precharged with the positive-polarity voltages.

[**0123**] According to the present invention, the odd-column pixels Po are charged with data voltage using a gate pulse having a first voltage V**1**, and the even-column pixels Pe are charged with data voltage using a gate pulse having a second voltage V**2** smaller than the first voltage V**1**.

[**0124**] In the apparatus and method for driving a liquid crystal display device according to the second embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **212**, can be minimized by supplying gate pulses having different voltages V**1** and V**2** to the odd-column pixels Po and the even-column pixels Pe, respectively.

[**0125**] **FIG. 10** illustrates an apparatus for driving a liquid crystal display device according to the third embodiment of the present invention. **FIG. 11** illustrates first and second gate driver circuits of **FIG. 10**.

[**0126**] Referring to **FIG. 10** and **FIG. 11**, the apparatus for driving the liquid crystal display device comprises a liquid crystal panel **210**. The liquid crystal panel **210** comprises an image display **212** including 'm' data lines DL and 'n' gate lines GL. The image display **212** also includes odd-column pixels Po each of which is connected to a first side of one of the data lines DL and connected to one of the odd gate lines GL**1**, GL**3**, . . . , GLn−1, and even-column pixels Pe each of which is connected to a second side of one of the data lines and, connected to one of the even gate lines GL**2**, GL**4**, GLn. The driving apparatus also comprises a gate driver for providing gate pulses of first and second voltages having different voltage values to the odd-column pixels Po and the even-column pixels Pe, and a plurality of data integrated circuits **240** for providing data voltages having a positive or negative polarity to the data lines DL, respectively. The driving apparatus further comprises a timing controller **222** for performing supply and control of data signals to provide the data voltages to the data lines DL, and for controlling the gate driver.

[**0127**] Except the structure of the gate driver, the apparatus for driving the liquid crystal display device according to

the third embodiment of the present invention is same in structure as the apparatus for driving the liquid crystal display device according to the second embodiment of the present invention. Thus, the gate driver in the apparatus for driving the liquid crystal display device according to the third embodiment of the present invention will be mainly explained as follows.

[0128] In the apparatus for driving the liquid crystal display device according to the third embodiment of the present invention, the gate driver is provided with a first gate driver circuit **250** and a second gate driver circuit **260**. The first gate driver circuit **250** provides the gate pulse of the first voltage V**1** to the '4i+1' ('i' corresponds to the positive number of 0 to 4/n) gate line (GL**1**, GL**5** . . .), and provides the gate pulse of the second voltage V**2** to the '4i+4' gate line (GL**4**, GL**8** . . .). Also, the second gate driver circuit **260** provides the gate pulse of the first voltage V**1** to the '4i+2' gate line (GL**2**, GL**6** . . .), and provides the gate pulse of the second voltage V**2** to the '4i+3' gate line (GL**3**, GL**7** . . .).

[0129] The first gate driver circuit **250** is directly formed at one side of the liquid crystal panel **210**, and is electrically connected with the '4i+1' and '4i+4' gate lines (GL**1**, GL**4**, GL**5**, GL**8**). The first gate driver circuit **250** is driven by the gate start pulse GSP from the timing controller **222**, generates the gate pulses having the first and second voltages which are sequentially phase-delayed by one horizontal period according to the first and fourth gate shift clocks CLK**1** and CLK**4** from the timing controller **222**, and sequentially supplies the gate pulses having the first and second voltages to the '4i+1' and '4i+4' gate lines (GL**1**, GL**4**, GL**5**, GL**8**) according to the gate output enable signal GOE.

[0130] The second gate driver circuit **260** is directly formed at the other side of the liquid crystal panel **110**, and is electrically connected with the '4i+2' and '4i+3' gate lines (GL**2**, GL**3**, GL**6**, GL**7**) The second gate driver circuit **260** is driven by the gate start pulse GSP from the timing controller **222**, generates the gate pulses having the first and second voltages which are sequentially phase-delayed by one horizontal period according to the second and third gate shift clocks CLK**2** and CLK**3** from the timing controller **222**, and sequentially supplies the gate pulses having the first and second voltages to the '4i+2' and '4i+3' gate lines (GL**2**, GL**3**, GL**6**, GL**7**) according to the gate output enable signal GOE.

[0131] In the apparatus and method for driving the liquid crystal display device according to the third embodiment of the present invention, vertical dimming, which are generated by the difference of luminance between the odd-column pixels Po and the even-column pixels Pe, can be minimized by supplying the gate pulses having the different voltages to the odd-column pixels Po and the even-column pixels Pe, respectively.

[0132] **FIG. 12** illustrates first and second gate driver circuits **250** and **260** in an apparatus for driving a liquid crystal display device according to the fourth embodiment of the present invention.

[0133] On explaining **FIG. 12** in connection with **FIG. 6**, the first gate driver circuit **250** includes first and third gate shift clock CLK**1** and CLK**3** input lines, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and 'm' stages (m, positive number of n/2) connected with the respective input lines for supplying the gate pulse of the first voltage V**1** to the odd gate lines (GL**1**, GL**3**, . . . , GLn−1). The first gate driver circuit **250** is directly formed on the liquid crystal panel **210**.

[0134] The first and third gate shift clocks CLK**1** and CLK**3** having the first voltage V**1** are sequentially phase-delayed by one horizontal period from the timing controller **222**, and are sequentially supplied to the first and third gate shift clock CLK**1** and CLK**3** input lines.

[0135] Except the first stage **2521**, each stage **2521** to **252***m* supplies the clock signal CLK**1** and CLK**3** of the first voltage V**1** provided from any one of the first and third gate shift clock input lines to the corresponding odd gate line GL**1**, GL**3**, . . . , GLn−1 according to the output signal of the previous stage **2522** to **252***m*. At this time, the first stage **2521** supplies the first gate shift clock CLK**1** of the first voltage V**1** provided from the input line of the first gate shift clock CLK**1** to the first gate line GL**1** according to the gate start pulse GSP from the timing controller **222**.

[0136] The first gate driver circuit **250** sequentially supplies the gate pulses having the first voltage to the odd gate lines (GL**1**, GL**3**, . . . , GLn−1), wherein the gate pulses having the first voltage are sequentially phase-delayed by one horizontal period according to the first and third gate shift clocks CLK**1** and CLK**3**.

[0137] The second gate driver circuit **260** is provided with second and fourth gate shift clock CLK**2** and CLK**4** input lines, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and a voltage converter **264** connected between the second and fourth gate shift clock input lines and the base voltage input line to convert the second and fourth gate shift clocks CLK**2** and CLK**4** of the first voltage V**1** to the second voltage V**2**, and 'm' stages (m, positive number of n/2) connected with the respective input lines for supplying the gate pulse of the second voltage V**2** to the even gate lines (GL**2**, GL**4**, . . . , GLn). The second gate driver circuit **260** is directly formed on the liquid crystal panel **210**.

[0138] The second and fourth gate shift clocks CLK**2** and CLK**4** having the second voltage V**2** are sequentially phase-delayed by one horizontal period from the timing controller **222**, and are sequentially supplied to one end of the second and fourth gate shift clock CLK**2** and CLK**4** input lines.

[0139] The voltage converter **264** is comprised of a first variable resistor VR**1** and a second variable resistor VR**2**. The first variable resistor VR**1** is connected between the other end of the second gate shift clock input line and the base voltage input line. Also, the second variable resistor VR**2** is connected between the other end of the fourth gate shift clock input line and the base voltage input line. The first variable resistor VR**1** converts the second gate shift clock CLK**2** having the first voltage inputted to the second gate shift clock input line to the second voltage V**2**, which is lower than the first voltage V**1**. Also, the second variable resistor VR**2** converts the fourth gate shift clock CLK**4** having the first voltage inputted to the fourth gate shift clock input line to the second voltage V**2**.

[0140] Except the first stage **2621**, each stage **2621** to **262***m* supplies the clock signal CLK**2** and CLK**4** of the second voltage V**2** provided from one of the second and

fourth gate shift clock input lines to the corresponding even gate line GL**2**, GL**4**, . . . , GLn according to the output signal of the previous stage **2622** to **262***m*. The first stage **2621** supplies the second gate shift clock CLK**2** of the second voltage V**2** provided from the input line of the second gate shift clock CLK**2** to the second gate line GL**2** according to the gate start pulse GSP from the timing controller **222**.

[**0141**] The second gate driver circuit **260** sequentially supplies the gate pulses having the second voltage V**2**, which are phase-delayed by one horizontal period according to the second and fourth gate shift clocks CLK**2** and CLK**4** having the second voltage V**2** converted by the voltage converter **264**, to the even gate lines (GL**2**, GL**4**, . . . , GLn).

[**0142**] **FIG. 13** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the fourth embodiment of the present invention, which illustrates a drive waveform outputted from the timing controller and a gate pulse supplied to the gate line.

[**0143**] On explaining **FIG. 14** in connection with **FIG. 6** and **FIG. 12**, first, in the apparatus for driving the liquid crystal display device according to the fourth embodiment of the present invention, the timing controller **222** outputs gate and data control signals of the same waveform as shown in **FIG. 9** except it outputs the first to fourth gate shift clocks CLK**1** to CLK**4** of the first voltage V**1**. That is, the timing controller **222** supplies the first to fourth gate shift clocks CLK**1** to CLK**4** having the first voltage V**1**, which are sequentially phase-delayed for being overlapped by ½ horizontal period according to vertical and horizontal synchronous signals, to the first and second gate driver circuits **250** and **260**. The first and third gate shift clocks CLK**1** and CLK**3** are provided to the first gate driver circuit **250**, and the second and fourth gate shift clocks CLK**2** and CLK**4** are provided to the second gate driver circuit **260**.

[**0144**] In the apparatus and method for driving the liquid crystal display device according to the fourth embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **212**, can be minimized by supplying the gate pulses having different voltages V**1** and V**2** to the odd-column pixels Po and the even-column pixels Pe, respectively, with the voltage converter **264** provided in the second gate driver circuit **260**.

[**0145**] **FIG. 14** illustrates first and second gate driver circuits **250** and **260** in an apparatus for driving a liquid crystal display device according to the fifth embodiment of the present invention.

[**0146**] Referring to **FIG. 14**, in the apparatus for driving the liquid crystal display device according to the fifth embodiment of the present invention, the timing controller **222** outputs gate and data control signals of the same waveform as shown in **FIG. 9** except it outputs the first to fourth gate shift clocks CLK**1** to CLK**4** of the first voltage V**1**.

[**0147**] The first gate driver circuit **250** includes first and fourth gate shift clock CLK**1** and CLK**4** input lines of the first voltage V**1**, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, a first voltage converter **255** connected between the fourth gate shift clock input line and the base voltage input line to convert the fourth gate shift clock CLK**4** of the first voltage to the second voltage V**2**, and 'm' stages (m, positive number of n/2) **2521** to **252***m* connected with the respective input lines for supplying the gate pulse of the first voltage V**1** to the '4i+i' ('i' corresponds to the positive number of 0 to 4/n) gate line (GL**1**, GL**5** . . .), and for supplying the gate pulse of the second voltage to the '4i+4' gate line (GL**4**, GL**8** . . .).

[**0148**] The first and fourth gate shift clocks CLK**1** and CLK**4** having the first voltage V**1** are sequentially phase-delayed by one horizontal period from the timing controller **222**, and are sequentially supplied to one end of the first and fourth gate shift clock CLK**1** and CLK**4** input lines.

[**0149**] The first voltage converter **255** includes a first variable resistor VR**1**, wherein the first variable resistor VR**1** is connected between the other end of the fourth gate shift clock input line and the base voltage input line. The first variable resistor VR**1** converts the fourth gate shift clock CLK**4** having the first voltage inputted to the fourth gate shift clock input line to the second voltage V**2**, which is lower than the first voltage V**1**.

[**0150**] Except the first stage **2521**, each stage **2521** to **252***m* supplies the clock signal CLK**1** and CLK**4** of the first or second voltage V**1** or V**2** provided from one of the first and fourth gate shift clock input lines to the corresponding gate line GL**1**, GL**4**, . . . , GLn according to the output signal of the previous stage **2522** to **252***m*.

[**0151**] That is, the odd stage (**2521**, **2523**, . . . , **252***m*−1) sequentially supplies the first gate shift clock CLK**1** of the first voltage V**1** provided from the first gate shift clock input line to the '4i+1' gate line (GL**1**, GL**5** . . .) according to the gate start pulse GSP of the timing controller **222**. The first stage **2521** supplies the first gate shift clock CLK**1** of the first voltage V**1** provided from the first gate shift clock CLK**1** input line to the first gate line GL**1** according to the gate start pulse GSP from the timing controller **222**.

[**0152**] The even stage (**2522**, **2524**, . . . , **252***m*) sequentially supplies the fourth gate shift clock CLK**4** of the second voltage V**2** from the fourth gate shift clock input line, which is voltage-dropped by the first voltage converter **255**, to the '4i+4' gate line (GL**4**, GL**8**, . . .).

[**0153**] The second gate driver circuit **260** includes second and third gate shift clock CLK**2** and CLK**3** input lines of the first voltage V**1**, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and a second voltage converter **266** connected between the second gate shift clock input line and the base voltage input line to convert the second gate shift clock CLK**4** of the first voltage to the second voltage V**2**, and 'm' stages (m, positive number of n/2) **2621** to **262***m* connected with the respective input lines for supplying the gate pulse of the second voltage V**2** to the '4i+2' gate line (GL**2**, GL**6** . . .), and for supplying the gate pulse of the first voltage to the '4i+3' gate line (GL**3**, GL**7** . . .).

[**0154**] The second and third gate shift clocks CLK**2** and CLK**3** having the first voltage V**1** are sequentially phase-delayed by one horizontal period from the timing controller **222**, and are sequentially supplied to one end of the second and third gate shift clock CLK**2** and CLK**3** input lines.

[**0155**] The second voltage converter **266** includes a second variable resistor VR**2**, wherein the first variable resistor VR**2** is connected between the other end of the second gate

shift clock input line and the base voltage input line. The second variable resistor VR**2** converts the fourth gate shift clock CLK**2** having the first voltage inputted to the second gate shift clock input line to the second voltage V**2**, which is lower than the first voltage V**1**.

[**0156**] Except the first stage **2621**, each stage **2621** to **262***m* supplies the clock signal CLK**2** and CLK**3** of the first or second voltage V**1** or V**2** provided from one of the second and third gate shift clock input lines to the corresponding gate line GL**2**, GL**3**, . . . , GLn−1 according to the output signal of the previous stage **2622** to **262***m*.

[**0157**] That is, the odd stage (**2621**, **2623**, . . . , **262***m*−1) sequentially supplies the second gate shift clock CLK**2** of the second voltage V**2** provided from the second gate shift clock input line to the '4i+2' gate line (GL**2**, GL**6** . . .) according to the gate start pulse GSP of the timing controller **222**. The first stage **2621** supplies the second gate shift clock CLK**2** of the second voltage V**2** provided from the second gate shift clock CLK**2** input line to the second gate line GL**2** according to the gate start pulse GSP from the timing controller **222**.

[**0158**] The even stage (**2622**, **2624**, . . . , **262***m*) sequentially supplies the third gate shift clock CLK**3** of the first voltage V**1** from the third gate shift clock input line of the timing controller **222** to the '4i+3' gate line (GL**3**, GL**7**, . . .).

[**0159**] In the apparatus and method for driving a liquid crystal display device according to the fifth embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **212**, can be minimized by supplying the gate pulses having the different voltages V**1** and V**2** to the odd-column pixels Po and the even-column pixels Pe, respectively, with the voltage converters **255** and **266** provided in the first and second gate driver circuits **250** and **260**.

[**0160**] In another apparatus for driving a liquid crystal display device according to the preferred embodiment of the present invention, a gate driver may be provided with a first gate driver circuit **250** and a second gate driver circuit **260**, wherein the first gate driver circuit **250** generates gate pulses of a first voltage V**1** and/or a second voltage V**2** according to two gate shift clocks (CLK**1**, CLK**2**) (CLK**1**, CLK**3**) (CLK**1**, CLK**4**) (CLK**2**, CLK**3**) (CLK**3**, CLK**4**) among first to fourth gate shift clocks CLK**1** to CLK**4**, and the second gate driver circuit **260** generates gate pulses of a first voltage V**1** and/or a second voltage V**2** according to two gate shift clocks (CLK**3**, CLK**4**) (CLK**2**, CLK**4**) (CLK**2**, CLK**3**) (CLK**1**, CLK**4**) (CLK**1**, CLK**2**) among first to fourth gate shift clocks CLK**1** to CLK**4**. Thus, the gate driver according to another embodiment of the present invention supplies the gate pulses of the different voltages V**1** and V**2** to the odd-column pixels Po and the even-column pixels P**3**

[**0161**] **FIG. 15** illustrates an apparatus for driving a liquid crystal display device according to the sixth embodiment of the present invention.

[**0162**] Referring to **FIG. 15**, the apparatus for driving a liquid crystal display device comprises a liquid crystal panel **210**. The liquid crystal panel **210** comprises an image display **212** including a plurality of data lines DL and a plurality of gate lines GL. The image display **212** also includes odd-column pixels Po each of which is connected to a first side of one of the data lines DL and connected to one of the odd gate lines GL**1**, GL**3**, . . . , GLn−1, and even-column pixels Pe each of which is connected to a second side of one of the data lines and connected to one of the even gate lines GL**2**, GL**4**, . . . , GLn. The driving apparatus also comprises a gate driver for providing first and second gate pulses having different widths and voltages to the odd gate lines GL**1**, GL**3**, . . . , GLn−1 and the even gate lines GL**2**, GL**4**, . . . , GLn, respectively, and a plurality of data integrated circuits **240** for providing data voltages having a positive or negative polarity to the data lines DL, respectively. The driving apparatus further comprises a timing controller **322** for performing supply and control of data signals to provide the data voltages to the data lines DL, and for controlling the gate driver.

[**0163**] Except the timing controller **322** and the gate driver, the driving apparatus according to the sixth embodiment of the present invention is identical in structure with the driving apparatus according to the second embodiment of the present invention. Thus, in the driving apparatus according to the sixth embodiment of the present invention, the other parts except the timing controller and the gate driver will be explained with reference to **FIG. 6**.

[**0164**] Using the vertical and horizontal synchronous signals and the data enable signal, the timing controller **322** generates first and third gate shift clocks CLK**1** and CLK**3** having a first pulse width W**1** and a first voltage V**1**, and second and fourth gate shift clocks CLK**2** and CLK**4** having a second pulse width W**2** and a second voltage V**2**, as shown in **FIG. 17**. The first width W**1** is set to be wider than the second width W**2**, and the voltage V**1** is set to be higher than the second voltage V**2**.

[**0165**] As shown in **FIG. 15**, the gate driver further includes first and second gate driver circuits **250** and **260** for providing the first and second gate pulses having the different widths (W**1** and W**2**) and voltages (V**1** and V**2**) to the odd-column pixels Po and the even-column pixels Pe.

[**0166**] The first gate driver circuit **250** sequentially supplies the gate pulses having the first width W**1** and the first voltage V**1** to the gate lines (GL**1**, GL**3**, GL**5**, . . .) connected with the odd-column pixels Po according to the first and third gate shift clocks CLK**1** and CLK**3** having the first width W**1** and the first voltage V**1**.

[**0167**] The first gate driver circuit **250** includes first and third gate shift clock (CLK**1** and CLK**3**) input lines of the first width W**1** and the first voltage V**1**, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and 'm' stages (m, positive number of n/2) **2521** to **252***m* connected with the respective input lines for supplying the gate pulses of the first width W**1** and the first voltage V**1** to the odd gate lines (GL**1**, GL**3**, . . . , GLn−1). The first gate driver circuit **250** is directly formed on the liquid crystal panel **210**.

[**0168**] The second gate driver circuit **260** sequentially supplies the gate pulses having the second width W**2** and the second voltage V**2** to the gate lines (GL**2**, GL**4**, GL**6**, . . .) connected with the even-column pixels Pe according to the second and fourth gate shift clocks CLK**2** and CLK**4** having the second width W**2** and the second voltage V**2**.

[**0169**] The second gate driver circuit **260** includes second and fourth gate shift clock (CLK**2** and CLK**4**) input lines of

the second width W2 and the second voltage V2, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and 'm' stages (m, positive number of n/2) **2621** to **262***m* connected with the respective input lines for supplying the gate pulses of the second width W2 and the second voltage V2 to the even gate lines (GL2, GL4, . . . , GLn). The second gate driver circuit **260** is directly formed on the liquid crystal panel **210**.

[0170] **FIG. 17** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the sixth embodiment of the present invention.

[0171] On explaining **FIG. 17** in connection with **FIG. 15** and **FIG. 16**, the driving apparatus and method according to the sixth embodiment of the present invention are identical to the driving apparatus and method according to the second embodiment of the present invention except that the gate pulses having the different widths (W1 and W2) and voltages (V1 and V2) are respectively provided to the odd-column pixels Po and even-column pixels Pe.

[0172] In the apparatus and method for driving the liquid crystal display device according to the sixth embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **212**, can be minimized by supplying the gate pulses having different widths (W1 and W2) and voltages (V1 and V2) to the odd-column pixels Po and the even-column pixels Pe, respectively, with the first and third gate shift clocks (CLK1 and CLK3) of the first width W1 and the first voltage V1 and the second and fourth gate shift clocks (CLK2 and CLK4) of the second width W2 and the second voltage V2.

[0173] In an apparatus for driving a liquid crystal display device according to the seventh embodiment of the present invention, as shown in **FIG. 18**, a timing controller **322** generates first and third gate shift clocks CLK1 and CLK3 having a first width W1 and a first voltage V1, and second and fourth gate shift clocks CLK2 and CLK4 having a second width W2 and a first voltage V1. Then, the first to fourth gate shift clocks CLK1 to CLK4 generated in the timing controller **322** are provided to a gate driver. The first width W1 is set to be wider than the second width W2.

[0174] In the driving apparatus according to the seventh embodiment of the present invention, the gate driver includes first and second gate driver circuits **250** and **260** for providing the gate pulses having the different widths (W1 and W2) and voltages (V1 and V2) to the odd-column pixels Po and even-column pixels Pe.

[0175] The first gate driver circuit **250** sequentially supplies the gate pulses having the first width W1 and the first voltage V1 to the gate lines (GL1, GL3, GL5, . . .) connected with the odd-column pixels Po according to the first and third gate shift clocks CLK1 and CLK3 having the first width W1 and the first voltage V1.

[0176] The first gate driver circuit **250** includes first and third gate shift clock (CLK1 and CLK3) input lines of the first width W1 and the first voltage V1, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, and 'm' stages (m, positive number of n/2) **2521** to **252***m* connected with the respective input lines for supplying the gate pulses of the first width W1 and the first voltage V1 to the odd gate lines (GL1, GL3, . . . , GLn−1). The first gate driver circuit **250** is directly formed on the liquid crystal panel **210**.

[0177] The second gate driver circuit **260** converts the second and fourth gate shift clocks CLK2 and CLK4 from the second width W2 and the first voltage V1 to the second width W2 and the second voltage V2. Then, the gate pulses of the second width W2 and the second voltage V2 are sequentially provided to the gate lines (GL2, GL4, GL6, . . .) connected with the even-column pixels Pe.

[0178] The second gate driver circuit **260** includes the second and fourth gate shift clock (CLK2 and CLK4) input lines of the first width W1 and the first voltage V1, driving voltage Vdd and base voltage Vss input lines, a gate start pulse GSP input line, a voltage converter **264** connected between each of the second and fourth gate shift clock (CLK2 and CLK4) input lines and the base voltage (Vss) input line for converting the second and fourth gate shift clocks (CLK2 and CLK4) from the first width W1 and the first voltage V1 to the first width W1 and the second voltage V2, and 'm' stages (m, positive number of n/2) **2621** to **262***m* connected with the respective input lines for supplying the gate pulses of the first width W1 and the second voltage V2 to the even gate lines (GL2, GL4, . . . , GLn). The second gate driver circuit **260** is directly formed on the liquid crystal panel **210**.

[0179] In the apparatus and method for driving the liquid crystal display device according to the seventh embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **212**, can be minimized by supplying the gate pulses having the different widths (W1 and W2) and voltages (V1 and V2) to the odd-column pixels Po and the even-column pixels Pe, respectively, with the first and third gate shift clocks (CLK1 and CLK3) of the first width W1 and the first voltage V1 and the second and fourth gate shift clocks (CLK2 and CLK4) of the second width W2 and the first voltage V1.

[0180] **FIG. 19** is a waveform diagram illustrating a driving method for the liquid crystal display device according to the seventh embodiment of the present invention.

[0181] On explaining **FIG. 19** in connection with **FIG. 12** and **FIG. 18**, the driving apparatus and method according to the seventh embodiment of the present invention are identical to the driving apparatus and method according to the sixth embodiment in that the gate pulses having the different widths (W1 and W2) and voltages (V1 and V2) are provided to the odd-column pixels Po and even-column pixels Pe.

[0182] In the driving apparatus and method according to the seventh embodiment of the present invention, vertical dimming, which arises during line inversion driving of the image display **212**, can be minimized by supplying the gate pulses having the different widths (W1 and W2) and voltages (V1 and V2) to the odd-column pixels Po and even-column pixels Pe, respectively, with the first and third gate shift clocks CLK1 and CLK3 of the first width W1 and the first voltage V1 and the second and fourth gate shift clocks CLK2 and CLK4 of the second width W2 and the first voltage V1.

[0183] In the meantime, in case of the driving apparatus according to the seventh embodiment of the present invention, it is possible to provide the gate driver having the structure of **FIG. 14**.

[0184] In the driving apparatus according to the sixth and seventh embodiments of the present invention, the gate

driver provides the different gate pulses to the odd-column pixels Po and the even-column pixels Pe with at least two gate shift clocks according to the connection structure between each pixel **216** and gate line.

[**0185**] In the apparatus and method for driving the liquid crystal display device, vertical dimming can be minimized to enhance picture quality. During line inversion driving, gate pulses having different widths and/or voltages are applied to the odd-column pixels and the even-column pixels with respect to each data line. The odd-column pixels and the even-column pixels are precharged with voltages having different polarities. Gate pulses having different widths and/or voltages make the effective charge times of the odd-column pixels and the even-column pixels different, minimizing vertical dimming. As indicated, any combination of altering the width and voltage of the gate pulse during the precharging period and charging period may be used to reduce the disparity between the charging of the odd-column pixels and the even-column pixels.

[**0186**] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An apparatus for driving a liquid crystal display device, comprising:

a liquid crystal panel comprising an image display including a plurality of data lines, a plurality of gate lines, a plurality of pixels having odd-column pixels each of which is connected to a first side of one of the data lines and connected to an associated odd gate line, and even-column pixels each of which is connected to a second side of one of the data lines and connected to an associated even gate lines;

a gate driver that provides different gate pulses to the odd-column pixels than to the even-column pixels;

a plurality of data drivers that provide data voltages having a positive or negative polarity to the data lines; and

a timing controller that controls the gate driver and the data driver.

2. The apparatus of claim 1, wherein the gate driver provides gate pulses having different voltages to the odd-column pixels than to the even-column pixels.

3. The apparatus of claim 1, wherein the gate driver provides gate pulses of different widths to the odd-column pixels and the even-column pixels.

4. The apparatus as set forth in claim 3, wherein the timing controller repeatedly generates first and third gate shift clocks having a first width and a first phase delay for one horizontal period, repeatedly generates second and fourth gate shift clocks having a second width different from the first width and a second phase delay for one horizontal period, and supplies the first to fourth gate shift clocks to the gate driver.

5. The apparatus as set forth in claim 4, wherein the gate driver comprises:

a first gate driver circuit that provides gate pulses, which have the first width, to the gate lines connected to the odd-column pixels using the first and the third gate shift clocks; and

a second gate driver circuit that provides gate pulses, which have the second width, to the gate lines connected to the even-column pixels using the second and the fourth gate shift clocks.

6. The apparatus as set forth in claim 5, wherein the first width of the gate pulses provided to the odd-column pixels is wider than the second width of the gate pulses provided to the even-column pixels.

7. The apparatus as set forth in claim 5, wherein the ratio of the first width to the second width is about 10:7.

8. The apparatus as set forth in claim 5, wherein the gate pulses provided to the odd-column pixels and the even-column pixels overlap each other.

9. The apparatus as set forth in claim 2, wherein the timing controller repeatedly generates first and second gate shift clocks of a first voltage and a first phase delay for one horizontal period, repeatedly generates third and fourth gate shift clocks of a second voltage different from the first voltage and a second phase delay for one horizontal period, and supplies the first to fourth clocks to the gate driver.

10. The apparatus as set forth in claim 9, wherein the gate driver comprises:

a first gate driver circuit that provides gate pulses, which have the first voltage, to the gate lines connected to the odd-column pixels using the first and the second gate shift clocks; and

a second gate driver circuit that provides gate pulses, which have the second voltage, to the gate lines connected to the even-column pixels using the third and the fourth gate shift clocks.

11. The apparatus as set forth in claim 9, wherein the gate driver comprises:

a first gate driver circuit that provides gate pulses of the first voltage to the '4i+1' ('i' corresponds to the positive number of 0 to 4/n) gate line, and provides gate pulses of the second voltage to the '4i+4' gate line using one of the first and second gate shift clocks and one of the third and fourth gate shift clocks; and

a second gate driver circuit that provides gate pulses of the first voltage to the '4i+2' gate line, and provides gate pulses of the second voltage to the '4i+3' gate line using the other of the first and second gate shift clocks and the other of the third and fourth gate shift clocks.

12. The apparatus as set forth in claim 2, wherein the timing controller repeatedly generates first to fourth gate shift clocks having a first voltage and a phase delay for ½ of a horizontal period, and supplies the first to fourth clocks to the gate driver.

13. The apparatus as set forth in claim 12, wherein the gate driver comprises:

a first gate driver circuit that provides gate pulses of the first voltage to gate lines connected with the odd-column pixels using the first and third gate shift clocks; and

a second gate driver circuit that provides gate pulses of a second voltage to gate lines connected with the even-column pixels by converting the second and fourth gate

shift clocks of the first voltage to the second voltage which is different from the first voltage.

14. The apparatus as set forth in claim 13, wherein the second gate driver circuit includes a voltage converter that converts the first voltage of the second and fourth gate shift clocks to the second voltage.

15. The apparatus as set forth in claim 14, wherein the voltage converter includes first and second resistors connected between second and fourth gate shift clock input lines and a base voltage input line.

16. The apparatus as set forth in claim 13, wherein the gate driver comprises:

a first gate driver circuit that converts one of the first and second gate shift clocks having the first voltage to the second voltage, supplies gate pulses of the first voltage to the '4i+1' gate line ('i' corresponds to the positive number of 0 to 4/n) using one of the first and second gate shift clocks converted to the second voltage and one of the third and fourth gate shift clocks having the first voltage, and supplies gate pulses of the second voltage to the '4i+4' gate line; and

a second gate driver circuit that converts one of the third and fourth gate shift clocks having the first voltage to the second voltage, supplies gate pulses of the first voltage to the '4i+2' gate line using the other of the third and fourth gate shift clocks converted to the second voltage and the other of the first and second gate shift clocks having the first voltage, and supplies gate pulses of the second voltage to the '4i+3' gate line.

17. The apparatus as set forth in claim 16, wherein the first gate driver circuit includes a first voltage converter that converts one of the first and second gate shift clocks having the first voltage to the second voltage.

18. The apparatus as set forth in claim 17, wherein the first voltage converter includes a first resistor connected between one of first and second gate shift clock input lines having the first voltage and a base voltage input line.

19. The apparatus as set forth in claim 16, wherein the second gate driver circuit includes a second voltage converter that converts one of the third and fourth gate shift clocks having the first voltage to the second voltage.

20. The apparatus as set forth in claim 19, wherein the second voltage converter includes a second resistor connected between one of the third and fourth gate shift clock input lines having the first voltage to a base voltage input line.

21. The apparatus as set forth in claim 10, wherein the first voltage is higher than the second voltage.

22. The apparatus as set forth in claim 11, wherein the first voltage is higher than the second voltage.

23. The apparatus as set forth in claim 13, wherein the first voltage is higher than the second voltage.

24. The apparatus as set forth in claim 16, wherein the first voltage is higher than the second voltage.

25. The apparatus as set forth in claim 10, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

26. The apparatus as set forth in claim 11, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

27. The apparatus as set forth in claim 13, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

28. The apparatus as set forth in claim 16, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

29. The apparatus as set forth in claim 9, wherein the first and second gate shift clocks have a first width and the third and fourth gate shift clocks have a second width different from the first width.

30. The apparatus as set forth in claim 9, wherein the first to fourth gate shift clocks have the same width.

31. The apparatus as set forth in claim 12, wherein the first and third gate shift clocks have a first width and the second and fourth gate shift clocks have a second width different from the first width.

32. The apparatus as set forth in claim 12, wherein the first to fourth gate shift clocks have the same width.

33. The apparatus as set forth in claim 1, wherein the data driver reverses the polarity of the data voltages for every horizontal period.

34. The apparatus as set forth in claim 1, wherein the gate driver is formed on the liquid crystal panel.

35. A method for driving a liquid crystal display device which comprises an image display including a plurality of data lines, a plurality of gate lines, a plurality of pixels having odd-column pixels each of which is connected to a first side of one of the data lines and connected to an associated odd one of the gate lines, and even-column pixels each of which is connected to a second side of one of the data lines and connected to an associated even one of the gate lines, the method comprising:

providing different gate pulses to the odd-column pixels than to the even-column pixels; and

providing data voltages having a positive or negative polarity to each of the data lines in synchronization with the gate pulses.

36. The method of claim 35, wherein gate pulses provided to the odd-column pixels have different voltages from gate pulses provided to the even-column pixels.

37. The method of claim 35, wherein gate pulses provided to the odd-column pixels have different widths from gate pulses provided to the even-column pixels.

38. The method as set forth in claim 37, further comprising:

repeatedly generating first and third gate shift clocks having a first width and a first phase delay for one horizontal period; and

repeatedly generating second and fourth gate shift clocks having a second width different from the first width and a second phase delay for one horizontal period.

39. The method as set forth in claim 38, wherein supplying the gate pulses having the different widths comprises:

supplying the gate pulses, which have the first width, to the gate lines connected to the odd-column pixels using the first and the third gate shift clocks; and

supplying the gate pulses, which have the second width, to the gate lines connected to the even-column pixels using the second and the fourth gate shift clocks.

40. The method as set forth in claim 39, wherein the first width of the gate pulses provided to the odd-column pixels is wider than the second width of the gate pulses provided to the even-column pixels.

41. The method as set forth in claim 40, wherein the ratio of the first width to the second width is about 10:7.

42. The method as set forth in claim 39, wherein the gate pulses of the first width overlap the gate pulses of the second width.

43. The method as set forth in claim 36, further comprising:

repeatedly generating first and third gate shift clocks having a first voltage and a first phase delay for one horizontal period; and

repeatedly generating second and fourth gate shift clocks having a second voltage different from the first voltage and a second phase delay for one horizontal period.

44. The method as set forth in claim 43, wherein providing the gate pulses having the different voltages comprises:

supplying the gate pulses, which have the first voltage, to the gate lines connected to the odd-column pixels using the first and the third gate shift clocks; and

supplying the gate pulses, which have the second voltage, to the gate lines connected to the even-column pixels using the second and the fourth gate shift clocks.

45. The method as set forth in claim 43, wherein providing the gate pulses having the different voltages comprises:

providing gate pulses of the first voltage to the '4i+1' ('i' corresponds to the positive number of 0 to 4/n) gate line, and providing the gate pulse of the second voltage to the '4i+4' gate line using one of the first and second gate shift clocks and one of the third and fourth gate shift clocks; and

providing gate pulses of the first voltage to the '4i+2' gate line, and providing gate pulses of the second voltage to the '4i+3' gate line by using the other one of the first and second gate shift clocks and the other of the third and fourth gate shift clocks.

46. The method as set forth in claim 36, further comprising repeatedly generating first to fourth gate shift clocks having a first voltage and a phase delay for about ½ of a horizontal period.

47. The method as set forth in claim 46, wherein providing the gate pulses having the different voltages comprises:

converting the second and fourth gate shift clocks having the first voltage to the second voltage which different from the first voltage;

providing gate pulses of the first voltage to the gate line connected with the odd-column pixels using the first and third gate shift clocks; and

providing gate pulses of the second voltage to the gate line connected with the even-column pixels using the second and fourth gate shift clocks.

48. The method as set forth in claim 46, wherein providing the gate pulses having the different voltages comprises:

converting one of the first and second gate shift clocks having the first voltage to the second voltage;

converting the other of the third and fourth gate shift clocks having the first voltage to the second voltage;

providing gate pulses of the first voltage to the '4i+1' gate line ('i' corresponds to the positive number of 0 to 4/n) using one of the first and second gate shift clocks and one of the third and fourth gate shift clocks, and providing gate pulses of the second voltage to the '4i+4' gate line; and

providing gate pulses of the first voltage to the '4i+2' gate line using the other of the third and fourth gate shift clocks and the other of the first and second gate shift clocks, and providing gate pulses of the second voltage to the '4i+3' gate line.

49. The method as set forth in claim 44, wherein the first voltage is higher than the second voltage.

50. The method as set forth in claim 45, wherein the first voltage is higher than the second voltage.

51. The method as set forth in claim 47, wherein the first voltage is higher than the second voltage.

52. The method as set forth in claim 48, wherein the first voltage is higher than the second voltage.

53. The method as set forth in claim 44, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

54. The method as set forth in claim 45, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

55. The method as set forth in claim 47, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

56. The method as set forth in claim 48, wherein the gate pulse of the first voltage is overlapped with the gate pulse of the second voltage for about ½ of one horizontal period.

57. The method as set forth in claim 35, wherein the polarity of the data voltage is reversed for every horizontal period.

58. The method as set forth in claim 43, wherein the first and third gate shift clocks have a first width and the second and fourth gate shift clocks have a second width different from the first width.

59. The method as set forth in claim 43, wherein the first to fourth gate shift clocks have the same width.

60. The method as set forth in claim 46, wherein the first and third gate shift clocks have a first width and the second and fourth gate shift clocks have a second width different from the first width.

61. The method as set forth in claim 46, wherein the first to fourth gate shift clocks have the same width.

62. A method for driving a display device having pixels, the method comprising:

precharging a first set of pixels with a first precharge voltage of a first polarity using first gate pulses and a second set of pixels with a second precharge voltage of a second polarity using second gate pulses; and

charging the first and second set of pixels with a data voltage of a second polarity using the first and second gate pulses, respectively, the first and second gate pulses having at least one of different widths or voltages.

63. The method as set forth in claim 62, wherein the first set of pixels are odd-column pixels and the second set of pixels are even-column pixels.

64. The method as set forth in claim 62, wherein the first and second gate pulses have different widths.

65. The method as set forth in claim 64, wherein the first and second gate pulses have different voltages.

66. The method as set forth in claim 65, further comprising generating the first and second gate pulses using first and second gate clock signals having different widths and different voltages.

67. The method as set forth in claim 65, further comprising generating the first and second gate pulses using first and second gate clock signals having the same voltage but different widths.

68. The method as set forth in claim 64, wherein the first and second gate pulses have the same voltage.

69. The method as set forth in claim 62, wherein the first and second gate pulses have different voltages.

70. The method as set forth in claim 69, wherein the first and second gate pulses have the same width.

71. The method as set forth in claim 70, further comprising generating the first and second gate pulses using first and second gate clock signals having the same width but different voltages.

72. The method as set forth in claim 70, further comprising generating the first and second gate pulses using first and second gate clock signals having the same voltage and width.

73. The method as set forth in claim 62, further comprising maintaining a constant voltage for the first and second gate pulses and for the width of the first and second gate pulses, respectively.

74. The method as set forth in claim 62, further comprising supplying the first gate pulses to the first set of pixels using a first gate driver and the second gate pulses to the second set of pixels using a second gate driver, the first gate driver supplying gate pulses other than the second gate pulses and the second gate driver supplying pulses other than the first gate pulses.

75. The method as set forth in claim 74, further comprising converting the first gate pulses into the second gate pulses using a resistor connected between input lines carrying the first gate pulses and base voltage input lines.

76. The method as set forth in claim 62, further comprising supplying the first gate pulses to the first set of pixels using a first gate driver and a second gate driver and supplying the second gate pulses to the second set of pixels using the first and second gate drivers.

77. The method as set forth in claim 76, further comprising converting the first gate pulses into the second gate pulses using a resistor connected between input lines carrying the first gate pulses and base voltage input lines.

78. The method as set forth in claim 62, further comprising providing data voltages having different polarities to the first and second set of pixels at different times such that each row of pixels has the same polarity and adjacent rows of pixels have different polarities.

79. The method as set forth in claim 62, further comprising reversing the polarity of the data voltages applied to the first set of pixels and the second set of pixels every horizontal period.

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专利名称(译)	用于驱动液晶显示装置的装置和方法		
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摘要(译)

公开了一种用于驱动液晶显示装置的设备和方法。该装置包括具有由数据和栅极线限定的像素的液晶面板。栅极驱动器向奇数列像素提供与偶数列像素不同的栅极脉冲。栅极脉冲具有不同的电压和/或宽度。数据驱动器为数据线提供具有正极性或负极性的数据电压。时序控制器控制栅极和数据驱动器，并向栅极驱动器提供具有不同电压和/或宽度的栅极时钟脉冲。