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**Song**

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(54) **LIQUID CRYSTAL DISPLAY AND THIN FILM TRANSISTOR ARRAY PANEL THEREFOR**

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(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon-Si (KR)

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 87 days.

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(22) Filed: **Aug. 4, 2009**

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**Related U.S. Application Data**

(63) Continuation of application No. 10/806,379, filed on Mar. 23, 2004, now Pat. No. 7,580,102.

(30) **Foreign Application Priority Data**

Mar. 24, 2003 (KR) ..... 2003-0018195

(51) **Int. Cl.**  
**G02F 1/1343** (2006.01)

(52) **U.S. Cl.** ..... **349/139; 349/142; 349/143; 349/144; 349/145; 349/146; 349/147; 349/129; 349/130**

(58) **Field of Classification Search** ..... None  
See application file for complete search history.

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(57) **ABSTRACT**

A gate line extending in a transverse direction and a data line intersecting the gate line are formed on the substrate. The data line includes a curved portion and an intermediate portion crossing the gate line substantially at a right angle. A pixel electrode is formed on an insulating layer. The pixel electrode is connected to a thin film transistor and it has an edge extending substantially parallel to the curved portion of the data line.

**20 Claims, 21 Drawing Sheets**

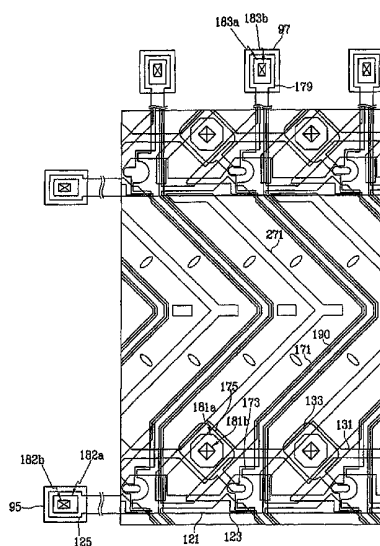




FIG. 1

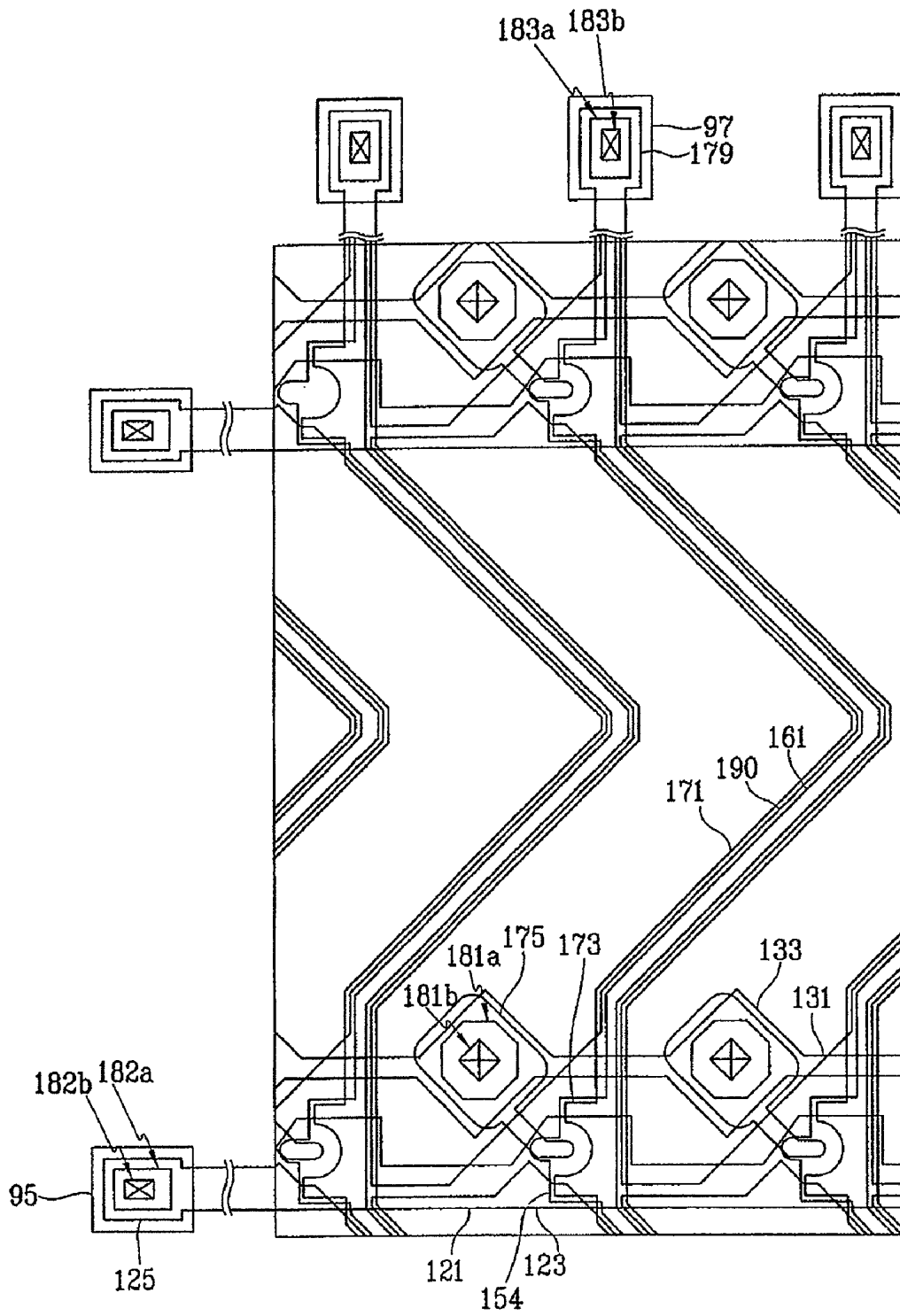


FIG.2

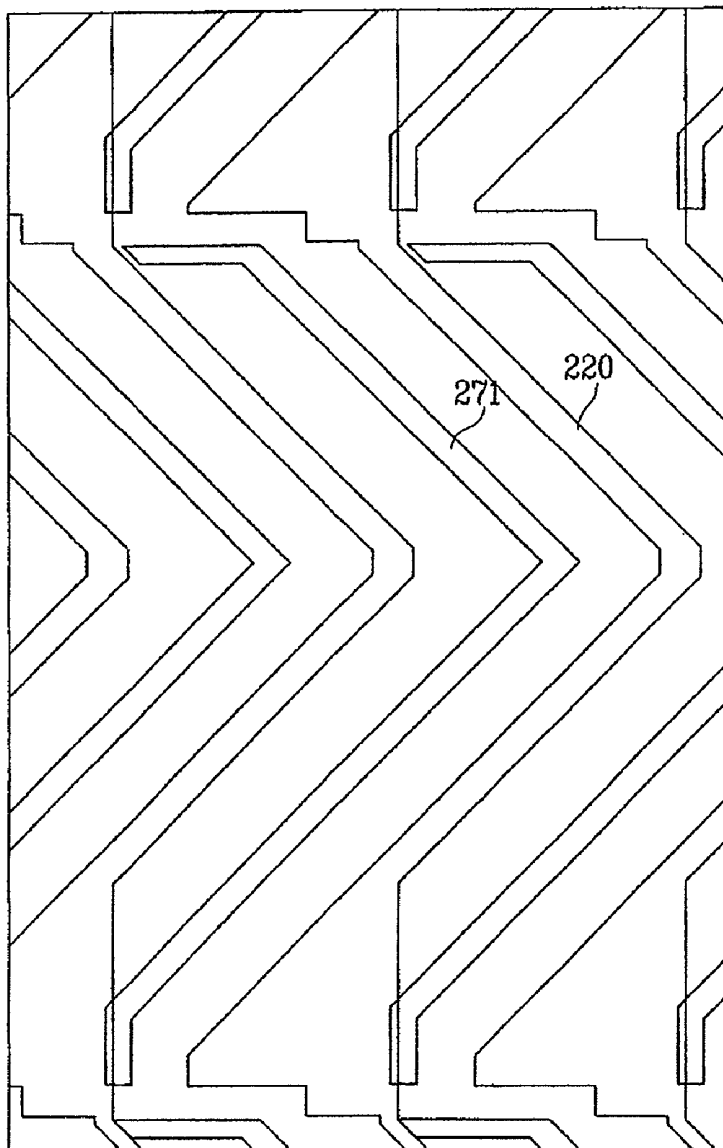


FIG.3

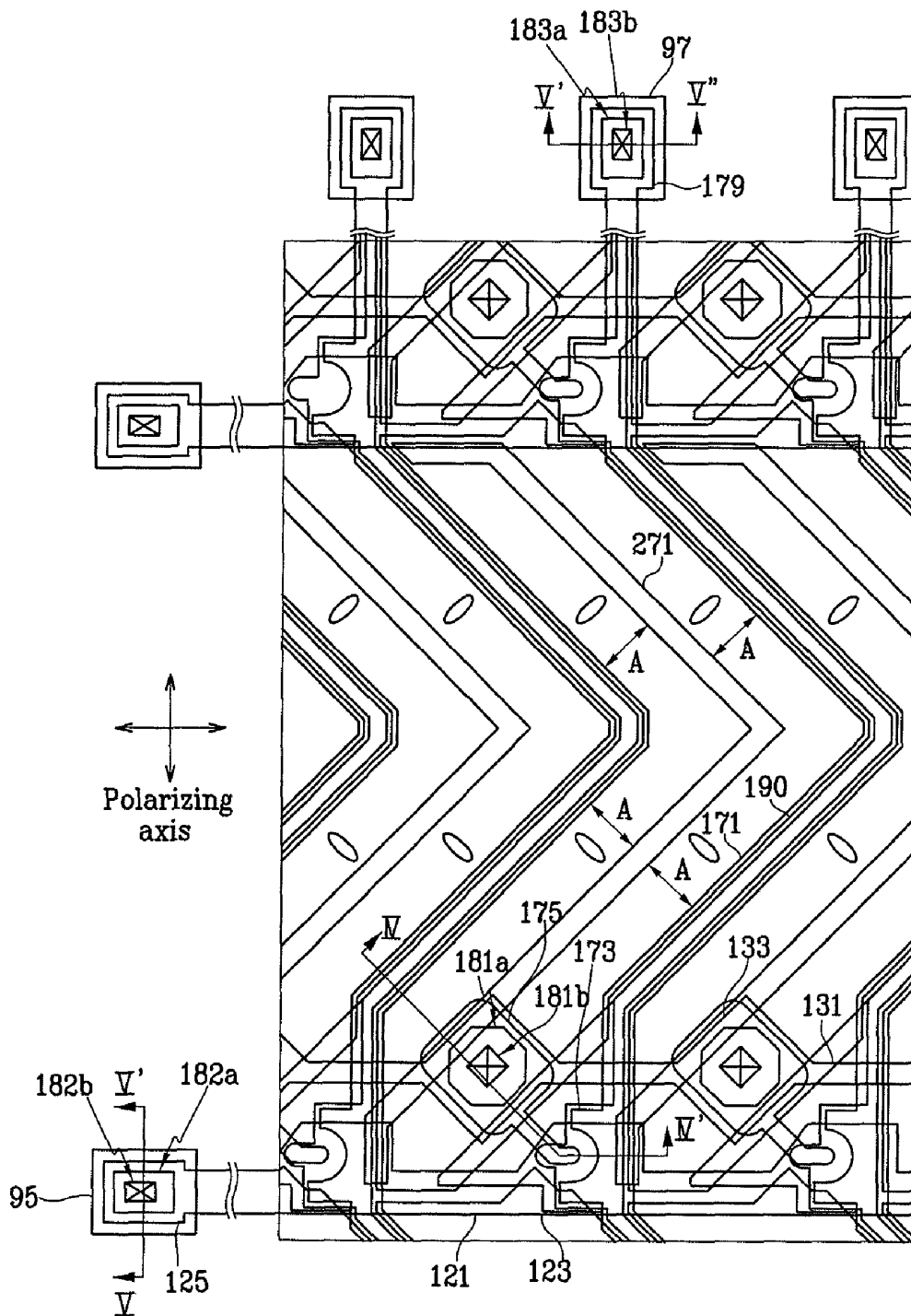


FIG. 4

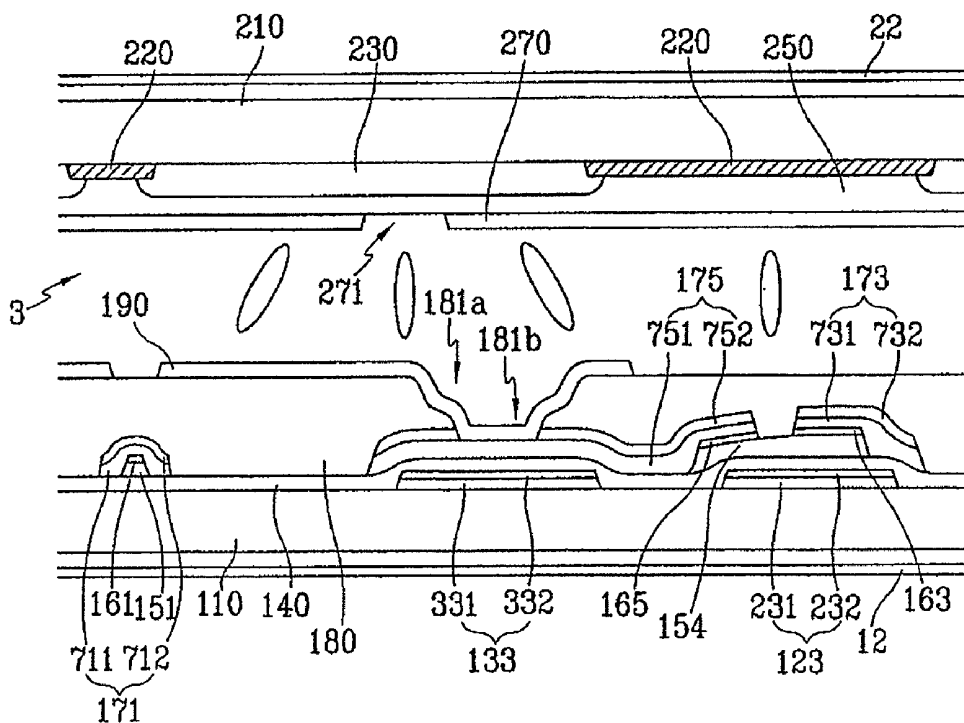


FIG. 5

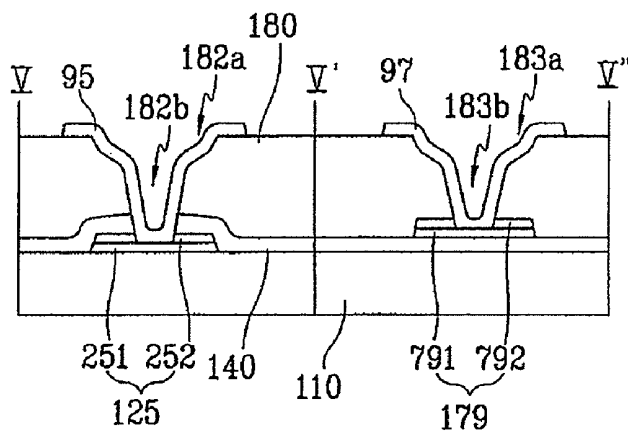


FIG.6A

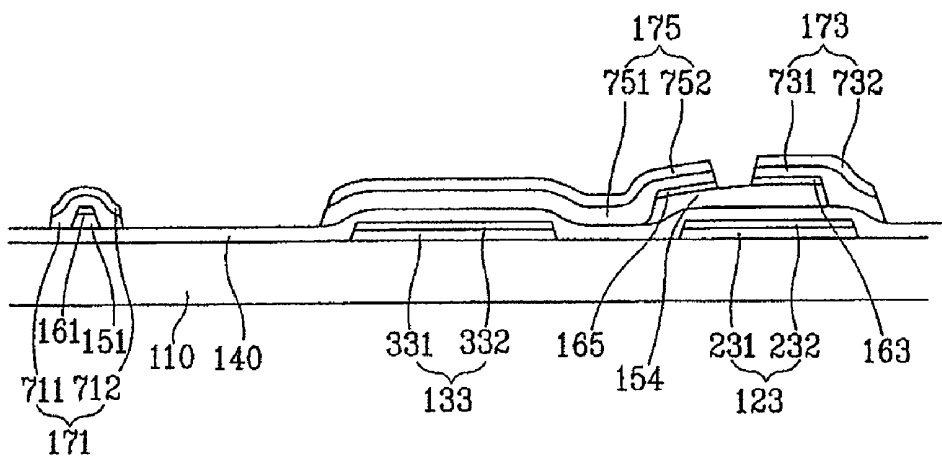


FIG.6B

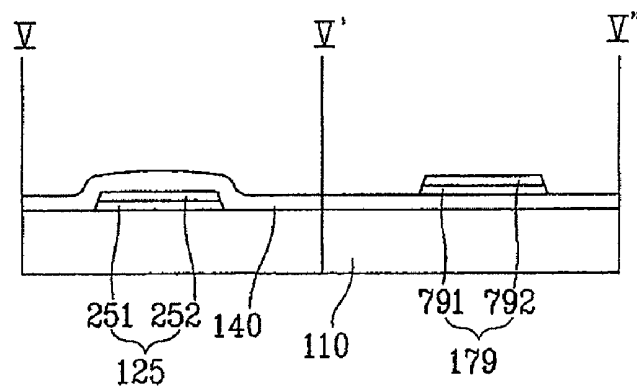


FIG.7A

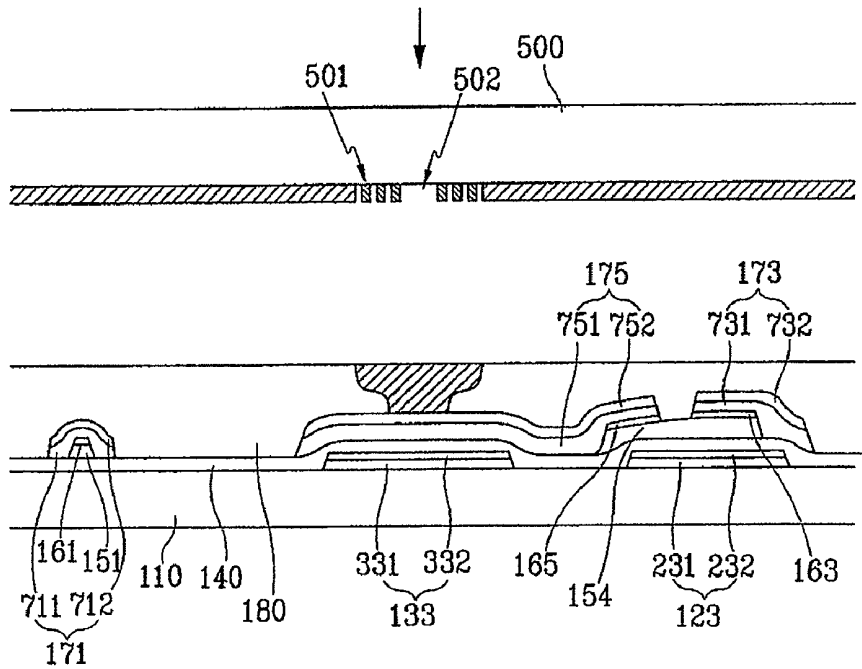


FIG.7B

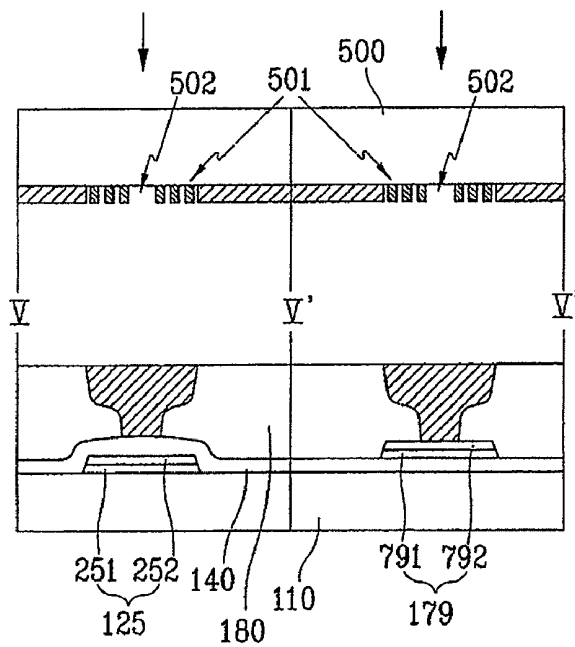


FIG. 8

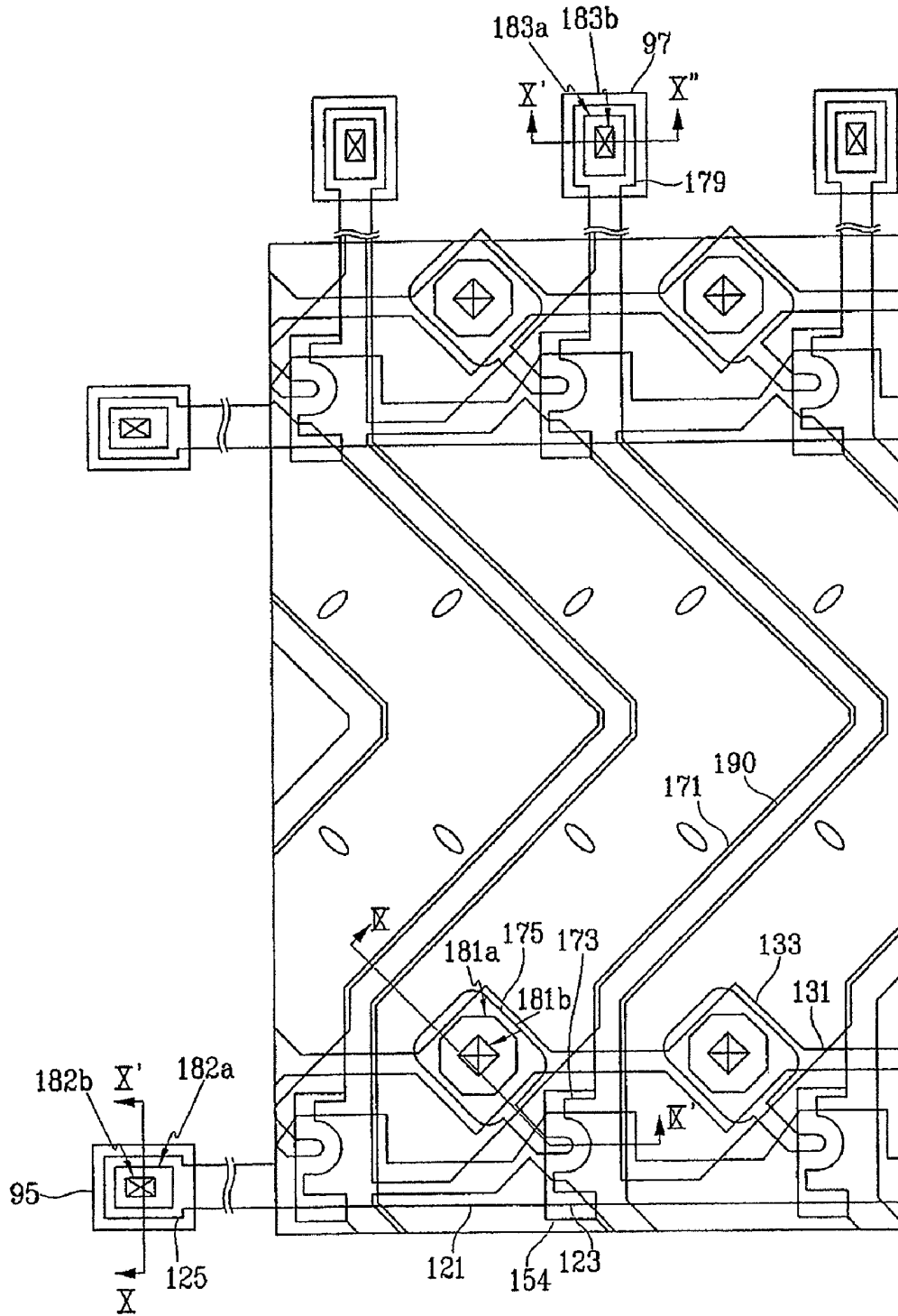


FIG.9

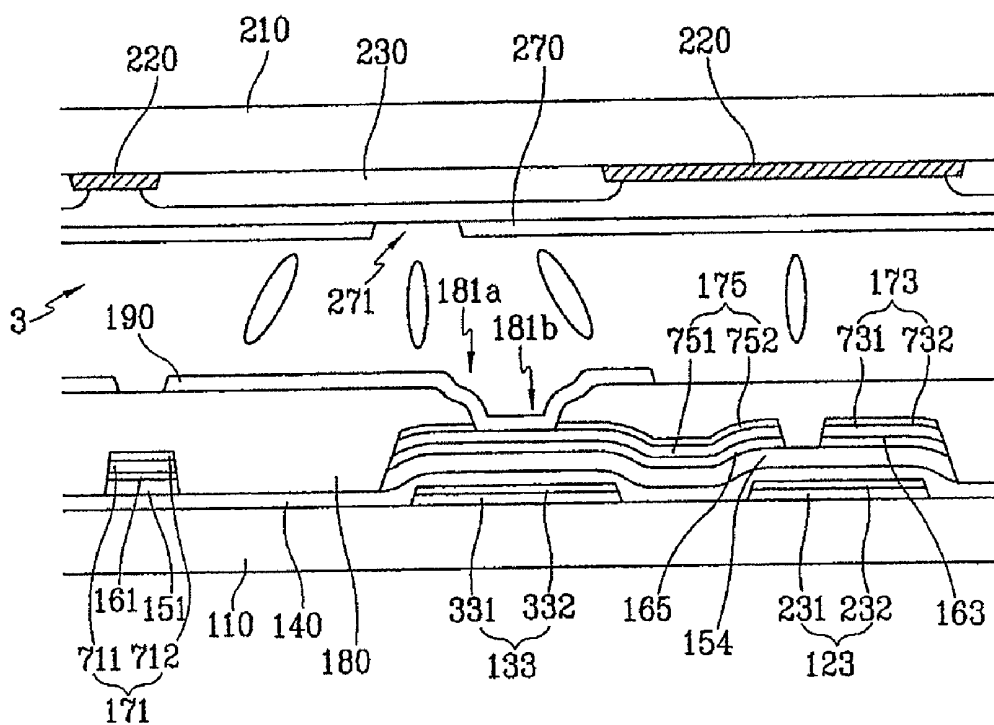


FIG.10

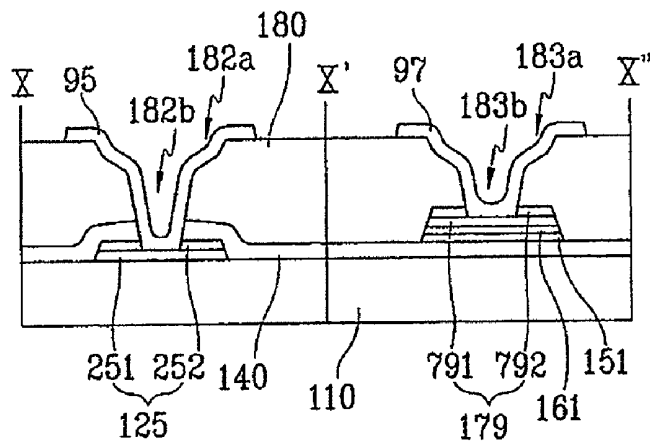


FIG.11A

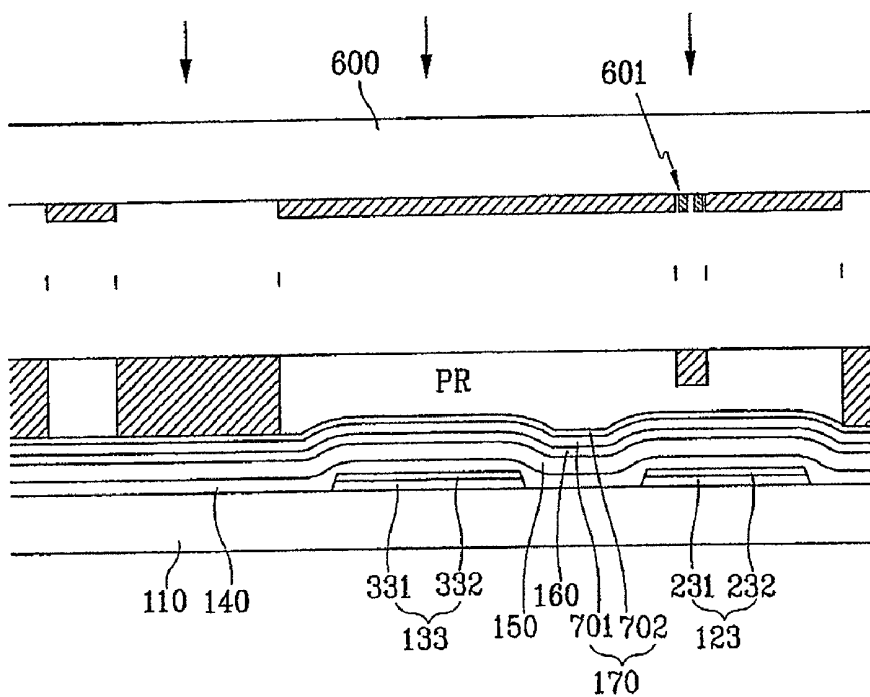


FIG.11B

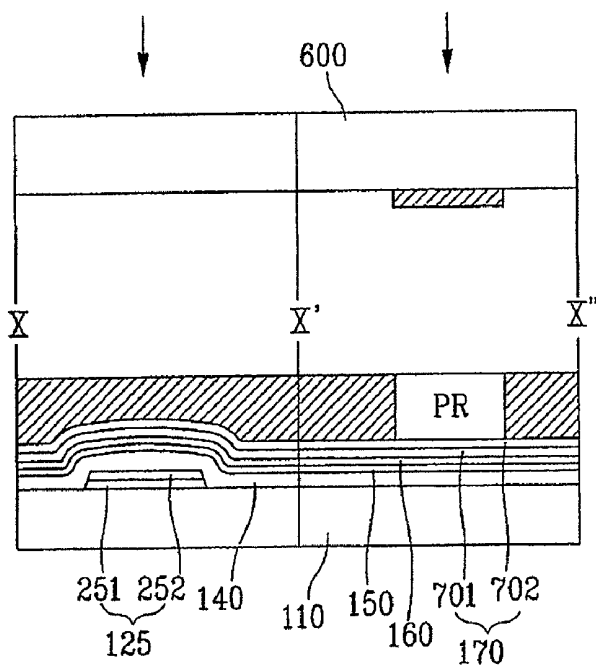


FIG.12A

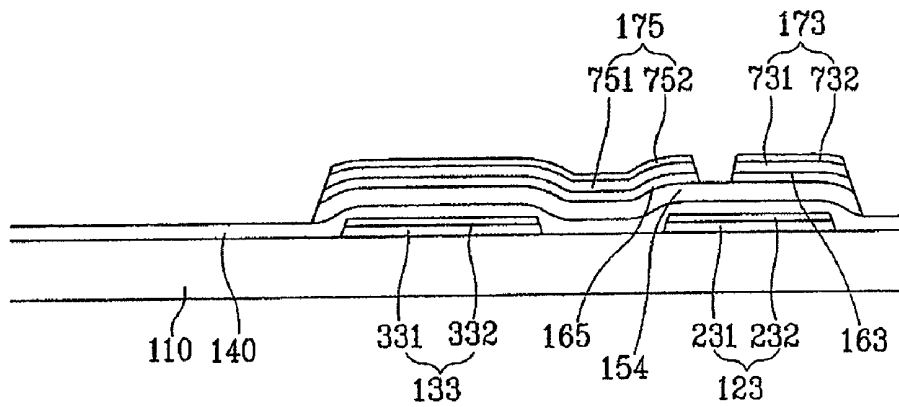


FIG.12B

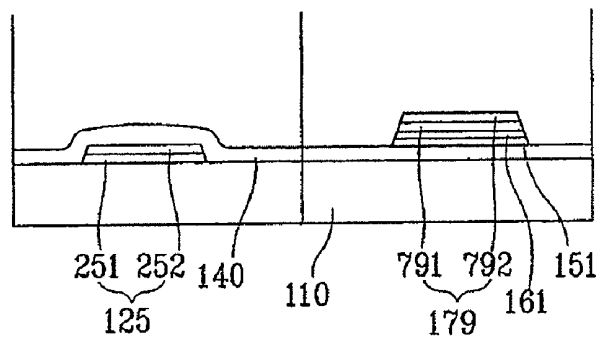


FIG.13A

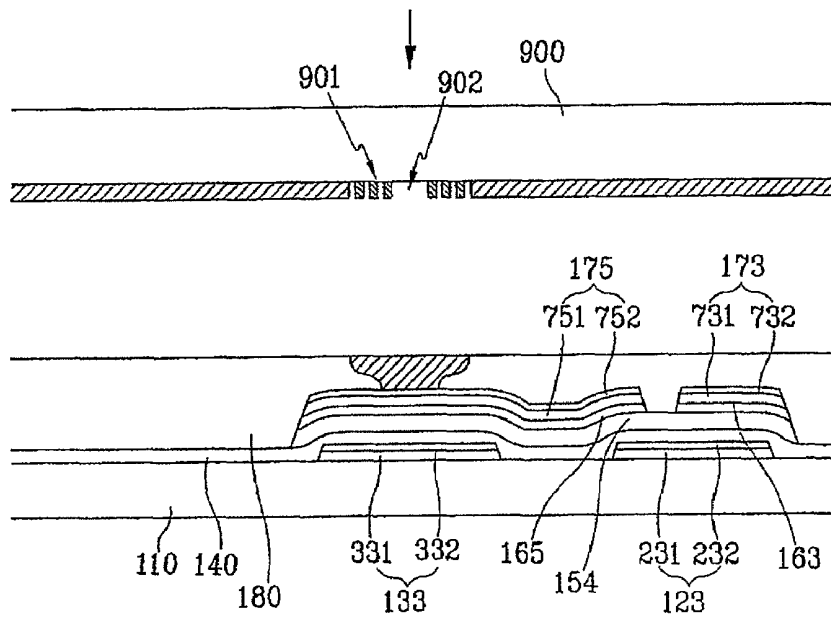


FIG.13B

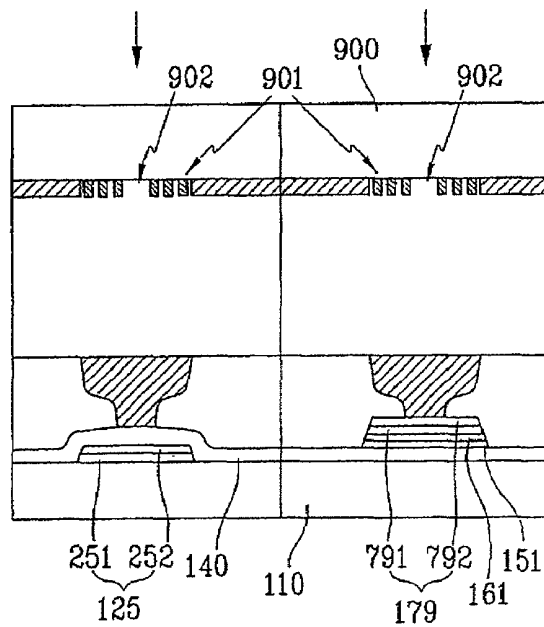


FIG. 14

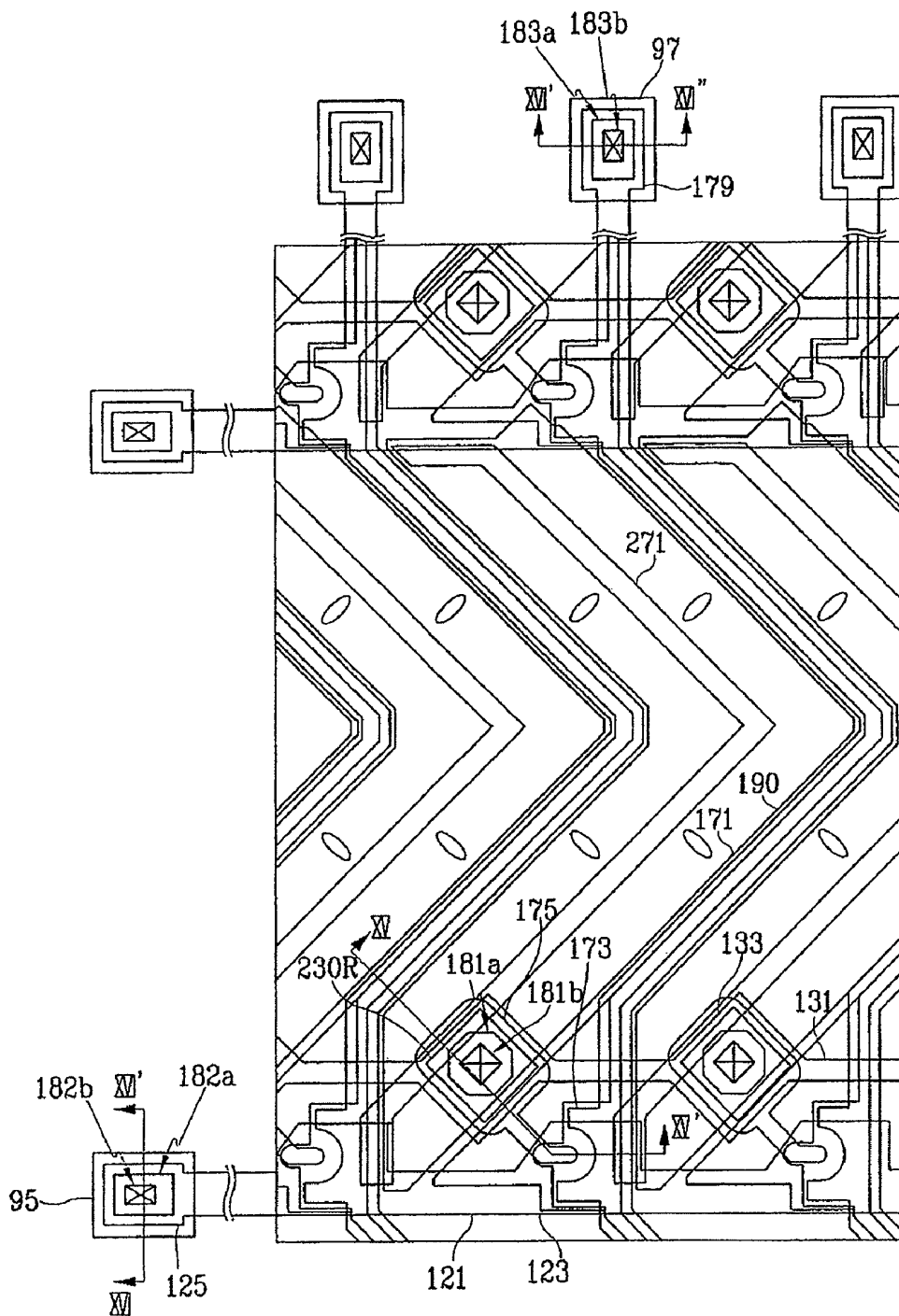


FIG. 15

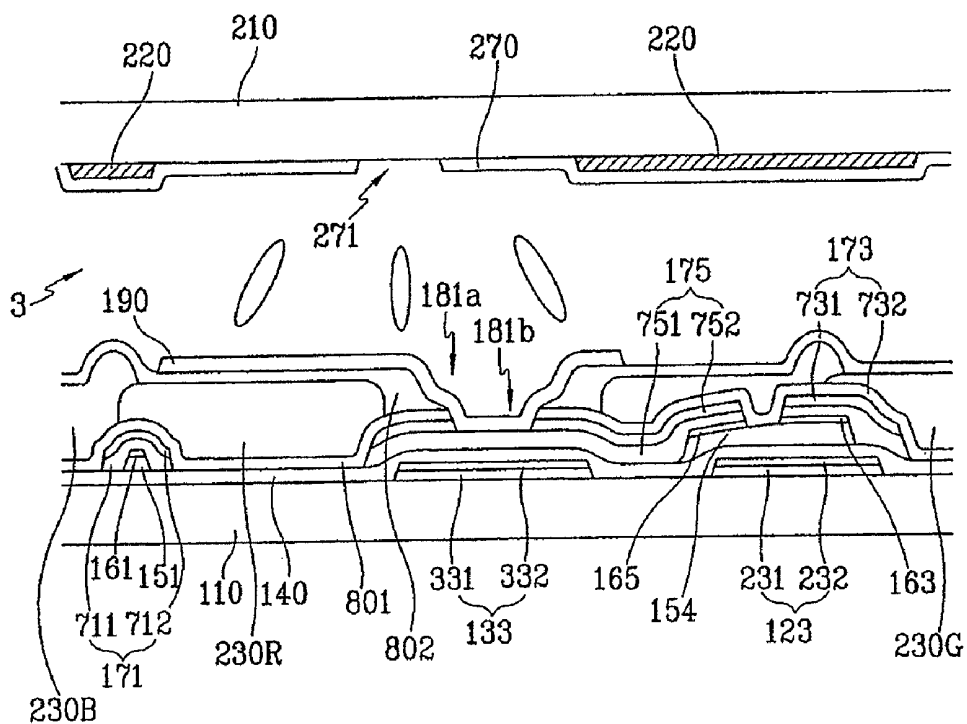


FIG. 16

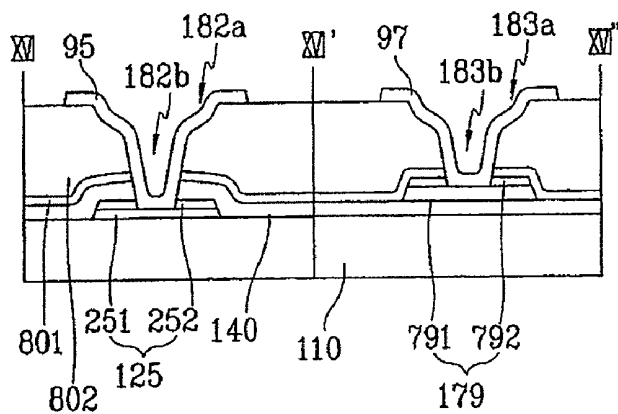


FIG. 17

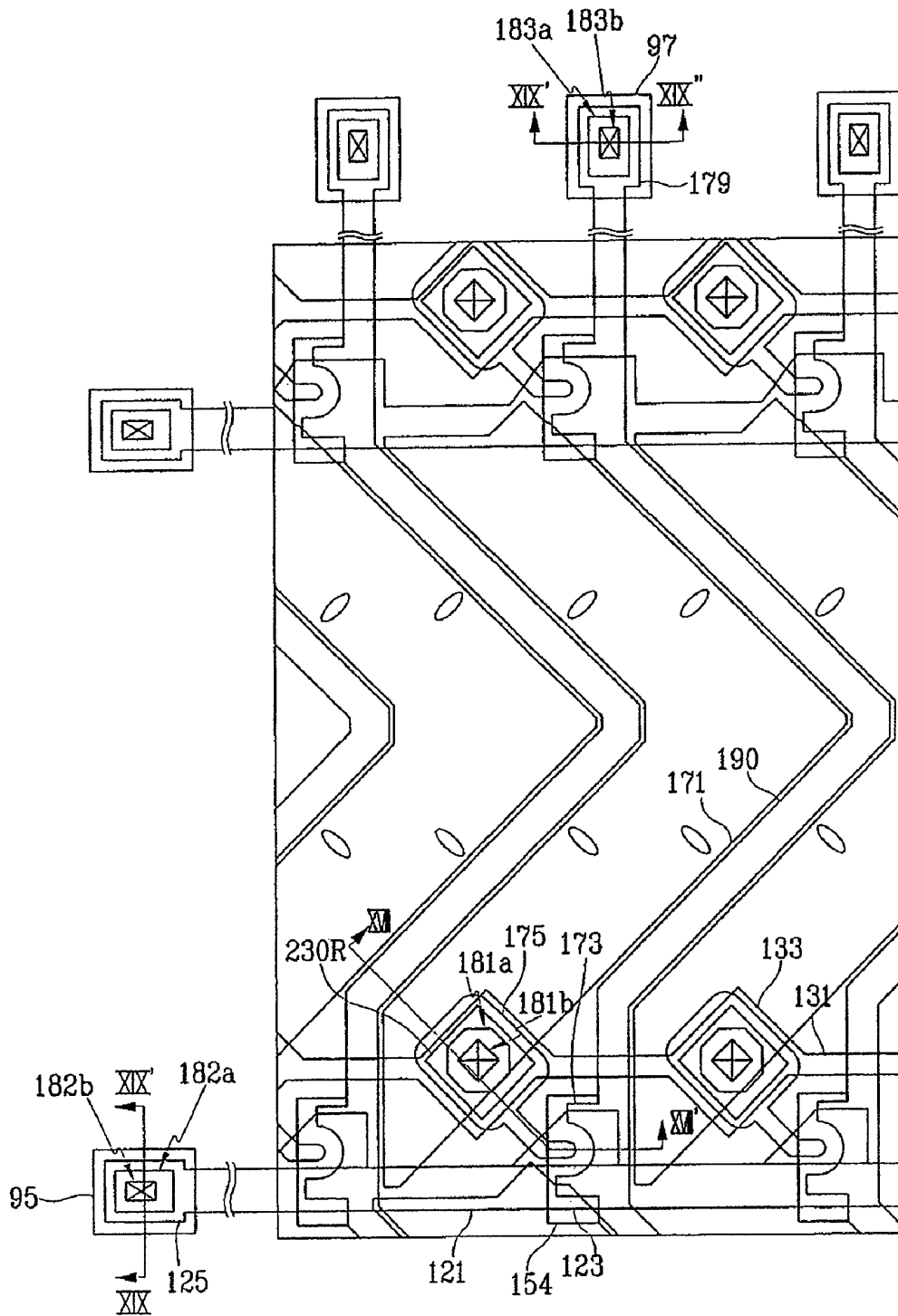


FIG.18

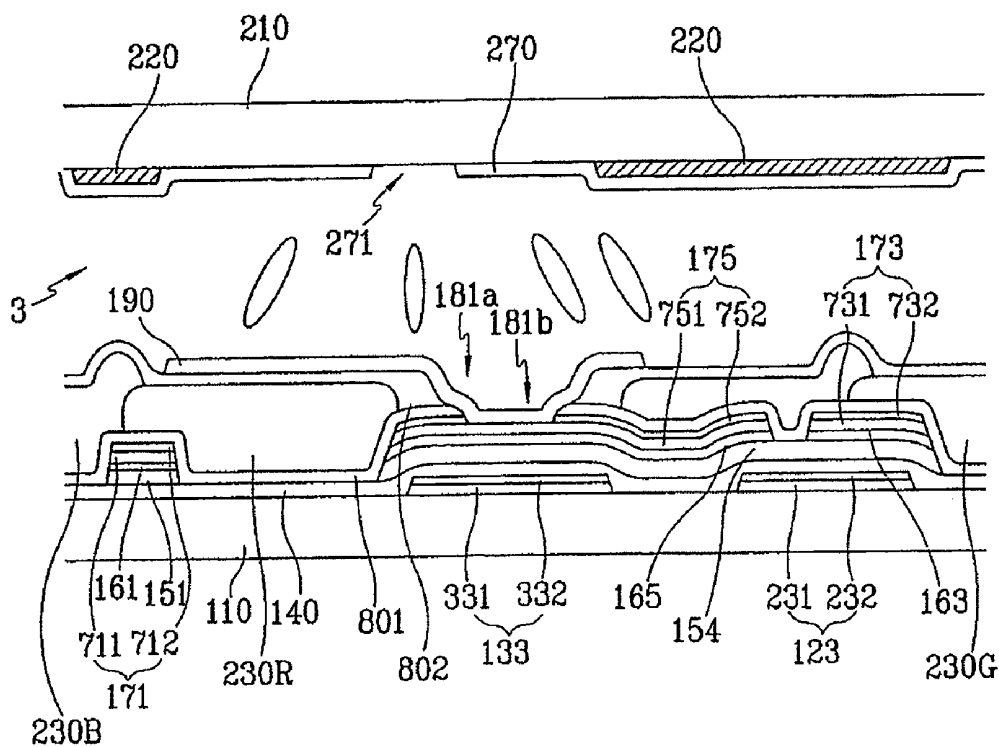


FIG.19

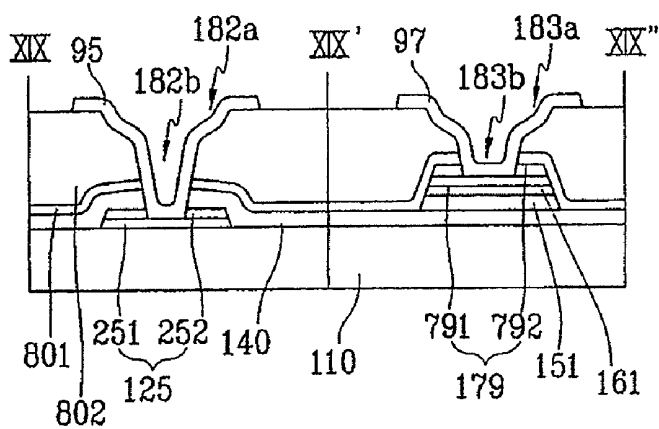


FIG.20

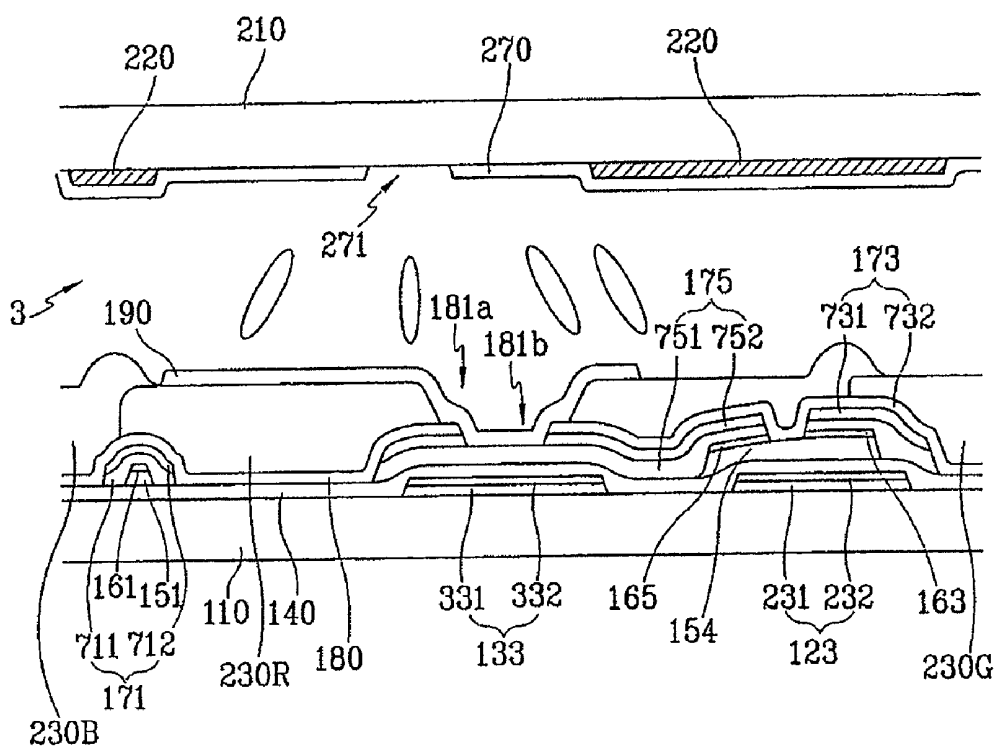


FIG.21

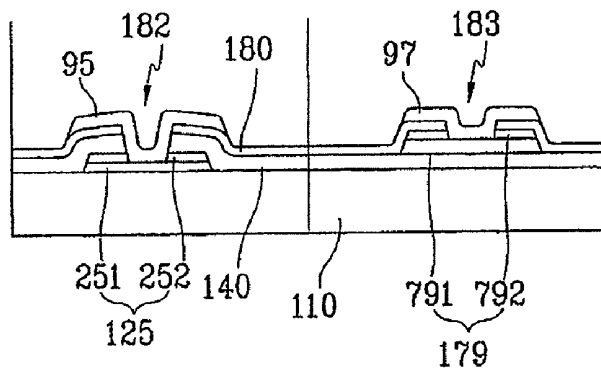


FIG.22

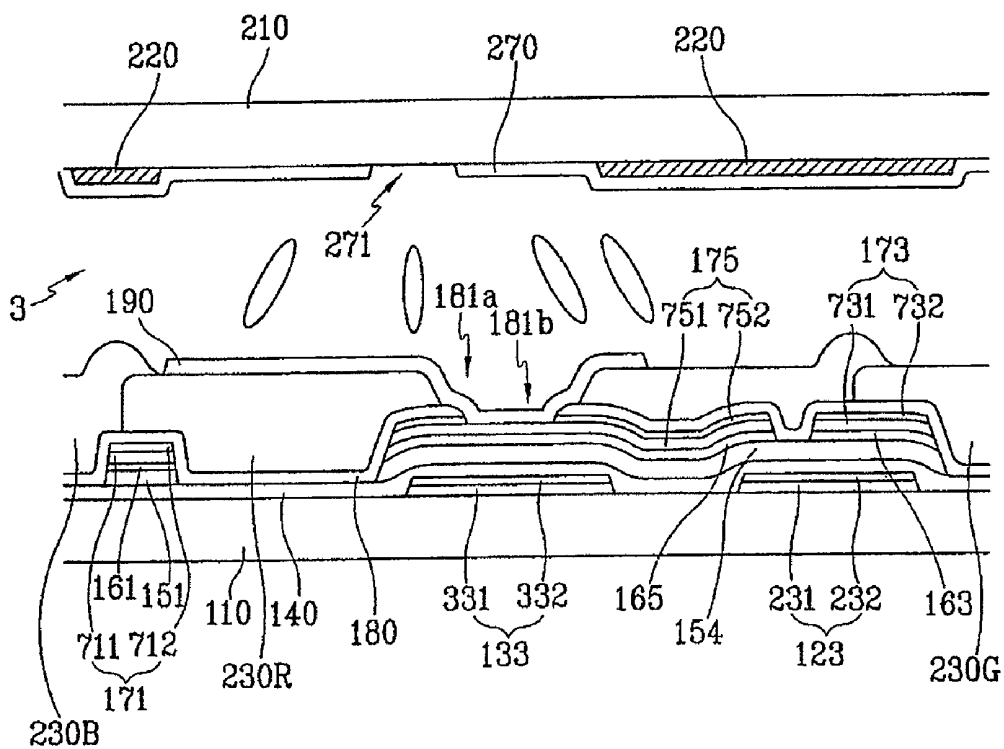


FIG.23

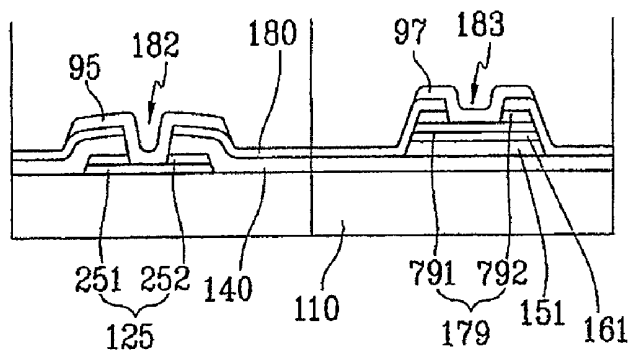


FIG.24

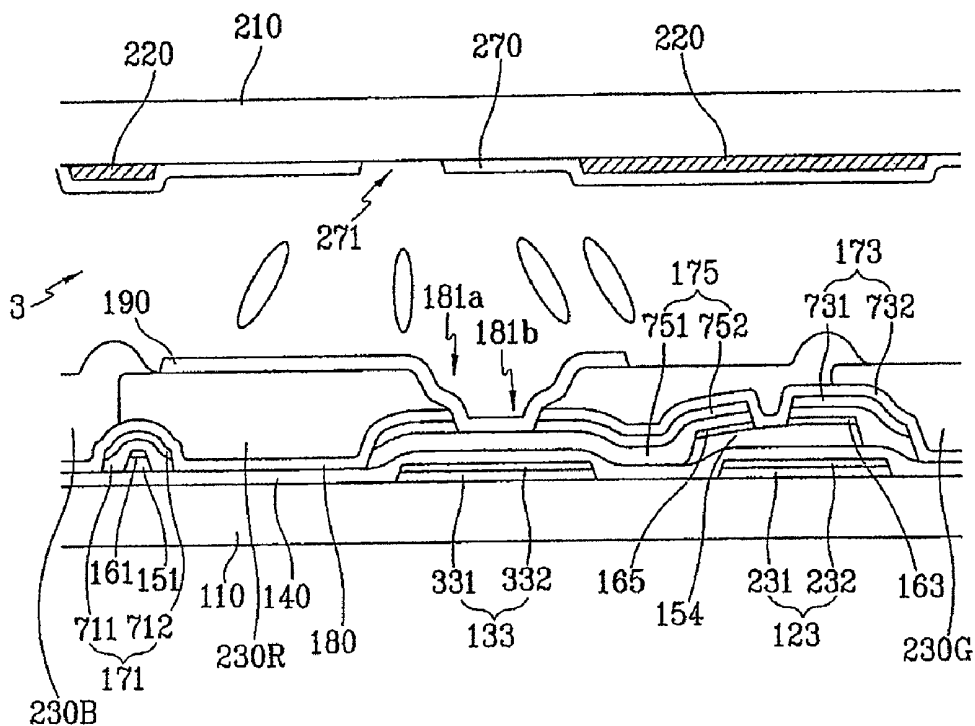


FIG.25

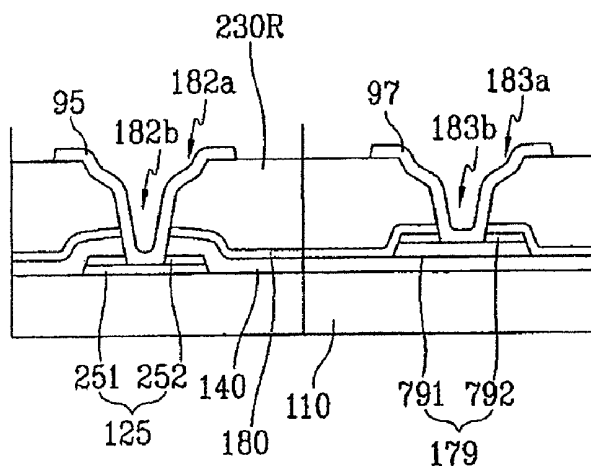


FIG.26

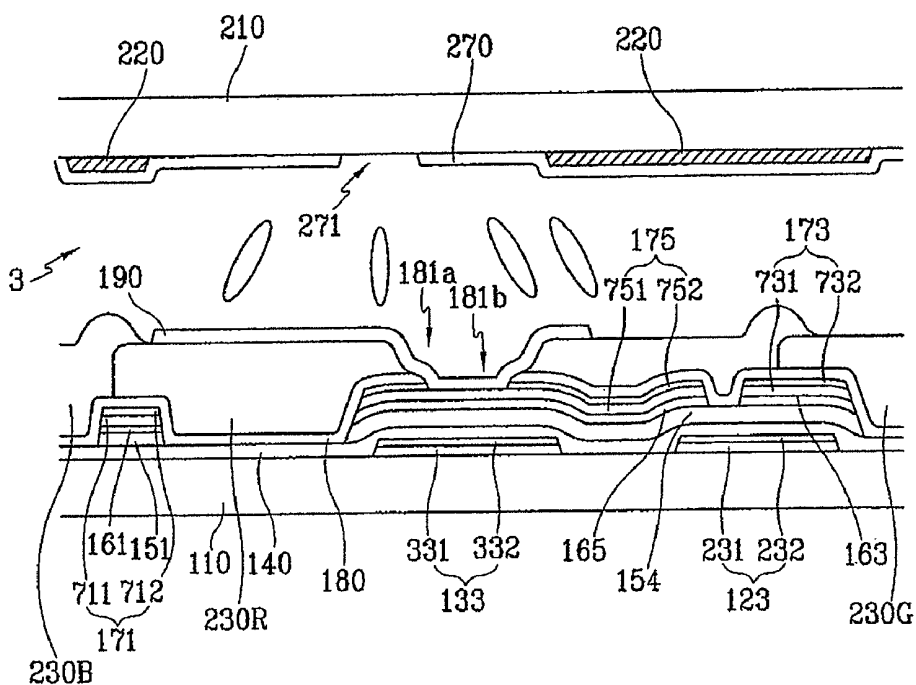


FIG.27

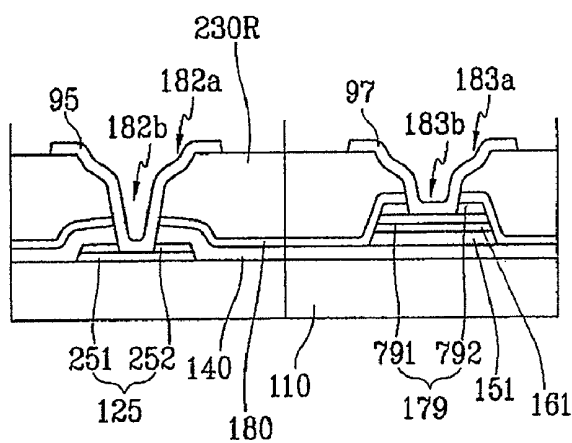


FIG.28

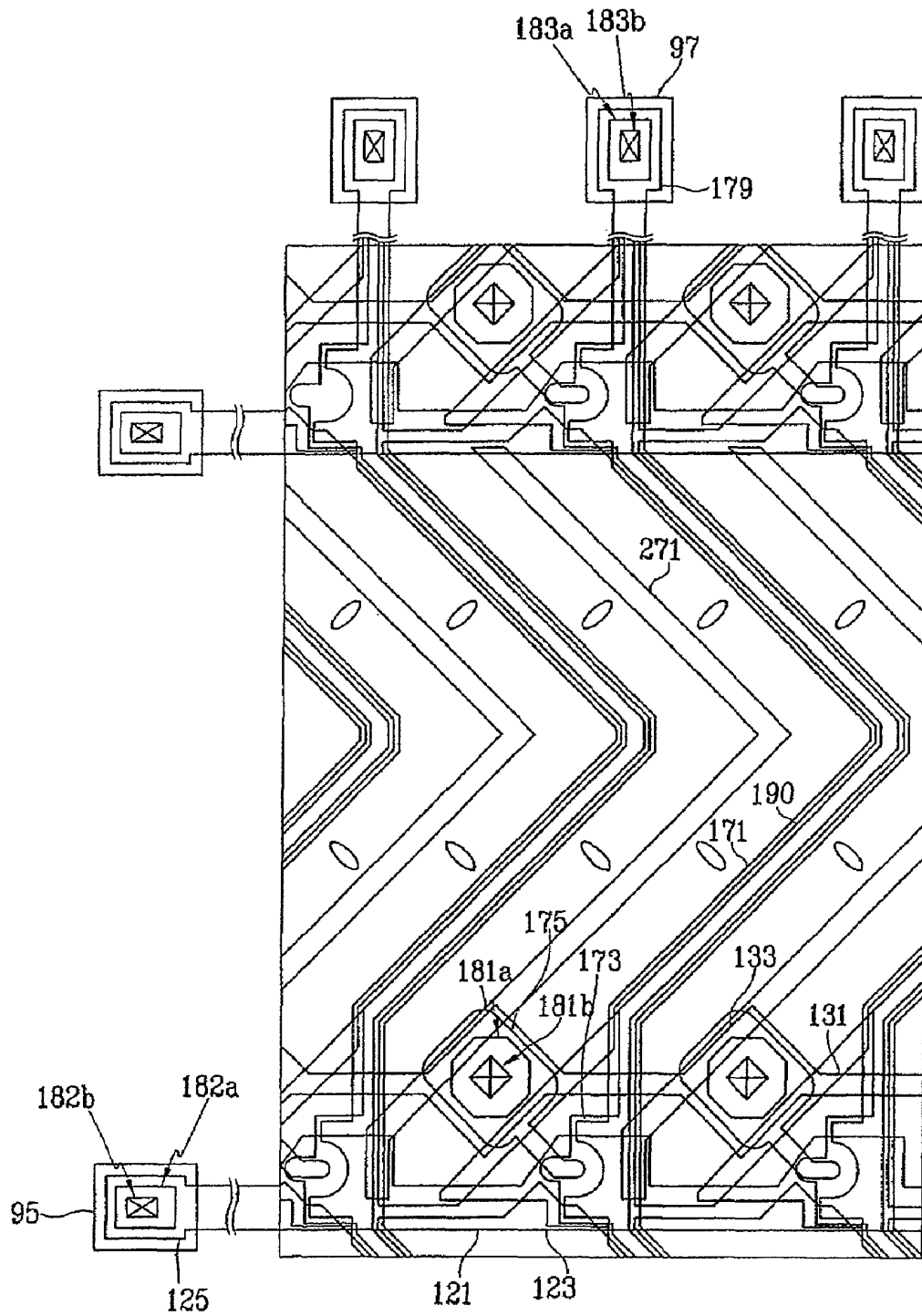
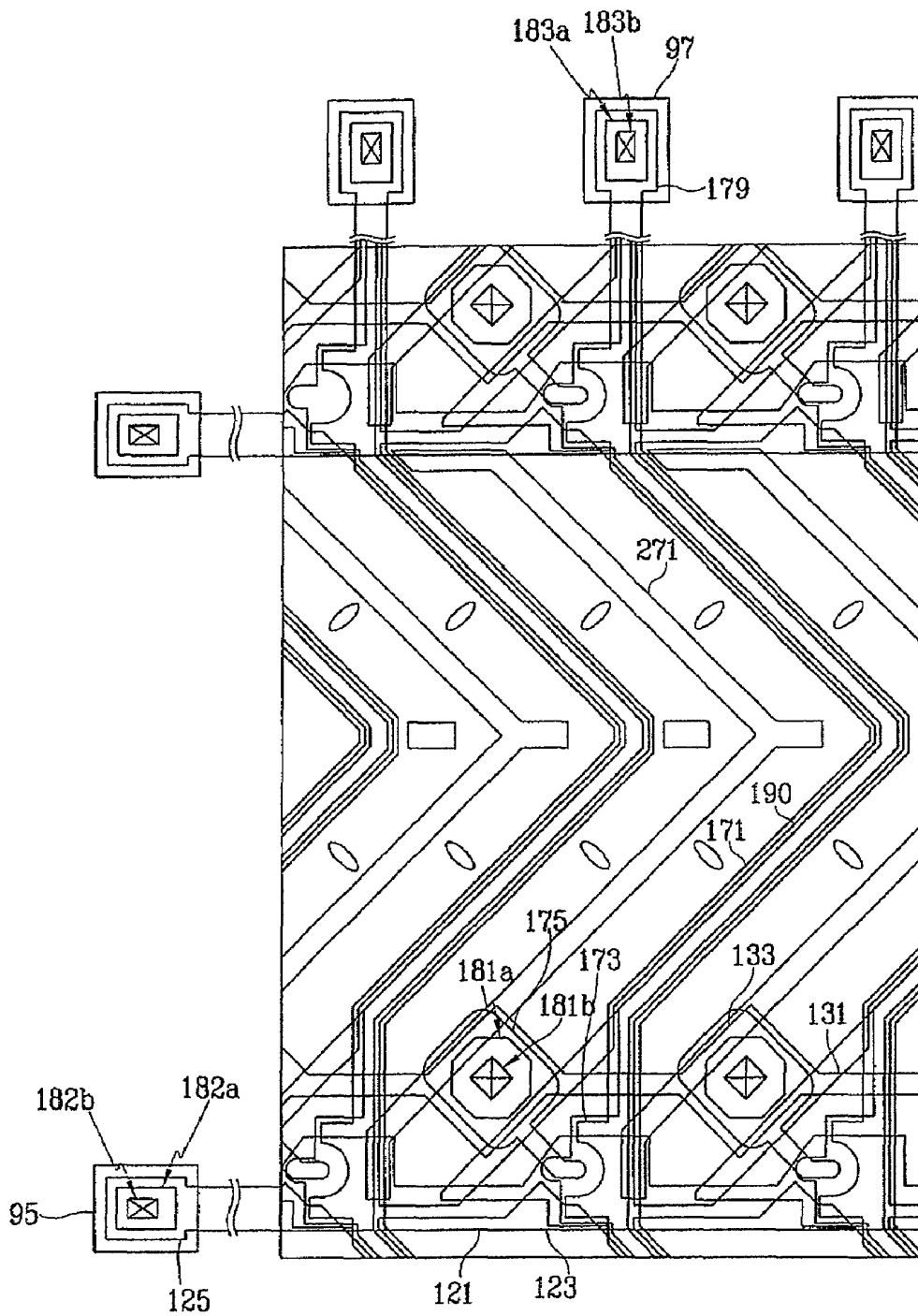


FIG.29



# LIQUID CRYSTAL DISPLAY AND THIN FILM TRANSISTOR ARRAY PANEL THEREFOR

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. application Ser. No. 10/806,379 filed on Mar. 23, 2004 now U.S. Pat. No. 7,580,102, which claims priority to Korean Application No. 2003-0018195 filed on Mar. 24, 2003, the disclosures of which are hereby incorporated herein by reference in their entirety.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a liquid crystal display and a thin film transistor array panel therefor.

### 2. Description of the Related Art

A liquid crystal display (LCD) is one of the most widely used flat panel displays. LCDs are used in notebook or laptop computers, desktop computer monitors and televisions. LCDs are lightweight and occupy less space than conventional cathode ray tube (CRT) displays.

The general structure of an LCD consists of a liquid crystal (LC) layer that is positioned between pair of panels including field generating electrodes and polarizers. The LC layer is subject to an electric field generated by the electrodes and variations in the field strength change the molecular orientation of the LC layer. For example, upon application of an electric field, the molecules of the LC layer change their orientation and polarize light passing through the LC layer. Appropriately positioned polarized filters block the polarized light, creating dark areas that can represent desired images.

One measure of LCD quality is viewing angle (i.e., the available area when viewing the LCD in which minimum contrast can be seen). Various techniques for enlarging the viewing angle have been suggested, including a technique utilizing a vertically aligned LC layer and providing cutouts or protrusions at pixel electrodes. However, cutouts and the protrusions reduce the aperture ratio (i.e., ratio between the actual size of a sub-pixel and the area of the sub-pixel that can transmit light). To increase aperture ratio, it has been suggested that the size of the pixel electrodes be maximized. However, maximization of the size of the pixel electrodes results in a close distance between the pixel electrodes, causing strong lateral electric fields between the pixel electrodes. The strong electric fields cause unwanted altering of the orientation of the LC molecules, yielding textures and light leakage and deteriorating display characteristics.

## SUMMARY OF THE INVENTION

A thin film transistor array panel is provided, which includes: a substrate; a plurality of first signal lines formed on the substrate, extending in a first direction, and separated from each other by a predetermined interval; a plurality of second lines formed on the substrate, intersecting the first signal lines, and including a plurality of curved portions and intermediate portions extending in a second direction and alternately arranged by the predetermined interval; a plurality of pixel electrodes located substantially in areas defined by the first and the second signal lines; and a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes.

Each of the curved portions of the data lines may include a pair of rectilinear portions connected to each other and making an angle of about 45 degrees.

The thin film transistor array panel may further include a plurality of third signal lines formed on the substrate, extending substantially in the first direction, and overlapping the pixel electrodes to form storage capacitors.

The thin film transistors may include terminal electrodes connected to the pixel electrodes and overlapping one of the third signal lines with interposing an insulator.

The thin film transistors may include terminal electrodes connected to the intermediate portions of the second signal lines.

The first signal lines may intersect the intermediate portions of the second signal lines.

A thin film transistor array panel is provided, which includes: a substrate; a gate line formed on the substrate and including a gate electrode; a gate insulating layer formed on the gate line; a semiconductor layer formed on the gate insulating layer; a data line formed on the semiconductor layer at least in part and including a curved portion and an intermediate portion crossing the gate line substantially at a right angle, at least one of the curved portions and the intermediate portions having a source electrode; a drain electrode formed on the semiconductor layer at least in part and separated from the data line; a first passivation layer formed on the data line and the drain electrode; and a pixel electrode formed on the first passivation layer, connected to the drain electrode, and having an edge extending substantially parallel to the curved portion of the data line.

The curved portion of the data line may include a pair of portions making a clockwise angle of about 45 degrees and a counterclockwise angle of about 45 degrees, respectively.

The thin film transistor array panel may further include a storage electrode line formed on the substrate, extending substantially parallel to the gate lines, and including a storage electrode having an increased width, wherein the drain electrode has an expansion connected to the pixel electrode and overlapping the storage electrode.

The first passivation layer may include organic insulating material, and it is preferably made of photosensitive material.

The first passivation layer may include inorganic insulating material.

The thin film transistor array panel may further include a color filter formed on the first passivation layer.

The color filter may extend substantially parallel to the data line.

The color filter may have an opening on the drain electrode, the first passivation layer may have a contact hole exposing at least a portion of the drain electrode, and the pixel electrode is preferably connected to the drain electrode through the opening and the contact hole.

The opening may expose a top surface of the first passivation layer.

The thin film transistor array panel may further include a contact assistant formed on a portion of the gate line or a portion of the data line and made of the same material as the pixel electrode. The color filter may include a portion formed under the contact assistant.

The thin film transistor array panel may further include a second passivation layer formed on the color filter and made of a photosensitive organic material.

The first and the second passivation layers may have a contact hole that exposes at least a portion of the drain electrode and may have a sidewall making an angle of about 30 degrees to about 85 degrees with a surface of the substrate.

The first and the second passivation layers may have a contact hole that exposes at least a portion of the drain electrode and may have a stepped sidewall.

The pixel electrode may be connected to the drain electrode through the contact hole.

Entire bottom surfaces of the data line and the drain electrode may be disposed substantially on the semiconductor layer, the data line and the drain electrode may have substantially the same planar shape as the semiconductor layer, and the semiconductor layer may include a portion that is not covered with the data line and the drain electrode and disposed between the source electrode and the drain electrode.

A length of the curved portion of the data line may be about one to nine times a length of the intermediate portion of the data line.

The thin film transistor array panel may further include a pair of color filters formed on the first passivation layer and partly overlapping each other to form a hill.

The thin film transistor array panel may further include a second passivation layer formed on the color filters and forming a projection on the hill of the color filters.

A liquid crystal display is provided, which includes: a first substrate; a plurality of first signal lines formed on the substrate; a plurality of second lines formed on the substrate, intersecting the first signal lines, and including a plurality of curved portions; a plurality of pixel electrodes located substantially in areas defined by the first and the second signal lines; a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes; a second substrate facing the second substrate; a common electrode formed on the second substrate; a region partitioning member formed on at least one of the first and the second substrates; and a liquid crystal layer disposed between the first substrate and the second substrate and partitioned into a plurality of tilt regions by the region partitioning member, each tilt region including a pair of major edges parallel to the curved portions of the second signal lines.

The liquid crystal layer may have negative dielectric anisotropy and is subject to vertically alignment.

The region partitioning member may include a plurality of cutouts formed in the common electrode. The cutouts may have width ranging about 9 microns to about 12 microns.

A distance between the major edges of each region may be in a range between about 10 microns and about 30 microns.

The tilt regions are preferably classified into four domains based on tilt directions of liquid crystal molecules included therein upon application of an electric field.

The number of the tilt regions in a pixel region defined by the first signal lines and the second signal lines may be four if a planar area of the pixel region is smaller than about 100×300 square microns, and the number of the tilt regions in a pixel region defined by the first signal lines and the second signal lines is four or eight if a planar area of the pixel region is equal to or larger than about 100×300 square microns.

A pair of crossed polarizers may be provided on outer surfaces of the first and the second substrates, respectively, and the first and the second polarizers are preferably aligned so that one of the transmissive axes of the polarizers be parallel to the first signal lines.

The region partitioning member comprises a protrusion formed on the common electrode and having a width ranging about 5 microns to about 10 microns.

A liquid crystal display is provided, which includes: a first substrate; a plurality of first signal lines formed on the substrate; a plurality of second lines formed on the substrate, intersecting the first signal lines, and including a plurality of curved portions; a plurality of pixel electrodes located sub-

stantially in areas defined by the first and the second signal lines; a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes; a second substrate facing the second substrate; a common electrode formed on the second substrate; a region partitioning member formed on at least one of the first and the second substrates; and a liquid crystal layer disposed between the first substrate and the second substrate and partitioned into a plurality of tilt regions by the region partitioning member, wherein liquid crystal molecules included in each tilt region tend to tilt in a direction parallel to an electric field generated between adjacent pixel electrodes.

A pair of crossed polarizers may be provided on outer surfaces of the first and the second substrates, respectively, and the first and the second polarizers are aligned so that one of the transmissive axes of the polarizers be parallel to the first signal lines.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

FIG. 1 is a layout view of a TFT array panel for an LCD according to an embodiment of the present invention;

FIG. 2 is a layout view of a common electrode panel for an LCD according to an embodiment of the present invention;

FIG. 3 is a layout view of an LCD including the TFT array panel shown in FIG. 1 and the common electrode panel shown in FIG. 2;

FIG. 4 is a sectional view of the LCD shown in FIG. 3 taken along the line IV-IV';

FIG. 5 is a sectional view of the LCD shown in FIG. 3 taken along the lines V-V' and V'-V'';

FIGS. 6A and 6B are sectional views of the TFT array panel shown in FIGS. 1, 4 and 5 taken along the line IV-IV' and the lines V-V' and V'-V'', respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention;

FIGS. 7A and 7B are sectional views of the TFT array panel shown in FIGS. 1, 4 and 5 taken along the line IV-IV' and the lines V-V' and V'-V'', respectively, in the step of the manufacturing method following the step shown in FIGS. 4A and 4B;

FIG. 8 is a layout view of an LCD according to another embodiment of the present invention;

FIG. 9 is a sectional view of the LCD shown in FIG. 8 taken along the line IX-IV';

FIG. 10 is a sectional view of the LCD shown in FIG. 8 taken along the lines X-X' and X'-X'';

FIGS. 11A and 11B are sectional views of the TFT array panel shown in FIG. 8-10 taken along the line IX-IX' and the lines X-X' and X'-X'', respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention;

FIGS. 12A and 12B are sectional views of the TFT array panel shown in FIG. 8-10 taken along the line IX-IX' and the lines X-X' and X'-X'' in the step of the manufacturing method following the step shown in FIGS. 11A and 11B;

FIGS. 13A and 13B are sectional views of the TFT array panel shown in FIG. 8-10 taken along the line IX-IX' and the lines X-X' and X'-X'' in the step of the manufacturing method following the step shown in FIGS. 12A and 12B;

FIG. 14 is a layout view of an LCD according to another embodiment of the present invention;

FIG. 15 is a sectional view of the LCD shown in FIG. 14 taken along the line XV-XV';

FIG. 16 is a sectional view of the LCD shown in FIG. 14 taken along the lines XVI-XV1' and XV1'-XVI";

FIG. 17 is a layout view of an LCD according to another embodiment of the present invention;

FIG. 18 is a sectional view of the LCD shown in FIG. 17 taken along the line XVIII-XVIII';

FIG. 19 is a sectional view of the LCD shown in FIG. 17 taken along the lines XIX-XIX' and XIX'-XIX";

FIGS. 20 and 21 are sectional views of an LCD according to another embodiment of the present invention;

FIGS. 22 and 23 are sectional views of an LCD according to another embodiment of the present invention;

FIGS. 24 and 25 are sectional views of an LCD according to another embodiment of the present invention;

FIGS. 26 and 27 are sectional views of an LCD according to another embodiment of the present invention;

FIG. 28 is a layout view of an LCD according to another embodiment of the present invention; and

FIG. 29 is a layout view of an LCD according to another embodiment of the present invention.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Now, liquid crystal displays and thin film transistor (TFT) array panels for LCDs according to embodiments of the present invention will be described with reference to the accompanying drawings.

FIG. 1 is a layout view of a TFT array panel for an LCD according to an embodiment of the present invention, FIG. 2 is a layout view of a common electrode panel for an LCD according to an embodiment of the present invention, FIG. 3 is a layout view of an LCD including the TFT array panel shown in FIG. 1 and the common electrode panel shown in FIG. 2, FIG. 4 is a sectional view of the LCD shown in FIG. 3 taken along the line IV-IV', and FIG. 5 is a sectional view of the LCD shown in FIG. 3 taken along the lines V-V' and V'-V".

An LCD according to an embodiment of the present invention includes a TFT array panel, a common electrode panel facing the TFT array panel, and a LC layer 3 interposed between the TFT array panel and the common electrode panel.

The TFT array panel is now described in detail with reference to FIGS. 1, 4 and 5.

A plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on an insulating substrate 110.

The gate lines 121 extend substantially in a transverse direction and are separated from each other and transmit gate signals. Each gate line 121 includes a plurality of projections forming a plurality of gate electrodes 123 and an end portion 125 having a large area for contact with another layer or an external device.

Each storage electrode line 131 extends substantially in the transverse direction and includes a plurality of projections forming storage electrodes 133. Each storage electrode 133 has a shape of a diamond or a rectangle rotated by about 45 degrees and they are located close to the gate lines 121. The storage electrode lines 131 are supplied with a predetermined voltage such as a common voltage, which is applied to a common electrode 270 on the common electrode panel of the LCD.

The gate lines 121 and the storage electrode lines 131 have a multi-layered structure including two films having different physical characteristics, a lower film and an upper film. The upper film is preferably made of low resistivity metal including Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy, or Cu containing metal such as Cu and Cu alloy for reducing signal delay or voltage drop in the gate lines 121 and the storage electrode lines 131. On the other hand, the lower film is preferably made of material such as Cr, Mo, Mo alloy, Ta, or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). A good exemplary combination of the lower film material and the upper film material is Cr and Al—Nd alloy. In FIG. 4, the lower and the upper films of the gate electrodes 123 are indicated by reference numerals 231 and 232, respectively, the lower and the upper films of the end portions 125 are indicated by reference numerals 251 and 252, respectively, and the lower and the upper films of the storage electrodes 133 are indicated by reference numerals 331 and 332, respectively. Portions of the upper film 252 of the end portions 125 of the gate lines 121 are removed to expose the underlying portions of the lower films 251.

The gate lines 121 and the storage electrode lines 131 may have a single layer structure or may include three or more layers.

In addition, the lateral sides of the gate lines 121 and the storage electrode lines 131 are inclined relative to a surface of the substrate 110, and the inclination angle thereof ranges about 30-80 degrees.

A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121 and the storage electrode lines 131.

A plurality of semiconductor stripes 151 preferably made of hydrogenated amorphous silicon (abbreviated as "a-Si") or polysilicon are formed on the gate insulating layer 140. Each semiconductor stripe 151 extends substantially in the longitudinal direction while it is curved periodically. Each semiconductor stripe 151 has a plurality of projections 154 branched out toward the gate electrodes 123. Each semiconductor island 150 is located opposite the gate electrodes 123.

A plurality of ohmic contact stripes and islands 161 and 165 preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity are formed on the semiconductor stripes 151. Each ohmic contact stripe 161 has a plurality of projections 163, and the projections 163 and the ohmic contact islands 165 are located in pairs on the projections 154 of the semiconductor stripes 151.

The lateral sides of the semiconductor stripes 151 and the ohmic contacts 161 and 165 are inclined relative to a surface of the substrate 110, and the inclination angles thereof are preferably in a range between about 30-80 degrees.

A plurality of data lines 171 and a plurality of drain electrodes 175 separated from each other are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140.

The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121 and the storage electrode lines 131. Each data

line 171 has an end portion 179 having a large area for contact with another layer or an external device and it includes a plurality of pairs of oblique portions and a plurality of longitudinal portions such that it curves periodically. A pair of oblique portions are connected to each other to form a chevron and opposite ends of the pair of oblique portions are connected to respective longitudinal portions. The oblique portions of the data lines 171 make an angle of about 45 degrees with the gate lines 121, and the longitudinal portions cross over the gate electrodes 123. The length of a pair of oblique portions is about one to nine times the length of a longitudinal portion, that is, it occupies about 50-90 percents of the total length of the pair of oblique portions and the longitudinal portion.

Each drain electrode 175 includes a rectangular expansion overlapping a storage electrode 133. The edges of the expansion of the drain electrode 175 are substantially parallel to the edges of the storage electrodes 133. Each longitudinal portion of the data lines 171 includes a plurality of projections such that the longitudinal portion including the projections forms a source electrode 173 partly enclosing an end portion of a drain electrode 175. Each set of a gate electrode 123, a source electrode 173, and a drain electrode 175 along with a projection 154 of a semiconductor stripe 151 form a TFT having a channel formed in the semiconductor projection 154 disposed between the source electrode 173 and the drain electrode 175.

The data lines 171 and the drain electrodes 175 also include a lower film 711 and 751 preferably made of Mo, Mo alloy or Cr and an upper film 712 and 752 located thereon and preferably made of Al containing metal. In FIGS. 4 and 5, the lower and the upper films of the source electrodes 173 are indicated by reference numerals 731 and 732, respectively, and the lower and the upper films of the end portions 179 of the data lines 171 are indicated by reference numerals 791 and 792, respectively. Portion of the upper films 792, 752 of the expansions 179 of the data lines 171 and the drain electrodes 175 are removed to expose the underlying portions of the lower films 791 and 751.

Like the gate lines 121 and the storage electrode lines 131, the data lines 171 and the drain electrodes 175 have inclined lateral sides, and the inclination angles thereof range about 30-80 degrees.

The ohmic contacts 161 and 165 are interposed only between the underlying semiconductor stripes 151 and the overlying data lines 171 and the overlying drain electrodes 175 thereon and reduce the contact resistance therebetween.

A passivation layer 180 is formed on the data lines 171 and the drain electrodes 175, and exposed portions of the semiconductor stripes 151, which are not covered with the data lines 171 and the drain electrodes 175. The passivation layer 180 is preferably made of photosensitive organic material having a good flatness characteristic, low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), or inorganic material such as silicon nitride and silicon oxide. The passivation layer 180 may have a double-layered structure including a lower inorganic film and an upper organic film.

The passivation layer 180 has a plurality of contact holes 181*b* and 183*b* exposing the drain electrodes 175 and the end portions 179 of the data lines 171, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 182*b* exposing the end portions 125 of the gate lines 121. The contact holes 181*b*, 182*b* and 183*b* can have various shapes such as polygon or circle. The area of each contact hole 182*b* or 183*b* is preferably equal to or larger than 0.5 mm×15 μm and not larger than 2 mm×60 μm. The sidewalls 181*a*, 182*a* and 183*a* of the contact holes 181*b*,

182*b* and 183*b* are inclined with an angle of about 30-85 degrees or have stepwise profiles.

A plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97, which are preferably made of ITO or IZO, are formed on the passivation layer 180.

Each pixel electrode 190 is located substantially in an area enclosed by the data lines 171 and the gate lines 121, and thus it also forms a chevron. The pixel electrodes 190 cover the storage electrode lines 131 including the storage electrodes 133 and the expansions of the drain electrodes 175 and have chamfered edges substantially parallel to edges of the storage electrodes 133 that are close to the chamfered edges.

The pixel electrodes 190 are physically and electrically connected to the drain electrodes 175 through the contact holes 181 such that the pixel electrodes 190 receive the data voltages from the drain electrodes 175. The pixel electrodes 190 supplied with the data voltages generate electric fields in cooperation with the common electrode 270, which reorient liquid crystal molecules disposed therebetween.

A pixel electrode 190 and a common electrode form a capacitor called a "liquid crystal capacitor," which stores applied voltages after turn-off of the TFT. An additional capacitor called a "storage capacitor," which is connected in parallel to the liquid crystal capacitor, is provided for enhancing the voltage storing capacity. The storage capacitors are implemented by overlapping the pixel electrodes 190 with the storage electrode lines 131. The capacitances of the storage capacitors, i.e., the storage capacitances are increased by providing the projections (i.e., the storage electrodes) 133 at the storage electrode lines 131, elongating the drain electrodes 175 connected to the pixel electrodes 190, and providing the expansions at the drain electrodes 175 overlapping the storage electrodes 133 of the storage electrode lines 131 for decreasing the distance between the terminals and increasing the overlapping areas.

The pixel electrodes 190 overlap the data lines 171 as well as the gate lines 121 to increase aperture ratio.

The contact assistants 95 and 97 are connected to the exposed end portions 125 of the gate lines 121 and the exposed end portions 179 of the data lines 171 through the contact holes 181 and 182, respectively. The contact assistants 95 and 97 protect the exposed portions 125 and 179 and complement the adhesiveness of the exposed portions 125 and 179 and external devices.

Finally, an alignment layer (not shown) is formed on the pixel electrodes 190, the contact assistants 95 and 97, and the passivation layer 180.

The description of the common electrode panel follows with reference to FIGS. 2, 4 and 5.

A light blocking member called a light blocking member 220 is formed on an insulating substrate 210 such as transparent glass and it includes a plurality of oblique portions facing the oblique portions of the data lines 171 and a plurality of right-angled-triangular portions facing the TFTs and the longitudinal portions of the data lines 171 such that the light blocking member 220 prevents light leakage between the pixel electrodes 190 and defines open areas facing the pixel electrodes 190. Each of the triangular portions of the light blocking member 220 has a hypotenuse parallel to a chamfered edge of a pixel electrode 190.

A plurality of color filters 230 are formed on the substrate 210 and the light blocking member 220 and it is disposed substantially in the open areas defined by the light blocking member 220. The color filters 230 disposed in adjacent two data lines 171 and arranged in the longitudinal direction may

be connected to each other to form a stripe. Each color filter **230** may represent one of three primary colors such as red, green and blue colors.

An overcoat **250** preferably made of organic material is formed on the color filters **230** and the light blocking member **220**. The overcoat **250** protects the color filters **230** and has a flat top surface.

A common electrode **270** preferably made of transparent conductive material such as ITO and IZO is formed on the overcoat **250**. The common electrode **270** is supplied with the common voltage and it has a plurality of chevron-like cutouts **271**. Each cutout **271** includes a pair of oblique portions connected to each other, a transverse portion connected to one of the oblique portions, and a longitudinal portion connected to the other of the oblique portions. The oblique portions of the cutout **271** extend substantially parallel to the oblique portions of the data lines **171** and face a pixel electrode **190** so that they may bisect the pixel electrode **190** into left and right halves. The transverse and the longitudinal portions of the cutout **271** are aligned with transverse and longitudinal edges of the pixel electrode **190**, respectively, and they make obtuse angles with the oblique portions of the cutout **190**. The cutouts **271** are provided for controlling the tilt directions of the LC molecules in the LC layer **3** and preferably have a width in a range between about 9-12 microns. The cutouts **271** may be substituted with protrusions preferably made of organic material and preferably having width ranging about 5 microns to 10 microns.

A homogeneous or homeotropic alignment layer (not shown) is coated on the common electrode **270**.

A pair of polarizers **12** and **22** are provided on outer surfaces of the panels such that their transmissive axes are crossed and one of the transmissive axes is parallel to the gate lines **121**.

The LCD may further include at least one retardation film for compensating the retardation of the LC layer **3** and a backlight unit for providing light for the LCD.

The LC layer **3** has negative dielectric anisotropy and the LC molecules in the LC layer **3** are aligned such that their long axes are vertical to the surfaces of the panels in absence of electric field.

Upon application of the common voltage to the common electrode **270** and a data voltage to the pixel electrodes **190**, a primary electric field substantially perpendicular to the surfaces of the panels is generated. The LC molecules tend to change their orientations in response to the electric field such that their long axes are perpendicular to the field direction. In the meantime, the cutouts **271** of the common electrode **270** and the edges of the pixel electrodes **190** distort the primary electric field to have a horizontal component which determines the tilt directions of the LC molecules. The horizontal component of the primary electric field is perpendicular to the edges of the cutouts **271** and the edges of the pixel electrodes **190**.

Accordingly, four sub-regions having different tilt directions, which are partitioned by edges of a pixel electrode **190**, a cutout **271** bisecting the pixel electrode **190**, and an imaginary transverse center line passing through the meeting point of the oblique portions of the cutout **271**, are formed in a pixel region of the LC layer **3**, which are located on the pixel electrode **190**. Each sub-region has two major edges defined by the cutout **271** and an oblique edge of the pixel electrode **190**, respectively, which are spaced apart preferably from about 10 microns to about 30 microns, as shown by arrows A in FIG. 3. The number of the sub-regions in a pixel region is preferably four if the planar area of the pixel region is smaller than about 100×300 square microns, and, if not, it is prefer-

ably four or eight. The number of the sub-regions can be varied by changing the number of the cutouts **271** of the common electrode **270**, by providing cutouts at the pixel electrodes **190**, or by changing the number of curved points of the edges of the pixel electrodes **190**. The sub-regions are classified into a plurality of, preferably four, domains based on the tilt directions.

In the meantime, the direction of a secondary electric field due to the voltage difference between the pixel electrodes **190** is perpendicular to the edges of the cutouts **271**. Accordingly, the field direction of the secondary electric field coincides that of the horizontal component of the primary electric field. Consequently, the secondary electric field between the pixel electrodes **190** enhances the determination of the tilt directions of the LC molecules.

Since the LCD performs inversion such as dot inversion, column inversion, etc., adjacent pixel electrodes are supplied with data voltages having opposite polarity with respect to the common voltage and thus a secondary electric field between the adjacent pixel electrodes is almost always generated to enhance the stability of the domains.

Since the tilt directions of all domains make an angle of about 45 degrees with the gate lines **121**, which are parallel to or perpendicular to the edges of the panels, and the 45-degree intersection of the tilt directions and the transmissive axes of the polarizers gives maximum transmittance, the polarizers can be attached such that the transmissive axes of the polarizers are parallel to or perpendicular to the edges of the panels and it reduces the production cost.

The resistance increase of the data lines **171** due to the curving can be compensated by widening the data lines **171** since distortion of the electric field and increase of the parasitic capacitance due to the increase of the width of the data lines **171** can be compensated by maximizing the size of the pixel electrodes **190** and by adapting a thick organic passivation layer.

A method of manufacturing the TFT array panel shown in FIGS. 1-5 according to an embodiment of the present invention will be now described in detail with reference to FIGS. 6A, 6B, 7A and 7B as well as FIGS. 1-5.

FIGS. 6A and 6B are sectional views of the TFT array panel shown in FIGS. 1, 4 and 5 taken along the line IV-IV' and the lines V-V' and V'-V'', respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention, and FIGS. 7A and 7B are sectional views of the TFT array panel shown in FIGS. 1, 4 and 5 taken along the line IV-IV' and the lines V-V' and V'-V'', respectively, in the step of the manufacturing method following the step shown in FIGS. 6A and 6B.

Referring to FIGS. 1, 6A and 6B, a lower conductive film preferably made of Cr, Mo, or Mo alloy and an upper conductive film preferably made of Al containing metal or Ag containing metal are sputtered in sequence on an insulating substrate **110** and they are wet or dry etched in sequence to form a plurality of gate lines **121**, each including a plurality of gate electrodes **123** and an expansion **125**, and a plurality of storage electrode lines **131** including a plurality of storage electrodes **133**. In FIGS. 6A and 6B, the lower and the upper films of the gate electrodes **123** are indicated by reference numerals **231** and **232**, respectively, the lower and the upper films of the expansions **125** are indicated by reference numerals **251** and **252**, respectively, and the lower and the upper films of the storage electrodes **133** are indicated by reference numerals **331** and **332**, respectively.

After sequential deposition of a gate insulating layer **140** with thickness of about 1,500-5,000 Å, an intrinsic a-Si layer with thickness of about 500-2,000 Å, and an extrinsic a-Si

layer with thickness of about 300-600 Å, the extrinsic a-Si layer and the intrinsic a-Si layer are photo-etched to form a plurality of extrinsic semiconductor stripes and a plurality of intrinsic semiconductor stripes **151** including a plurality of projections **154** on the gate insulating layer **140**.

Subsequently, two conductive films including a lower conductive film and an upper conductive film and having a thickness of 1,500-3,000 Å are sputtered in sequence and patterned to form a plurality of data lines **171**, each including a plurality of source electrodes **173** and an expansion **179**, and a plurality of drain electrodes **175**. The lower conductive film is preferably made of Cr, Mo, or Mo alloy, and the upper conductive film is preferably made of Al containing metal or Ag containing metal. In FIGS. **6A** and **6B**, the lower and the upper films of the drain electrodes **171** are indicated by reference numerals **711** and **712**, respectively, the lower and the upper films of the source electrodes **173** are indicated by reference numerals **731** and **732**, respectively, the lower and the upper films of the drain electrodes **175** are indicated by reference numerals **751** and **752**, respectively, and the lower and the upper films of the end portions **179** of the data lines **171** are indicated by reference numerals **791** and **792**, respectively.

Thereafter, portions of the extrinsic semiconductor stripes, which are not covered with the data lines **171** and the drain electrodes **175**, are removed to complete a plurality of ohmic contact stripes **161** including a plurality of projections **163** and a plurality of ohmic contact islands **165** and to expose portions of the intrinsic semiconductor stripes **151**. Oxygen plasma treatment preferably follows in order to stabilize the exposed surfaces of the semiconductor stripes **151**.

Referring to FIGS. **1**, **7A** and **7B**, a passivation layer **180** made of a photosensitive organic insulator is coated and exposed through a photo-mask **500** having a plurality of transmissive areas **502** and a plurality of slit areas **501** disposed around the transmissive areas **502**. Accordingly, portions of the passivation layer **180** facing the transmissive areas **502** absorb the full energy of the light, while portions of the passivation layer **180** facing the slit areas **501** partially absorb the light energy. The passivation layer **180** is then developed to form a plurality of contact holes **181b** and **183b** exposing portions of the drain electrodes **175** and portions of the expansions **179** of the data lines **171**, respectively, and to form upper portions of a plurality of contact holes **182b** exposing portions of the gate insulating layer **140** disposed on the expansions **125** of the gate lines **121**. Since the portions of the passivation layer **180** facing the transmissive areas **502** are removed to its full thickness, while the portions facing the slit areas **501** remain to have reduced thickness, sidewalls **181a**, **182a** and **183a** of the contact holes **181b**, **182b** and **183b** have stepped profiles.

After removing the exposed portions of the gate insulating layer **140** to expose the underlying portions of the expansions **125** of the gate insulating layer **140**, the exposed portions of the upper conductive films **752**, **792** and **252** of the drain electrodes **175**, the expansions **179** of the data lines **171**, and the expansions **125** of the gate lines **121** are removed to expose underlying portions of the lower conductive films **751**, **791** and **251** of the drain electrodes **175**, the expansions **179** of the data lines **171**, and the expansions **125** of the gate lines **121**.

Finally, a plurality of pixel electrodes **190** and a plurality of contact assistants **92** is and **97** are formed on the passivation layer **180** and on the exposed portions of the lower conductive films **751**, **791** and **251** of the drain electrodes **175**, the expansions **125** of the gate lines **121**, and the expansions **179** of the

data lines **171** by sputtering and photo-etching an IZO or ITO layer with thickness of about 400-500 Å as shown in FIGS. **1**, **4** and **5**.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. **8-10**.

FIG. **8** is a layout view of an LCD according to another embodiment of the present invention, FIG. **9** is a sectional view of the LCD shown in FIG. **8** taken along the line IX-IV', and FIG. **10** is a sectional view of the LCD shown in FIG. **8** taken along the lines X-X' and X'-X''.

Referring to FIGS. **8-10**, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer **3** interposed therebetween.

Layered structures of the panels according to this embodiment are almost the same as those shown in FIGS. **1-5**.

Regarding the TFT array panel, a plurality of gate lines **121** including a plurality of gate electrodes **123** and a plurality of storage electrode lines **131** including a plurality of storage electrodes **133** are formed on a substrate **110**, and a gate insulating layer **140**, a plurality of semiconductor stripes **151** including a plurality of projections **154**, and a plurality of ohmic contact stripes **161** including a plurality of projections **163** and a plurality of ohmic contact islands **165** are sequentially formed thereon. A plurality of data lines **171** including a plurality of source electrodes **173** and a plurality of drain electrodes **175** are formed on the ohmic contacts **161** and **165**, and a passivation layer **180** is formed thereon. A plurality of contact holes **181b**, **182b** and **183b** are provided at the passivation layer **180** and the gate insulating layer **140**, and a plurality of pixel electrodes **190** and a plurality of contact assistants **95** and **97** are formed on the passivation layer **180**.

Regarding the common electrode panel, a light blocking member **220**, a plurality of color filters **230**, an overcoat **250**, and a common electrode **270** are formed on an insulating substrate **210**.

Different from the LCD shown in FIGS. **1-5**, the semiconductor stripes **151** have almost the same planar shapes as the data lines **171** and the drain electrodes **175** as well as the underlying ohmic contacts **161** and **165**. However, the projections **154** of the semiconductor stripes **151** include some exposed portions, which are not covered with the data lines **171** and the drain electrodes **175**, such as portions located between the source electrodes **173** and the drain electrodes **175**.

Many of the above-described features of the LCD shown in FIGS. **1-5** may be appropriate to the LCD shown in FIGS. **8-10**.

Now, a method of manufacturing the TFT array panel shown in FIGS. **8-10** according to an embodiment of the present invention will be described in detail.

FIGS. **11A** and **11B** are sectional views of the TFT array panel shown in FIG. **8-10** taken along the line IX-IX' and the lines X-X' and X'-X'', respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention; FIGS. **12A** and **12B** are sectional views of the TFT array panel shown in FIG. **8-10** taken along the line IX-IX' and the lines X-X' and X'-X'' in the step of the manufacturing method following the step shown in FIGS. **11A** and **11B**; and FIGS. **13A** and **13B** are sectional views of the TFT array panel shown in FIG. **8-10** taken along the line IX-IX' and the lines X-X' and X'-X'' in the step of the manufacturing method following the step shown in FIGS. **12A** and **12B**.

Referring to FIGS. **11A** and **11B**, two conductive films, a lower conductive film and an upper conductive film are sputtered in sequence on an insulating substrate **110** and they are

wet or dry etched in sequence to form a plurality of gate lines **121**, each including a plurality of gate electrodes **123** and an expansion **125**, and a plurality of storage electrode lines **131** including a plurality of storage electrodes **133**. In FIGS. **11A** and **11B**, the lower and the upper films of the gate electrodes **123** are indicated by reference numerals **231** and **232**, respectively, the lower and the upper films of the expansions **125** are indicated by reference numerals **251** and **252**, respectively, and the lower and the upper films of the storage electrodes **133** are indicated by reference numerals **331** and **332**, respectively.

Next, a gate insulating layer **140**, an intrinsic a-Si layer **150**, and an extrinsic a-Si layer **160** are sequentially deposited by CVD such that the layers **140**, **150** and **160** bear thickness of about 1,500-5,000 Å, about 500-2,000 Å and about 300-600 Å, respectively. A conductive layer **170** including a lower film **701** and an upper film **702** is deposited by sputtering, and a photoresist film with the thickness of about 1-2 microns is coated on the conductive layer **170**.

The photoresist film is exposed to light through an exposure mask **600** including slit areas **601**, and developed such that the developed photoresist PR has a position dependent thickness. The photoresist shown in FIGS. **11A** and **11B** includes a plurality of first to third portions with decreased thickness. The first portions are located on first areas (referred to as "wire areas" hereinafter) and the second portions are located on second areas (referred to as "channel areas" hereinafter), respectively, while the third portions located on remaining third areas are not illustrated in the figures since they have substantially zero thickness to expose underlying portions of the conductive layer **170**.

The different thickness of the photoresist PR enables to selectively etch the underlying layers when using suitable process conditions. Therefore, a plurality of data lines **171** including a plurality of source electrodes **173**, and a plurality of drain electrodes **175** as well as a plurality of ohmic contact stripes **161** including a plurality of projections **163**, a plurality of ohmic contact islands **165** and a plurality of semiconductor stripes **151** including a plurality of projections **154** are obtained by a series of etching steps as shown in FIGS. **12A** and **12B**. In FIGS. **12A** and **12B**, the lower and the upper films of the drain electrodes **171** are indicated by reference numerals **711** and **712**, respectively, the lower and the upper films of the source electrodes **173** are indicated by reference numerals **731** and **732**, respectively, the lower and the upper films of the drain electrodes **175** are indicated by reference numerals **751** and **752**, respectively, and the lower and the upper films of the end portions **179** of the data lines **171** are indicated by reference numerals **791** and **792**, respectively.

For descriptive purpose, portions of the conductive layer **170**, the extrinsic a-Si layer **160**, and the intrinsic a-Si layer **150** on the wire areas are called first portions, portions of the conductive layer **170**, the extrinsic a-Si layer **160**, and the intrinsic a-Si layer **150** on the channel areas are called second portions, and portions of the conductive layer **170**, the extrinsic a-Si layer **160**, and the intrinsic a-Si layer **150** on the third areas are called third portions.

An exemplary sequence of forming such a structure is as follows:

- (1) Removal of third portions of the conductive layer **170**, the extrinsic a-Si layer **160** and the intrinsic a-Si layer **150** on the wire areas;
- (2) Removal of the second portions of the photoresist;
- (3) Removal of the second portions of the conductive layer **170** and the extrinsic a-Si layer **160** on the channel areas; and
- (4) Removal of the first portions of the photoresist.

Another exemplary sequence is as follows:

- (1) Removal of the third portions of the conductive layer **170**;
- (2) Removal of the second portions of the photoresist;
- (3) Removal of the third portions of the extrinsic a-Si layer **160** and the intrinsic a-Si layer **150**;
- (4) Removal of the second portions of the conductive layer **170**;
- (5) Removal of the first portions of the photoresist; and
- (6) Removal of the second portions of the extrinsic a-Si layer **160**.

The first example is described in detail.

At first, the exposed third portions of the conductive layer **170** on the third areas are removed by wet etching or dry etching to expose the underlying third portions of the extrinsic a-Si layer **160**. The dry etching may etch out the top portions of the photoresist PR.

Next, the third portions of the extrinsic a-Si layer **160** on the third areas and of the intrinsic a-Si layer **150** are removed preferably by dry etching and the second portions of the photoresist PR are removed to expose the second portions of the conductors **170**. The removal of the second portions of the photoresist PR are performed either simultaneously with or independent from the removal of the third portions of the extrinsic a-Si layer **160** and of the intrinsic a-Si layer **150**. A gas mixture of SF<sub>6</sub> and HCl or a gas mixture of SF<sub>6</sub> and O<sub>2</sub> can etch the a-Si layers **150** and **160** and the photoresist PR by nearly the same etching ratio. Residue of the second portions of the photoresist PR remained on the channel areas is removed by ashing.

Next, the third portions of the extrinsic a-Si layer **160** on the third areas and of the intrinsic a-Si layer **150** are removed preferably by dry etching and the second portions of the photoresist PR are removed to expose the second portions of the conductors **170**. The removal of the second portions of the photoresist PR are performed either simultaneously with or independent from the removal of the third portions of the extrinsic a-Si layer **160** and of the intrinsic a-Si layer **150**. A gas mixture of SF<sub>6</sub> and HCl or a gas mixture of SF<sub>6</sub> and O<sub>2</sub> can etch the a-Si layers **150** and **160** and the photoresist PR by nearly the same etching ratio. Residue of the second portions of the photoresist PR remained on the channel areas is removed by ashing.

The semiconductor stripes **151** are completed in this step.

Next, the second portions of the conductors **170** and the extrinsic a-Si layer **160** on the channel areas as well as the first portion of the photoresist PR are removed.

Both the conductors **170** and the extrinsic a-Si layer **160** may be dry etched.

Alternatively, the conductors **170** are wet etched, while the extrinsic a-Si layer **160** is dry etched. Since the wet etch etches out lateral sides of the conductors **170**, while the dry etch hardly etch out lateral sides of the extrinsic a-Si layer **160**, step-wise lateral profiles are obtained. Examples of the gas mixtures are CF<sub>4</sub> and HCl and CF<sub>4</sub> and O<sub>2</sub>, as described above. The latter gas mixture leaves uniform thickness of the intrinsic semiconductor stripes **151**.

In this way, each conductor **170** is divided into a data line **171** and a plurality of drain electrodes **175** to be completed, and the extrinsic a-Si layer **160** is divided into an ohmic contact stripe **161** and a plurality of ohmic contact islands **165** to be completed.

Referring to FIGS. **13A** and **13B**, a passivation layer **180** made of a photosensitive organic insulator is coated and exposed through a photo-mask **900** having a plurality of transmissive areas **902** and a plurality of slit areas **901** disposed around the transmissive areas **902**. Accordingly, por-

tions of the passivation layer **180** facing the transmissive areas **902** absorb the full energy of the light, while portions of the passivation layer **180** facing the slit areas **901** partially absorb the light energy. The passivation layer **180** is then developed to form a plurality of contact holes **181b** and **183b** exposing portions of the drain electrodes **175** and portions of the expansions **179** of the data lines **171**, respectively, and to form upper portions of a plurality of contact holes **182b** exposing portions of the gate insulating layer **140** disposed on the expansions **125** of the gate lines **121**. Since the portions of the passivation layer **180** facing the transmissive areas **902** are removed to its full thickness, while the portions facing the slit areas **901** remain to have reduced thickness, sidewalls **181a**, **182a** and **183a** of the contact holes **181b**, **182b** and **183b** have stepped profiles.

After removing the exposed portions of the gate insulating layer **140** to expose the underlying portions of the expansions **125** of the gate insulating layer **140**, the exposed portions of the upper conductive films **752**, **792** and **252** of the drain electrodes **175**, the expansions **179** of the data lines **171**, and the expansions **125** of the gate lines **121** are removed to expose underlying portions of the lower conductive films **751**, **791** and **251** of the drain electrodes **175**, the expansions **179** of the data lines **171**, and the expansions **125** of the gate lines **121**.

The passivation layer **180** may be made of a photo-insensitive organic insulator or inorganic insulator having a low dielectric constant less than 4. In this case, an additional etching step for forming the contact holes **181b**, **182b** and **183b** is required.

Finally, a plurality of pixel electrodes **190** and a plurality of contact assistants **92** and **97** are formed on the passivation layer **180** and on the exposed portions of the lower conductive films **751**, **791** and **251** of the drain electrodes **175**, the expansions **125** of the gate lines **121**, and the expansions **179** of the data lines **171** by sputtering and photo-etching an IZO or ITO film with thickness of about 400-500 Å as shown in FIGS. **8-10**.

The etching of the IZO film may include wet etching using a Cr etchant such as  $\text{HNO}_3/(\text{NH}_4)_2\text{Ce}(\text{NO}_3)_6/\text{H}_2\text{O}$ , which does not erode the exposed Al portions of the drain electrodes **175**, the gate lines **121**, and the data lines **171** through the contact holes **181b**, **182b** and **183b**. A preferred deposition temperature for minimizing the contact resistance ranges from room temperature to about 200° C. A sputtering target for depositing IZO preferably includes  $\text{In}_2\text{O}_3$  and ZnO and the content of ZnO is preferably in a range about 15-20 atomic %.

Nitrogen, which can prevent the formation of metal oxides on the exposed portions of the drain electrodes **175**, the gate lines **121**, and the data lines **171** through the contact holes **181b**, **182b** and **183b**, is preferably used for a pre-heating process before the deposition of the ITO film or the IZO film.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. **14-16**.

FIG. **14** is a layout view of an LCD according to another embodiment of the present invention, FIG. **15** is a sectional view of the LCD shown in FIG. **14** taken along the line XV-XV', and FIG. **16** is a sectional view of the LCD shown in FIG. **14** taken along the lines XVI-XVI' and XVI'-XVI''.

Referring to FIGS. **14-16**, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer **3** interposed therebetween.

Regarding a TFT array panel, a plurality of gate lines **121** including a plurality of gate electrodes **123** and a plurality of storage electrode lines **131** including a plurality of storage electrodes **133** are formed on a substrate **110**, and a gate insulating layer **140**, a plurality of semiconductor stripes **151**

including a plurality of projections **154**, and a plurality of ohmic contact stripes **161** including a plurality of projections **163** and a plurality of ohmic contact islands **165** are sequentially formed thereon. A plurality of data lines **171** including a plurality of source electrodes **173** and a plurality of drain electrodes **175** are formed on the ohmic contacts **161** and **165** and the gate insulating layer **140**.

A first passivation layer **801** preferably made of inorganic insulator such as  $\text{SiN}_x$  is formed on the data lines **171** and the drain electrodes **175**.

A plurality of red, green and blue color filters **230R**, **230G** and **230B** is formed on the first passivation layer **801** and they are disposed substantially between the data lines **171**. The color filters **230R**, **230G** or **230B** in adjacent two data lines **171** and arranged in the longitudinal direction may be connected to each other to form a periodically-curved stripe. The neighboring color filters **230R**, **230G** and **230B** overlap each other on the data lines **171** to form hills. The color filters **230R**, **230G** and **230B** have a plurality of openings disposed on the drain electrodes **175** and are not provided on a peripheral area which is provided with the expansions **125** and **179** of the gate lines **121** and the data lines **179**.

A second passivation layer **802** preferably made of photo-sensitive organic material is formed on the color filters **230R**, **230G** and **230B**. The second passivation layer **802** also forms hills when running over the hills formed by the color filters **230R**, **230G** and **230B** and the hills of the second passivation layer **802** enhance the control of the tilt directions of LC molecules in the LC layer **3**. The second passivation layer **802** The overcoat **250** prevents the color filters **230** from being exposed through the cutouts **271** of the common electrode **270** to contaminate the LC layer **3** and it may be made of inorganic insulator such as  $\text{SiN}_x$  and  $\text{SiO}_2$ .

The passivation layers **801** and **802** have a plurality of contact holes **181b** and **183b**, and the passivation layers **801** and **802** and the gate insulating layer **140** have a plurality of contact holes **182b**. The openings of the color filters **230R**, **230G** and **230B** expose the contact holes **181b** and a top surface of the first passivation layer **801**.

A plurality of pixel electrodes **190** and a plurality of contact assistants **95** and **97** are formed on the second passivation layer **802**.

The common electrode panel includes a light blocking member **220** and a common electrode **270** formed on an insulating substrate **210**. Comparing the common electrode panel shown in FIGS. **2**, **4** and **5**, the common electrode panel shown in FIGS. **14-16** has no color filter and no overcoat.

Since the color filters **230R**, **230G** and **230B** and the pixel electrodes **190** are provided on the TFT array panel, the LCD shown in FIGS. **14-16** may have a large alignment margin for aligning the TFT array panel and the common electrode panel.

A TFT array panel shown in FIGS. **14-16** may be manufactured by depositing a first passivation layer **801**, forming a plurality of red, green, and blue color filters **230R**, **230G**, and **230B**, coating a second passivation layer **802** made of a photosensitive organic layer, exposing and developing the passivation layer **802** to form upper portions of a plurality of contact holes **181b**, **182b** and **183b**, removing exposed portions of the first passivation layer **801** and the gate insulating layer **140** to form lower portions of the contact holes **181b**, **182b** and **183b**, and forming a plurality of pixel electrodes **190** and a plurality of contact assistants **95** and **97**, after forming the gate lines **121**, the storage electrode lines **131**, the gate insulating layer **140**, the semiconductor stripes **151**, the ohmic contacts **161** and **165**, the data lines **171**, and the drain electrodes **175** as described above with reference to FIGS. **6A-7B**. The formation of the color filters **230R**, **230G**, and **230B** includes thrice repetitions of coating, exposing, and developing a photosensitive film including a colored pigment.

Many of the above-described features of the LCD shown in FIGS. 1-5 may be appropriate to the LCD shown in FIGS. 14-16.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 17-19.

FIG. 17 is a layout view of an LCD according to another embodiment of the present invention, FIG. 18 is a sectional view of the LCD shown in FIG. 17 taken along the line XVIII-XVIII', and FIG. 19 is a sectional view of the LCD shown in FIG. 17 taken along the lines XIX-XIX' and XIX'-XIX''.

Referring to FIGS. 17-19, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Layered structures of the panels according to this embodiment are almost the same as those shown in FIGS. 14-16.

Concerning the TFT array panel, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a first passivation layer 801 is formed thereon. A plurality of red, green and blue color filters 230 are formed on the first passivation layer 801 and a second passivation layer 802 is formed thereon. A plurality of contact holes 181b, 182b and 183b are provided at the first and the second passivation layers 801 and 802 and the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the second passivation layer 802.

Concerning the common electrode panel, a light blocking member 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in FIGS. 14-16, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165. However, the projections 154 of the semiconductor stripes 151 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175 such as portions located between the source electrodes 173 and the drain electrodes 175.

A TFT array panel shown in FIGS. 17-19 may be manufactured by forming a first passivation layer 801, a plurality of red, green, and blue color filters 230R, 230G, and 230B, a second passivation layer 802, a plurality of pixel electrodes 190, and a plurality of contact assistants 95 and 97 based on the steps described with reference to FIGS. 14-16, after forming the gate lines 121, the storage electrode lines 131, the gate insulating layer 140, the semiconductor stripes 151, the ohmic contacts 161 and 165, the data lines 171, and the drain electrodes 175 based on the steps described with reference to FIGS. 11A-13B.

Many of the above-described features of the LCD shown in FIGS. 14-16 may cover the LCD shown in FIGS. 17-19.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 20 and 21.

FIGS. 20 and 21 are sectional views of an LCD according to another embodiment of the present invention, which have a similar layout as the LCD shown in FIG. 14.

Referring to FIGS. 20 and 21, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Layered structures of the panels according to this embodiment are almost the same as those shown in FIGS. 15 and 16.

Concerning the TFT array panel, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of red, green and blue color filters 230R, 230G, and 230B are formed on the passivation layer 801 and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the second passivation layer 802. A plurality of contact holes 181b, 182b and 183b are provided at the passivation layer 180 and the gate insulating layer 140.

Concerning the common electrode panel, a light blocking member 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in FIGS. 14-16, there is no additional passivation layer on the color filters 230R, 230G, and 230B. Accordingly, lateral surfaces of openings of the color filters 230R, 230G, and 230B exposing the contact holes 181b serve as upper portions of sidewalls 181a of the contact holes 181b to smooth the profiles thereof as shown in FIG. 20. This structure is preferable when the color filters 230R, 230G and 230B do not discharge impurities such as pigment.

Many of the above-described features of the LCD shown in FIGS. 14-16 may cover the LCD shown in FIGS. 20-21.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 22 and 23.

FIGS. 22 and 23 are sectional views of an LCD according to another embodiment of the present invention, which have a similar layout as the LCD shown in FIG. 17.

Referring to FIGS. 22 and 23, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Layered structures of the panels according to this embodiment are almost the same as those shown in FIGS. 20 and 21.

Concerning the TFT array panel, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of red, green and blue color filters 230 are formed on the passivation layer 180. A plurality of contact holes 181b, 182b and 183b are provided at the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the passivation layer 180.

Concerning the common electrode panel, a light blocking member 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in FIGS. 20 and 21, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165. However, the projections 154 of the semiconductor stripes 151 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175 such as portions located between the source electrodes 173 and the drain electrodes 175.

Many of the above-described features of the LCD shown in FIGS. 20 and 21 may cover the LCD shown in FIGS. 22 and 23.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 24 and 25.

FIGS. 24 and 25 are sectional views of an LCD according to another embodiment of the present invention, which have a similar layout as the LCD shown in FIG. 14.

Referring to FIGS. 24 and 25, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Layered structures of the panels according to this embodiment are almost the same as those shown in FIGS. 20 and 21.

Concerning the TFT array panel, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of red, green and blue color filters 230R, 230G, and 230B are formed on the passivation layer 801 and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the second passivation layer 802. A plurality of contact holes 181b, 182b and 183b are provided at the passivation layer 180 and the gate insulating layer 140.

Concerning the common electrode panel, a light blocking member 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in FIGS. 20 and 21, the color filters 230R, 230G or 230B are also disposed on a peripheral area which is provided with expansions 125 and 179 of the gate lines 121 and the data lines 179. Although FIG. 25 shows that a red color filter 230R is disposed on the peripheral area, any one or more of the red, green and blue color filters 230G and 230B may be provided on the peripheral area. In addition, the color filters 230R, 230G, and 230B have a plurality of openings forming upper portions of sidewalls 181a, 182a and 183a of the contact holes 181b, 182b and 183b. Accordingly, lateral surfaces of the openings of the color filters 230R, 230G, and 230B are smoothly connected to the lateral surfaces of the contact holes 181b, 182b and 183b at the passivation layer 180.

A TFT array panel shown in FIGS. 14-16 may be manufactured by depositing a passivation layer 180, forming a plurality of red, green, and blue color filters 230R, 230G, and 230B having openings forming upper portions of a plurality of contact holes 181b, 182b and 183b exposing portions of the passivation layer 180, removing exposed portions of the passivation layer 180 and the gate insulating layer 140 to form lower portions of the contact holes 181b, 182b and 183b, and forming a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97, after forming the gate lines 121, the storage electrode lines 131, the gate insulating layer 140, the semiconductor stripes 151, the ohmic contacts 161 and 165, the data lines 171, and the drain electrodes 175 as described above with reference to FIGS. 6A-7B.

Many of the above-described features of the LCD shown in FIGS. 20 and 21 may cover the LCD shown in FIGS. 24 and 25.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 26 and 27.

FIGS. 26 and 27 are sectional views of an LCD according to another embodiment of the present invention, which have a similar layout as the LCD shown in FIG. 17.

Referring to FIGS. 26 and 27, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Layered structures of the panels according to this embodiment are almost the same as those shown in FIGS. 24 and 25.

Concerning the TFT array panel, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of red, green and blue color filters 230 are formed on the passivation layer 180. A plurality of contact holes 181b, 182b and 183b are provided at the color filters 230R, 230G, and 230B, the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the passivation layer 180.

Concerning the common electrode panel, a light blocking member 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in FIGS. 24 and 25, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165. However, the projections 154 of the semiconductor stripes 151 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175 such as portions located between the source electrodes 173 and the drain electrodes 175.

Many of the above-described features of the LCD shown in FIGS. 24 and 25 may cover the LCD shown in FIGS. 26 and 27.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIG. 28.

FIG. 28 is a layout view of an LCD according to another embodiment of the present invention.

The structure of the LCD according to this embodiment is almost the same as that shown in FIGS. 1-5. Referring to FIG. 28 as well as FIGS. 4 and 5, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Regarding the TFT array panel, a plurality of gate lines 121 including a plurality of gate electrodes 123 and a plurality of storage electrode lines 131 including a plurality of storage electrodes 133 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 181b, 182b and 183b are provided at the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the passivation layer 180.

Regarding the common electrode panel, a light blocking member 220, a plurality of color filters 230, an overcoat 250, and a common electrode 270 having a plurality of cutouts 217 are formed on an insulating substrate 210. Each cutout 271 includes a pair of oblique portions connected to each other and a longitudinal portion connected to one of the oblique portions.

Different from the LCD shown in FIG. 3, the cutouts 271 of the common electrode 270 have no transverse portion.

Many of the above-described features of the LCD shown in FIGS. 1-5 may be appropriate to the LCD shown in FIG. 28.

An LCD according to another embodiment of the present invention will be described in detail with reference to FIG. 29.

FIG. 29 is a layout view of an LCD according to another embodiment of the present invention.

The structure of the LCD according to this embodiment is almost the same as that shown in FIGS. 1-5. Referring to FIG. 29 as well as FIGS. 4 and 5, an LCD according to this embodiment also includes a TFT array panel, a common electrode panel, and a LC layer 3 interposed therebetween.

Regarding the TFT array panel, a plurality of gate lines 121 including a plurality of gate electrodes 123 and a plurality of storage electrode lines 131 including a plurality of storage electrodes 133 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 181*b*, 182*b* and 183*b* are provided at the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 95 and 97 are formed on the passivation layer 180.

Regarding the common electrode panel, a light blocking member 220, a plurality of color filters 230, an overcoat 250, and a common electrode 270 having a plurality of cutouts 217 are formed on an insulating substrate 210. Each cutout 271 includes a pair of oblique portions connected to each other, a transverse edge portion connected to one of the oblique portions, and a longitudinal edge portion connected to the other of the oblique portions.

Different from the LCD shown in FIG. 3, each of the cutouts 271 of the common electrode 270 has a transverse center portion connected to a meeting point of the oblique portions and making an obtuse angle with the oblique portions. In addition, each of the pixel electrodes 190 has a transverse cutout coinciding with the transverse center portion of the common electrode 270. The transverse portions of the pixel electrode 190 and the common electrode 270 assist the domain partitioning.

Many of the above-described features of the LCD shown in FIGS. 1-5 may be appropriate to the LCD shown in FIG. 28.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

The invention claimed is:

1. A liquid crystal display comprising:
  - a first substrate;
  - a gate line disposed on the first substrate;
  - a data line disposed on the first substrate and intersecting the gate line;
  - a pixel electrode disposed on the first substrate;
  - a second substrate comprising at least one region partitioning member having a transverse center portion; and
  - a liquid crystal layer disposed between the first substrate and the second substrate,

wherein the data line, the pixel electrode and the at least one region partitioning member have at least one chamfered portion, respectively, and chamfered portions of the data line, the pixel electrode, and the at least one region partitioning member except for the transverse center portion are substantially parallel to each other.

2. The liquid crystal display of claim 1, wherein a length of the chamfered portions of the data line is about 50% to about 90% of a total length of the data line.

3. The liquid crystal display of claim 2, wherein the region partitioning member is a cutout.

4. The liquid crystal display of claim 3, wherein the liquid crystal layer has negative dielectric anisotropy and is vertically aligned in absence of an electric field.

5. The liquid crystal display of claim 4, wherein the region partitioning member comprises at least one edge parallel to an edge of the gate line.

6. The liquid crystal display of claim 2, wherein the region partitioning member is a protrusion.

7. The liquid crystal display of claim 6, wherein a width of the protrusion is about 5 μm to about 10 μm.

8. The liquid crystal display of claim 6, wherein the liquid crystal layer has negative dielectric anisotropy and is vertically aligned in absence of an electric field.

9. The liquid crystal display of claim 8, wherein a width of the protrusion is about 5 μm to about 10 μm.

10. The liquid crystal display of claim 2, wherein the liquid crystal layer has negative dielectric anisotropy and is vertically aligned in absence of an electric field.

11. The liquid crystal display of claim 1, wherein the region partitioning member is a cutout.

12. The liquid crystal display of claim 11, wherein the liquid crystal layer has negative dielectric anisotropy and is vertically aligned in absence of an electric field.

13. The liquid crystal display of claim 1, wherein the region partitioning member is a protrusion.

14. The liquid crystal display of claim 13, wherein the liquid crystal layer has negative dielectric anisotropy and is vertically aligned in absence of an electric field.

15. The liquid crystal display of claim 14, wherein a width of the protrusion is about 5 μm to about 10 μm.

16. The liquid crystal display of claim 1, wherein the liquid crystal layer has negative dielectric anisotropy and is vertically aligned in absence of an electric field.

17. The liquid crystal display of claim 1, wherein chamfered portion of the data line has an angle of about ±45 degrees with respect to the plurality of gate lines.

18. The liquid crystal display of claim 1, wherein at least one of the plurality of gate lines and the plurality of data lines are formed as a single layer or multilayer.

19. The liquid crystal display of claim 18, wherein at least one of the gate line and the data line has a tapered structure, which has an angle of about 30 degrees to about 80 degrees with respect to a surface of the first substrate.

20. The liquid crystal display of claim 1, further comprising a drain electrode connected to the pixel electrode; and a passivation layer comprising a contact hole connecting the drain electrode and the pixel electrode, wherein the contact hole has a stepwise profile.

\* \* \* \* \*

专利名称(译)	液晶显示器及其薄膜晶体管阵列面板		
公开(公告)号	<a href="#">US8040479</a>	公开(公告)日	2011-10-18
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[标]申请(专利权)人(译)	SONG JANG KUN		
申请(专利权)人(译)	SONG JANG-KUN		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	SONG JANG KUN		
发明人	SONG, JANG-KUN		
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摘要(译)

在基板上形成沿横向延伸的栅极线和与栅极线交叉的数据线。数据线包括弯曲部分和与栅极线基本上成直角交叉的中间部分。像素电极形成在绝缘层上。像素电极连接到薄膜晶体管，并且其具有基本平行于数据线的弯曲部分延伸的边缘。

