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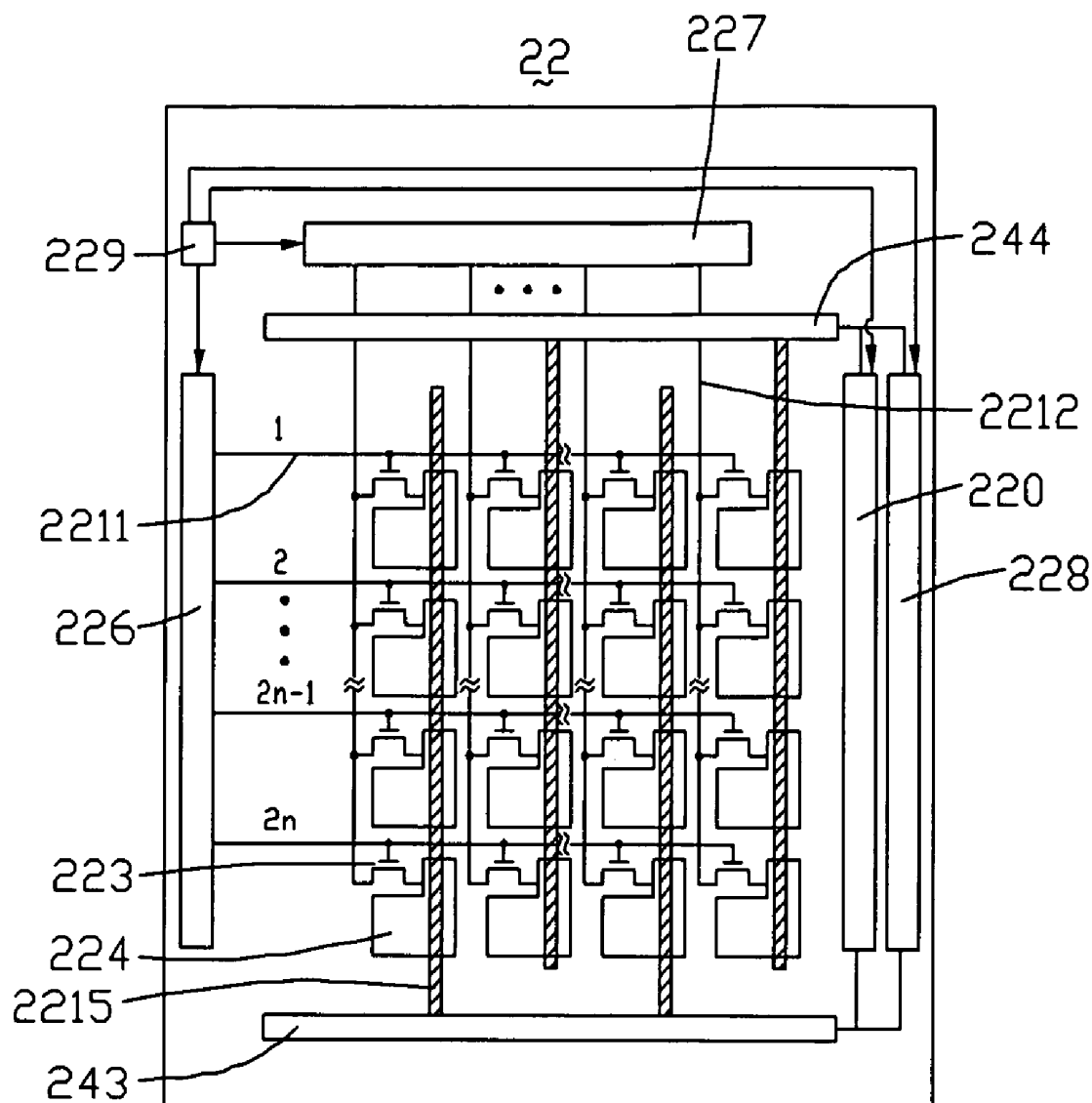
(19) **United States**(12) **Patent Application Publication**
Shie(10) **Pub. No.: US 2008/0180371 A1**(43) **Pub. Date: Jul. 31, 2008**(54) **LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF****Publication Classification**(51) **Int. Cl.**
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(57) **ABSTRACT**(75) **Inventor:** **De-Ching Shie, Miao-Li (TW)**

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An exemplary liquid crystal display (1) includes a first substrate assembly (11), a second substrate assembly (12) parallel to the first substrate assembly (11), a liquid crystal layer (13) sandwiched between the first substrate assembly and the second substrate assembly, and a discharging circuit (120). The first substrate assembly includes common electrodes (110) formed thereat. The common electrodes are parallel to each other. The second substrate assembly includes scanning lines (1211) that are parallel to each other and that each extends along a first direction, and signal lines (1212) that are parallel to each other and that each extends along a second direction orthogonal to the first direction. The discharging circuit is electrically connected with the common electrodes.



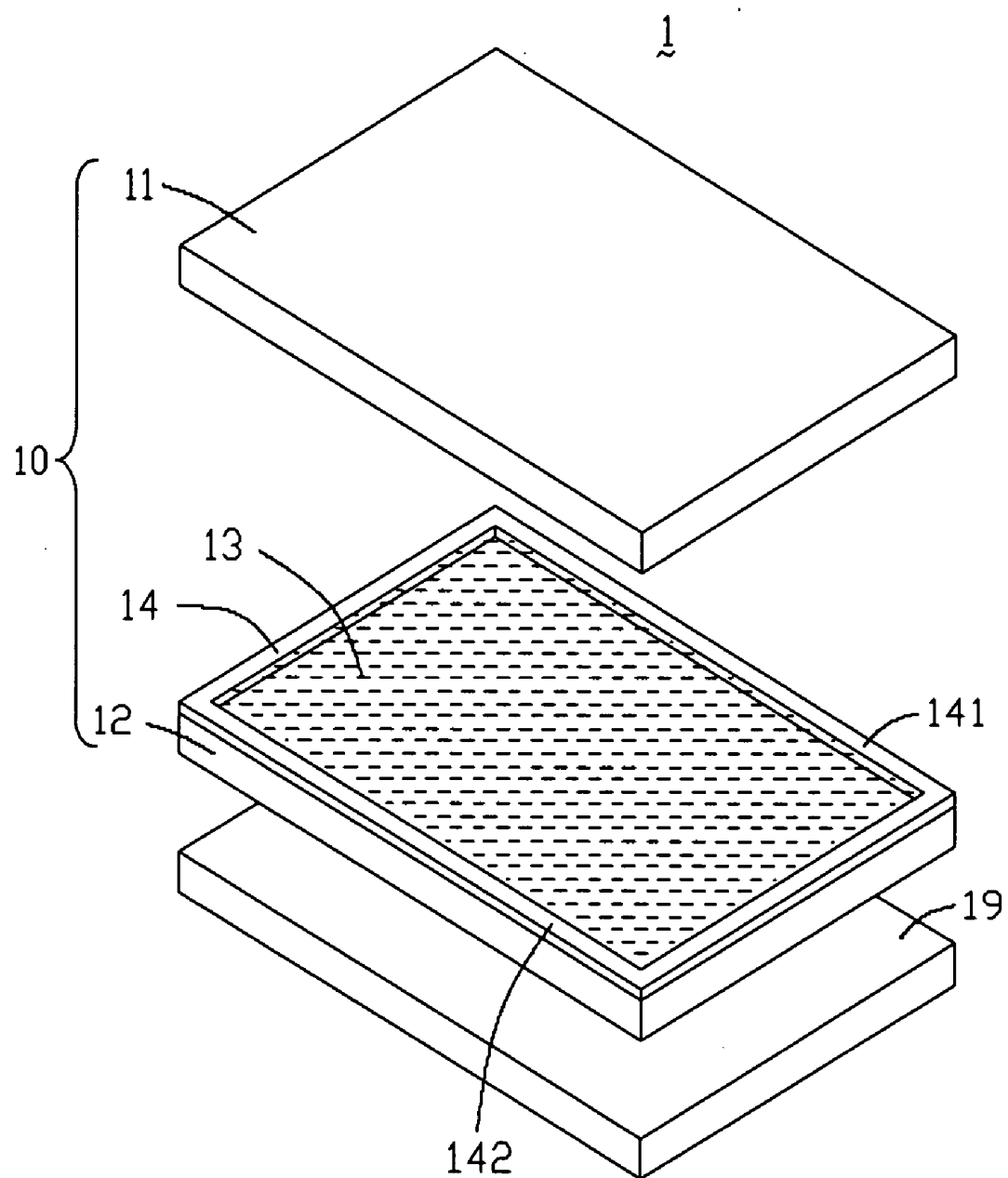


FIG. 1

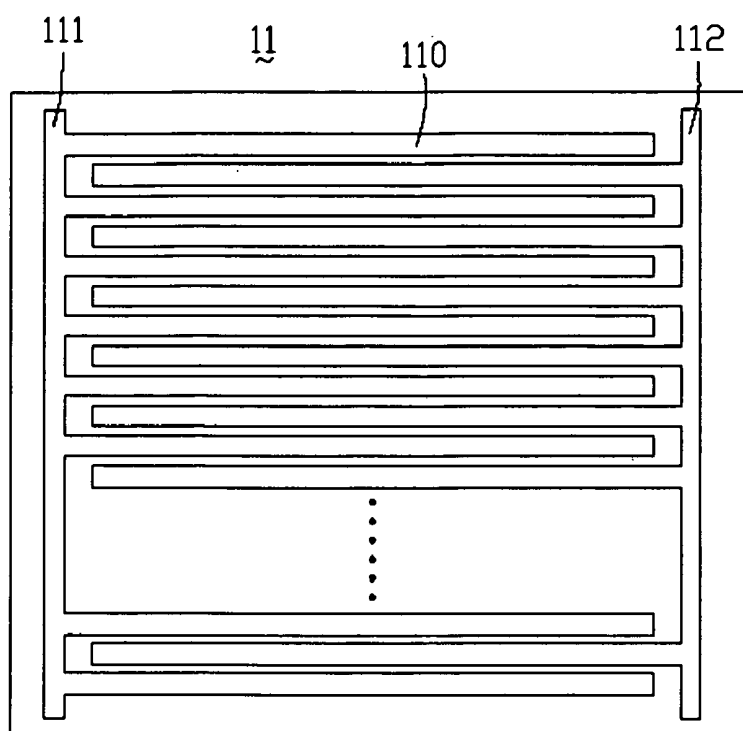


FIG. 2

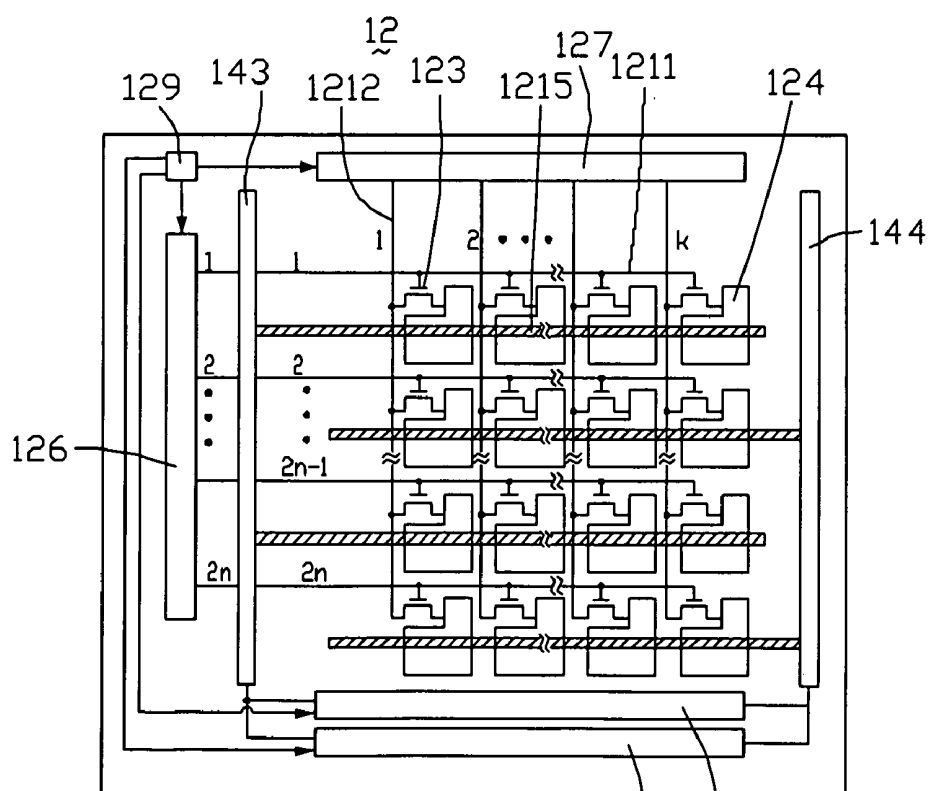


FIG. 3

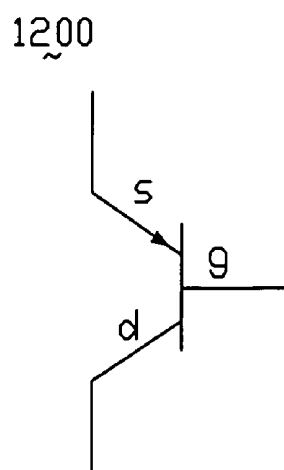


FIG. 4

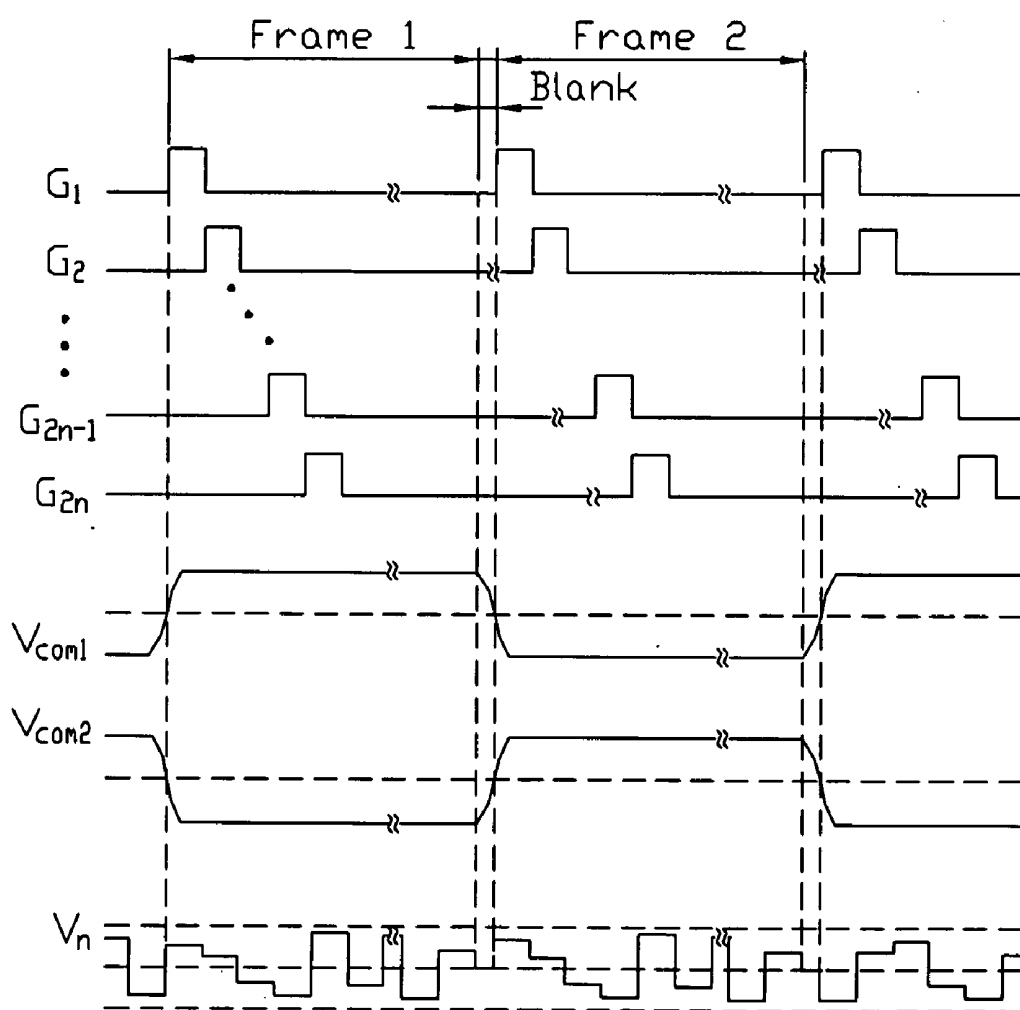


FIG. 5

FIG. 7

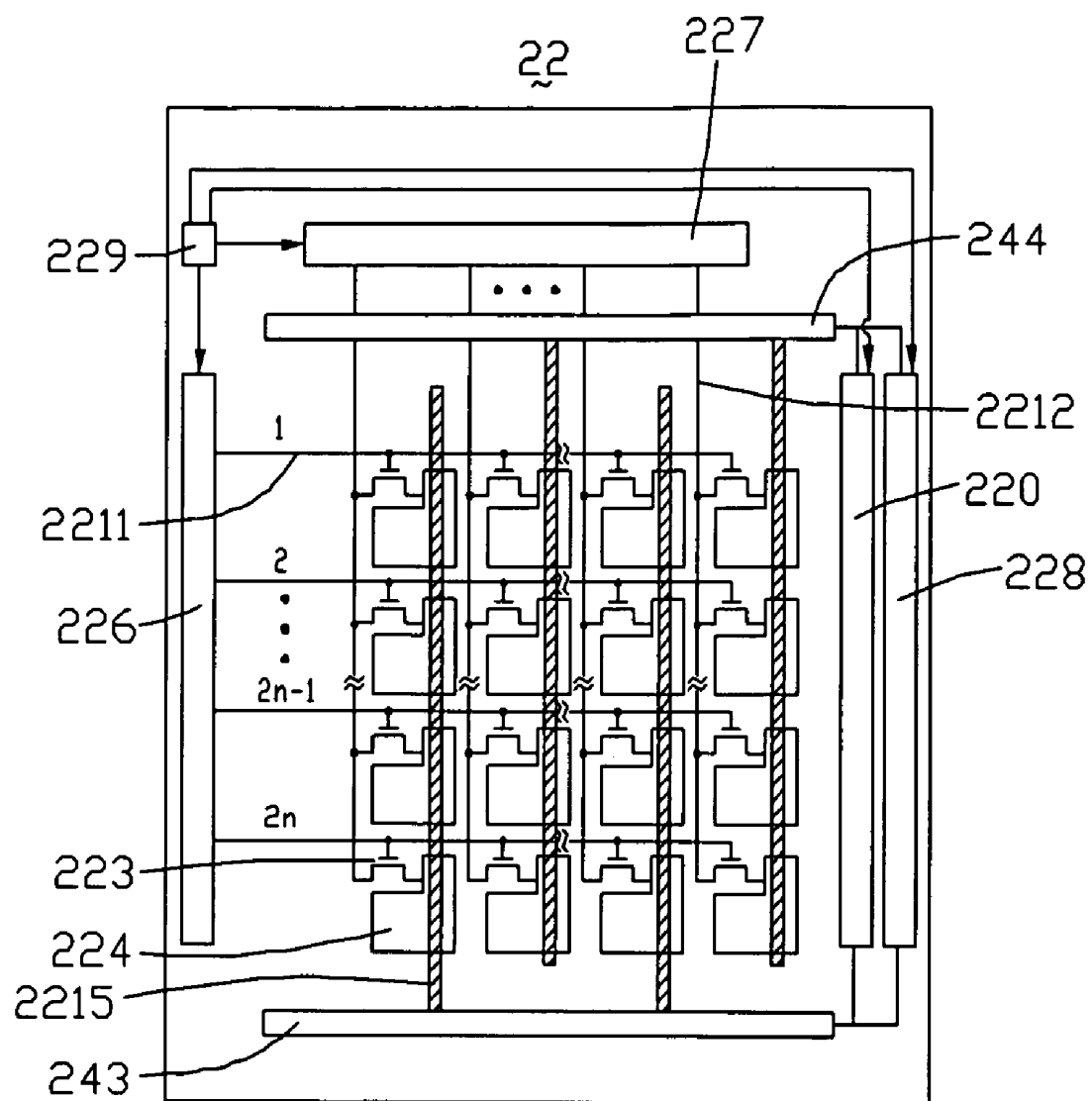


FIG. 8

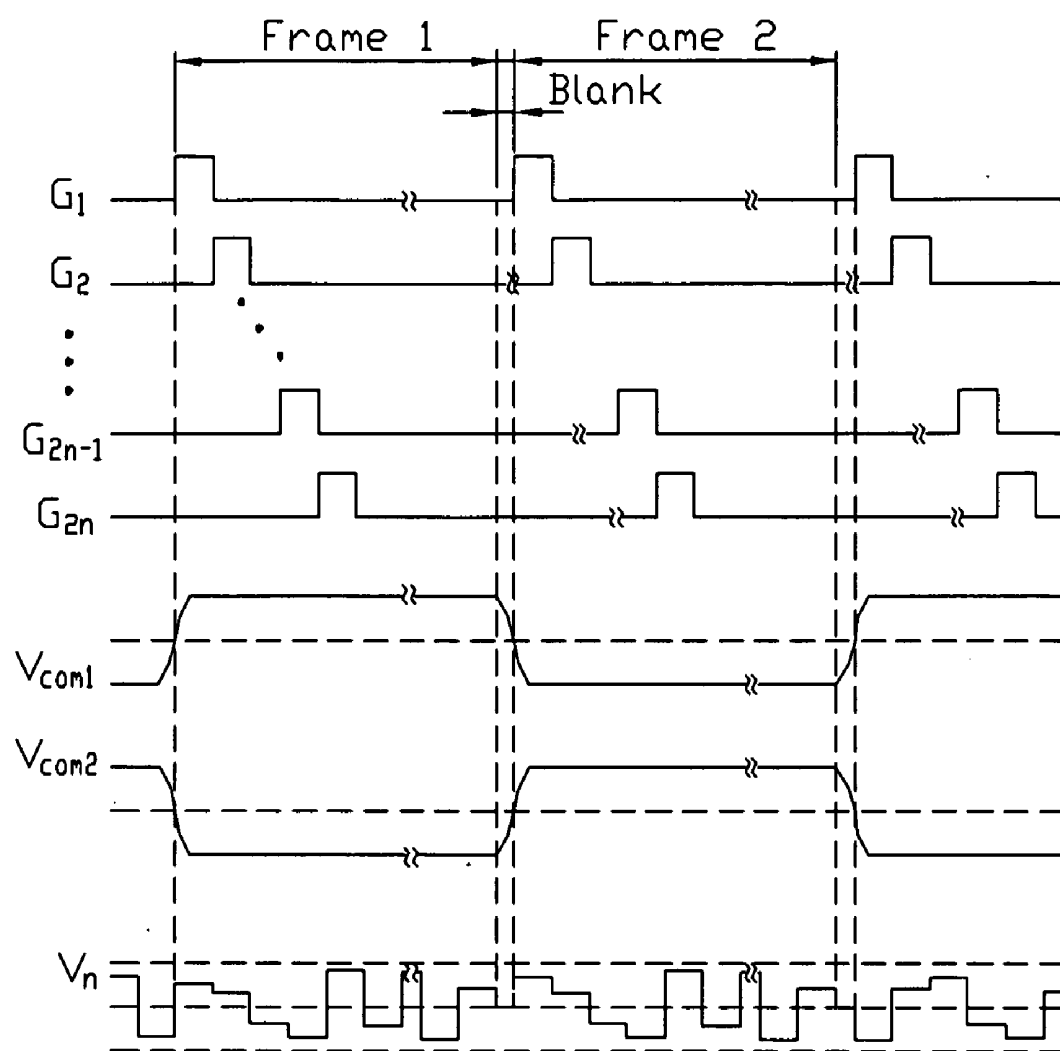


FIG. 9

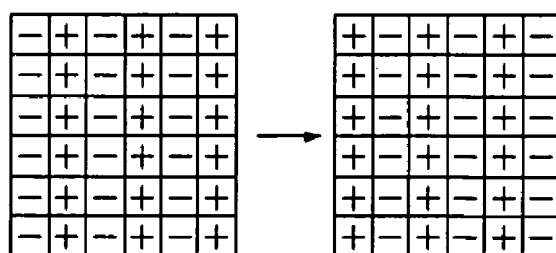


FIG. 10

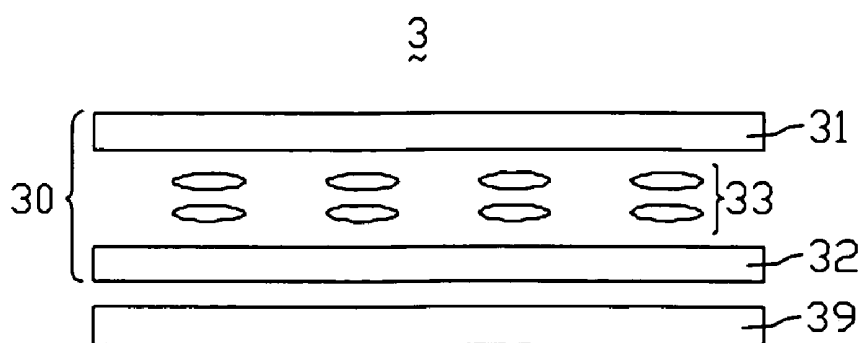


FIG. 11
(RELATED ART)

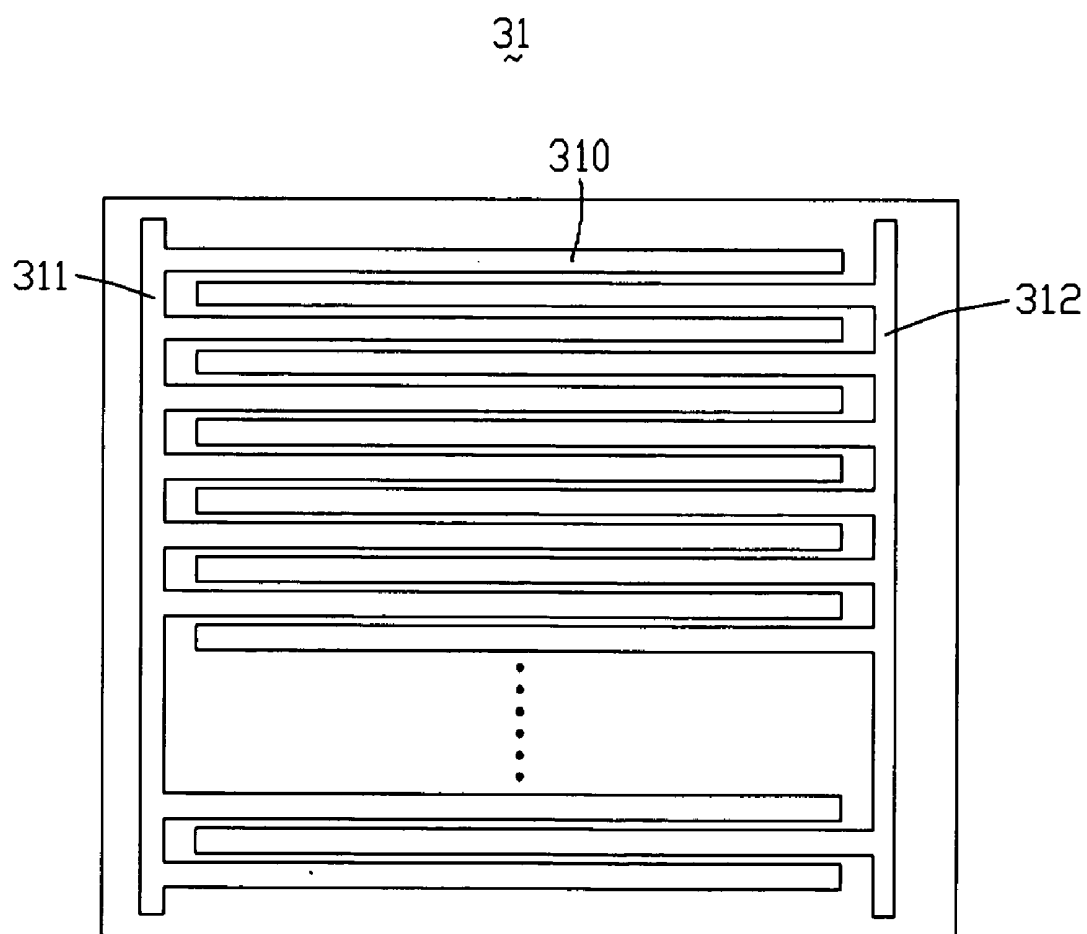


FIG. 12
(RELATED ART)

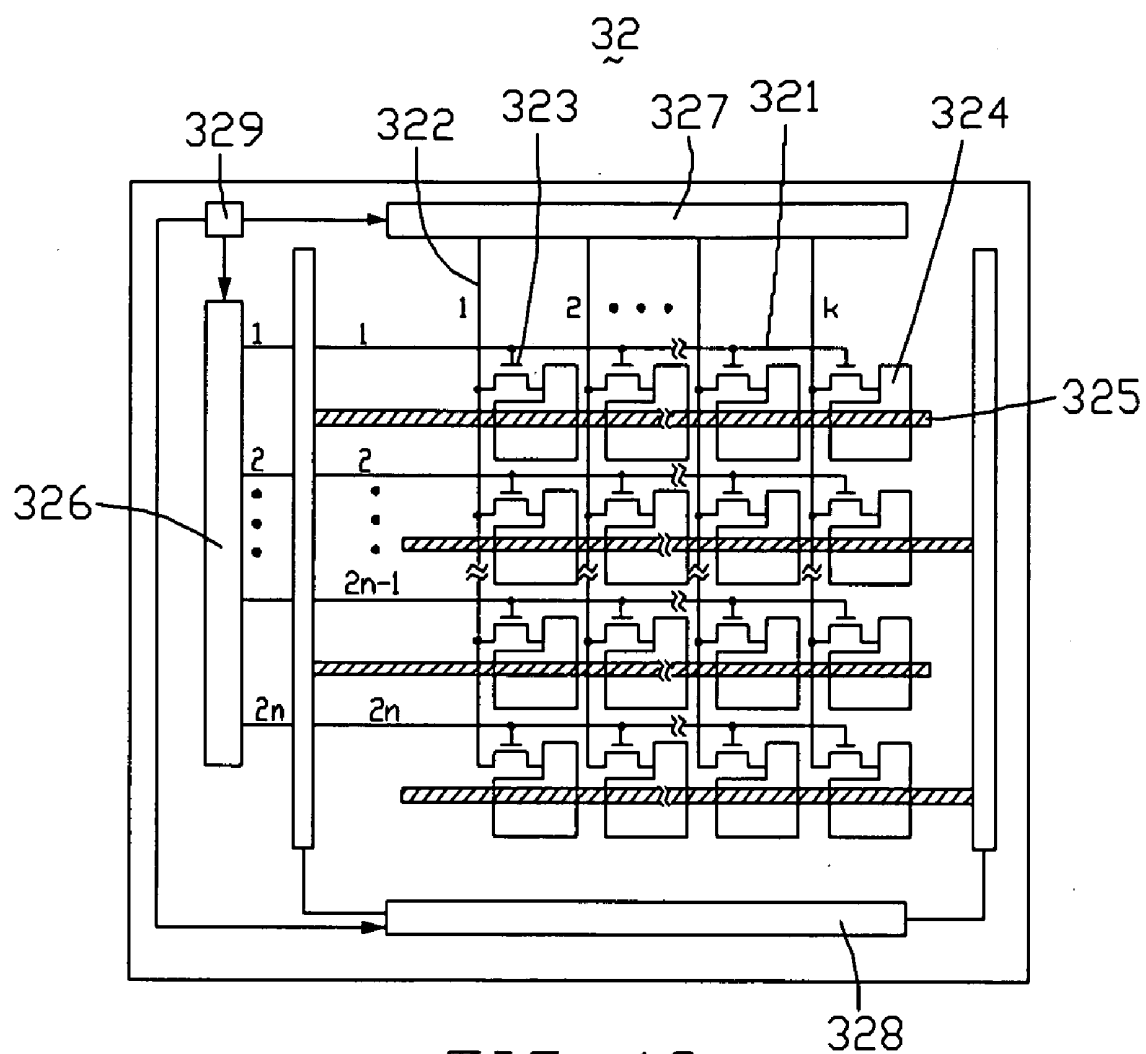


FIG. 13
(RELATED ART)

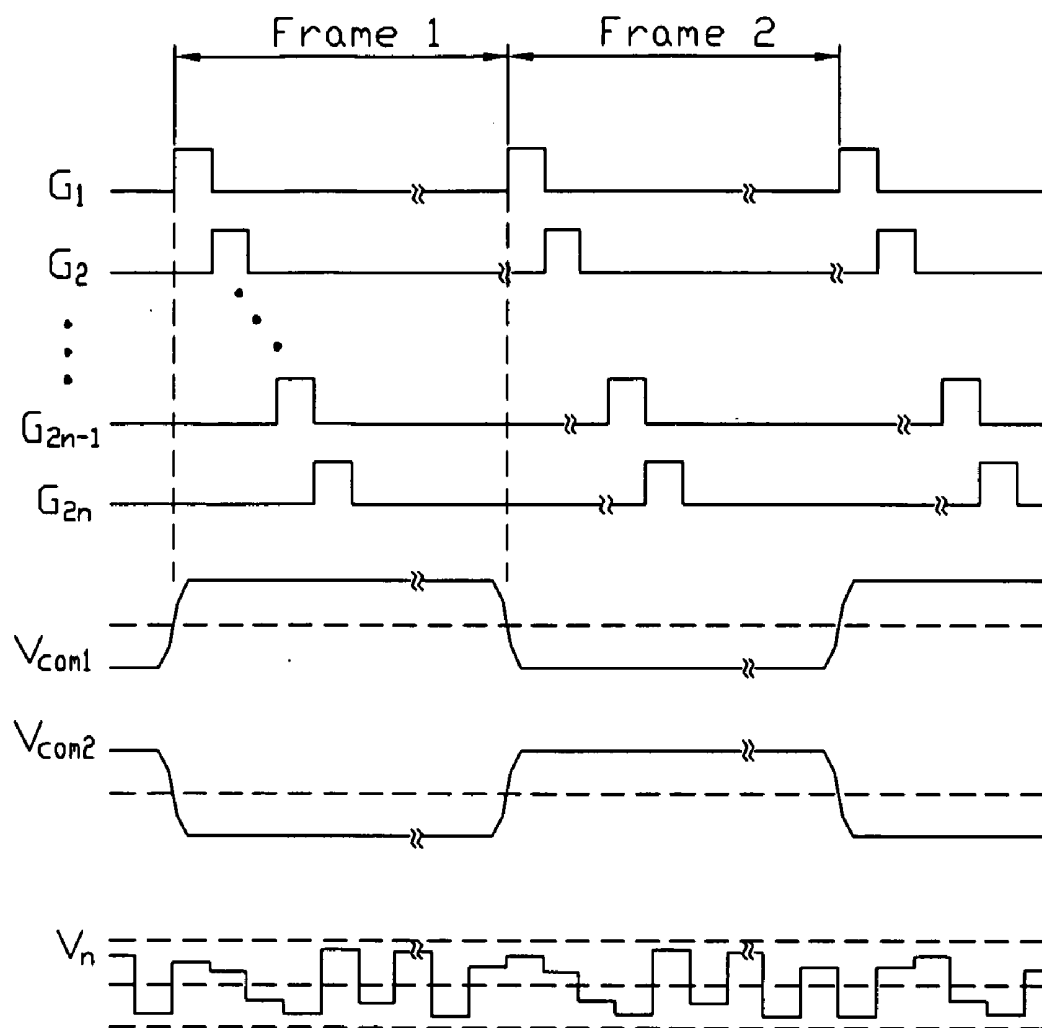


FIG. 14
(RELATED ART)

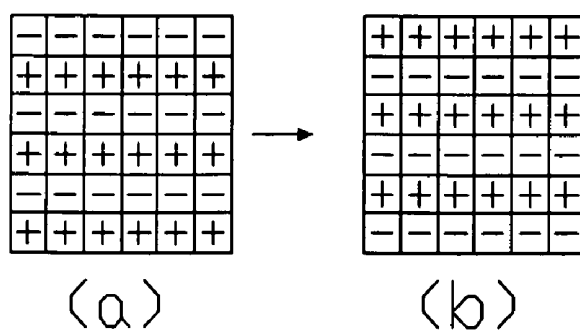


FIG. 15
(RELATED ART)

LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

FIELD OF THE INVENTION

[0001] The present invention relates to liquid crystal displays (LCD), and driving methods of the liquid crystal displays.

BACKGROUND

[0002] Because liquid crystal displays have the advantages of portability, low power consumption, and low radiation, they have been widely used in various portable information products such as notebooks, personal digital assistants (PDAs), video cameras, and the like. Furthermore, liquid crystal displays are considered by many to have the potential to completely replace cathode ray tube (CRT) monitors and televisions.

[0003] Referring to FIG. 1, a typical liquid crystal display 3 is shown. The liquid crystal display 3 includes a liquid crystal panel 30 and a backlight module 39 adjacent to the liquid crystal panel 30. The liquid crystal panel 30 includes a first substrate assembly 31, a second substrate assembly 32 parallel to the first substrate assembly 31, a liquid crystal layer 33 sandwiched between the first substrate assembly 31 and the second substrate assembly 32.

[0004] Referring to FIG. 12, the first substrate assembly 31 includes a plurality of parallel strip-shaped common electrodes 310 at an inner surface thereof, which are made from indium tin oxide (ITO). Odd-numbered common electrodes 310 are electrically connected with a first common electrode bus line 311. Even-numbered common electrodes 310 are electrically connected with a second common electrode bus line 312.

[0005] Referring to FIG. 13, the second substrate assembly 32 includes a number $2n$ (where n is a natural number) of scanning lines 321 that are parallel to each other and that each extend along a first direction, and a number k (where k is also a natural number) of signal lines 322 that are parallel to each other and that each extend along a second direction orthogonal to the first direction, a number $2n$ of common electrode lines 325 that are parallel to each other and that each extend along the first direction, and a plurality of thin film transistors (TFTs) 323 that function as switching elements. Each thin film transistor 323 is provided in the vicinity of a respective point of intersection of the scanning lines 321 and the signal lines 322. The second substrate assembly 32 further includes a plurality of pixel electrodes 324 formed on a surface thereof facing the first substrate assembly 32.

[0006] Each thin film transistor 323 includes a gate electrode (not labeled), a source electrode (not labeled), and a drain electrode (not labeled). The gate electrode of each thin film transistor 323 is connected with a corresponding scanning line 321. The source electrode of each thin film transistor 323 is connected with a corresponding signal line 322. The drain electrode of each thin film transistor 323 is connected to a corresponding pixel electrode 324.

[0007] The scanning lines 321 are connected with a scanning line driving circuit 326 for receiving scanning signals. The signal lines 322 are connected with a signal line driving circuit 327 for receiving gradation voltages. The common electrode lines 325 are connected to a common voltage generating circuit 328. The common voltage generating circuit 328 is configured for generating a first common voltage and a

second common voltage to the common electrode lines 325 of the second substrate assembly 32 and the common electrodes 310 of the first substrate assembly 31. The scanning line driving circuit 326, the signal line driving circuit 327 and the common voltage generating circuit 328 are connected with a timing control circuit 329 in order to work in a predetermined sequence.

[0008] The pixel electrodes 324, the common electrodes 310 facing the pixel electrodes 324, and the liquid crystal layer 33 sandwiched between the pixel and common electrodes 324, 310 cooperatively define a plurality of pixel units (not labeled). Each pixel unit includes a liquid crystal capacitor C_{lc} and a storage capacitor C_s . The liquid crystal capacitor C_{lc} and the storage capacitor C_s are both electrically connected with the common electrodes 310. A common voltage of each common electrode 310 and a gradation voltage of the corresponding pixel electrode 324 cooperatively define a display voltage, which is used to control an amount of light transmission at the corresponding pixel unit. The display voltage keeps in a frame period.

[0009] Referring to FIG. 14, an abbreviated waveform diagram of driving signals of the liquid crystal display 3 is shown. Scanning signals $G1-G2n$ are generated by the scanning line driving circuit 326, and are applied to the scanning lines 321. Gradation voltages (V_n) are generated by the signal line driving circuit 327, and are sequentially applied to the signal lines 322. A common voltage (V_{com1}) is applied to odd-numbered common electrodes 310. A common voltage (V_{com2}) is applied to even-numbered common electrodes 310. Even-numbered common electrodes 310 and odd-numbered common electrodes 310 are respectively provided voltages having opposite polarities and a constant potential in each frame period. And, the polarities of even-numbered common electrodes 310 and odd-numbered common electrodes 310 are respectively alternated in a next frame period. Only one scanning signal pulse is applied to each scanning line 321 during each frame period, the scanning signal pulse having a duration which is equal to a period of clock pulses of a scanning clock signal. The scanning signal pulses are output sequentially to the scanning lines 321 to activate the thin film transistors 323 connected to the scanning lines 321.

[0010] During Frame 1, when an odd-numbered scanning line 321 is scanned, the signal line driving circuit 327 outputs first gradation voltages corresponding to image data to the signal lines 322. Then the first gradation voltages are applied to the pixel electrodes 324 via the activated thin film transistors 323. A corresponding odd-numbered common electrodes 310 is provided with the first common voltage. The first common voltage has a positive polarity, and is greater than the first gradation voltages. Thus, the display voltages of corresponding pixel units have negative polarities.

[0011] When an even-numbered scanning line 321 is scanned, the signal line driving circuit 327 outputs second gradation voltages corresponding to image data to the signal lines 322. Then the second gradation voltages are applied to the pixel electrodes 324 via the activated TFTs 323. A corresponding even-numbered common electrode 310 is provided with the second common voltage. The second common voltage has a negative polarity, and is less than the second gradation voltages. Thus, the display voltages of corresponding pixel units have positive polarities. FIG. 15 (a) shows the polarities of the display voltages of the pixel units in Frame 1.

[0012] During Frame 2, when odd-numbered scanning line 321 is scanned, the signal line driving circuit 327 outputs

second gradation voltages to the corresponding pixel electrodes 324 via the activated TFTs 323. The corresponding odd-numbered common electrode 310 is applied with a second common voltage. The second common voltage has a negative polarity, and is less than the second gradation voltages. Thus, the display voltages have positive polarities.

[0013] When even-numbered scanning line 321 is scanned, the signal line driving circuit 327 outputs first gradation voltages to the corresponding pixel electrodes 324 via the activated TFTs 323. The corresponding even-numbered common electrode 310 is applied with a first common voltage. The first common voltage has a positive polarity, and is greater than the first gradation voltages. Thus, the display voltages of corresponding pixel units have negative polarities. FIG. 15 (b) shows the polarities of the display voltages of the pixel units in Frame 2.

[0014] The pixel units connected with the same scanning lines 321 have the same polarities of the display voltages, the pixel units in an adjacent scanning line 321 have the alternated polarities of the display voltages, and the polarities of the display voltages of the pixel units are alternated in a next frame period. As a result, a row inversion mode is realized.

[0015] However, the liquid crystal capacitors C_{lc} and the storage capacitors C_s are both electrically connected with the common electrodes 310. During a period between every continuous two frame periods, the voltages of odd-numbered common electrodes 310 and even-numbered common electrodes 310 are respectively alternated. Thus the liquid crystal capacitors C_{lc} and the storage capacitors C_s need to be discharged reversely. Therefore, a power consuming of the liquid crystal display 3 is great.

[0016] What is needed, therefore, is a liquid crystal display that can overcome the above-described deficiencies. What is also needed, is a driving method of such liquid crystal display.

SUMMARY

[0017] In one preferred embodiment, a liquid crystal display includes a first substrate assembly, a second substrate assembly parallel to the first substrate assembly, a liquid crystal layer sandwiched between the first substrate assembly and the second substrate assembly, and a discharging circuit. The first substrate assembly includes a plurality of common electrodes formed thereat. The common electrodes are parallel to each other. The second substrate assembly includes a plurality of scanning lines that are parallel to each other and that each extends along a first direction, and a plurality of signal lines that are parallel to each other and that each extends along a second direction orthogonal to the first direction. The discharging circuit is electrically connected with the common electrodes.

[0018] Other advantages and novel features will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The components in the drawings are not necessarily drawn to scale, the emphasis instead being placed upon clearly illustrating the principles of at least one embodiment of the present invention. In the drawings, like reference numerals designate corresponding parts throughout various views, and all the views are schematic.

[0020] FIG. 1 is an exploded, isometric view of a liquid crystal display according to a first embodiment of the present

invention, the liquid crystal display including a first substrate assembly and a second substrate assembly, and defining a plurality of pixel units, the second substrate assembly including a discharging circuit having a transistor.

[0021] FIG. 2 is an enlarged, top plan view of the first substrate assembly of the liquid crystal display of FIG. 1.

[0022] FIG. 3 is an enlarged, top plan view of the second substrate assembly of the liquid crystal display of FIG. 1.

[0023] FIG. 4 is an abbreviated equivalent circuit diagram of the transistor of the discharging circuit of the second substrate assembly of the liquid crystal display of FIG. 1.

[0024] FIG. 5 is an abbreviated waveform diagram of driving signals of the liquid crystal display of FIG. 1.

[0025] FIG. 6 is an explanatory view illustrating the polarities of the display voltages of the plurality of the pixel units in a row inversion mode of the liquid crystal display of FIG. 1.

[0026] FIG. 7 is similar to FIG. 2, but showing a corresponding view in the case of a first substrate assembly of a liquid crystal display according to a second embodiment of the present invention, the liquid crystal display defining a plurality of pixel units.

[0027] FIG. 8 is similar to FIG. 3, but showing a corresponding view in the case of a second substrate assembly of the liquid crystal display of the second embodiment.

[0028] FIG. 9 is an abbreviated waveform diagram of driving signals of the liquid crystal display of the second embodiment.

[0029] FIG. 10 is an explanatory view illustrating the polarities of the display voltages of the pixel units in a column inversion mode of the liquid crystal display of the second embodiment.

[0030] FIG. 11 is an exploded, side-on view of a conventional liquid crystal display, the liquid crystal display including a first substrate assembly and a second substrate assembly, and defining a plurality of pixel units.

[0031] FIG. 12 is an enlarged, top plan view of the first substrate assembly of the liquid crystal display of FIG. 11.

[0032] FIG. 13 is a plan view of the second substrate assembly of the liquid crystal display of FIG. 11.

[0033] FIG. 14 is an abbreviated waveform diagram of driving signals of the liquid crystal display of FIG. 11.

[0034] FIG. 15 is an explanatory view illustrating the polarities of the display voltages of a plurality of the pixel units in a row inversion mode of the liquid crystal display of FIG. 11.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0035] Reference will now be made to the drawings to describe various embodiments of the present invention in detail.

[0036] Referring to FIG. 1, a liquid crystal display 1 according to a first embodiment of the present invention is shown. The liquid crystal display 1 includes a liquid crystal panel 10, and a backlight module 19 adjacent to the liquid crystal panel 10. The liquid crystal panel 10 includes a first substrate assembly 11, a second substrate assembly 12 parallel to the first substrate assembly 11, a liquid crystal layer 13 sandwiched between the first substrate assembly 11 and the second substrate assembly 12, and a sealant 14. The sealant 14 seals the liquid crystal layer 13 therein, and includes a first conductive portion 141 and a second conductive portion 142

parallel to the first conductive portion 141. The first conductive portion 141 and the second conductive portion 142 are insulated with each other.

[0037] Referring to FIG. 2, the first substrate assembly 11 includes a plurality of parallel strip-shaped common electrodes 110, which are made from indium tin oxide (ITO). Odd-numbered common electrodes 110 are electrically connected to a first common electrode bus line 111. Even-numbered common electrodes 110 are electrically connected to a second common electrode bus line 112.

[0038] Referring to FIG. 3, the second substrate assembly 12 includes a scanning line driving circuit 126, a signal line driving circuit 127, a timing control circuit 129, a common voltage generating circuit 128, a discharging circuit 120, a first common bus line 143, a second common bus line 144, a number $2n$ (where n is a natural number) of scanning lines 1211 that are parallel to each other and that each extend along a first direction, a number k (where k is also a natural number) of signal lines 1212 that are parallel to each other and that each extend along a second direction orthogonal to the first direction, a number $2n$ of common electrode lines 1215 that are parallel to each other and that each extend along the first direction, a plurality of thin film transistors 123 and a plurality of pixel electrodes 124.

[0039] The common voltage generating circuit 128 is connected with the first common bus line 143 and the second common bus line 144, and is configured for generating a first common voltage for the first common bus line 143 and a second common voltage for the second common bus line 144. The discharging circuit 120 is connected with the first common bus line 143 and the second common bus line 144, and is configured for shorting the two common bus lines 143, 144 during a period between every two continuous frame periods. The scanning line driving circuit 126, the signal line driving circuit 127, the common voltage generating circuit 128 and the discharging circuit 120 are connected with the timing control circuit 129 in order to work in a predetermined sequence.

[0040] The pixel electrodes 124 are formed on an inner surface of the second substrate assembly 12 thereof facing the first substrate assembly 11. Each thin film transistor 123 is provided in the vicinity of a respective point of intersection of the scanning lines 1211 and the signal lines 1212 functioning as switching element. Each thin film transistor 123 includes a gate electrode (not labeled), a source electrode (not labeled) and a drain electrode (not labeled). Each gate electrode is connected with a corresponding scanning line 1211. Each source electrode is connected with a corresponding signal line 1212. Each drain electrode is connected with a corresponding pixel electrode 124.

[0041] One pixel electrode 124, one corresponding common electrode 110 facing the pixel electrode 124 and the liquid crystal layer 13 sandwiched between the two electrodes 110, 124 cooperatively define a single pixel unit (not labeled) as a minimum display unit, and form a liquid crystal capacitor Clc. A voltage of each common electrode 110 and a voltage of each pixel electrode 124 cooperate to define a display voltage, which is used to control an amount of light transmission at the corresponding pixel unit.

[0042] Each common electrode line 1215 is insulated with the corresponding pixel electrode 124. The common electrode line 1215, the corresponding pixel electrode 124 and an insulator (not shown) therebetween define a storage capacitor Cs (not shown).

[0043] The scanning lines 1211 are connected to the scanning line driving circuit 126 for receiving scanning signals. The signal lines 1212 are connected to the signal line driving circuit 127 for receiving gradation voltages. Odd-numbered common electrode lines 1215 are electrically connected with the first common bus line 143. Even-numbered common electrode lines 1215 are electrically connected with the second common bus line 144.

[0044] After the first substrate assembly 11 and the second substrate assembly 12 are assembled together, the first conductive portion 141 of the sealant 14 electrically connects the first common electrode bus line 111 with the first common bus line 143, and the second conductive portion 142 of the sealant 14 electrically connects the second common electrode bus line 112 with the second common bus line 144.

[0045] That is, the first common bus line 143 is electrically connected with the corresponding storage capacitors Cs via odd-numbered common electrode lines 1215, and is electrically connected with the corresponding liquid crystal capacitors Clc via the first conductive portion 141, the first common electrode bus line 111 and odd-numbered common electrodes 110. The second common bus line 144 is electrically connected with the corresponding storage capacitors Cs via even-numbered common electrode lines 1215, and is electrically connected with the corresponding liquid crystal capacitors Clc via the second conductive portion 142, the second common electrode bus line 112 and even-numbered common electrodes 110.

[0046] The discharging circuit 120 includes a transistor 1200. Referring to FIG. 4, the transistor 1200 includes a drain electrode (not labeled) coupled to the first common bus line 143, a source electrode (not labeled) coupled to the second common bus line 144, and a gate electrode (not labeled) coupled to the timing control circuit 129.

[0047] Referring to FIG. 5, an abbreviated waveform diagram of driving signals of the liquid crystal display 1 is shown. Scanning signals G1-G $2n$ are generated by the scanning line driving circuit 126, and are applied to the scanning lines 1211. Gradation voltages (Vn) are generated by the signal line driving circuit 127, and are sequentially applied to the signal lines 1212. Even-numbered common electrodes 110 and odd-numbered common electrodes 110 are respectively provided voltages having opposite polarities and a constant potential in each frame period. The polarities of even-numbered common electrodes 110 and odd-numbered common electrodes 110 are respectively alternated in a next frame period. Only one scanning signal pulse is applied to each scanning line 1211 during each frame period. The scanning signal pulse has a duration that is equal to a period of the clock pulses of a scanning clock signal. The scanning signal pulses are output sequentially to the scanning lines 1211 to activate the thin film transistors 123 connected to the scanning lines 1211.

[0048] During a "Frame 1" period, when odd-numbered scanning lines 1211 are scanned, the signal line driving circuit 126 outputs first gradation voltages Vn corresponding to image data to the signal lines 1211. Then the first gradation voltages are applied to the pixel electrodes 124 via the activated thin film transistors 123. The corresponding odd-numbered common electrodes 110 are provided with the first common voltage. The first common voltage has a positive polarity, and is greater than the first gradation voltages. Thus, the display voltages of corresponding pixel units have negative polarities.

[0049] In the "Frame 1" period, when even-numbered scanning lines 1211 are scanned, the signal line driving circuit 126 outputs second gradation voltages V_n corresponding to image data to the signal lines 1211. Then the second gradation voltages are applied to the pixel electrodes 124 via the activated thin film transistors 123. The corresponding even-numbered common electrodes 110 are provided with the second common voltage. The second common voltage has a negative polarity, and is less than the second gradation voltages. Thus, the display voltages of corresponding pixel units have positive polarities. FIG. 5 (a) shows the polarities of the display voltages of the pixel units in the "Frame 1" period.

[0050] In a "Blank" period between the "Frame 1" and a "Frame 2", the common voltage generating circuit 128 stop generating the first common voltage and the second common voltage under control of the timing control circuit 129. The discharging circuit 120 works and shorts the first common bus line 143 and the second common bus line 144 under control of the timing control circuit 129. That is, the timing control circuit 129 generates a high level voltage to the gate electrode of the transistor 1200 of the discharging circuit 120, and the transistor 1200 is switched on. Thus, charges in the storage capacitors C_s and the liquid crystal capacitors C_{lc} connected with the first common bus line 143 are neutralized with charges of the storage capacitors C_s and the liquid crystal capacitors C_{lc} connected with the second common bus line 144.

[0051] Then the timing control circuit 129 generates a low level voltage, and output the low level voltage to the transistor 1200 of the discharging circuit 120. The transistor 1200 as well as the discharging circuit 120 is switched off.

[0052] In the "Frame 2" period, when odd-numbered scanning lines 1211 are scanned, the signal line driving circuit 127 outputs second gradation voltages V_n corresponding to image data to the signal lines 1212. Then the second gradation voltages are applied to the pixel electrodes 124 via the activated thin film transistors 123. The corresponding odd-numbered common electrodes 110 are provided with the second common voltage. The second common voltage has a negative polarity, and is less than the second gradation voltage. Thus, the display voltages of the corresponding pixel units connected with odd-numbered scanning lines 1211 have positive polarities.

[0053] In the "Frame 2" period, when even-numbered scanning lines 1211 are scanned, the signal line driving circuit 127 outputs first gradation voltages V_n corresponding to image data to the signal lines 1212. Then the first gradation voltages are applied to the pixel electrodes 124 via the activated thin film transistors 123. The corresponding even-numbered common electrodes 110 are provided with the first common voltage. The first common voltage has a positive polarity, and is greater than the first gradation voltages. Thus, the display voltages of the corresponding pixel units have negative polarities. FIG. 5 (b) shows the polarities of the display voltages of the pixel units in the "Frame 2" period.

[0054] In operation, even-numbered common electrode lines 1215 and odd-numbered common electrode lines 1215 are respectively provided voltages having opposite polarities and a constant potential in one frame period. And, the polarities of even-numbered common electrode lines 1215 and odd-numbered common electrode lines 1215 are respectively alternated in a next frame period. Thus, a row inversion display mode is realized.

[0055] Comparing with a conventional liquid crystal display, the liquid crystal display 1 includes a discharging circuit 120, thus charges in the liquid crystal capacitors C_{lc} and the storage capacitors C_s connected with the first common bus line 143 are neutralized via the discharging circuit 120 with charges in the liquid crystal capacitors C_{lc} and the storage capacitors C_s connected with the second common bus line 144. No external charges are needed to neutralize the charges in the liquid crystal capacitors C_{lc} and the storage capacitors C_s . Therefore, an electrical power consumption of the liquid crystal display 1 is reduced.

[0056] Referring to FIG. 7 and FIG. 8, a first substrate assembly 21 and a second substrate assembly 22 of a liquid crystal display 2 according to a second embodiment of the present invention is shown. The liquid crystal display 2 is similar to the liquid crystal display 1 of the first embodiment. However, a plurality of common electrodes 210 and a plurality of common electrode lines 2215 are arranged perpendicular to a plurality of scanning lines 2211.

[0057] Referring to FIG. 9, an abbreviated timing chart illustrating operation of the liquid crystal display 2 is shown. Scanning signals $G1-G2n$ are generated by a scanning line driving circuit 226, and are applied to the scanning lines 2211. Gradation voltages (V_n) are generated by a signal line driving circuit 227, and are sequentially applied to signal lines 2212. Even-numbered common electrode lines 2215 and odd-numbered common electrode lines 2215 are respectively provided voltages having opposite polarities and a constant potential in one frame period. The polarities of even-numbered common electrode lines 2215 and odd-numbered common electrode lines 2215 are respectively alternated in a next frame period. Only one scanning signal pulse is applied to each scanning line 2211 during each frame period. The scanning signal pulse has a duration that is equal to a period of the clock pulses of the scanning clock signal. The scanning signal pulses are output sequentially to the scanning lines 2211 to activate thin film transistors 223 connected to the scanning lines 2211.

[0058] During a "Frame 1" period, when the scanning lines 2211 are sequentially scanned, the signal line driving circuit 227 outputs first gradation voltages V_n corresponding to image data to odd-numbered signal lines 2212. Then the first gradation voltages are applied to the pixel electrodes 224 in odd-numbered columns, corresponding to odd-numbered signal lines 2211, through the activated thin film transistors 223. The corresponding odd-numbered common electrodes 210 are provided with a first common voltage. The first common voltage has a positive polarity, and is greater than the first gradation voltages. Thus, the display voltages of the corresponding pixel units in odd-number column have negative polarities. At the same time, the signal line driving circuit 226 outputs second gradation voltages V_n corresponding to image data to even-numbered signal lines 2212. Then the second gradation voltages are applied to the pixel electrodes 224 in even-number column through the activated thin film transistors 223. The corresponding even-numbered common electrodes 210 are provided with a second common voltage. The second common voltage has a negative polarity and is less than the second gradation voltage. Thus, the display voltages of the corresponding pixel units in even-number column have positive polarities. FIG. 9 (a) shows the polarities of the display voltages of the pixel units in the "Frame 1" period.

[0059] In a "Blank" period between the "Frame 1" and a "Frame 2", a common voltage generating circuit 228 stop generating the first common voltage and the second common

voltage under control of a timing control circuit 229. A discharging circuit 220 works and shorts a first common bus line 243 and a second common bus line 244 under control of the timing control circuit 229. That is, the timing control circuit 229 generates a high level voltage to a gate electrode (not shown) of a transistor (not shown) in the discharging circuit 220, and the transistor as well as the discharging circuit 220 is switched on. Thus, charges in the storage capacitors Cs and the liquid crystal capacitors Clc connected with the first common bus line 243 are neutralized with charges of the storage capacitors Cs and the liquid crystal capacitors Clc connected with the second common bus line 244.

[0060] Then the timing control circuit 229 generates a low level voltage, and outputs the low level voltage to the discharging circuit 220. The discharging circuit 220 is switched off.

[0061] During the "Frame 2" period, when the scanning lines 2211 are sequentially scanned, the signal line driving circuit 227 outputs second gradation voltages Vn corresponding to image data to odd-numbered signal lines 2212. Then the second gradation voltages are applied to the pixel electrodes 224 in odd-number column through the activated thin film transistors 223. Odd-numbered common electrodes 210 are provided with the second common voltage. The second common voltage has a negative polarity and is less than the second gradation voltages. Thus, the display voltages of the pixel units in odd-number column have positive polarities. At the same time, the signal line driving circuit 227 outputs first gradation voltages Vn corresponding to image data to even-numbered signal lines 2212. Then the first gradation voltages are applied to the pixel electrodes 224 in even-number column through the activated thin film transistors 223. Even-numbered common electrodes 210 are provided with the first common voltage. The first common voltage has a positive polarity and is greater than the first gradation voltages. Thus, the display voltages of the pixel electrodes in even-number column have negative polarities. FIG. 9 (b) shows the polarities of the display voltages of the pixel units in the Frame 1.

[0062] It is believed that the present embodiments and their advantages will be understood from the foregoing description, and it will be apparent that various changes may be made thereto without departing from the spirit or scope of the invention or sacrificing all of its material advantages, the examples hereinbefore described merely being preferred or exemplary embodiments of the invention.

What is claimed is:

1. A liquid crystal display comprising:
 - a first substrate assembly comprising a plurality of common electrodes, parallel to each other;
 - a second substrate assembly parallel to the first substrate assembly, the second substrate assembly comprising:
 - a plurality of scanning lines that are parallel to each other and that each extend along a first direction;
 - a plurality of signal lines that are parallel to each other and that each extend along a second direction orthogonal to the first direction; and
 - a discharging circuit electrically connected with the common electrodes; and
 - a liquid crystal layer sandwiched between the first substrate assembly and the second substrate assembly.
2. The liquid crystal display as claimed in claim 1, wherein the common electrodes are disposed parallel to the scanning lines.

3. The liquid crystal display as claimed in claim 1, wherein the common electrodes are disposed parallel to the signal lines.

4. The liquid crystal display as claimed in claim 1, wherein odd-numbered common electrodes are electrically connected with each other, even-numbered common electrodes are electrically connected with each other and the discharging circuit electrically connects odd-numbered common electrodes with even-numbered common electrodes.

5. The liquid crystal display as claimed in claim 2, wherein the second substrate assembly further comprises a plurality of common electrode lines corresponding to the plurality of the common electrodes, the common electrode lines being parallel to the common electrodes.

6. The liquid crystal display as claimed in claim 5, wherein odd-numbered common electrode lines are electrically connected with each other, and even-numbered common electrode lines are electrically connected with each other.

7. The liquid crystal display as claimed in claim 6, further comprising a sealant sandwiched between the first substrate assembly and the second substrate assembly, forming a space to accommodating the liquid crystal layer, the sealant comprising a first conductive portion and a second conductive portion insulated to each other, the first conductive portion electrically connecting odd-numbered common electrodes with odd-numbered common electrode lines, the second conductive portion electrically connecting even-numbered common electrodes with even-numbered common electrode lines.

8. The liquid crystal display as claimed in claim 7, wherein the second substrate assembly further comprises a scanning driving circuit applying scanning signals to the scanning lines, a signal driving circuit applying gradation voltages to the signal lines, a common voltage generating circuit applying a first common voltage and a second common voltage to the common electrodes and the common electrode lines, and a timing control circuit making the scanning driving circuit, the signal driving circuit, the common voltage generating circuit and the discharging circuit work in predetermined sequence.

9. The liquid crystal display as claimed in claim 8, wherein the discharging circuit comprises a transistor, the transistor comprising a gate electrode electrically connected with the timing control circuit, a source electrode electrically connected with odd-numbered common electrode lines, and a drain electrode electrically connected with even-numbered common electrode lines.

10. The liquid crystal display as claimed in claim 1, wherein the second substrate assembly further comprises a plurality of pixel electrodes, the common electrode lines facing the pixel electrodes, the common electrode lines being insulated with the pixel electrodes, one pixel electrode and a corresponding common electrode line forming a storage capacitor.

11. The liquid crystal display as claimed in claim 1, wherein one pixel electrode, a corresponding common electrode and a liquid crystal layer sandwiched therebetween form a liquid crystal capacitor.

12. A driving method of the liquid crystal display in claim 1, the method comprising:

during a first frame period, providing a first common voltage to odd-numbered common electrodes, and providing a second common voltage to even-numbered common electrodes;

during a blank period between the first frame period and a second frame period, the discharging circuit shorting odd-numbered common electrodes and even-numbered common electrodes;

during the second frame period, providing a second common voltage to odd-numbered common electrodes, and providing a first common voltage to even-numbered common electrodes;

during a blank period between the second frame period and a third frame period, the discharging circuit shorting odd-numbered common electrodes and even-numbered common electrodes; and

the above steps being repeated.

13. The method as claimed in claim **12**, wherein during the first frame period, when odd-numbered scanning lines corresponding to odd-numbered common electrodes are scanned, the signal lines are provided with first gradation voltages; when even-numbered scanning lines corresponding to even-numbered common electrodes are scanned, the signal lines are provided with second gradation voltages.

14. The method as claimed in claim **12**, wherein during the second frame period, when odd-numbered scanning lines corresponding to odd-numbered common electrodes are scanned, the signal lines are provided with second gradation

voltages; when even-numbered scanning lines corresponding to even-numbered common electrodes are scanned, the signal lines are provided with first gradation voltages.

15. The method as claimed in claim **13**, wherein the first common voltage is greater than the first gradation voltages, and the second common voltage is less than the second gradation voltages.

16. The method as claimed in claim **13**, wherein the first common voltage is less than the first gradation voltages, and the second common voltage is greater than the second gradation voltages.

17. The method as claimed in claim **12**, wherein during the first frame period, odd-numbered signal lines corresponding to odd-numbered common electrodes are provided with first gradation voltages, and even-numbered signal lines corresponding to even-numbered common electrodes are provided with second gradation voltages.

18. The method as claimed in claim **12**, wherein during the second frame period, odd-numbered signal lines corresponding to odd-numbered common electrodes are provided with second gradation voltages, and even-numbered signal lines corresponding to even-numbered common electrodes are provided with first gradation voltages.

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摘要(译)

示例性液晶显示器 (1) 包括第一基板组件 (11) , 平行于第一基板组件 (11) 的第二基板组件 (12) , 夹在第一基板组件和第二基板组件之间的液晶层 (13) 基板组件和放电电路 (120) 。第一基板组件包括在那里形成的公共电极 (110) 。公共电极彼此平行。第二基板组件包括彼此平行并且每个沿第一方向延伸的扫描线 (1211) , 以及彼此平行并且每个沿与第一方向正交的第二方向延伸的信号线 (1212) 。放电电路与公共电极电连接。

