US 20030063229A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2003/0063229 A1

Takahashi et al. (43) Pub. Date: Apr. 3, 2003

(54) LIQUID CRYSTAL DISPLAY DEVICE

(76) Inventors: **Takuya Takahashi**, Hitachi (JP); **Toshiki Kaneko**, Chiba (JP); **Katsumi Tamura**, Hitachi (JP); **Kenichi Onisawa**, Hitachinaka (JP)

Correspondence Address:
ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

(21) Appl. No.: **10/101,166**

(22) Filed: **Mar. 20, 2002**

(30) **Foreign Application Priority Data**

Sep. 28, 2001 (JP) 2001-298993

Publication Classification

(51) **Int. Cl.**[7] **G02F 1/136**

(52) **U.S. Cl.** **349/43**

(57) **ABSTRACT**

A liquid crystal display device having image signal lines of a bottom gate type TFT in which image signal lines comprise a laminated film of a first conductive film as a lower layer and a second conductive film as an upper layer, the first conductive film being made of an alloy comprising Mo as a main ingredient and W and the second conductive film being made of an alloy comprising Mo as a main ingredient and Zr. The device is capable of satisfying requirements of reduced resistance, improved dry etching resistance, selective wet etching with respect to the gate insulative film, the number of laminated layer of two or less and tapered fabrication for the cross section.

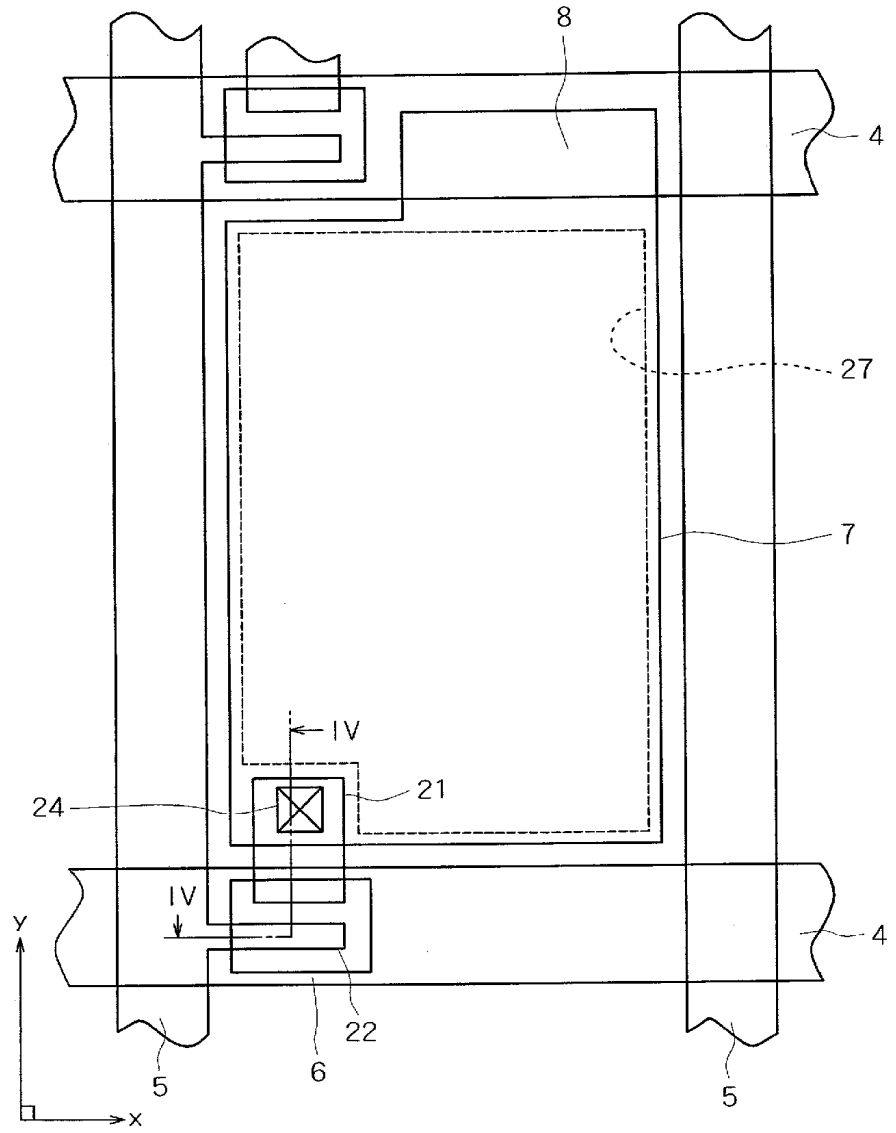


FIG. 1

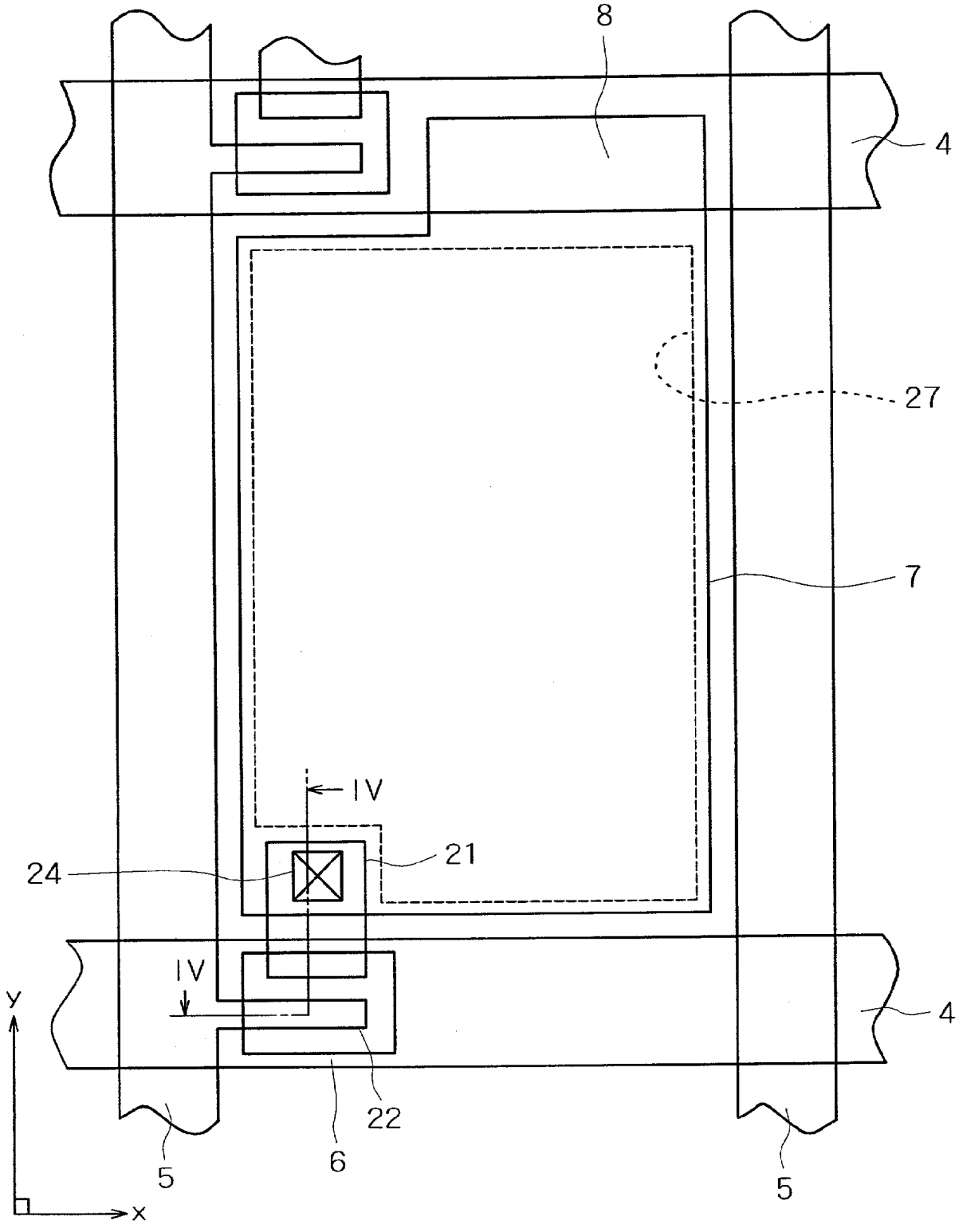


FIG. 2

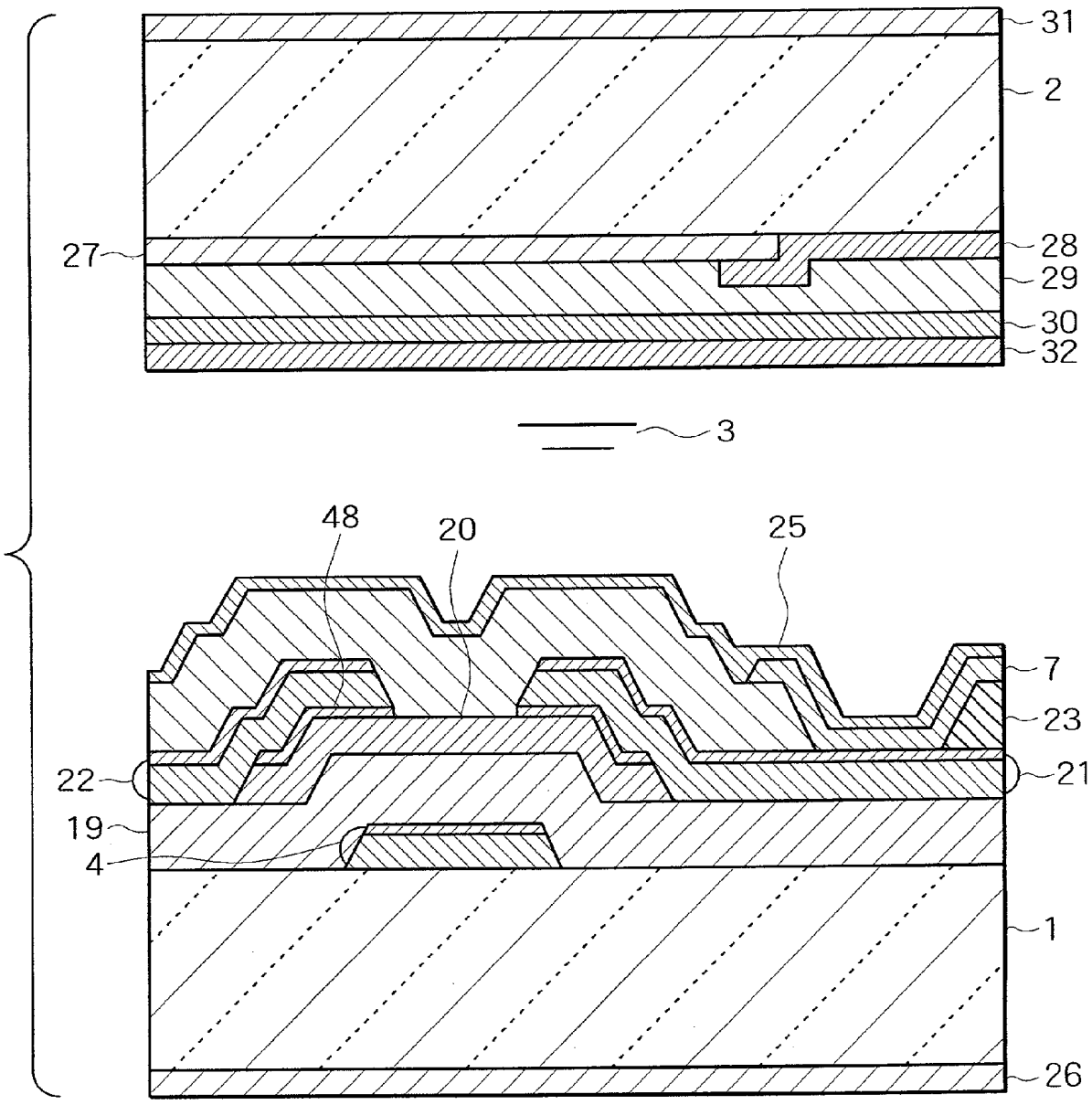


FIG. 3

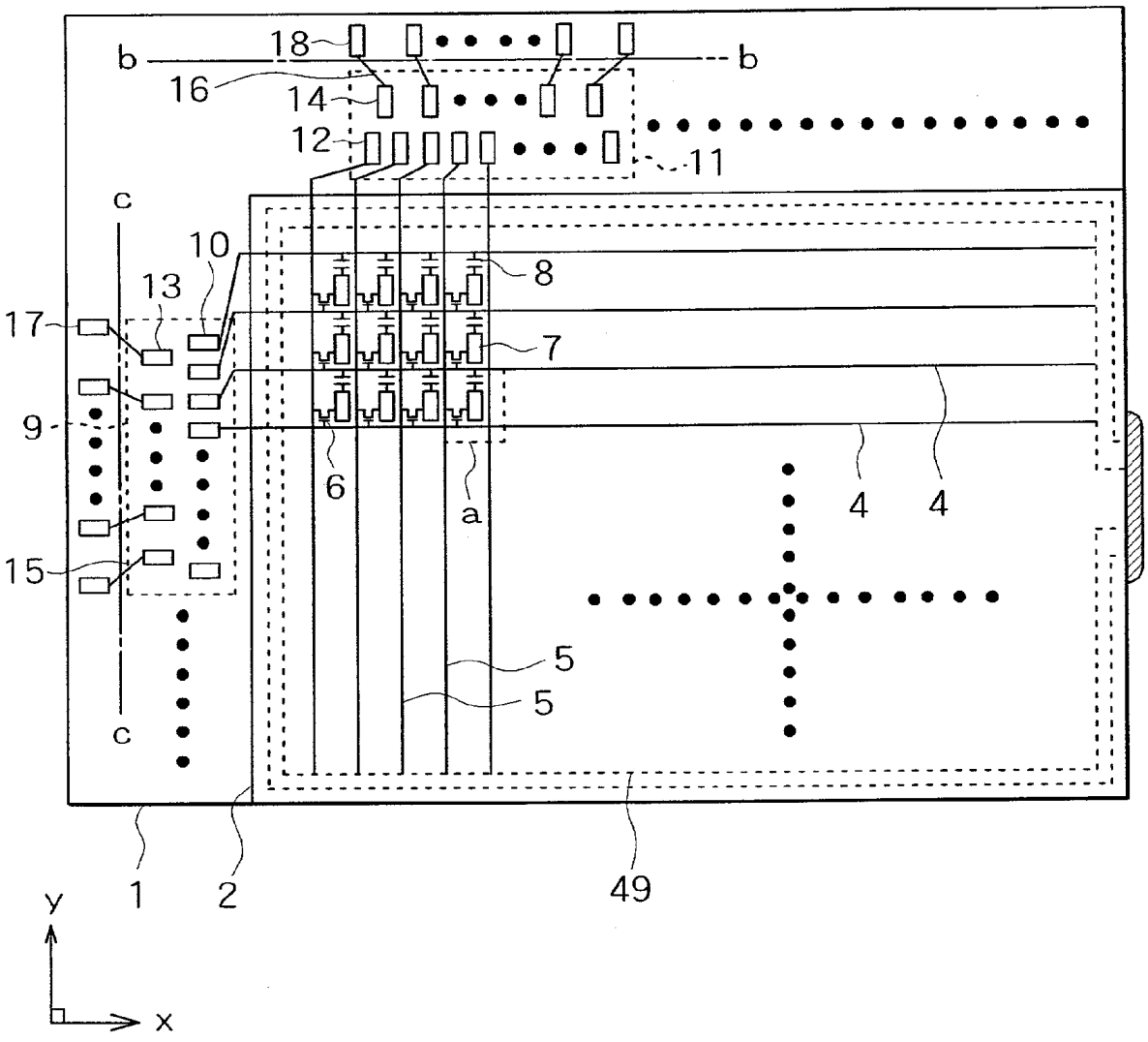


FIG. 4A

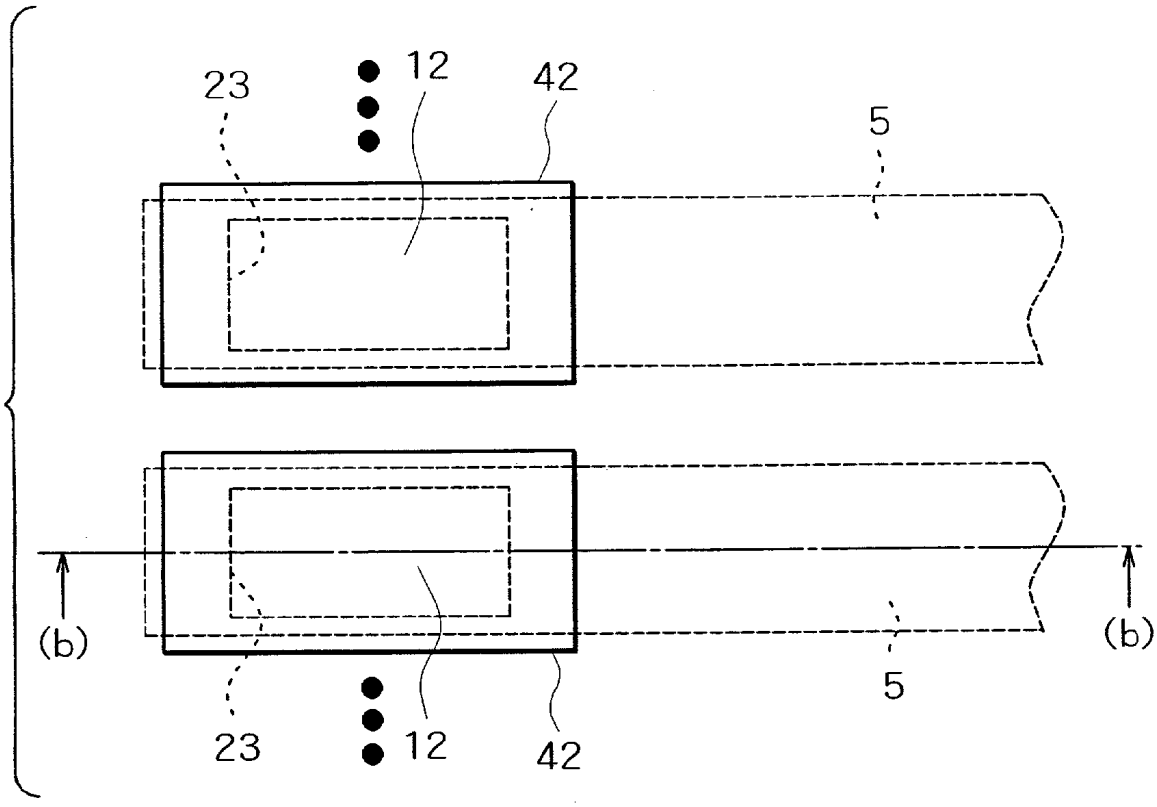


FIG. 4B

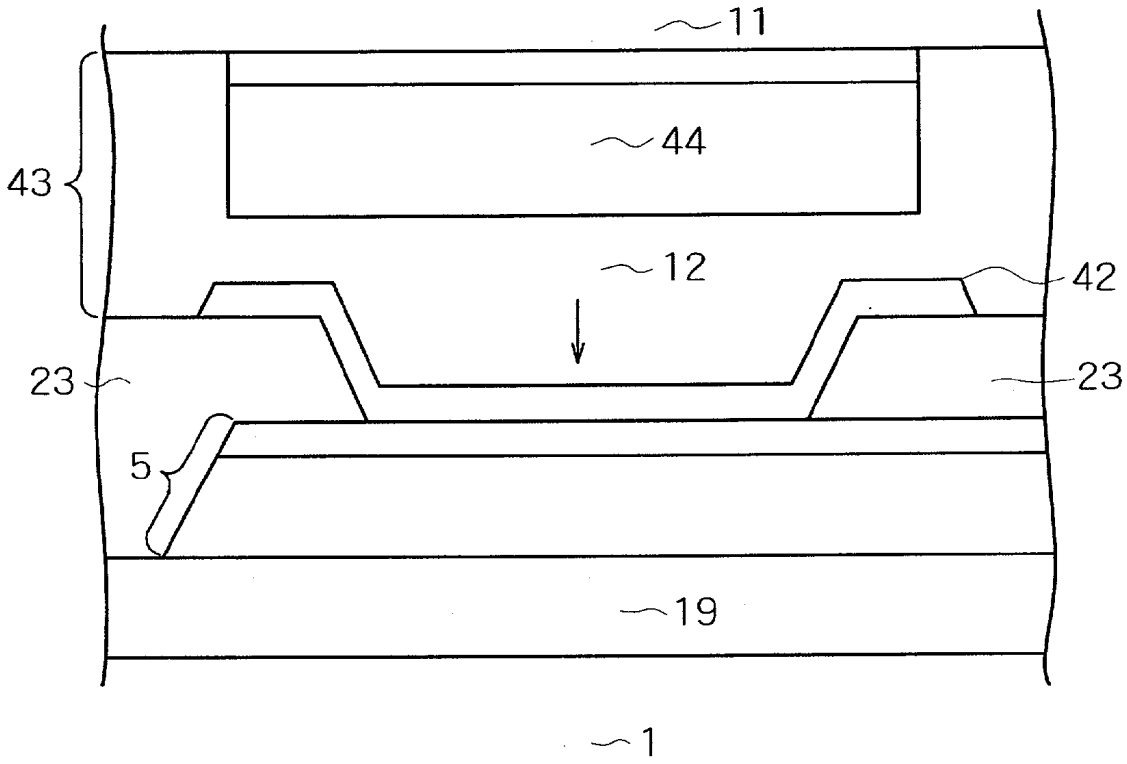


FIG. 5A

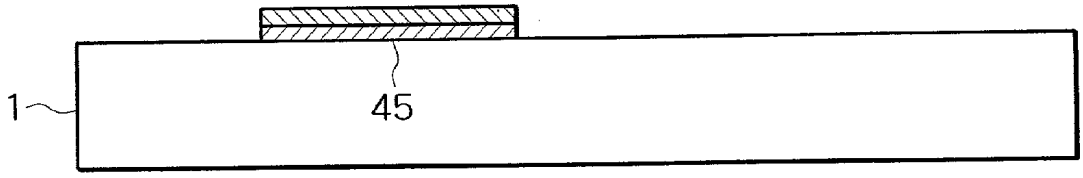


FIG. 5B

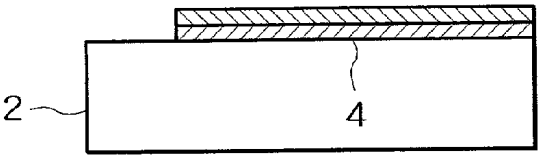


FIG. 5C

FIG. 5D

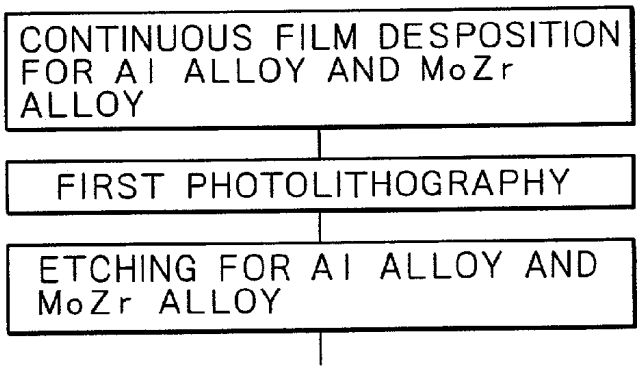


FIG. 6A

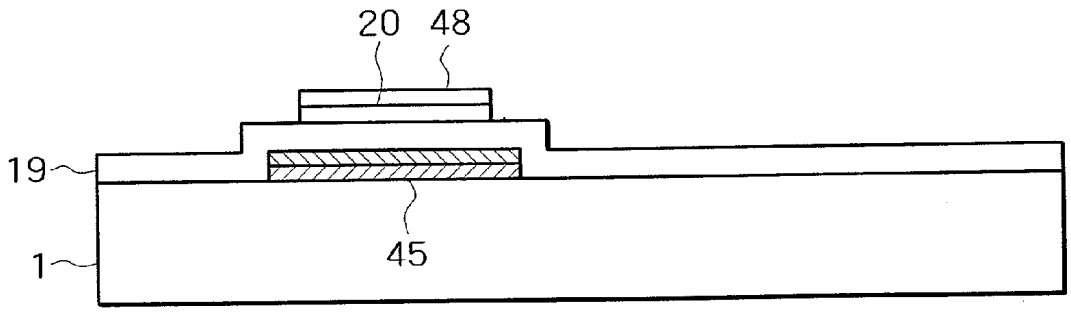


FIG. 6B

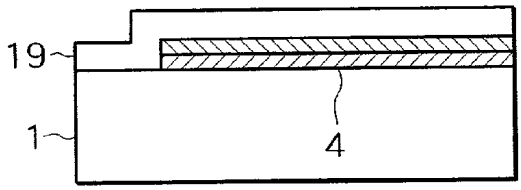


FIG. 6C

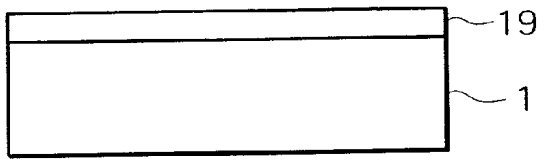


FIG. 6D

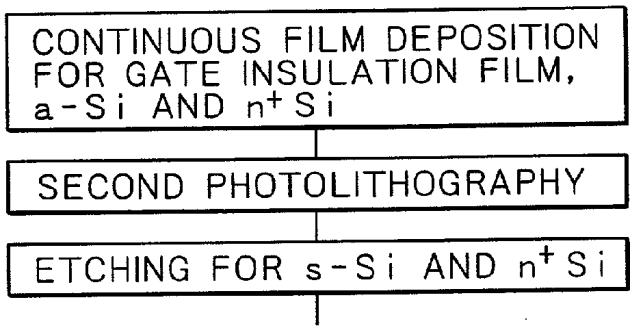


FIG. 7A

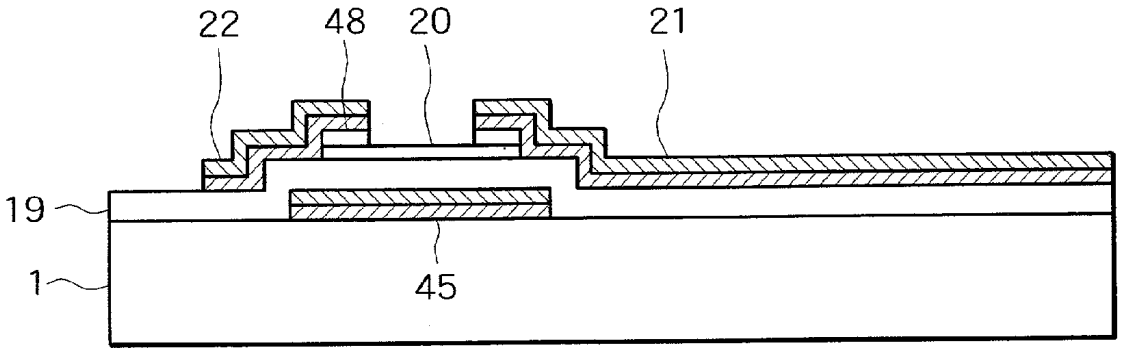


FIG. 7B

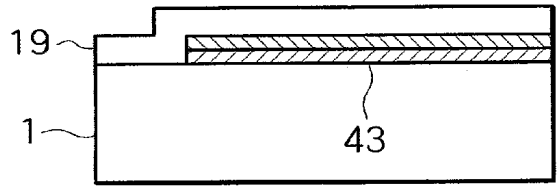


FIG. 7C

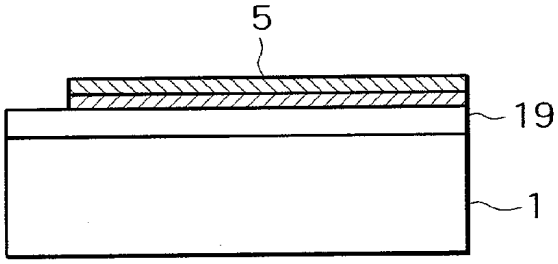


FIG. 7D

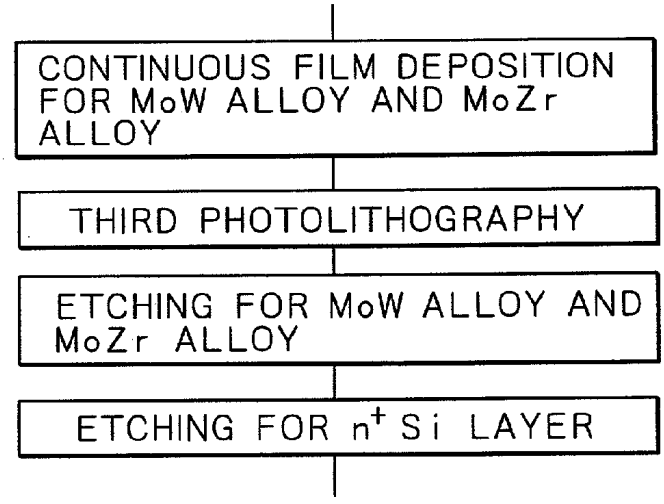


FIG. 8A

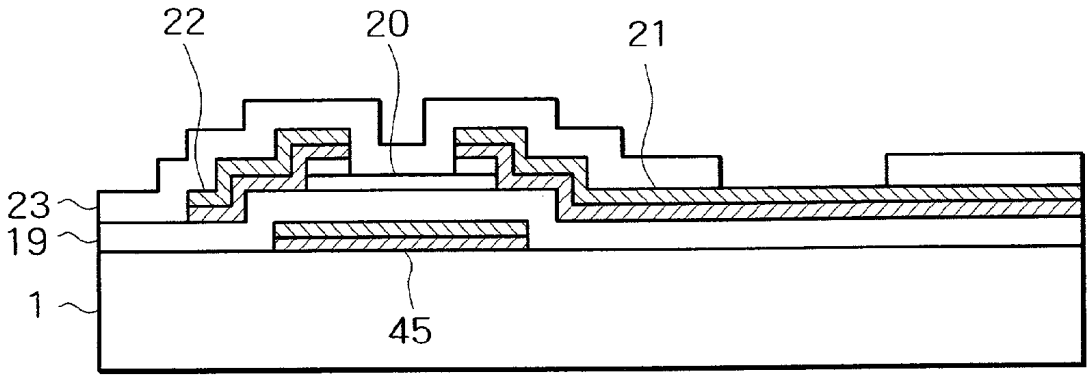


FIG. 8B

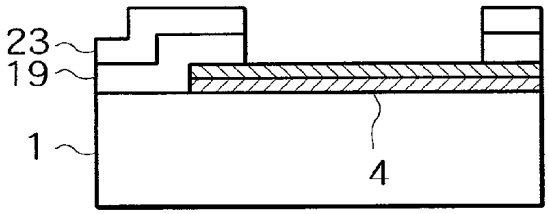


FIG. 8C

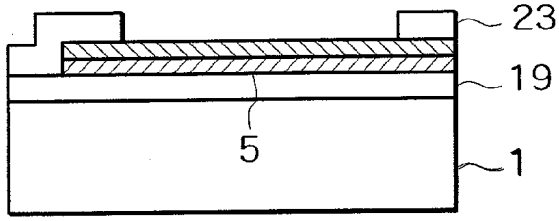


FIG. 8D

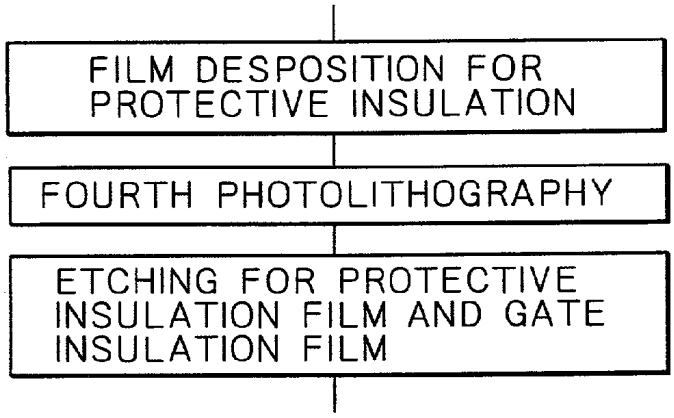


FIG. 9A

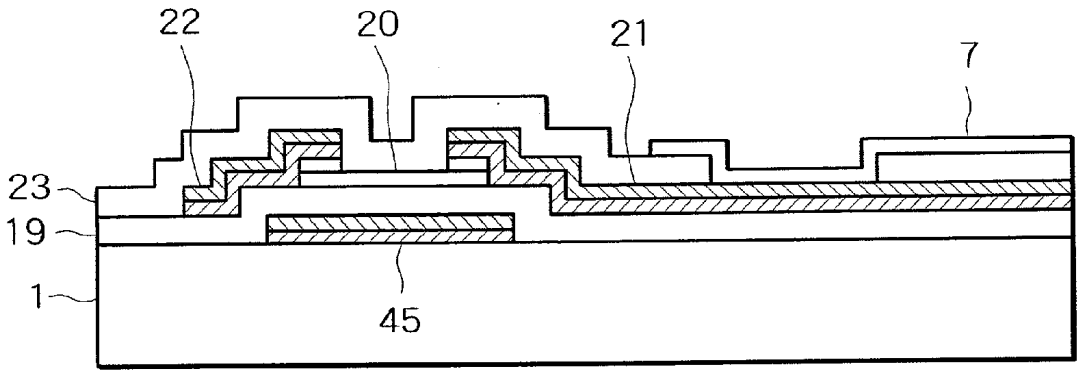


FIG. 9B

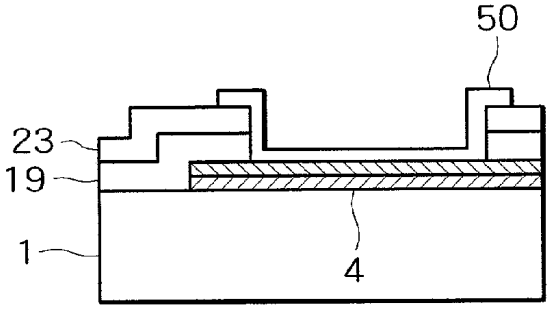


FIG. 9C

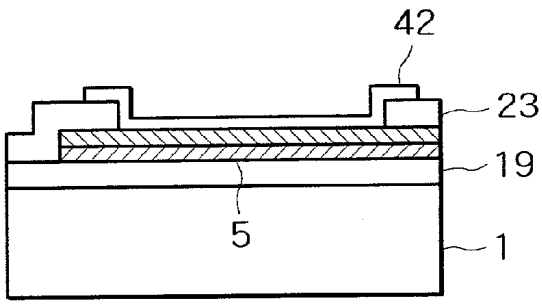


FIG. 9D

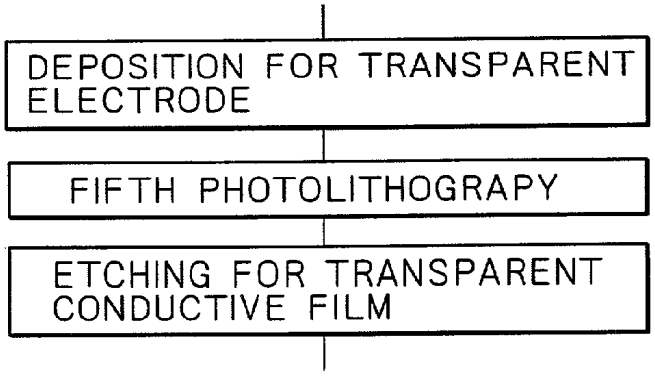


FIG. 10

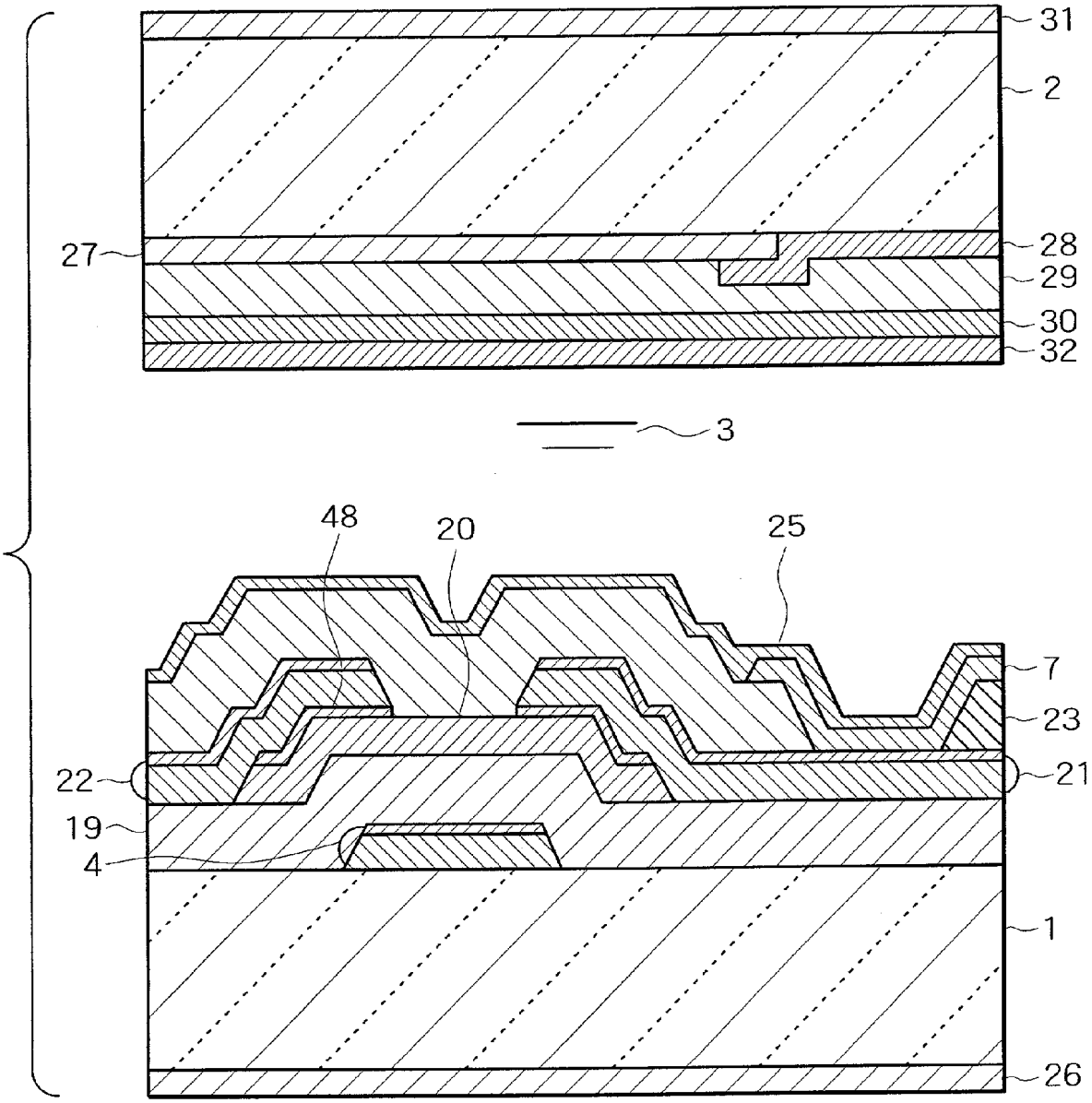


FIG. 11

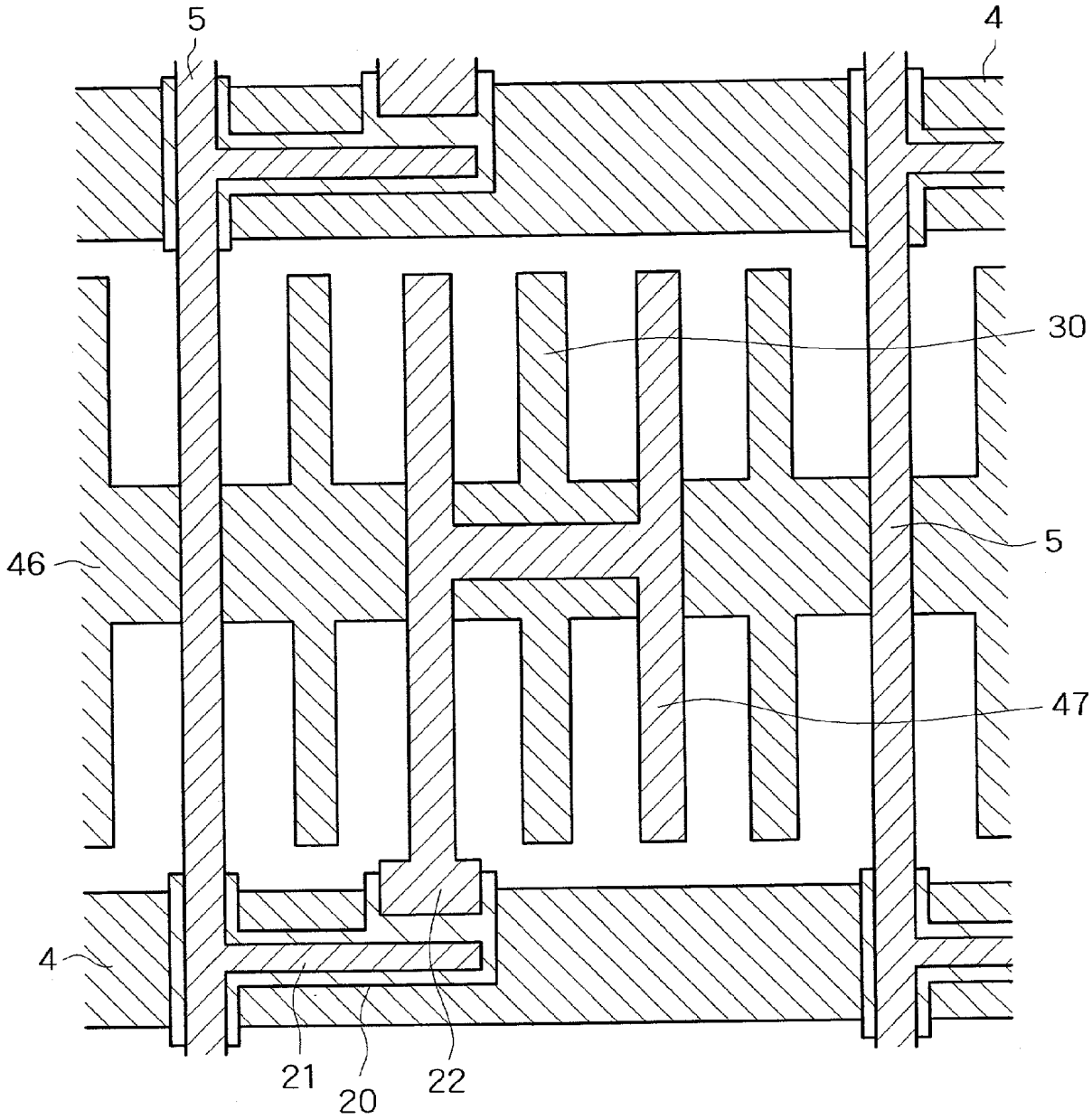


FIG. 12

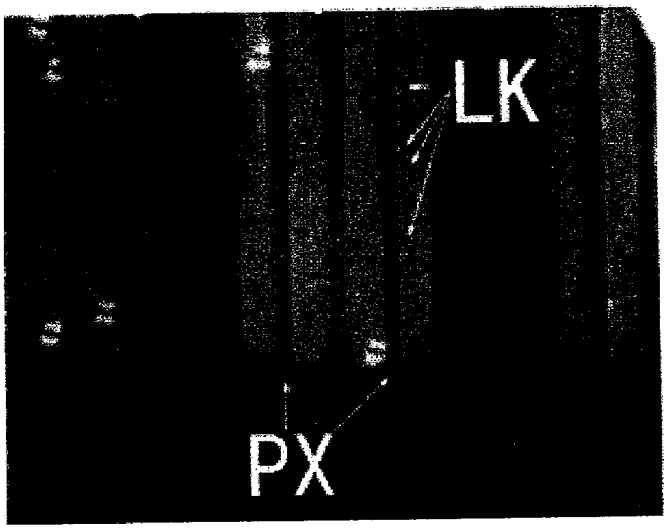


FIG. 13

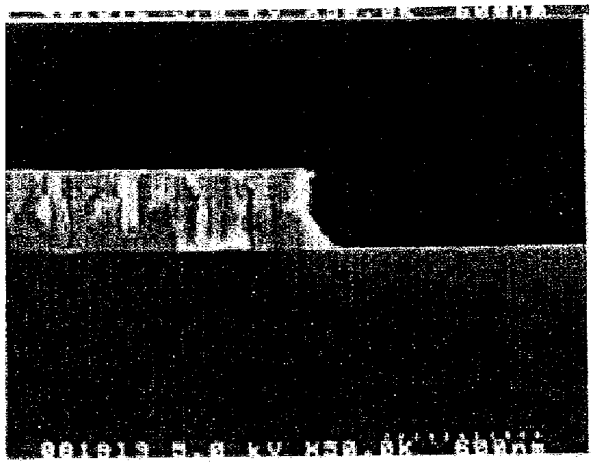


FIG. 14

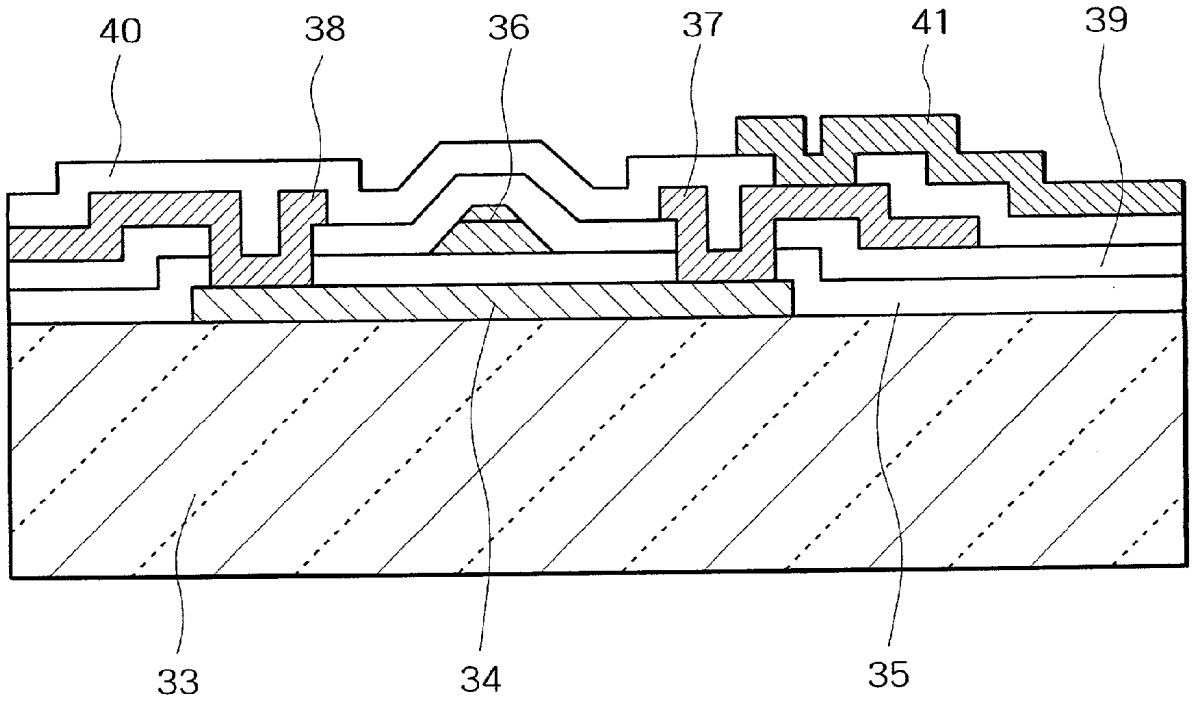


FIG. 15

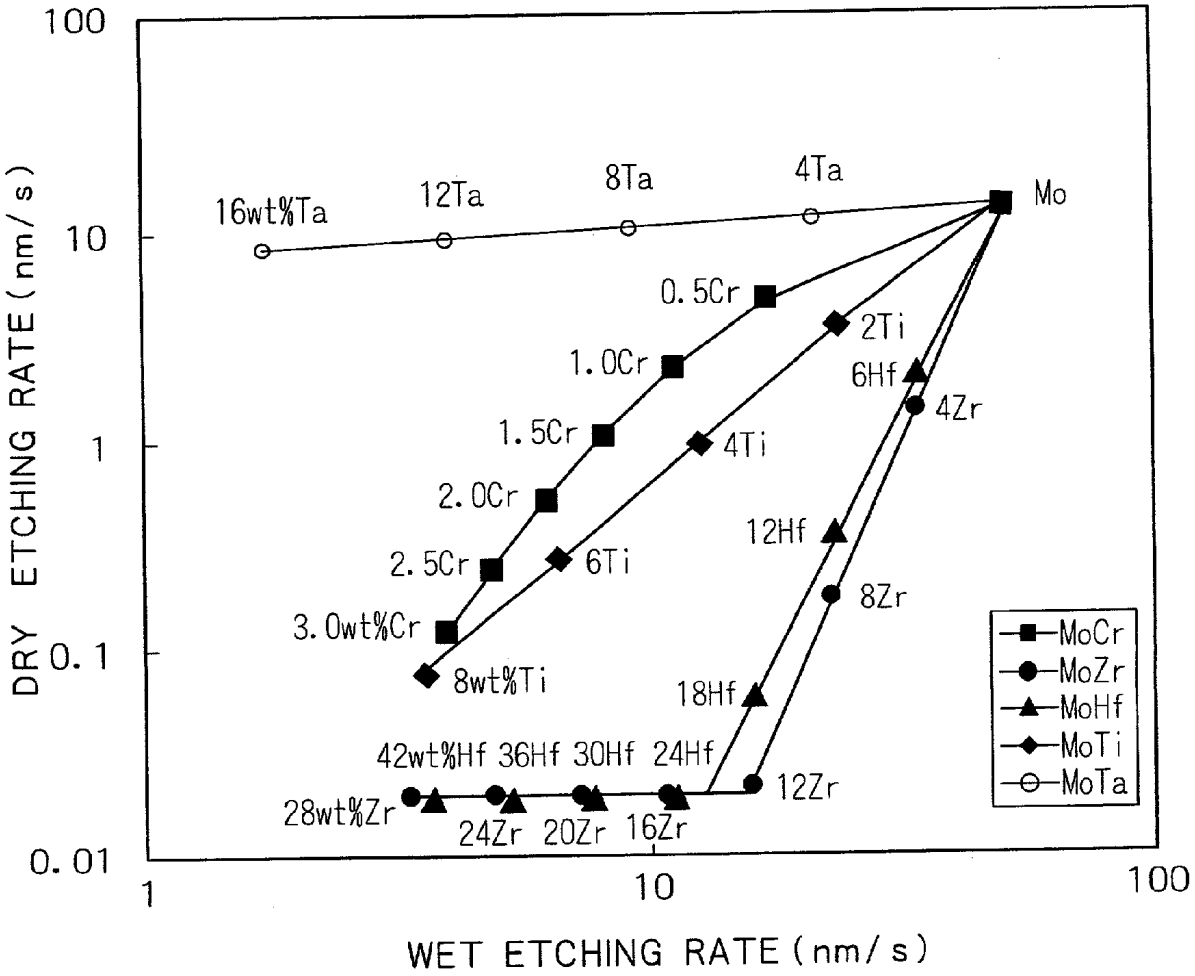

100
10
1
0.1
0.01
DRY ETCHING RATE (nm/s)
1
10
100
WET ETCHING RATE (nm/s)
16wt%Ta
12Ta
8Ta
4Ta
Mo
0.5Cr
1.0Cr
1.5Cr
2.0Cr
2.5Cr
3.0wt%Cr
2Ti
4Ti
6Ti
8wt%Ti
6Hf
4Zr
12Hf
8Zr
18Hf
12Zr
42wt%Hf 36Hf 30Hf 24Hf
28wt%Zr
24Zr 20Zr 16Zr
MoCr
MoZr
MoHf
MoTi
MoTa

FIG. 16

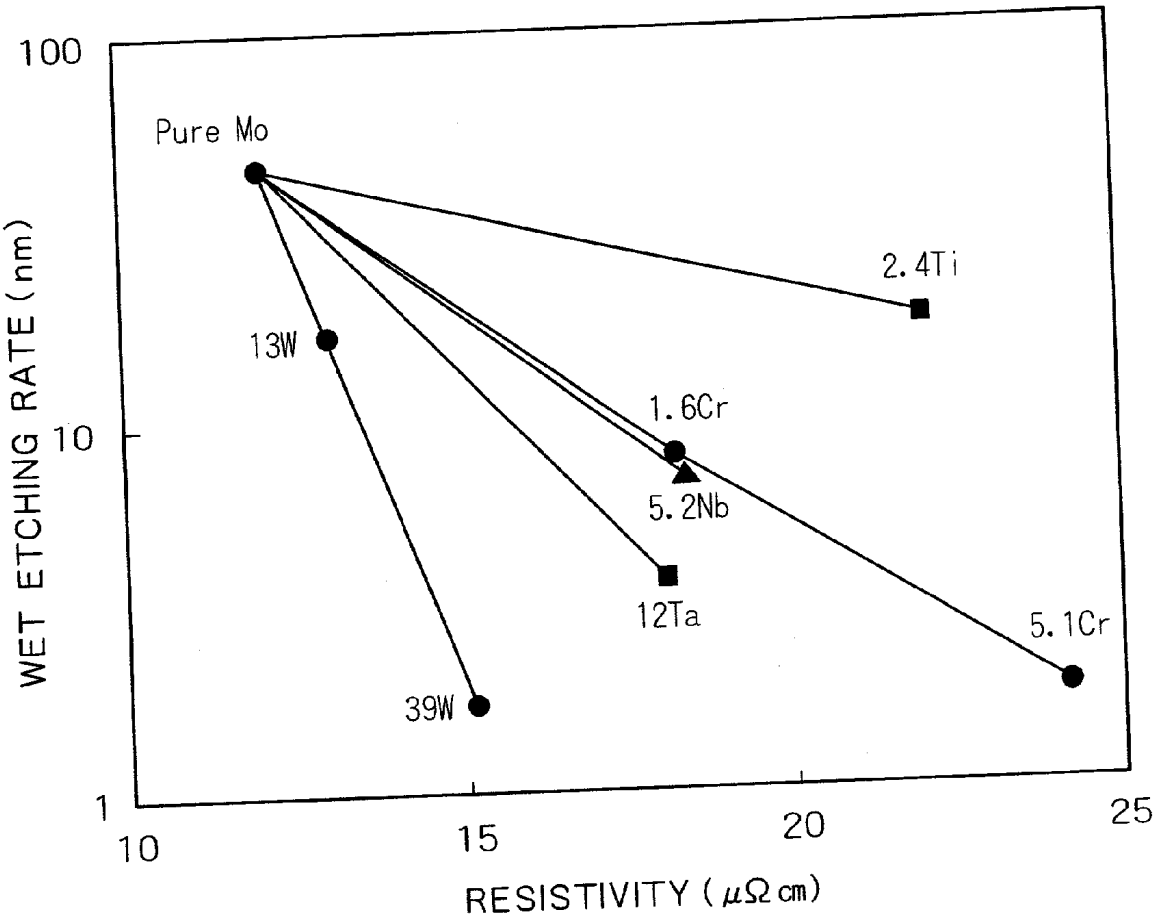
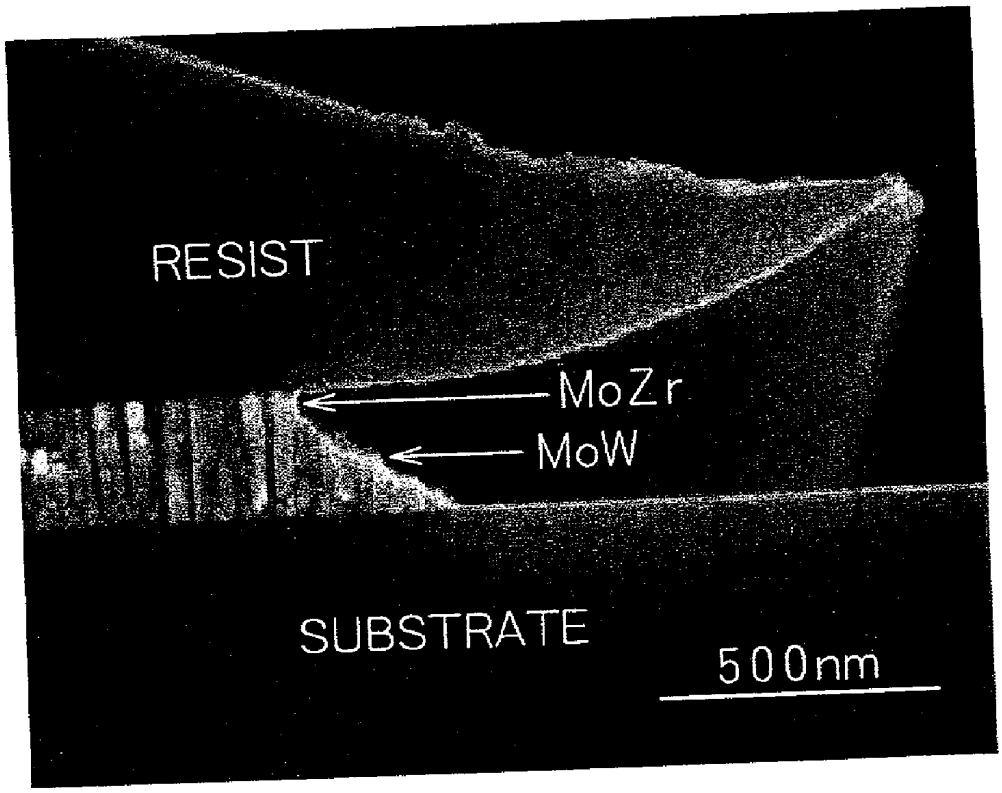

100
10
1
WET ETCHING RATE (nm)
Pure Mo
2.4Ti
13W
1.6Cr
5.2Nb
12Ta
5.1Cr
39W
10
15
20
25
RESISTIVITY (μΩ cm)

FIG. 17



LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] The present invention relates to an active matrix type liquid crystal display device (AM-LCD) driven by thin film transistors (TFT) and a manufacturing method thereof.

[0002] As image display devices that can be reduced in thickness and weight and attain high definition, a market has been expanded for thin film transistor-driven liquid crystal display devices (TFT-LCD) instead of existent cathode ray tubes. The TFT-LCD comprises scanning signal lines, image signal lines, thin film transistors formed in the vicinity of intersections between the scanning signal lines and the image signal lines, pixel electrodes connected with the thin film transistors, a gate insulative film and a protection film formed on a glass substrate, a counter substrate and a liquid crystal layer put between the glass substrate and the counter substrate. In recent years, along with an increasing size and improved definition of a screen of TFT-LCD, specifications required for a reduction in resistance for scanning signal lines and image signal lines and production yields have become more and more severe. Further, it has also been demanded to reduce the production cost by simplifying the production steps.

[0003] For the image signal lines of the bottom gate type amorphous silicon TFT-LCD, those comprising a single layer of a metal film such as Ti, Ta, Cr, Mo and CrMo or those of a laminated metal films such as Mo/Cr, Al/Ti, CrMo/Cr, Mo/Al/Mo, Ti/Al/Ti, Cr/Al/Cr and MoCr/Al/MoCr have been adopted. In the foregoing, the slash (/) represents the constitution of laminated films in which an upper layer is indicated on the left and a lower layer is indicated on the right of the slash. Such wiring constitutions are properly selected depending on wiring resistance specifications required for liquid crystal driving, production performance of a sputtering step, performance of an etching apparatus, and so on.

[0004] Among them, the constitution capable of obtaining the lowest wiring resistance can include, employing Al, Al/Ti, Mo/Al/Mo, Ti/Al/Ti, Cr/Al/Cr and MoCr/Al/MoCr and the similar constitution capable of obtaining the second lowest wiring resistance can include, employing pure Mo, Mo and Mo/Cr. Incidentally, Ti or Mo is laminated as an upper or a lower layer on Al, such as in Ti/Al/Ti or Mo/Al/Mo, in order to improve contact with silicon constituting a thin film transistor and a pixel electrode comprising indium oxide or the like as the main ingredient. Further, those simple constitutions providing lowest load on the sputtering step can include single-layered constitutions of Ti, Ta, Cr, Mo or CrMo, and the similar constitutions for providing the second lowest load can include two-layered constitution of Mo/Cr, Al/Ti. Further, the constitutions capable of selective wet etching for a gate insulative film without the use of a hydrofluoric system etching solution can include Cr, Mo, CrMo, Al/Cr, Mo/Al/Mo, Cr/Al/Cr and MoCr/Al/MoCr. Further, those constitutions capable of forming through holes in the protection insulative film substantially covering a drain electrode and a source electrode without eliminating the wiring film can include Cr, CrMo, Mo/Cr, CrMo/Cr, Cr/Al/Cr and MoCr/Al/MoCr.

[0005] The constitutions of the image signal lines described above have respective features as described previously but constitutions capable of simultaneously satisfying requirements for reduced wiring resistance, a reduced load on the sputtering step, selective wet etching for the gate insulative film, and formation of the through hole in the protection insulative film by dry etching have not yet been known.

[0006] For example, Ti has a high resistivity and since buffered hydrofluoric acid is used for wet etching for Ti, selective wet etching with respect to the gate insulative film is difficult. Further, Ta has high resistivity and since buffered hydrofluoric acid is used for wet etching for Ta, selective wet etching with respect to the gate insulative film is difficult, further, and since it is etched with an SF_6 gas, formation of the through holes in the protection insulative film by dry etching is difficult. Further, Cr, CrMo, and CrMo/Cr each have high resistivity. Further, since Mo is etched by the SF_6 gas, formation of the through hole in the protection insulative film by dry etching is difficult. Since a Mo layer is dissolved abnormally rapidly upon wet etching in Mo/Cr, patterning is difficult. Since it is necessary for Al/Ti that the through hole has to be formed by dry etching in the protection insulative film and Al has to be etched, the step is complicate. Further, for Mo/Al/Mo, since Mo as a cap layer is etched by an SF_6 gas, and formation of the through hole in the protection insulative film by dry etching is difficult and also requires three-layered deposition, it gives a large load on the sputtering step. Similarly, since Ti/Al/Ti, Cr/Al/Cr and MoCr/Al/MoCr each require the deposition of three layers, they impose a great load on the sputtering step.

SUMMARY OF THE INVENTION

[0007] A first subject of this invention is to attain a constitution of image signal lines capable of simultaneously satisfying the requirements of reduced wiring resistance, a reduced load on a sputtering step, selective wet etching relative to a gate insulative film, formation of a through hole in a protection insulative film by dry etching, and favorable contact with silicon of a thin film transistor and a transparent conductive film constituting a pixel electrode and provide a liquid crystal display device adopting the same. An aimed value for the wiring resistance is assumed as 170 nΩ/m or lower of an average conductivity defined as a product of sheet resistance and an entire film thickness. This average conductivity is at a level lower than 180 nΩ/m that can be attained with a single Cr layer film or single CrMo layer film.

[0008] An aimed reduction in load imposed on the sputtering step is that the number of laminated layers is two or less. The selective wet etching with respect to the gate insulative film is that etching can be conducted with a chemical solution excluding those chemically attacking the gate insulative film such as a buffered hydrofluoric acid or an alkali solution giving damage to a resist. Further, from the viewpoint of the simplicity of the steps, it is a necessary condition that upper and lower layers can be etched simultaneously on the wiring constitution of laminated layers. Further, it is a necessary condition that the cross section of the wirings can be fabricated into a tapered shape. For the formation of the through hole in the protection insulative film by dry etching, it is necessary that the contact layer of wirings has durability to dry etching using an SF_6 gas for forming contact between the wirings and the pixel electrode. As a matter of fact, it is difficult to use an alloy comprising Al as a main ingredient for the contact layer.

[0009] A second subject of this invention is, in addition to the solution of the foregoing first subject, to provide good matching property with a process for forming scanning signal lines. Since particularly lowered resistance is required for the scanning signal lines, it is desirable that a film constituting them is a laminated film containing an alloy comprising aluminum as the main ingredient. When the etching solution for fabricating the same and that for fabricating the image signal lines can be used in common, it is preferred in view of a reduction in the manufacturing cost.

[0010] According to a first aspect of the present invention, a liquid crystal display device comprises: a pair of substrates; a liquid crystal layer put between the pair of substrates; a plurality of scanning signal lines formed on one of the pair of substrates; a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement; thin film transistors formed in the vicinity of intersections of the scanning signal lines and the image signal lines; pixel electrodes connected with the thin film transistors; a gate insulative film substantially covering the scanning signal lines; and a protection insulative film substantially covering the image signal lines and the thin film transistors, wherein at least one of the signal lines of the scanning signal lines and the image signal lines is made of a two-layered film of a first conductive film as a lower layer and a second conductive film as an upper layer, the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film is made of an alloy comprising molybdenum as a main ingredient and containing zirconium.

[0011] Preferably, the first conductive film may be made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film may be made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

[0012] Preferably, average conductivity defined as a product of sheet resistance and the entire film thickness of the two-layered film may be 170 nΩ/m or less.

[0013] Preferably, a cross section at a fabrication end of the first conductive film may form a forwardly tapered shape.

[0014] Preferably, the first conductive film may be made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film may be made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

[0015] Preferably, average conductivity defined as a product of sheet resistance and the entire film thickness of the two-layered film may be 170 nΩ/m or less.

[0016] Preferably, a cross section at a fabrication end of the first conductive film may form a forwardly tapered shape.

[0017] According to a second aspect of the invention, a liquid crystal display device comprises: a pair of substrates; a liquid crystal layer put between the pair of substrates; a plurality of scanning signal lines formed on one of the pair of substrates; a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement; thin film transistors formed in the vicinity of intersections between the scanning signal lines and the image signal lines; pixel electrodes connected with the thin film transistors; a gate insulative film substantially covering the scanning signal lines; and a protection insulative film substantially covering the image signal lines and the thin film transistors, wherein the image signal lines and a source and drain electrodes of the thin film transistor are made of a two-layered film of a first conductive film as a lower layer and a second conductive film as an upper layer, the first conductive film is directly connected with silicon constituting the thin film transistor, the second conductive film is directly connected with the pixel electrode by way of a through hole disposed in the protection insulative film, the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film is made of an alloy containing zirconium.

[0018] Preferably, the first conductive film may be made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film may be made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

[0019] Preferably, average conductivity defined as a product of sheet resistance and the entire film thickness of the two layered film may be 170 nΩ/m or less.

[0020] Preferably, a cross section at a fabrication end of the first conductive film may form a forwardly tapered shape. Preferably, the scanning signal lines may be made of a laminated film of an alloy comprising aluminum as a main ingredient and an alloy comprising molybdenum as a main ingredient.

[0021] Preferably, the pixel electrode may be made of a mixed oxide of indium oxide, tin oxide and zinc oxide.

[0022] According to a third aspect of the invention, a liquid crystal display device comprises: a pair of substrates; a liquid crystal layer put between the pair of substrates; a plurality of scanning signal lines formed on one of the pair of substrates; a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement; thin film transistors formed in the vicinity of intersections of the scanning signal lines and the image signal lines; a gate insulative film substantially covering the scanning signal lines; a protection insulative film substantially covering the image signal lines and the thin film transistors; at least a pair of pixel electrodes and counter electrodes formed on one of the pair of substrates within a plurality of pixels formed in regions surrounded with the plurality of scanning signal line and the plurality of image signal lines, wherein an image signal is supplied to the pixel electrode by way of the thin film transistor driven based on the supply of a scanning signal from the scanning signal line, a reference voltage is supplied to the counter electrode by way of the counter voltage signal line formed over the plurality of pixels, the pixel electrode made of a two-layered film of a first conductive film as a lower layer and a second conductive film as an upper layer, the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film is made of an alloy containing zirconium.

[0023] Preferably, the first conductive film may be made of an alloy comprising molybdenum as a main ingredient

and containing tungsten, and the second conductive film is made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

[0024] Preferably, average conductivity defined as a product of sheet resistance and the entire film thickness of the two layered film may be 170 nΩ/m or less.

[0025] Preferably, a cross section at a fabrication end of the first conductive film may form a forwardly tapered shape.

[0026] According to a fourth aspect of the invention, a liquid crystal display device comprises: a pair of substrates; a liquid crystal layer put between the pair of substrates; a plurality of scanning signal lines formed on one of the pair of substrates; a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement; thin film transistors formed in the vicinity of intersections between the scanning signal lines and the image signal lines; pixel electrodes connected with the thin film transistors; a gate insulative film substantially covering polycrystal silicon of the thin film transistors; an interlayer insulative film for substantially covering the scanning signal lines and insulating the scanning signal lines from the image signal lines; a protection insulative film substantially covering the image signal lines, wherein the gate electrodes of the thin film transistors may be made of a two-layered film of a first conductive layer as a lower layer and a second conductive layer as an upper layer, the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and the second conductive film is made of an alloy containing zirconium.

[0027] The subject of this invention can be solved by the constitutions described above. The reasons will be described below.

[0028] Metal elements with relatively low resistivity can include, Ag, Cu, Al, Mo and W when poisonous elements and those elements which are considered to be difficult for film deposition by sputtering such as noble metals, alkali metals, alkaline earth metals and ferromagnetic materials are excluded from the metal elements in the periodical table. Among them, Ag, Cu and Al each have poor contact with silicon of a thin film transistor or a transparent conductive film that constitutes a pixel electrode and they require the so-called barrier metal or cap metal. That is, for connecting Ag, Cu or Al with silicon and the transparent conductive film, it is necessary to laminate Mo or the like on an upper layer and a lower layer of Ag, Cu or Al. In this case, a metal film has a three-layered constitution, which remarkably increases a load imposed on a sputter film deposition step.

[0029] Further, W requires a buffered hydrofluoric acid or alkali solution for wet etching fabrication. However, the former buffered hydrofluoric acid damages the glass substrate or SiN of the gate insulative film, while the latter damages the resist, so that it is difficult to use them for the wiring forming step.

[0030] As a result of the screening described above, Ag, Cu, Al and W have been judged not suitable regarding the subject of the invention and remaining Mo and alloys thereof with a high melting metal (Ti, Cr, Zr, Nb, Hf, Ta and w) require no barrier metal or cap metal and can be wet etched by using a mixed acid of phosphoric acid—nitric acid. However, pure Mo has no durability to SF_6 dry etching upon fabrication of through holes in the SiN film. Further, it is difficult that the wiring cross section is fabricated into a tapered shape by wet etching. In view of the above, laminating and alloying of the wiring film are considered with the following approach.

[0031] At first, for forming the wiring cross section into a tapered shape the upper layer, in the two-layered film, is provided with a relatively high wet etching rate and formed as a relatively thin film, while the lower layer is provided with a relatively low wet etching rate and formed as a relatively thick film. Further, the upper layer is provided with durability to dry etching, while the lower layer is adapted to serve as a conductive layer. That is, the upper layer is required for a high wet etching rate and high dry etching durability, while the lower layer is required for a low wet etching rate and low resistivity. The present inventors have made a study of the property of alloys formed by adding a second element to Mo and have found Mo alloys capable of satisfying the foregoing required characteristics.

[0032] **FIG. 15** shows a wet etching rate and SF_6 dry etching rate of Mo alloys with addition of Ta, Cr, Ti, Hf and Zr to Mo. For each of the additive elements, the wet etching rate and the dry etching rate are lowered as the addition amount increases. Although not illustrated, when W or Nb is added to Mo, similar trace as in a case of adding Ta is obtained. Among the additive elements, Zr is an additive element having the greatest ratio for the reduction amount of dry etching rate relative to the reduction amount of wet etching rate and Hf is next to Zr. When material cost is considered for Zr and Hf, Hf is outstandingly expensive. Accordingly, the optimum element as the upper layer for the two-layered film is an alloy formed by adding Zr to Mo. In order to provide the image signal line with required dry etching durability, it is desirable that Zr is added by 4% by weight or more.

[0033] **FIG. 16** shows the wet etching rate and the resistivity of the Mo alloys with addition of W, Ta, Nb, Hf and Zr to Mo. In each of the additive elements, the wet etching rate lowers and the resistivity increases as the addition amount increases. Among the additive elements, W is an additive element showing a minimum increasing ratio of the resistivity to the reduction amount of the wet etching rate and Ta is next to W. Although not illustrated, Zr and Hf are additive elements showing an extremely large increasing ratio of the resistivity to the reduction amount of the wet etching rate. In view of the foregoing, the optimal lower layer for the two-layered film is made of an alloy with addition of W to Mo. The addition amount of W in the MoW alloy as the lower layer depends on the Zr addition amount in the MoZr alloy for the upper layer. That is, in order to provide a wiring cross section having a favorable tapered shape, W has to be added within such a range that the wet etching rate for the lower layer is less than that for the upper layer and at an addition amount as less as possible so as to decrease a rise in the resistivity.

[0034] **FIG. 17** illustrates a cross sectional shape of a two-layered film comprising the MoZr alloy for the upper layer and the MoW alloy for the lower layer as described above which is subjected to wet etching. It is wet etched into a tapered cross sectional shape in which the MoZr layer as the upper layer is retracted. The etching solution is a mixed acid containing phosphoric acid—nitric acid used as an

aluminum etching solution, and when a film containing an aluminum alloy is used for the scanning signal lines, the etching solution can be used in common.

[0035] Further, when a film containing an aluminum alloy is used for the scanning signal line, the yield in view of the disconnection of the scanning signal line is worsened when polycrystal indium tin oxide is adopted for the pixel electrode. This is because dissolution disconnection is caused by intrusion of an intense halogenic acid such as hydrobromic acid asian etching solution for the polycrystal indium tin oxide as far as scanning signal lines. Dissolution disconnection is essentially eliminated by adopting an amorphous transparent conductive film such as made of a mixed oxide of indium oxide, tin oxide and zinc oxide as the pixel electrode and changing the etching solution with a mild etchant such as oxalic acid. Contact characteristics between mixed oxide of indium oxide, tin oxide and zinc oxide and the MoZr alloy described above are favorable and the transparent conductive film can be adopted as the pixel electrode.

[0036] In the case of the scanning signal lines, since there is no requirement for considering contact with silicon, an aluminum alloy of lower resistance can be adopted as the lower layer for the wiring film. However, when the polycrystal indium tin oxide is used as the pixel electrode as described above, the use of the aluminum alloy is not desirable in view of the disconnection yield. The advantage of adopting the polycrystal indium tin oxide is that the connection resistance is low and stable at the wiring terminal formed simultaneously with the pixel electrode. In this case, it is possible to apply the two-layered film constitution in which the upper layer is made of the MoZr alloy and the lower layer is made of the MoW alloy as described above to the scanning signal line. As described above, in the case of the two-layered film constitution, since the tapered shape at the fabrication end is satisfactory, the coverage and the image signal line overriding characteristics of the gate insulative film are improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] **FIG. 1** is a plan view showing a constitution of a main portion of a pixel in a liquid crystal display device according to an embodiment of the invention;

[0038] **FIG. 2** is a cross sectional view showing a constitution of a main portion of the constitution of a pixel in a liquid crystal display device according to an embodiment of the invention;

[0039] **FIG. 3** is a diagram of an equivalent circuit in a liquid crystal display device according to an embodiment of the invention;

[0040] **FIGS. 4A and 4B** are constitutional views of a main portion (terminal portion) of a liquid crystal display device according to an embodiment of the invention;

[0041] **FIGS. 5A through 5D** are step charts showing an embodiment of a manufacturing method of a liquid crystal display device according to this invention which is to be combined with **FIG. 6**, **FIG. 7**, **FIG. 8** and **FIG. 9**;

[0042] **FIGS. 6A through 6D** are step charts showing an embodiment of a manufacturing method of a liquid crystal display device according to this invention which is to be combined with **FIG. 5**, **FIG. 7**, **FIG. 8** and **FIG. 9**;

[0043] **FIGS. 7A through 7D** are step charts showing the embodiment of the manufacturing method of the liquid crystal display device according to the invention which is to be combined with **FIG. 5**, **FIG. 6**, **FIG. 8** and **FIG. 9**;

[0044] **FIGS. 8A through 8D** are step charts showing the embodiment of the manufacturing method of the liquid crystal display device according to the invention which is to be combined with **FIG. 5**, **FIG. 6**, **FIG. 7** and **FIG. 9**;

[0045] **FIGS. 9A through 9D** are step charts showing the embodiment of the manufacturing method of the liquid crystal display device according to this invention which is to be combined with **FIG. 5**, **FIG. 6**, **FIG. 7** and **FIG. 8**;

[0046] **FIG. 10** is a cross sectional view showing a constitution of a main portion of a pixel in a liquid crystal display device according to an embodiment of this invention;

[0047] **FIG. 11** is a plan view showing a constitution of a main portion of a pixel in a liquid crystal display device according to the embodiment of this invention;

[0048] **FIG. 12** is a photograph showing an example of display defects in a liquid crystal display device;

[0049] **FIG. 13** is a photograph showing in cross section an example of a pixel electrode in a liquid crystal display device showing the display defect in **FIG. 12**;

[0050] **FIG. 14** is a cross sectional view showing a constitution of a main portion of a pixel in a liquid crystal display device according to an embodiment of the invention;

[0051] **FIG. 15** is a graph showing characteristics data of materials intended to be used for signal lines in a liquid crystal display device;

[0052] **FIG. 16** is a graph showing characteristics data of materials intended to be used for signal lines in a liquid crystal display device; and

[0053] **FIG. 17** is a graph showing characteristics data of materials intended to be used for signal lines in a liquid crystal display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0054] (Embodiment 1)

[0055] <Equivalent Circuit>

[0056] **FIG. 3** is an equivalent circuit diagram showing a structure of a liquid crystal display device according to Embodiment **1** of this invention. While **FIG. 3** is a circuit diagram, it is drawn corresponding to an actual geometrical arrangement.

[0057] In Embodiment 1 of **FIG. 3, a** transparent substrate **1** and a transparent substrate **2** are opposed to each other with a liquid crystal layer put therebetween.

[0058] At the surface of a transparent substrate **1** on the side of liquid crystals, are formed gate (scanning) signal lines **4** extended in the direction x and arranged in parallel with each other along the direction y, and drain (image) signals lines **5** extended in the direction y while being

insulated from the gate signal lines **4** and arranged in parallel with each other along the direction x. A rectangular region surrounded by the gate (scanning) signal lines **4** and the drain (image) signal lines **5** constitutes a pixel region. Pixel regions are collected to constitute a display section.

[**0059**] A thin film transistor **6** driven by a scanning signal (voltage) from one of the gate signal lines **4** and a pixel electrode **7** supplied with an image signal (voltage) from the drain signal line **5** by way of the thin film transistor **6** are formed in each of the pixel regions.

[**0060**] Since the length of the signal line increases as the size of the liquid crystal display device increases, the resistance of the gate signal line **4** and the drain signal line **5** is increased. Further, since the signal line width decreases as the definition of the liquid crystal display device becomes finer, the resistance of the gate signal line **4** and drain signal line **5** is increased. Then, when the resistance of the signal lines **4** and **5** is increased, since the voltage waveform of the scanning signal and the image signal becomes dull, no sufficient signal voltage is supplied to the thin film transistor **6**. As a result, significant deterioration occurs in image quality such as gradient of brightness.

[**0061**] Further, a capacitance element **8** is formed between the pixel electrode **7**, and one of the gate signal lines **4** adjacent to the other gate signal line **4**. The capacitance element **8** stores the image signal supplied to the pixel electrode **7** for a long time when the thin film transistor **6** is turned off.

[**0062**] The pixel electrode **7** in each of the pixel regions generates an electric field between counter electrodes (not illustrated) and the same to control the light transmittance of the liquid crystals between each of the electrodes. The counter electrodes are formed in common with each of the pixel regions on the surface of the other transparent substrate **2**, which is opposed by way of the liquid crystal, on the side of the liquid crystals.

[**0063**] One end of each gate signal line **4** extends to one side (left side in the drawing) of the transparent substrate. A terminal portion **10** to be connected with bumps of a semiconductor integrated circuit **9** of a vertical scanning circuit mounted on the transparent substrate **1** is formed at the extended portion of each gate signal line **4**.

[**0064**] One end of each drain signal line **5** extends to one side (upper side in the drawing) of the transparent substrate **1**. A terminal portion **12** to be connected with bumps of a semiconductor integrated circuit **11** of an image signal driving circuit mounted on the transparent substrate **1** is formed at the extended portion of each drain signal line **5**.

[**0065**] The semiconductor integrated circuits **9** and **11** are completely mounted, respectively, on the transparent substrate **1** by the so-called COG system.

[**0066**] Respective bumps on the input side of the semiconductor integrated circuit **9** and **11** are connected to terminal portions **13** and **14** formed on the transparent substrate **1**. The terminal portions **13** and **14** are connected by way of wiring layers **15** and **16** with terminal portions **17** and **18**, respectively, which is disposed on the periphery of the transparent substrate **1** at a portion nearest to the end face.

[**0067**] The transparent substrate **2** is opposed to the transparent substrate **1** so as to keep off a region in which the semiconductor integrated circuit is mounted and has a smaller area than that of the transparent substrate **1**.

[**0068**] The transparent substrate **2** is secured to the transparent substrate **1** by means of a sealing material **47** formed on the periphery of the transparent substrate **2**. The sealing material also has a function of encapsulating liquid crystals between the transparent substrates **1** and **2**.

[**0069**] In the explanation of the structure described above, while the liquid crystal display device by the COG system has been explained, this invention is applicable also to a liquid crystal display device of a TCP (Tape Carrier Package) system. The TCP system is a packaging system for forming a pattern by photolithography on a flexible tape to form a tape carrier and mounting a semiconductor integrated circuit chip by a TAB method (Tape Automated Bonding). Output terminals of the package are connected with a terminal portion formed on a transparent substrate SUB1 and input terminals thereof are connected to a terminal portion on a printed substrate disposed in the vicinity of the transparent substrate **1**.

[**0070**] <Structure of Pixel>

[**0071**] Referring further to **FIG. 1** and **FIG. 2**, **FIG. 1** is a plan view showing a structure of an pixel region of the transparent substrate **1**, which correspond to a portion indicated by a dotted frame a in **FIG. 3**. **FIG. 1** is a cross sectional view showing a structure taken along line IV-IV in **FIG. 1**.

[**0072**] In **FIGS. 1 and 2**, the gate signal lines **4** extended in the direction X and arranged in parallel with the direction y are formed on the surface of the transparent substrate **1** on the side of the liquid crystals.

[**0073**] The gate signal line **4** has a two-layered structure in this Embodiment 1 in which a lower layer is, for example, made of an alloy layer comprising Al as a main ingredient while an upper layer is made of an alloy layer comprising Mo as a main ingredient such as MoZr alloy.

[**0074**] Such two-layered structure can provide an effect of greatly lowering the wiring resistance of the gate signal lines and forming the cross section into a forwardly tapered shape upon etching. Other effects will be apparent by subsequent explanations.

[**0075**] An insulative film **19**, for example, made of SiN is formed on the surface of the transparent substrate **1** so as to cover the gate signal line **4**. The insulative film **19** functions as an interlayer insulative film for the drain signal line **5** to be described later with respect to the gate signal line **4**, functions as a gate insulative film for a thin film transistor **6** to be described later and functions as a dielectric film for the capacitance element **8** to be described later.

[**0076**] A semiconductor layer **20**, for example, made of a-Si is formed at a lower left portion of the pixel region that overlaps with the gate signal line **4**. When a source electrode **21** and a drain electrode **22** are formed on the upper surface of the semiconductor layer **20**, a semiconductor layer of an MIS type thin film transistor **6** having a portion of the gate signal line **4** as a gate electrode is formed.

[**0077**] The source electrode **21** and the drain electrode **22** of the thin film transistor **6** are formed simultaneously with

the drain signal line **5** formed on the insulative film **19**. That is, when a portion of the drain signal lines **5** extended in the direction y and arranged in parallel with the direction x in **FIG. 1** are formed by being extended as far as the upper surface of the semiconductor layer **20**, the extended portion forms the drain electrode **22** of the thin film transistor **6**. In this case, an electrode formed being spaced apart from the drain electrode **22** constitutes the source electrode **21**. Since the source electrode **21** is connected with a pixel electrode **7** to be described later, it has an extended portion being extended somewhat to a central portion of the pixel region in order to ensure the connection portion.

[**0078**] The drain signal line **5** has a two-layered structure in this Embodiment 1 in which a lower layer thereof is a relatively thick layer made of an MoW alloy layer (for example, 17 wt % W content) and an upper layer thereof is a relatively thin layer made of an MoZr alloy layer (for example, 8 wt % Zr content).

[**0079**] The upper layer is made of the MoZr alloy layer, in order to provide durability to dry etching by fluorine plasmas upon forming a contact hole **24** in a protection insulative film **23** and so as not to eliminate the source electrode **21**. It also serves as a contact with the pixel electrode **7**. The lower layer is made of the MoW alloy layer, in order to lower the resistance of the drain signal lines **5**. It also serves as the contact with the semiconductor layer **20** of the thin film transistor **6**. Further, the MoZr alloy has less wet etching rate compared with MoW and such a two-layered film enables tapering fabrication.

[**0080**] A semiconductor layer doped with impurities is formed at the interface between each of the drain electrode **22** and the source electrode **21** and the semiconductor layer **20**. The doped semiconductor layer functions as a contact layer **48**.

[**0081**] A protection insulative film **23**, for example, made of SiN is formed on the surface of the transparent substrate **1** formed with the drain signal line **5** (drain electrode **22**, source electrode **21**) as described above to cover the drain signal lines **5** and so on. The protection insulative film **23** is disposed so as to avoid direct contact of the thin film transistor **6** with the liquid crystals.

[**0082**] A contact hole **24** is formed by dry etching of fluorine plasmas with an aim of exposing a portion of the extended portion of the source electrode **21** of the thin film transistor **6** and causing the portion to connect with the pixel electrode **7** described later.

[**0083**] A transparent electrode **7** is formed on the upper surface of the protective insulative film **23** while covering most of the portion of the pixel region. The transparent electrode **7** is made of any of indium-tin-zinc oxide (ITZO) film, indium-tin oxide (ITO) film, indium zinc oxide (IZO) film or indium germanium oxide (IGO) film. ITZO is employed in this embodiment. Since ITZO is deposited as an amorphous film, it can be fabricated by a mild etching solution such as oxalic acid. Accordingly, even when an alloy comprising Al as a main ingredient is used for the gate signal lines **4** as in this embodiment, reduction of yield by dissolution disconnection does not occur. The pixel electrode **7** is formed so as to cover also the contact hole **24** of the protective insulative film **23** and connected with the MoZr alloy of the source electrode **21** of the thin film transistor **6**. The contact resistance between ITZO and MoZr alloys is low and favorable electric connection can be obtained.

[**0084**] On the surface of the transparent substrate **1** in which the pixel electrode **7** is formed as described above, an orientation film **25** is formed also covering the pixel electrode **7**. The orientation film **25** is made, for example, of a resin and a rubbing treatment is applied in a certain direction to the surface thereof. The orientation film **25** is in contact with the liquid crystal layer **3** to determine the initial orientation direction of the liquid crystal molecular.

[**0085**] A polarization plate **26** is mounted on the surface of the transparent substrate **1** on the side opposite to the liquid crystal layer **3**.

[**0086**] On the other hand, a black matrix **27** is formed at the surface of the transparent electrode substrate **2** on the side of the liquid crystals so as to define each of the pixel regions. The black matrix **27** is disposed so as to prevent irradiation of external light to the thin film transistor **6** and improve the contrast of display.

[**0087**] Further, a color filter **28** having a color corresponding to each pixel region is formed at an opening that forms a light transmitting region and forms a substantial pixel region. For the color filter **28**, filters of an identical color are used in each of pixel regions arranged in parallel with the direction y, and filters of red (R), green (G) and blue (B) are sequentially arranged repeatedly on every pixel regions in the direction x.

[**0088**] A planarization film **29** comprising a resin formed, for example, by coating is disposed to the surface of the transparent substrate **2** formed with the black matrix **27** and the color filters **28** while covering also the black matrix **27** so that a step caused by the black matrix **27** and the color filter **28** does not appear on the surface.

[**0089**] A counter electrode **30** made, for example, of ITO is formed in common with each of the pixel regions on the surface of the planarization film **20**. The counter electrode **30** generates an electric field corresponding to the image signal (voltage) between the pixel electrode **7** in each of the pixel regions and the same so as to control the direction of orientation in the liquid crystal molecular and control the light transmittance based on appropriate combination of the polarization plate **26** described previously and a polarization plate **31** to be described subsequently.

[**0090**] Further, an orientation film **32** is formed on the surface of the transparent electrode **2** covering the counter electrode **30**. The orientation film **32** is made, for example, of a resin and subjected to a rubbing treatment in a certain direction on the surface thereof. The orientation film **32** is in contact with the liquid crystal layer **3** and determines the initial orientation direction of the liquid crystal molecular.

[**0091**] A polarization plate **31** is mounted on the surface of the transparent substrate **2** on the side opposite to the liquid crystal layer **3**.

[**0092**] <Constitution of Terminal Portion>

[**0093**] **FIGS. 4A and 4B** are views showing the constitution of the drain terminal portion **12**, in which **FIG. 4A** is a plan view showing two out of plural drain terminal

portions **12** formed in parallel with one another and **FIG. 4B** is a cross sectional view taken along line b-b in **FIG. 4A**.

[**0094**] At first, drain signals **5** extending from the display section are formed on the surface of the transparent substrate **1**.

[**0095**] The drain signal line **5** comprises a two-layered film having the upper layer made of the MoZr alloy and the lower layer made of the MoW alloy as described previously.

[**0096**] The drain signal **5** is initially covered with the protection insulative film **23** made of SiN and then exposed from the protection insulative film **23** by boring a hole in a region for forming the terminal portion.

[**0097**] The boring in the protection insulative film **23** is preferably conducted by fluoro-dry etching gas. The dry etching is excellent compared with wet etching in view of fabrication accuracy and controllability for the processing time and is advantageous for fabrication such as boring in the terminal portion and fabrication for the contact hole in the pixel portion. Further, the MoZr alloy as the upper layer of drain signal line **5** has a high dry etching durability and is not removed upon etching.

[**0098**] At the exposed portion of the signal line in the terminal portion, a conductive oxide film **42** made of an ITZO (Indium-Tin-Zinc-Oxide) film is laminated. As the material for the conductive oxide film **42**, an ITO (Indium-Tin-Oxide) film, an IZO (Indium-Zinc-Oxide) film or an IGO (Indium-Germanium-Oxide) film may be selected. However, while the ITO film is excellent in that the terminal connection resistance is low, it involves a problem of causing dissolution disconnection for the gate signal line using an Al alloy since the etching solution used for fabrication is a strong halogenic acid such as hydrobromic acid. On the other hand, while an IZO film or an IGO film does not bring about dissolution disconnection for the gate signal line using the Al alloy since the etching solution for the fabrication is a mild chemical such as oxalic acid, it involves a problem of tending to increase the terminal connection resistance. In some cases, COG mounting is difficult. When ITZO is adopted, the problems of the welding disconnection of the gate signal line and the terminal connection resistance can be overcome in a balanced manner.

[**0099**] Then, the drain terminal **12** thus constituted is connected, as shown in **FIG. 4**B, with a bump **44** of the semiconductor integrated circuit **11** by way of an anisotropic conductive film **43**. The anisotropic conductive film **43** comprises a sheet-like resin film containing many conductive particles and the bump **44** and the conductive material (conductive oxide film **42**) of the drain terminal portion **12** are electrically connected by way of the conductive particles by applying a certain pressure while interposing the resin film between the group of the drain terminal portions **12** and the semiconductor integrated circuit **11**.

[**0100**] <Manufacturing Method>

[**0101**] Next, the method of manufacturing the portions on the side of the transparent substrate **1** of the liquid crystal display device as described above is to be explained with reference to **FIGS. 5A through 5D** to **FIGS. 9A through 9D**. In each of **FIGS. 5A through 5D** to **FIGS. 9A through 9D**, are shown a thin film transistor portion (**FIGS. 5A through 9A**), a gate terminal portion (**FIGS. 5B through 9B**), a drain terminal portion (**FIGS. 5C through 9C**) and a flow of steps (**FIGS. 5D through 9D**).

[**0102**] **FIGS. 5A through 5D** to **FIGS. 9A through 9D** are divided corresponding to each of photolithographic steps in which each figure shows a stage where fabrication after photolithography is completed and a photoresist is removed. The photolithography means a series of operations from the coating of a photoresist, by way of the selective exposure using a mask and to the development thereof in this explanation, while saving duplicated explanations. A description is to be made in accordance with the divided steps.

[**0103**] First photolithographic step, **FIGS. 5A** to **5**D:

[**0104**] In each of the thin film transistor portion (**FIG. 5A**), gate terminal portion (**FIG. 5B**) and drain terminal portion (**FIG. 5C**), an AlNd alloy layer of 2000 Å in thickness is formed by sputtering on a transparent substrate **1** made of AN 635 glass (trade name) and, further, an MoZr alloy layer of 400 Å in thickness is further formed continuously by sputtering. After photolithography, the MoZr alloy layer and the AlNd alloy layer are etched collectively selectively by an etching solution comprising, for example, phosphoric acid, nitric acid, acetic acid, purified water or ammonium fluoride.

[**0105**] Thus, gate electrodes **45**, gate signal lines **4**, gate terminal portions **10**, terminal portions **13** on the input side of a semiconductor integrated circuit **9**, terminal portions **17** connected to the terminal portions **13** by way of a wiring layer **15**, terminal portions **14** on the input side of a semiconductor integrated circuit **11**, and terminal portions **18** connected to the terminal portions **14** by way of a wiring layer **16** are formed.

[**0106**] Second photolithographic step, **FIGS. 6A** to **6**D:

[**0107**] An ammonia gas, a silane gas and a nitrogen gas are introduced into a plasma CVD apparatus to form an insulative film **19** made of SiN having 3500 Å in thickness. Then, a silane gas and a hydrogen gas are introduced into the plasma CVD apparatus to form an intrinsic amorphous Si film **20** of 1200 Å in thickness is formed and, subsequently, a hydrogen gas and a phosphine gas are introduced into the plasma CVD apparatus to form N(+) amorphous Si film **48** of 300 Å in thickness.

[**0108**] After photolithography, the N(+) amorphous Si film **48**, and the intrinsic amorphous Si film **20** are selectively etched by using SF_6 and CCl_4 as dry etching gases to form an island shape semiconductor layers **20** and **48**.

[**0109**] Third photolithographic step, **FIGS. 7A** to **7**D:

[**0110**] An MoW alloy layer of 2100 Å in thickness is formed by sputtering and continuously an MoZr alloy layer of 400 Å in thickness is formed by sputtering. After the photolithographic step, the MoZr alloy layer and the MoW alloy layer are etched collectively selectively with an etching solution of an identical composition with that for the first lithography. Thus, drain signal lines **5**, source electrodes **21**, drain electrodes **22** and drain terminals **12** are formed.

[**0111**] The conductive film may be a three layered film comprising, for example, MoZr/AlNd/MoZr but it is not preferred in view of poor productivity requiring long film deposition time and a large scale film deposition apparatus required for film deposition to increase the investment cost.

[0112] Then, CCl_4 and SF_6 are introduced to a dry etching apparatus to selectively eliminate the N(+) semiconductor layer **48**.

[0113] Fourth photolithographic step, **FIGS. 8A** to **8D**:

[0114] An ammonia gas, a silane gas and a nitrogen gas are introduced into the plasma CVD apparatus to form a protection insulative film **23** made of SiN and having a film thickness of 0.4 μm. After the photolithography, the SiN film is selectively etched by using SF_6 as a dry etching gas to pattern the protection insulative film **23** and the insulative film **19**. Since MoZr has a sufficient dry etching durability, it is not removed by dry etching and the SiN film can be etched selectively.

[0115] Fifth photolithographic step, **FIGS. 9A** to **9D**:

[0116] A transparent conductive film comprising an ITZO film (Indium-Tin-Zinc-Oxide) of 1150 Å is formed by sputtering. After photolithography, the transparent conductive film is selectively etched with an aqueous solution comprising oxalic acid as a main ingredient for the etching solution to form pixel electrodes **7**, the uppermost layer **50** of the gate terminal portions **10**, the uppermost layer **42** of the drain terminal portions **12**, the uppermost layer of the terminal portions **13** and **14** on the input side of a semiconductor integrated circuit **9** and **11**, and the uppermost layer of the terminal portions **17** and **18** connected to the terminal portions **13** and **14** by way of a wiring layers **15** and **16**.

[0117] (Embodiment 2)

[0118] Embodiment 2 of this invention is to be explained referring to **FIG. 10**.

[0119] **FIG. 10** is a view showing a cross sectional structure taken along line IV-IV in **FIG. 1** similarly to that in **FIG. 2**. **FIG. 2** and **FIG. 10** are different from each other in that the gate signal line **4** comprises a film formed by laminating the Mo alloy on the Al alloy in **FIG. 2**, whereas it comprises a film formed by laminating an MoZr alloy on the MoW alloy in **FIG. 10**. Further, the transparent conductive film used for the pixel electrode **7** comprises ITZO (Indium-Tin-Zinc-Oxide) that can be formed stably into an amorphous film in **FIG. 2**, whereas it comprises polycrystal ITO (Indium-Tin-Oxide) in **FIG. 10**.

[0120] A film formed by laminating the MoZr alloy on the MoW alloy adopted for the gate signal line **4** is inferior to wirings using the Al alloy in view of the wiring resistance but it has an advantage of being not chemically attacked even by a strong halogenic acid such as hydrobromic acid as an etching solution of polycrystal ITO. Accordingly, polycrystal ITO that has low and stable terminal connection resistance can be adopted as the uppermost layer for the pixel electrode, the gate terminal portion **10**, the drain terminal portion **12**, and the others terminal portions **13**, **14**, **17**, and **18** formed simultaneously therewith.

[0121] (Embodiment 3)

[0122] In the embodiments described above, while the explanation has been made of the so-called vertical electric field system for the constitution of pixels, the invention is not restricted thereto and is applicable also, for example, to an in-plane-switching system.

[0123] **FIG. 11** is a plan view showing an embodiment of the constitution of pixels of a liquid crystal display device in an in-plane-switching system.

[0124] In this system, a counter electrode **30** is formed on the surface of a transparent substrate **1** formed with a pixel electrode **47** on the side of a liquid crystal and the respective electrodes are arranged alternately in a stripe-shaped pattern (extended in the direction y in the drawing).

[0125] The pixel electrode **47** and the counter electrode **30** are formed on different layers by way of an insulative film. The transmittance of the liquid crystals is controlled by an electric field which has a component substantially in parallel with the transparent substrate **1** among the electric fields generated therebetween.

[0126] Each of the pixel regions is formed at a region surrounded with each of the gate signal lines **4** extended in the direction x and arranged in parallel along the direction y and each of the drain signal lines **5** extended in the direction y and arranged in parallel along the direction x. The constitution is identical with that shown in **FIG. 1** in that the drain signal lines **5** are connected by way of the thin film transistor TFT to the pixel electrode **47** but different in that a counter voltage signal line **46** for supplying a counter voltage signal to each of the counter electrodes **30** is additionally formed.

[0127] In the case of in-plane switching system, a care has to be taken for the following point. When the cross sectional shape of the pixel electrode **47** is worsened, specifically, a tapered shape is steep, an orientation film on the sides of the electrode is not sometimes rubbed. This brings about a disadvantage that light leakage occurs at the portion upon black display to thereby bring about lowering of contrast in view of display quality. **FIG. 12** shows a pixel of the in-plane switching system, which is a result of optical microscopic observation upon black display. It can be seen that the sides of the pixel electrode **47** glistens white (indicated as LK in the drawing). **FIG. 13** is a cross sectional view of the pixel electrode **47** (a result of scanning electron microscopic observation). It can be seen that in the wirings containing a steep portion, the side of the electrode glistens white. However, in this embodiment, since the pixel electrode **47** is made of a film formed by laminating the MoZr alloy on the MoW alloy and the cross section thereof is formed in a forwardly tapered shape as described above, it can be coped with the disadvantage of the lowering of the contrast as shown in **FIG. 12**.

[0128] (Embodiment 4)

[0129] In the embodiment described previously, an example of the so-called bottom gate type is shown as the constitution of the thin film transistor TFT. This invention is not restricted thereto but also applicable also to the so-called coplanar type thin film transistor. A fourth embodiment of this invention is to be explained with reference to **FIG. 14**.

[0130] After forming an island of polycrystal silicon **34** on a substrate **33** overcoated at least with one of SiO_2 or SiN, a gate insulative film **35** comprising, for example, SiO_2 is formed.

[0131] Then, a gate electrode **36** is formed. In this embodiment, the gate electrode **36** is made of a laminated film comprising an alloy, as a lower layer, containing Mo as a main ingredient and W and an alloy, as an upper layer, containing Mo as a main ingredient and Zr. The total film thickness is about 200 nm.

[0132] The n-channel is formed by the following procedures. After forming a resist pattern by photolithography, the laminated film is side etched by about 1 μm from a resist end. The etching solution is a mixed acid of phosphoric acid, nitric acid and acetic acid also shown in Embodiment 1. Then, intense doping is applied to the polycrystal silicon **34** without removing the resist and, successively, the resist is removed and weak doping is applied. Thus, a weakly doped region can be formed in polycrystal silicon in a self-aligned manner. In usual wet etching, when side etching is applied by about 1 μm, the processed cross sectional shape forms a vertical shape. Further, it forms an inverted tapered shape in some places and a non-doped region is formed sometimes in the vicinity of the electrode. However, when a film formed by laminating the MoZr alloy on the MoW alloy is used as in this embodiment, the cross section is formed into a forward tapered shape as described above. Accordingly, the problem of forming the non-doped region can be eliminated and coverage of the film formed thereon is favorable.

[0133] As has been descried above, after forming the gate electrode, an interlayer insulative film **39** made, for example, of SiO_2 is formed. Subsequently, a through hole is formed at a portion of the region of the intensely doped polycrystal silicon **34**. Successively, the source electrode **37** and the drain electrode **38** are formed. Next, an interlayer insulative film **40** formed by laminating SiN, SiO_2 or an organic insulator, or at least two or more of them is formed. Successively, after forming a contact hole in the interlayer insulative film **40**, a pixel electrode **41** is formed to complete a thin film transistor substrate.

[0134] Although the invention has been described in several preferred embodiments, it is understood that the invention should not be restricted to them, and may be modified or improved variously within a range that those skilled in the art can recognize. The scope of the claim for patent is not restricted to the details shown and described above but include also the modifications and improvement described above. For example, it will be apparent that the thin film transistor substrate described in the foregoing embodiments is applicable not only to the liquid crystal display device but also to an organic LED (Light Emission Diode) display device.

[0135] This invention provides a liquid crystal display device having image signal lines of a bottom gate type TFT capable of satisfying respective requirements for reduced resistance, durability to dry etching, selective wet etching with respect to a gate insulative film, the number of laminated layers of two or less and tapered fabrication for a cross section. In turn, it can provide a liquid crystal display device having satisfactory characteristics.

What is claimed is

1. A liquid crystal display device comprising

a pair of substrates;

a liquid crystal layer put between the pair of substrates;

a plurality of scanning signal lines formed on one of the pair of substrates;

a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement;

thin film transistors formed in the vicinity of intersections of the scanning signal lines and the image signal lines;

pixel electrodes connected with the thin film transistors;

a gate insulative film substantially covering the scanning signal lines; and

a protection insulative film substantially covering the image signal lines and the thin film transistors,

wherein at least one of the scanning signal lines and the image signal lines is made of a two-layered film of a first conductive film as a lower layer and a second conductive film as an upper layer,

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and

the second conductive film is made of an alloy comprising molybdenum as a main ingredient and containing zirconium.

2. A liquid crystal display device as defined in claim 1, wherein

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and

the second conductive film is made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

3. A liquid crystal display device as defined in claim 1 or **2**, wherein

average conductivity defined as a product of sheet resistance and the entire film thickness of the two-layered film is 170 nΩ/m or less.

4. A liquid crystal display device as defined in any one of claims 1 to 3, wherein

a cross section formed at a fabrication end of the first conductive film forms a forwardly tapered shape.

5. A liquid crystal display device comprising;

a pair of substrates;

a liquid crystal layer put between the pair of substrates;

a plurality of scanning signal lines formed on one of the pair of substrates;

a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement;

thin film transistors formed in the vicinity of intersections of the scanning signal lines and the image signal lines;

pixel electrodes connected with the thin film transistors;

a gate insulative film substantially covering the scanning signal lines; and

a protection insulative film substantially covering the image signal lines and the thin film transistors,

wherein the image signal lines and a source and drain electrodes of the thin film transistor made of a two-layered film of a first conductive film as a lower layer and a second conductive film as an upper layer,

the first conductive film is directly connected with silicon constituting the thin film transistor,

the second conductive film is directly connected with the pixel electrode by way of a through hole disposed in the protection insulative film,

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten and

the second conductive film is made of an alloy containing zirconium.

6. A liquid crystal display device as defined in claim **5**, wherein

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and

the second conductive film is made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

7. A liquid crystal display device as defined in claim 5 or **6**, wherein

average conductivity defined as a product of sheet resistance and the entire film thickness of the two-layered film is 170 nΩ/m or less.

8. A liquid crystal display device as defined in any one of claims 5 to 7, wherein

a cross section at a fabrication end of the first conductive film forms a forwardly tapered shape.

9. A liquid crystal display device as defined in any one of claims 5 to 8, wherein

the scanning signal line is made of a laminated film of an alloy comprising aluminum as the main ingredient and an alloy comprising molybdenum as a main ingredient.

10. A liquid crystal display device as defined claim 9, wherein

the pixel electrode is made of a mixed oxide of indium oxide, tin oxide and zinc oxide.

11. A liquid crystal display device comprising;

a pair of substrates;

a liquid crystal layer put between the pair of substrates;

a plurality of scanning signal lines formed on one of the pair of substrates;

a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement;

thin film transistors formed in the vicinity of intersections of the scanning signal lines and the image signal lines;

a gate insulative film substantially covering the scanning signal lines;

a protection insulative film substantially covering the image signal lines and the thin film transistors; and

at least a pair of pixel electrodes and counter electrodes formed on one of the pair of substrates within a plurality of pixels formed in regions surrounded with the plurality of scanning signal line and the plurality of image signal lines,

wherein an image signal is supplied to the pixel electrode by way of the thin film transistor driven based on the supply of a scanning signal from the scanning signal line,

a reference voltage is supplied to the counter electrode by way of the counter voltage signal line formed over the plurality of pixels, and

the pixel electrode is made of a two-layered film of a first conductive film as a lower layer and a second conductive film as an upper layer, wherein

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and

the second conductive film is made of an alloy containing zirconium.

12. A liquid crystal display device as defined in claim 11, wherein

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and

the second conductive film is made of an alloy comprising molybdenum as a main ingredient and containing 4% by weight or more of zirconium.

13. A liquid crystal display device as defined in claim 11 or **12**, wherein

average conductivity defined as a product of sheet resistance and the entire film thickness of the two layered film is 170 nΩ/m or less.

14. A liquid crystal display device as defined in any one of claims 11 to 13, wherein

a cross section at a fabrication end of the first conductive film forms a forwardly tapered shape.

15. A liquid crystal display device comprising;

a pair of substrates;

a liquid crystal layer put between the pair of substrates;

a plurality of scanning signal lines formed on one of the pair of substrates;

a plurality of image signal lines crossing the scanning signal lines in a matrix arrangement;

thin film transistors formed in the vicinity of intersections of the scanning signal lines and the image signal lines;

pixel electrodes connected with the thin film transistors;

a gate insulative film substantially covering polycrystal silicon of the thin film transistors;

an interlayer insulative film for substantially covering the scanning signal lines and insulating the scanning signal lines from the image signal lines; and

a protection insulative film substantially covering the image signal lines,

wherein a gate electrode of the thin film transistor is formed of a two-layered film of a first conductive layer as a lower layer and a second conductive layer as an upper layer,

the first conductive film is made of an alloy comprising molybdenum as a main ingredient and containing tungsten, and

the second conductive film is made of an alloy containing zirconium.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US20030063229A1	公开(公告)日	2003-04-03
申请号	US10/101166	申请日	2002-03-20
[标]申请(专利权)人(译)	高桥TAKUYA 金子俊 田村克己 ONISAWA KENICHI		
申请(专利权)人(译)	高桥TAKUYA 金子俊 田村克己 ONISAWA KENICHI		
当前申请(专利权)人(译)	高桥TAKUYA 金子俊 田村克己 ONISAWA KENICHI		
[标]发明人	TAKAHASHI TAKUYA KANEKO TOSHIKI TAMURA KATSUMI ONISAWA KENICHI		
发明人	TAKAHASHI, TAKUYA KANEKO, TOSHIKI TAMURA, KATSUMI ONISAWA, KENICHI		
IPC分类号	G02F1/1368 G02F1/1343 G02F1/1362 G09F9/00 G09F9/30 G09F9/35 H01L29/786 G02F1/136		
CPC分类号	G02F1/134363 G02F2001/13629 G02F1/136286		
优先权	2001298993 2001-09-28 JP		
其他公开文献	US6731364		
外部链接	Espacenet USPTO		

摘要(译)

一种液晶显示装置，具有底栅型TFT的图像信号线，其中图像信号线包括作为下层的第一导电膜和作为上层的第二导电膜的层压膜，第一导电膜由包含Mo作为主要成分的合金和W，第二导电膜由包含Mo作为主要成分的合金和Zr制成。该器件能够满足降低电阻，改善抗干蚀刻性，相对于栅极绝缘膜的选择性湿法蚀刻，两个或更少的叠层数量以及横截面的锥形制造的要求。