



US 20090207118A1

(19) **United States**(12) **Patent Application Publication****Lee et al.**(10) **Pub. No.: US 2009/0207118 A1**(43) **Pub. Date: Aug. 20, 2009**(54) **DATA DRIVING UNIT AND LIQUID CRYSTAL DISPLAY**

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(21) Appl. No.: **12/372,283**

(22) Filed: **Feb. 17, 2009**

(30) **Foreign Application Priority Data**

Feb. 15, 2008 (KR) 10-2008-0013858

Publication Classification

(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.** **345/98**

(57) **ABSTRACT**

A data driving unit and a liquid crystal display (LCD) are provided. The data driving unit includes a first buffer, a second buffer, a charge sharing switch connected between an output terminal of the first buffer and an output terminal of the second buffer, and a controller configured to compare a previous line-time data pattern with a current line-time data pattern and generate a control signal for controlling a switching operation of the charge sharing switch according to a comparison result.

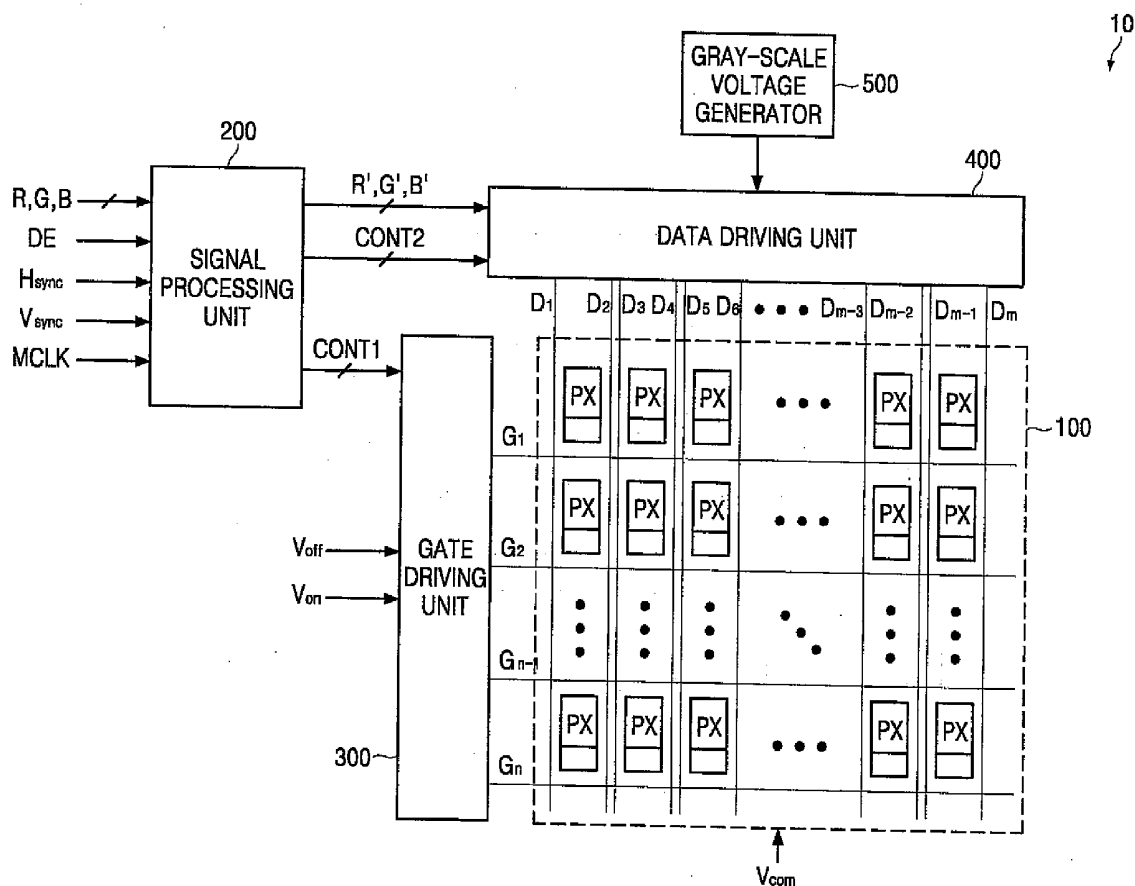


FIG. 1

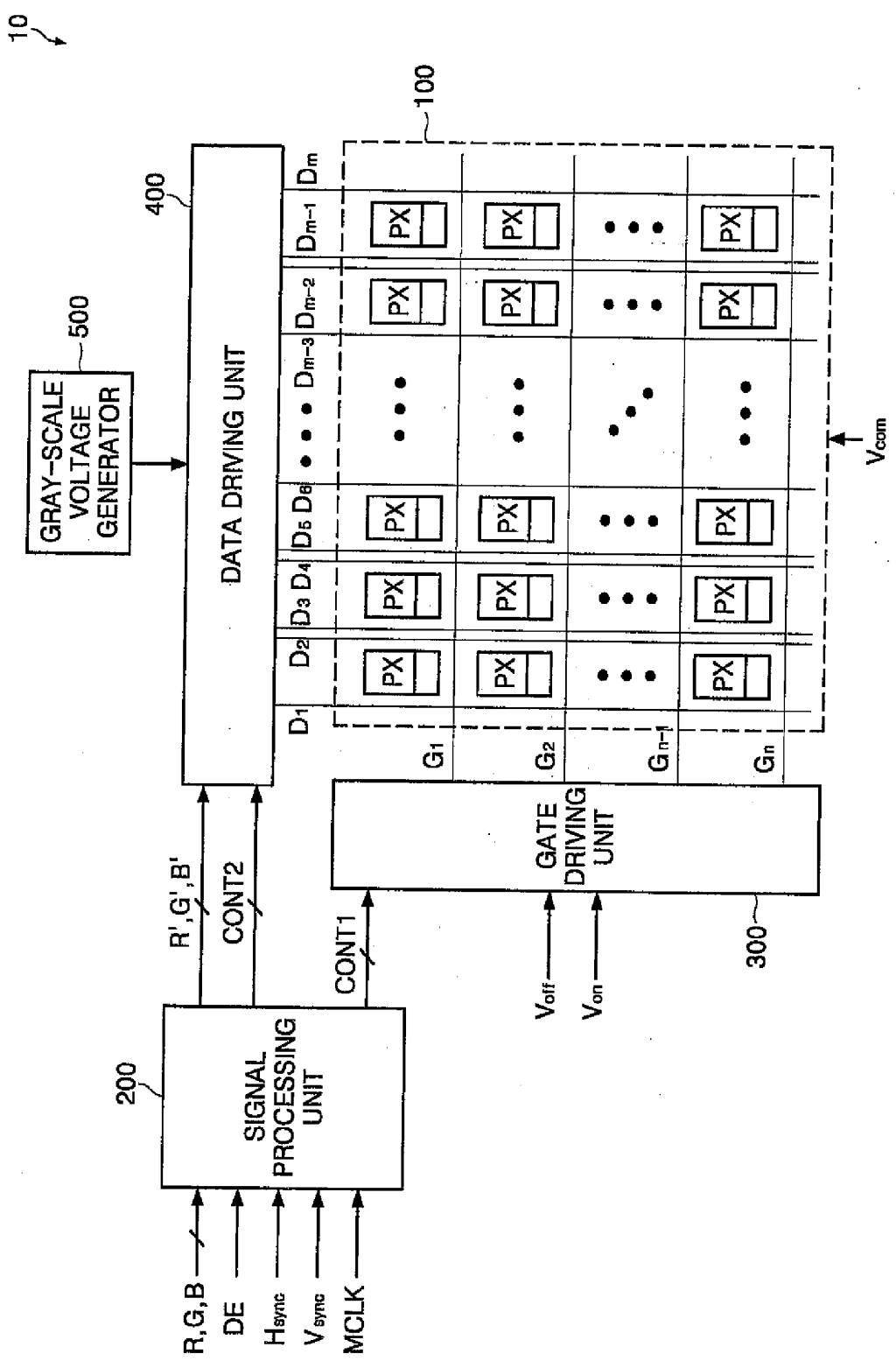


FIG. 3

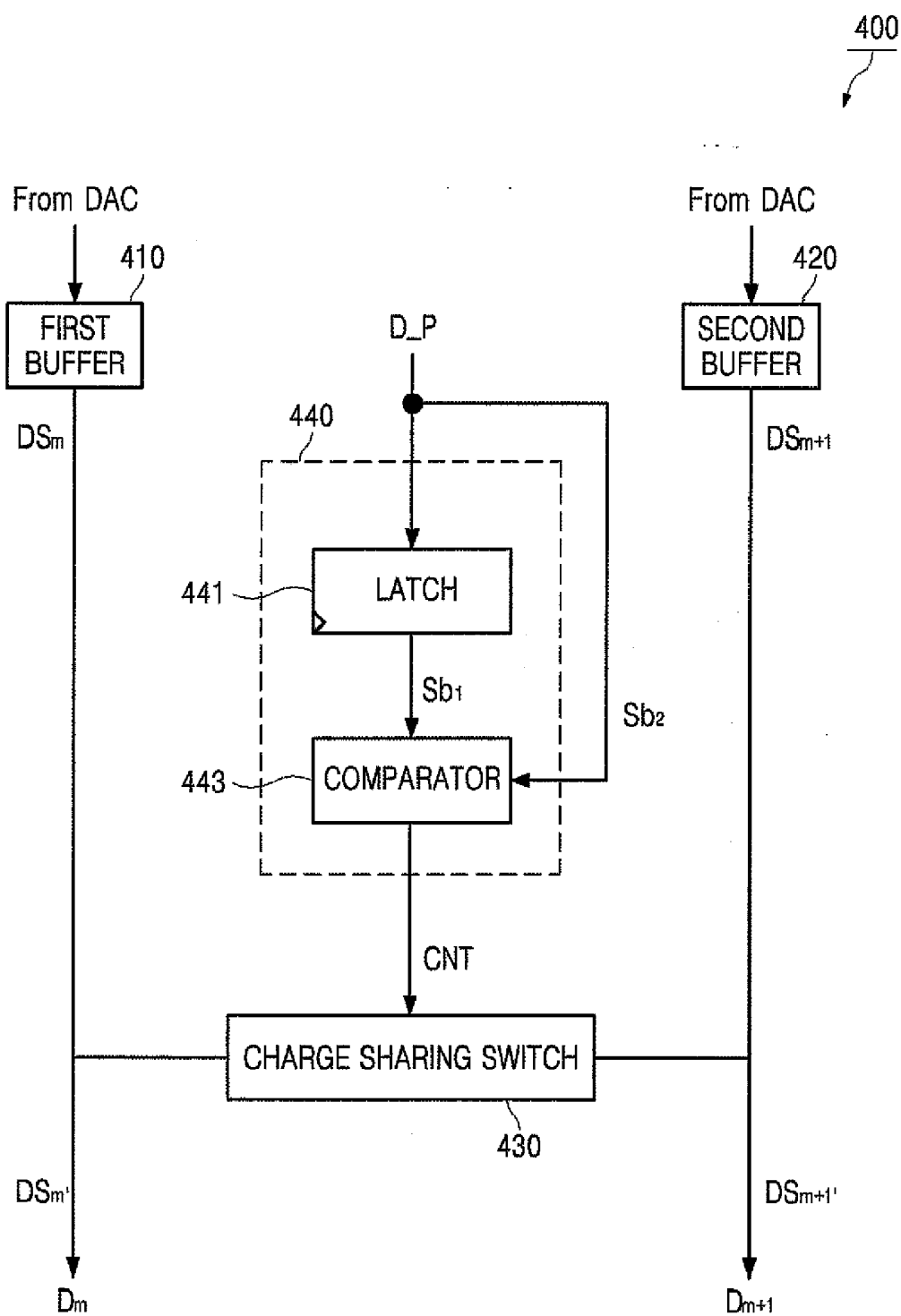
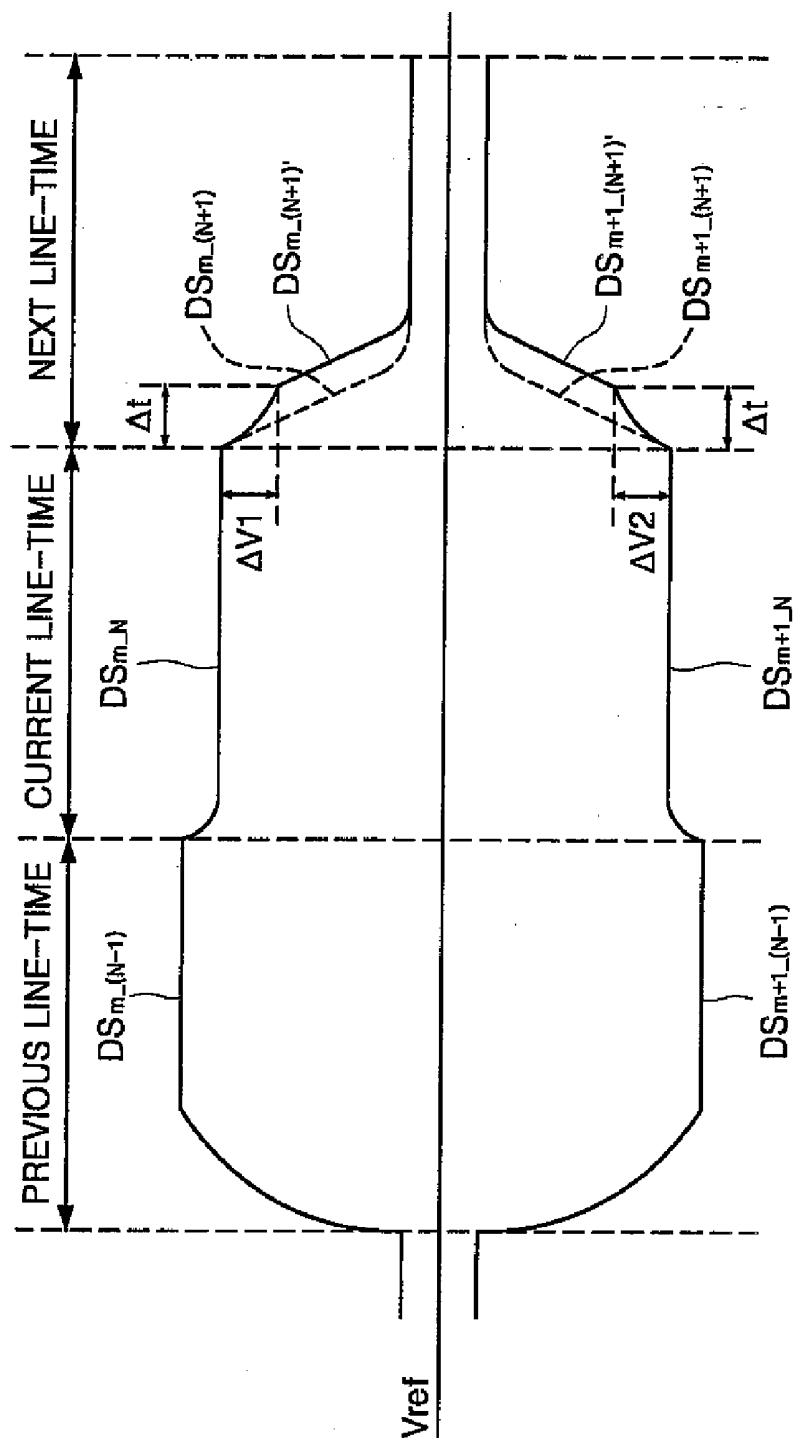


FIG. 4



DATA DRIVING UNIT AND LIQUID CRYSTAL DISPLAY

BACKGROUND

[0001] The invention relates generally to a data driving unit and a liquid crystal display (LCD) including same. More particularly, the invention relates to a data driving unit having reduced heat generation properties and an LCD including same.

[0002] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2008-0013858, filed on Feb. 15, 2008, the subject matter of which is hereby incorporated by reference.

[0003] Recently, large-size displays, for example, liquid crystal displays (LCDs) have been developed. Large-size LCDs are characterized by high resolution and high picture quality. For instance, conventional high definition (HD) LCDs provide 1366×768 wide XGA (WXGA) resolution and conventional full-HD LCDs provide 1920×1080 widescreen ultra XGA (WUXGA) resolution. As the resolution of LCDs increases, the use of 10 or more digital data bits to represent color gradations is required. Therefore, a data driving unit, (i.e., a source driver supplying a driving current to the liquid crystal panel of a LCD) must support multiple channels and a very fast interface.

[0004] In addition, the general increase in liquid panel size requires a commensurate increase in the driving current supplied from the data driving unit to the liquid crystal panel. In turn, this increase in driving current requires an increase in driving power in the data driving unit. However, this increase in driving power also results in the generation of greater heat by the data driving unit. This increased heat generation by the data driving unit has adverse consequences on the long term reliability of the unit, and malfunction of the data driving unit leads to failure of the constituent LCD.

SUMMARY

[0005] Certain embodiments of the invention provide a data driving unit capable of operating with reduced heat generation and a liquid crystal display (LCD) including same.

[0006] According to one embodiment, the invention provides a data driving unit including; a first buffer and a second buffer, a charge sharing switch connected between an output terminal of the first buffer and an output terminal of the second buffer, and a controller configured to compare a previous line-time data pattern with a current line-time data pattern and generate a control signal controlling a switching operation of the charge sharing switch according to a comparison result.

[0007] In another embodiment, the invention provides a liquid crystal display including; a data driving unit comprising a first buffer, a second buffer, a charge sharing switch connected between an output terminal of the first buffer and an output terminal of the second buffer, and a controller configured to compare a previous line-time data pattern with a current line-time data pattern and generate a control signal for controlling a switching operation of the charge sharing switch according to a comparison result, a gate driving unit configured to output a gate on/off voltage, and a liquid crystal panel configured to display an image, wherein the liquid crystal panel comprising a plurality of gate lines each configured to receive the gate on/off voltage, a plurality of data lines respectively connected with the output terminal of the first

buffer and the output terminal of the second buffer, and a plurality of pixels each connected with one of the gate lines and one of the data lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The above and other features and advantages of the present invention will become more apparent upon a review of certain exemplary embodiments with reference to the attached drawings in which:

[0009] FIG. 1 is a block diagram of a liquid crystal display (LCD) according to some embodiments of the present invention;

[0010] FIG. 2 is a equivalent circuit diagram of a single pixel in the LCD illustrated in FIG. 1;

[0011] FIG. 3 is a block diagram of a data driving unit illustrated in FIG. 2; and

[0012] FIG. 4 is a waveform diagram of signals of the data driving unit illustrated in FIG. 3.

DESCRIPTION OF EMBODIMENTS

[0013] The present invention now will be described in some additional detail with reference to the accompanying drawings. The invention may, however, be embodied in many different forms and should not be construed as being limited to only the illustrated embodiments. Rather, the embodiments are provided as teaching examples. In the drawings, the size and relative sizes of various components and elements may be exaggerated for clarity. Throughout the written description and drawings, like reference indicators refer to like or similar elements.

[0014] It will be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items and may be abbreviated as “/”.

[0015] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first signal could be termed a second signal, and, similarly, a second signal could be termed a first signal without departing from the teachings of the disclosure.

[0016] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” and/or “comprising,” or “includes” and/or “including” when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0017] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictio-

naries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present application, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0018] FIG. 1 is a partial block diagram of a liquid crystal display (LCD) 10 according to an embodiment of the invention. FIG. 2 is an equivalent circuit diagram for a single pixel in the LCD 10 illustrated in FIG. 1.

[0019] Referring to FIG. 1, the LCD 10 generally includes a liquid crystal panel 100, a signal processing unit 200, a gate driving unit 300, a data driving unit 400, and a gray-scale voltage generator 500. The liquid crystal panel 100 includes a plurality of pixels PX, a plurality of gate lines G_1 through G_n , and a plurality of data lines D_1 through D_m where “n” and “m” are natural numbers.

[0020] The gate signal, e.g., a gate on/off voltage V_{on} or V_{off} from the gate driving unit 300 is applied to each of the gate lines G_1 through G_n . The data signal from the data driving unit 400 is applied to each of the data lines D_1 through D_m . The gate lines G_1 through G_n extend roughly in parallel with one another in a row direction and the data lines D_1 through D_m extend roughly in parallel with one another in a column direction. Two of the data lines D_1 through D_m are provided for each pixel PX.

[0021] Referring to FIG. 2, each pixel PX in the liquid crystal panel 100 includes a first subpixel 130 and a second subpixel 140. The first subpixel 130 and the second subpixel 140 are formed between a first substrate 110 having a first pixel electrode 131 and a second pixel electrode 141 and a second substrate 120 having a common electrode CE and a color filter CF.

[0022] In the first substrate 110 are formed a gate line G_n extending in the row direction and two data lines D_m and D_{m+1} extending in the column direction. The gate line G_n and the two data lines D_m and D_{m+1} are electrically connected with the first subpixel 130 and the second subpixel 140. A first data signal and a second data signal, which are different from each other, are applied to the first subpixel 130 and the second subpixel 140, respectively. The second data signal may have an opposite phase to the first data signal or may be lower than the first data signal.

[0023] The first subpixel 130 includes a first capacitor C_1 which charges the first data signal and a first switch Q_1 which provides the first data signal to the first capacitor C_1 in response to a gate on voltage provided from the gate line G_n . The second subpixel 140 includes a second capacitor C_2 which charges the second data signal and a second switch Q_2 which provides the second data signal to the second capacitor C_2 in response to the gate on voltage provided from the gate line G_n .

[0024] When the first data signal is applied to the first subpixel 130, light provided from a backlight assembly (not shown) is transmitted at a first transmittance corresponding to the first data signal. When the second data signal lower than the first data signal is applied to the second subpixel 140, light provided from the backlight assembly is transmitted at a second transmittance corresponding to the second data signal. Accordingly, an image displayed on the pixel PX has brightness corresponding to an in-between of the first transmittance and the second transmittance. The first pixel electrode 131 and the second pixel electrode 141 are not restricted to the shapes illustrated in FIG. 2 but may be formed in various shapes.

[0025] Referring back to FIG. 1, the signal processing unit 200 such as a timing controller receives a plurality of input control signals from an external graphics controller (not shown) and generates a gate control signal CONT1 and a data control signal CONT2 based on the input control signals. The signal processing unit 200 outputs the gate control signal CONT1 to the gate driving unit 300 and the data control signal CONT2 to the data driving unit 400. The input control signals transmitted from the graphics controller to the signal processing unit 200 may include a vertical sync signal V_{sync} , a horizontal sync signal H_{sync} , a main clock signal MCLK, and a data enable signal DE.

[0026] The gate control signal CONT1 transmitted from the signal processing unit 200 to the gate driving unit 300 is for controlling the operation of the gate driving unit 300. For instance, the gate control signal CONT1 may include a vertical start signal for starting the operation of the gate driving unit 300, a gate clock signal for determining when to output the gate on voltage V_{on} , and an output enable signal for determining a pulse width of the gate on voltage V_{on} .

[0027] The data control signal CONT2 transmitted from the signal processing unit 200 to the data driving unit 400 is for controlling the operation of the data driving unit 400. For instance, the data control signal CONT2 may include a horizontal start signal for starting the operation of the data driving unit 400 and an output instruction signal for instructing output of two data voltages.

[0028] The signal processing unit 200 receives video signals R, G, and B from the graphics controller, processes them to be suitable to the operating conditions of the liquid crystal panel 100, outputs video data signals R', G', and B' to the data driving unit 400. The gate driving unit 300 outputs the gate on/off voltage V_{on} or V_{off} input from outside to the gate lines G_1 through G_n sequentially in response to the gate control signal CONT1 provided from the signal processing unit 200.

[0029] The data driving unit 400 sequentially receives the video data signals R', G', and B' in response to the data control signal CONT2 provided from the signal processing unit 200. Also, the data driving unit 400 selects gray-scale voltages corresponding to the video data signals R', G', and B' from among a plurality of gray-scale voltages provided from the gray-scale voltage generator 500 and provides the selected gray-scale voltages to the data line D_m in the first subpixel 130 (FIG. 2) and the data line D_{m+1} in the second subpixel 140 as the first data signal and the second data signal, respectively.

[0030] In addition, in order to prevent the amount of heat generation from increasing due to increase in driving power when the size of the liquid crystal panel 100 increases, the data driving unit 400 may include a charge sharing switch that performs charge sharing. For example, “charge sharing” may include control steps to pre-charge or pre-discharge the first data signal and/or the second data signal. A constituent controller may be used to control charge sharing by means of a (e.g.,) a selectively operated switch. An exemplary charge sharing switch and corresponding controller will be described in some additional detail with reference to FIGS. 3 and 4.

[0031] The gray-scale voltage generator 500 includes a plurality of resistors (not shown) connected in series between a node (not shown) to which a driving voltage is applied and a ground (not shown) to divide the voltage level of the driving voltage and generate a plurality of gray-scale voltages. The gray-scale voltage generator 500 is not restricted to the above-described internal structure but may be implemented in various forms.

[0032] Hereinafter, the data driving unit 400 according to certain embodiments of the invention will be described in some additional detail with reference to FIGS. 3 and 4. FIG. 3 is a block diagram of an exemplary data driving unit 400 capable of use within the context of FIG. 2. FIG. 4 is a corresponding waveform diagram illustrating signals associated with the data driving unit 400 of FIG. 3.

[0033] Referring to FIG. 3, the data driving unit 400 includes a pair of output units, i.e., a first buffer 410 and a second buffer 420, a charge sharing switch 430, and a controller 440. The pair of output units may be implemented by a plurality of buffers, as illustrated in FIG. 3, or may be implemented by an amplifier.

[0034] The first buffer 410 outputs a signal provided from outside, for example, a digital-to-analog converter (DAC) (not shown), to the data line D_m illustrated in FIG. 2 as an output signal DS_m of the first buffer 410, for example, the first data signal. The second buffer 420 outputs a signal provided from the DAC to the data line D_{m+1} as an output signal DS_{m+1} of the second buffer 420, for example, the second data signal. Each of the signals respectively provided from the DAC to the first buffer 410 and the second buffer 420 may be a signal obtained by converting a digital signal, e.g., a data pattern D_P , transmitted from the signal processing unit 200 (FIG. 1) to the DAC included in the data driving unit 400, into an analog signal corresponding to a gray-scale voltage. The data pattern D_P may be N-bit data, where N is a natural number, (e.g., $N=10$).

[0035] The charge sharing switch 430 may be connected between an output terminal of the first buffer 410 and an output terminal of the second buffer 420. The charge sharing switch 430 performs a switching operation in response to a control signal CNT provided from outside, for example, the controller 440. When the charge sharing switch 430 performs the switching operation, the first data signal DS_m and the second data signal DS_{m+1} are subjected to charge sharing, for example, they may be pre-charged or pre-discharged to a predetermined level. The charge sharing switch 430 may be implemented by a P-channel metal-oxide-semiconductor field effect transistor (PMOSFET) or N-channel metal-oxide-semiconductor field effect transistor (NMOSFET) switching element.

[0036] The controller 440 may include a latch 441 and a comparator 443. The latch 441 may receive and store at least one upper bit including a most significant bit (MSB) of a data pattern D_P provided from outside. For instance, the latch 441 may receive a data pattern D_P corresponding to the first data signal DS_m input to the first buffer 410 and store at least one upper bit, for example, two upper bits Sb1 including the MSB of the data pattern D_P . In addition, the latch 441 may receive a data pattern D_P corresponding to the second data signal DS_{m+1} input to the second buffer 420 and store at least one upper bit, for example, two upper bits Sb1 including the MSB of the data pattern D_P . Here, the latch 441 may receive the data pattern D_P corresponding to the first data signal DS_m or the data pattern D_P corresponding to the second data signal DS_{m+1} and store at least one upper bit Sb1 of the received data pattern D_P . The latch 441 may be implemented by a flip-flop, for example, a D flip-flop.

[0037] The comparator 443 compares the at least one upper bit Sb1 of the data pattern D_P stored in the latch 441 with at least one upper bit Sb2 of another data pattern D_P provided from outside and outputs the control signal CNT according to a comparison result. The control signal CNT may be output at

a different level, (e.g., a logically "high" level or a logically "low" level). The control signal CNT may control the switching operation, (e.g., turn-ON or turn-OFF, of the charge sharing switch 430).

[0038] When the comparator 443 outputs a high control signal CNT according to the comparison result, the charge sharing switch 430 may be turned ON in response to the high control signal CNT. Then, the charge sharing switch 430 may connect the output terminal of the first buffer 410 with the output terminal of the second buffer 420 and pre-discharge or pre-charge the output signal DS_m of the first buffer 410 and the output signal DS_{m+1} of the second buffer 420, e.g., the first data signal DS_m and the second data signal DS_{m+1} corresponding to data patterns D_P input to the latch 441. Accordingly, the first buffer 410 and the second buffer 420 may output a pre-discharged or pre-charged first data signal DS_m and a pre-discharged or pre-charged second data signal DS_{m+1} , respectively.

[0039] In other words, the first buffer 410 and the second buffer 420 are driven the moment the first data signal DS_m and the second data signal DS_{m+1} have been pre-discharged or pre-charged by the charge sharing switch 430, and therefore, driving power for the first buffer 410 and the second buffer 420 can be reduced. As a result, the amount of heat generated by the data driving unit 400 may be reduced. The comparator 443 may be implemented using a logic gate, (e.g., a NAND gate or a NOR gate).

[0040] Hereinafter, the operation of the data driving unit 400 will be described in some additional detail with reference to FIGS. 1 through 4. Firstly, the operation of the data driving unit 400 during a previous line-time of the LCD 10, for example, an (N-1) line-time (where N denotes a current line-time of the LCD 10) while a plurality of switches Q_1 and Q_2 connected with the first gate line G_1 are turned on when the gate on voltage V_{on} is applied from the gate driving unit 300 to the first gate line G_1 of the liquid crystal panel 100, will be described.

[0041] During the previous line-time of the LCD 100, the first buffer 410 of the data driving unit 400 outputs an (N-1) line-time first output signal $DS_{m_ (N-1)}$ to the first subpixel 130 connected with the first gate line G_1 and the first data line D_1 and the second buffer 420 of the data driving unit 400 outputs an (N-1) line-time second output signal $DS_{m+1_ (N-1)}$ to the second subpixel 140 connected with the first gate line G_1 and the second data line D_2 . At this time, the (N-1) line-time first output signal $DS_{m_ (N-1)}$ and the (N-1) line-time second output signal $DS_{m+1_ (N-1)}$ may have opposite phases to each other with respect to a reference voltage signal Vref.

[0042] Meanwhile, the latch 441 of the controller 440 in the data driving unit 400 receives a data pattern D_P corresponding to the (N-1) line-time first output signal $DS_{m_ (N-1)}$ output from the first buffer 410 or a data pattern D_P corresponding to the (N-1) line-time second output signal $DS_{m+1_ (N-1)}$ output from the second buffer 420. The latch 441 stores upper bits of the received data pattern D_P , for example, two upper bits Sb1 including the MSB of the data pattern D_P . In the illustrated embodiments of the invention, it is assumed that the latch 441 receives the data pattern D_P corresponding to the (N-1) line-time first output signal $DS_{m_ (N-1)}$ output from the first buffer 410 and stores the two upper bits Sb1 including the MSB of the data pattern D_P .

[0043] Secondly, the operation of the data driving unit 400 during a current line-time of the LCD 10, for example, an N line-time while a plurality of switches Q_1 and Q_2 connected

with the second gate line G_2 are turned on when the gate on voltage V_{on} is applied from the gate driving unit **300** to the second gate line G_2 of the liquid crystal panel **100**, will be described. During the current line-time of the LCD **10**, the first buffer **410** of the data driving unit **400** outputs an N line-time first output signal DS_{m_N} to the first subpixel **130** connected with the second gate line G_2 and the first data line D_1 and the second buffer **420** of the data driving unit **400** outputs a N line-time second output signal DS_{m+1_N} to the second subpixel **140** connected with the second gate line G_2 and the second data line D_2 . As described above, the N line-time first output signal DS_{m_N} and the N line-time second output signal DS_{m+1_N} may have opposite phases with respect to the reference voltage signal V_{ref} .

[0044] Meanwhile, the latch **441** of the controller **440** in the data driving unit **400** outputs to the comparator **443** the two upper bits Sb1 including the MSB of the stored data pattern D_P , i.e., the data pattern D_P corresponding to the (N-1) line-time first output signal DS_{m_N} output from the first buffer **410** during the (N-1) line-time of the LCD **10**, in response to a predetermined clock signal provided from outside. The latch **441** also receives a data pattern D_P corresponding to the N line-time first output signal DS_{m_N} output from the first buffer **410** and stores upper bits of the received data pattern D_P , for example, two upper bits including the MSB of the data pattern D_P .

[0045] The comparator **443** compares the two upper bits Sb1 including the MSB of the data pattern D_P corresponding to the (N-1) line-time first output signal DS_{m_N} received from the first buffer **410** during the (N-1) line-time of the LCD **10** with two upper bits Sb2 including the MSB of the data pattern D_P corresponding to the N line-time first output signal DS_{m_N} or the MSB of a data pattern D_P corresponding to the N line-time second output signal DS_{m+1_N} . In the illustrated embodiments of the invention, the comparator **443** compares the two upper bits Sb1 including the MSB of the data pattern D_P corresponding to the (N-1) line-time first output signal DS_{m_N} with the two upper bits Sb2 including the MSB of the data pattern D_P corresponding to the N line-time first output signal DS_{m_N} .

[0046] Thereafter, the comparator **443** outputs the control signal CNT according to a comparison result. For instance, when the two upper bits Sb1 of the data pattern D_P provided from the latch **441** to the comparator **443** are "11" and the two upper bits Sb2 of the data pattern D_P corresponding to the N line-time first output signal DS_{m_N} are slightly less than the two upper bits Sb1 provided from the latch **441**, for example, "10", the comparator **443** may output a low control signal CNT since the MSB of the (N-1) line-time data pattern D_P is substantially the same as that of the N line-time data pattern D_P .

[0047] In response to the low control signal CNT output from the comparator **443**, the charge sharing switch **430** is turned OFF and does not perform charge sharing, for example, pre-charge or pre-discharge, with respect to the output signal DS_{m_N} of the first buffer **410** and the output signal DS_{m+1_N} of the second buffer **420** during the N line-time of the LCD **10**. Accordingly, during the N line-time, the data driving unit **400** provides the N line-time first output signal DS_{m_N} and the N line-time second output signal DS_{m+1_N} as data signals to the first subpixel **130** connected with the second gate line G_2 and the first data line D_1 and the second subpixel **140** connected with the second gate line G_2 and the second data line D_2 , respectively.

[0048] Thirdly, the operation of the data driving unit **400** during a next line-time of the LCD **10**, for example, an (N+1) line-time while a plurality of switches Q_1 and Q_2 connected with the third gate line G_3 are turned on when the gate on voltage V_{on} is applied from the gate driving unit **300** to the third gate line G_3 of the liquid crystal panel **100**, will be described. During the next line-time of the LCD **10**, the first buffer **410** of the data driving unit **400** outputs an (N+1) line-time first output signal DS_{m_N+1} to the first subpixel **130** connected with the third gate line G_3 and the first data line D_1 and the second buffer **420** of the data driving unit **400** outputs a (N+1) line-time second output signal DS_{m+1_N+1} to the second subpixel **140** connected with the third gate line G_3 and the second data line D_2 .

[0049] Meanwhile, the latch **441** of the controller **440** in the data driving unit **400** outputs to the comparator **443** two upper bits Sb1 including the MSB of the stored data pattern D_P , i.e., the data pattern D_P corresponding to the N line-time first output signal DS_{m_N} output from the first buffer **410** during the N line-time of the LCD **10**, in response to a predetermined clock signal provided from outside. The latch **441** also receives a data pattern D_P corresponding to the (N+1) line-time first output signal DS_{m_N+1} output from the first buffer **410** and stores upper bits of the received data pattern D_P , for example, two upper bits including the MSB of the data pattern D_P , in response to the predetermined clock.

[0050] The comparator **443** compares the two upper bits Sb1 including the MSB of the data pattern D_P corresponding to the N line-time first output signal DS_{m_N} received from the latch **441** with two upper bits Sb2 including the MSB of the data pattern D_P corresponding to the (N+1) line-time first output signal DS_{m_N+1} . Thereafter, the comparator **443** outputs the control signal CNT according to a comparison result. For instance, when the two upper bits Sb1 of the data pattern D_P provided from the latch **441** to the comparator **443** are at the high level, for example, "10", and the two upper bits Sb2 of the data pattern D_P corresponding to the (N+1) line-time first output signal DS_{m_N+1} are low, for example, "00", the comparator **443** may output a high control signal CNT since the MSB of the N line-time data pattern D_P is different from that of the (N+1) line-time data pattern D_P .

[0051] In other words, the comparator **443** outputs the high control signal CNT to control the operation of the charge sharing switch **430** when the data pattern D_P corresponding to the (N+1) line-time first output signal DS_{m_N+1} is greatly lower than the data pattern D_P provided from the latch **441**. This means that heat generated in the data driving unit **400** may be generated mostly from the first buffer **410** or the second buffer **420**. By the way, the output signal of the first buffer **410** and the output signal of the second buffer **420** may have opposite phases to each other with respect to the reference voltage signal V_{ref} .

[0052] At this time, when the output signal DS_{m_N+1} of the first buffer **410** during the (N+1) line-time is lower than the output signal DS_{m_N} of the first buffer **410** during the N line-time, most of heat is generated from the first buffer **410** and the second buffer **420**. Accordingly, the comparator **443** may compare the data pattern D_P corresponding to the (N+1) line-time first output signal DS_{m_N+1} with the data pattern D_P corresponding to the N line-time first output signal DS_{m_N} and output the high control signal CNT when the data pattern D_P decreases so as to control the operation of the charge sharing switch **430**.

[0053] In response to the high control signal CNT output from the comparator **443**, the charge sharing switch **430** is turned ON and performs charge sharing with respect to the output signal $DS_{m_{(N+1)}}$ of the first buffer **410** and the output signal $DS_{m+1_{(N+1)}}$ of the second buffer **420** during the (N+1) line-time of the LCD **10**. In some additional detail, the charge sharing switch **430** is turned ON in response to the high control signal CNT and pre-discharges the (N+1) line-time first output signal $DS_{m_{(N+1)}}$ of the first buffer **410** for a predetermined period of time Δt to decrease it by a first level $\Delta V1$ during the (N+1) line-time. In addition, the charge sharing switch **430** turned ON in response to the high control signal CNT pre-charges the (N+1) line-time second output signal $DS_{m+1_{(N+1)}}$ of the second buffer **420** for the predetermined period of time Δt to increase it by a second level $\Delta V2$ during the (N+1) line-time.

[0054] Accordingly, during the (N+1) line-time, the data driving unit **400** outputs as a data signal a first output signal $DS_{m_{(N+1)}}$ resulting from pre-discharging the output signal $DS_{m_{(N+1)}}$ of the first buffer **410** by the first level $\Delta V1$ to the first subpixel **130** connected with the third gate line G_3 and the first data line D_1 in the liquid crystal panel **100** and outputs as another data signal a second output signal $DS_{m+1_{(N+1)}}$ resulting from pre-charging the output signal $DS_{m+1_{(N+1)}}$ of the second buffer **420** by the second level $\Delta V2$ to the second subpixel **140** connected with the third gate line G_3 and the second data line D_2 in the liquid crystal panel **100**.

[0055] In other words, the first buffer **410** of the data driving unit **400** is driven from the moment it has been pre-discharged by the first level $\Delta V1$ by the charge sharing switch **430** and outputs the first output signal $DS_{m_{(N+1)}}$, and the second buffer **420** of the data driving unit **400** is driven from the moment it has been pre-charged by the second level $\Delta V2$ by the charge sharing switch **430** and outputs the second output signal $DS_{m+1_{(N+1)}}$, so that the driving power for the first buffer **410** and the second buffer **420** is decreased. As a result, the amount of heat generated in the data driving unit **400** is also decreased.

[0056] As described above, a data driving unit according to embodiments of the invention compares the patterns of data signals provided to adjacent pixels, for example, a plurality of pixels respectively connected with adjacent gate lines, during different line-times in an LCD and selectively performs charge sharing with respect to the data signals, thereby decreasing driving power and reducing the amount of heat generated.

[0057] According to embodiments of the invention, data signals are selectively pre-charged or pre-discharged in a data driving unit, so that the driving power and the amount of heat generation in the data driving unit are decreased. As a result, the likelihood of LCD malfunction may be reduced.

[0058] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in forms and details may be made therein without departing from the scope of the present invention as defined by the following claims.

What is claimed is:

1. A data driving unit comprising:

a first buffer and a second buffer;

a charge sharing switch connected between an output terminal of the first buffer and an output terminal of the second buffer; and

a controller configured to compare a previous line-time data pattern with a current line-time data pattern and generate a control signal controlling a switching operation of the charge sharing switch according to a comparison result.

2. The data driving unit of claim 1, wherein the charge sharing switch pre-charges or pre-discharges an output signal of the first buffer corresponding to the current line-time data pattern and an output signal of the second buffer in response to the control signal.

3. The data driving unit of claim 1, wherein the controller comprises:

a latch configured to store at least one upper bit of the previous line-time data pattern; and

a comparator configured to compare at least one upper bit of the current line-time data pattern with the at least one upper bit of the previous line-time data pattern stored in the latch and output the control signal according to a comparison result.

4. The data driving unit of claim 3, wherein, when the at least one upper bit of the previous line-time data pattern is different from the at least one upper bit of the current line-time data pattern, the comparator outputs the control signal at a first level and the charge sharing switch connects the output terminal of the first buffer with the output terminal of the second buffer in response to the first-level control signal.

5. The data driving unit of claim 1, wherein the charge sharing switch is a P-channel metal-oxide semiconductor (PMOS) or an N-channel metal-oxide semiconductor (NMOS).

6. A liquid crystal display comprising:

a data driving unit comprising a first buffer, a second buffer, a charge sharing switch connected between an output terminal of the first buffer and an output terminal of the second buffer, and a controller configured to compare a previous line-time data pattern with a current line-time data pattern and generate a control signal for controlling a switching operation of the charge sharing switch according to a comparison result;

a gate driving unit configured to output a gate on/off voltage; and

a liquid crystal panel configured to display an image, wherein the liquid crystal panel comprising a plurality of gate lines each configured to receive the gate on/off voltage, a plurality of data lines respectively connected with the output terminal of the first buffer and the output terminal of the second buffer, and a plurality of pixels each connected with one of the gate lines and one of the data lines.

7. The liquid crystal display of claim 6, wherein the charge sharing switch pre-charges or pre-discharges an output signal of the first buffer corresponding to the current line-time data pattern and an output signal of the second buffer in response to the control signal.

8. The liquid crystal display of claim 6, wherein the controller comprises:

a latch configured to store at least one upper bit of the previous line-time data pattern; and

a comparator configured to compare at least one upper bit of the current line-time data pattern with the at least one upper bit of the previous line-time data pattern stored in the latch and output the control signal according to a comparison result.

9. The liquid crystal display of claim 8, wherein, when the at least one upper bit of the previous line-time data pattern is different from the at least one upper bit of the current line-time data pattern, the comparator outputs the control signal at a first level and the charge sharing switch connects the output terminal of the first buffer with the output terminal of the second buffer in response to the first-level control signal.

10. The liquid crystal display of claim 6, wherein the charge sharing switch is a P-channel metal-oxide semiconductor (PMOS) or an N-channel metal-oxide semiconductor (NMOS).

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专利名称(译)	数据驱动单元和液晶显示器		
公开(公告)号	US20090207118A1	公开(公告)日	2009-08-20
申请号	US12/372283	申请日	2009-02-17
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IPC分类号	G09G3/36		
CPC分类号	G09G2330/021 G09G3/3688		
优先权	1020080013858 2008-02-15 KR		
外部链接	Espacenet USPTO		

摘要(译)

提供数据驱动单元和液晶显示器 (LCD)。数据驱动单元包括第一缓冲器，第二缓冲器，连接在第一缓冲器的输出端和第二缓冲器的输出端之间的电荷共享开关，以及配置成将先前的线时间数据模式与当前线路时间数据模式并根据比较结果产生用于控制电荷共享开关的切换操作的控制信号。

