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(19) **United States**(12) **Patent Application Publication**
Nakazaki(10) **Pub. No.: US 2007/0001949 A1**(43) **Pub. Date: Jan. 4, 2007**(54) **PROTECTIVE CIRCUIT FOR A THIN FILM
TRANSISTOR AND A LIQUID CRYSTAL
DISPLAY DEVICE****Publication Classification**(51) **Int. Cl.**
G09G 3/36 (2006.01)(52) **U.S. Cl.** **345/87**(76) **Inventor: Yoshiaki Nakazaki, Yokohama-shi (JP)**

Correspondence Address:

GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901 (US)(57) **ABSTRACT**

An input-output (I/O) protective circuit having more stable I/O protective function for use in the liquid crystal display device and including in one embodiment a resistance provided between an I/O terminal pad and an I/O primary stage thin film transistor, a wiring connecting the I/O terminal pad with the resistance, and two I/O protective thin film transistors connected in series between a ground terminal and a power source terminal. The above wiring is connected with each joint portion of the two I/O protective thin film transistors and, each of the two I/O protective thin film transistors has p-type substrate potential fixing terminals and n-type substrate potential fixing terminals, which are connected with each of the channel layers of the I/O protective thin film transistors, and p-type substrate potential fixing terminals and n-type substrate potential fixing terminals are connected with the ground terminals.

(21) **Appl. No.: 11/514,759**(22) **Filed: Sep. 1, 2006****Related U.S. Application Data**

(63) Continuation of application No. 10/401,311, filed on Mar. 26, 2003, now Pat. No. 7,138,987.

(30) **Foreign Application Priority Data**

Mar. 29, 2002 (JP) 2002-94476

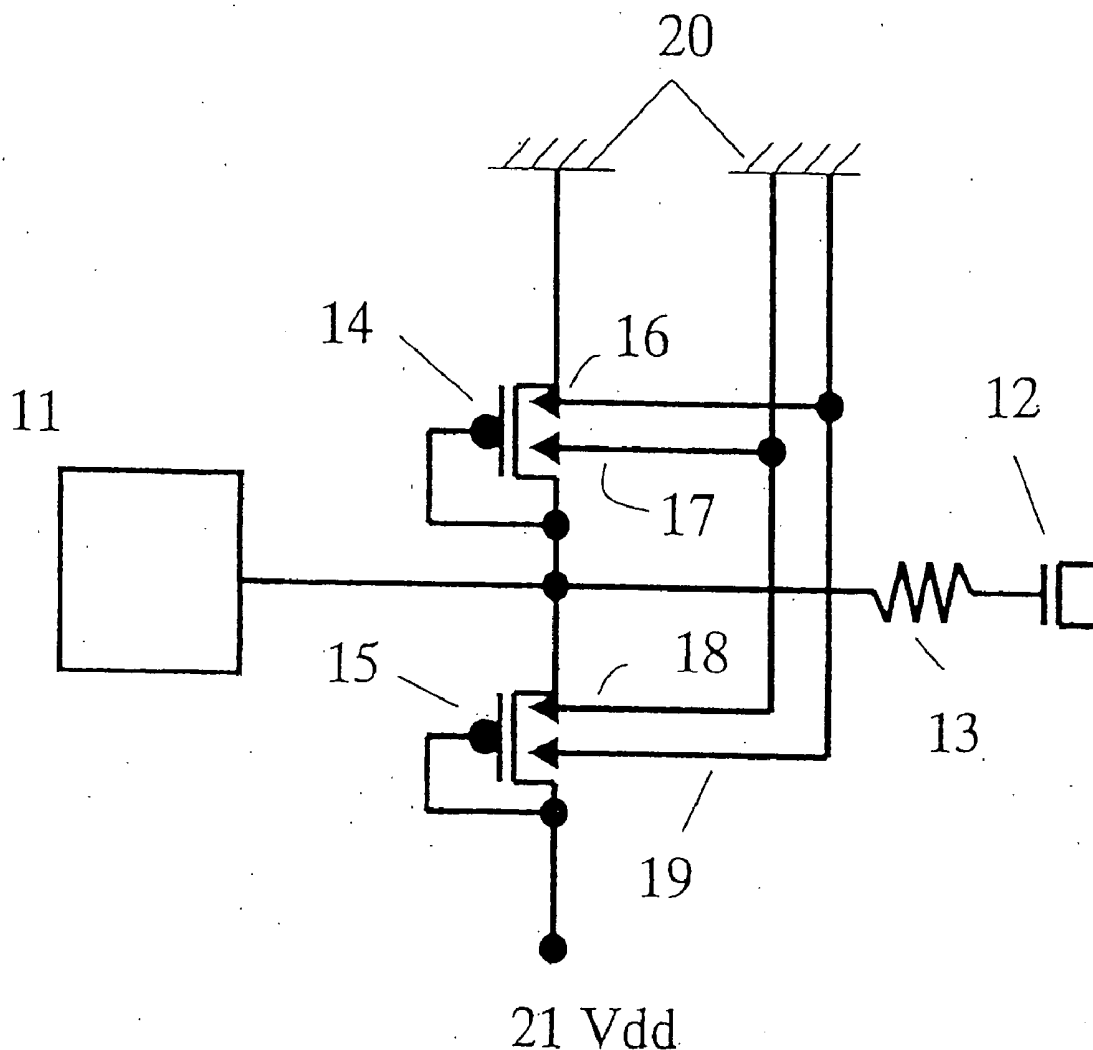


FIG. 1

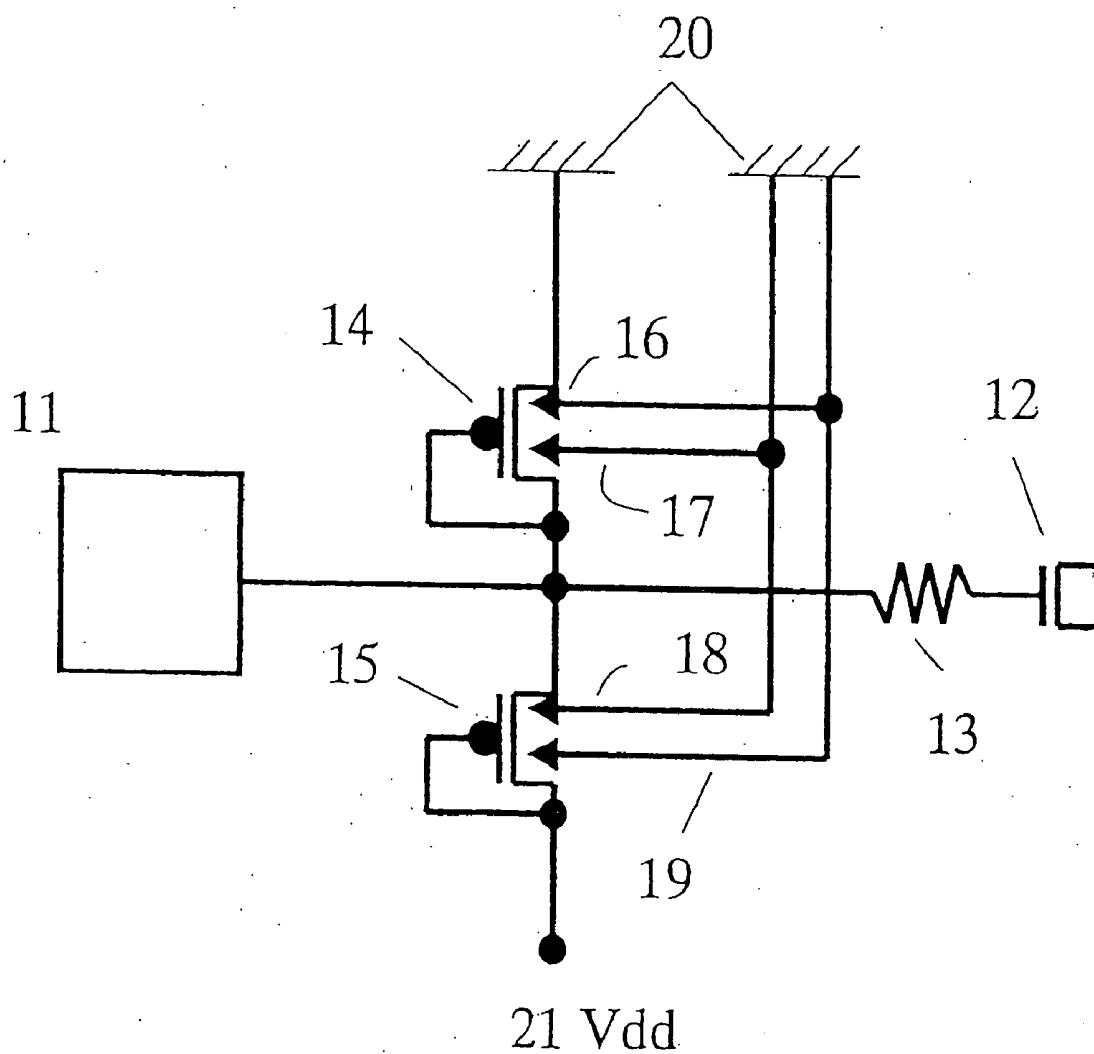


FIG. 2a

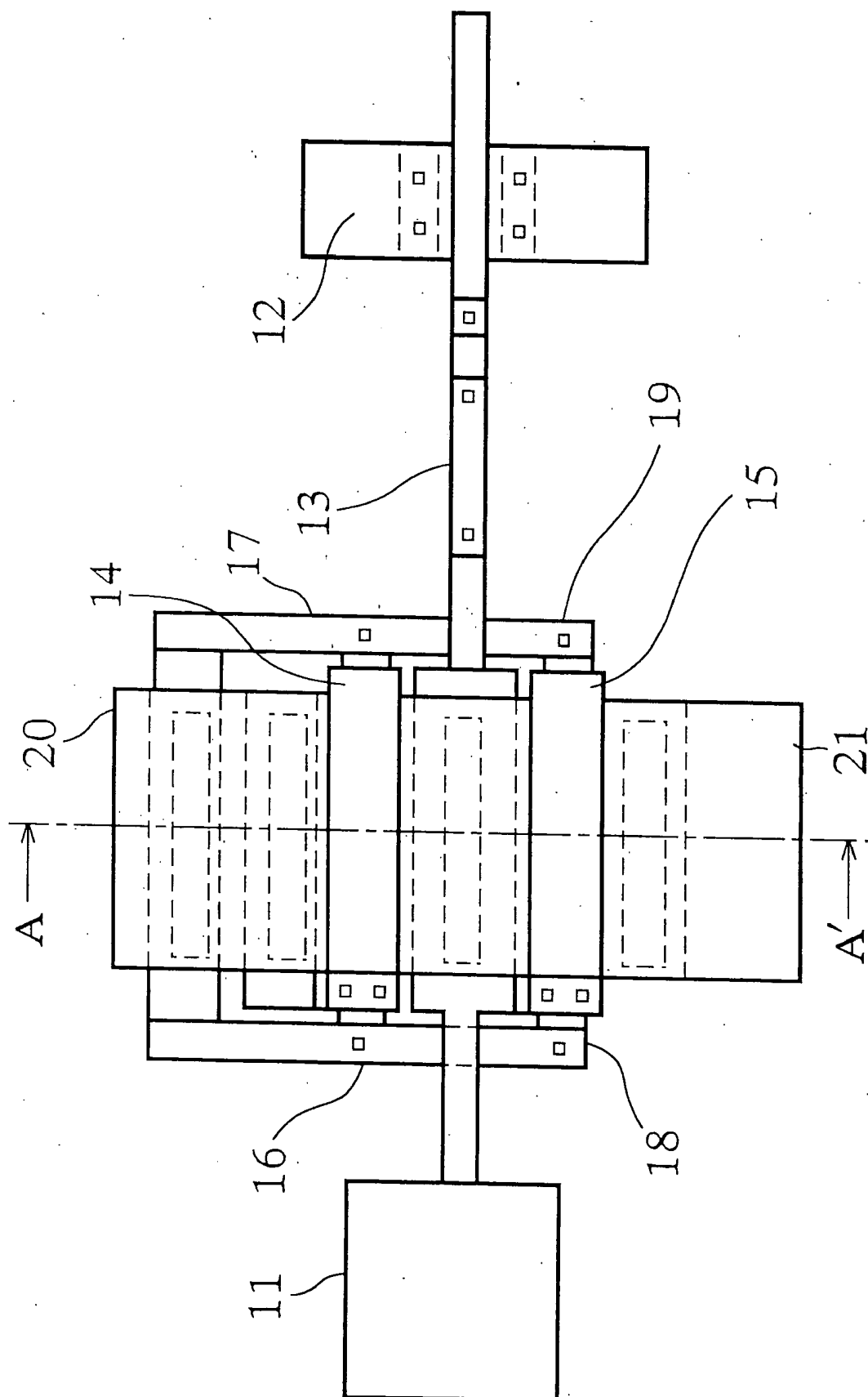


FIG. 2 b

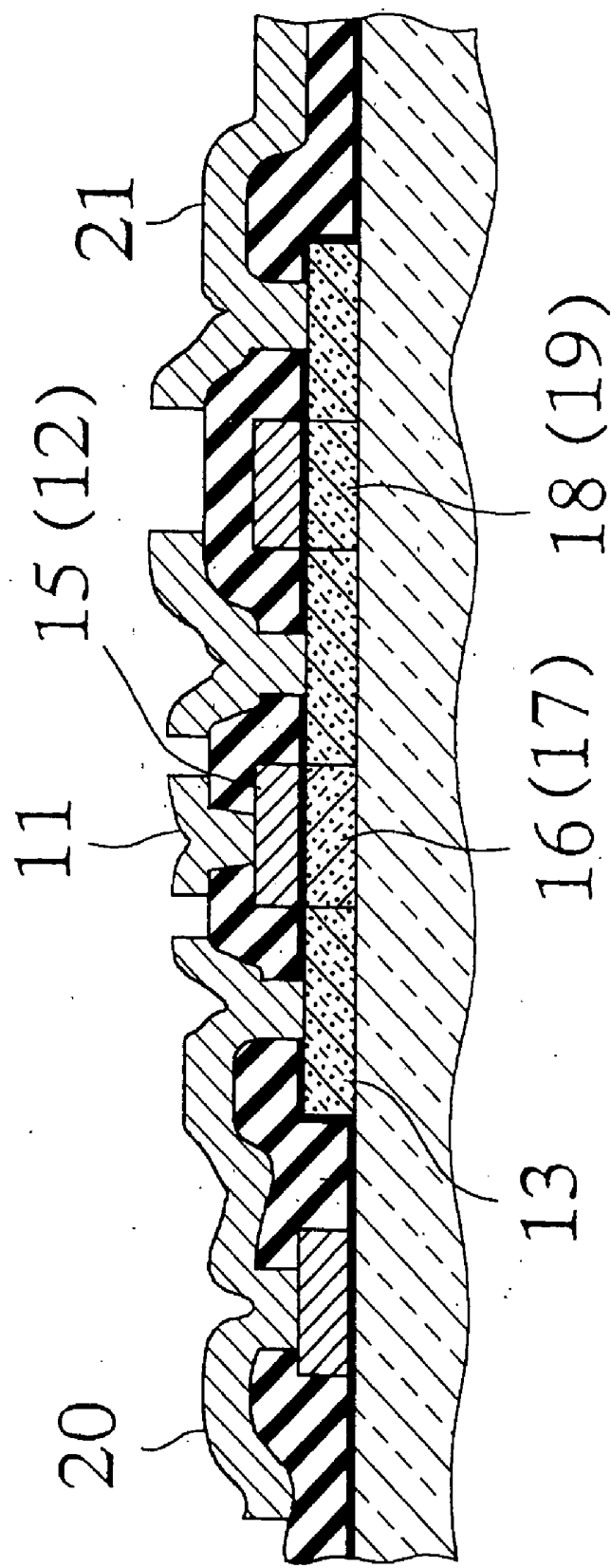


FIG. 3

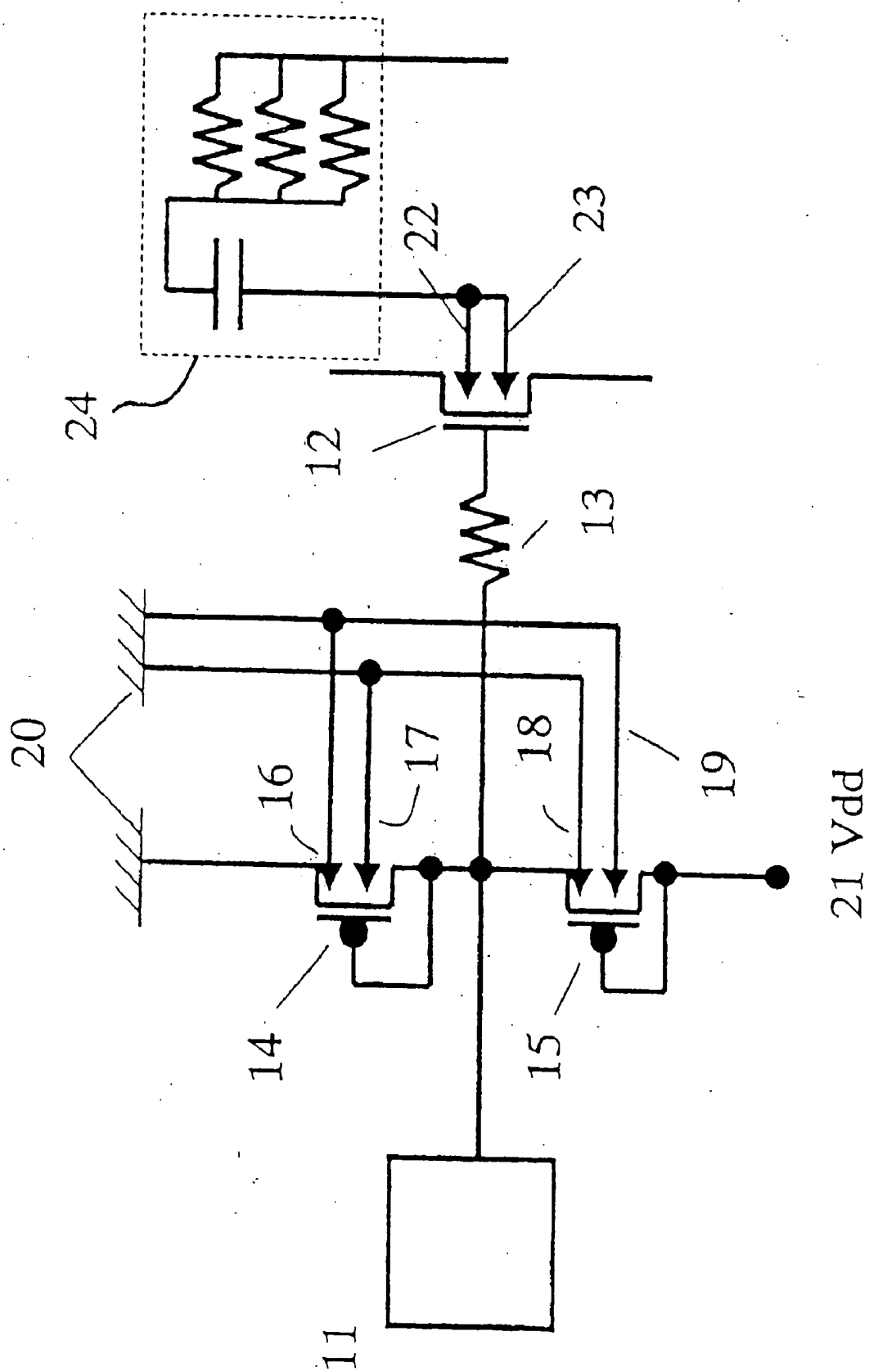


FIG. 4a

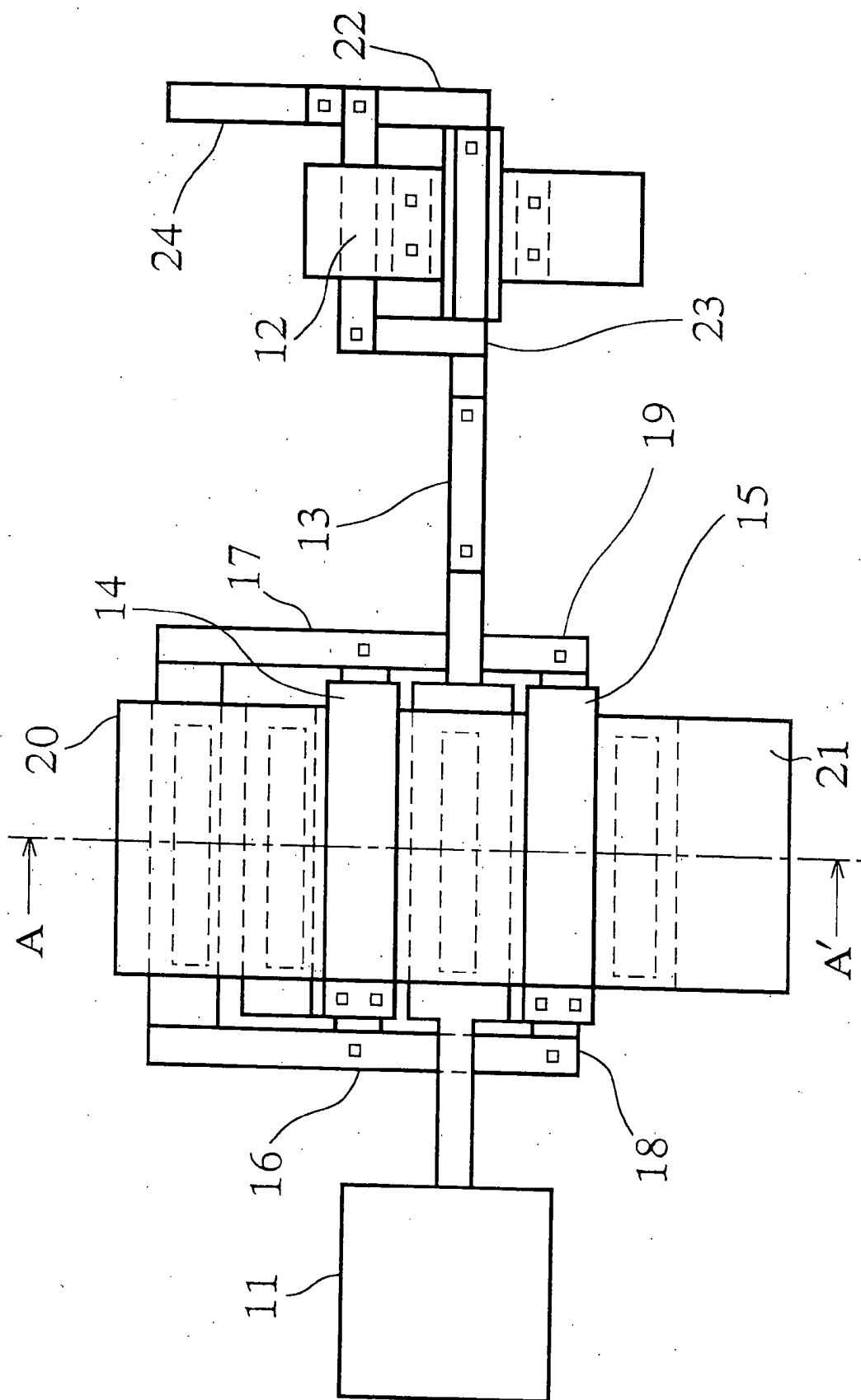


FIG. 4 b

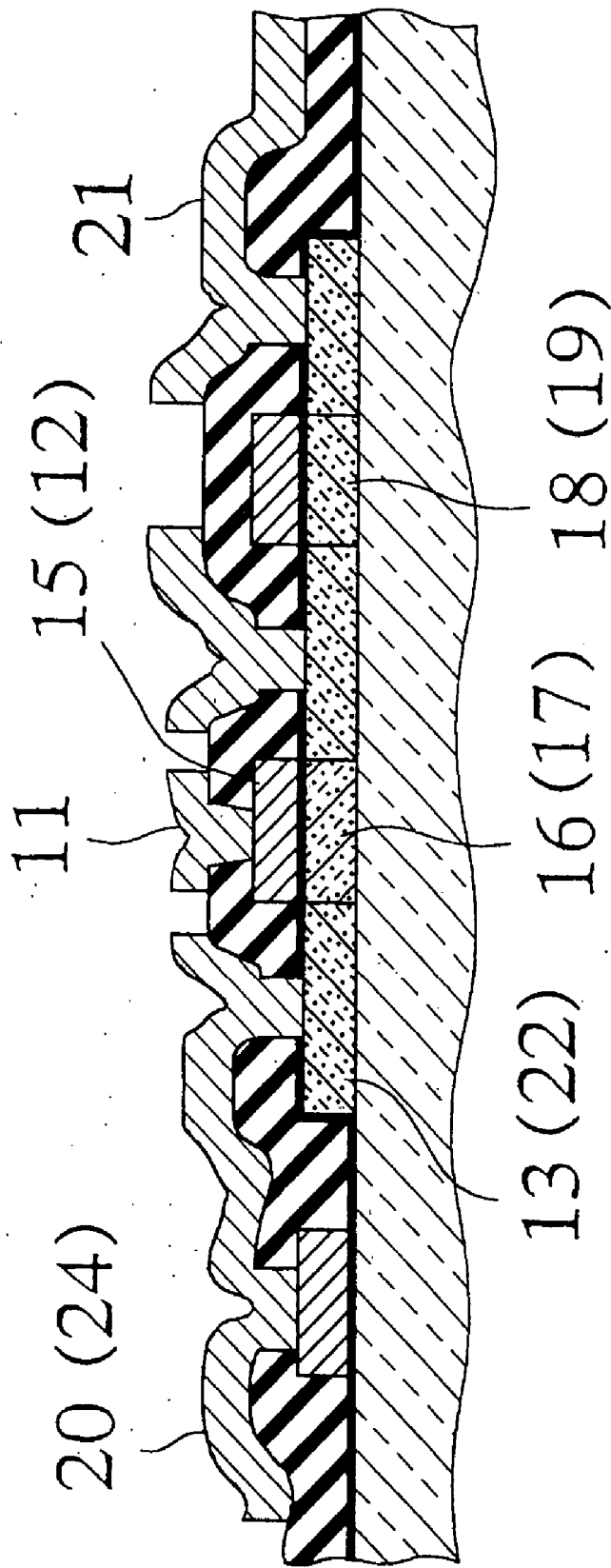
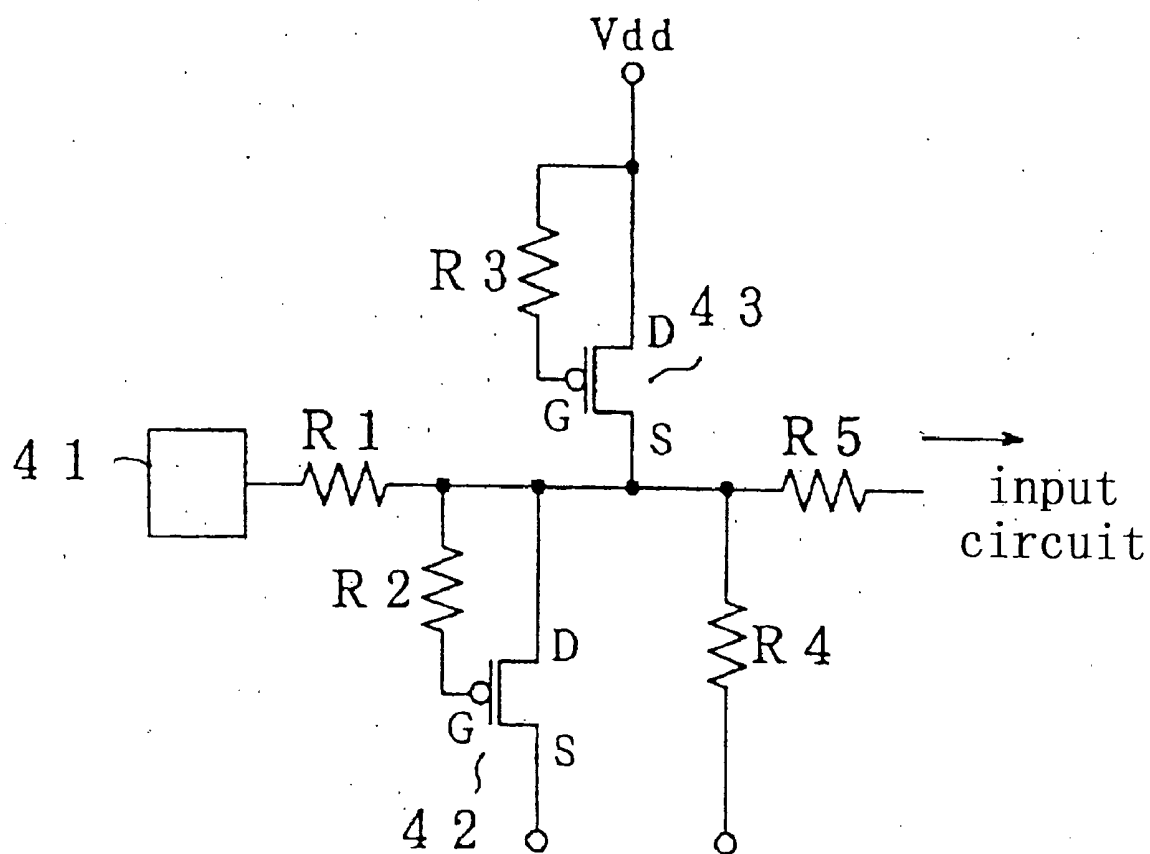
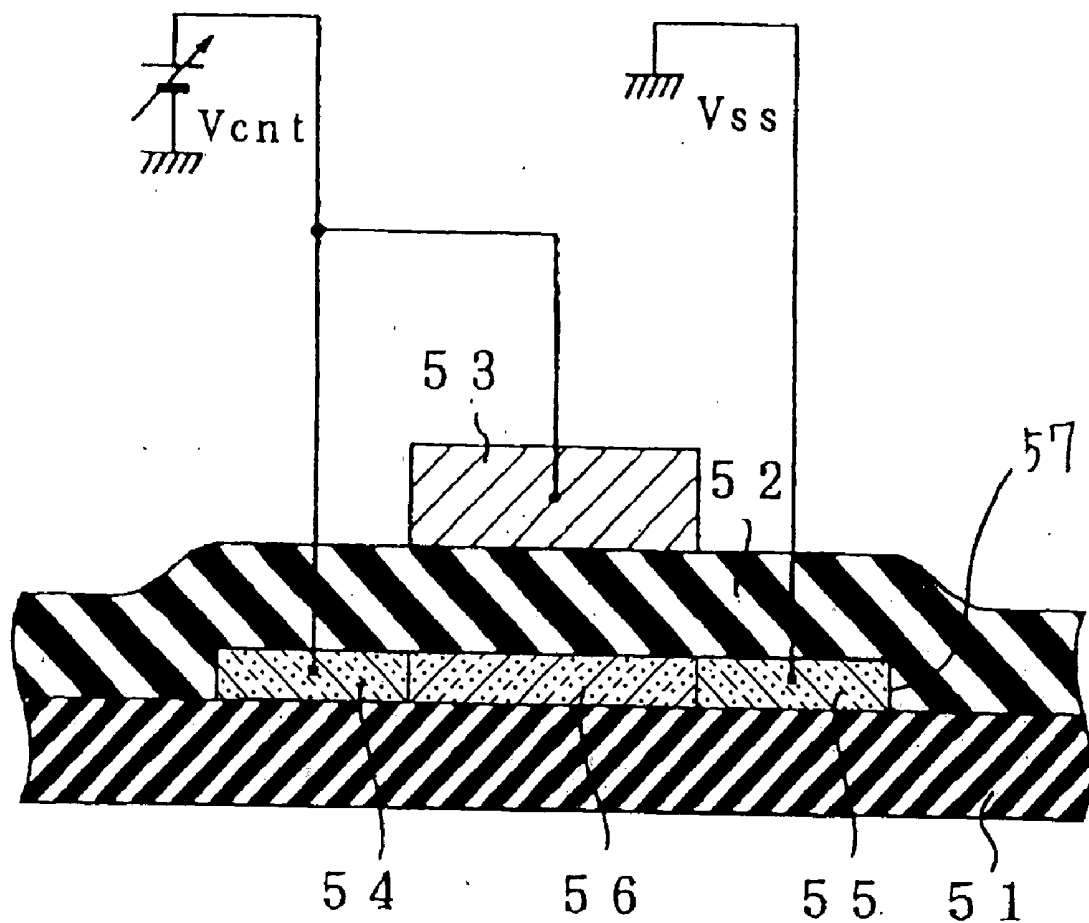


FIG. 5



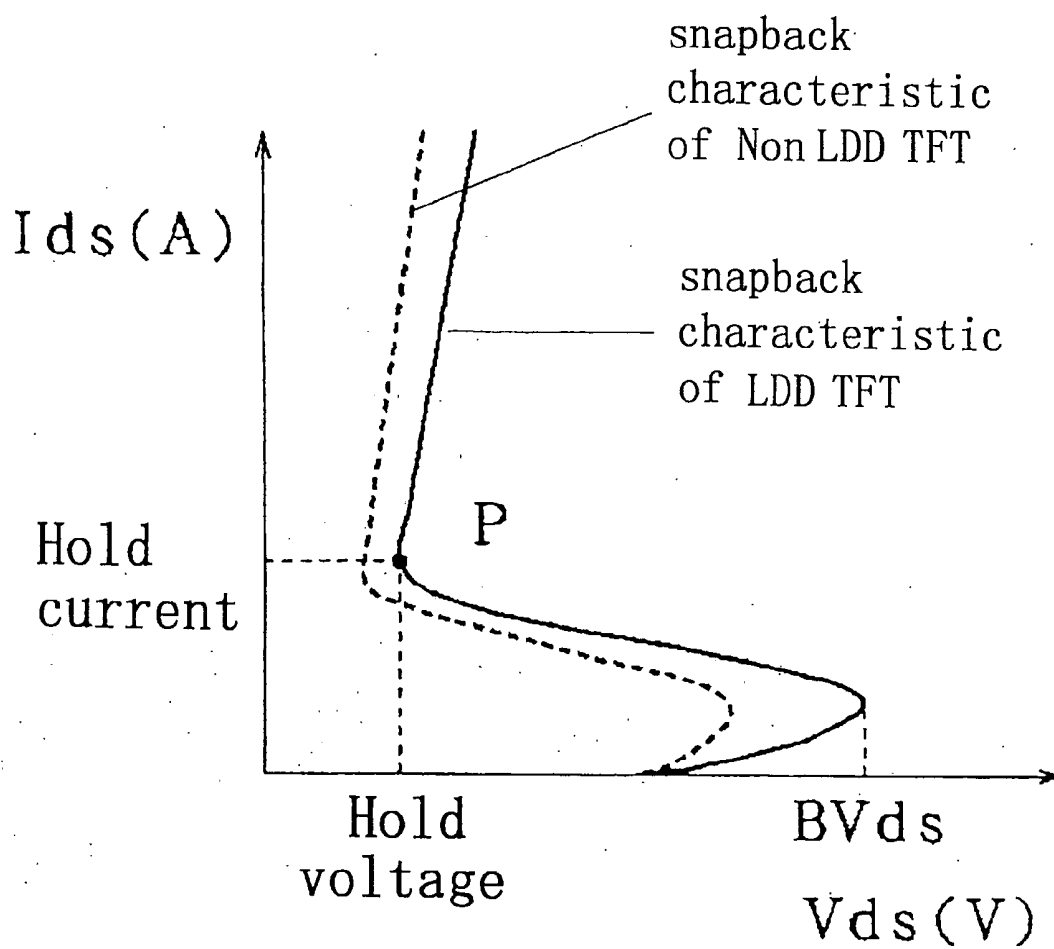
PRIOR ART

FIG. 6



PRIOR ART

FIG. 7



PRIOR ART

PROTECTIVE CIRCUIT FOR A THIN FILM TRANSISTOR AND A LIQUID CRYSTAL DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This is a continuation application claiming benefit, under 35 USC §120, of co-pending U.S. utility application Ser. No. 10/401,311 filed on 26 Mar. 2003, which claims foreign priority benefits under 35 USC §119 (a) to Japan Patent Application No. 2002-094476, filed Mar. 29, 2002, which applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an input-output (I/O) protective circuit for use in a liquid crystal display device, wherein an I/O primary stage thin film transistor is provided with an I/O protective function as an antistatic countermeasure against the surge current, the noise voltage and so forth.

[0004] 2. Prior Art

[0005] In a liquid crystal display device (abbreviated as LCD hereinafter) including a prior art thin film transistor (abbreviated as TFT hereinafter) made of a polycrystalline silicon layer formed at a low temperature, the switching TFT set up at each pixel position, a driving circuit for the liquid crystal panel and the I/O protective circuit respectively include an n-channel lightly-doped-drain TFT (referred to as LDD MOS TFT hereinafter).

[0006] FIG. 5 is a circuit diagram showing an equivalent circuit of a prior art I/O protective circuit for LCD.

[0007] As shown in FIG. 5, the voltage supplied to opposing electrodes and others via an I/O terminal pad 41 is applied to this I/O protective circuit.

[0008] The I/O protective circuit includes an I/O protective TFT 42, an I/O resistance R1, and a resistance R2 connected between the gate G and the drain D of the I/O protective TFT 42. In the output portion of the I/O protective circuit, on one hand, there are provided an I/O primary stage TFT 43 and resistances R3, R4 and R5. The I/O protective TFT 42 and the I/O primary stage TFT 43 are a TFT having a LDD structure. The source S formed of the diffusion layer of the I/O protective TFT 42 is connected with a power source Vss. The I/O primary stage TFT 43 is a buffer giving the voltage (current) to the opposed electrodes of the liquid crystal panel, and the drain D of it is connected with the gate G via the resistance R3 as well as with the power source Vdd. The source S of the I/O primary stage TFT 43 is connected with the power source Vss via the resistance R4 as well as with the drain D of the I/O protective TFT 42 and further connected with an input circuit via the resistance R5.

[0009] The I/O protective TFT 42 and the I/O primary stage TFT 43 are not formed on a semiconductor substrate like silicon (Si) different from an ordinary semiconductor element. They are made of polycrystalline silicon and formed on a glass plate by mean of a photolithographic method. In case of the TFT for LCD, as the channel layer of the TFT is made of intrinsic semiconductor (non-doped Si),

it is often seen that any potential to be referred to as a standard potential is not given to the substrate i.e. the channel layer.

[0010] However, as the circuit constitution as described above fails to make sure of a sufficient way of escape for the electric current having flowed into the I/O protective circuit, the electrostatic breakdown might be caused at the insulating film or the junction of the I/O protective TFT constituting the I/O protective circuit, thus it becoming hard for the I/O protective circuit to play its essential role. This is one problem to be solved.

[0011] The snapback phenomenon will now be explained with reference to FIGS. 6 and 7.

[0012] In the MOS TFT having a structure as shown in FIG. 6, a polycrystalline silicon layer 57 is formed on an insulating oxide film 51 and then, a gate insulating film 52 is further formed to cover the silicon film 57. Still further, the gate electrode 53 is formed on the gate insulating film 52. In the next, a predetermined impurity is doped in the polycrystalline silicon layer 57 by making use of the pattern of the gate electrode 53, thereby a drain region 54 and a source region 55 being formed and at the same time, a region between the above two regions 54 and 55 being formed as a channel region 56. In a TFT having the LDD structure like this, the source region 55 is connected with the power source Vss while the drain region 54 and the gate electrode 53 are commonly connected with each other such that a control voltage Vcnt is given to both of them.

[0013] In the next, it is studied how the current Ids flowing between the drain region 54 and the source region 55 changes in response to the change of the control voltage Vcnt which controls the voltage Vds applied between the drain region 54 and the source region 55. As a result, it is found that the relation between the voltage Vds and the current Ids changes along a solid line of a graph as shown in FIG. 7. As will be seen from the above graph, if the applied voltage Vds once exceeds the breakdown voltage (breakout voltage) BVds of the above MOS TFT, the current Ids abruptly begins to flow and can not decrease even though the applied voltage Vds is returned to the level lower than the breakdown voltage BVds. Moreover, the current Ids begins to rather increase at a still lower applied voltage Vds, that is, the secondary breakdown takes place. The phenomenon like this is called a snapback phenomenon.

[0014] In FIG. 7 showing the snapback characteristic of the MOS TFT, the voltage at a point P is called a hold voltage while the current at P is called a hold current. The snapback characteristic like this is called the bipolar action of the MOS TFT. If the impurity density difference between the drain and the substrate (i.e. channel) becomes large, the characteristic is shifted from that which is indicated by a solid line to that which is shown by a dotted line as shown in FIG. 7. In other words, the breakdown voltage BVds becomes lower and at the same time, the hold voltage becomes lower, too. The TFT of this type is herein called a non-LDD TFT.

[0015] The TFT having the high breakdown voltage BVds as well as the high hold voltage like the above-mentioned, might be most suitably used as a driving TFT for the liquid crystal display panel, but it is not suitable for using as the I/O protective TFT. On one hand, in case of the TFT as used in

LCD, as it is not possible to fix the standard potential of the substrate, the potential of the substrate can not be free from the influence of the fixed electric charge existing in the foundation film on the substrate side, the semiconductor layer, insulating gate film and so forth. Thus, the potential of the substrate is made unstable due to the above electrostatic charges, thereby the characteristic of the TFT being changed and becoming unstable. This is another problem to be solved in addition to the one as mentioned above.

[0016] As described above, however, as the prior art I/O protective circuit for LCD fails to provide a sufficient way of escape allowing the current having flowed into the I/O protective circuit to get out therefrom, it constitutes the switching element for driving each pixel of the liquid crystal panel or the I/O primary TFT by using the LDD TFT, but with regard to the I/O protective circuit, there has been not used the non-LDD TFT of which the breakdown voltage BV_ds and the hold voltage at the time of the snapback are lower than those of the LDD TFT, respectively.

[0017] Accordingly, the invention has been made in view of the above-mentioned problems and others and an object of the invention is to provide an I/O protective circuit for LCD having more stable I/O protective function.

SUMMARY OF THE INVENTION

[0018] In order to solve the problems as described above, the invention takes such constitutions as recited in the scope of claim for patent as attached to this specification.

[0019] The invention, in certain embodiments, relates to an input-output (I/O) protective circuit for a LCD having an I/O primary stage thin film transistor, and includes an I/O protective thin film transistor having a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal, both of which are operatively coupled to a channel layer of the I/O protective thin film transistor, wherein both of the p- and n-type substrate potential fixing terminals are connected with a ground terminal. A breakdown voltage and a hold voltage of the I/O protective thin film transistor are made, respectively, lower than those of the I/O primary stage thin film transistor or those of a thin film transistor used as a switching element for driving a pixel of the LCD device.

[0020] The invention, in certain other embodiments, relates to an IO protective circuit for a LCD and includes a resistance provided between an I/O terminal pad and an I/O primary stage thin film transistor, a wiring connecting the I/O terminal pad with the resistance, and two I/O protective thin film transistors connected in series between a ground terminal and a power source terminal, wherein the wiring is connected with each joint portion of the two I/O protective thin film transistors, each of the two I/O protective thin film transistors has a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal, both of which are connected with a channel layer of the I/O protective thin film transistor, and the p- and n-type substrate potentials fixing terminals are connected with the ground terminal. In addition, a breakdown voltage and a hold voltage of the I/O protective thin film transistors are made, respectively, lower than those of the I/O primary stage thin film transistor or those of a thin film transistor used as a switching element for driving a pixel of the LCD device.

[0021] The invention, in yet other embodiments, relates to a protective circuit for use in a LCD device connectable to an input circuit of a primary stage thin film transistor, and includes a thin film transistor having a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal operatively coupled to a channel layer, and a ground terminal operatively coupled to the p-type and the n-type substrate potential fixing terminal, wherein a breakdown voltage and a hold voltage of the protective thin film transistor are made, respectively, lower than those of the primary stage thin film transistor or those of a thin film transistor used as a switching element for driving a pixel of the LCD device.

[0022] The invention, in still other embodiments, relates to a protective circuit for use in a LCD device connectable to an input circuit of a primary stage thin film transistor, and includes first and second protective thin film transistors, each having a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal operatively coupled to a channel layer on a positive side of the circuit, and a ground terminal operatively coupled to the p-type and the n-type substrate potential fixing terminals, wherein a breakdown voltage and a hold voltage of the protective thin film transistor are made, respectively, lower than those of the primary stage thin film transistor or those of a thin film transistor used as a switching element for driving a pixel of the LCD device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] In the drawings:

[0024] FIG. 1 is a circuit diagram of an I/O protective circuit for LCD according to the first embodiment of the invention.

[0025] FIG. 2a is a plan view showing a structure of the I/O protective circuit for LCD according to the first embodiment of the invention, corresponding to the circuit as shown in FIG. 1. FIG. 2b is a sectional view taken on line A-A' in FIG. 2a.

[0026] FIG. 3 is an input-output (I/O) protective circuit for LCD according to the second embodiment of the invention.

[0027] FIG. 4a is a plan view corresponding to the circuit as shown in FIG. 3, that is, the I/O protective circuit for LCD according to the second embodiment of the invention. FIG. 4b is a sectional view taken on line A-A' in FIG. 4a.

[0028] FIG. 5 is an equivalent circuit diagram of the prior art I/O protective circuit for LCD.

[0029] FIG. 6 is a diagram showing an electrical connection between respective electrodes as used in a method of measuring the snapback characteristic of a MOS TFT.

[0030] FIG. 7 is a graph showing the snapback characteristic of a MOS TFT.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] An I/O protective circuit for LCD according to the invention will now be described in detail by way of some embodiments thereof with reference to the accompanying drawings in which constituents of the invention having like

function are designated by like reference numerals and signs, thus repetitive description thereabout being omitted for simplification.

First Embodiment

[0032] FIG. 1 is a circuit diagram of an input-output (I/O) protective circuit for LCD according to the first embodiment of the invention, FIG. 2a is a plan view showing a structure of the I/O protective circuit for LCD according to the first embodiment of the invention, corresponding to the circuit as shown in FIG. 1, and FIG. 2b is a sectional view taken on line A-A' in FIG. 2a.

[0033] In FIGS. 1, 2a and 2b, a reference numeral 11 indicates an I/O terminal pad, 12 an I/O primary stage TFT, 13 an I/O protective resistance, 14 and 15 an I/O protective TFT, 16 an n-type substrate potential fixing terminal connected with the channel layer of the I/O protective TFT 14, in other words, a metal electrode terminal which fixes the potential of an n-type substrate (i.e. channel layer) and is connected with an n-type impurity doped region provided so as to be connected with the channel layer, similar to the above, 17 a p-type substrate potential fixing terminal connected with the channel layer of the I/O protective TFT 14, 18 an n-type substrate potential fixing terminal connected with the channel layer of the I/O protective TFT 15, 19 a p-type substrate potential fixing terminal connected with the channel layer of the I/O protective TFT 15, 20 a ground terminal (earth terminal), and 21 a power source.

[0034] As the circuit constitution after the I/O primary stage TFT 12 is publicly known well, it is omitted to show it by means of an illustration and others.

[0035] The resistance 13 ($300\ \Omega \sim 2.0\ K\Omega$) is provided between the I/O terminal pad 11 and the I/O primary stage TFT 12, the resistances 13 being made in the form of a diffusion layer for instance a layer similar to an n-type high impurity density layer used for forming source and drain regions. The number of resistance 13 is not limited to only one. Two or more resistances may be prepared, for instance between a joint portion at which the wiring connecting the I/O terminal 11 with the resistance joins to two I/O protective TFT's, and the I/O terminal pad 11. With introduction of this resistance 13, the surge current can be guided to the I/O protective circuit before it flows into the I/O primary stage TFT 12 forming a part of the I/O circuit and also flows into the I/O circuit related to the I/O primary stage 12, thereby making the response characteristic inferior, for instance by making the response speed slow.

[0036] Two I/O protective TFT's 14 and 15 are connected between the resistance 13 and the I/O terminal 11. The breakdown voltage BVds and the hold voltage in the snap-back characteristic of these I/O protective TFE's 14 and 15 are set to be lower than those of the I/O primary stage TFT 12 (or the before-mentioned TFT as a switching element for driving the pixel of the LCD. This means that the I/O protective circuit is set such that it can begin its operation before the above-mentioned I/O protective circuit enters its on-operation state. The gate width of the I/O protective TFT's 14, 15 is made larger than that of the I/O primary stage TFT 12 in order to prevent the destruction of the I/O protective TFT's 14, 15 by a large surge current. The gate width is determined by the magnitude of the power supply, the preferable width is 100 μm or more.

[0037] The I/O protective TFT 14 is an I/O protective TFT against the noise surge on the plus side and its source is connected with the ground terminal 20 as shown in FIG. 1. The channel layer of the I/O protective TFT 14 is connected with the n- and p-type substrate potential fixing terminals 16, 17. That is, as shown in FIG. 2a, these n- and the p-type substrate potential fixing terminals 16, 17 are made of a metal electrode electrically connected with the n- and the p-type impurity doped regions, both of which are provided in a region connected with the channel layer of the I/O protective TFT 14.

[0038] The I/O protective TFT 15 is an I/O protective TFT against the noise surge on the minus side and its source is connected with the terminal 21 of the power source (Vdd). The channel layer of the I/O protective TFT 15 is connected with the n- and p-type substrate potential fixing terminals 18, 19. That is, as shown in FIG. 2a, the n- and p-type substrate potential fixing terminals 18, 19 are constituted by a metal electrode electrically connected with the n- and p-type impurity doped region, both of which are provided in a region connected with the channel layer of the I/O protective TFT 15.

[0039] The I/O terminal pad 11 is made up of an upper layer and a lower layer and is made of a metal for instance titanium (Ti) for the upper layer and aluminum (Al) for the lower layer. The order of the metal layers may be reversed, that is, Al for the upper layer and Ti for the lower layer.

[0040] The I/O primary stage TFT 21 has a gate electrode made of a metal for instance MoW, Al and so for forth, a source and a drain of which each is made in the form of an n-type semiconductor layer made of silicon. The above semiconductor layer including the source and the drain is electrically separated from the gate electrode by an insulating film while the source and the drain are connected with a metal film such as an Al film through corresponding contact holes.

[0041] The resistance 13 is made in the form of an n-type silicon layer, but it may be made in the form of a p-type silicon layer and other material.

[0042] I/O protective TFT's 14, 15 are similar to the I/O primary stage TFT 21 as far as the structure of their gate, source and drain are concerned. In case of the I/O protective TFT 14, however, the n- and p-type substrate potential fixing terminals 16 and 17 are connected with an intrinsic semiconductor layers (I-layer) under the gate electrode. Similarly, in case of the I/O protective TFT 15, the n- and p-type substrate potential fixing terminals 18, 19 are connected with an intrinsic semiconductor layers (I-layer) under the gate electrode. These substrate potential fixing terminals 16, 17, 18 and 19 are put together by a wiring made of a gate electrode material and connected with the ground terminal 20 in a lump through a contact hole.

[0043] As described above, in the I/O protective TFT 14, the substrate (i.e. channel layer) potential of it is fixed by n- and p-type substrate potential fixing terminals 16, 17 while in the I/O protective TFT 15, the substrate potential of it is fixed by n- and p-type substrate potential fixing terminals 18, 19.

[0044] The characteristic of the I/O protective TFT's 14 and 15 can be stabilized by these n- and p-type substrate potential fixing terminals 16, 17 and n- and p-type substrate

potential fixing terminals **18, 19**. Furthermore, even though the surge current takes place, as it flows into these n- and p-type substrate potential fixing terminals **16, 17** and n- and p-type substrate potential fixing terminals **18, 19**, the I/O protective TFT's **14, 15** are prevented from being destroyed by one attack of the surge current.

[0045] In case of the ordinary TFT, it is difficult to evaluate the characteristic of it separately in the vertical direction and in the lateral direction unless the boundary level and the bulk level are permitted to think of them as completely independent level. As described above, according to the invention, the I/O protective TFT **14** is provided with one each of substrate potential fixing terminals of the n- and p-type **16** and **17** and, similarly, the I/O protective TFT **15** is provided with one each of substrate potential fixing terminals of the n- and p-type **18** and **19**. With provision of the above potential fixing terminals, I/O protective TFT's **14, 15** come to show the same effect as is obtainable if a PIN diode is provided in the lateral direction of n-type (or p-type) TFT's **14, 15**. In other words, each of I/O protective TFT's **14, 15** comes to have a 5-terminal structure including the above two potential fixing terminals and three terminals for the gate, source and drain. Thus, it becomes possible to independently to evaluate the characteristic of the I/O protective TFT's **14, 15** in the vertical direction as well as in the lateral direction, that is, in the longitudinal direction of the PIN diode.

[0046] As described above, the I/O protective circuit according to the first embodiment includes I/O protective TFT's **14, 15** having p-type substrate potential fixing terminals **17, 19** and n-type substrate potential fixing terminals **16, 18** both of which are connected with the channel layer of the I/O protective TFT **14, 15**, wherein p-type substrate potential fixing terminals **17, 19** and n-type substrate potential fixing terminals **16, 18** are connected with a ground terminal **20** (corres. To claim 1).

[0047] Furthermore, an I/O protective circuit according to the first embodiment includes a resistance **13** provided between an I/O terminal pad **11** and an I/O primary stage TFT **12**, a wiring connecting the I/O terminal pad **11** with the resistance **13**, and two I/O protective TFT's **14, 15** connected in series between a ground terminal **20** and a power source terminal **21**, wherein the wiring is connected with the joint portion of the two I/O protective thin film transistors **14, 15**, each of two I/O protective TFT's **14, 15** has p-type substrate potential fixing terminals **17, 19** and n-type substrate potential fixing terminals **16, 18**, both of which are connected with the channel layer of the I/O protective TFT, and p-type substrate potential fixing terminals **17, 19** and n-type substrate potential fixing terminals **16, 18** are connected with the ground terminal **20** (corres. To claim 2).

[0048] Still further, in an I/O protective circuit according to the first embodiment, the breakdown voltage and the hold voltage of the I/O protective TFT's **14, 15** are respectively made lower than those of the I/O primary stage TFT **12** or those of the TFT used as a switching element for driving the pixel of the LCD (corres. To claim 4).

Second Embodiment

[0049] FIG. 3 is a circuit diagram of an I/O protective circuit for LCD according to the second embodiment of the invention, and FIG. 4a is a plan view showing a structure of

the I/O protective circuit for LCD according to the second embodiment of the invention, corresponding to the circuit as shown in FIG. 3, FIG. 4b is a sectional view taken on line A-A' in FIG. 4a.

[0050] In FIGS. 3, 4a and 4b, a reference numeral **22** indicates an n-type substrate potential fixing terminal connected with the channel layer of an I/O primary stage TFT **12**, in other words, a metal electrode terminal which fixes the potential of an n-type substrate (i.e. channel layer) and is connected with an n-type impurity doped region provided so as to be connected with the channel layer, similar to the above, **23** a p-type substrate potential fixing terminal connected with the channel layer of the I/O primary stage protective TFT **12**, and **24** a substrate bias generation circuit (substrate potential generation circuit, substrate bias correction circuit) which is connected with n- and p-type substrate potential fixing terminals **22, 23** connected with the I/O primary stage TFT **12**.

[0051] As the first embodiment as shown in FIGS. 1, 2a, 2b and the second embodiment as shown in FIGS. 3, 4a, 4b have the same structure with regard to the circuit from the I/O terminal pad **11** up to the ground terminal **20** with which the I/O protective circuit is connected, the description thereabout will be omitted.

[0052] In FIGS. 3, 4a and 4b, an I/O primary stage TFT **12** is connected with n- and p-type substrate potential fixing terminals **22, 23**, which are connected with a substrate bias generation circuit **24** applying a predetermined voltage to the above substrate potential fixing terminals **22** and **23**. I/O protective TFT's **14, 15** are able to stably operates by setting the breakdown voltage BVds of the I/O primary stage TFT **12** to be higher than that of the I/O protective TFT's **14, 15**. As shown in FIG. 3, the substrate bias generation circuit **24** includes a resistance made of a fuse and others before a capacitance and is able to adjust the substrate potential of the I/O primary stage TFT **12**.

[0053] As described above, according to the second embodiment, the electrical instability of the I/O protective TFT's **14, 15** due to the unfixed substrate potential thereof can be obviated by providing n-type substrate potential fixing terminal **16, 18** and p-type substrate potential fixing terminal **17, 19**, and also the I/O protective TFT's **14, 15** is prevented from being destroyed by the one attack of the surge noise current flowing into not only the source side but the substrate side.

[0054] In the second embodiment, the channel layer of the I/O primary stage TFT **12** is connected with the n- and p-type substrate potential fixing terminals **22, 23**. The substrate bias generation circuit **24** applies an adjusted substrate potential to the I/O primary stage TFT **12** such that the breakdown voltage BVds of the I/O primary stage TFT **12** is always kept larger than that of the I/O protective circuit.

[0055] Accordingly, similar to the first embodiment, as the I/O protective TFT's **14, 15** and the I/O primary stage TFT **12** are provided with the n-type substrate potential fixing terminals **16, 18, 22** and the p-type substrate potential fixing terminals **17, 19, 23**, the I/O protective TFT's **14, 15** and the I/O primary stage TFT **12** come to show the same effect as is obtainable if a PIN diode is provided in the respective lateral direction of them. In other words, each of I/O protective TFT's **14, 15** and the I/O primary stage TFT **12**

comes to have a 5-terminal structure including the above two potential fixing terminals and three terminals for the gate, source and drain. Thus, it becomes possible to independently evaluate each characteristic of the I/O protective TFT's 14, 15 and the I/O primary stage TFT 12 in the vertical direction as well as in the lateral direction, that is, in the longitudinal direction of the PIN diode.

[0056] As described above, an I/O protective circuit for LCD including the I/O primary stage TFT 12 having the n-type substrate potential fixing terminal 22 and the p-type substrate potential fixing terminal 23 both of which are connected with the channel layer of the I/O primary stage TFT 12 as well as with the substrate bias generation circuit 24.

[0057] While some embodiments of the invention have been concretely shown and described in the above with reference to the accompanying drawings, the invention is not limited to such embodiments. Various changes and modifications will be possible without departing from the gist of the invention.

[0058] As has been described so far, according to the invention, it becomes possible to provide an I/O protective circuit for LCD, having more stable I/O protective function.

What is claimed:

1. A protective circuit for a thin film transistor formed from a protective thin film transistor connected with an input circuit of a protected thin film transistor, comprising:

a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal, both of which are connected with the channel layer of said protective thin film transistor; and

a ground terminal connected with said p-type and n-type substrate potential fixing terminals.

2. A protective circuit for a thin film transistor connected with an input circuit of a protected thin film transistor, comprising:

a first protective thin film transistor connected with said input circuit and having a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal in its channel layer acting against surge noise input on the positive side;

a second protective thin film transistor connected with said input circuit and having a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal in its channel layer acting against surge noise input on the negative side; and

a ground terminal connected with p-type substrate potential fixing terminals and n-type substrate potential fixing terminals of said first and second protective thin film transistors.

3. A protective circuit for a thin film transistor as claimed in claim 1 or 2, wherein the width of a gate of said protective thin film transistor is larger than the width of a gate of said protected thin film transistor.

4. A protective circuit for a thin film transistor as claimed in claim 1 or 2, wherein the width of the gate of said protective thin film transistor is 100 μm or more.

5. A protective circuit for a thin film transistor as claimed in claim 1 or 2, wherein said protected thin film transistor has a p-type substrate potential fixing terminal and an n-type

substrate potential fixing terminal in its channel layer, and wherein said p-type and n-type substrate potential fixing terminals are connected with a substrate bias generation circuit.

6. A protective circuit for a thin film transistor as claimed in claim 1,

a breakdown voltage and a hold voltage of said protective thin film transistor are made respectively lower than a breakdown voltage and a hold voltage of the thin film transistor of said protected circuit or those of a thin film transistor used as a switching element for driving a pixel.

7. A liquid crystal display device having a glass substrate, a switching thin film transistor circuit provided at each pixel position on said glass substrate, and a liquid crystal panel having a drive circuit for driving the switching thin film transistor,

wherein a protective thin film transistor is connected with an input circuit of a primary stage thin film transistor which gives a voltage (current) to an opposing electrode of said liquid crystal panel;

wherein said protective thin film transistor is a transistor having a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal in its channel layer; and

wherein a circuit for connecting said p-type substrate potential fixing terminal and said n-type substrate potential fixing terminal are connected with a ground terminal is provided.

8. A liquid crystal display device having a protective circuit formed from a protective thin film transistor, connected with the input circuit of a protected thin film transistor, comprising:

a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal provided in a channel layer of the thin film transistor of said protective circuit; and

a ground terminal connected with said p-type substrate potential fixing terminal and said n-type substrate potential fixing terminal,

wherein a breakdown voltage and a hold voltage of said protective thin film transistor are respectively made lower than those of said protected thin film transistor or the thin film transistor used as a switching element for driving a pixel.

9. A liquid crystal display device comprising:

a resistance connected between a terminal pad and a protected thin film transistor;

a wiring connecting said terminal pad with said resistance; and

two protective thin film transistors connected in series between a ground terminal and a source terminal, wherein

said wiring is connected with a joint portion of said two protective thin film transistors;

each of said two protective thin film transistors has a p-type substrate potential fixing terminal and an n-type substrate potential fixing terminal connected with its channel layer;

said p-type and n-type substrate potential fixing terminals are connected with the ground terminal; and

the breakdown voltage and the hold voltage of said protective thin film transistor are respectively made lower than those of said primary stage thin film transistor or a thin film transistor used as a switching element for driving the pixel.

10. A liquid crystal display device as claimed in claim 9,

said protected thin film transistor has the p-type and n-type substrate potential fixing terminals connected with the channel layer and connects said p-type and n-type substrate potential fixing terminals connected with a substrate bias generation circuit.

11. A protective circuit formed from a protective thin film transistor connected with the input circuit of a protected thin film transistor, comprising:

a p-type and an n-type substrate potential fixing terminals provided in the channel layer of said protective thin film transistor; and

a ground terminal connected with said p-type and n-type substrate potential fixing terminals,

wherein a breakdown voltage and a hold voltage of said protective thin film transistor are made respectively lower than those of said protected thin film transistor or of a thin film transistor used as a switching element for driving a pixel.

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