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(54) **LIQUID CRYSTAL DRIVE CIRCUIT AND LIQUID CRYSTAL DISPLAY DEVICE**

(76) Inventors: **Yasuyuki Kudo**, Kamakura (JP);
Yoshikazu Yokota, Kodaira (JP);
Kazunari Kurokawa, Mobara (JP);
Atsushiro Higa, Yokohama (JP)

Correspondence Address:
**ANTONELLI, TERRY, STOUT & KRAUS,
LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889 (US)**

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(57) **ABSTRACT**

A matrix type liquid crystal display device has a function of suppressing power consumption without calling for an extra circuit arrangement such as the arrangement of storage capacitance and wiring to storage capacitance and without disposing new external components. A switch is disposed in the liquid crystal display device to temporarily short-circuit both column electrodes and common electrodes sandwiching a liquid crystal between them in synchronism with an alternation timing.

FIG. 1

A VOLTAGE ⊕   A ELECTRODE

⊕ LIQUID
⊖ CRYSTAL

B VOLTAGE ⊖   B ELECTRODE

⊕→⊖

0

⊖→⊕

⊖

⊖
⊕

⊕

⊖→⊕

0

⊕→⊖

FIG. 2

GRAPHIC CONTROLLER

VSYNC
HSYNC
DTMG
DCLK
DATA

~210

VCC GND

~201

~203

TIMING
CONTROL

COLUMN ELECTRODE DRIVER

202

VX1 VX2 VX3   VXN

COMMON
ELECTRODE
DRIVER

ROW ELECTRODE DRIVER

VY1 ---- P11

VY2 ---- P12

VY3

204

POWER
SOURCE

~207

206

VYM

205

VCOM

LIQUID
CRYSTAL
CELL

HOLDING
CAPACITANCE

SWITCH
DEVICE
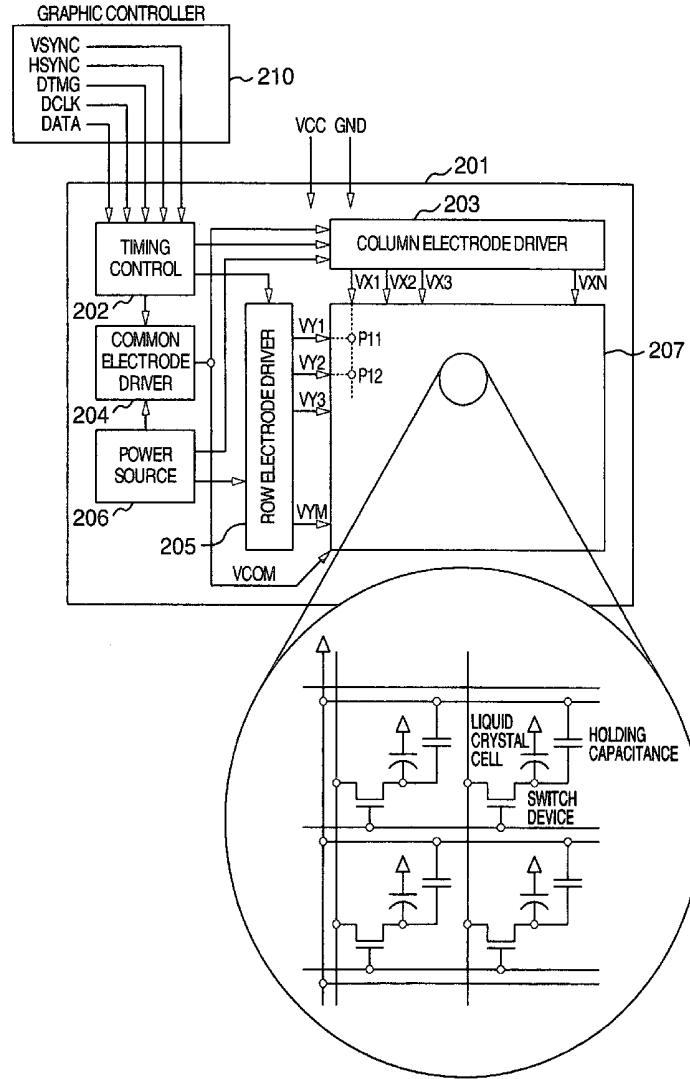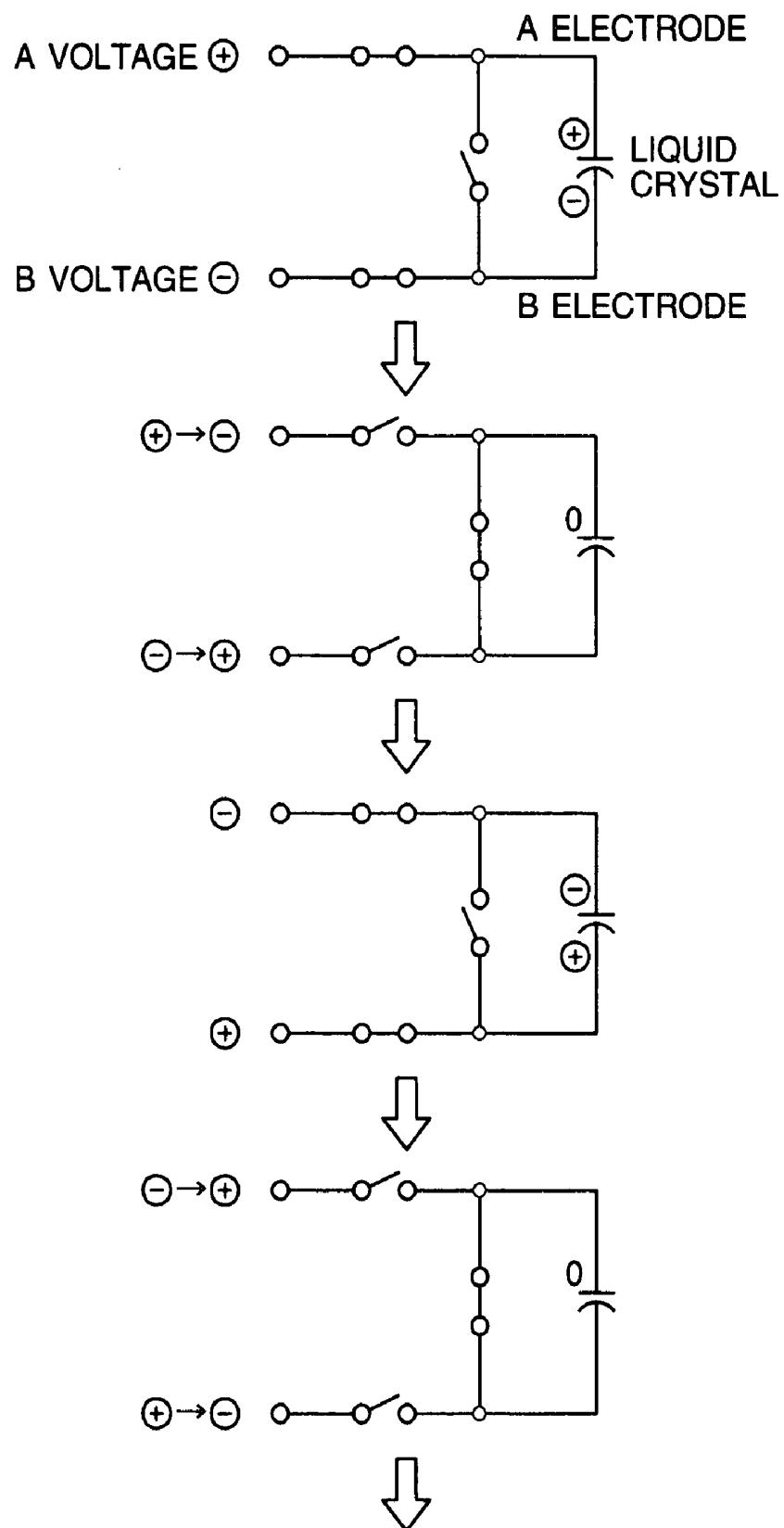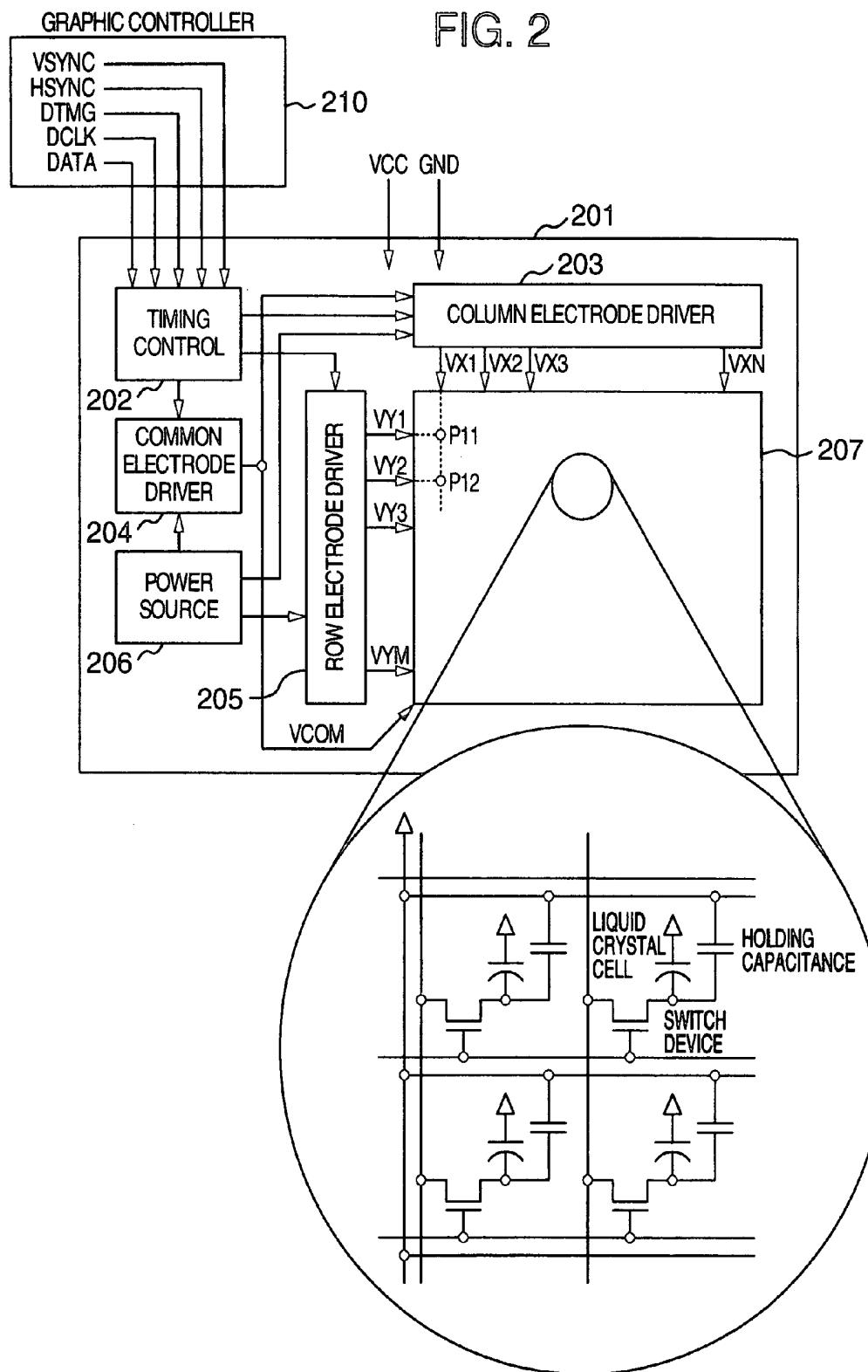
FIG. 3
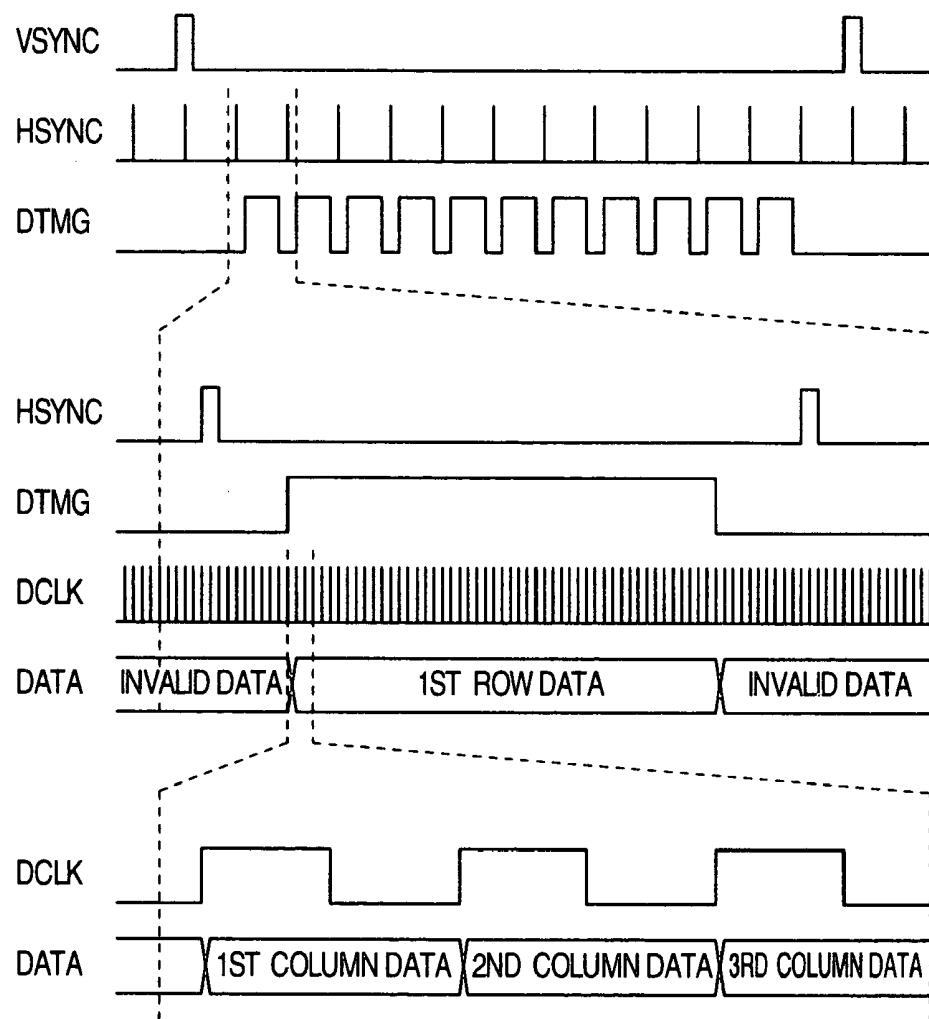
FIG. 4
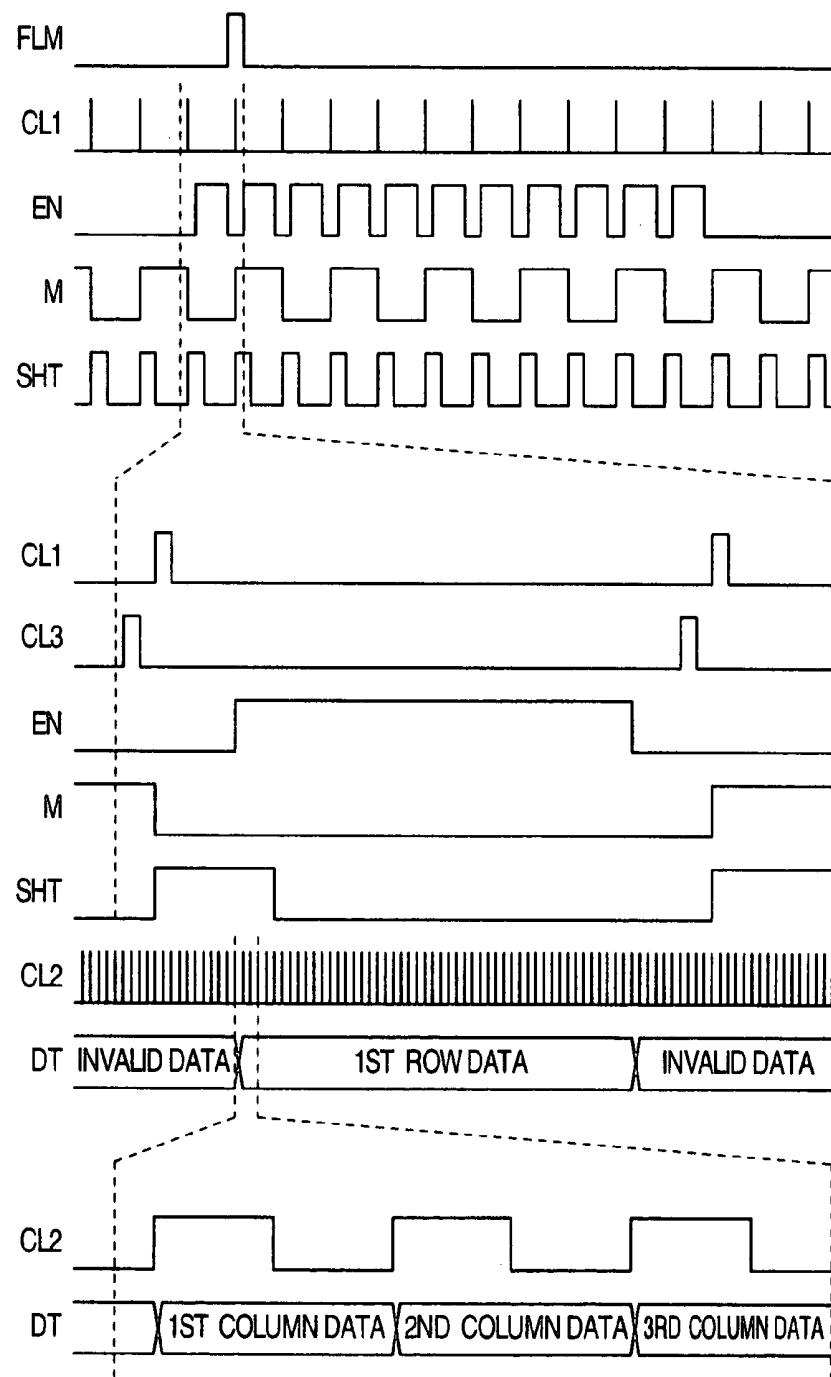
FIG. 5
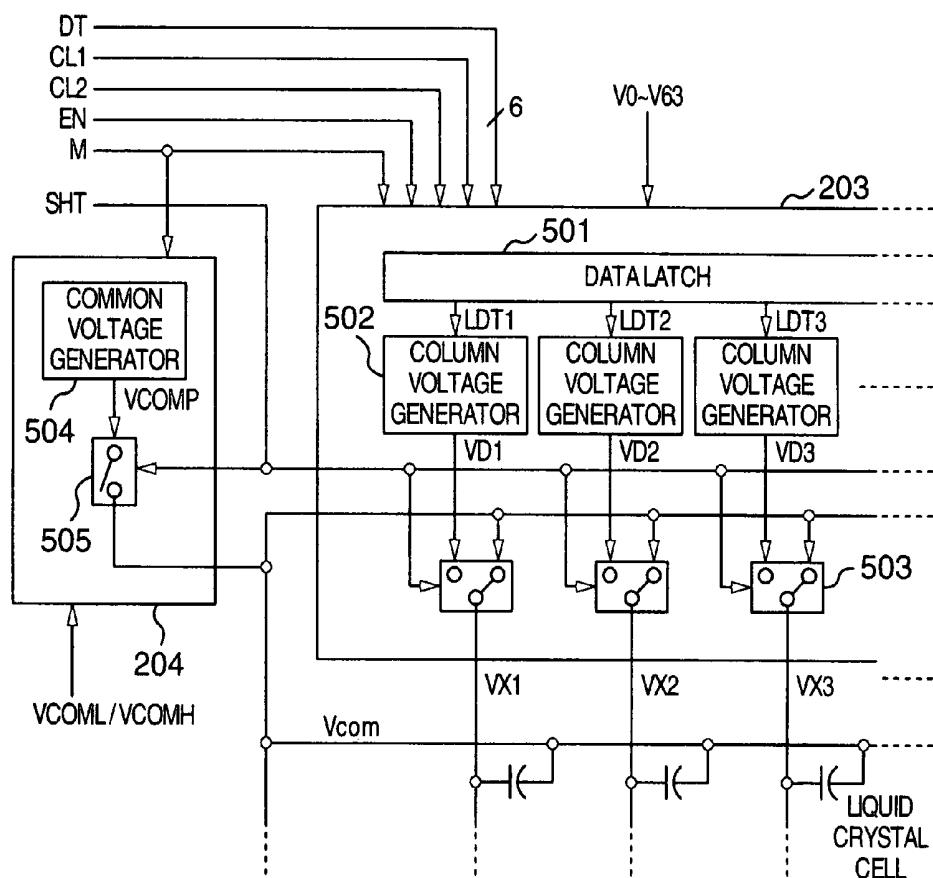
FIG. 6

LDATA	M	VD	
		NW MODE LIQUID CRYSTAL	NB MODE LIQUID CRYSTAL
BLACK 0 0 0 0 0 0	HIGH	LOW POTENTIAL V0	HIGH POTENTIAL V63
0 0 0 0 0 1		V1	V62
0 0 0 0 1 0		V2	V61
0 0 0 0 1 1		V3	V60
0 0 0 1 0 0		V4	V59
0 0 0 1 0 1		V5	V58
0 0 0 1 1 0		V6	V57
1 1 1 1 0 1		V61	V2
1 1 1 1 1 0		V62	V1
WHITE 1 1 1 1 1 1		HIGH POTENTIAL V63	LOW POTENTIAL V0
BLACK 0 0 0 0 0 0	LOW	HIGH POTENTIAL V63	LOW POTENTIAL V0
0 0 0 0 0 1		V62	V1
0 0 0 0 1 0		V61	V2
0 0 0 0 1 1		V60	V3
0 0 0 1 0 0		V59	V4
0 0 0 1 0 1		V58	V5
0 0 0 1 1 0		V57	V6
1 1 1 1 0 1		V2	V61
1 1 1 1 1 0		V1	V62
WHITE 1 1 1 1 1 1		LOW POTENTIAL V0	HIGH POTENTIAL V63

NW MODE LIQUID CRYSTAL :
LIQUID CRYSTAL DISPLAYING WHITE AT NON-APPLICATION OF VOLTAGE
NB MODE LIQUID CRYSTAL :
LIQUID CRYSTAL DISPLAYING BLACK AT NON-APPLICATION OF VOLTAGE

FIG. 7
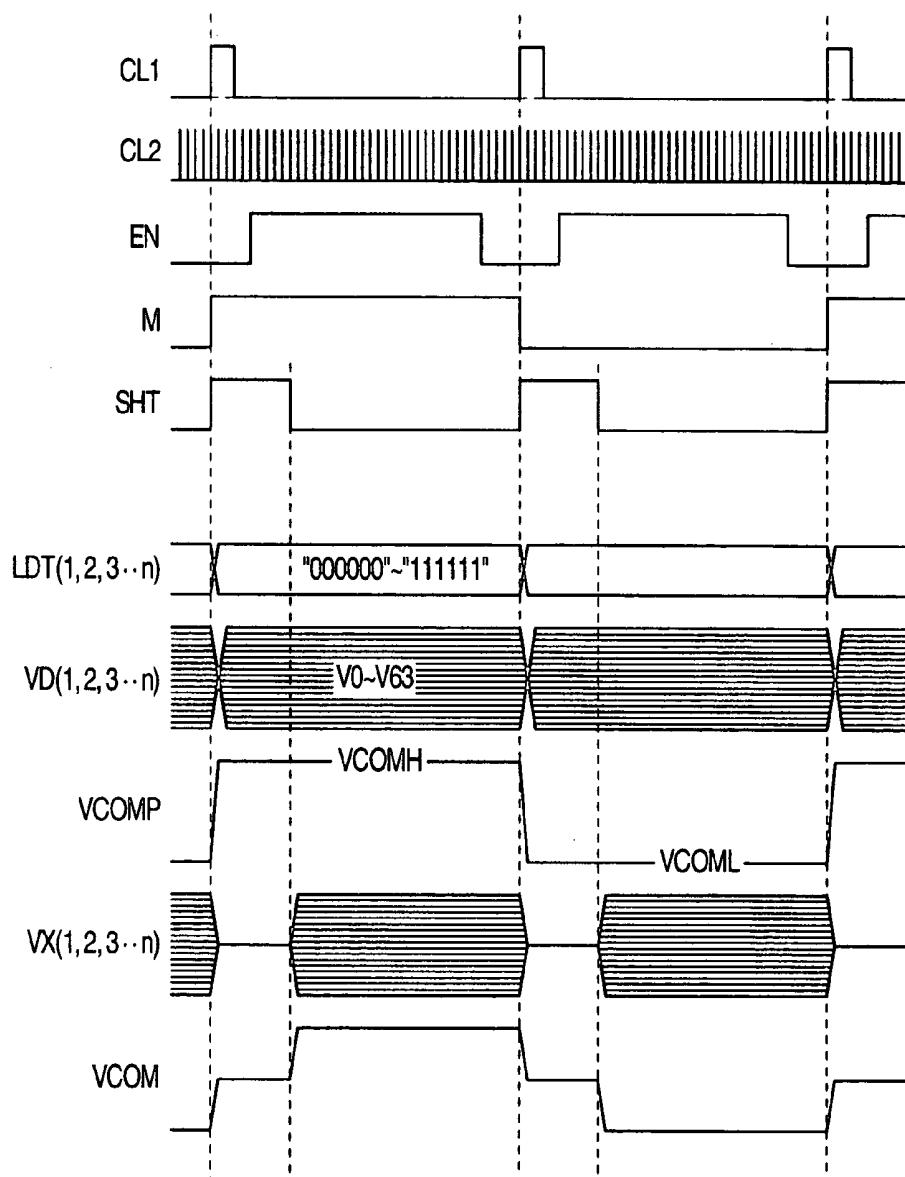
FIG. 8
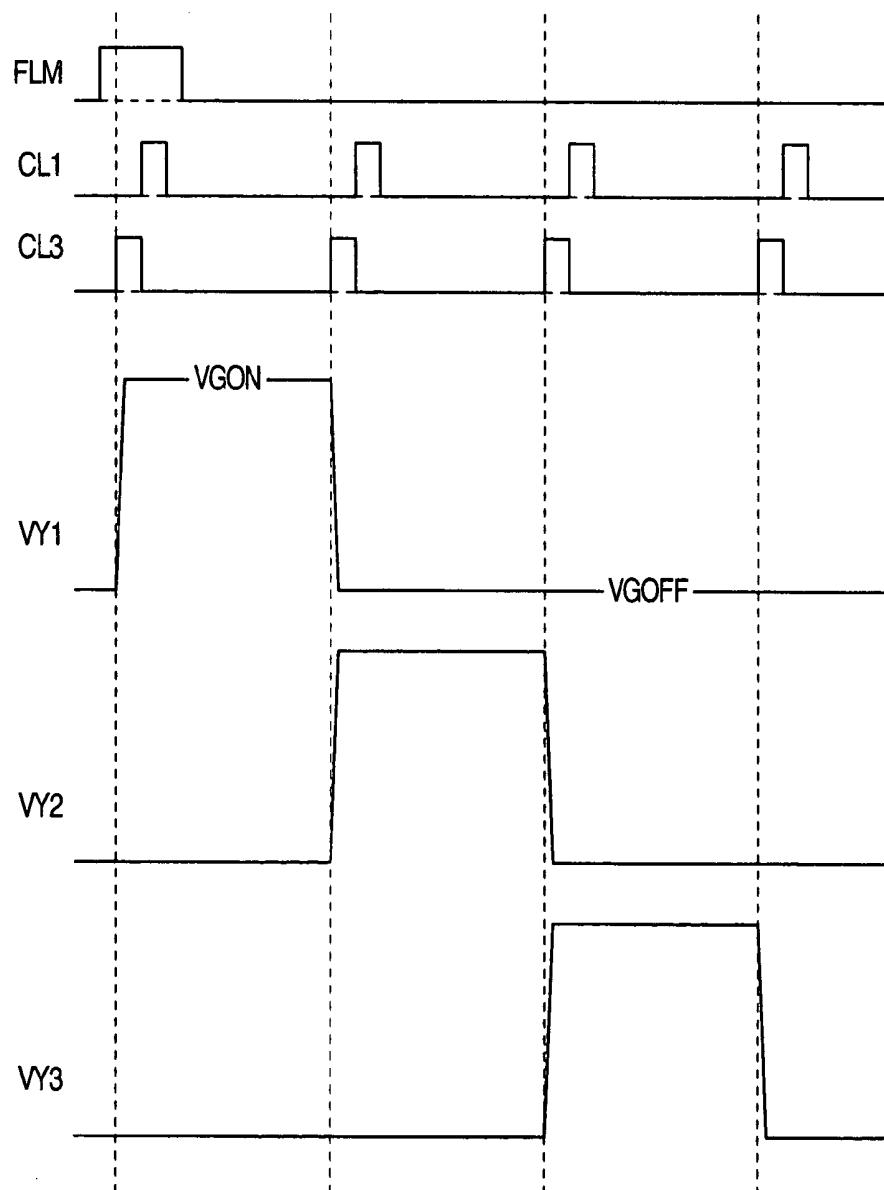
FIG. 9
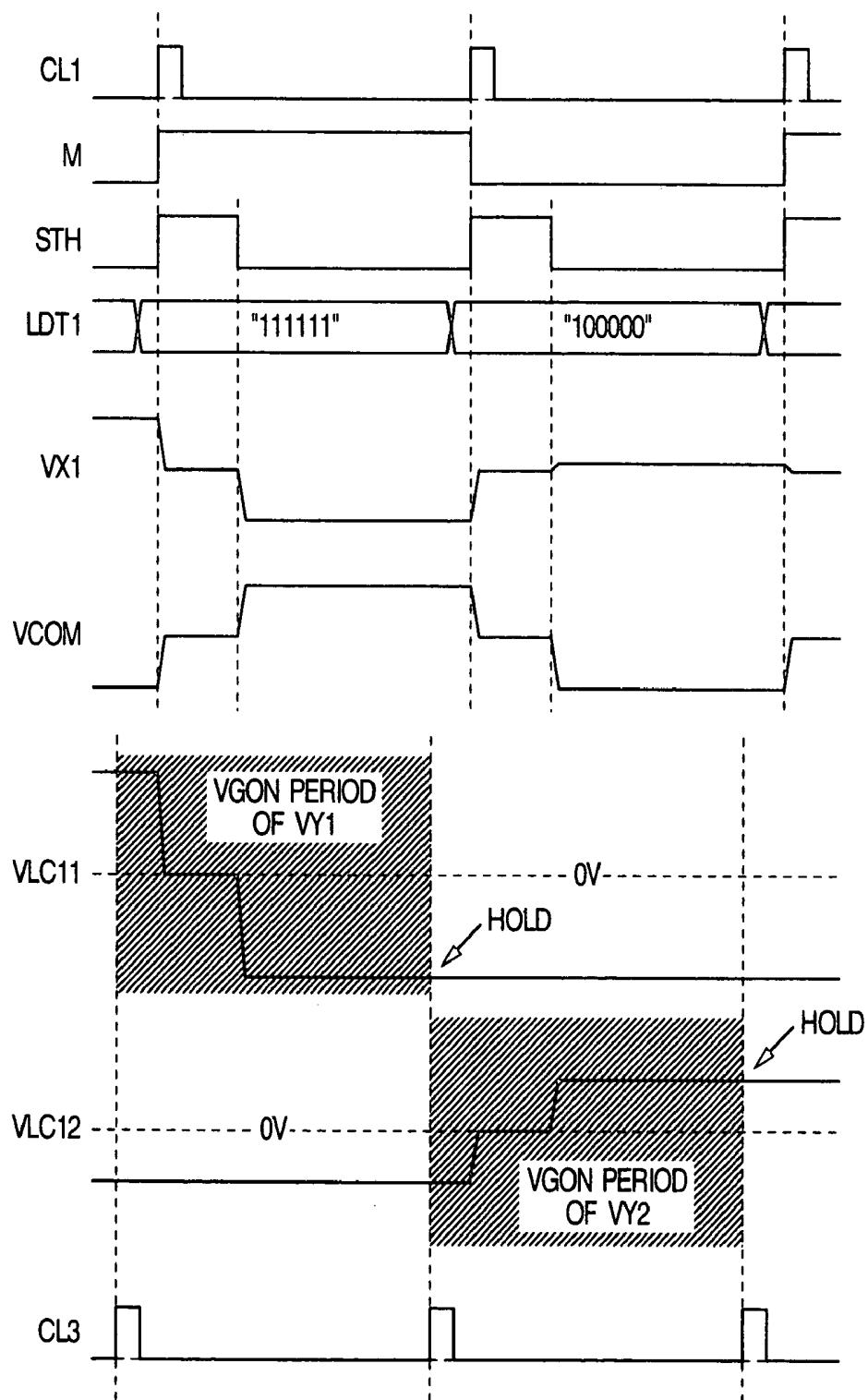
FIG. 10
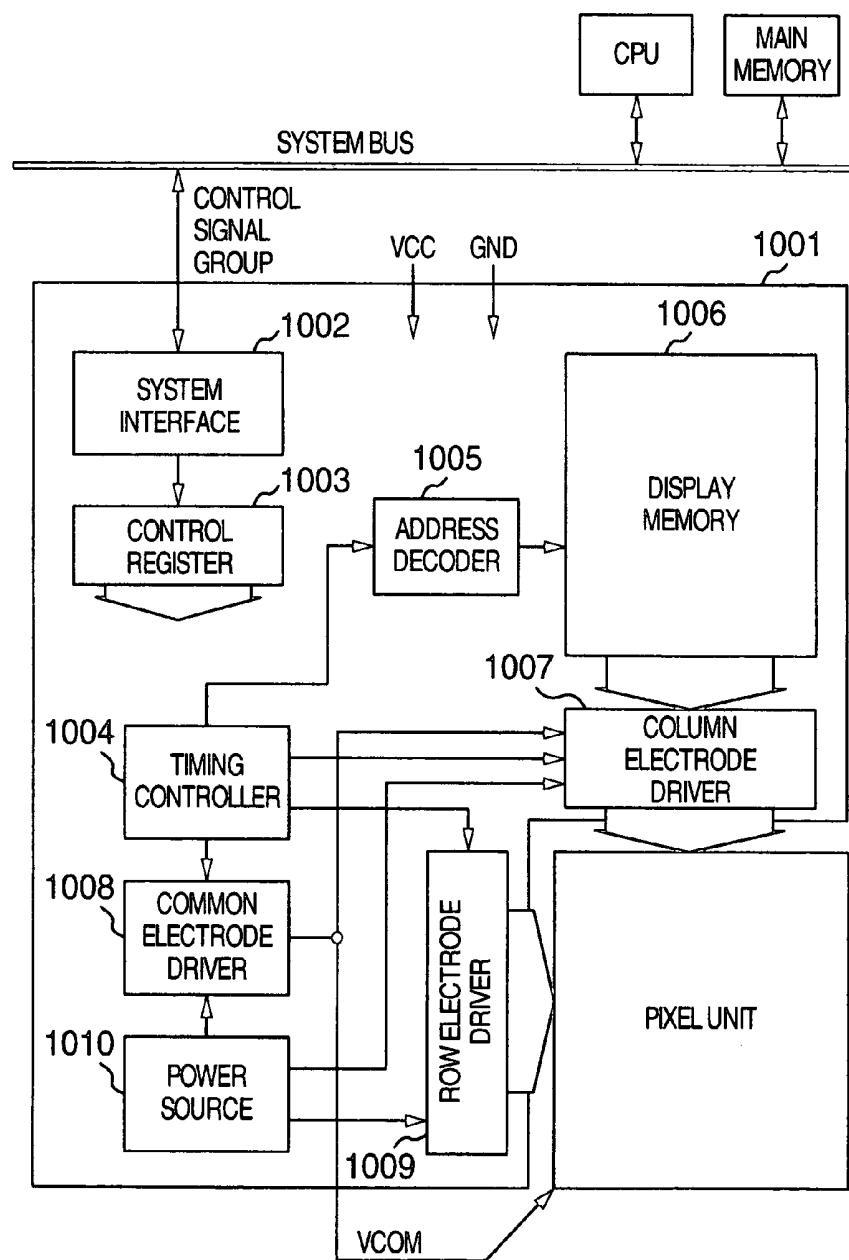
FIG. 11

SIGNAL NAME	MEANING	"Low"	"High"
CS	CHIP SELECTION	ACCESSIBLE	NOT ACCESSIBLE
RS	REGISTER ADDRESS / DATA SELECTION	ADDRESS	DATA
E	ENABLING OF DATA WRITE / READ	DISABLE	ENABLE
RW	SELECTION OF DATA WRITE / READ	WRITE	READ
D	BI-DIRECTIONAL DATA	–	–

FIG. 12

FIG. 13

FIG. 14

FIG. 15

FLM

CL3

SHTR

1501

1504

VGON

VGOFF

R1

SR1

1502

1503

ROW SELECTOR

SWITCH CONTROLLER

R2

SR2

VY1

VY2

R3

SR3

VY3

R4

SR4

VY4

FIG. 16

FLM

CL1

CL3

SHTR

R2

GND

SR2

VY2

GND

FIG. 17

LIQUID
CRYSTAL
CELL

HOLDING
CAPACITANCE

FIG. 18

FIG. 19

CL1

CL3

SHT

VCOM

VY

DIFFERENT
POTENTIAL
RELATIONSHIP

FIG. 20

CL1

CL3

SHT

VCOM

Hi-Z

VY   Hi-Z   Hi-Z   Hi-Z
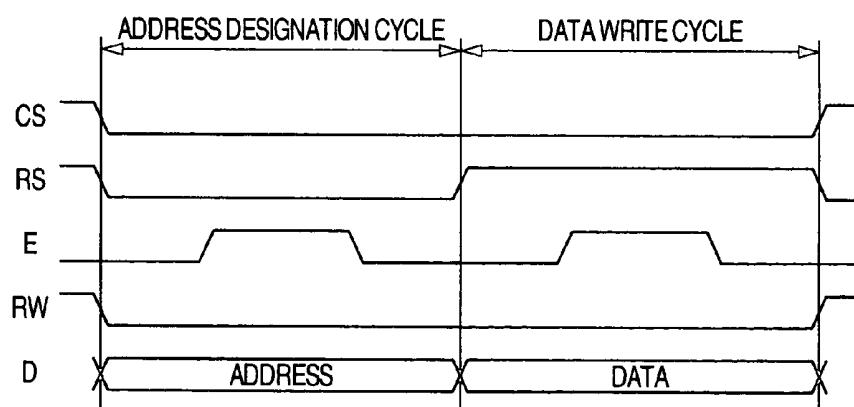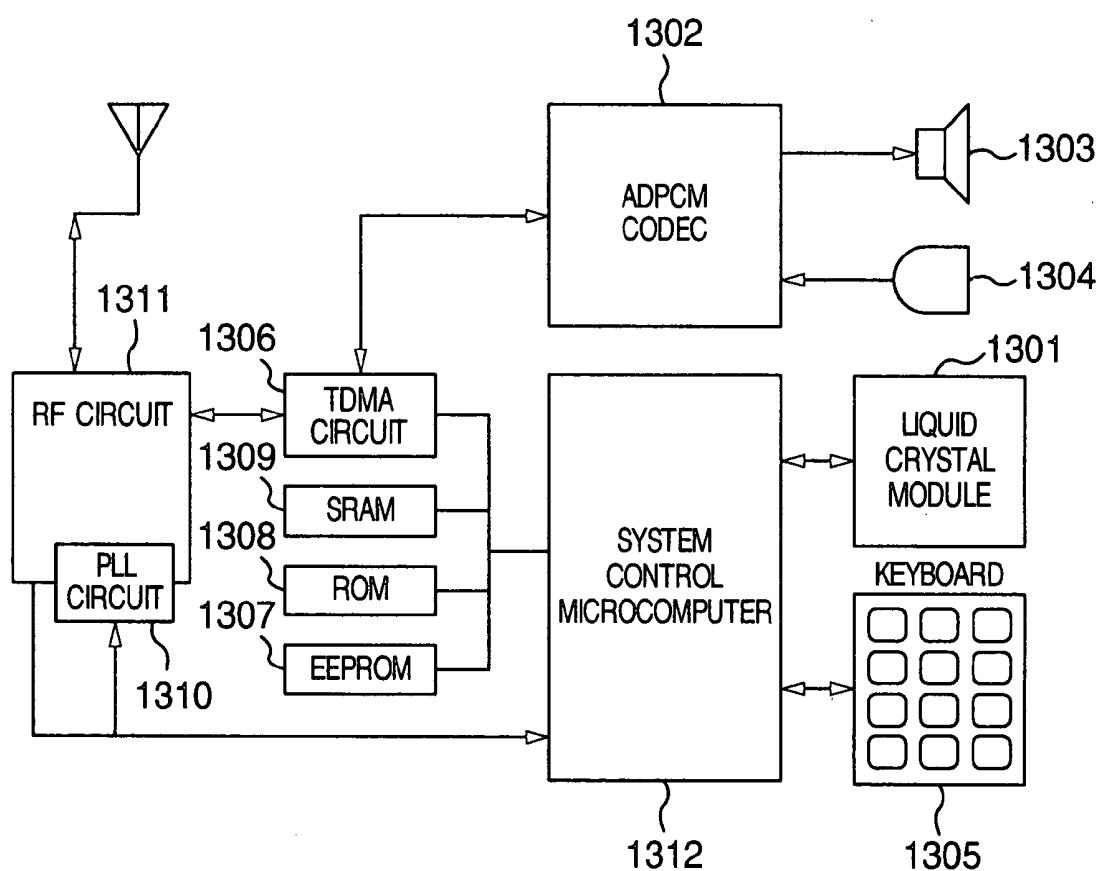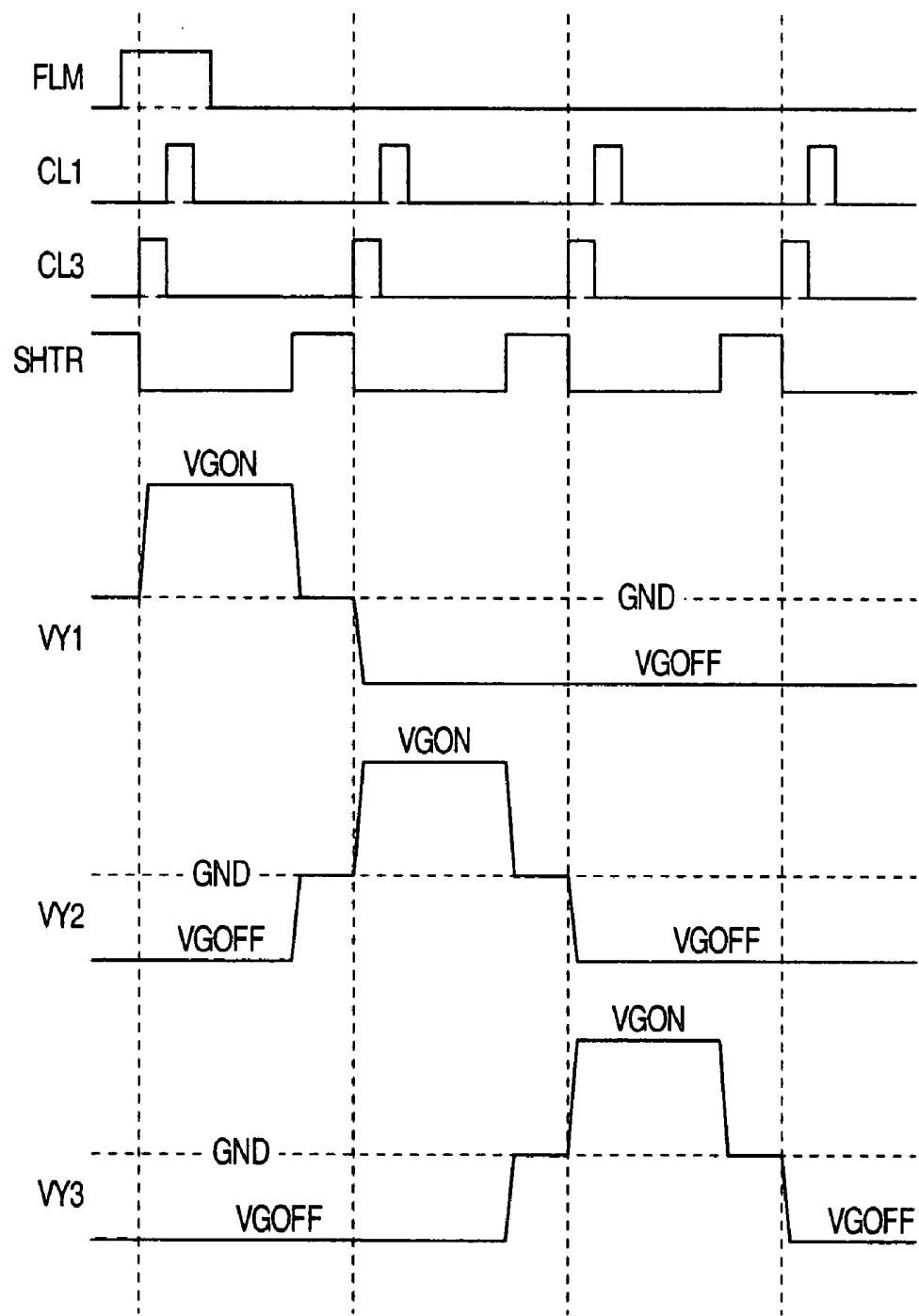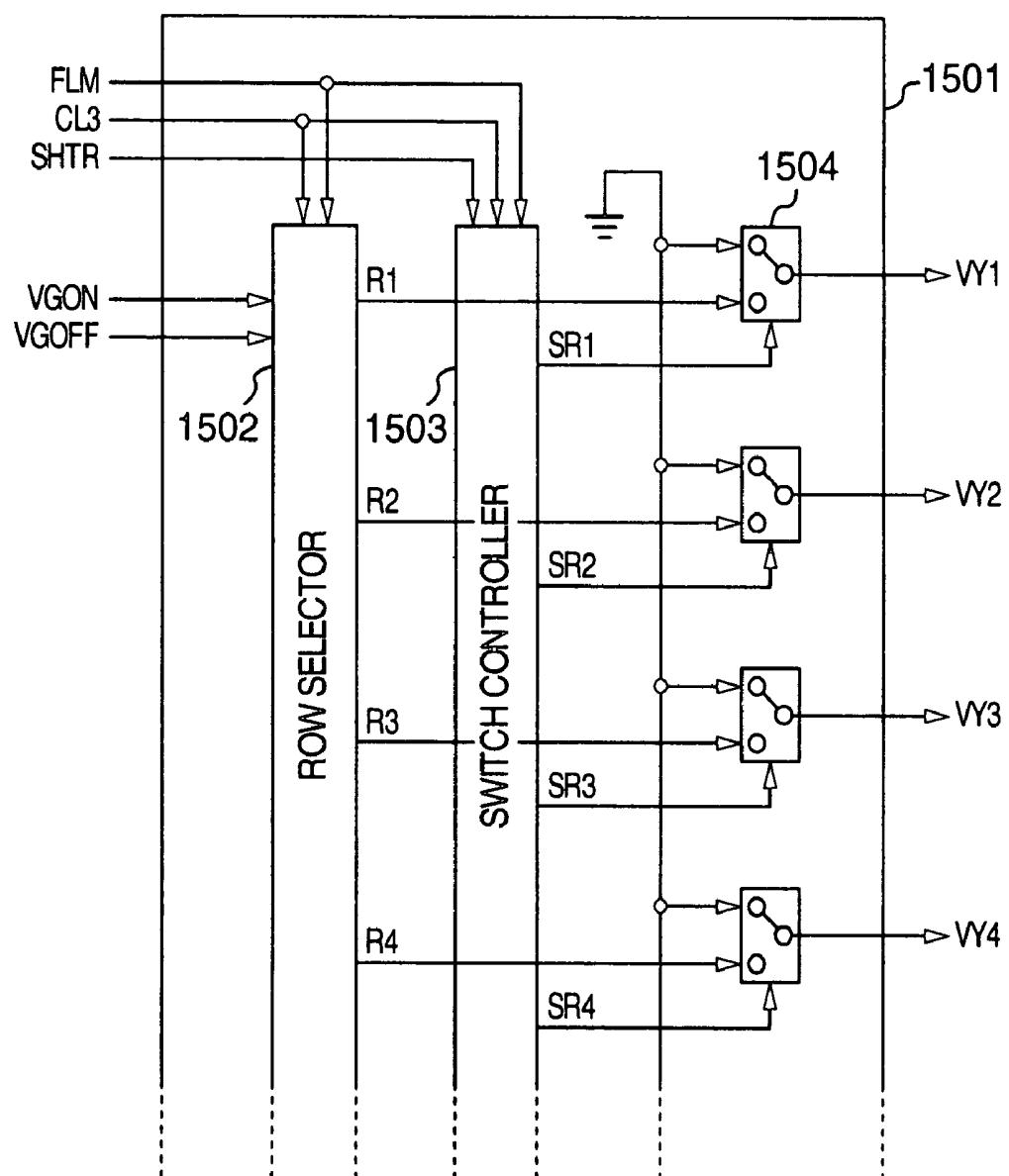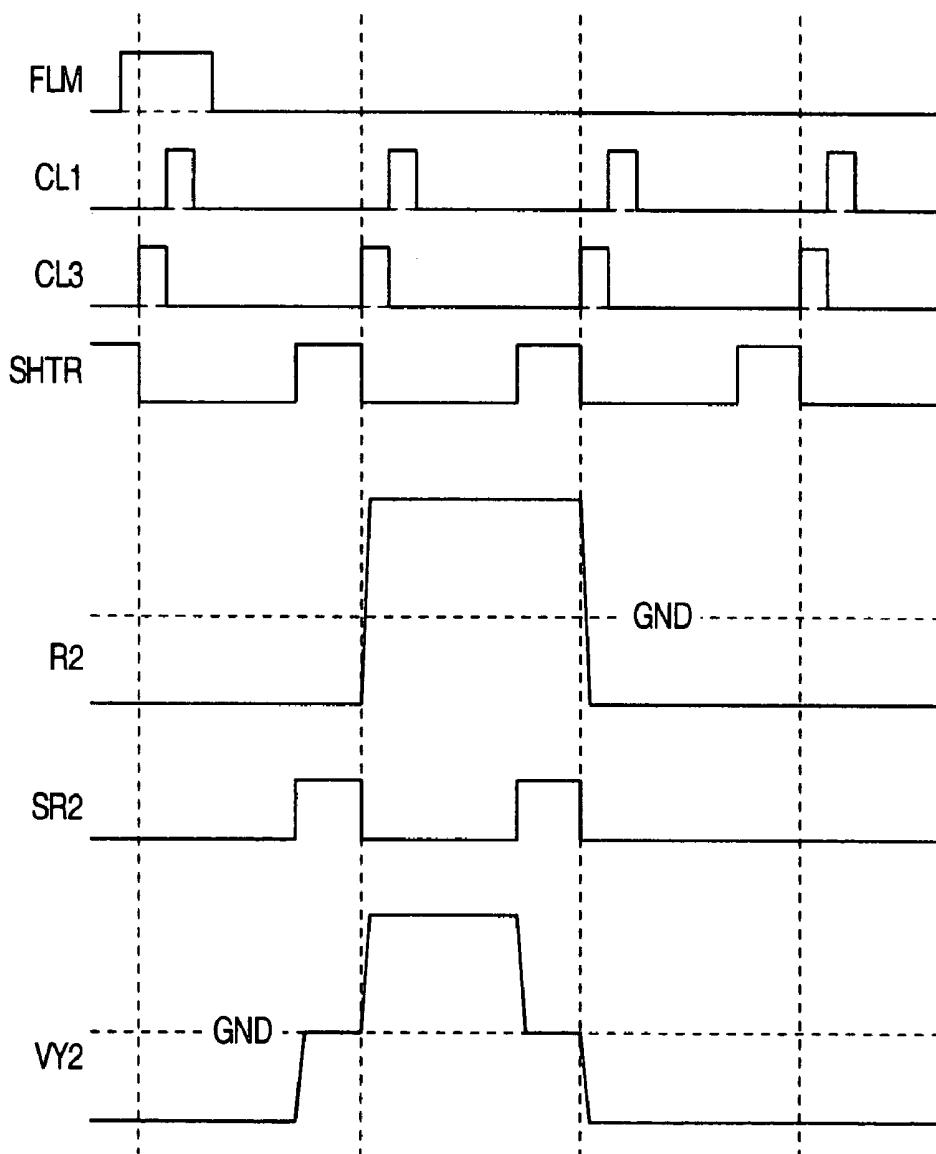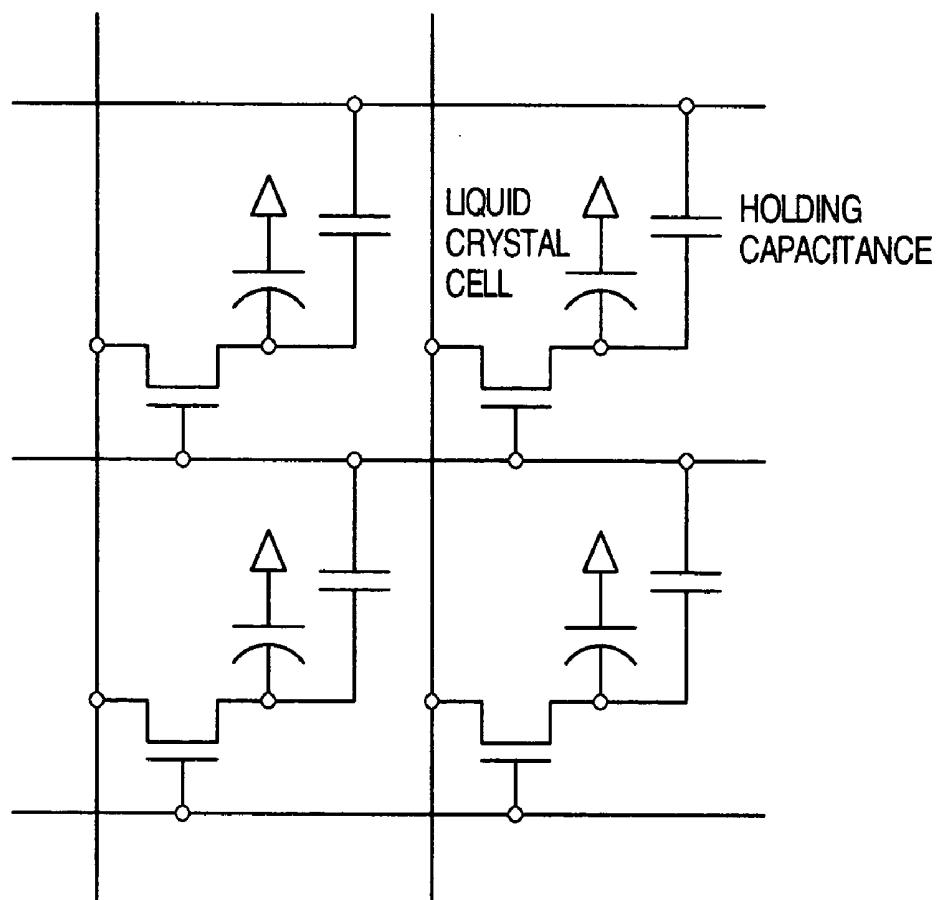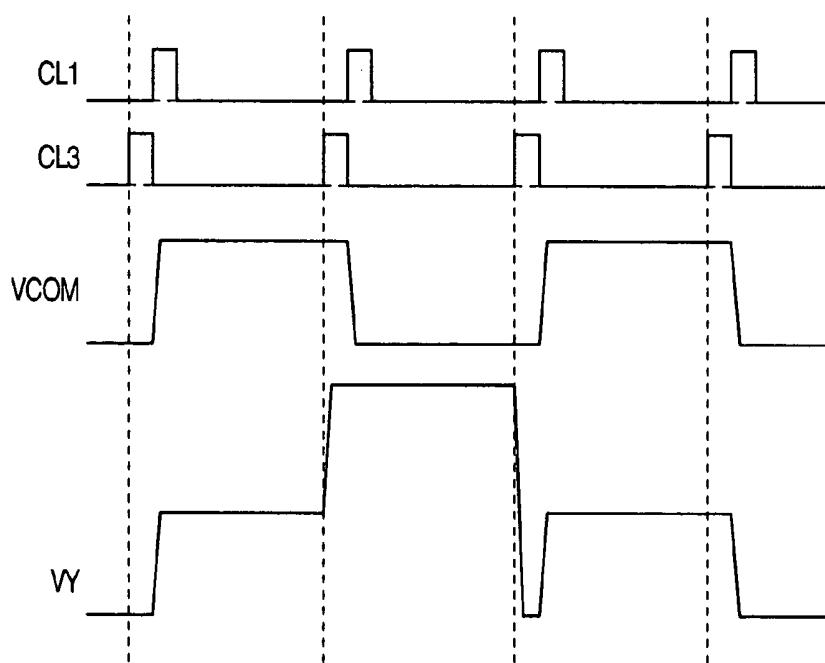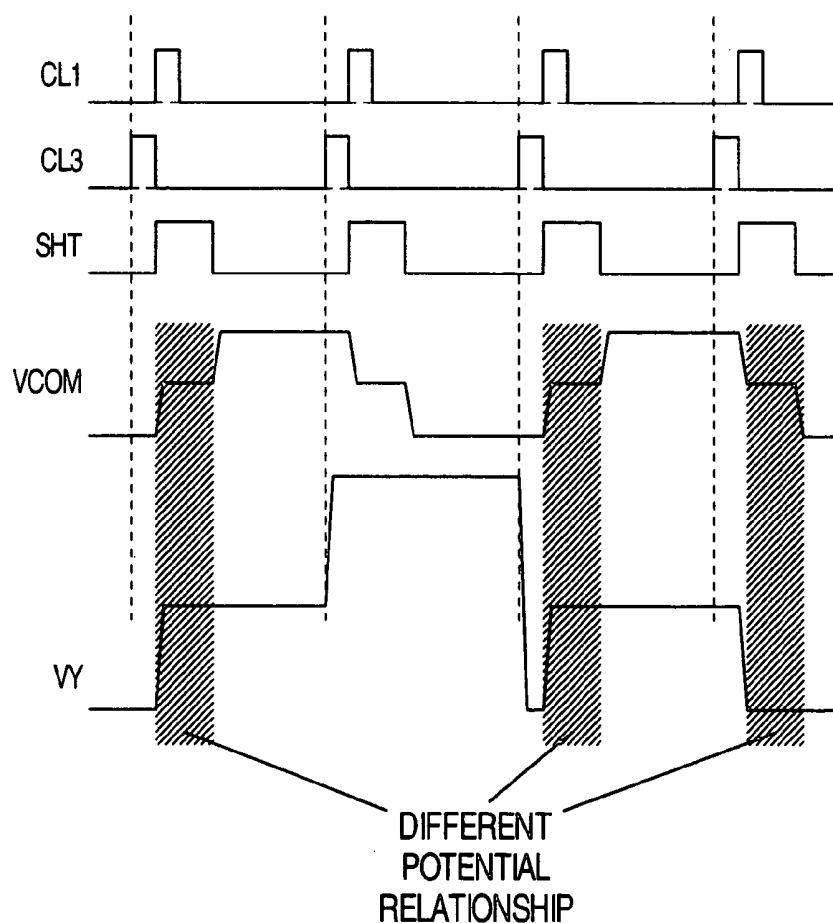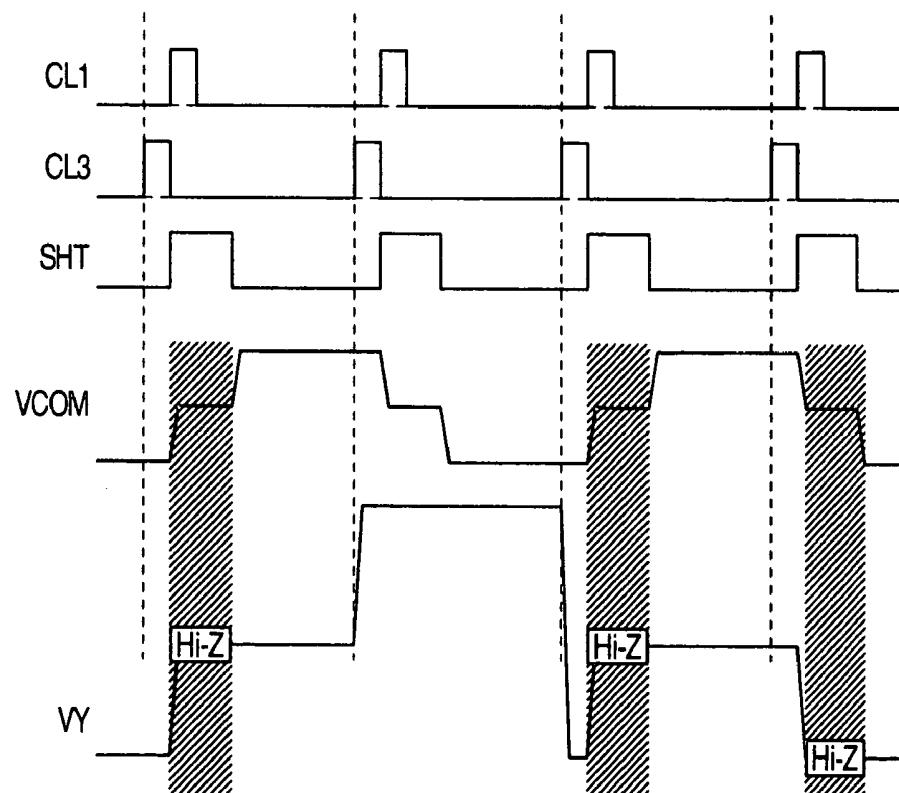
FIG. 21
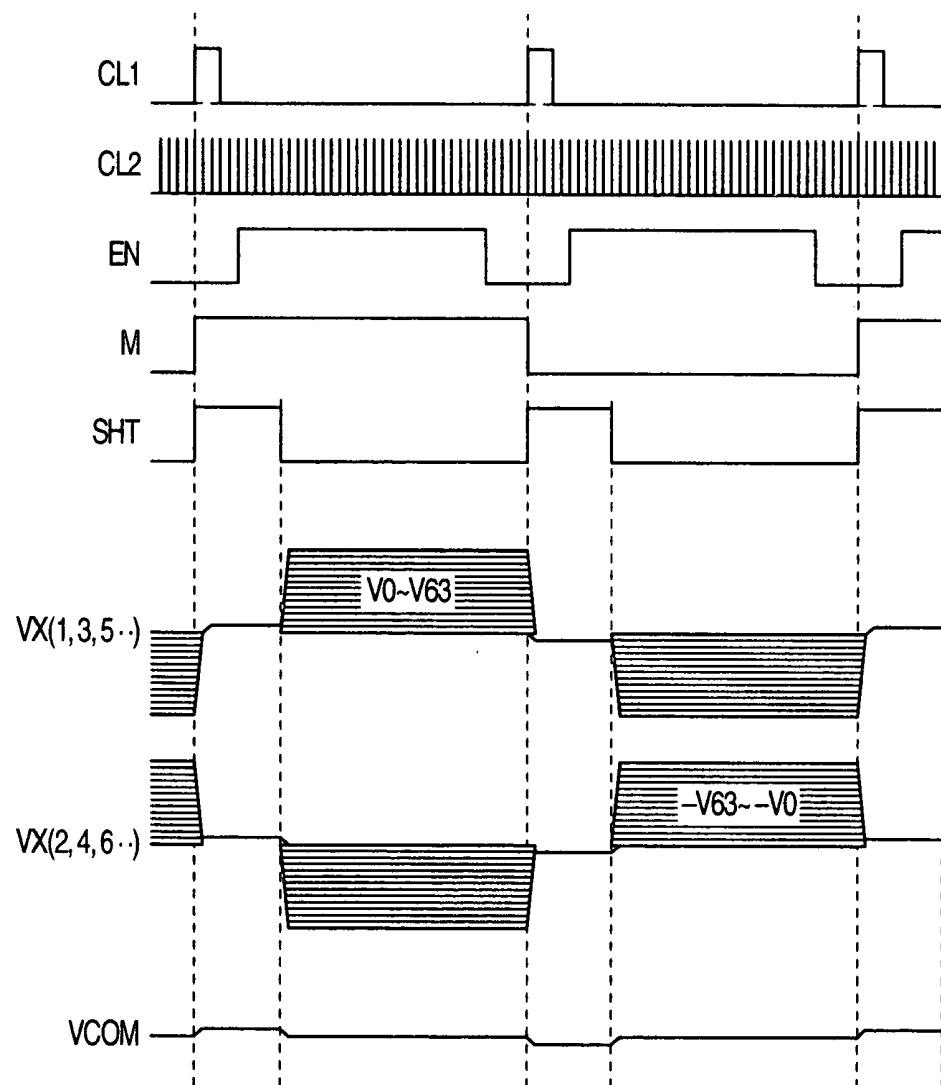
LIQUID CRYSTAL DRIVE CIRCUIT AND LIQUID CRYSTAL DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Ser. No. 09/930,311 filed on Aug. 16, 2001. The contents of application Ser. No. 09/930,311 are hereby incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] This invention relates to a technology for achieving lower power consumption in an active matrix type liquid crystal display device.

[0003] To prevent degradation of a liquid crystal, a matrix type liquid crystal display device for controlling a transmission factor (brightness) of each pixel at an effective value of an applied voltage has to employ so-called "alternation" in which the polarity of the applied voltage to the liquid crystal is inversed in a predetermined cycle. Since the liquid crystal is made of a dielectric in this instance, charging and discharging of the liquid crystal consume power in the alternation process described above.

[0004] U.S. Pat. No. 5,852,426 describes a method of reducing this power consumption. In this method, a switch is provided to change connection of liquid crystal driving electrodes to a liquid crystal driver circuit or to external storage capacitance. The switch selects the external storage capacitance in the first period of one scanning cycle and the liquid crystal driver circuit in the second period. When the external storage capacitance is sufficiently large, the driving voltage can be shifted to a substantial midpoint of the AC amplitude in the first period without consuming power. In consequence, power consumption can be reduced much more than when no means is employed.

[0005] U.S. Pat. No. 5,852,426 needs disposition of the storage capacitance outside the liquid crystal driver circuit. Therefore, to employ this method, a new circuit board design such as the arrangement of the storage capacitance and wiring to the storage capacitance becomes necessary, and the number of components increases, as well.

SUMMARY OF THE INVENTION

[0006] It is an object of the present invention to provide a matrix type liquid crystal display device, and a driving method thereof, that can save power consumption resulting from alternation without disposing any component such as the storage capacitance outside the liquid crystal driver circuit.

[0007] The present invention for solving the problem described above is based on the concept that a charge stored in a liquid crystal can be initialized to 0 (or substantially 0) when an A electrode and a B electrode sandwiching a liquid crystal between them are temporarily short-circuited at a timing of alternation as shown in **FIG. 1**. In other words, the sequence having this short-circuit can shift the voltage to a substantial midpoint of alternation amplitude without consuming power. This means that the power-saving effect can be obtained the same way as in U.S. Pat. No. 5,852,426 without involving the disposition of external components.

[0008] The liquid crystal display controller and the liquid crystal display device according to the present invention based on this concept provide switch means for temporarily short-circuiting both of column electrodes and common electrodes sandwiching a liquid crystal in synchronism with the timing of alternation to these electrodes. The present invention includes means for setting a charge stored in the liquid crystal to or below a predetermined value in synchronism with the timing of alternation. The predetermined value includes 0 (or substantially 0).

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **FIG. 1** is a circuit model of a liquid crystal that represents the concept of the present invention;

[0010] **FIG. 2** is a block diagram showing a construction of a liquid crystal display device according to a first embodiment of the present invention;

[0011] **FIG. 3** is a timing chart showing input signals for timing control in the first embodiment of the present invention;

[0012] **FIG. 4** is a timing chart showing output signals for timing control in the first embodiment of the present invention;

[0013] **FIG. 5** is a block diagram showing a column electrode driver unit and a common electrode driver unit in the first embodiment of the present invention;

[0014] **FIG. 6** is a table useful for explaining the operation of a column voltage generation unit in the first embodiment of the present invention;

[0015] **FIG. 7** is a timing chart showing operations of the column electrode driver unit and the common electrode driver unit in the first embodiment of the present invention;

[0016] **FIG. 8** is a timing chart showing the operation of a row electrode driver unit in the first embodiment of the present invention;

[0017] **FIG. 9** is a timing chart showing a liquid crystal applied voltage in the first embodiment of the present invention;

[0018] **FIG. 10** is a block diagram showing a construction of a liquid crystal display controller according to a second embodiment of the present invention;

[0019] **FIG. 11** is an explanatory view of input signals of a system interface in the second embodiment of the present invention;

[0020] **FIG. 12** is a timing chart showing the operation of the input signals of the system interface in the second embodiment of the present invention;

[0021] **FIG. 13** is a block diagram showing a construction of a cellular telephone set in the second embodiment of the present invention;

[0022] **FIG. 14** is a timing chart showing the operation of a liquid crystal display device according to a third embodiment of the present invention;

[0023] **FIG. 15** is a block diagram showing a construction of a row electrode driver unit in the third embodiment of the present invention;

[0024] FIG. 16 is a timing chart showing the operation of the row electrode driver unit in the third embodiment of the present invention;

[0025] FIG. 17 shows a circuit model that represents a structure of pixels in a fourth embodiment of the present invention;

[0026] FIG. 18 is a timing chart showing an applied voltage to a pixel unit in the fourth embodiment of the present invention;

[0027] FIG. 19 is a timing chart showing the applied voltage to the pixel unit in the fourth embodiment of the present invention;

[0028] FIG. 20 is a timing chart showing the operation of a row electrode driver unit in the fourth embodiment of the present invention; and

[0029] FIG. 21 is a timing chart showing an operation of a liquid crystal display device according to a fifth embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[0030] Initially, the first embodiment of the present invention will be explained with reference to FIGS. 2 to 9. FIG. 2 shows a construction of a liquid crystal display device according to a first embodiment of the present invention. Referring to FIG. 2, reference numeral 201 denotes the liquid crystal display device according to the present invention. Numeral 202 denotes a timing control unit. Numeral 203 denotes a column electrode driver unit. Numeral 204 denotes a common electrode driver unit. Numeral 205 denotes a column electrode driver unit. A 3-terminal switch device, a liquid crystal cell and a holding capacitance are arranged at a position corresponding to each pixel of a pixel unit 207. A drain terminal of the switch device is connected to a column electrode. Its gate terminal is connected to a row electrode and its source terminal, to the liquid crystal cell and the holding capacitance. The other terminal of the liquid crystal cell is connected to a common opposing electrode. The other terminal of the holding capacitance is connected to a common storage electrode. A common electrode driver unit 204 drives both of them. To achieve this connection, the column electrode, the row electrode and the storage electrode are formed in a matrix shape on the inner surface of one of the two transparent substrates that sandwich the liquid crystal between them. The common electrode is formed in a mat shape on the inner surface of the other transparent electrode.

[0031] Next, the operation of each block will be explained about the case where so-called "Vcom modulation drive", in which the applied voltage to the common electrode is allowed to modulate, is conducted by way of example on the assumption that the liquid crystal display device 201 is scanned by a line sequential scanning system.

[0032] First, the timing control unit 202 receives a group of standard image input signals in a matrix type liquid crystal using a switch device (hereinafter called merely the "active matrix type liquid crystal") from an external graphic controller 210. FIG. 3 shows a timing chart of the signal group. From the signal group FLM, the timing control unit 202 generates FLM representing a scanning start timing of a front scanning line, CL1 representing a voltage application

start timing to the column electrode and to the common electrode, EN representing a transfer period of effective display data for one scanning line, M representing the polarity of alternation, SHT representing an execution timing of short-circuiting, CL3 representing a voltage application start timing to the row electrode, CL2 representing a transfer clock of display data of each column in one scanning line and DT representing display data for one scanning line. The timing control unit 202 outputs these signals to the column electrode driver unit 203, the common electrode driver unit 204 and the row electrode driver unit 205. In this embodiment, DT is assumed to have 64 gray-scale information or 6 bits per pixel.

[0033] Next, FIG. 5 shows an internal construction of the column electrode driver unit 203 and the common electrode driver unit 204. In FIG. 5, reference numeral 501 denotes a data latch circuit. Numeral 502 denotes a column voltage generation circuit. Numeral 503 denotes a short-circuit switch A. Numeral 504 denotes a common voltage generation circuit. Numeral 505 denotes a short-circuit switch B. Inputs of the column electrode driver unit 203 are DATA, CL1, CL2, EN, M, SHT and column voltages V0 to V63 corresponding to 64 gray scales. Inputs of the common electrode driver unit 204 are M and VCOMH and VCOML (two kinds of voltage are necessary for alternation) as reference voltages of the common voltage. Incidentally, a power source circuit 206 generates the voltage level of each of V0 to V63, VCOMH and VCOML on the basis of a VCC voltage inputted from outside. The mutual relation of each voltage level has the same setting as that of ordinary Vcom modulation drive, and the voltage is set to an optimal value in accordance with applied voltage-v-transmission factor characteristics of the liquid crystal.

[0034] First, in the column electrode driver unit 203, the data latch circuit 501 stores DT for one row (one scanning line) in the High period of EN by use of CL2 and repeats the operation of outputting altogether the data stored as LDT1 to LDTn (hereinafter called generically "LDT") in synchronism with CL1. The column voltage generation circuit 502 selects one of the column voltages V0 to V63 corresponding to the gray scale of the pixel in accordance with LDT of each column and the signal M and outputs it as VD (generically representing one of VD1 to VDn). FIG. 6 shows an example of this selection operation.

[0035] The short-circuit switch A503 is a switch that selects either one of the terminal from the column voltage generation circuit 502 and the terminal from the common electrode in accordance with the signal SHT. It selects the common electrode when the signal SHT is High and the terminal of the column voltage generation circuit when the signal SHT is Low. The short-circuit switch A503 outputs VX (generically representing VX1 to VXn) to the respective column electrode.

[0036] Next, in the common electrode driver unit 204, the common voltage generation circuit 504 selects VCOMH when the input signal M is High and VCOML when the signal M is Low, and outputs the selected signal as VCOMP. The short-circuit switch B505 is a switch that selects whether or not the terminal from the common voltage generation circuit 504 is to be as such connected, in accordance with the signal SHT. The common voltage generation circuit 504 cuts off the connection when the signal SHT is

High, connects the terminal when the signal is Low, and outputs the signal as VCOM to the common electrode and to the storage electrode.

[0037] **FIG. 7** shows altogether the timing chart of the operations described above. As can be appreciated from **FIG. 7**, VX and VCOM are short-circuited and reach a certain equal potential level when SHT is High, are released from short-circuit when SHT falls thereafter to Low, and execute the ordinary driving operation. This is equal to the above-mentioned operation of saving power consumption.

[0038] Next, the operation of the row electrode driver portion **205** will be explained with reference to **FIGS. 2 and 8**. First, inputs of the row electrode driver unit **205** are FLM, CL3 and VGON and VGOF as the reference voltages of the row voltage. Incidentally, the power source circuit **206** generates VGON and VGOFF on the basis of the VCC voltage that is inputted from outside. VGON has a voltage level at which the gate of the transistor connected to the row electrode is turned ON and VGOFF has a voltage level at which the gate is turned OFF. As shown in the timing chart of **FIG. 8**, the row electrode driver unit **205** acquires High of FLM at the rise of CL3, sequentially shifts this FLM in synchronism with CL3 and outputs it as VY to the row electrode to sequentially shift the scanning line. This operation can be achieved by use of shift registers, for example.

[0039] In the liquid crystal display device shown in **FIG. 2**, for example, let's consider the liquid crystal applied voltages VLC11 and VLC12 at an intersection P11 where the column to which VX1 is applied intersects the row to which VY1 is applied, and at an intersection P12 where VX1 and VY2 intersect each other. It will be assumed hereby that the display data of P11 and P12 are (111111) and (100000) and the mode of the liquid crystal is the NB mode in **FIG. 6**.

[0040] **FIG. 9** shows the applied voltage waveforms of VLC11 and VLC12. As can be seen from **FIG. 9**, after a difference voltage between VCOM and VX1 is applied during the VGON period of VLC11 and VLC12, the voltages at the end of the VGON period are held. Since the voltages at this time have the voltage levels corresponding to the display data, display can be accomplished in the same way as ordinary Vcom modulation drive.

[0041] Incidentally, the switching period of M is one scanning cycle in this embodiment. However, the switching period is not particularly limited but may be a plurality of scanning cycles. In such a case, it is preferred that SHT outputs High and Low for only the first one scanning period after switching of M and remains Low in other periods.

[0042] Next, the second embodiment of the present invention will be explained with reference to FIGS. **10** to **13**. The second embodiment of the present invention represents an application example of the present invention to a liquid crystal display controller of a display memory built-in type. Referring to **FIG. 10**, reference numeral **1001** denotes a liquid crystal display controller. Numeral **1002** denotes a system interface. Numeral **1003** denotes a control register. Numeral **1004** denotes a timing generation unit. Numeral **1005** denotes an address decoder. Numeral **1006** denotes a display memory. Numeral **1007** denotes a column electrode driver unit. Numeral **1008** denotes a common electrode driver unit. Numeral **1009** denotes a row electrode driver unit. Numeral **1010** denotes a power source circuit. Numeral **1011** denotes a pixel unit comprising a plurality of pixels that are arranged in matrix.

[0043] First, the interface of the liquid crystal display controller is based on a so-called "MPU6800 Series" bus interface, for example. As shown in **FIG. 11**, CS representing chip selection, RS for selecting the address/data of the control register, E designating the enabling of the operation, RW for selecting write/read of the data and D as the actual value of the address/data are given as signals through a system bus. These control signals have a cycle for designating the address of the control register and a cycle for writing the data. The operations of the control signals in these cycles will be explained with reference to **FIG. 12**. In the address designation cycle, CS is set to "Low", RS, to "Low", RW, to "Low" and D, to a predetermined address value. Thereafter, E is set to "High" for a predetermined period. In the data write cycle, on the other hand, CS is set to "Low", RS, to "High", RW, to "Low" and D, to a desired data. Thereafter, E is set to "High" for a predetermined period. Incidentally, these operations are programmed in advance by an operating system and application software for controlling the overall apparatus.

[0044] The system interface **1002** is the portion that decodes the control signals described above. The system interface **1002** outputs the signal for bringing the corresponding address into the write state in the address designation cycle to the control register **1003** and a data to be written in the data write cycle to the control register **1003**.

[0045] The control register **1003** brings the register having the designated address into the write state and stores the data in this register. Incidentally, the data to be written into the control register **1003** are various driving parameters such as resolution of the liquid crystal panel, the display data and the display position data. These data are written to separate addresses, respectively. The driving parameters stored in the control registers **1003** are outputted to each block, and the display data is outputted to the display memory **1006**.

[0046] The timing generation unit **1004** is a portion that generates by itself the timing signal group on the basis of the driving parameters given from the control register **1003**, and its content is substantially equal to the timing signal group shown in **FIG. 4**. At the same time, the timing generation unit **1004** generates a read address of the display memory and outputs it to the address decoder **1005**.

[0047] The address decoder **1005** decodes the display position data given from the control register **1003** at the time of write of the display data and selects the bit line and the word line inside the corresponding display memory **1006**. The address decoder **1005** then outputs the display data given from the control register **1003** to the data line of the display memory **1006** and completes the write operation. At the time of read-out, on the other hand, the address decoder **1005** decodes the read address outputted by the timing generation unit **1004** and selects the word line inside the corresponding display memory. Thereafter, the display data for one line is collectively outputted from the data line of the display memory **1006**.

[0048] Incidentally, the read address described above is switched one line by line from the address at which the data of the leading line of the screen panel is stored, for example, and after the address of the final line, this operation is repeated while returning again to the leading line. The address switch timing of each line is in synchronism with CL1 and the timing for outputting the address of the leading

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line is in synchronism with FLM. The address decoder **1005** has a so-called "arbitration function" that assigns priority for either of the write operation and the read operation when they occur simultaneously.

[0049] The column electrode driver unit **1007** is the portion that converts the display data of each column of one line read out from the display memory **1006** to a predetermined column voltage, and selects and outputs either one of the voltage output and the terminal from the common electrode. This unit **1007** can be accomplished by use of the column voltage generation circuit in combination with the short-circuit switch in the same way as the column voltage driver circuit **203** of the first embodiment shown in **FIG. 5**.

[0050] The common electrode driver unit **1008** and the row electrode driver unit **1009** have the same construction and execute the same operation as those of the common electrode driver unit **204** and the row electrode driver unit **205** in the first embodiment. Therefore, the detailed explanation will be omitted. The timing generation unit **1004** and the power source circuit **1010** provide the input signal and the input voltage necessary for each block, respectively.

[0051] The operation of the liquid crystal display controller **1001** described above can accomplish the temporary short-circuit operation between the column electrode and the common electrode at the alternation timing as the feature of the present invention. Therefore, this embodiment can achieve lower power consumption in the same way as in the first embodiment.

[0052] The liquid crystal display controller **1001** according to the second embodiment can be applied to a cellular telephone set, for example. **FIG. 13** shows a block construction of the cellular telephone set. Referring to **FIG. 13**, reference numeral **1301** denotes a liquid crystal module including the liquid crystal display controller of this invention and the pixel unit. Numeral **1302** denotes an ADPCM CODEC circuit for compressing/expanding speech. Numeral **1303** denotes a speaker. Numeral **1304** denotes a microphone. Numeral **1305** denotes a keyboard. Numeral **1306** denotes a TDMA circuit for time division multiplexing the digital data. Numeral **1307** denotes EEPROM for storing a registered ID number. Numeral **1308** denotes ROM for storing a program. Numeral **1309** denotes SRAM for temporarily storing the data and providing a work area of a microcomputer. Numeral **1310** denotes a PLL circuit for setting a carrier frequency of a wireless signal. Numeral **1311** denotes an RF circuit for transmitting and receiving the wireless signals. Numeral **1312** denotes a system controlling microcomputer. In **FIG. 13**, the aforementioned driving parameters and display data are given from the system controlling microcomputer **1312**. These data are stored in ROM **1308** and SRAM **1309**, respectively. The detailed explanation of each block will be hereby omitted, but the construction shown in **FIG. 13** makes it possible to apply the liquid crystal display controller of the second embodiment to the cellular telephone unit.

[0053] Next, the third embodiment of the present invention will be explained with reference to FIGS. **14** to **16**. To achieve lower power consumption at the row electrode driver unit, this embodiment contemplates to apply the short-circuit operation of the present invention. In the driving system of the ordinary active matrix type liquid crystal, the GON voltage shown in **FIG. 8** is higher than GND and

GOFF is lower than GND. If the row voltage is temporarily short-circuited to GND on the basis of this voltage relationship as shown in **FIG. 14**, power consumption with the voltage shift to GND does not exist, and power consumption of the row voltage driver unit can be reduced. Therefore, the construction of the row electrode driver unit and its construction for accomplishing this operation will be explained with reference to **FIGS. 15 and 16**.

[0054] **FIG. 15** shows the internal construction of the row electrode driver unit according to the third embodiment of the present invention. Numeral **1501** denotes the row electrode driver unit. Numeral **1502** denotes a row selection circuit. Numeral **1503** denotes a switch controlling circuit. Numeral **1504** denotes a short-circuit switch C. First, the row selection circuit **1502** is a portion that outputs VGON/VGOFF in the same way as the row electrode driver unit **205** in the first embodiment of the present invention. The row selection circuit **1502** acquires High of FLM at the rise of CL3, sequentially shifts the signal FLM in synchronism with CL3 and outputs the signal so shifted as R (generically representing R1 to Rm). The switch controlling circuit **1503** is a portion that controls the short-circuit switch C**1504**. Its inputs are FLM, CL3 and SHTR. The switch controlling circuit **1503** outputs as such SHTR during the scanning period in which VGON is applied to the row and during one previous period, and outputs Low in other periods. The short-circuit switch C**1504** selects GND when the control signal SR (generically representing SR1 to SRm) outputted by the switch controlling circuit **1503** is High, selects the terminal from the row selection circuit **1502** when the control signal SR is Low and outputs VY (generically representing VY1 to VYm). **FIG. 16** shows altogether the operation timing chart of the operation for VY2, by way of example. As can be appreciated from **FIG. 16**, the row electrode driver unit **1501** according to the third embodiment of the present invention can accomplish the operation shown in **FIG. 14**.

[0055] When combined with the first liquid crystal display device and the second liquid crystal display controller according to the present invention, the row electrode driver unit according to the third embodiment can further reduce power consumption.

[0056] Next, the fourth embodiment of the present invention will be explained with reference to FIGS. **17** to **20**. Besides the structure shown in **FIG. 2**, the structure in which the terminal of the holding capacitance is connected to a preceding row of a given row is known as the pixel structure of the active matrix type liquid crystal as shown in **FIG. 17**. When such a pixel structure is employed, it is customary to change the voltage waveform of GOFF in the same amplitude as that of the common voltage in order to keep the same potential relationship between the holding capacitance and the liquid crystal cell as shown in **FIG. 18**. When the short-circuit operation of the present invention is applied to this driving method, the potential relationship between VCOM and VY becomes different in the short-circuit period in which SHT is High as shown in **FIG. 19**. As a result, the charge stored in the holding capacitance migrates and power consumption increases. To solve this problem, the output of VY is brought into the high impedance (Hi-Z) state during the short-circuit period as shown in **FIG. 20**, for example. This operation can be easily accomplished when a switch is disposed inside the row electrode driver unit, for example,

and connection of VY is cut off in match with High of SHT. In **FIG. 20**, VY becomes VGON in synchronism with the second CL3 pulse and write of the column voltage is executed. The output is not brought into the Hi-Z state during this period because it does not have much technical meaning.

[0057] The fourth embodiment described above can acquire the power consumption saving effect in the same way as in the first to third embodiments in the pixel structure in which the terminal of the holding capacitance is connected to the row of a preceding stage of a given stage.

[0058] Though the foregoing embodiments have been explained about Vcom modulation drive by way of example, the present invention can be applied also to dot inversion drive and column inversion drive on the basis of the same concept. **FIG. 21** shows the voltage waveforms of the column voltage and common voltage in the drive systems as the fifth embodiment of the present invention.

[0059] The embodiments of the present invention provide the following effects in the active matrix type liquid crystal display device in which the effective value of the applied voltage controls the transmission factor (brightness) of each pixel:

[0060] The voltage can be substantially shifted to the midpoint of alternation magnitude without consuming power when the column electrode and the common electrode sandwiching the liquid crystal between them are temporarily short-circuited at the timing of alternation;

[0061] Power consumption can be saved when the applied voltage to the row electrode as the signal for selecting the row is temporarily short-circuited to GND; and

[0062] The power consumption reduction methods described above can be applied without unnecessary power consumption to the pixel structure for connecting the terminal of the holding capacitance to the row of a preceding stage of a given stage when the applied voltage to the row electrode is brought into the high impedance state during the short-circuit period described above.

What is claimed is:

1: A display driver circuit for driving an active matrix type display panel which includes column electrodes and row electrodes arranged in a matrix form, a common electrode disposed opposite to the column electrodes and the row electrodes, and pixel units disposed at intersection points between the column electrodes and the row electrodes with each pixel unit being connected to a column electrode, a row electrode and the common electrode, the display driver circuit comprising:

    a row selector circuit for switching over to either a first potential of a row voltage or a second potential of the row voltage, and outputting a potential thus switched to the row electrodes, the first potential of the row voltage causing the pixel units to be in an "on" state, and the second potential of the row voltage causing the pixel units to be in an "off" state; and

    a switching circuit disposed on the row electrodes between the row selector circuit and the pixel units,

    wherein the switching circuit switches over to either a third potential or a potential on a side of the row selector circuit, the third potential being a potential between the first and second potentials.

2: The display driver circuit according to claim 1, wherein the switching circuit temporarily selects the third potential, when the row selector circuit switches over to either first potential or the second potential.

3: The display driver circuit according to claim 2, wherein the switching circuit temporarily selects the third potential for every scanning period at a second half of a scanning period.

4: A display driver circuit for driving an active matrix type display panel which includes column electrodes and row electrodes arranged in a matrix form, a common electrode disposed opposite to the column electrodes and the row electrodes, and pixel units disposed at intersection points between the column electrodes and the row electrodes with each pixel unit being connected to a column electrode, a row electrode and the common electrode, the display driver circuit comprising:

    a row selector circuit for switching over to either a first potential of a row voltage or a second potential of the row voltage, and outputting a potential thus switched to the row electrodes, the first potential of the row voltage causing the pixel units to be in an "on" state, and the second potential of the row voltage causing the pixel units to be in an "off" state; and

    a switching circuit for temporarily switching over to a third potential, when the row selector circuit switches over to either the first potential of the row voltage or the second potential of the row voltage, the third voltage being a potential between the first potential and the second potential.

5: A display driver circuit for driving an active matrix type display panel which includes column electrodes and row electrodes arranged in a matrix form, a common electrode disposed opposite to the column electrodes and the row electrodes, and pixel units disposed at intersection points between the column electrodes and the row electrodes with each pixel unit being connected to a column electrode, a row electrode and the common electrode, the display driver circuit comprising:

    a row selector circuit for switching over to either a first potential of a row voltage or a second potential of the row voltage, and outputting a potential thus switched to the row electrodes, the first potential of the row voltage causing the pixel units to be in an "on" state, and the second potential of the row voltage causing the pixel units to be in an "off" state; and

    a short-circuiting circuit for temporarily short-circuiting the row electrodes to the ground, when the row selector circuit switches over to either the first potential of the row voltage or the second potential of the row voltage.

* * * * *

专利名称(译)	液晶驱动电路和液晶显示装置		
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[标]申请(专利权)人(译)	工藤YASUYUKI 横田YOSHIKAZU 黑川十成 HIGA ATSUSHIRO		
申请(专利权)人(译)	工藤YASUYUKI 横田YOSHIKAZU 黑川十成 HIGA ATSUSHIRO		
当前申请(专利权)人(译)	瑞萨电子公司		
[标]发明人	KUDO YASUYUKI YOKOTA YOSHIKAZU KUROKAWA KAZUNARI HIGA ATSUSHIRO		
发明人	KUDO, YASUYUKI YOKOTA, YOSHIKAZU KUROKAWA, KAZUNARI HIGA, ATSUSHIRO		
IPC分类号	G02F1/133 G09G3/20 G09G3/36		
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摘要(译)

矩阵型液晶显示装置具有抑制功耗的功能，而不需要额外的电路布置，例如存储电容的布置和布线到存储电容，并且不需要设置新的外部元件。开关设置在液晶显示装置中，以使交替定时同步地暂时使列电极和将液晶夹在其间的公共电极短路。