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(54) LIQUID CRYSTAL DISPLAY APPARATUS HAVING LEVEL CONVERSION CIRCUIT

(76) Inventors: **Hideo Sato**, Hitachi-shi (JP); **Yoshiro Mikami**, Hitachi-shi (JP); **Hiroshi Kageyama**, Hitachi-shi (JP); **Ohkubo Tatsuya**, Chigasaki-shi (JP)

Correspondence Address:
ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

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(57) **ABSTRACT**

A liquid crystal display apparatus having a level conversion circuit in which a high speed operation can be attained and also a small transistor capacity can be obtained is provided. In the liquid crystal display apparatus, a signal circuit for driving pixel elements of a display unit and a scanning circuit are provided. The level conversion circuit is constituted of a first and a second transistors **111** and **112** in which a respective gate electrodes is connected to a first bias voltage power supply, and a third and a fourth transistors **121** and **122** in which a respective gate electrodes is connected to a second bias voltage power supply and a respective source electrodes is connected to a power supply.

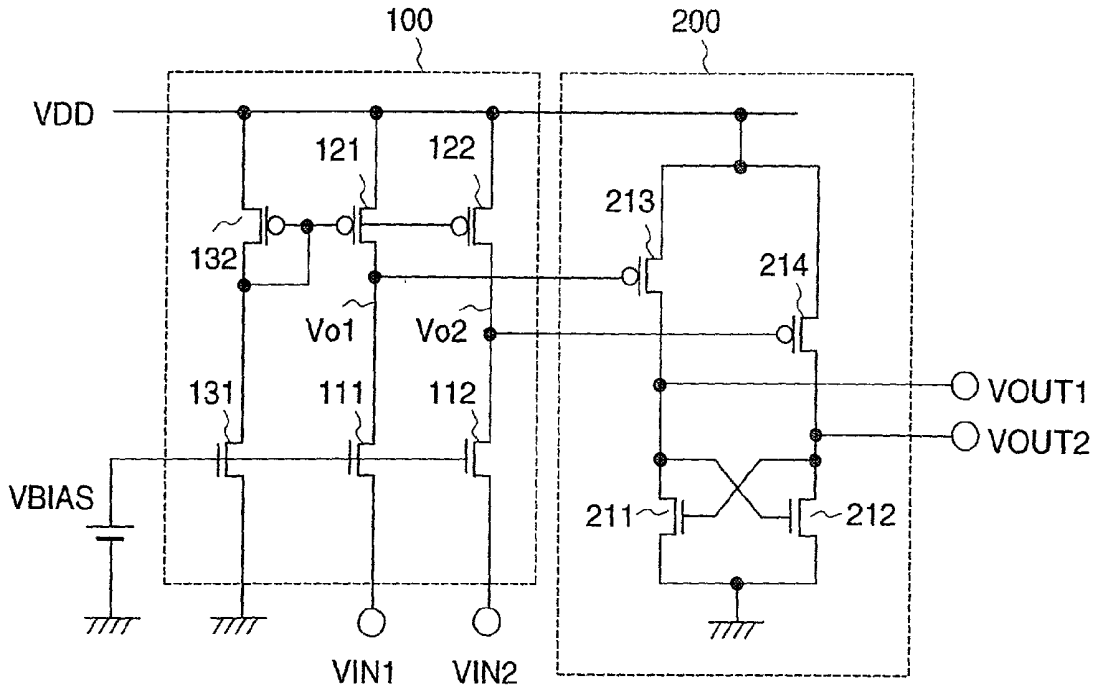


FIG. 1

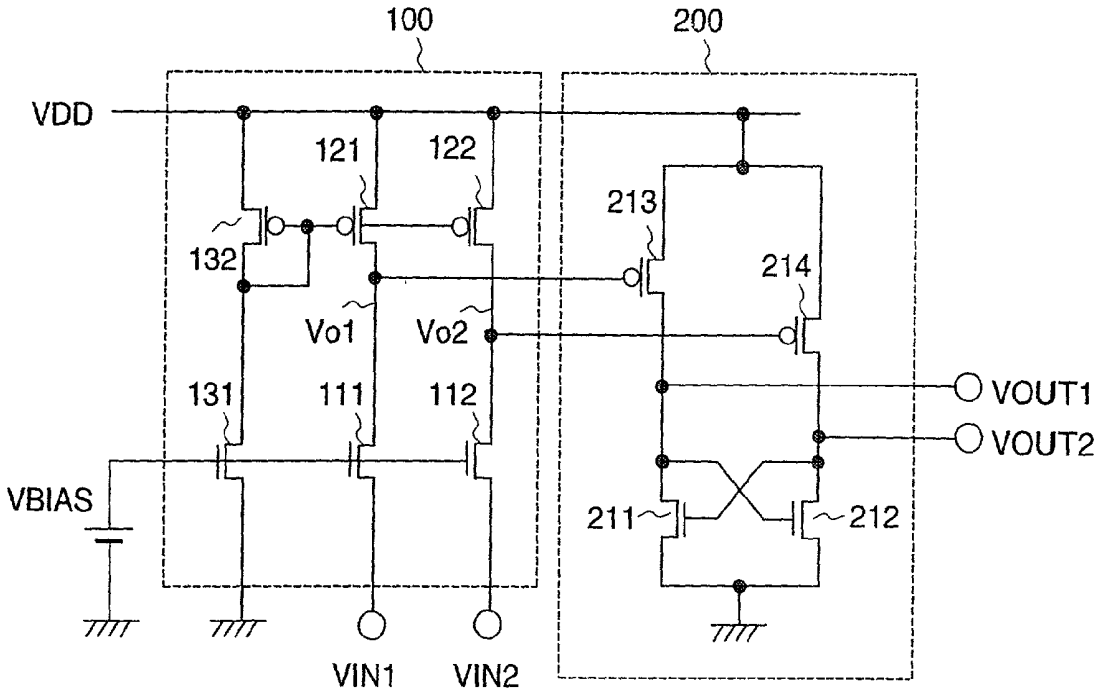

100
200
VDD
121
122
213
132
214
Vo1
Vo2
131
111
112
VOUT1
VOUT2
VBIAS
211
212
VIN1
VIN2

FIG. 2

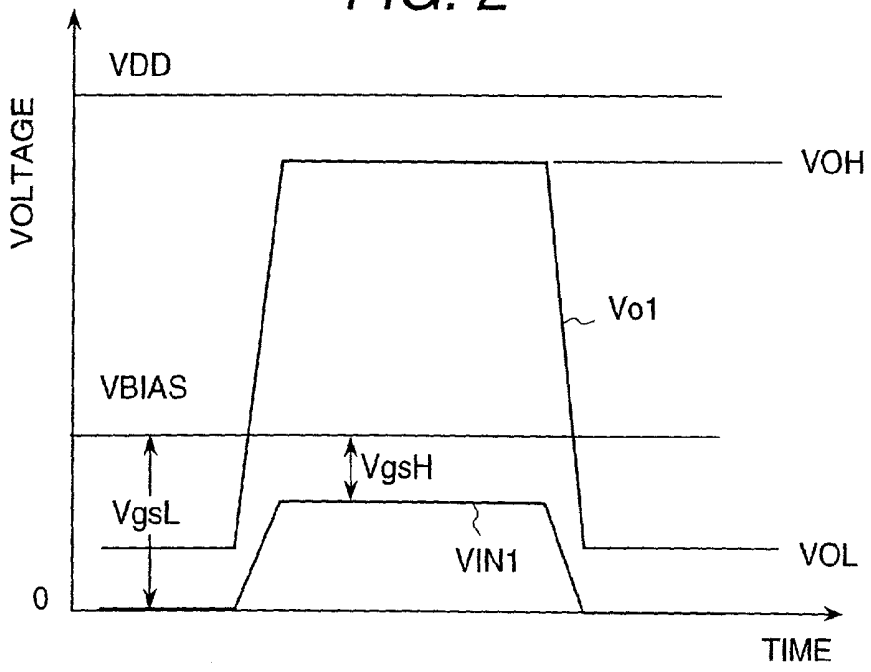

VDD
VOLTAGE
VOH
Vo1
VBIAS
VgsH
VgsL
VIN1
VOL
0
TIME

FIG. 3

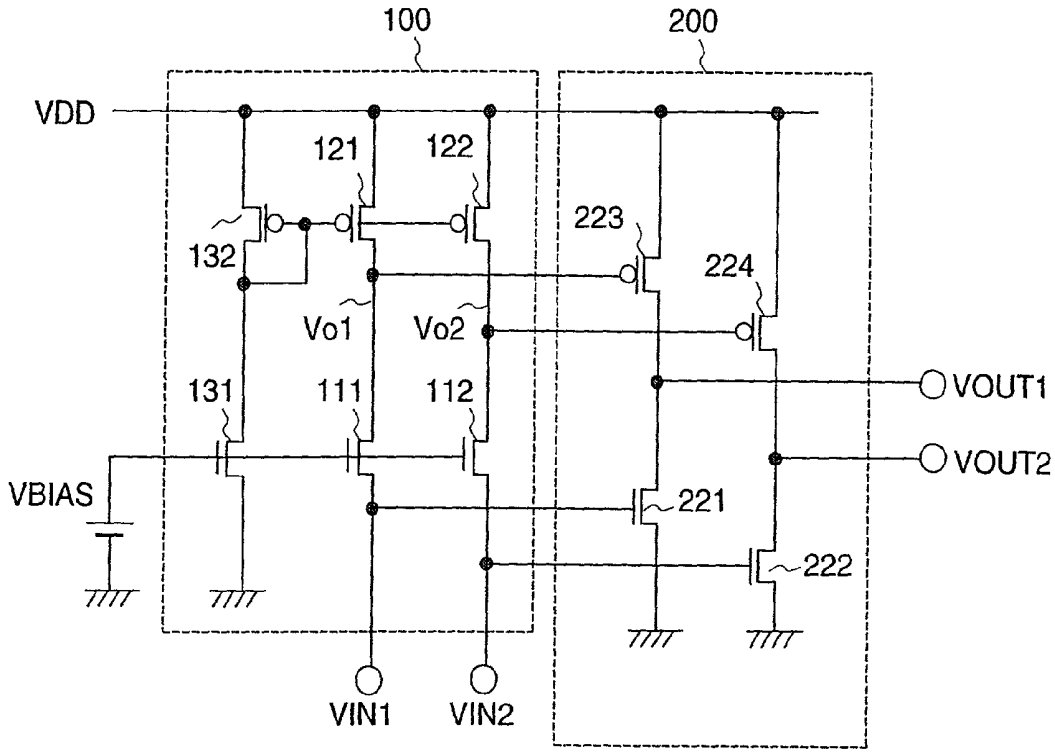

100
200
VDD
121
122
132
223
224
Vo1
Vo2
131
111
112
VOUT1
VOUT2
VBIAS
221
222
VIN1
VIN2

FIG. 4

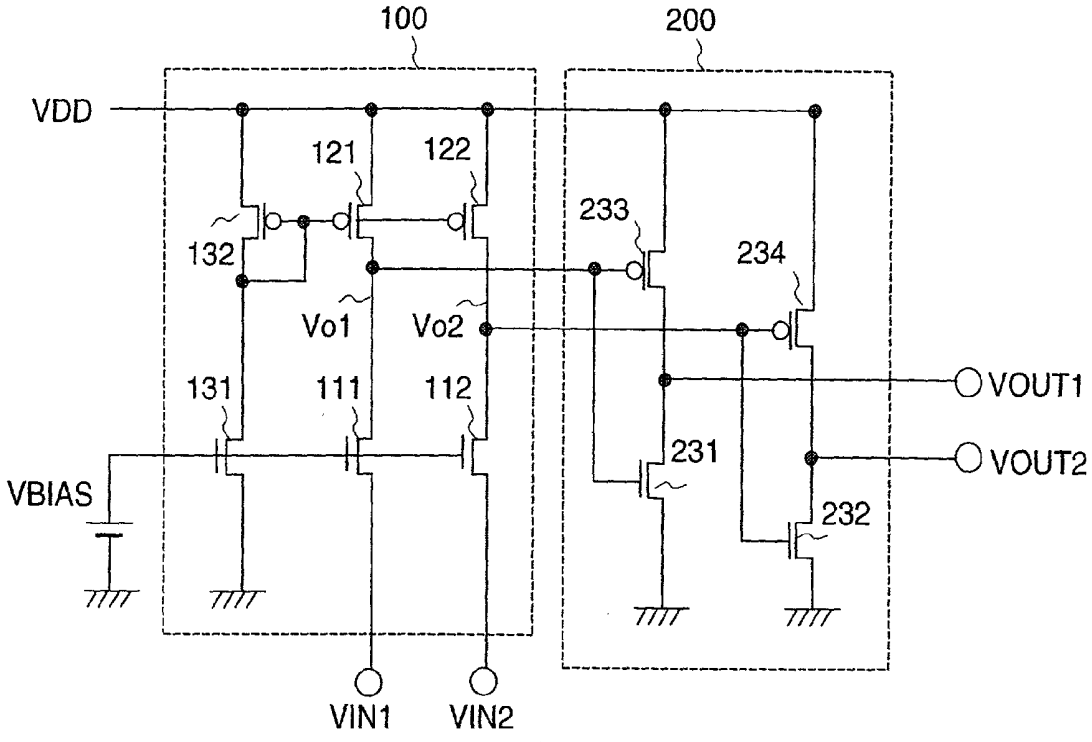

100
200
VDD
121
122
132
233
234
Vo1
Vo2
131
111
112
VOUT1
VOUT2
VBIAS
231
232
VIN1
VIN2

FIG. 5

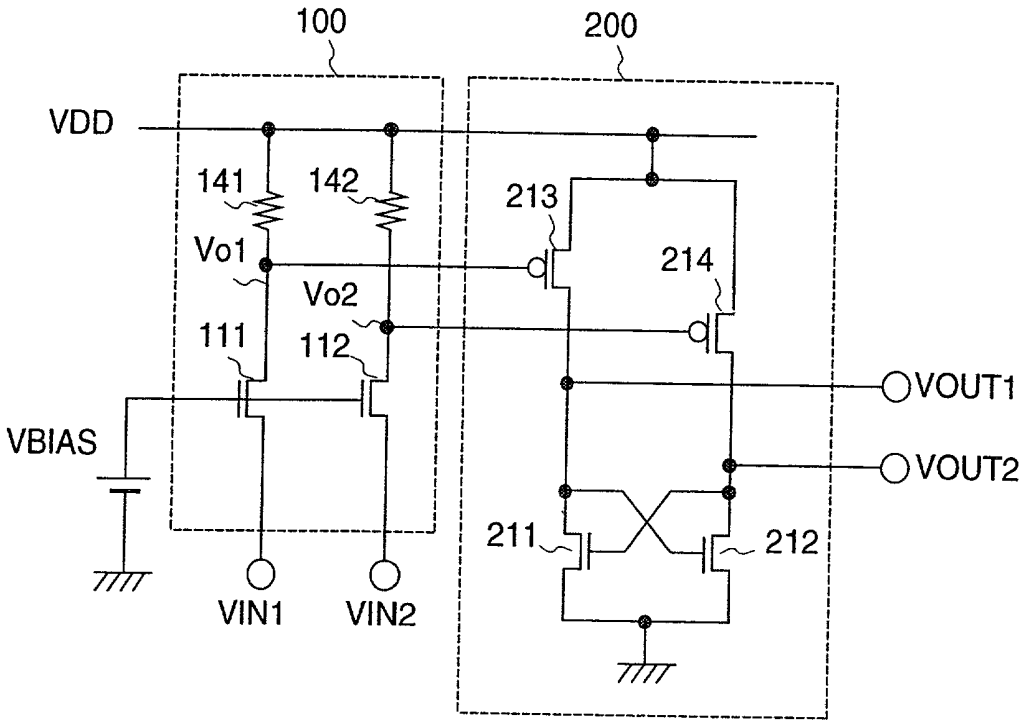

100
200
VDD
141
142
213
Vo1
214
Vo2
111
112
VOUT1
VBIAS
VOUT2
211
212
VIN1
VIN2

FIG. 6

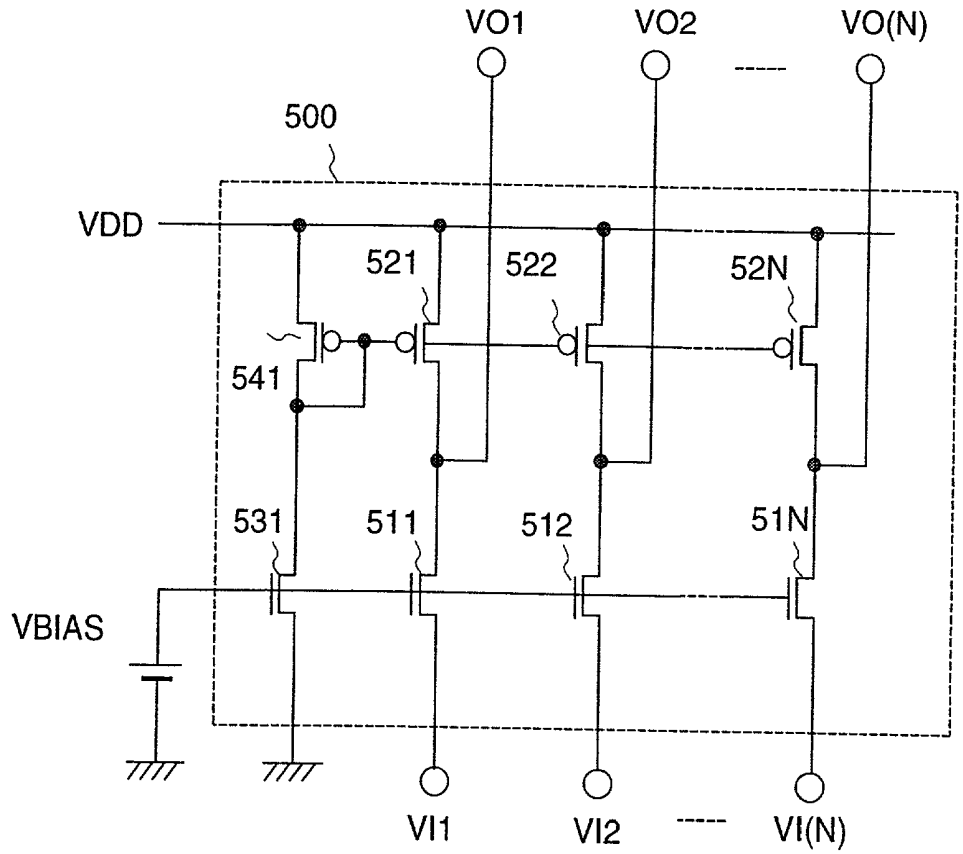

VO1
VO2
VO(N)
500
VDD
521
522
52N
541
531
511
512
51N
VBIAS
VI1
VI2
VI(N)

FIG. 7

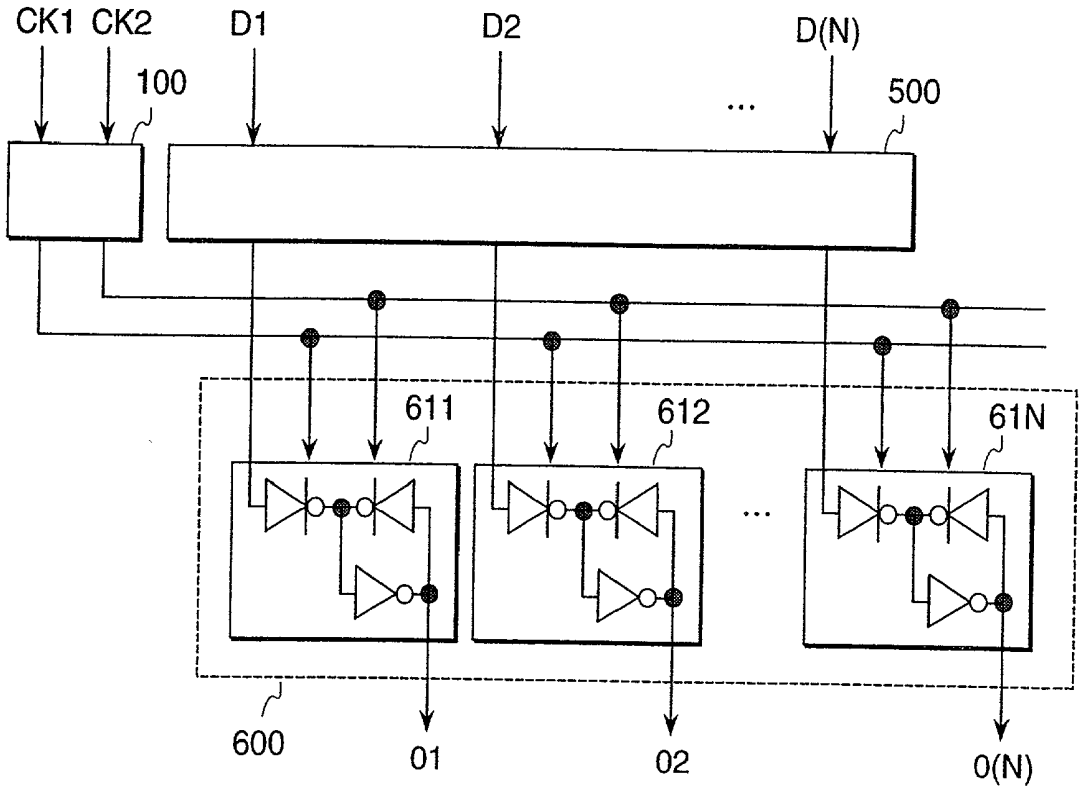

CK1
CK2
D1
D2
D(N)
100
500
611
612
61N
600
01
02
0(N)

FIG. 8

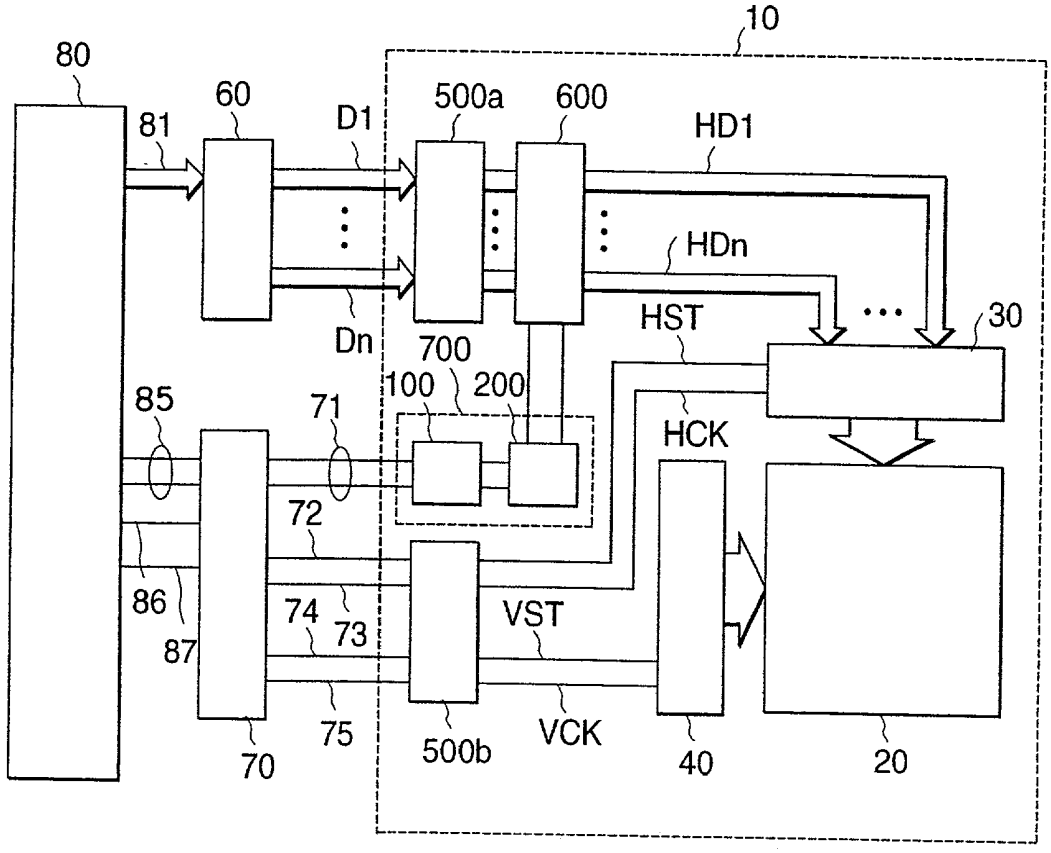
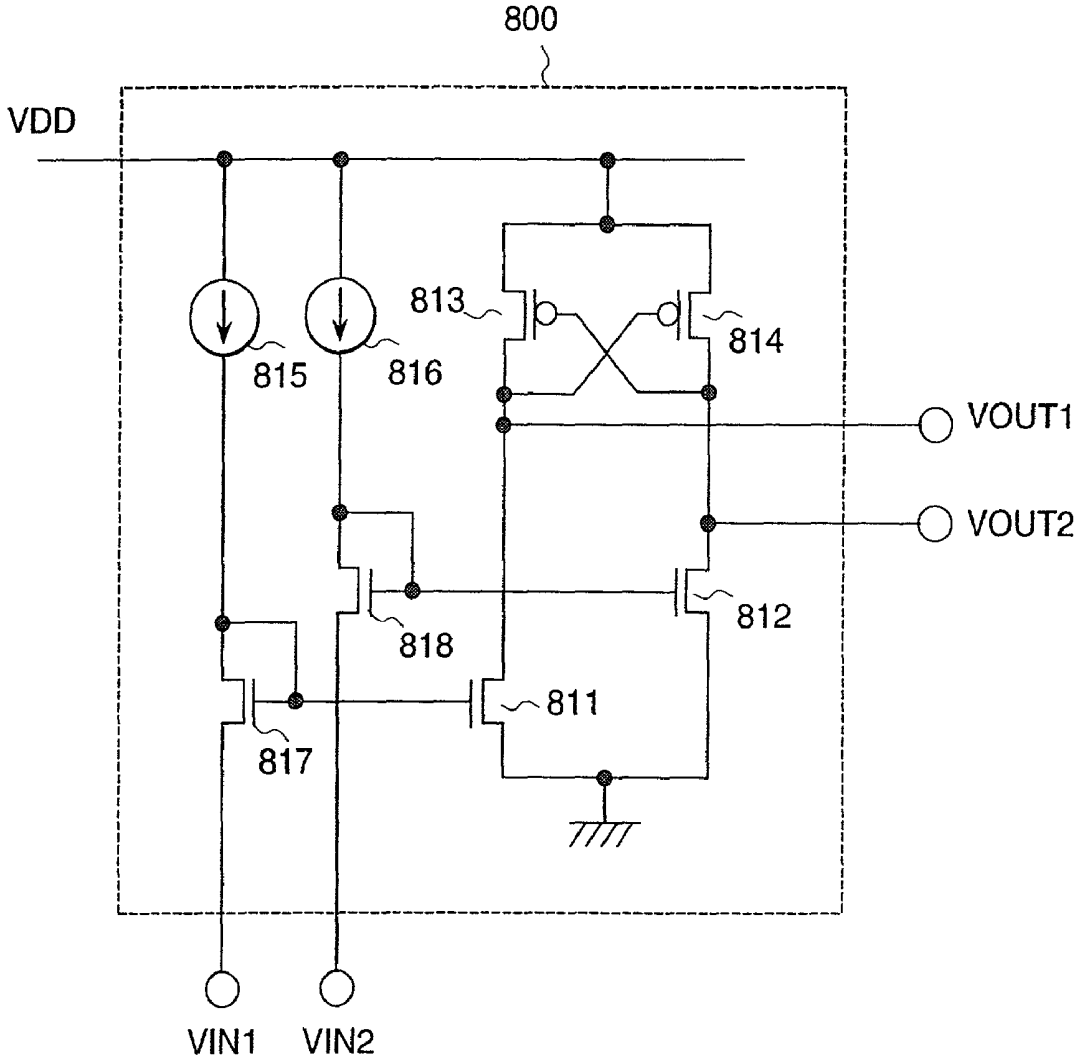

10
80
81
60
D1
500a
600
HD1
HDn
Dn
700
100
200
HST
30
85
71
HCK
72
86
74
73
VST
87
75
500b
VCK
70
40
20

FIG. 9 (PRIOR ART)



LIQUID CRYSTAL DISPLAY APPARATUS HAVING LEVEL CONVERSION CIRCUIT

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a liquid crystal display apparatus having a level conversion circuit in which a signal having a low voltage amplitude is converted to a signal having a high voltage amplitude and in particular to relates to a level conversion circuit in a clock interface and a data interface of a liquid crystal display apparatus using thin-film transistors (TFT: Thin-Film Transistor).

[0002] A level conversion circuit used in a clock interface and a data interface of a liquid crystal display apparatus is described in, for example JP-A 6-216753 and JP-A 6-283979, etc.. In the level conversion circuit shown in these prior arts, a thin-film transistor having a multi-crystallization silicon and a metal-oxide semiconductor (MOS: Metal-Oxide Semiconductor) having a mono-crystallization silicon are employed. In the above stated level conversion circuit, an input signal having a low voltage amplitude is converted to an output signal having a high voltage amplitude for use in a drive circuit for the liquid crystal display apparatus.

[0003] The above stated input signal has, for example, the voltage amplitude of 5 V or 3.3 V which is used in a common use LSI. Further, the above stated output signal has, for example, the voltage amplitude of 12 V or 15 V which corresponds to a power supply voltage of an interior circuit of the level conversion circuit.

[0004] As this level conversion circuit, there are a differential input type level conversion circuit which input a mutually reverse phase signal and a single phase input type level conversion circuit which input an independent signal. The differential input type level conversion circuit is used for in a comparative high speed operation clock interface and the single phase input type level conversion circuit is used for in a data interface.

[0005] **FIG. 9** shows an example of the differential input type level conversion circuit described in JP-A 6-216753. This level conversion circuit **800** in the prior art is constituted by a pair of input transistors **811** and **812**, a pair of load transistors **813** and **814**, a pair of constant current power supplies **815** and **816**, and a pair of level shift transistors **817** and **818**.

[0006] The respective input transistors **811** and **812** and the respective level shift transistors **817** and **818** is a N type TFT. The respective load transistors **813** and **814** is a P type TFT. In the level shift transistors **817** and **818**, a drain electrode and a gate electrode are connected each other and a respective source electrodes is connected to input terminals VIN1 and VIN2. Further, to a connection point of the drain electrode and the gate electrode, the constant current power supplies **815** and **816** and the gate electrodes of the input transistors **811** and **812** are connected.

[0007] The respective source electrodes of the input transistors **811** and **812** is connected to a ground and the respective drain electrodes of the input transistors **811** and **812** is connected to the respective output terminals VOUT1 and VOUT2. The respective drain electrodes of the load transistors **813** and **814** is connected respectively to output terminals VOUT1 and VOUT2. The respective gate electrodes of the load transistors **813** and **814** are respectively to the output terminals VOUT1 and VOUT2. The respective source electrodes of the load transistors **813** and **814** is connected to a power supply VDD.

[0008] To the level conversion circuit **800** connected with the above manner, the signals at the input terminals VIN1 and VIN2 which have mutually the reverse phase are supplied. Herein, it will be explained, as the operation state of the level conversion circuit **800**, on the assumption that each the voltages which are inputted to the input terminals VIN1 and VIN2 is 3.3 V and 0 V, the voltage of the power supply VDD is 15 V, and a threshold voltage of the respective N type transistors is 2 V.

[0009] Since each of the level shift transistors **817** and **818** operates to heighten respectively the input terminals VIN1 and VIN2 with the threshold voltage part, the voltages of 5.3 V and 2 V are applied respectively to gate electrodes of the input transistors **811** and **812**. As a result, the input transistor **811** presents a continuity state and the input transistor **812** presents a non-continuity state, respectively, and then the voltage of the output terminal VOUT1 becomes 0 V.

[0010] Since this output terminal VOUT1 is connected to the gate electrode of the load transistor **814**, the load transistor **814** presents a continuity state and then the voltage of the output terminal VOUT2 becomes 15 V. Further, since the load transistor **814** in which the gate electrode of the load transistor **814** is connected to the output terminal VOUT2 becomes a non-conductive state, then the output terminal VOUT1 maintains the voltage of 0 V.

[0011] Next, from the above stated state, the operation wherein the voltages of the input terminals VIN1 and VIN2 change respectively to 0 V and 3.3 V will be explained. When the voltages of the input terminals VIN1 and VIN2 change respectively to 0 V and 3.3 V, the input transistor **811** presents the conductive state but the input transistor **812** presents a non-conductive state, respectively.

[0012] In this time, since the load transistor **814** which is connected to the drain electrode of the input transistor **812** becoming the conductive state presents the conductive state, when the resistances at the conductive states of the input transistor **812** and the load transistor **814** are expressed by RON2 and RON4, the voltage VOUT2 of the output terminal VOUT2 at the time in which the voltage of the input terminal changes is expressed by a following formula 1.

$$VOUT2=RON2/(RON2+RON4)\times VDD \quad (1)$$

[0013] As understood from the above stated formula 1, the voltage of the output terminal VOUT2 at the time in which the voltage of the input terminal changes is determined by a divided voltage ratio between the resistors RON2 and RON4. With the above stated voltage, the load transistor **813** presents the conductive state and the voltage of the output terminal VOUT1 changes to 15 V. Since the voltage of the output terminal VOUT1 changes to 15 V, the resistance of the load transistor **814** increases, and finally the load transistor **814** presents a non-conductive state. As a result, the voltage of the output terminal VOUT2 becomes 0 V.

[0014] Herein, to shorten the time where from the conductive state of the input transistor **812** to the voltage of the output terminal VOUT2 becomes 0 V, the voltage of the output terminal VOUT2 is necessary to approach 0 V as soon as possible by making small the resistor RON2 in the formula 1.

[0015] On the other hand, in the single phase input type level conversion circuit, one manner is employed using the differential input type level conversion circuit explained in above, the single signal is inputted to one input terminal and the voltage having ½ of the single phase input amplitude is supplied to another input terminal or another manner is employed using the differential input type level conversion circuit explained in above, the single signal is inputted to one input terminal and the single phase input amplitude is supplied to another input terminal by reversing the single phase signal.

SUMMARY OF THE INVENTION

[0016] When the voltage between the drain electrode and the source electrode is constant, the drain current of TFT or MOS transistor changes in proportion to a square of an effective gate voltage VE which is a difference between a gate voltage and a threshold voltage Vth. Since the resistor RON such as RON**2** and RON**4** under the above stated conductive state is in inverse proportion to this drain current, the gate voltage increases abruptly at a vicinity of the threshold voltage Vth.

[0017] In the case of the above stated level conversion circuit **800** stated in above, the drive condition of the gate voltages of the input transistors **811** and **812** corresponds that a voltage Vg**1** between the gate electrode and the drain electrode is 2 V and a voltage Vg**2** between the gate electrode and the drain electrode is 5.3 V.

[0018] To obtain the resistance under the conductive state necessary for in the voltage Vg**2** having 5.3 V, it is necessary to make large a size of the input transistor. When the size of the input transistor is made large, a capacity of the input terminal increases and also a capacity between the gate electrode and the drain electrode increases.

[0019] Further, since the input transistors **811** and **812** of the level conversion circuit **800** shown in **FIG. 9** constitute a source ground type amplification circuit, the capacity between the gate electrode and the drain electrode is made large equivalently with a magnification part of an amplification by a miller effect. The increase in the equivalent load capacity becomes an obstacle to perform the high speed operation.

[0020] Further, the conventional single phase input type level conversion circuit is more complicated in comparison with the differential input type level conversion circuit. This means, for example, when the single phase input type level conversion circuit is tried to apply to a digital type liquid crystal display apparatus which is operated by an image signal having a digital signal, it becomes a large obstacle.

[0021] When the image is sent by the digital signal, a data number thereof depends on a number of color (a number of gray level) with the image signal, a pixel element number of the liquid crystal display apparatus, a frame frequency, and an operation frequency of the level conversion circuit. For example, in a case where the number of color (number of gray level) is 8 bits, the pixel element number is 1280×1024, the frame frequency is 60 Hz, and the operation frequency is 20 MHz, accordingly the input data number is about 32 numbers.

[0022] An object of the present invention is to provide a liquid crystal display apparatus wherein a level conversion circuit enable to carry out a high speed operation in the liquid crystal display apparatus.

[0023] Another object of the present invention is to provide a liquid crystal display apparatus wherein a level conversion circuit can be constituted a small transistor capacity in the liquid crystal display apparatus.

[0024] According to the present invention, the above stated objects can be solved that in a liquid crystal display apparatus, a level conversion circuit is provided to a signal circuit for driving the pixel elements of a display unit and a scanning circuit, the level conversion circuit is constituted of a first transistor and a second transistor in which a respective gate electrodes of the first transistor and the second transistor is connected to a first bias voltage power supply, and a third transistor and a fourth transistor in which a respective gate electrodes of the third transistor and the fourth transistor is connected to a second bias voltage power supply and a respective drain electrodes of the third transistor and the fourth transistor is connected to a power supply.

[0025] A respective drain electrodes of the first transistor and the second transistor is connected to a respective drain electrodes of the third transistor and the fourth transistor each other, a signal having a mutually different polarity and having a low amplitude is inputted to the respective source electrodes of the first transistor and the second transistor, and from the drain electrode of the first transistor and the respective drain electrode of the first transistor and the second transistor, a signal having a mutually different polarity and having a high amplitude is taken out.

[0026] In the present invention, an output voltage is determined in accordance with a resistance ratio between the drain electrode and the source electrode of the first transistor and the second transistor in which a respective gate electrodes is biased by the first bias voltage power supply and the third transistor and the fourth transistor in which a respective gate electrodes is biased by the second bias voltage power supply.

[0027] Herein, a third resistor and a fourth resistor can be made large within an allowable range of an operation speed. Further, since the respective gate electrodes of the first transistor and the second transistor is biased to the fixed voltage, a capacity between the drain electrode and the source electrode is not depended on an amplification rate of the first transistor and the second transistor. As a result, the level conversion circuit according to the present invention can be operated with a high speed and a size of the transistor can be reduced.

BRIEF DESCRIPTION OF DRAWINGS

[0028] **FIG. 1** is a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a first embodiment according to the present invention;

[0029] **FIG. 2** is an explanatory view showing an operation of the level conversion circuit in the liquid crystal display apparatus according to the present invention;

[0030] **FIG. 3** is a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a second embodiment according to the present invention;

[0031] **FIG. 4** is a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a third embodiment according to the present invention;

[0032] **FIG. 5** is a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a fourth embodiment according to the present invention;

[0033] **FIG. 6** is a circuitry construction view showing a multi-input type level conversion circuit in a liquid crystal display apparatus of a fifth embodiment according to the present invention;

[0034] **FIG. 7** is a circuitry construction view showing a logic input circuit of one embodiment to which the level conversion circuit according to the present invention is applied;

[0035] **FIG. 8** is a block diagram showing a liquid crystal display apparatus according to the present invention; and

[0036] **FIG. 9** is a circuitry construction view showing a differential input type level conversion circuit according to the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] Hereinafter, a liquid crystal display apparatus having a level conversion circuit of one embodiment according to the present invention will be explained referring to the drawings.

[0038] **FIG. 1** shows a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a first embodiment according to the present invention. The level conversion circuit in the liquid crystal display apparatus of the first embodiment according to the present invention is constituted of a level conversion unit **100** and a wave-form shaping unit **200**.

[0039] The level conversion unit **100** is constituted of input transistors **111** and **112**, load transistors **121** and **122**, and bias use transistors **131** and **132**. In the input transistors **111** and **112**, a respective gate electrode of the respective input transistors **111** and **112** is connected to a bias power supply VBIAS, a respective source electrode of the respective input transistors **111** and **112** is connected to input terminals VIN1 and VIN2, and a respective drain electrode of the respective input transistors **111** and **112** is connected to outputs Vo1 and Vo2, respectively.

[0040] In the load transistors **121** and **122**, a respective gate electrode of the respective load transistors **121** and **122** is connected commonly to a bias use transistor **132**, a respective source electrode of the respective load transistors **121** and **122** is connected to a power supply VDD, and a respective drain electrode of the respective load transistors **121** and **122** is connected to the outputs Vo1 and Vo2, respectively.

[0041] In the bias use transistor **131**, a gate electrode of the bias use transistor **131** is connected to the bias power supply VBIAS, a source electrode of the bias use transistor **131** is connected to a ground point, and a drain electrode of the bias use transistor **131** is connected to the gate electrode and the drain electrode of the bias use transistor **132**. Herein, the bias use transistor **132** and the load transistors **121** and **122** constitutes so called a current-miller circuit.

[0042] On the other hand, the wave-form shaping unit **200** is constituted of input transistors **213** and **214**, and load transistors **211** and **212**. Each of the input transistors **213** and **214** employs a P-type transistor and further each of the load transistors **211** and **212** employs a N-type transistor. In comparison with the circuitry construction shown in the above stated level conversion circuit **800** according to the prior art, this circuitry construction of the first embodiment according to the present invention differs from that a conductive type of the transistor is reversal and an input is a high voltage amplitude. However, this circuitry construction of the first embodiment according to the present invention is equivalent to the level conversion circuit **800** according to the prior art.

[0043] To the respective gate electrodes of a pair of the input transistors **111** and **112** of the level conversion unit **100** connected in above, the signals VIN1 and VIN2 are supplied, such signals VIN1 and VIN2 have mutually the reverse phase. The signal levels of these signals VIN1 and VIN2 have voltages having a low amplitude of, for example, 0 V and 3.3 V and a voltage of the power supply VDD has a voltage of 15 V, a voltage of the bias power supply VBIAS has a voltage which exceeds over the maximum voltage of the input signals VIN1 and VIN2 and is 5.3 V, for example.

[0044] The operation of the level conversion circuit having the above stated conditions in the liquid crystal display apparatus of the first embodiment according to the present invention will be explained referring to **FIG. 2**. Herein, a response of the output Vo1 against to the input signal VIN1 is shown. When the input signals VIN1 and VIN2 are 0 V and 3.3 V, the voltages VgsL and VgsH between the gate electrode and the source electrode of the input transistor **111** are 5.3 V and 2 V, respectively.

[0045] Since the resistance values RdsL and RdsH between the gate electrode and the source electrode of the input transistor **111** which corresponds to the above stated voltages form to be RdsL<RdsH, the output voltage Vo1 has a relationship of the same phase to the input signal VIN1. A high level output voltage VOH (the input transistor **111** is the non-conductive state) and a low level output VOL (the input transistor **111** is the conductive state) of the output voltage Vo1 of this time becomes a divided voltage between a resistance value RL1 between the drain electrode and the source electrode of the load transistor **121** and the resistance value RdsL or RdsH between the drain electrode and the source electrode of the input transistor **111**. As a result, as shown in **FIG. 2**, the high level output voltage VOH slips off a little from the power supply voltage VDD or the low level output VOL slips off a little from the voltage of 0 V.

[0046] A response of the output voltage Vo2 against to the input signal VIN2 is not shown in figure but such a response of the output voltage Vo2 has a relationship of the reverse phase of the response of the input signal VIN1. Namely, a relationship between the input signals VIN1 and VIN2 of the level conversion unit **100** and the output voltages Vo1 and Vo2 of the level conversion unit **100** has the same phase. As a result, the output voltage Vo1 slips off a little from the power supply voltage VDD or the output voltage Vo2 slips off a little from 0 V.

[0047] Next, as stated in above, the wave-form shaping unit **200** is constituted of the input transistors **213** and **214**, and the load transistors **211** and **212**. The respective input transistors **213** and **214** is a P-type TFT and the respective load transistors **211** and **212** is a N-type TFT. The respective gate electrodes of the input transistors **213** and **214** is

connected to the respective output terminals Vo1 and Vo2 of the level conversion circuit **100**, respectively, the respective drain electrodes of the input transistors **213** and **214** is connected to the output terminals VOUT1 and VOUT2, respectively, and further the respective source electrodes of the input transistors **213** and **214** is connected to the power supply voltage VDD, respectively.

[**0048**] Further, the respective drain electrode of the load transistors **211** and **212** is connected to respective the output terminals VOUT1 and VOUT2, respectively, the respective gate electrodes of the load transistors **211** and **212** is connected to the output terminals VOUT1 and VOUT2, respectively, and further the respective source electrode of the load transistors **211** and **212** is connected to the ground point, respectively.

[**0049**] The wave-form shaping unit **200** as connected in above has a different unit which differs from the conductive type transistor constituted by the input transistors **811** and **812** and the load transistors **813** and **814** according to the prior art but this wave-form shaping unit **200** is equivalent to the above stated circuit according to the prior art.

[**0050**] The different circuitry construction of this first embodiment according to the present invention in comparison with the circuitry construction shown in **FIG. 9** is as following, namely the input signal is amplified in the level conversion unit **100** and has a substantially equal amplitude to the power supply voltage. As a result, it is unnecessary to make large the size the transistor which is a problem in the prior art and then it is possible to carry out the high speed operation.

[**0051**] Entering into details, in the level conversion circuit for use in the liquid crystal display apparatus of this first embodiment according to the present invention, using the bias use power supply VBIAS, the gate voltage for applying the input transistors **111** and **112** is controlled in accordance with the voltage of the bias power supply VBIAS. With the above stated reasons, it is possible to make the high current the drain current operation points of the input transistors **111** and **112** and the drain current operation points of the load transistors **121** and **122** and it is possible to carry out the high speed operation.

[**0052**] Further, since the relationship between the input and the output is the same phase, it can be prevented the increase in the capacity according to the miller effect and with this point it is possible to carry out the high speed operation.

[**0053**] In the level conversion circuit for use in the liquid crystal display apparatus of this first embodiment according to the present invention, since the level conversion circuit is constituted of only the transistors, it has a merit that the level conversion circuit can be manufactured easily.

[**0054**] Further, in the level conversion circuit for use in the liquid crystal display apparatus of this first embodiment according to the present invention, the bias use transistor **131** and the input transistors **111** and **112** are constituted mutually of the N-type transistor and the currents of the load transistors **121** and **122** are controlled in accordance with the bias use transistor **132** and the output voltage is generated through this current and the resistances of the input transistors **111** and **112**.

[**0055**] As a result, the fluctuation of the output voltage against to the fluctuation of the characteristic of the transistor can be restrained and there is a merit the yield in the manufacturing can be heightened.

[**0056**] **FIG. 3** shows a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a second embodiment according to the present invention. This second embodiment according to the present invention shown in **FIG. 3** differs from the first embodiment according to the present invention shown in **FIG. 1** and the different construction is a wave-form shaping unit **200** shown in **FIG. 3**.

[**0057**] The wave-form shaping unit **200** of this second embodiment according to the present invention is constituted of N-type load transistors **221** and **222** and P-type input transistors **223** and **224**. The respective source electrodes of the N-type load transistors **221** and **222** is grounded, the respective gate electrodes of the load transistors **221** and **222** is connected to the input terminals VIN1 and VIN2, and the respective drain electrodes of the load transistors **221** and **222** is connected to the respective drain electrodes of the P-type input transistors **223** and **224**, respectively.

[**0058**] The respective source electrodes of the P-type input transistors **223** and **224** is connected to the power supply VDD and the respective gate electrodes of the input transistors **223** and **224** is connected to the outputs Vo1 and Vo2 of the level conversion unit **100**, respectively.

[**0059**] The operation of the wave-form shaping unit **200** constituted in above will be explained. As one example of the operation condition, when the voltages of the input terminals VIN1 and VIN2 are respectively 3.3 V and 0 V, the voltage of the power supply VDD is 15 V. and the voltage of the bias power supply is 5.3 V. In this case, to the gate electrodes of the N-type load transistors **221** and **222** the voltages of 3.3 V and 0 V are applied respectively, and the load transistors **221** presents the conductive state and the load transistor **222** presents the non-conductive state.

[**0060**] On the other hand, to the gate electrodes of the P-type input transistors **223** and **224** to which the output of the level conversion unit **100** is inputted, since the voltages of a substantial 15 V and a substantial 0 V are inputted, the load transistor **221** presents the conductive state and the load transistor **222** presents the non-conductive state.

[**0061**] As a result, the output terminals VOUT1 and VOUT2 become respectively 0 V and 15 V, the low amplitude voltage signals having 3.3 V and 0 V are converted to the high amplitude voltage signals having 0 V and 15 V.

[**0062**] According to the level conversion circuit in the liquid crystal display apparatus of the second embodiment according to the present invention, since each of the gate electrodes of the N-type load transistors and the gate electrodes of the P-type input transistors constituting the wave-form shaping unit **200** is controlled independently 0.5 V and 15 V as a standard, there is a merit in which the level conversion circuit can be operated suitably against to the fluctuation of the power supply voltage VDD.

[**0063**] **FIG. 4** shows a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a third embodiment according to the present invention. This third embodiment shown according to the

present invention in **FIG. 4** differs from the first embodiment according to the present invention shown in **FIG. 1** and the different construction is the wave-form shaping unit **200**.

[**0064**] The wave-form shaping unit **200** of this third embodiment according to the present invention is constituted of N-type load transistors **231** and **232** and P-type input transistors **233** and **234**. Each of the N-type load transistor **231** and the P-type input transistor **233** and each of the N-type load transistor **232** and the P-type input transistor **234** constitutes respectively an inverter circuit.

[**0065**] The operation of the wave-form shaping unit **200** constituted in above will be explained. As one example of the operation condition, the voltages of the input terminals VIN1 and VIN2 are respectively 3.3 V and 0 V, the voltage of the power supply VDD is 15 V and the voltage of the bias power supply is 5.3 V. In this case, the respective input transistors **111** and **112** presents respectively the conductive state and the non-conductive state, and the output voltages Vo1 and Vo2 of the level conversion circuit **100** are substantial 15 V and substantial 0 V. Since these voltages of the output voltages are carried out the wave-form shaping and are amplified in the inverter circuit, the voltages of the output terminals VOUT1 and VOUT2 become respectively 0 V and 15 V.

[**0066**] According to the level conversion circuit **100** in the liquid crystal display apparatus of this third embodiment according to the present invention, the low amplitude voltage signals having 3.3 V and 0 V which are supplied to the input terminals can be converted to the high amplitude voltage signals having 0 V and 15 V.

[**0067**] **FIG. 5** shows a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a fourth embodiment according to the present invention. This fourth embodiment according to the present invention shown in **FIG. 5** differs from the first embodiment according to the present invention shown in **FIG. 1** and the different construction is the level conversion unit **100**. The level conversion unit **100** of this fourth embodiment according to the present invention is constituted of resistors **141** and **142** in place of the load transistors **121** and **112** which are described in the first embodiment shown in **FIG. 1**.

[**0068**] The operation of the level conversion unit **100** constituted in the above fourth embodiment according to the present invention will be explained. As one example of the operation condition, the voltages of the input terminals VIN1 and VIN2 are respectively 3.3 V and 0 V, the voltage of the power supply VDD is 15 V and the voltage of the bias power supply is 5.3 V. In this case, the respective input transistors **111** and **112** presents respectively the conductive state and the non-conductive state.

[**0069**] As a result, the output voltages Vo1 and Vo2 of the level conversion circuit **100** are a substantial 15 V and a substantial 0 V. Since these output voltages are carried out the wave-form shaping in the wave-form shaping unit **200**, the voltages of the output terminals VOUT1 and VOUT2 become respectively 0 V and 15 V.

[**0070**] According to the level conversion circuit **100** in the liquid crystal display apparatus of this fourth embodiment according to the present invention, the low amplitude voltage signals having 3.3 V and 0 V which are supplied to the input terminals VIN1 and VIN2 can be converted to the high amplitude voltage signals having 0 V and 15 V.

[**0071**] **FIG. 6** shows a circuitry construction view showing a level conversion circuit in a liquid crystal display apparatus of a fifth embodiment according to the present invention and shows a multi-input type level conversion circuit. The level conversion circuit of this fifth embodiment according to the present invention shown in **FIG. 6** is one in which the level conversion unit of the second embodiment according to the present invention shown in **FIG. 3** is formed with a multi-input type level conversion circuit.

[**0072**] A level conversion circuit **500** of this fifth embodiment according to the present invention is constituted of a N number input transistors **511**-**51**N, a N number load transistors **521**-**52**N and bias use transistors **531** and **541**. The respective source electrodes of the input transistors **511**-**51**N is connected to a N number input terminals V**11**-VI(N) and the respective drain electrodes of the input transistors **511**-**51**N is connected to the respective drain electrodes of the N number load transistors **521**-**52**N and to a N number output terminals Vo**1**-VO(N).

[**0073**] In the level conversion circuit **500** of this fifth embodiment according to the present invention, by adding two transistors of the input transistor and the load transistor to the level conversion circuit **500** an effect in which the input number can be increased.

[**0074**] **FIG. 7** shows one embodiment of a logic input circuit to which the level conversion circuit according to the present invention is adopted. The logic input circuit of this embodiment according to the present invention is constituted of the differential input type level conversion circuit **100**, the multi-input type level conversion circuit **500**, and a latch circuit unit **600** comprised of a N number latch circuits **611**-**61**(N).

[**0075**] Herein, in the differential input type level conversion circuit **100**, differential clock signals CK**1** and CK**2** having the low voltage amplitude are inputted and differential clock signals which are converted to the high voltage amplitude are outputted to the latch circuits **611**-**61**N. In the multi-input type level conversion circuit **500**, a N number data signals D**1**-D(N) having the low voltage amplitude are inputted and the data signals D**1**-D(N) which are converted to the high voltage amplitude are outputted to the respective latch circuits **611**-**61**N.

[**0076**] In the respective latch circuits of the latch circuit unit **600**, a clock signal having the high voltage amplitude and a data signal having the high voltage amplitude are inputted and the respective latch circuits is operated, and then a N number latch data O**1**-O(N) are outputted.

[**0077**] **FIG. 8** is a system construction example showing a liquid crystal display apparatus of one embodiment according to the present invention. This system of the liquid crystal display apparatus is constituted of an image signal generation apparatus **80**, an image signal processing circuit **60**, a timing control circuit **70**, and a liquid crystal display panel **10**.

[**0078**] Herein, the liquid crystal display panel **10** is constituted of a display unit **20** which is comprised of a plural pixel elements arranged with a matrix form, a signal circuit **30** and a scanning circuit **40** for driving these pixel elements,

a differential input type level conversion circuit **700**, a multi-input type level conversion circuits **500***a* and **500***b*, and a data latch circuit **600**.

[**0079**] Among these construction elements, the differential input type level conversion circuit **700** is constituted of the level conversion unit **100** and the wave-form shaping unit **200** which are explained as from the first embodiment to the fourth embodiment according to the present invention. The multi-input type level conversion circuits **500***a* and **500***b* correspond to the multi-input type level conversion circuit **500** which is explained as the fifth embodiment according to the present invention and further the data latch circuit **600** corresponds to the latch circuit unit **600** shown in **FIG. 7**, respectively.

[**0080**] The operation of the system of the liquid crystal display apparatus constituted in above will be explained. In the image signal generation apparatus **80**, an image signal **81** is outputted to the image signal conversion circuit **60**, and a clock signal **85**, a horizontal synchronization signal **86** and a vertical synchronization signal **87** are inputted to the timing control circuit **70**, respectively.

[**0081**] In the image signal conversion circuit **60**, a signal frequency of the inputted image signal **81** is lowered according to a serial-parallel conversion processing, and a n-parallel image signals D1-Dn are formed, and further these image signals D1-Dn are outputted to the multi-input type level conversion circuit **500***a* of the liquid crystal display panel **10**. These image signals D1-Dn are converted to the high amplitude signals according to the multi-input type level conversion circuit **500***a* and are stored into the data latch circuit **600**. The data latch circuit **600** output these stored vidual signals having the high amplitude HD1-HDn into the signal circuit **30**.

[**0082**] On the other hand, in the timing control circuit **70**, in accordance with the inputted clock signal **85**, the inputted horizontal synchronization signal **86** and the inputted vertical synchronization signal **87**, a clock signal **71** for taking into the image signals D1-Dn is outputted to the differential input type level conversion circuit **700** of the liquid crystal display panel **10** and further control signals **72-75** and the scanning circuit **40** for driving the signal circuit **30** are outputted into the multi-input type level conversion circuit **500***b* of the liquid crystal display panel **10**.

[**0083**] The differential input type level conversion circuit **700** converts the clock signal **71** to the high amplitude clock signal and output the converted clock signal to the data latch circuit **600**. The multi-input type level conversion circuit **500***b* converts the control signals **72-75** to the amplitude signals and a clock signal HCK for controlling the signal circuit **30**, a start signal HST, a clock signal VCK for controlling the scanning circuit **40**, and a start signal VST are outputted. The display unit **20** is controlled in accordance with the outputs of the signal circuit **20** and the scanning circuit **40** and displays the images which correspond to the image signals D1-Dn.

[**0084**] In the liquid crystal display apparatus constituted in above, the level conversion circuit comprised of the level conversion unit **100** and the wave-form shaping unit **200** which are shown in from the first embodiment to the fourth embodiment according to the present invention and the multi-input type level conversion circuit **500** shown in the fifth embodiment according to the present invention are employed.

[**0085**] Accordingly, the input of the liquid crystal display panel **10** can be formed with the low amplitude, the output circuits of the image signal processing circuit **60** and also the timing control circuit **70** can be constituted simply. Further, an unnecessary radiation of an electromagnetic wave can be reduced.

[**0086**] Further, in the embodiments according to the present invention the examples using TFT are exemplified, however, it is possible to obtain the same effects using the mono-crystallization silicon form MOS transistor. Further, the transistor according to the present invention can be obtained the same effects when the N conductive type transistor and the P conductive type transistor are reversed.

[**0087**] Further, according to the bias power supply of the level conversion circuit, since the drain current operation point of the input transistor and the drain current operation point of the load transistor can be formed with the high current, the high speed operation in the level conversion circuit can be attained and further the size of the transistor can be reduced.

[**0088**] Further, since the level conversion circuit is constituted using only the transistors, the level conversion circuit can be manufactured easily, further since the current of the load transistor is controlled according to the bias use transistor and the output voltage can be generated through the above stated current and the resistance of the input transistor, the fluctuation of the output voltage against to the fluctuation of the characteristic of the transistor can be restrained, as a result the yield on the manufacture of the level conversion circuit can be heightened.

[**0089**] The level conversion circuit according to the present invention is used as both of the signal circuit and the scanning circuit for driving the pixel elements of the display unit of the liquid crystal display apparatus. Of course, the level conversion circuit according to the present invention can use as one of the signal circuit and the scanning circuit.

What is claimed is:

1. In a liquid crystal display apparatus comprising a display unit having plural matrix form arranged pixel elements, a signal circuit for driving said plural pixel elements, and a scanning circuit, wherein

said signal circuit and said scanning circuit have a level conversion circuit;

said level conversion circuit has a first transistor and a second transistor in which a respective gate electrodes of said first transistor and said second transistor is connected to a first bias voltage power supply, and a first resistor and a second resistor which are connected between a respective drain electrodes of said first transistor and said second transistor and a power supply;

to a respective source electrodes of said first transistor and said second transistor, pixel element drive signals having a mutually different polarity and having a low amplitude are inputted; and

from said respective drain electrodes of said first transistor and said second transistor, pixel element drive signals having a mutually different polarity and having a high amplitude are outputted.

* * * * *

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申请(专利权)人(译)	SATO HIDEO 郎三上 影山HIROSHI TATSUYA大久保		
当前申请(专利权)人(译)	SATO HIDEO 郎三上 影山HIROSHI TATSUYA大久保		
[标]发明人	SATO HIDEO MIKAMI YOSHIRO KAGEYAMA HIROSHI TATSUYA OHKUBO		
发明人	SATO, HIDEO MIKAMI, YOSHIRO KAGEYAMA, HIROSHI TATSUYA, OHKUBO		
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摘要(译)

本发明提供一种液晶显示装置，其具有能够获得高速操作并且还能够获得小晶体管容量的电平转换电路。在液晶显示装置中，提供了用于驱动显示单元的像素元件的信号电路和扫描电路。电平转换电路由第一和第二晶体管111和112以及第三和第四晶体管121和122构成，其中各个栅电极连接到第一偏置电压电源，第三和第四晶体管121和122中连接有相应的栅电极第二偏压电源和各个源极连接到电源。