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(54) **LIQUID CRYSTAL DISPLAY DEVICE**

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(57) **ABSTRACT**

A liquid crystal display device including an image line drive circuit having an amplifier circuit for outputting an image voltage to an image line. The amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal or the non-inverting input terminal. The switching unit switches, according to a switching control signal input every two display lines, one of the two input terminals of the amplifier circuit to an inverting input terminal and the other of the two input terminals to a non-inverting input terminal or switches one of the two input terminals of the amplifier circuit to the non-inverting input terminal and the other of the two input terminals to the inverting input terminal.

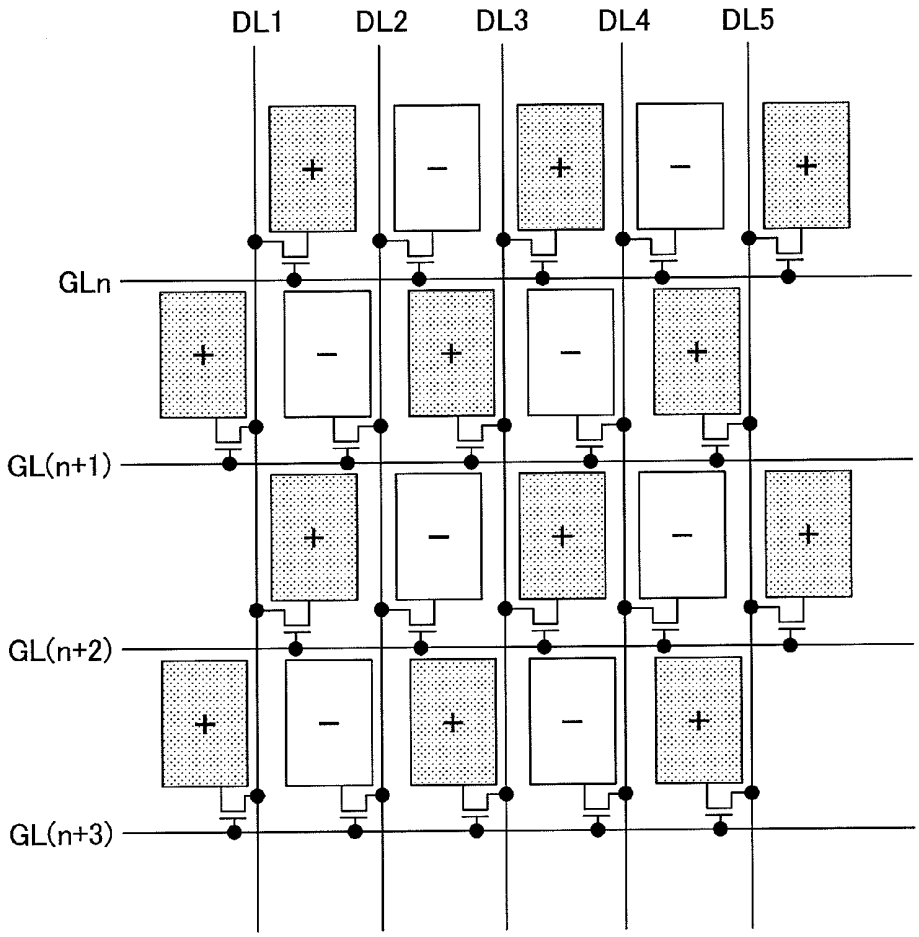


FIG.1

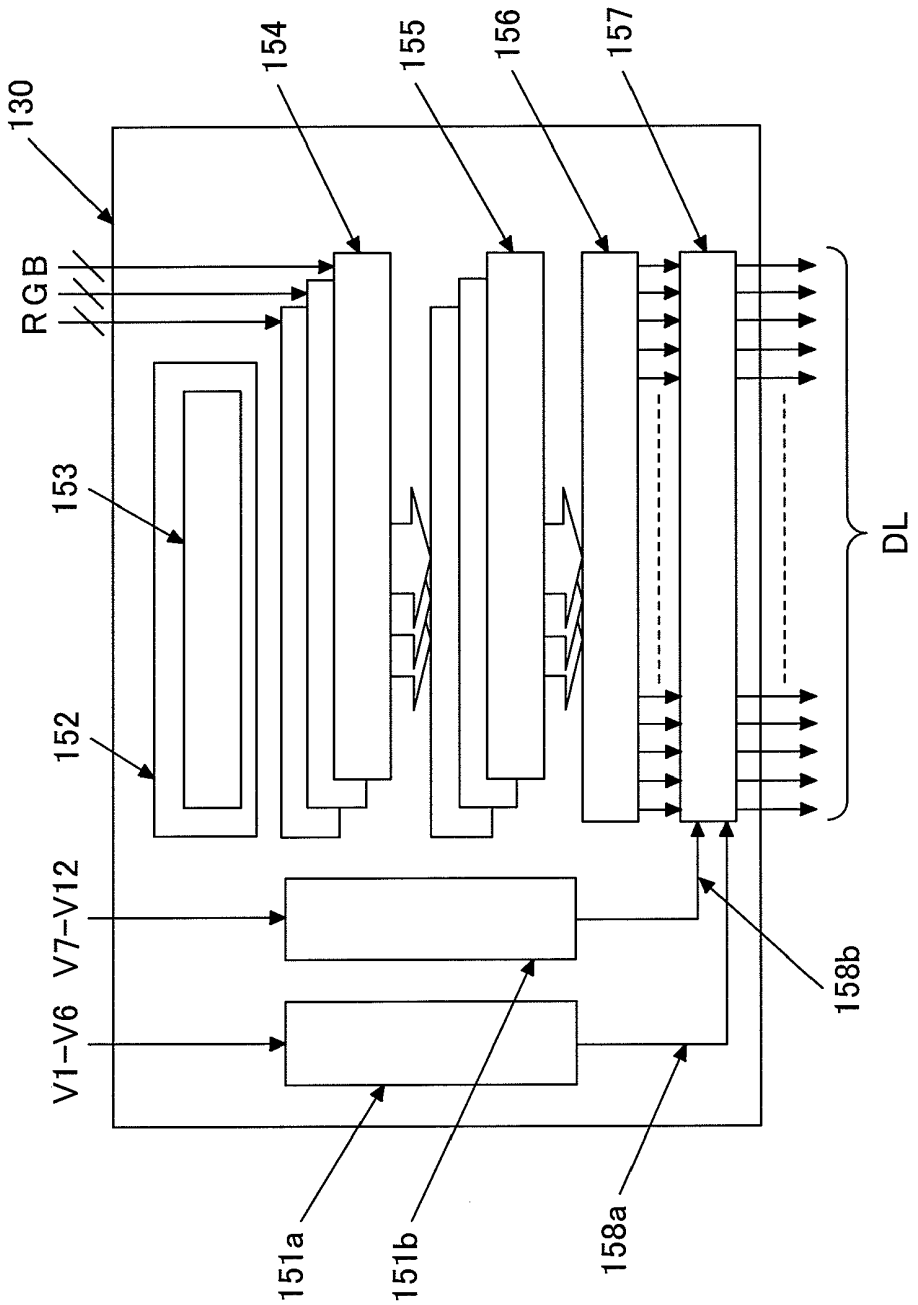

130
154
155
156
157
RGB
153
152
V7-V12
V1-V6
DL
158b
151a
151b
158a

FIG.2

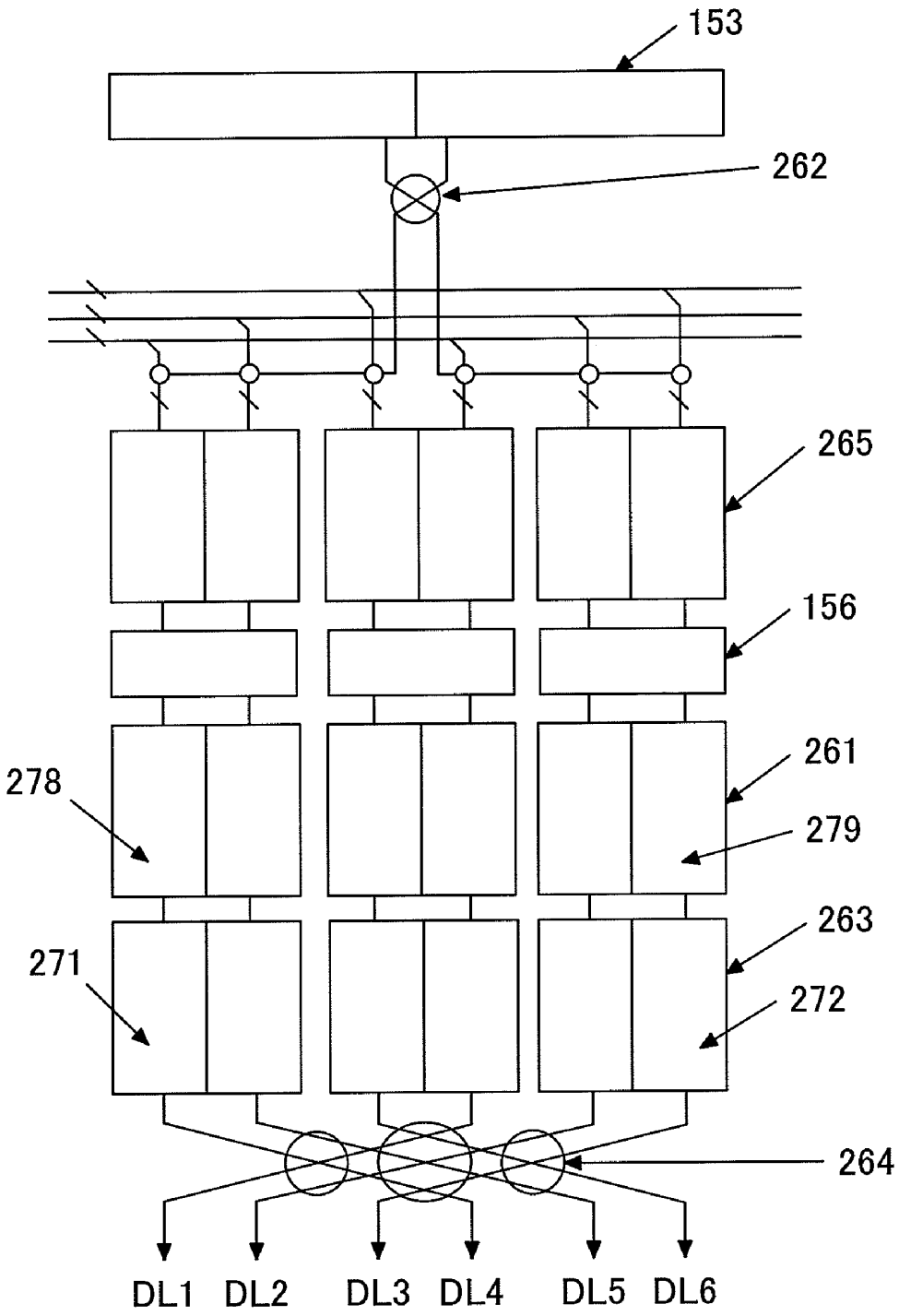

153
262
265
156
261
278
279
263
271
272
264
DL1
DL2
DL3
DL4
DL5
DL6

FIG.3

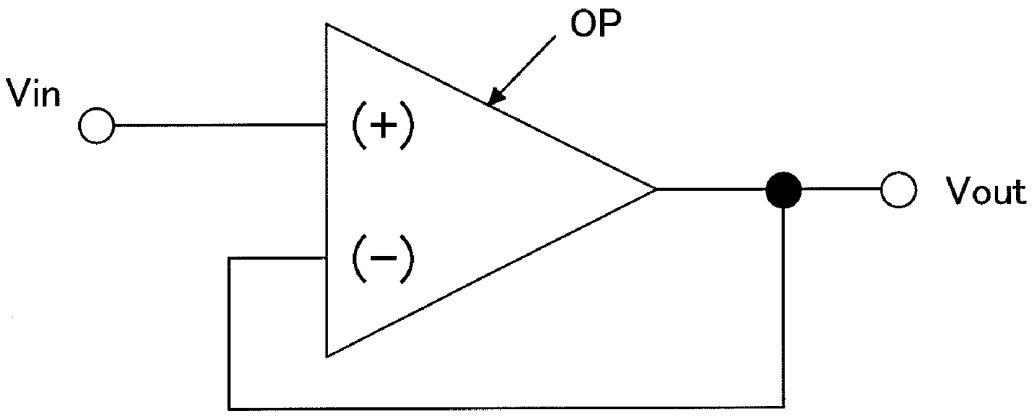


FIG.4

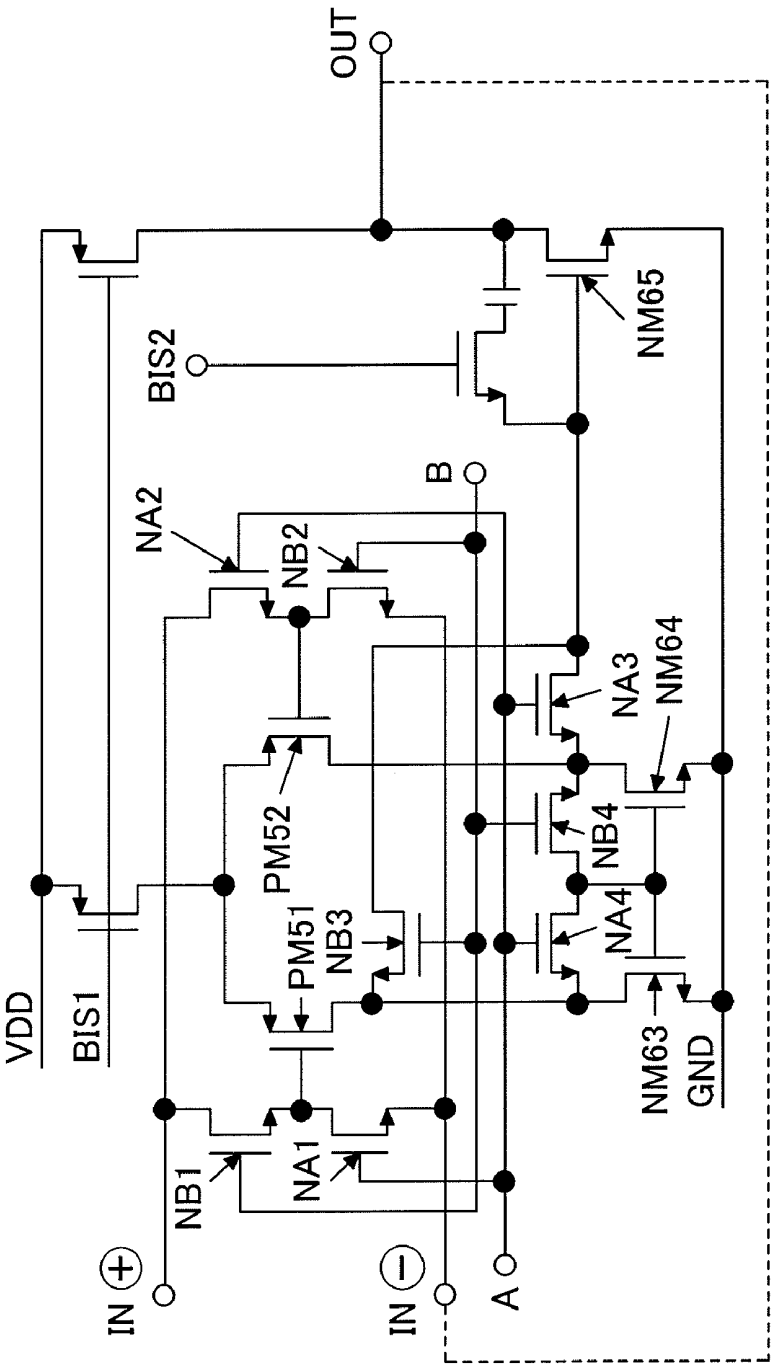
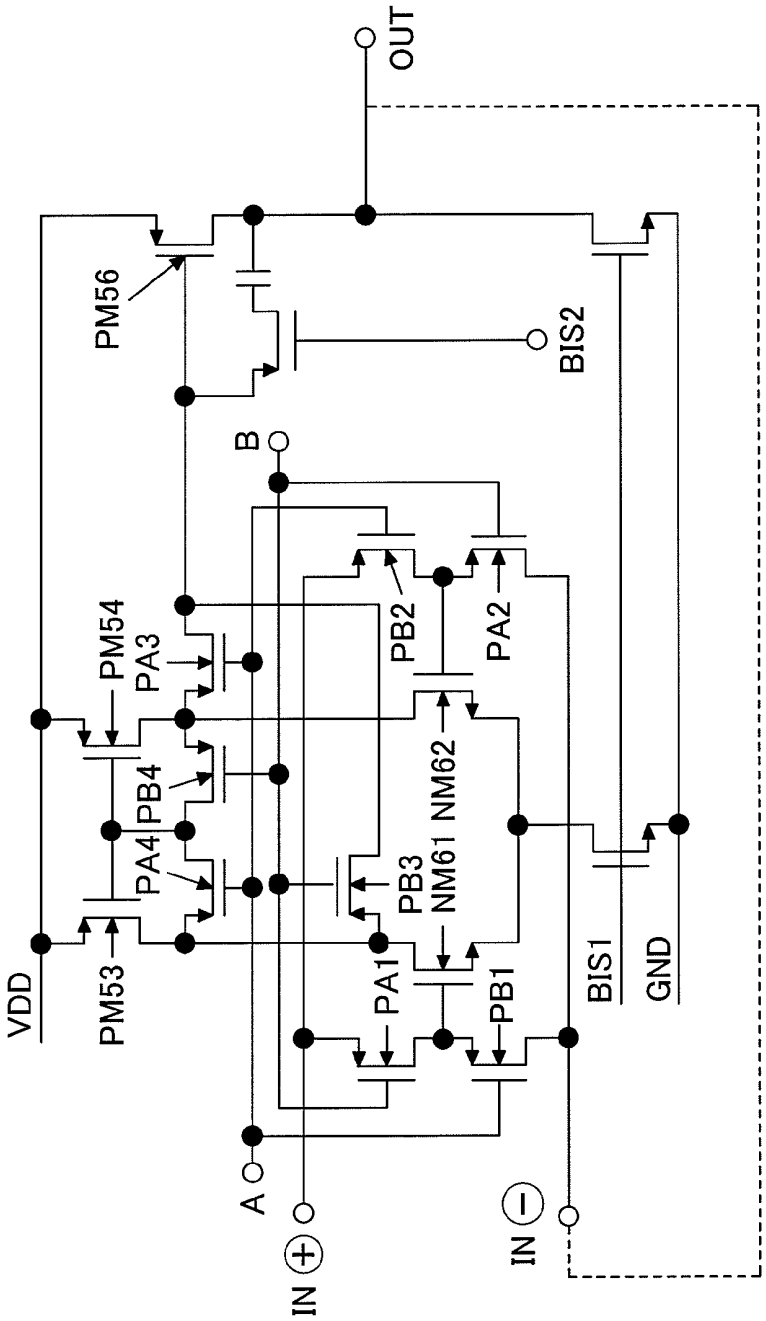

OUT
BIS2
NM65
B
NA2
NB2
NA3
NM64
PM52
NB4
PM51
NB3
NA4
VDD
BIS1
NM63
GND
NB1
NA1
IN ⊕
IN ⊖
A

FIG.5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PM56
BIS2
B
PM54
PA3
PB2
PA2
PB4
PA4
PB3
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VDD
PA1
PB1
BIS1
GND
A
IN ⊕
IN ⊖

FIG.6

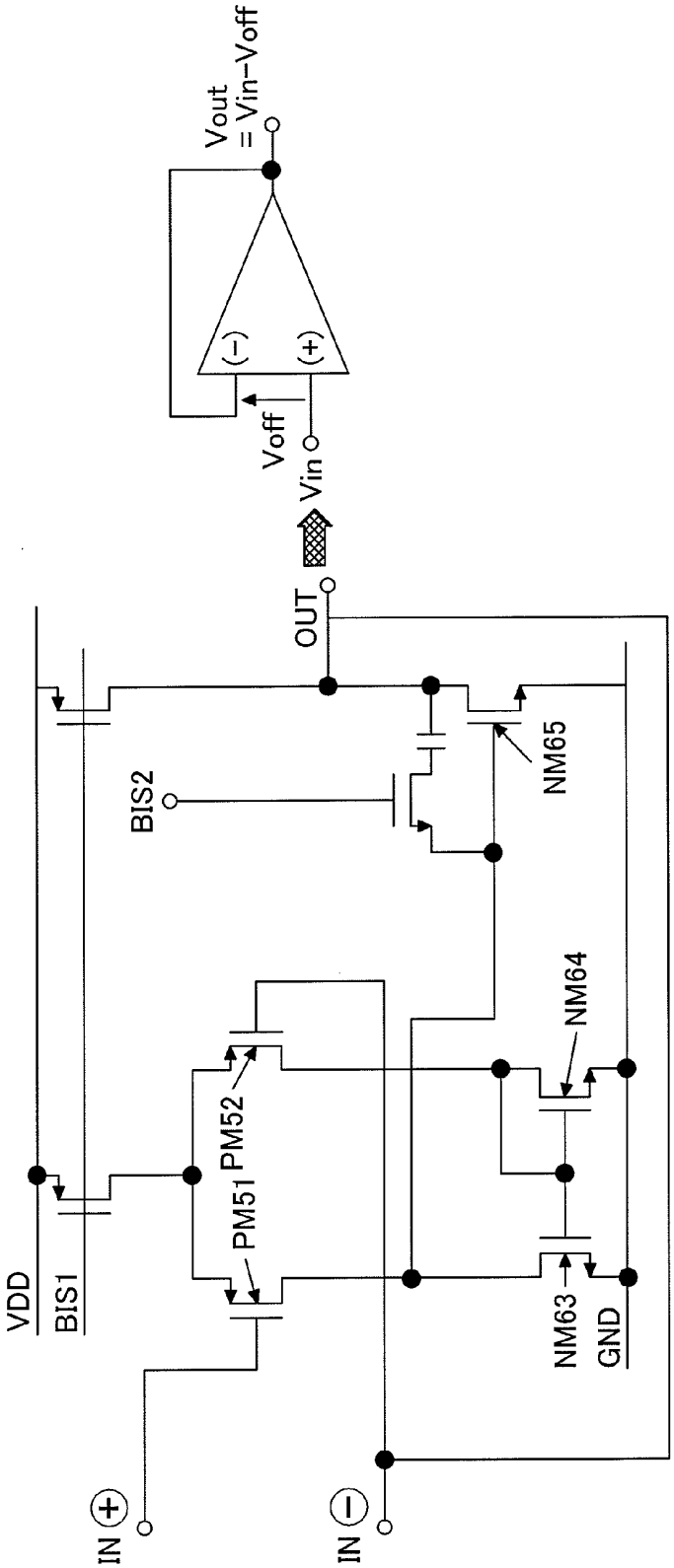

Vout
= Vin−Voff
(−)
(+)
Voff
Vin
OUT
BIS2
NM65
NM64
PM52
PM51
VDD
BIS1
NM63
GND
IN ⊕
IN ⊖

FIG.7

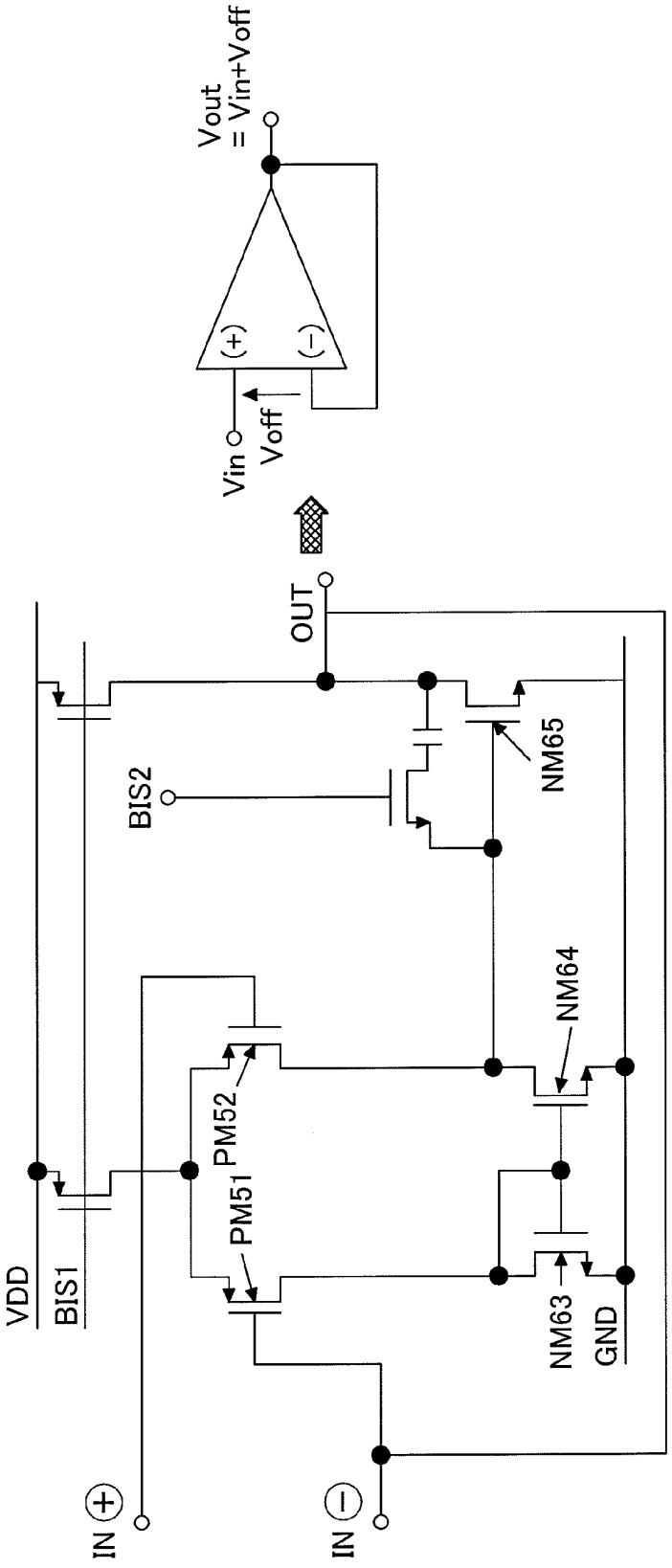

Vout
= Vin+Voff
(+)
(-)
Vin
Voff
OUT
BIS2
NM65
NM64
PM52
PM51
VDD
BIS1
NM63
GND
IN ⊕
IN ⊖

FIG.8A

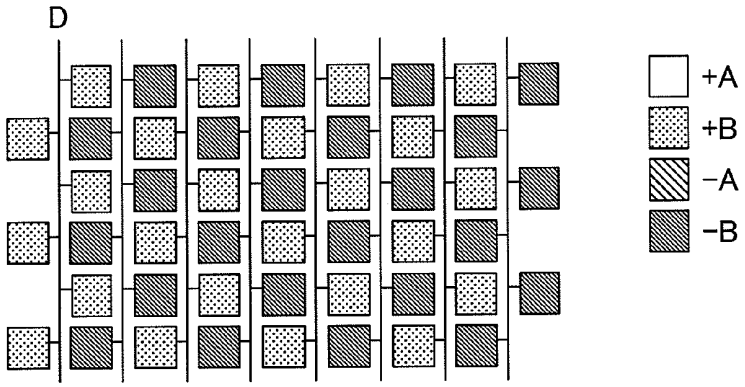


FIG.8B

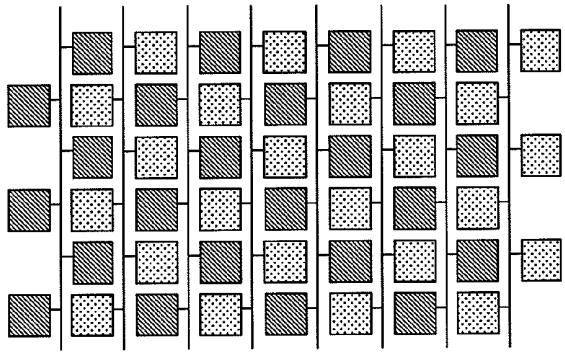


FIG.8C

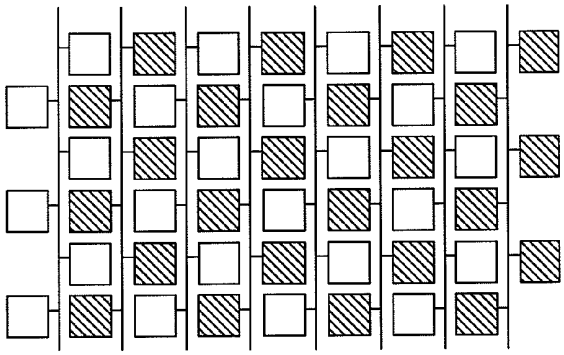


FIG.8D

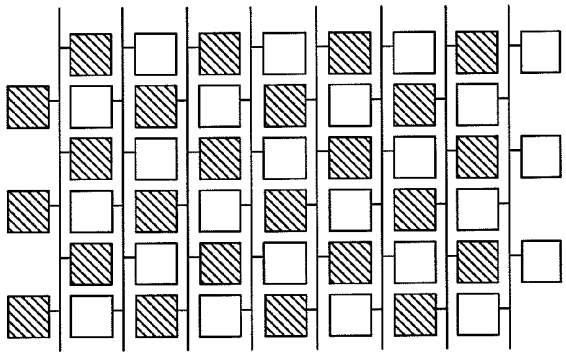


FIG.9A

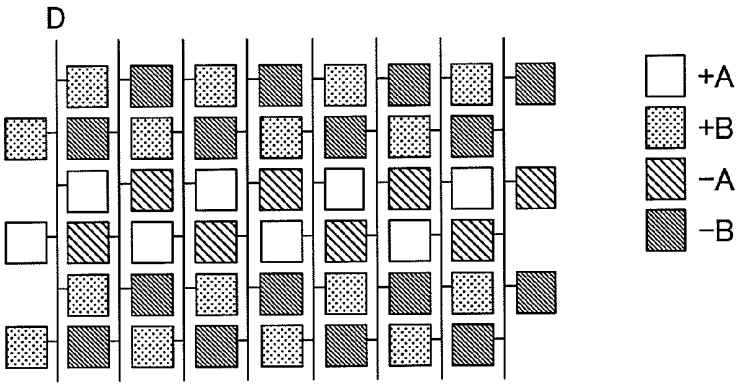


FIG.9B

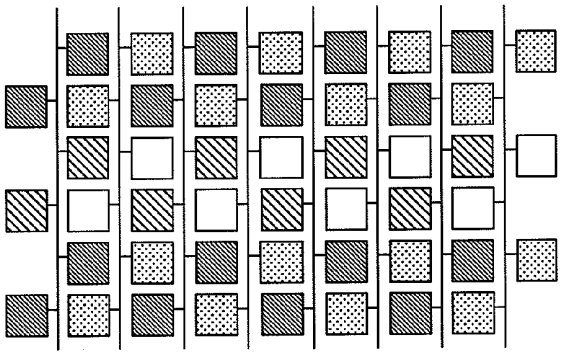


FIG.9C

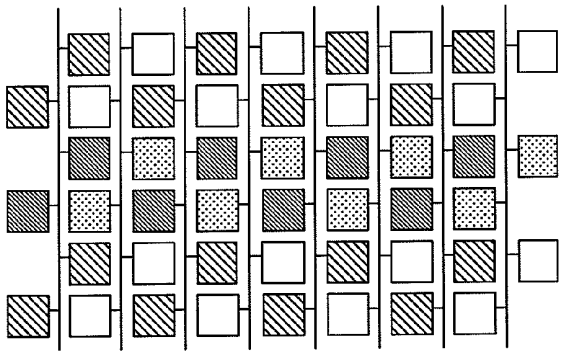


FIG.9D

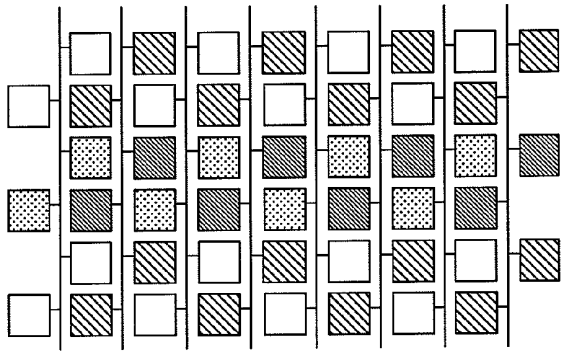


FIG.10A

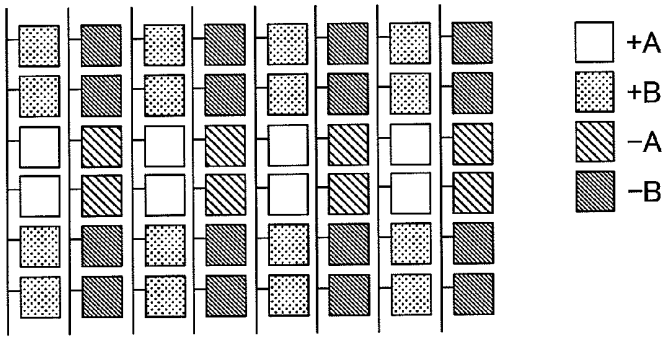


FIG.10B

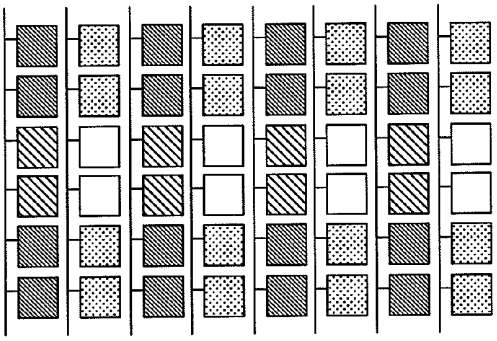


FIG.10C

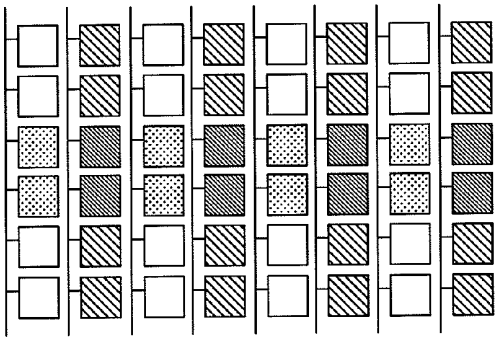


FIG.10D

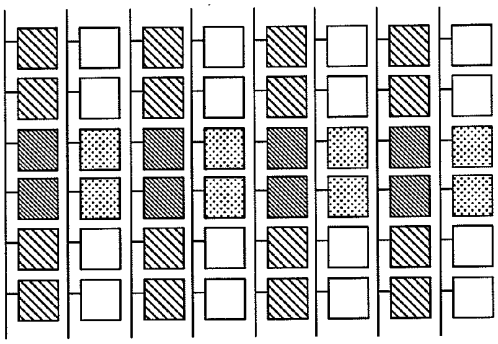


FIG.11

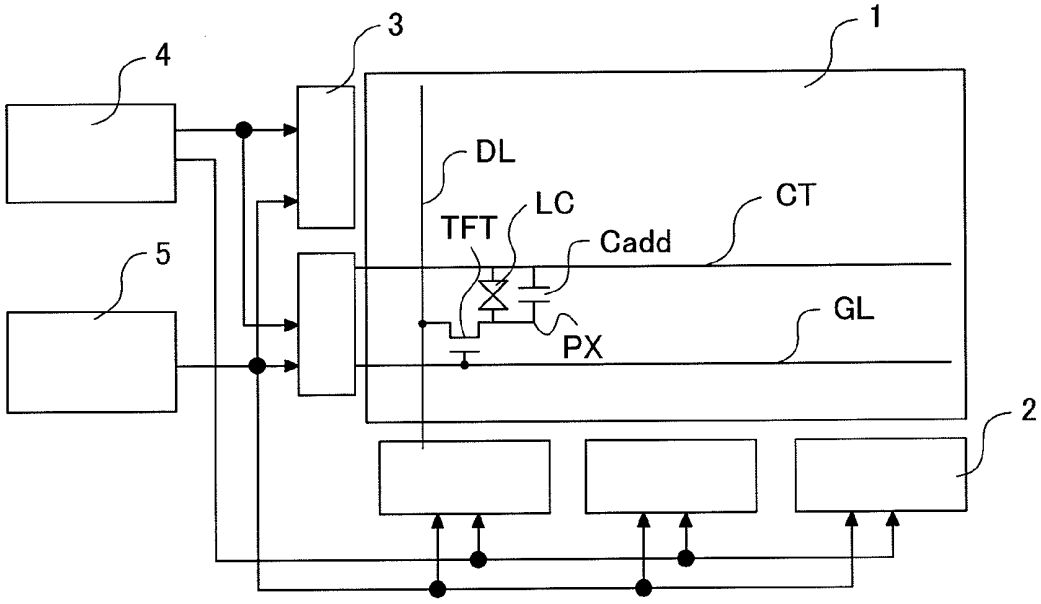


FIG.12

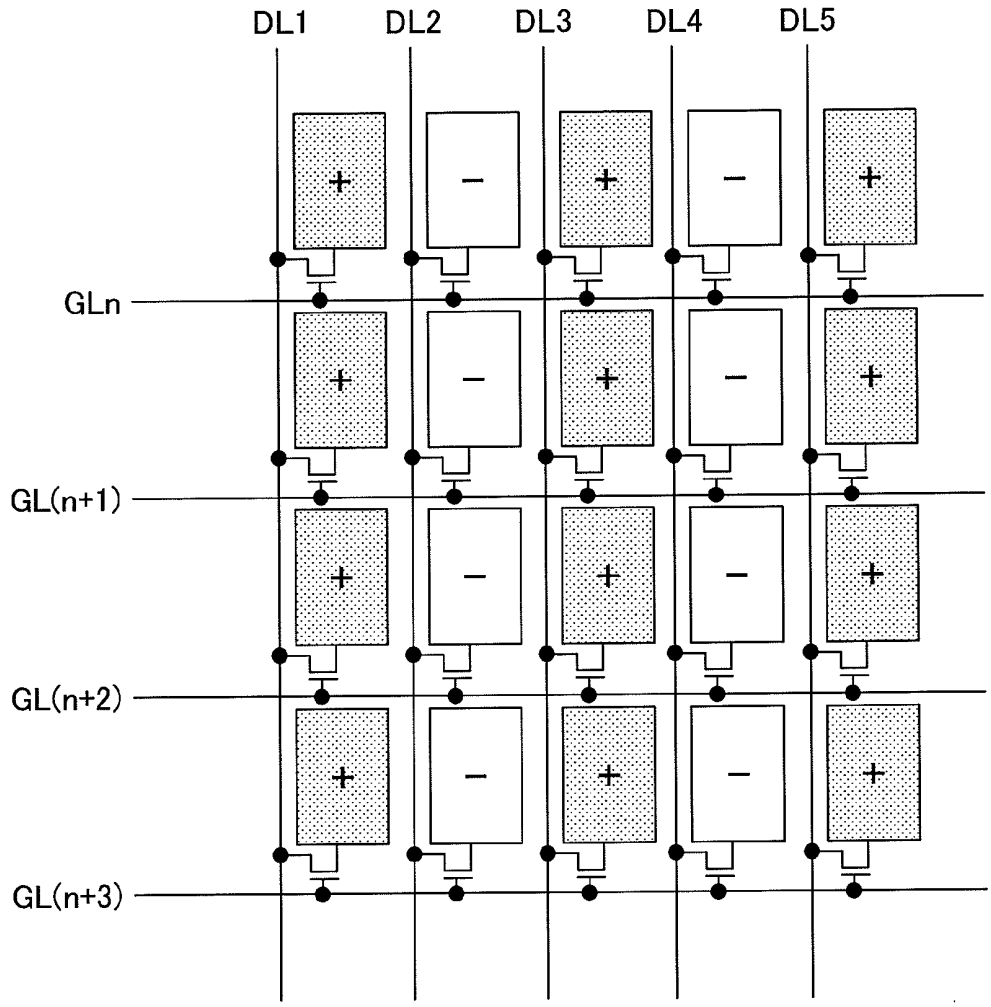
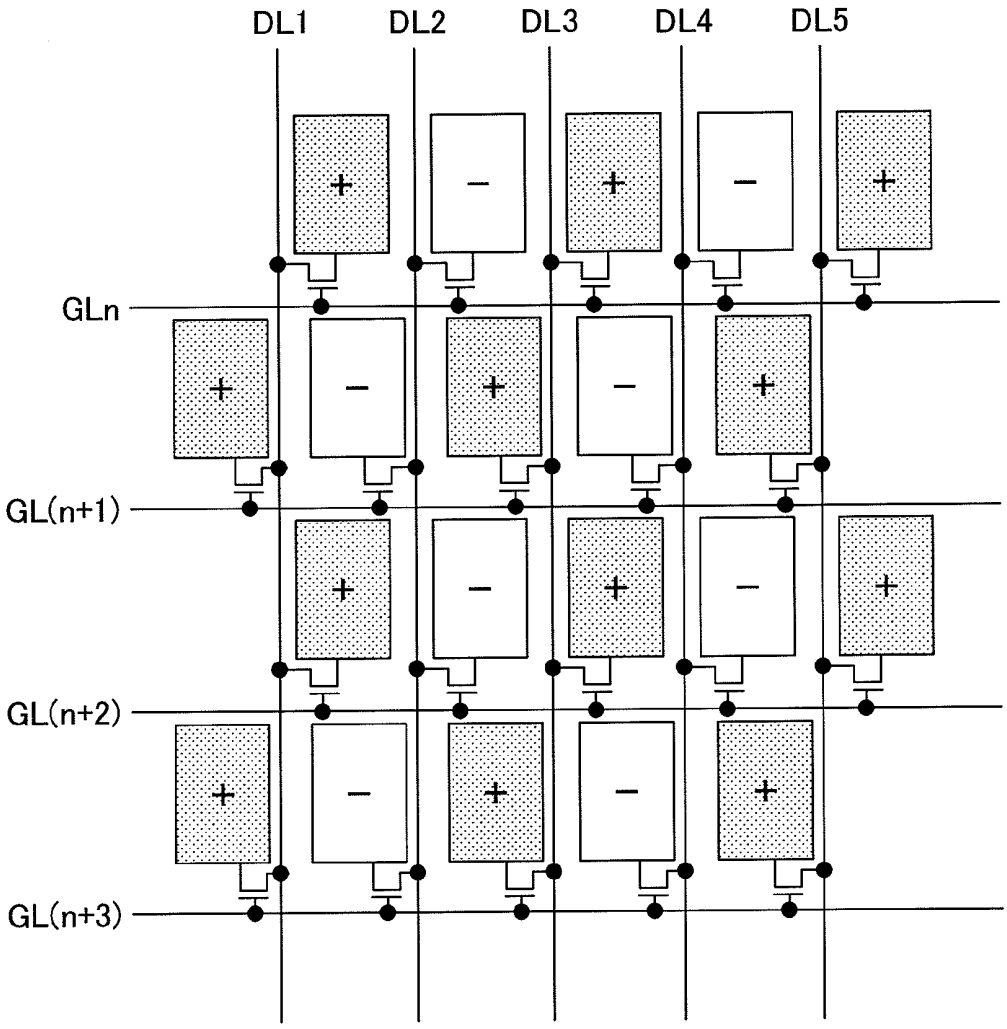


FIG.13



LIQUID CRYSTAL DISPLAY DEVICE

CLAIM OF PRIORITY

[0001] The present application claims priority from Japanese Application JP 2007-097033 filed on Apr. 3, 2007, the content of which is hereby incorporated by reference into this application.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device, and more specifically to a technique effective when applied to a drain driver for a liquid crystal display device capable of multi-gray-scale display.

[0004] 2. Description of the Related Art

[0005] A liquid crystal display module is used as a high-definition color monitor for a computer and other information technology devices or as a display device for a TV receiver.

[0006] The liquid crystal display module generally has a so-called liquid crystal display panel having a liquid crystal layer held between two (a pair of) substrates, at least one of which is made of transparent glass or the like, in which voltages are selectively applied to various electrodes of sub-pixels formed on the liquid crystal display panel to turn on or off particular sub-pixels. The display module is excellent in contrast performance as well as in high-speed display performance.

[0007] FIG. **11** is a block diagram illustrating a schematic configuration of a liquid crystal display module based on the conventional technology.

[0008] The liquid crystal display module shown in FIG. **11** has a liquid crystal display panel **1**, a drain driver **2**, a gate driver **3**, a display control circuit **4**, and a power circuit **5**.

[0009] The drain driver **2** and the gate driver **3** are provided in peripheral portions of the liquid crystal display panel **1**. The gate driver **3** comprises a plurality of gate drivers ICs provided on one edge of the liquid crystal display panel **1**. The drain driver **2** comprises a plurality of drain drivers ICs provided on another edge of the liquid crystal display panel **1**.

[0010] The display control circuit **4** performs timing control appropriate for display on the liquid crystal display panel **1**, such as AC-conversion of data, on display signals received from a display signal source (host side) such as a personal computer or a TV receiver circuit to convert the signals to display data in a desired display format. The display control circuit **4** then inputs the display data to the gate driver **3** and to the drain driver **2** together with synchronization signals (clock signals). The power circuit **5** generates various types of voltages necessary for the liquid crystal display module.

[0011] In FIG. **11**, reference symbol DL denotes an image line (also referred to as a drain line or source line), GL denotes a scanning line (also referred to as a gate line), and PX denotes a pixel electrode for each of red, green, and blue colors. Also, reference symbol CT denotes an opposite electrode (also referred to as a common electrode), LC denotes a liquid crystal capacitor equivalently showing a liquid crystal layer, and Cadd denotes a storage capacitor between the opposite electrode (CT) and the pixel electrode (PX).

[0012] In the liquid crystal display panel **1** shown in FIG. **11**, drain electrodes of thin-film transistors (TFT) for sub-pixels arrayed in the column direction are each connected to the image lines (DL). The image lines (DL) are each connected to the drain driver **2** for supplying an image voltage corresponding to the display data to the sub-pixels arrayed in the column direction.

[0013] The gate electrodes of thin-film transistors (TFT) in the sub-pixels arrayed in the row direction are each connected to the scanning lines (GL). Each of the scanning lines (GL) is connected to the gate driver **3** for supplying a scanning voltage (positive or negative bias-voltage) to a gate of each thin-film transistor (TFT) for one horizontal scanning time.

[0014] The gate driver **3** supplies a scanning voltage to the scanning line (GL) based on control by the display control circuit **4**. The drain driver **2** supplies an image voltage to the image line (DL) for displaying an image based on control by the display control circuit **4**.

[0015] When an image is to be displayed on the liquid crystal display panel **1**, the gate driver **3** selects a scanning line (GL) scanning from top to bottom (or vice versa). While a particular scanning line (GL) is being selected, the drain driver **2** also supplies an image voltage corresponding to the display data to an image line to apply the voltage to a pixel electrode (PX).

[0016] The voltage supplied to the image line (DL) is applied via a thin-film transistor (TFT) to the pixel electrode (PX). Finally an electric charge is charged to the storage capacitor (Cadd) and the liquid crystal capacitor (LC) for controlling liquid crystal molecules to display the image.

[0017] The drain driver **2** has a multiple-gray-scale voltage generator circuit, a gray-scale voltage selector circuit for selecting one gray-scale voltage corresponding to the display data from among the multiple-gray-scale voltages generated by the multiple-gray-scale voltage generator circuit, and an amplifier circuit to which the one gray-scale voltage selected by the gray-scale voltage selector circuit is input.

[0018] Recently, in the field of liquid crystal display modules, the number of scales in the multiple gray-scale display has increased from 64-gray-scale display to 256-gray-scale display, and a voltage width of one gray-scale (namely, a potential difference between adjoining gray-scale voltages generated by the multiple-gray-scale voltage generator circuit) has become smaller.

[0019] On the other hand, in its amplifier circuit, an offset voltage is generated due to characteristic variation of active elements constituting the amplifier circuit. When an offset voltage is generated in the amplifier circuit, an error occurs in an output voltage from the amplifier circuit, and the output voltage from the amplifier circuit thus differs from a target value (a proper gray-scale voltage). Accordingly, a black or white stripe/stripes is/are generated in a display screen displayed on the liquid crystal display panel **1**, which leads to a problem of degraded display quality.

[0020] As a solution to the above problem, a method is known in which the offset voltage is canceled by switching one of two input terminals of the amplifier circuit to an inverting input terminal and the other to a non-inverting input terminal or vice versa with the use of a switch control signal (the method is hereinafter referred to as an "offset-voltage canceling method based on the chopper control system) (Refer to Japanese patent No. 3595153).

[0021] A prior art document related to the present invention is given below:

[0022] Japanese patent No. 3595153

SUMMARY OF THE INVENTION

[0023] Generally, when the same voltage (DC voltage) is applied to a liquid crystal layer for a long time, an inclination of the liquid crystal layer is fixed. As a result, this causes a residual image phenomenon, shortening the life duration of the liquid crystal layer. To prevent this, in a liquid crystal display module, a voltage applied to the liquid crystal layer is converted to an alternating voltage at regular time intervals. In other words, a voltage applied to a pixel electrode (PX) is changed to the positive voltage side or the negative voltage side at regular time intervals based on a voltage applied to an opposite electrode (CT).

[0024] There has been known the common symmetry method as an AC-drive method in which an AC voltage is applied to the liquid crystal layer. In the common symmetry method, a voltage applied to an opposite electrode (CT) is fixed at a certain level; based on this, a voltage applied to a pixel electrode (PX) is inverted alternately from the positive side to the negative side. As examples of the common symmetric method, there has been known the dot inversion method or the N-line inversion method.

[0025] Recently, for the purpose of cost reduction, the number of output lines from one drain driver has been increased to reduce the number of drain drivers used in a liquid crystal display module. When the dot inversion method is employed as an AC-drive system for a liquid crystal display module under the above condition, an amount of heat generated by each drain driver disadvantageously increases.

[0026] As an AC-drive system for a liquid crystal display module, therefore, the column-by-column inversion method as shown in FIG. **12** is employed favorably. In this column-by-column inversion method, in a particular frame period, an image voltage with positive polarity (or negative polarity) is supplied from the drain driver **2** to even-number-th image lines (DL), and at the same time an image voltage with negative polarity (or positive polarity) is supplied to odd-number-th image lines (DL). Then in the next frame period, an image voltage with negative polarity (or positive polarity) is supplied from the drain driver **2** to even-number-th image lines (DL), and at the same time an image voltage with positive polarity (or negative polarity) is supplied to odd-number-th image lines (DL).

[0027] Furthermore, there has been known the pseudo dot inversion method shown in FIG. **13** as an example of the column-by-column inversion method.

[0028] In the pseudo dot inversion method, pixel electrodes (PX) connected to one of the two adjoining image lines (DL) (for instance, DL**1**) via thin-film transistors (TFT) and those (PX) connected to the other image line (for instance, DL**2**) are arranged between the two adjoining image lines (DL) alternately in the direction in which the image lines (DL) extend.

[0029] Also, within one frame period, an image voltage with positive polarity is supplied to image lines DL**1**, DL**3**, and DL**5**, and at the same time an image voltage with negative polarity is supplied to image lines DL**2** and DL**4**. Accordingly, polarities of the image voltages supplied to sub-pixels are the same as those in the dot inversion method as shown in FIG. **13**. In FIG. **12** and FIG. **13**, squares with the sign (+) are pixel electrodes to which an image voltage with positive polarity is supplied, and squares with the sign (−) are pixel electrodes to which an image voltage with negative polarity is supplied.

[0030] In the column-by-column inversion method or in the pseudo dot inversion method described above, when the offset-voltage canceling method based on the chopper system is carried out every one frame period, flickering occurs on a display screen when a certain pattern is displayed, which disadvantageously degrades the display quality.

[0031] The present invention was made to solve the problems of the conventional technology as described above, and an object of the present invention is to provide a technique enabling prevention of flickering on a display screen in a liquid crystal display panel generated due to an offset voltage in an amplifier circuit of an image line drive circuit in a liquid crystal display device and improvement in display quality of the display screen.

[0032] The above-described and other objects and novel features of the present invention will be more clarified with reference to descriptions in the specification and the drawings attached hereto.

[0033] Of pieces of the invention disclosed herein, representative ones are briefly summarized below.

[0034] (1) The present invention provides, in one aspect, a liquid crystal display device comprising: a plurality of image lines; a plurality of scanning lines; a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and a image line drive circuit for supplying an image voltage to each of the image lines, in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

[0035] wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line; the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and the switching unit switches, according to a switching control signal input every two display lines, one of the two input terminals of the amplifier circuit to an inverting input terminal and the other of the two input terminals to a non-inverting input terminal or switches one of the two input terminals of the amplifier circuit to the non-inverting input terminal and the other of the two input terminals to the inverting input terminal.

[0036] (2) The present invention provides, in another aspect, a liquid crystal display device comprising: a plurality of image lines; a plurality of scanning lines; a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and an image line drive circuit for supplying an image voltage to each of the image lines, the plurality of thin-film transistors provided between two adjoining image lines along a direction in which the image lines extend having such an arrangement in which thin-film transistors connected to one of the two adjoining image lines and those connected to the other of the two adjoining image lines are alternately arranged, in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

[0037] wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line; the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and the switching unit switches, according to a switching control signal input every two display lines, one of the two input terminals of the amplifier circuit to an inverting input terminal and the other of the two input terminals to a non-inverting input terminal or switches one of the two input terminals of the amplifier circuit to the non-inverting input terminal and the other of the two input terminals to the inverting input terminal.

[0038] (3) In the liquid crystal display device described in (1) or (2) above, the image line drive circuit comprises: a data latch circuit for latching input display data; and a decoder circuit for selecting a gray-scale voltage based on the display data supplied from the data latch circuit, and the amplifier circuit outputs the gray-scale voltage selected by the decoder circuit as an image voltage to the image line.

[0039] (4) In the liquid crystal display device described in any of (1) to (3), a phase of the switching control signal is inverted every two frames.

[0040] (5) In the liquid crystal display device described in any of (1) to (3), a cycle of the switching control signal is twice as long as a horizontal scanning time.

[0041] (6) The present invention provides, in still another aspect, a liquid crystal display device comprising: a plurality of image lines; a plurality of scanning lines; a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and a image line drive circuit for supplying an image voltage to each of the image lines, in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

[0042] wherein: the image line drive circuit includes an amplifier circuit for outputting an image voltage to the image line; the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and an image voltage produced by adding an offset voltage to a gray-scale voltage and an image voltage produced by subtracting the offset voltage from the gray-scale voltage are supplied alternately via the image line to the thin-film transistor every two successive horizontal-scanning periods.

[0043] (7) The present invention provides, in still another aspect, a liquid crystal display device comprising: a plurality of image lines; a plurality of scanning lines; a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and an image line drive circuit for supplying an image voltage to each of the image lines, the plurality of thin-film transistors provided between two adjoining image lines along a direction in which the image lines extend having such an arrangement in which thin-film transistors connected to one of the two adjoining image lines and those connected to the other of the two adjoining image lines are alternately arranged, in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

[0044] wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line; the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and an image voltage produced by adding an offset voltage to a gray-scale voltage and an image voltage produced by subtracting the offset voltage from the gray-scale voltage are supplied alternately via the image line to the thin-film transistor every two successive horizontal-scanning periods.

[0045] Effects provided by the representative pieces of the invention disclosed herein can be briefly summarized as below.

[0046] With the liquid crystal display device according to the present invention, it is possible to prevent occurrence of flickering on a display screen of a liquid crystal display panel, which is attributed to an offset voltage in an amplifier circuit of an image line drive circuit, thereby improving display quality of the display screen.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047] FIG. **1** is a block diagram illustrating a schematic configuration of a drain driver of a liquid crystal display module according to an embodiment of the present invention;

[0048] FIG. **2** is a block diagram illustrating a configuration of the drain driver shown in FIG. **1**, centering on a configuration of an output circuit;

[0049] FIG. **3** is a diagram illustrating a voltage follower circuit using an operational amplifier;

[0050] FIG. **4** is a circuit diagram illustrating a basic circuit configuration of a low-voltage amplifier circuit in the drain driver according to the embodiment of the present invention;

[0051] FIG. **5** is a circuit diagram illustrating a basic circuit configuration of a high-voltage amplifier circuit in the drain driver according to the embodiment of the present invention;

[0052] FIG. **6** is a circuit diagram illustrating a circuit configuration of the lower-voltage amplifier circuit shown in FIG. **4** when a control signal (A) is at a low level while a control signal (B) is at a high level;

[0053] FIG. **7** is a circuit diagram illustrating a circuit configuration of the lower-voltage amplifier circuit shown in FIG. **4** when the control signal (A) is at a high level while the control signal (B) is at a low level;

[0054] FIGS. **8**A to **8**D are diagrams illustrating the polarity of an image voltage output from the drain driver to an image line when the pseudo dot inversion method is used as a AC-drive method for a liquid crystal display module;

[0055] FIGS. **9**A to **9**D are diagrams illustrating an AC-drive method for the liquid crystal display module according to an embodiment of the present invention;

[0056] FIGS. **10**A to **10**D are diagrams illustrating another example of the AC-drive method for the liquid crystal display module according to the embodiment of the present invention;

[0057] FIG. **11** is a block diagram illustrating a schematic configuration of a liquid crystal display module based on the conventional technology;

[0058] FIG. **12** is a diagram illustrating the column-by-column inversion method in the AC-drive method for a liquid crystal display module; and

[0059] FIG. **13** is a diagram illustrating the pseudo dot inversion method in the Ac-drive method for a liquid crystal display module.

DESCRIPTION OF REFERENCE NUMERALS AND SYMBOLS

[0060] **1**: Liquid crystal display panel
[0061] **2**, **130**: Drain driver
[0062] **4**: Display control circuit
[0063] **5**: Power circuit
[0064] **151***a*, **151***b*: Gray-scale voltage generator circuit
[0065] **152**: Control circuit
[0066] **153**: Shift register circuit
[0067] **154**: Input register circuit
[0068] **155**: Storage register circuit
[0069] **156**: Level shift circuit
[0070] **157**: Output circuit
[0071] **158***a*, **158***b*: Voltage bus line
[0072] **261**: Decoder circuit
[0073] **262**, **264**: Switch section
[0074] **263**: Amplifier circuit pair
[0075] **265**: Data latch section
[0076] **271**: High-voltage amplifier circuit
[0077] **272**: Low-voltage amplifier circuit
[0078] DL: Image line (drain line)
[0079] GL: Scanning line (gate line)
[0080] PS: Pixel electrode
[0081] CT: Opposite electrode
[0082] TFT: Thin-film transistor
[0083] LC: Liquid crystal capacitor
[0084] Cadd: Storage capacitor
[0085] PM, PA, PB: PMOS transistor
[0086] NM, NA, NB: NMOS transistor

Detailed Description of the Preferred Embodiments

[0087] An embodiment of the present invention is described below in detail with reference to the accompanying drawings.

[0088] It is to be noted that in the drawings illustrating the embodiment, the same reference numerals are given to those having same the function without duplicating explanations.

[0089] As the schematic configuration of a TFT-system liquid-crystal-display module of the embodiment is the same as that of FIG. **11**, detailed explanations therefor are omitted.

[0090] FIG. **1** is a block diagram illustrating the schematic configuration of a drain driver of the liquid crystal display module of the embodiment. In FIG. **1**, reference numeral **130** denotes the drain driver, and the drain driver **130** comprises one semiconductor integrated circuit (LSI).

[0091] A positive-polarity gray-scale voltage generating circuit **151***a* generates a 256-gray-scale voltage with positive polarity based on 6-value gray-scale reference voltages (V**1**-V**6**) with positive polarity input from a power circuit **5** and outputs the gray-scale voltage to an output circuit **157** via a voltage bus line **158***a*. A negative-polarity gray-scale voltage generating circuit **151***b* generates a 256-gray-scale voltage with negative polarity based on 6-value gray-scale reference voltages (V**7**-V**12**) with negative polarity input from the power circuit **5** and outputs the gray-scale voltage to the output circuit **157** via a voltage bus line **158***b*.

[0092] A shift register circuit **153** in a control circuit **152** of the drain driver **130** generates a data latch signal for an input register circuit **154** based on a clock (CL**2**) input from a display control circuit **4** and outputs the signal to an input register circuit **154**.

[0093] The input register circuit **154** latches for existing output lines 8-bit display data for each color, in synchronization with the clock (CL**2**) input from the display control circuit **4**, based on the data latch signal input from the shift register circuit **153**.

[0094] A storage resister circuit **155** latches the display data in the input register circuit **154** according to a clock (CL**1**) input from the display control circuit **4**.

[0095] The display data fetched by the storage resister circuit **155** is input to the output circuit **157** via a level shift circuit **156**. The output circuit **157** selects a gray-scale voltage corresponding to the display data (a voltage associated with one gray-scale out of 256 gray scales) and outputs the voltage to respective image lines (DL) according to the 256-gray-scale voltage with positive polarity or the 256-gray-scale voltage with negative polarity.

[0096] FIG. **2** is a block diagram illustrating the configuration of the drain driver **130** shown in FIG. **1**, mainly the configuration of the output circuit **157**.

[0097] In the figure, reference numeral **153** denotes the shift register circuit in the control circuit **152** shown in FIG. **1**. Reference numeral **156** denotes the level shift circuit shown in the FIG. **1**. A data latch section **256** denotes the input register circuit **154** and the storage resister circuit **155** both shown in the FIG. **1**. Also, a decoder section (a gray-scale voltage selection circuit) **261**, an amplifier circuit pair **263**, a switch section (**2**) **264** switching an output of the amplifier circuit pair **263** comprise the output circuit **157** shown in the FIG. **1**, wherein a switch section (**1**) **262** and the switch section (**2**) **264** are controlled according to an AC-converting current signal (M). Further, DL**1**, DL**2**, DL**3**, DL**4**, DL**5**, and DL**6** denote a first, second, third, fourth, fifth, and sixth image line (DL), respectively.

[0098] In the drain driver **130** shown in FIG. **2**, a data latch signal input to the data latch section **265** (more precisely, the input register **154** shown in FIG. **1**) is switched by the switch section (**1**) **262** to input display data for each color to adjoining data latch sections **265** for each color.

[0099] The decoder section **261** comprises: a high-voltage decoder circuit **278** which selects a gray-scale voltage with positive polarity corresponding to display data output from each data latch section **265** (more precisely, the storage resister **155** shown in FIG. **1**) among 256-gray-scale voltages with positive polarity output from the gray-scale voltage generating circuit **151***a* via the voltage bus line **158***a*; and a low-voltage decoder circuit **279** which selects a gray-scale voltage with negative polarity corresponding to display data output from each data latch section **265** among 256-gray-scale voltages with negative polarity output from the gray-scale voltage generating circuit **151***b* via the voltage bus line **158***b*. These high-voltage decoder circuit **278** and low-voltage decoder circuit for **279** are provided for each pair of adjoining data latch sections **265**.

[0100] The amplifier circuit pair **263** comprises a high-voltage amplifier circuit **271** and a low-voltage amplifier circuit **272**. A gray-scale voltage with positive polarity generated in the high-voltage decoder circuit **278** is input to the high-voltage amplifier circuit **271**, and the high-voltage amplifier circuit **271** generates a gray-scale voltage with positive polarity.

[0101] A gray-scale voltage with negative polarity generated in the low-voltage decoder circuit **279** is input to the low-voltage amplifier circuit **272**, and the low-voltage amplifier circuit **272** outputs a gray-scale voltage with negative polarity.

[0102] In the column-by-column inversion method or in the pseudo dot inversion method, the polarities of adjoining gray-scale voltages for each color are opposite to each other. In addition, the high-voltage amplifier circuit **271** and the low-voltage amplifier circuit **272** in the amplifier circuit pair **263** are arranged in the order from a high-voltage amplifier circuit **271**, a low-voltage amplifier circuit **272**, another high-voltage amplifier circuit **271**, to another low-voltage amplifier circuit **272** (from left to right in FIG. **2**). Therefore, it is possible to output a gray-scale voltage with positive polarity or with negative polarity to each image line (DL) by switching data latch signals input to the data latch sections **265** with the switching section (**1**) **262** to input display data for each color to the adjoining data latch sections **265** for each color and at the same time by switching output voltages output from the high-voltage amplifier circuits **271** or the low-voltage amplifier circuits **272** with the switching section (**2**) **264** to output the voltages to the image lines (DL), to which gray-scale voltages for each color are output (for instance, to the first image line (D**1**) and the fourth image line (D**4**)).

[0103] In the conventional technology, the high-voltage amplifier circuit **271** and the low-voltage amplifier circuit **272** are each configured with a voltage follower circuit in which an inverting input terminal (−) of an operational amplifier (OP) is directly connected to an output terminal, and a non-inverting input terminal (+) thereof functions as an input terminal as shown in FIG. **3**. An operational amplifier (OP) used in the low-voltage amplifier circuit **272** is a differential amplifier circuit.

[0104] Generally, an operational amplifier (OP) has an offset voltage (Voff), however. When a basic amplifier circuit of the operational amplifier (OP) is, for instance, a differential amplifier circuit, the offset voltage (Voff) is generated due to a subtle imbalance in the symmetric property of an MOS transistor in the input stage or that constituting an active load circuit.

[0105] When the operational amplifier (OP) is an ideal one without an offset voltage (Voff), its input voltage (Vin) is equal to its output voltage (Vout) (Vin=Vout). In contrast, when the operational amplifier has an offset voltage (Voff), the input voltage (Vin) is not equal to the output voltage (Vout), and the output voltage (Vout) is equal to the sum of the input voltage (Vin) and the offset voltage (Voff) (Vout=Vin+Voff).

[0106] In the conventional type of liquid crystal display module in which the voltage follower circuit as shown in FIG. **8** is used as the high-voltage amplifier circuit (denoted by reference numeral **271** in FIG. **2**) and the low-voltage amplifier circuit (denoted by reference numeral **272** shown in FIG. **2**) in the output circuit (denoted by reference numeral **157** in FIG. **1**) of the drain driver, therefore, an input voltage and an output voltage are not equal to each other in the voltage follower circuit. That is, a liquid crystal drive voltage output from the voltage follower circuit to the drain signal line (DL) is the sum of a gray-scale voltage input to the voltage follower circuit and an offset voltage in the operational amplifier. Because of the above configuration, black or white vertical stripes are generated in a display screen displayed on the liquid crystal panel of the conventional-type liquid crystal display module.

[0107] FIG. **4** is a circuit diagram illustrating a basic circuit configuration of the low-voltage amplifier circuit **272** in the drain driver **130** of the embodiment; FIG. **5** is a circuit diagram illustrating a basic circuit configuration of the high-voltage amplifier circuit **271** in the drain driver **130** of the embodiment.

[0108] The low-voltage amplifier circuit **272** shown in FIG. **4** additionally includes: switching transistors (NA**1** and NB**1**) for connecting a gate electrode (control electrode) of a PMOS transistor (PM**51**) in the input stage to a (+) input terminal or a (−) input terminal; switching transistors (NA**2** and NB**2**) for connecting a gate electrode of a PMOS transistor (PM**52**) in the input stage to a (+) input terminal or (−) input terminal; switching transistors (NA**3** and NB**3**) for connecting a gate electrode of an NMOS transistor (NM**65**) in the output stage to a drain electrode (second electrode) of the PMOS transistor (PM**51**) in the input stage or to a drain electrode of the PMOS transistor (PM**52**) in the input state; and switching transistors (NA**4** and NB**4**) for connecting gate electrodes of NMOS transistors (NM**63** and NM**64**) constituting an active load circuit to the drain electrode of the PMOS transistor (PM**51**) in the input stage or to the drain electrode of the PMOS transistor (PM**52**) in the input stage.

[0109] Similarly, the high-voltage amplifier circuit **271** shown in FIG. **5** also includes switching transistors (PA**1** to PA**4**; PB**1** to PB**4**) as in the low-voltage amplifier circuit **272** shown in FIG. **4**.

[0110] A control signal (A) is applied to each gate electrode of the switching transistors (NA**1** to NA**4**; PA**1** to PA**4**) while a control signal (B) is applied to each gate electrode of the switching transistors (NB**1** to NB**4**; PB**1** to PB**4**).

[0111] FIG. **6** illustrates a circuit configuration of the low-voltage amplifier circuit **272** according to the embodiment shown in FIG. **4** when the control signal (A) is at a low level (L level) and the control signal (B) is at a high level (H level). FIG. **7** illustrates the same circuit configuration when the control level (A) is at a high level (H level) and the control signal (B) is at a low level (L level). Also shown in FIG. **6** and FIG. **7** are circuit configurations of the amplifier circuits using general operational amplifier signs. Hereinafter, the circuit configuration shown in FIG. **7** is referred to as "the type A low-voltage amplifier circuit 272" while the circuit configuration shown in FIG. **6** is referred to as "the type B low-voltage amplifier circuit 272."

[0112] In the low-voltage amplifier circuit **272** of this embodiment, an MOS transistor in the input stage to which an input voltage (Vin) is applied and an MOS transistor in the input stage to which an output voltage (Vout) is returned are alternately switched.

[0113] Because of the configuration described above, in the circuit configuration shown in FIG. **7**, the output voltage (Vout) is the sum of the input voltage (Vin) and the offset voltage (Voff), as indicated by formula (1) below.

Formula 1

[0114]

$$Vout=Vin+Voff \tag{1}$$

[0115] In the circuit configuration shown in FIG. **6**, a indicated by formula (2) below, the output voltage (Vout) is the difference between the input voltage (Vin) and the offset voltage (Voff).

Formula 2

[0116]

$$Vout=Vin-Voff \tag{2}$$

[0117] FIGS. **8**A to **8**D are diagrams showing the polarity of an image voltage output from the drain driver **130** to the

image line (DL) when the pseudo dot inversion method is used as an AC-drive method for a liquid crystal display module. In the configuration shown in FIG. **8**, phases of the control signal (A) and the control signal (B) are inverted once every two frames. Also in FIGS. **8**A to **8**D and in FIGS. **9**A to **9**D and **10**A to **10**D, which are to be described later, each square represents a pixel electrode.

[0118] In FIGS. **8**A to **8**D, when it is assumed, for instance, that image voltages are output to the image line D from the high-voltage amplifier circuit **271** having an offset voltage (Vofh) and from the low-voltage amplifier circuit **272** having an offset voltage Vofl, a voltage (VH−Vofh)(voltage +B in FIG. **8**) is output in the first frame shown in FIG. **8**A from the high-voltage amplifier circuit **271** (type B high-voltage amplifier circuit). However, because a voltage (VH+Vofh) (+A in FIG. **8**) is output in the third frame shown in FIG. **8**C from the high-voltage amplifier circuit **271** (type A high-voltage amplifier circuit), increase or decrease of brightness in an associated sub-pixel generated due to the offset voltage (Vofh) of the high-voltage amplifier circuit **271** is offset.

[0119] Furthermore, in the second frame shown in FIG. **8**B, a voltage (Vl−Vofl) (−B in FIG. **8**) is output from the low-voltage amplifier circuit **272** (type B low-voltage amplifier circuit). However, because a voltage (VL+Vofl) (−A in FIG. **8**) is output in the fourth frame shown in FIG. **8**D from the low-voltage amplifier circuit **272** (type A low-voltage amplifier circuit), increase or decrease of brightness in an associated sub-pixel generated due to the offset voltage (Vofl) of the low-voltage amplifier circuit **272** is offset.

[0120] As will be understood by referring to FIGS. **8**A to **8**D, however, image voltages are output from the low-voltage amplifier circuit and the high-voltage amplifier circuit, both of which belong to the same type, to image lines in each column within each frame. This leads to a problem that flickering occurs when a certain pattern is displayed on a screen, which degrades the display quality.

[0121] FIGS. **9**A to **9**D are diagrams illustrating an AC-drive method for the liquid crystal display module in this embodiment. The figures show the polarity of an image voltage output from the drain driver **130** to the image line (DL) when the pseudo dot inversion method is employed as an AC-drive method for the liquid crystal display module. In FIGS. **9**A to **9**D, phases of the control signal (A) and the control signal (B) are inverted once every two lines and also once every two frames.

[0122] In FIGS. **9**A to **9**D, when, for instance, image voltages are output to the image line denoted by sign D from the high-voltage amplifier circuit **271** having an offset voltage Vofh and from the low-voltage amplifier circuit **272** having an offset voltage Vofl, a voltage of (VH−Vofh) (+B in FIG. **9**) is output from the high-voltage amplifier circuit **271** (type B high-voltage amplifier circuit) to the first and second lines in the first frame shown in FIG. **9**A; a voltage of (VH+Vofh) (+A in FIG. **9**) is output from the high-voltage amplifier circuit **271** (type A high-voltage amplifier circuit) to the third and fourth lines in the first frame shown in FIG. **9**A.

[0123] Because of the configuration described above, in the first frame shown in FIG. **9**A, an image voltage is successively supplied to the image line denoted by sign D from the type B high-voltage amplifier circuit, from the type B low-voltage amplifier circuit, from the type A high-voltage amplifier circuit, and from the type A low-voltage amplifier circuit in this order. Therefore, increase and decrease of brightness generated due to offset voltages in the high-voltage amplifier circuits and the lower-voltage amplifier circuits are canceled once every four display lines within one frame.

[0124] Likewise, in the second frame shown in FIG. **9**B, an image voltage is successively supplied to the image line D from the type B low-voltage amplifier circuit, from the type B high-voltage amplifier circuit, from the type A low-voltage amplifier circuit, and from the type A high-voltage amplifier circuit in this order. Therefore, increase and decrease of brightness generated due to offset voltages in the high-voltage amplifier circuits and the low-voltage amplifier circuits are canceled once every four display lines within one frame. This is also applicable to the third frame shown in FIG. **9**C and to the fourth frame shown in FIG. **9**D.

[0125] Under the AC-drive method of this embodiment, phases of the control signal (A) and the control signal (B) are inverted once every two lines within each frame and also once every two frames, thereby offsetting increase and decrease of brightness generated due to an offset voltage in the amplifier circuit at sub-pixels arranged in the column direction once every four successive frames and also once every four display lines within one frame. This results in no flicker on a screen when a certain pattern is displayed on it, thus not degrading its display quality.

[0126] FIGS. **10**A to **10**D are diagrams illustrating another example of the AC-drive method for the liquid crystal display module in this embodiment. The figures illustrate the polarity of an image voltage output from the drain driver **130** to the image line (DL) when the column-by-column inversion method is employed as the AC-drive method for a liquid crystal display module. FIG. **10** shows a case in which phases of the control signal (A) and the control signal (B) are inverted once every two lines and also once every two frames.

[0127] As shown in FIGS. **10**A to **10**D, image voltages are output from the type A high-voltage amplifier circuit and the type B high-voltage amplifier circuit or from the type A low-voltage amplifier circuit and the type B low-voltage amplifier circuit, respectively, to sub-pixels in each column every two line. Therefore, increase and decrease of brightness generated due to an offset voltage in the amplifier circuit are canceled once every four successive frames and also once every four display lines within one frame. The above configuration results in no flicker on the display screen when a certain pattern is displayed on it, thus not degrading its display quality.

[0128] The invention made by the present inventor has been described above in detail with reference to the embodiment, but the present invention is not limited to the embodiment. It is needless to say that various changes and modifications are possible without departing from the gist of the invention.

What is claimed is:

1. A liquid crystal display device comprising:

a plurality of image lines;

a plurality of scanning lines;

a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and

an image line drive circuit for supplying an image voltage to each of the image lines,

in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line;

the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input

terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and

the switching unit switches, according to a switching control signal input every two display lines, one of the two input terminals of the amplifier circuit to an inverting input terminal and the other of the two input terminals to a non-inverting input terminal or switches one of the two input terminals of the amplifier circuit to the non-inverting input terminal and the other of the two input terminals to the inverting input terminal.

2. A liquid crystal display device comprising:

a plurality of image lines;

a plurality of scanning lines;

a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and

an image line drive circuit for supplying an image voltage to each of the image lines,

the plurality of thin-film transistors provided between two adjoining image lines along a direction in which the image lines extend having such an arrangement in which thin-film transistors connected to one of the two adjoining image lines and those connected to the other of the two adjoining image lines are alternately arranged, in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line;

the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and

the switching unit switches, according to a switching control signal input every two display lines, one of the two input terminals of the amplifier circuit to an inverting input terminal and the other of the two input terminals to a non-inverting input terminal or switches one of the two input terminals of the amplifier circuit to the non-inverting input terminal and the other of the two input terminals to the inverting input terminal.

3. The liquid crystal display device according to claim **1**, wherein the image line drive circuit comprises:

a data latch circuit for latching input display data; and

a decoder circuit for selecting a gray-scale voltage based on the display data supplied from the data latch circuit and

wherein the amplifier circuit outputs the gray-scale voltage selected by the decoder circuit as an image voltage to the image line.

4. The liquid crystal display device according to claim **2**, wherein the image line drive circuit comprises:

a data latch circuit for latching input display data; and

a decoder circuit for selecting a gray-scale voltage based on the display data supplied from the data latch circuit and

wherein the amplifier circuit outputs the gray-scale voltage selected by the decoder circuit as an image voltage to the image line.

5. The liquid crystal display device according to claim **1**, wherein a phase of the switching control signal is inverted every two frames.

6. The liquid crystal display device according to claim **2**, wherein a phase of the switching control signal is inverted every two frames.

7. The liquid crystal display device according to claim **1**, wherein a cycle of the switching control signal is twice as long as a horizontal scanning time.

8. The liquid crystal display device according to claim **2**, wherein a cycle of the switching control signal is twice as long as a horizontal scanning time.

9. A liquid crystal display device comprising:

a plurality of image lines;

a plurality of scanning lines;

a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and

an image line drive circuit for supplying an image voltage to each of the image lines,

in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line;

the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and

an image voltage produced by adding an offset voltage to a gray-scale voltage and an image voltage produced by subtracting the offset voltage from the gray-scale voltage are supplied alternately via the image line to the thin-film transistor every two successive horizontal-scanning periods.

10. A liquid crystal display device comprising:

a plurality of image lines;

a plurality of scanning lines;

a plurality of thin-film transistors connected to each of the image lines and each of the scanning lines; and

an image line drive circuit for supplying an image voltage to each of the image lines,

the plurality of thin-film transistors provided between two adjoining image lines along a direction in which the image lines extend having such an arrangement in which thin-film transistors connected to one of the two adjoining image lines and those connected to the other of the two adjoining image lines are alternately arranged,

in which polarity of an image voltage supplied from the image line drive circuit to each of the image lines is kept constant during one frame period, and at the same time, between two successive frames, polarity of an image voltage supplied to each image line from the image line drive circuit during the former frame is different from that supplied during the latter frame,

wherein: the image line drive circuit has an amplifier circuit for outputting an image voltage to the image line;

the amplifier circuit has a switching unit for connecting one of two input terminals to either of an inverting input

terminal or a non-inverting input terminal and also for connecting the other of the two input terminals to the remaining one out of the inverting input terminal and the non-inverting input terminal; and

an image voltage produced by adding an offset voltage to a gray-scale voltage and an image voltage produced by subtracting the offset voltage from the gray-scale voltage are supplied alternately via the image line to the thin-film transistor every two successive horizontal-scanning periods.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US20080246718A1	公开(公告)日	2008-10-09
申请号	US12/060282	申请日	2008-04-01
[标]申请(专利权)人(译)	株式会社日立显示器		
申请(专利权)人(译)	日立显示器有限公司.		
当前申请(专利权)人(译)	松下液晶显示CO.，LTD.		
[标]发明人	TANAKA YASUHIRO		
发明人	TANAKA, YASUHIRO		
IPC分类号	G09G3/36		
CPC分类号	G09G3/3614 G09G3/3688 G09G2310/0291 G09G2310/0297 G09G2320/0233		
优先权	2007097033 2007-04-03 JP		
外部链接	Espacenet USPTO		

摘要(译)

一种液晶显示装置，包括图像线驱动电路，该图像线驱动电路具有用于将图像电压输出到图像线的放大器电路。放大器电路具有开关单元，用于将两个输入端子中的一个连接到反相输入端子或非反相输入端子，并且还用于将两个输入端子中的另一个连接到反相输入端子中的剩余一个或者非反相输入端子。切换单元根据每两条显示线输入的切换控制信号，将放大器电路的两个输入端之一切换到反相输入端，将两个输入端中的另一个切换到非反相输入端或切换一个放大器电路的两个输入端子连接到非反相输入端子，另一个输入端子连接到反相输入端子。