US 20040174483A1

(19) **United States**

(12) **Patent Application Publication**

Nakamura et al.

(10) **Pub. No.: US 2004/0174483 A1**

(43) **Pub. Date: Sep. 9, 2004**

(54) **LIQUID CRYSTAL DISPLAY DEVICE HAVING AUXILIARY CAPACITIVE ELECTRODE**

(76) Inventors: **Yayoi Nakamura**, Tokyo (JP); **Hiromitsu Ishii**, Tokyo (JP); **Shinichi Shimomaki**, Tokyo (JP); **Hitoshi Watanabe**, Tokyo (JP)

Correspondence Address:
FRISHAUF, HOLTZ, GOODMAN & CHICK, PC
767 THIRD AVENUE
25TH FLOOR
NEW YORK, NY 10017-2023 (US)

(21) Appl. No.: **10/794,276**

(22) Filed: **Mar. 4, 2004**

(30) **Foreign Application Priority Data**

Mar. 7, 2003 (JP) 2003-61440
May 15, 2003 (JP) 2003-137232

Publication Classification

(51) **Int. Cl.^{7}** **G02F 1/1343**
(52) **U.S. Cl.** **349/139**

(57) **ABSTRACT**

A display device includes a substrate, a plurality of scanning lines formed in parallel with each other on the substrate in one direction, a plurality of data lines formed in parallel with each other on the substrate in orthogonal to the scanning lines, a thin film transistor being formed in the vicinity of each intersection of the scanning lines and the data lines and having a semiconductor thin film, a gate electrode connected to one of the scanning lines, a source electrode, a drain electrode connected to one of the scanning lines; pixel electrodes each connected to the source electrode of the thin film transistor, auxiliary capacitive electrodes each having an overlap region that overlaps with the pixel electrodes and forming an auxiliary capacitance with the pixel electrodes, a first insulating film arranged between the auxiliary capacitive electrodes and the data lines, and a second insulting film arranged between the pixel electrodes and the auxiliary capacitive electrodes.

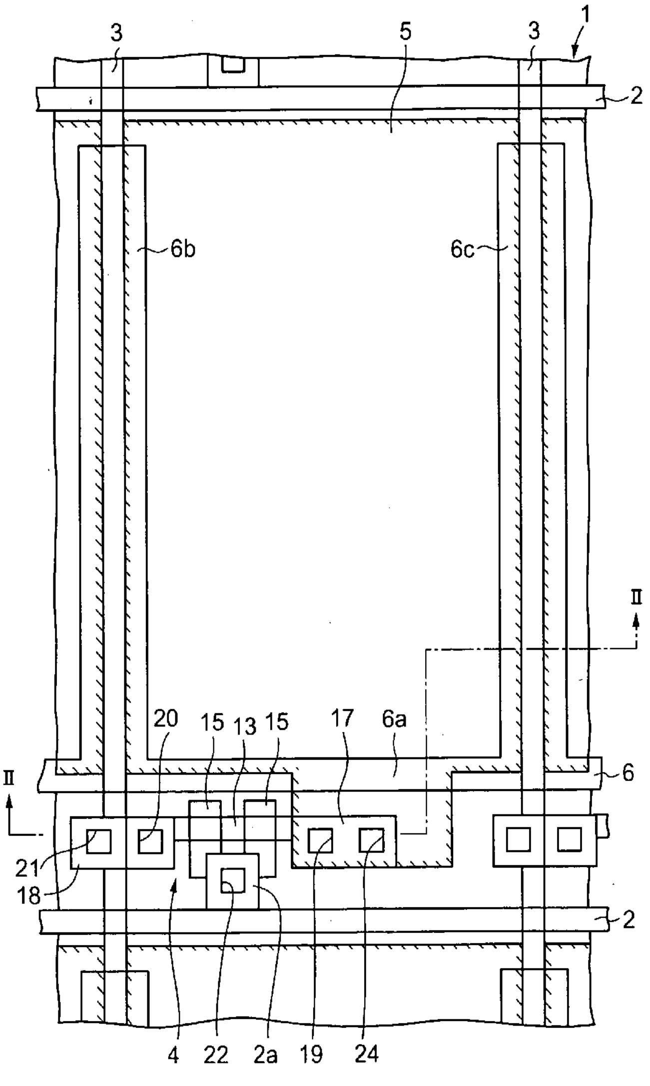


FIG. 1

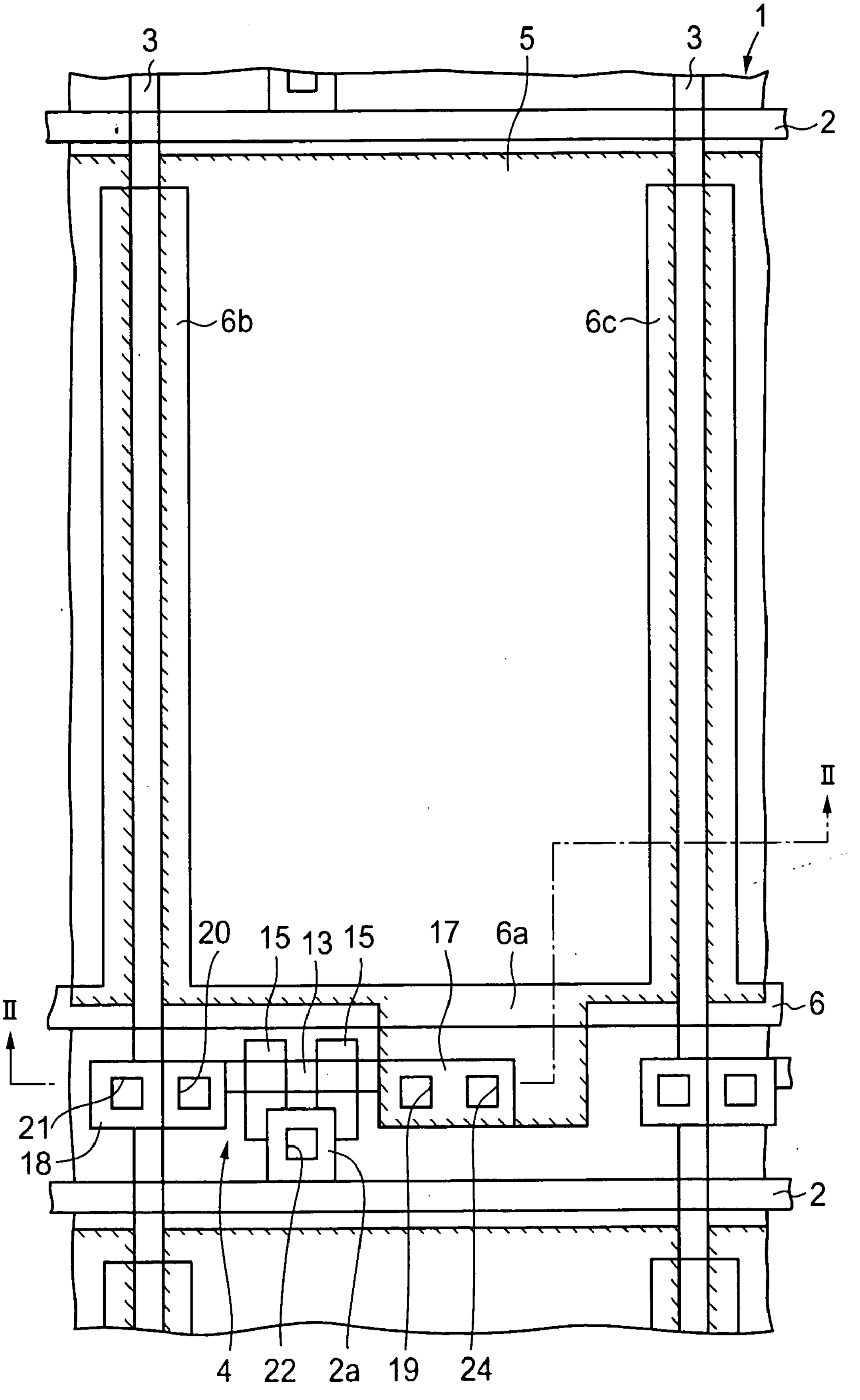


FIG. 2

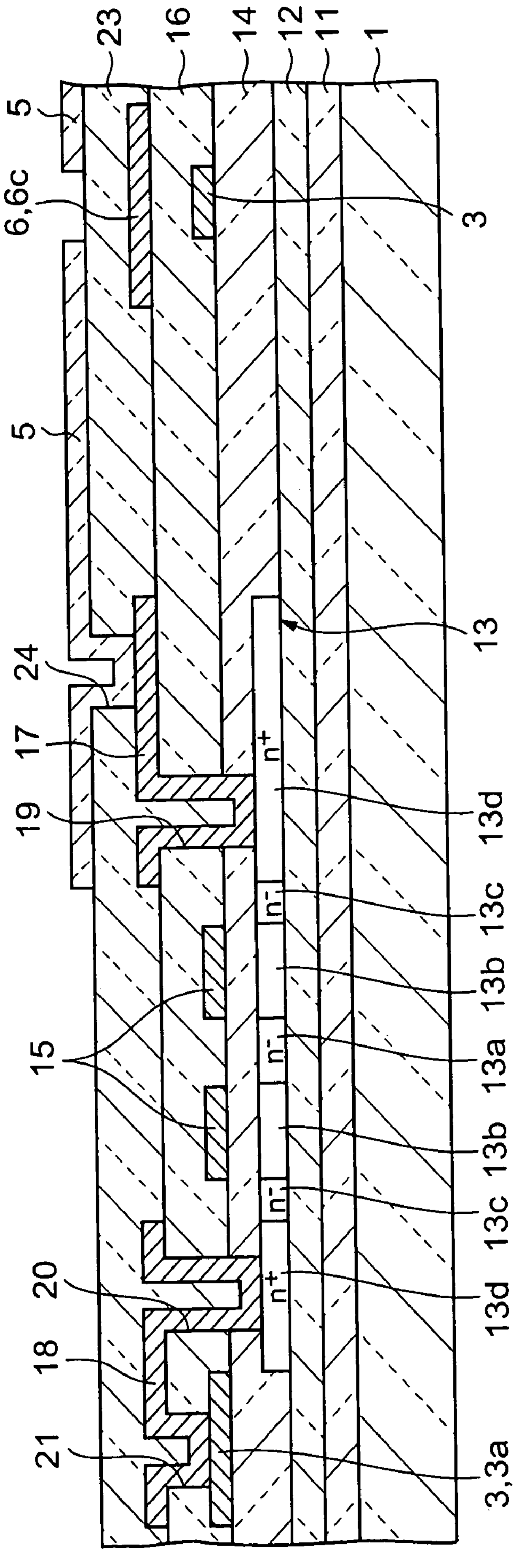

23
16
14
12
11
1
5
6,6c
3
5
13
24
17
19
n+
13d
n-
13c
13b
15
n-
13a
13b
n-
13c
20
n+
13d
18
21
3,3a

FIG. 3A

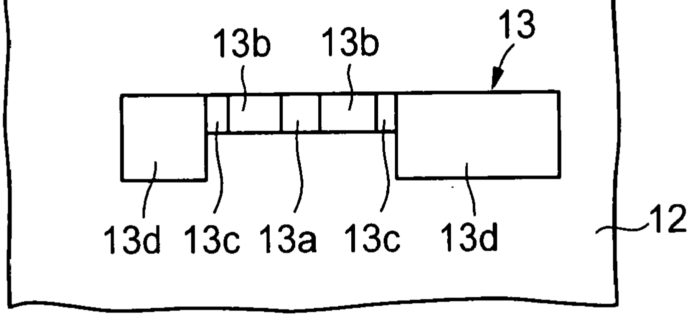


FIG. 3B

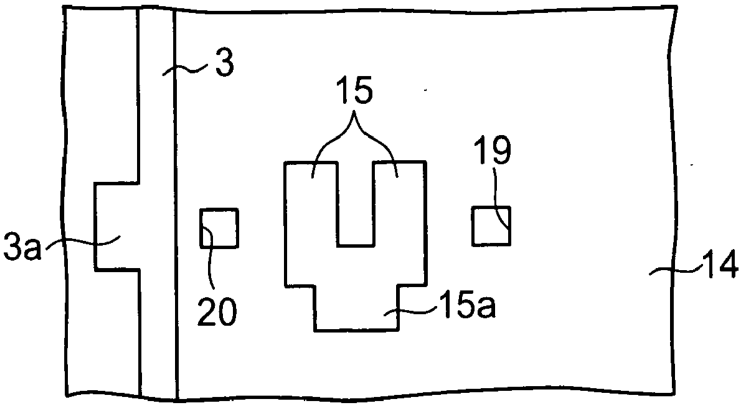


FIG. 3C

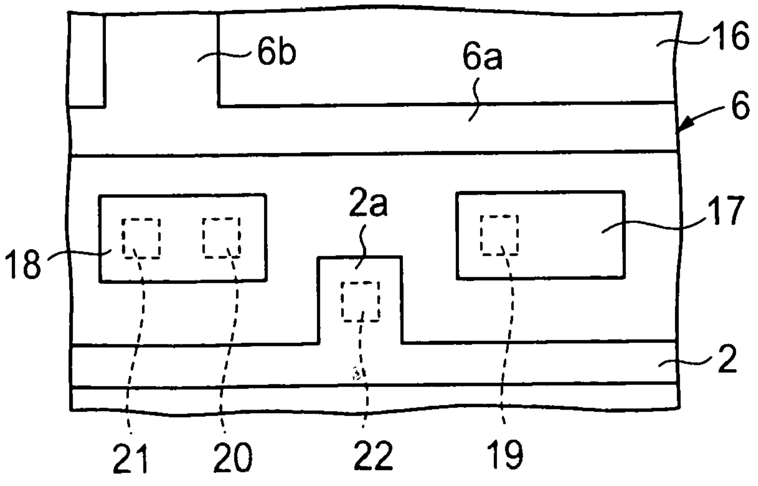


FIG. 4

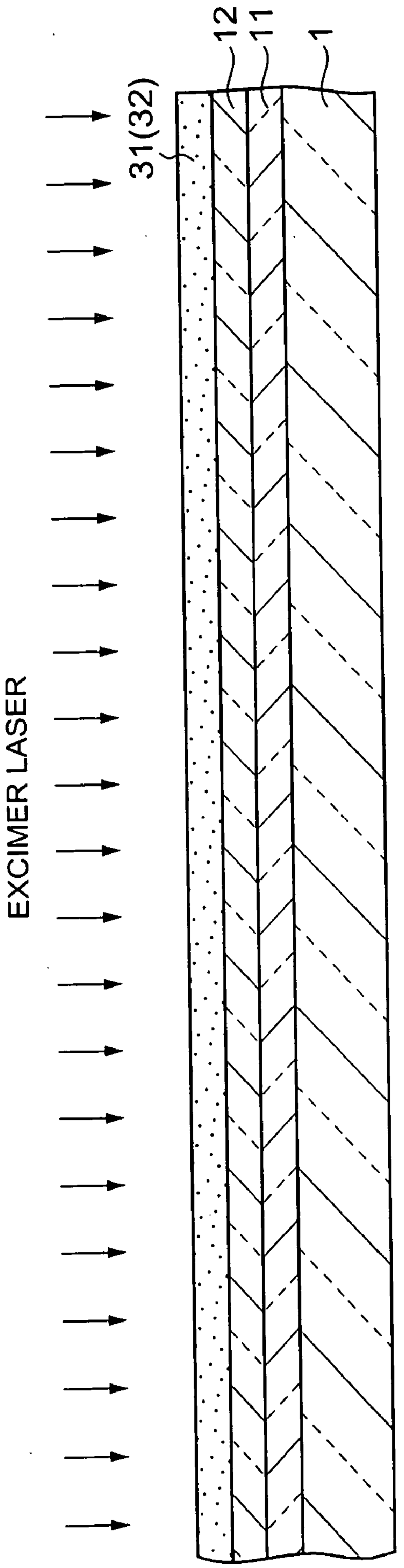


FIG. 5

INJECT N-TYPE IMPURITIES WITH CONCENTRATION

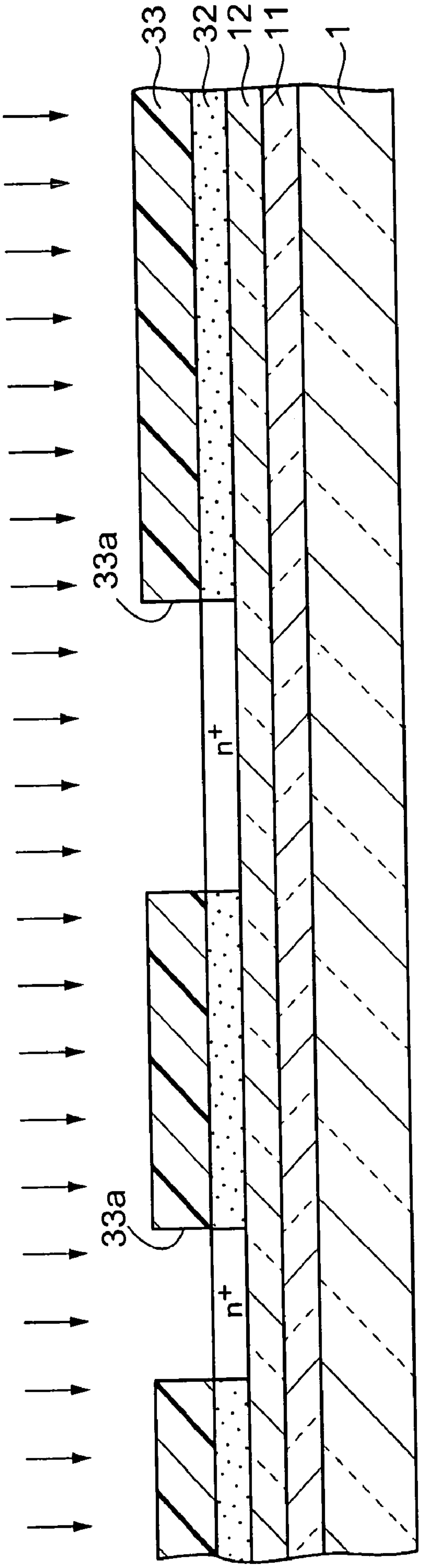


FIG. 6

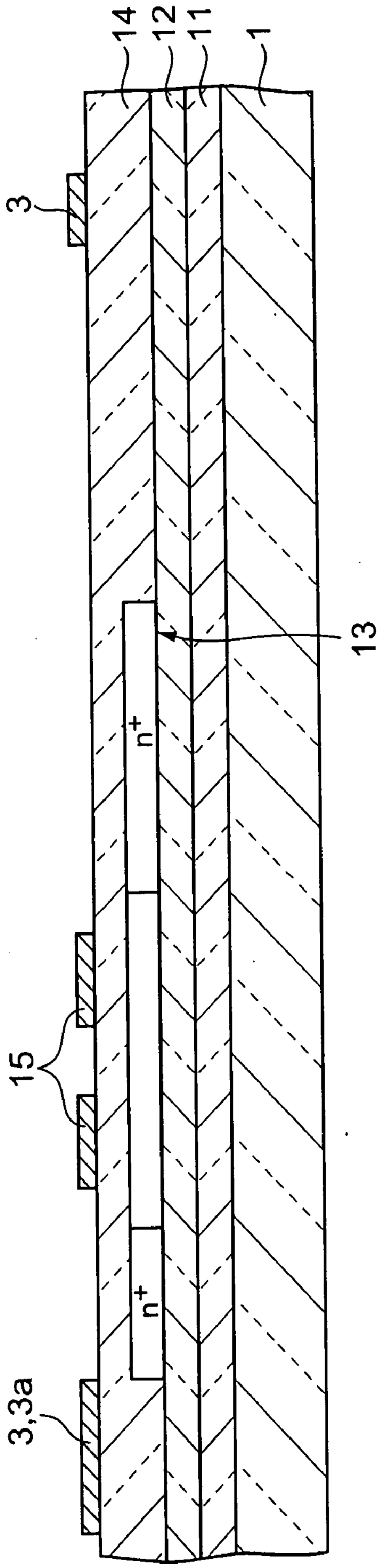


FIG. 7

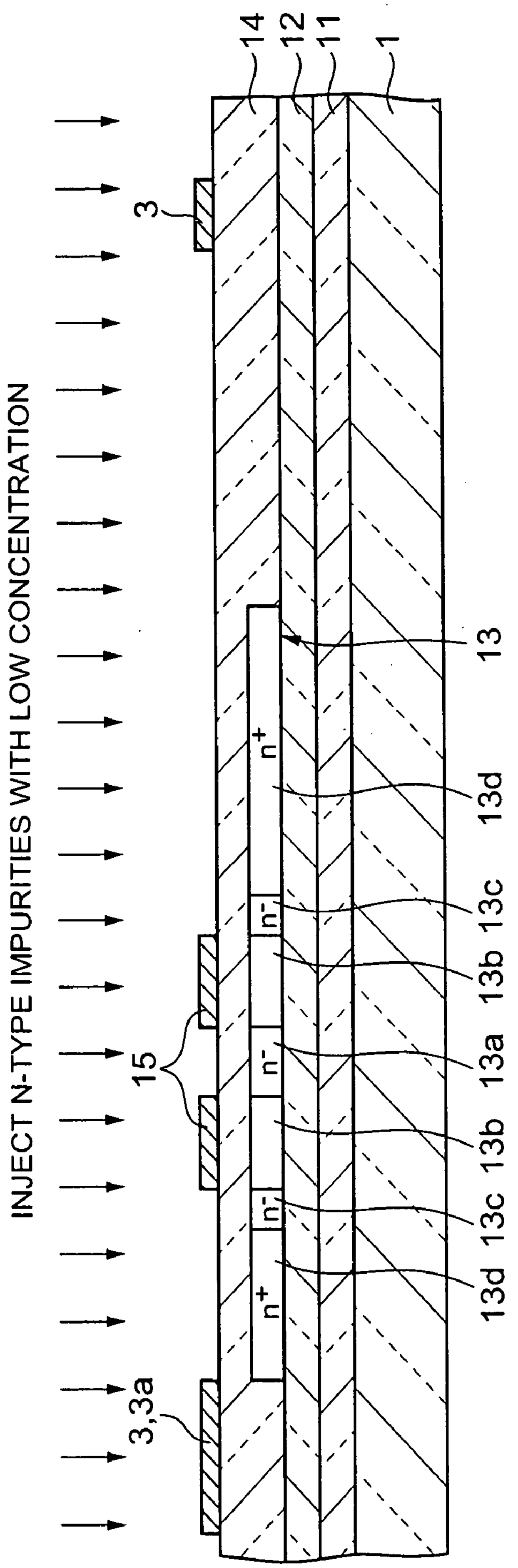

INJECT N-TYPE IMPURITIES WITH LOW CONCENTRATION
14
12
11
1
3
13
n+
13d
n-
13c
13b
15
n-
13a
13b
n-
13c
n+
13d
3,3a

FIG. 8

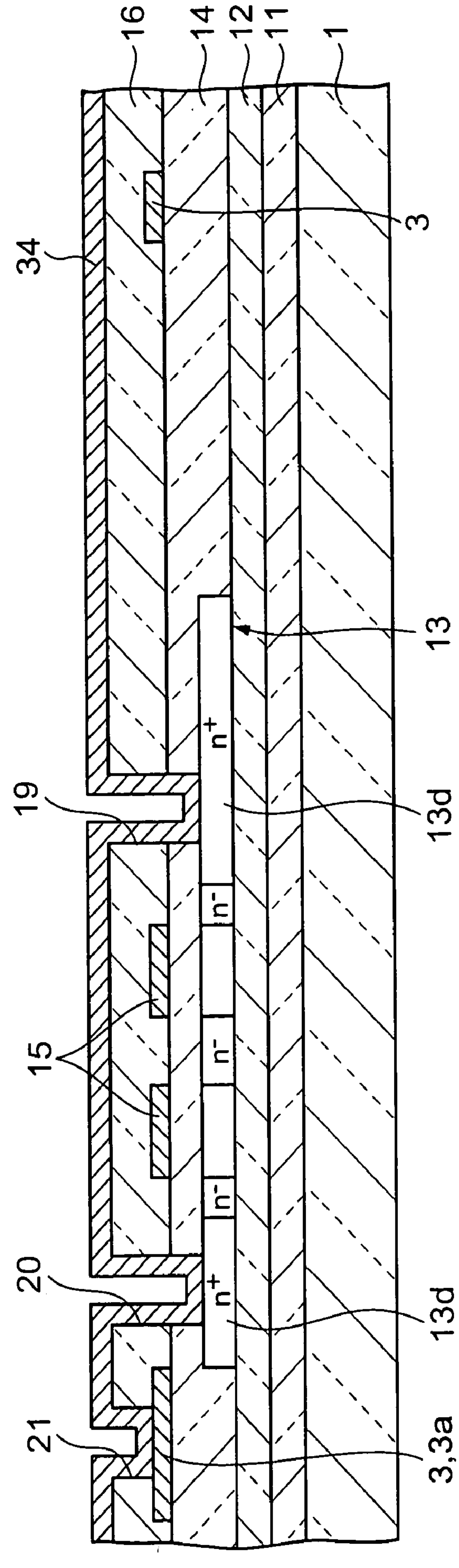


FIG. 9

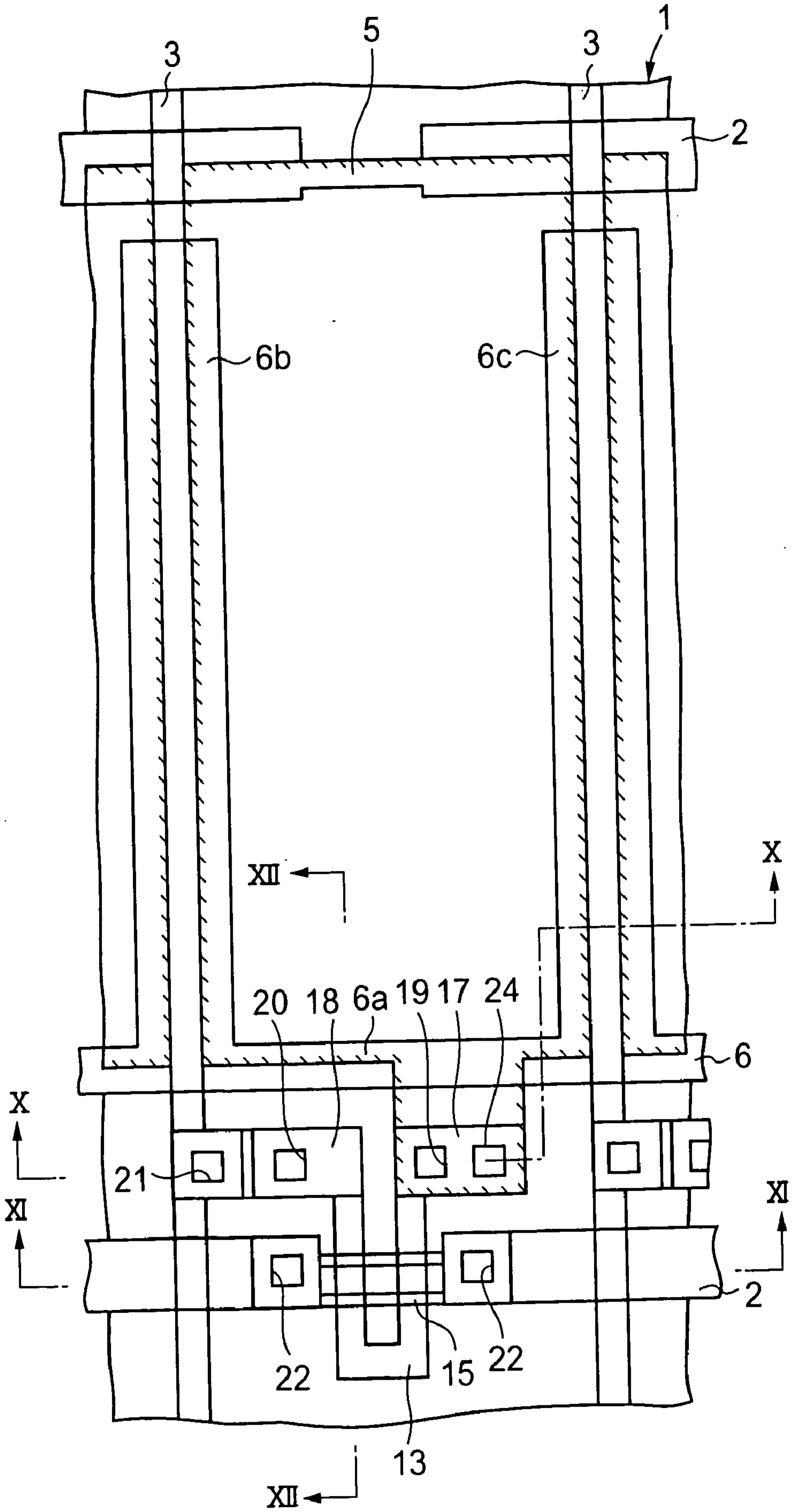


FIG. 10

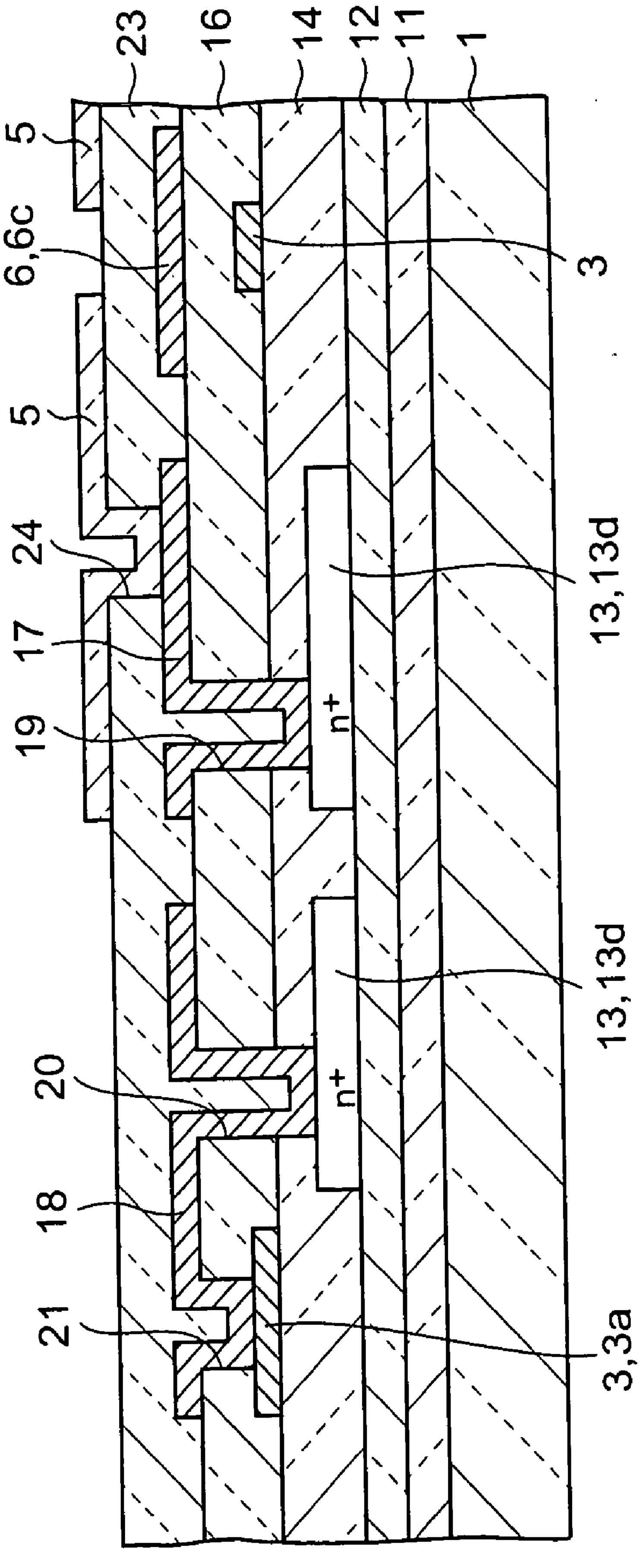


FIG. 11

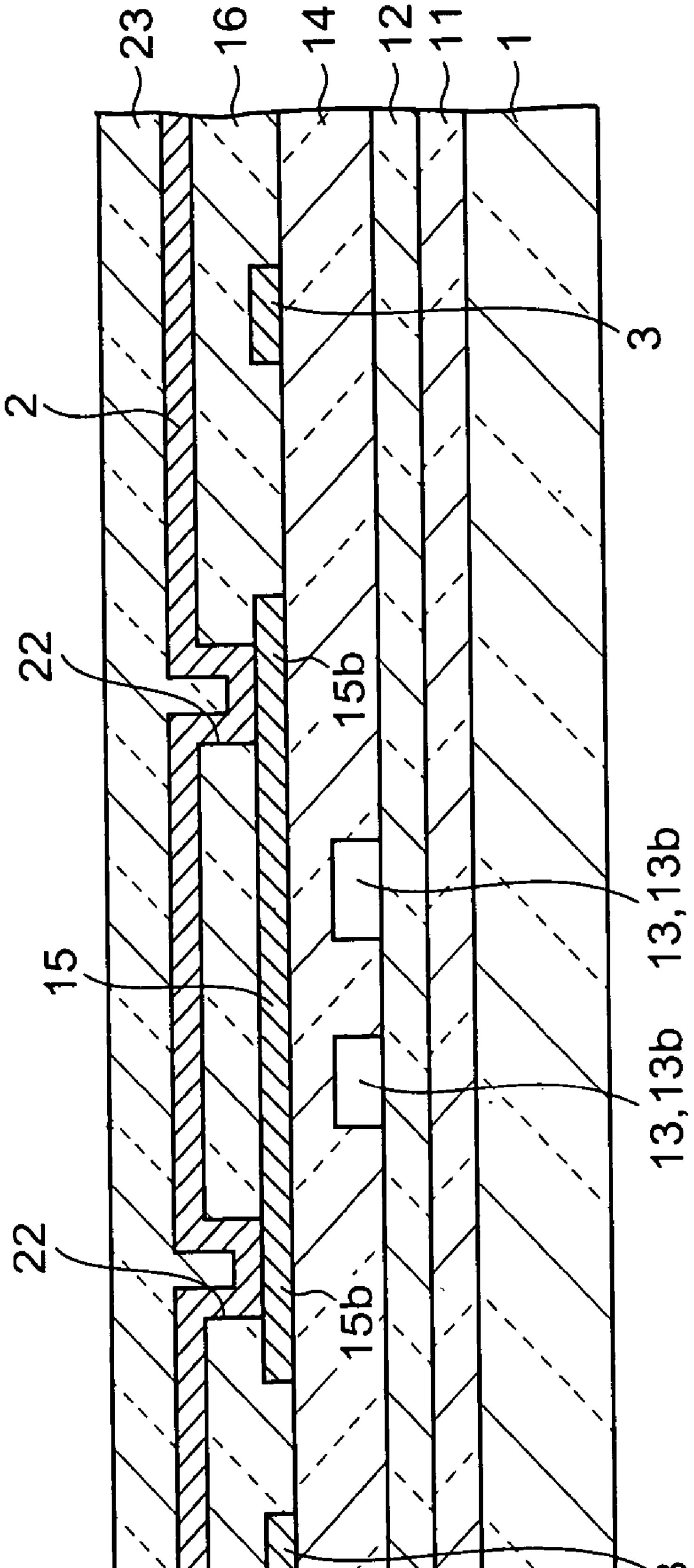


FIG. 12

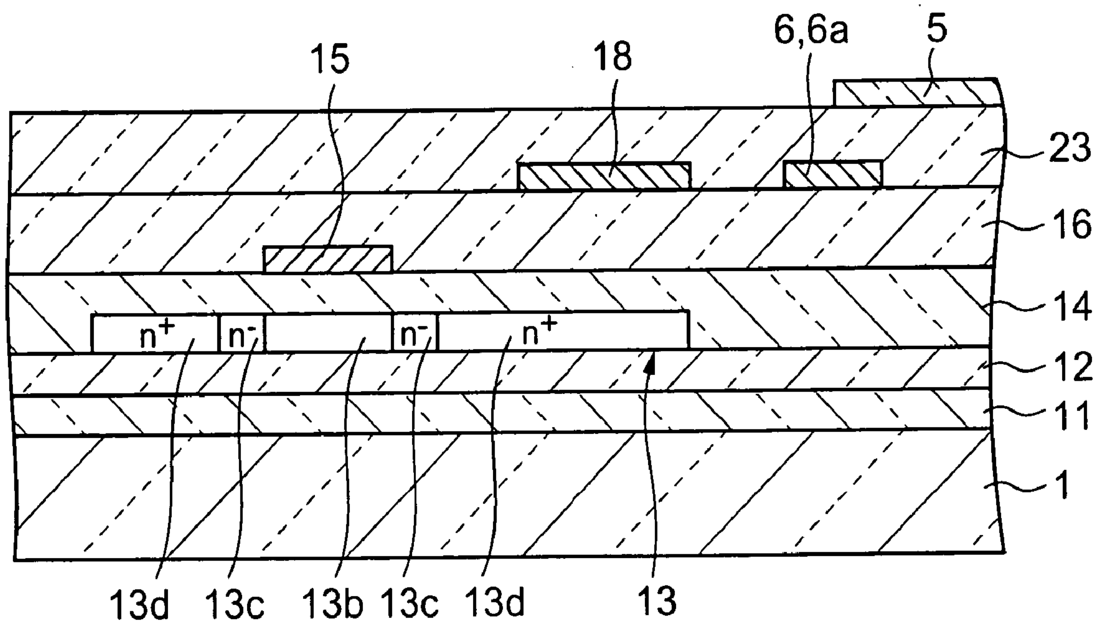


FIG. 13A

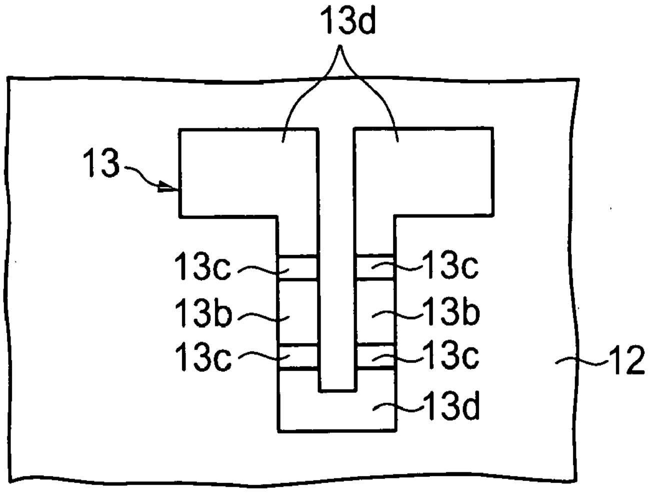


FIG. 13B

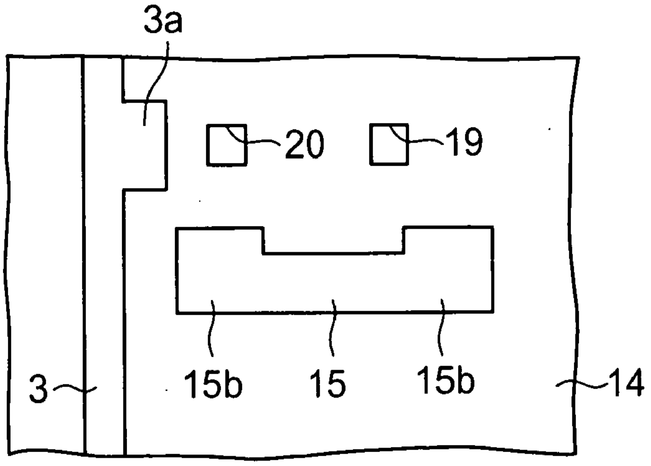


FIG. 13C

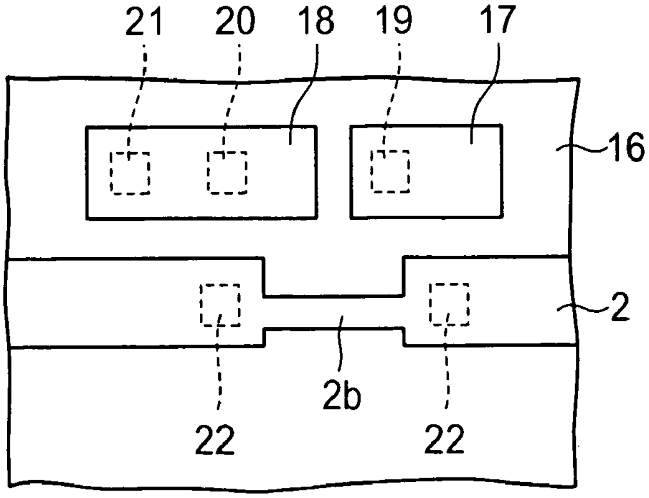


FIG. 14

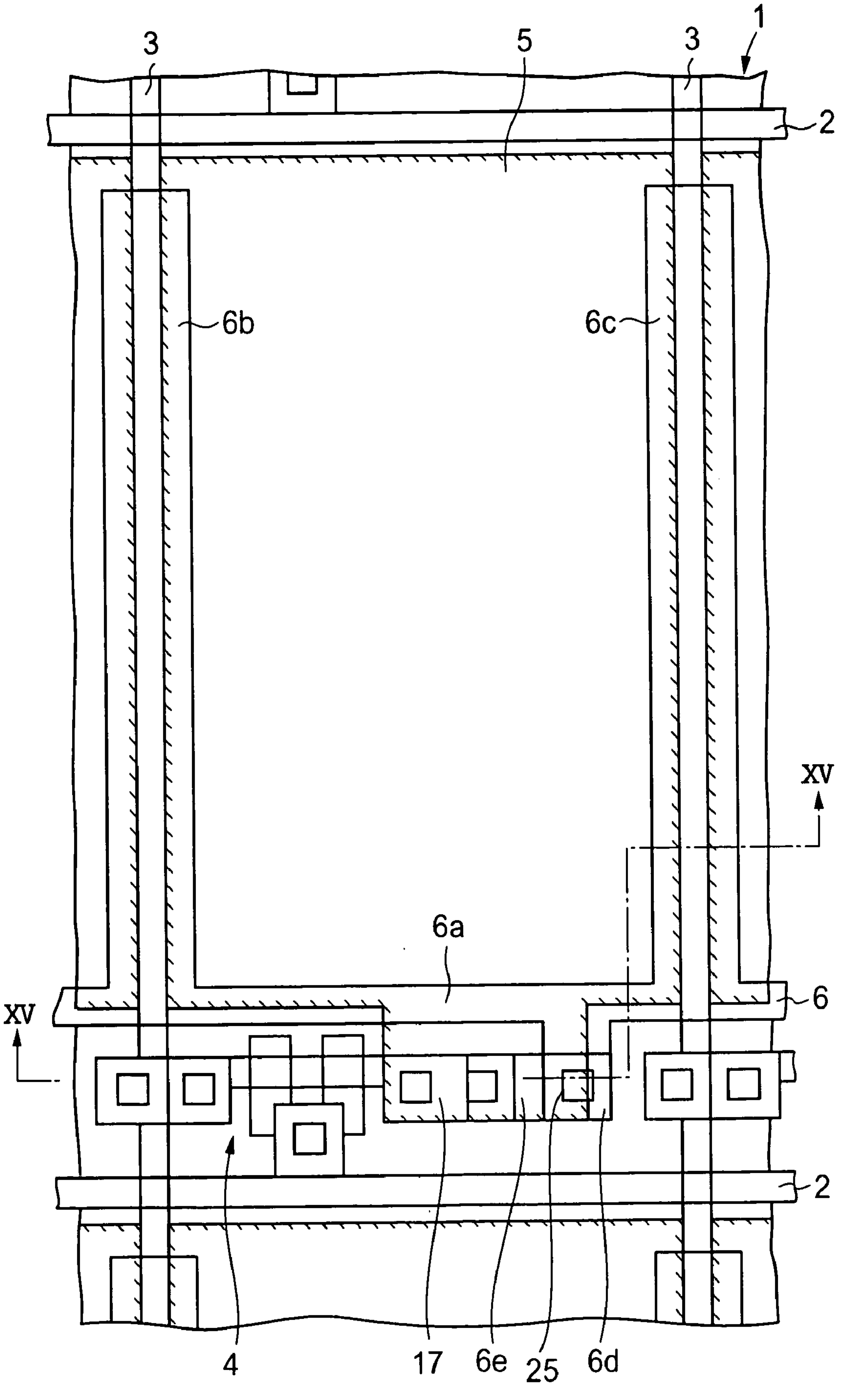


FIG. 15

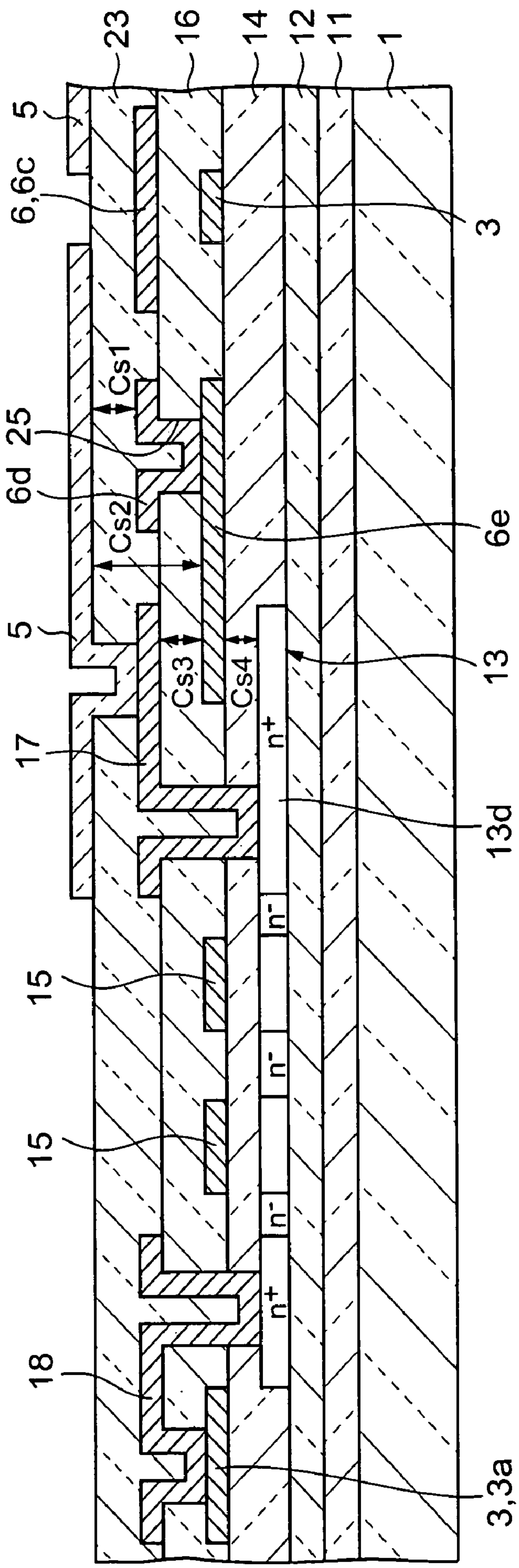

23
16
14
12
11
1
5
6,6c
3
Cs1
25
6d
Cs2
6e
5
Cs3
Cs4
13
17
n^+
13d
n^-
15
n^-
15
n^-
n^+
18
3,3a

FIG. 16

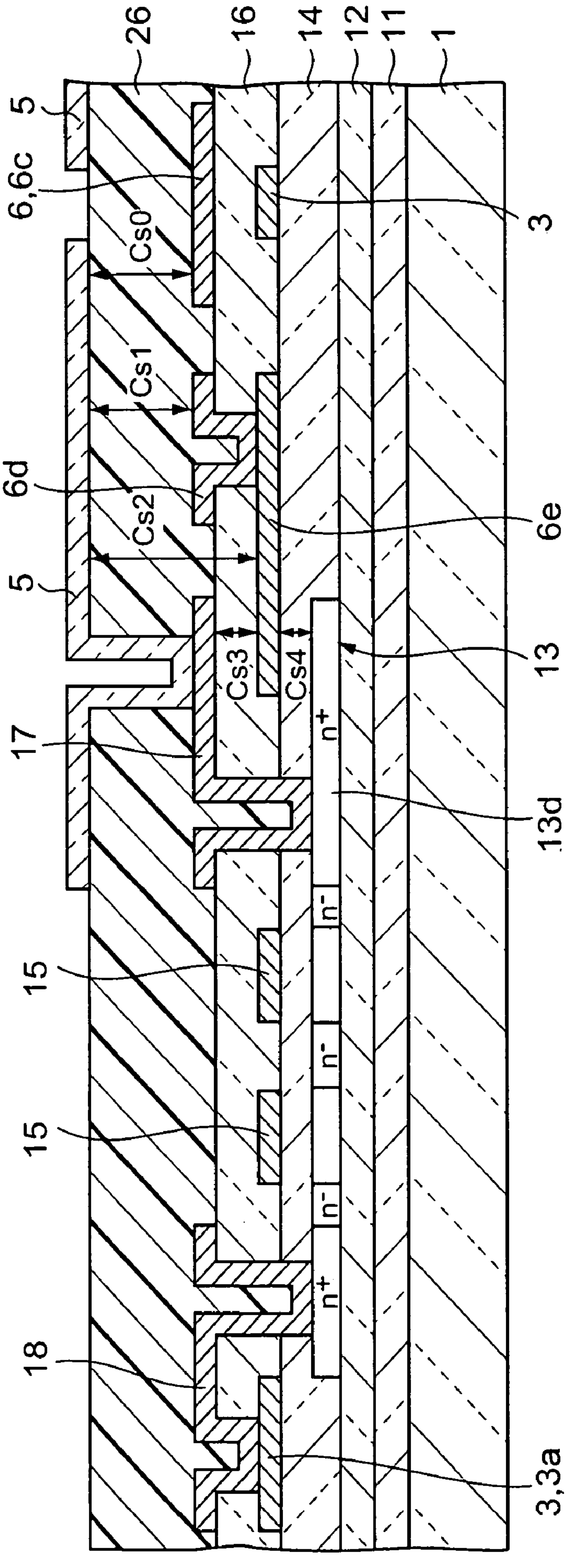

26
16
14
12
11
1
5
6,6c
3
Cs0
Cs1
6d
Cs2
6e
5
Cs3
Cs4
13
17
n^+
13d
15
n^-
15
n^-
n^-
n^+
18
3,3a

FIG. 17

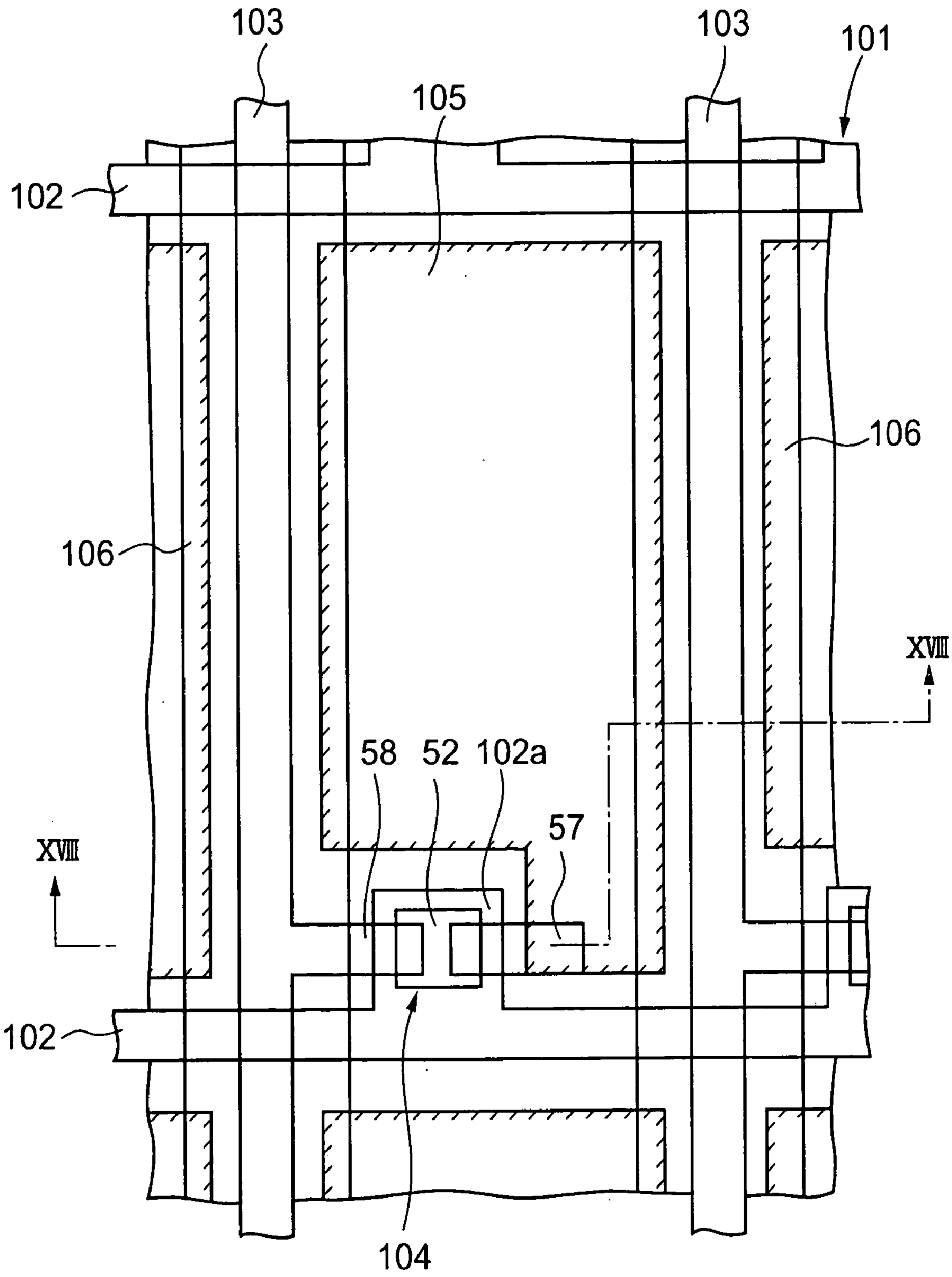


FIG. 18

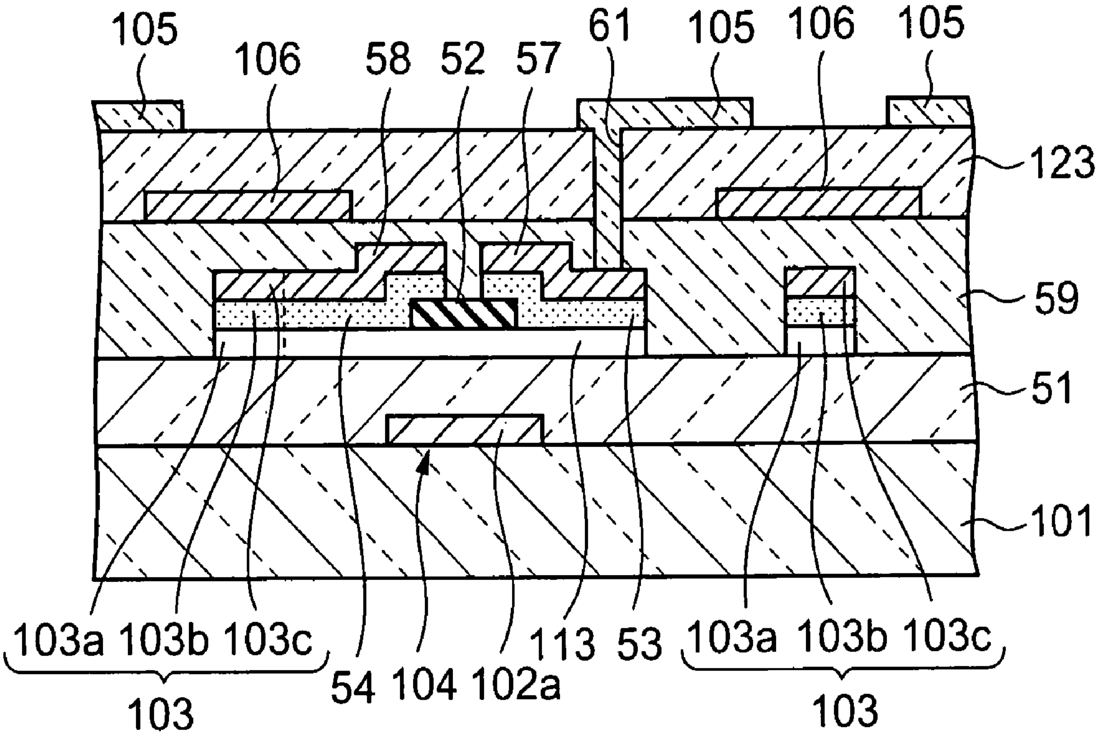

105
106
58
52
57
61
105
106
105
123
59
51
101
103a
103b
103c
103
54
104
102a
113
53
103a
103b
103c
103

FIG. 19

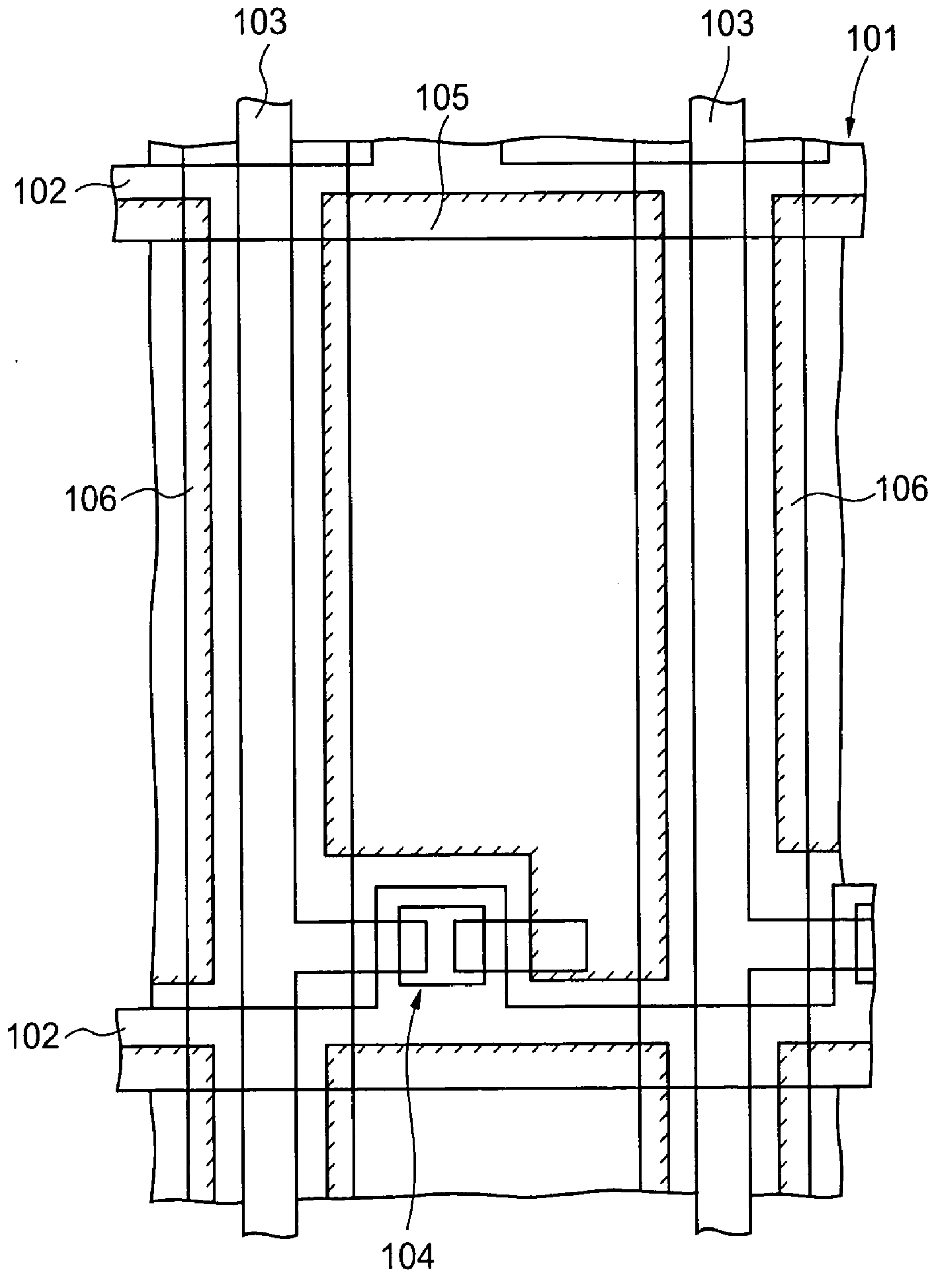


FIG. 20

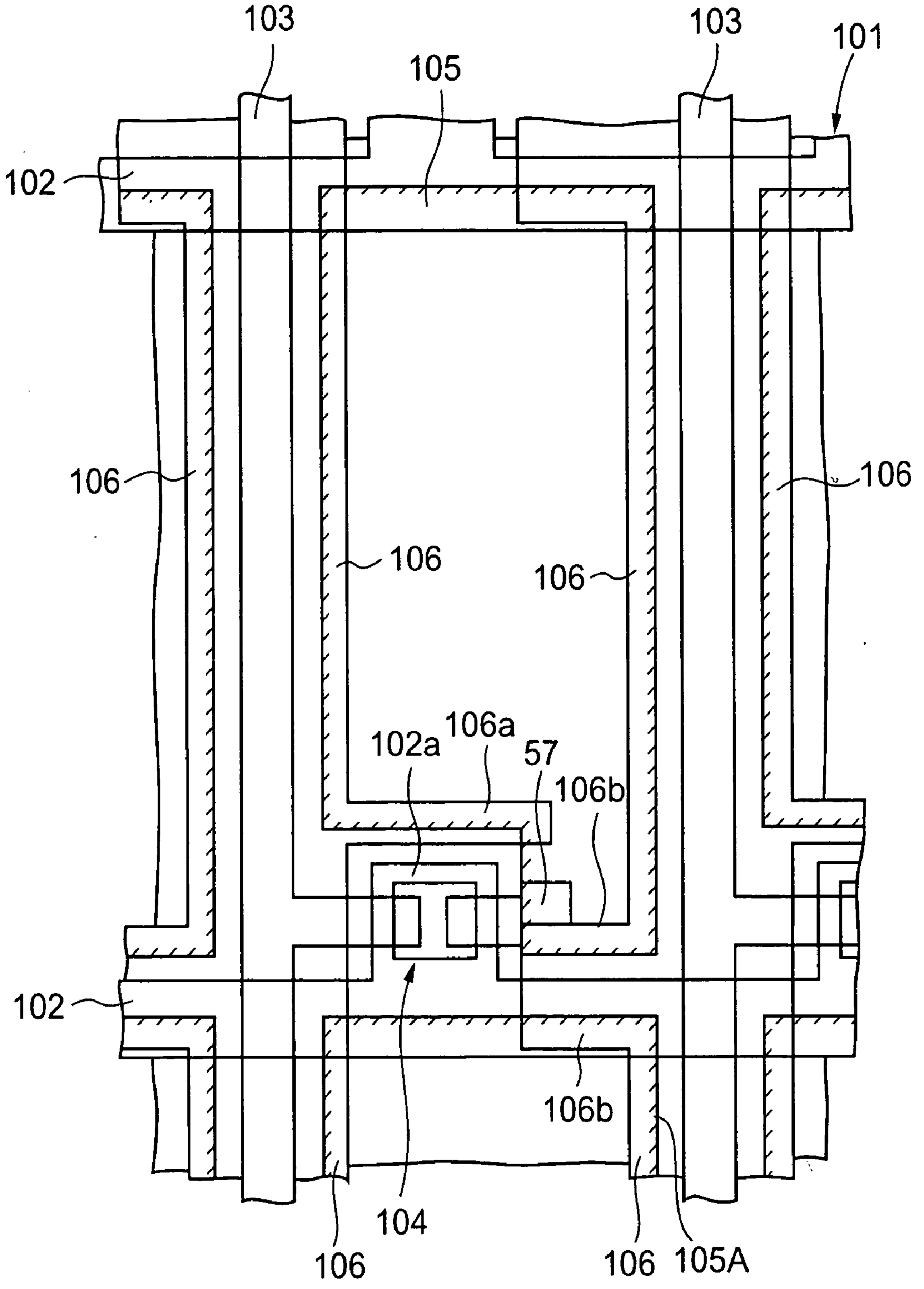

103
103
101
105
102
106
106
106
106
102a
106a
57
106b
102
104
106b
106
106
105A

FIG. 21

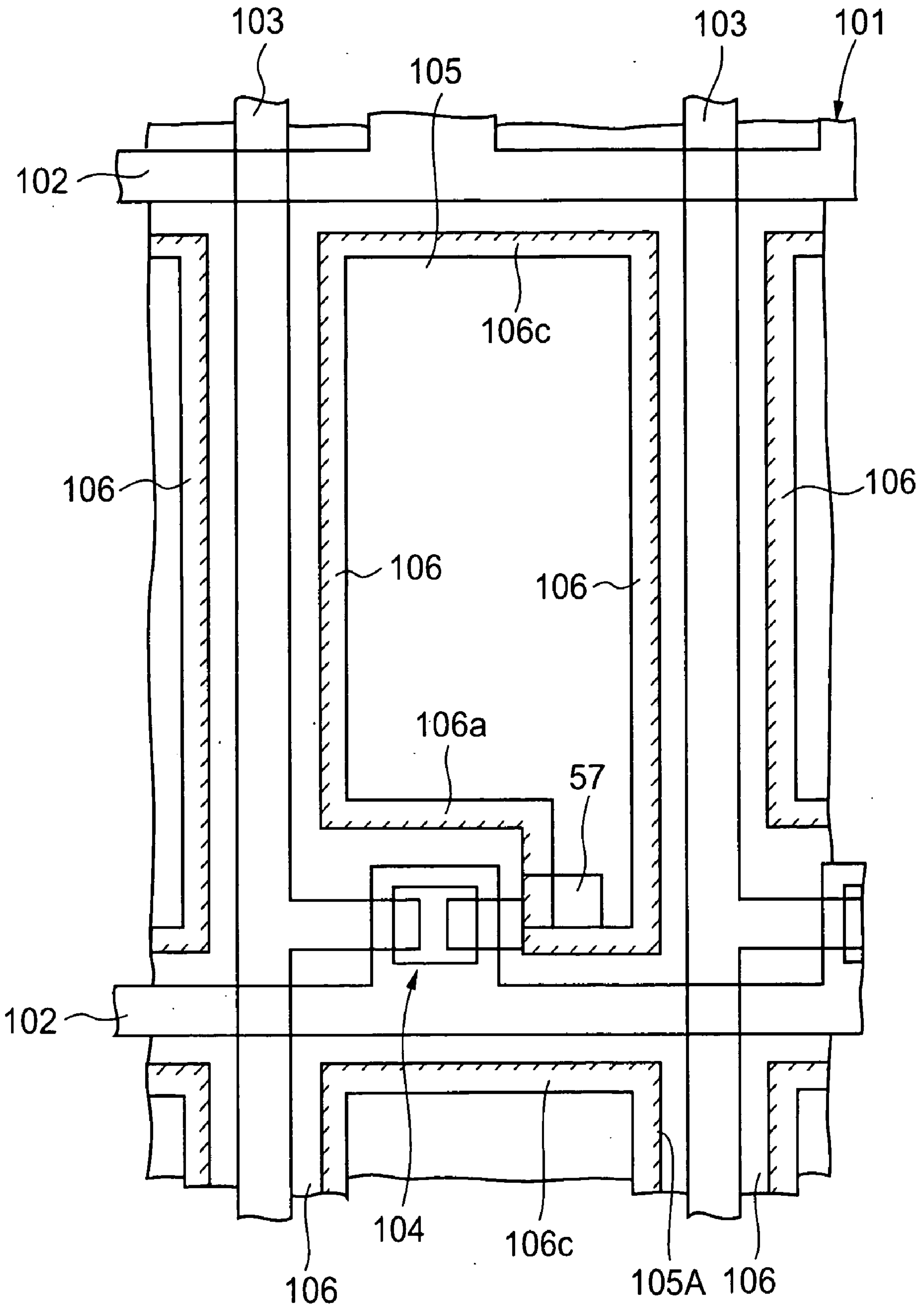

103
103
101
105
102
106c
106
106
106
106
106
106a
57
102
104
106c
106
105A
106

FIG. 22

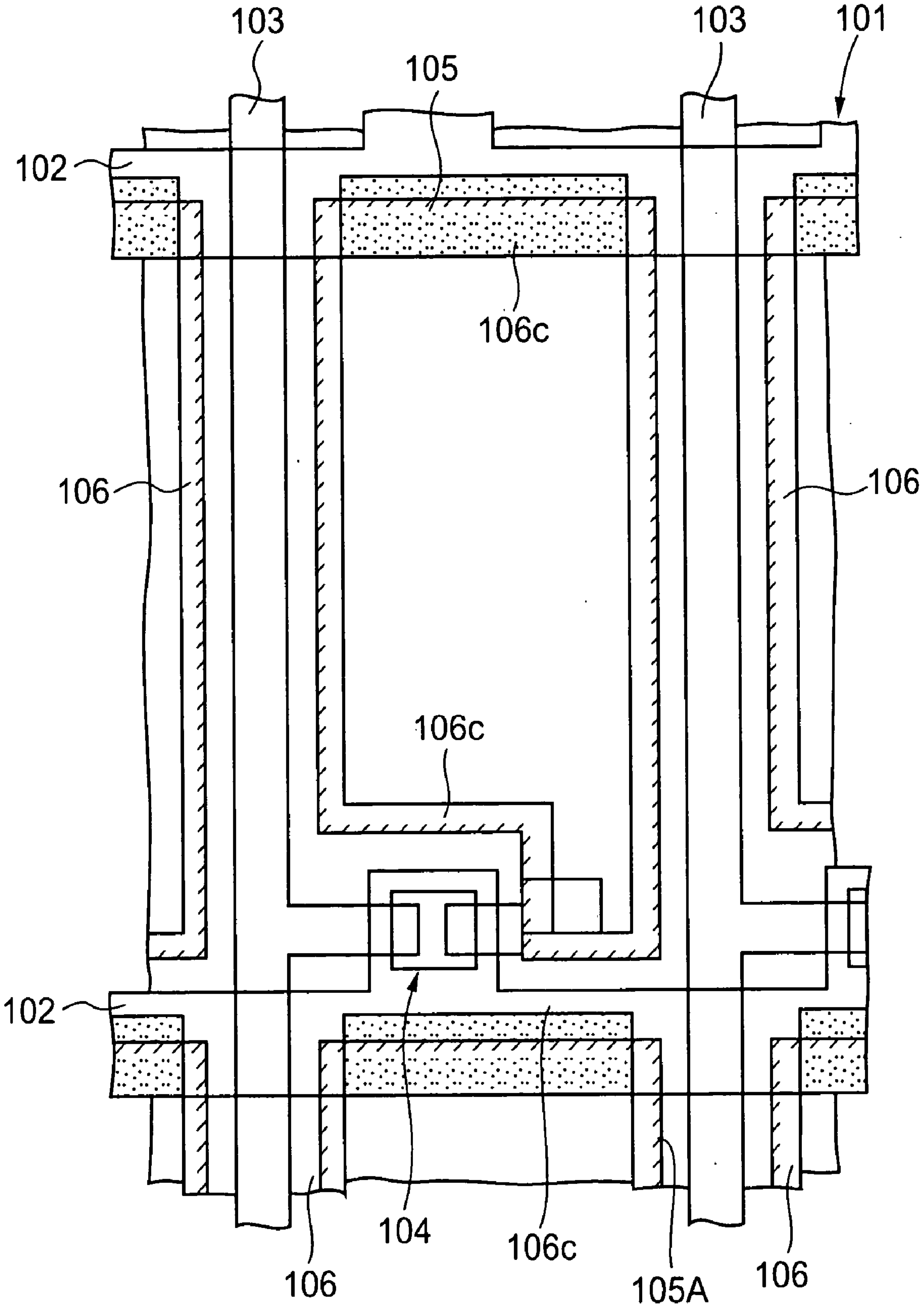


FIG. 23

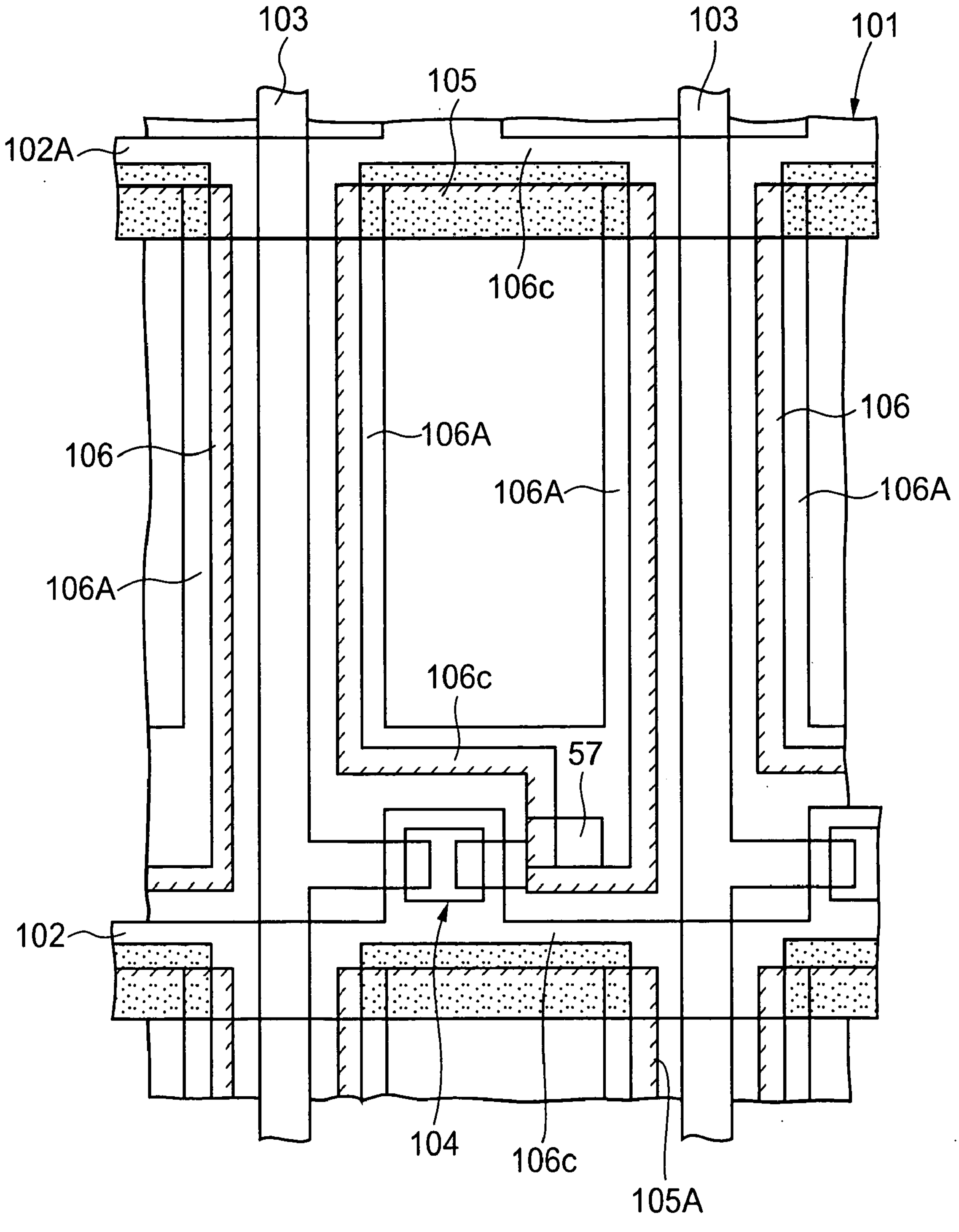

103
103
101
105
102A
106c
106
106A
106A
106
106A
106A
106c
57
102
104
106c
105A

FIG. 24A
PRIOR ART

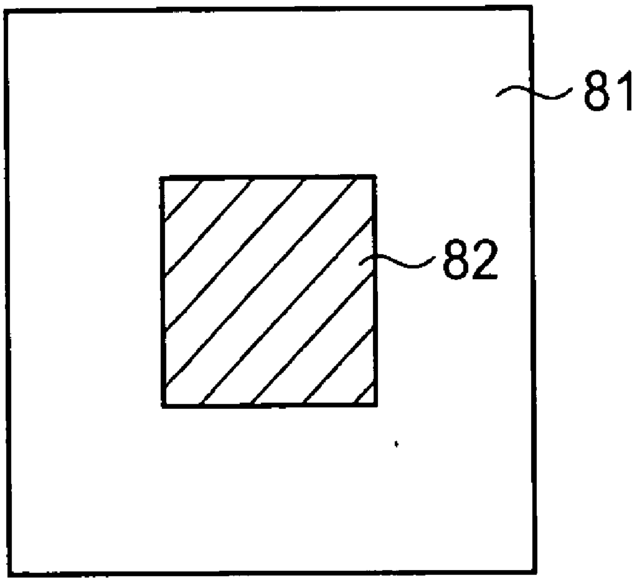
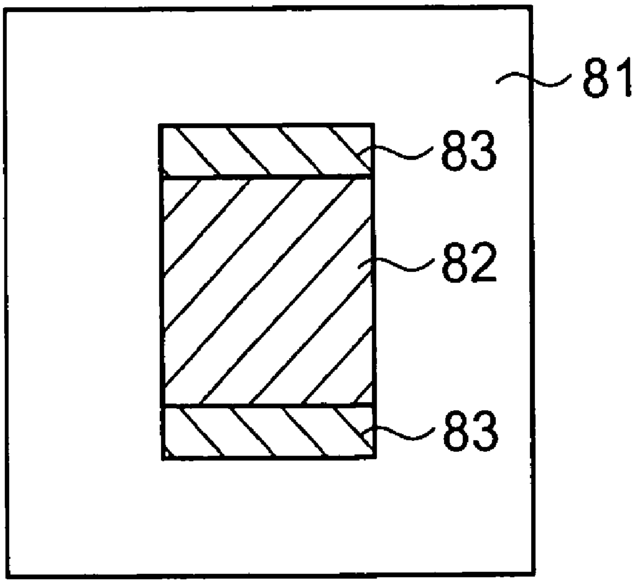


FIG. 24B
PRIOR ART



LIQUID CRYSTAL DISPLAY DEVICE HAVING AUXILIARY CAPACITIVE ELECTRODE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display device and particularly to a liquid crystal display device having a structure in which display quality is improved by an auxiliary capacitive electrode.

[0003] 2. Description of the Related Art

[0004] For example, in an active matrix type liquid crystal display device, scanning lines and data lines are formed on a glass substrate in a X-direction and a Y-direction, respectively. In the vicinity of each intersection of the scanning lines and the data lines, a thin film transistor connected to both lines is provided as a switching element. An insulating film is formed thereon, and on the insulating film, pixel electrodes are formed to be connected the thin film transistors, which are provided near the intersections, through contact holes provided to the insulating film, respectively. In this case, the edge portion of each pixel electrode is overlapped with both lines in order to obtain a high aperture ratio.

[0005] The above-explained liquid crystal display device is disclosed in, for example, **FIGS. 1 and 4** of Unexamined Japanese Patent Application KOKAI Publication No. H1-156725.

[0006] However, in the above-structured liquid crystal display device, since the edge portion of the pixel electrode is overlapped with the data lines, coupling capacitance occurs on the overlapped portion. For this reason, there is a problem in which vertical crosstalk resulting from the coupling capacitance occurs on the overlapped portion to degrade a display characteristic. In other words, for example, as illustrated in **FIG. 24**A, in a case where a black square **82** is displayed in one pixel **81** with a gray background, an electrical potential of the pixel **81** is varied as a drain voltage. Accordingly, as illustrated by reference numeral **83** of **FIG. 24**B, the background color of the upper and lower portions of the square **82** slightly deepens. In this way, the portion colored in black is pulled to the upper and lower sides of the square **82**, so that the display characteristic will deteriorate.

[0007] In addition, it is assumed that the contents of Unexamined Japanese Patent Application KOKAI Publication No. H1-156725 are incorporated into this specification.

SUMMARY OF THE INVENTION

[0008] Accordingly, an object of the present invention is to provide a liquid crystal display device capable of preventing occurrence of vertical crosstalk.

[0009] A display device of the present invention includes a substrate. The display device of the present invention further includes a plurality of scanning lines formed in parallel with each other on the substrate in one direction and a plurality of data lines formed in parallel with each other on the substrate in orthogonal to the scanning lines. The display device of the present invention further includes a thin film transistor being formed in the vicinity of each intersection of that scanning lines and that data lines and having a semiconductor thin film, a gate electrode connected to one of the scanning lines, a source electrode, a drain electrode connected to one of the scanning lines. The display device of the present invention further includes pixel electrodes each connected to the source electrode of that thin film transistor. The display device of the present invention further includes auxiliary capacitive electrodes each having an overlap region that overlaps with the pixel electrodes and forming an auxiliary capacitance with the pixel electrodes. The display device of the present invention further includes a first insulating film arranged between that auxiliary capacitive electrodes and that data lines. The display device of the present invention further includes a second insulting film arranged between that pixel electrodes and that auxiliary capacitive electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These objects and other objects and advantages of the present invention will become more apparent upon reading of the following detailed description and the accompanying drawings in which:

[0011] **FIG. 1** is a plan view of a main part of a thin film transistor panel in a liquid crystal display device shown as respective layers being seen through according to a first embodiment of the present invention;

[0012] **FIG. 2** is a cross-sectional view taken on the line II-II of **FIG. 1**;

[0013] **FIGS. 3**A to **3**C are plan views each explaining a thin film transistor portion illustrated in **FIG. 1**;

[0014] **FIG. 4** is a cross-sectional view of an initial process at the time of manufacturing a thin film transistor panel illustrated in **FIGS. 1 and 2**;

[0015] **FIG. 5** is a cross-sectional view of a process subsequent to **FIG. 4**;

[0016] **FIG. 6** is a cross-sectional view of a process subsequent to **FIG. 5**;

[0017] **FIG. 7** is a cross-sectional view of a process subsequent to **FIG. 6**;

[0018] **FIG. 8** is a cross-sectional view of a process subsequent to **FIG. 7**;

[0019] **FIG. 9** is a plan view of a main part of a thin film transistor panel in a liquid crystal display device shown as respective layers being seen through according to a second embodiment of the present invention;

[0020] **FIG. 10** is a cross-sectional view taken on the line X-X of **FIG. 9**;

[0021] **FIG. 11** is a cross-sectional view taken on the line XI-XI of **FIG. 9**;

[0022] **FIG. 12** is a cross-sectional view taken on the line XII-XII of **FIG. 9**;

[0023] **FIGS. 13**A to **13**C are plan views each explaining a thin film transistor portion illustrated in **FIG. 9**;

[0024] **FIG. 14** is a plan view of a main part of a thin film transistor panel in a liquid crystal display device shown as respective layers being seen through according to a third embodiment of the present invention;

[0025] **FIG. 15** is a cross-sectional view taken on the line XV-XV of **FIG. 14**;

[0026] **FIG. 16** is a cross-sectional view of a thin film transistor panel in a liquid crystal display device according to a fourth embodiment of the present invention, similar to FIG. **15**;

[0027] **FIG. 17** is a plan view of a thin film transistor panel in an active matrix type liquid crystal display device shown as respective layers being seen through according to a fifth embodiment of the present invention;

[0028] **FIG. 18** is a cross-sectional view taken on the line XVIII-XVIII of **FIG. 17**;

[0029] **FIG. 19** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a sixth embodiment of the present invention, similar to **FIG. 17**;

[0030] **FIG. 20** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a seventh embodiment of the present invention, similar to **FIG. 18**;

[0031] **FIG. 21** is a plan view of a thin film transistor panel shown as respective layers being seen through according to an eighth embodiment of the present invention, similar to **FIG. 17**;

[0032] **FIG. 22** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a ninth embodiment of the present invention, similar to **FIG. 21**;

[0033] **FIG. 23** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a tenth embodiment of the present invention, similar to **FIG. 22**; and

[0034] **FIGS. 24A and 24B** are views explaining the problem of the conventional liquid crystal display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0035] (First Embodiment)

[0036] **FIG. 1** is a plan view of a main part of a thin film transistor panel in a liquid crystal display device shown as respective layers being seen through according to a first embodiment of the present invention. The thin film transistor panel includes a glass substrate **1**. On an upper surface side of the glass substrate **1**, a plurality of scanning lines **2** are formed in parallel with each other in a horizontal direction and a plurality of data lines **3** are formed in parallel with each other in a vertical direction, orthogonal to the scanning lines **2**. In the vicinity of each intersection of scanning lines **2** and data lines **3**, a thin film transistor **4** having a double gate structure, a pixel electrode **5**, and an auxiliary capacitive electrode **6** are formed. Here, for the purpose of clarifying **FIG. 1**, an edge portion of each pixel electrode **5** is hatched with oblique short solid lines.

[0037] In this case, the right and left edges of the pixel electrode **5** are arranged at the same position as the edges of the data lines **3** arranged at right and left sides of the pixel electrode **5** as seen from the plane, respectively. However, the right and left edges of the pixel electrode **5** may be arranged to overlap with the data lines **3**. Accordingly, a region, which is obtained by removing forming regions of the data lines **3** provided at the right and left sides of the pixel electrode **5** and a forming region of the thin film transistor **4** from a forming region of the pixel electrode **5**, is used as a substantial pixel region. This makes it possible to obtain a high aperture ratio.

[0038] However, in this case, in order to prevent external light from being incident on the thin film transistors **4**, a black mask is formed on a portion, which corresponds to at least each of the thin film transistors **4**, of a counter panel (not shown) provided to be opposite to the thin film transistor panel.

[0039] Each auxiliary capacitive electrode **6** includes a linear electrode portion ***6a*** placed in parallel with the scanning line **2**, a strip electrode portion ***6b*** placed in parallel with the left data line **3** of the pixel electrode **5**, and a strip electrode portion ***6c*** placed in parallel with the right data line **3** of the pixel electrode **5**. In this case, the electrode portion ***6a*** is overlapped with a lower side portion of the pixel electrode **5**. Each of the electrode portions ***6b*** and ***6c*** is overlapped with the opposing side portions of the pixel electrodes **5**, which are adjacent to each right and left, and the data line **3** formed therebetween.

[0040] Moreover, though this is explained later, each of the electrode portions ***6b*** and ***6c*** is placed between the pixel electrodes **5** and the data line **3** in a thickness direction of the thin film transistor panel, namely, a vertical direction on paper of **FIG. 1**. The width of each of the electrodes ***6b*** and ***6c*** (a length in a direction parallel to the scanning line **2**) is set to be wider than the width of the data line **3** to some degree. Accordingly, the data line **3** is entirely covered with the electrode portion ***6b*** or ***6c***, not to oppose to the pixel electrodes **5** directly, even if there is a positional shift in a direction parallel to the scanning line **2** in an alignment step.

[0041] Next, a specific structure of the thin film transistor panel in one pixel will be explained. **FIG. 2** is a cross-sectional view taken on the line II-II of **FIG. 1**. On the upper surface of the glass substrate **1**, first and second underlying insulating films **11** and **12** are formed. A polysilicone thin film **13** is formed on a predetermined portion of an upper surface of the second underlying insulating film **12**. As illustrated in **FIG. 3**A, the polysilicone thin film **13** including multiple gate (channel) regions is substantially linearly formed. At a substantially central portion of the polysilicone thin film **13**, an n-type impurity low concentration region ***13a*** having a low concentration of n-type impurities is formed. Furthermore, channel regions ***13b*** each having an intrinsic region are formed at both sides of the n-type impurity low concentration region ***13a***. Moreover, n-type impurity low concentration regions ***13c*** are formed at both sides of the channel regions ***13b*** that sandwich the n-type impurity low concentration region ***13a***. Furthermore, n-type impurity high concentration regions ***13d*** each having a high concentration of n-type impurities are formed at both sides of channel regions ***13c*** that sandwich the n-type impurity low concentration region ***13a*** and the channel regions ***13b***.

[0042] On the upper surfaces of the second underlying insulating film **12** and the polysilicone thin film **13**, a gate insulating film **14** is formed. Two gate electrodes **15** are formed on predetermined portions of the upper surface of the gate insulting film **14**, so as to cover two channel regions

13*b* of the polysilicone thin film **13** as illustrated in **FIG. 3B**. In this case, two gate electrodes **15** have a common connecting portion **15***a* that connects both electrodes **15** to each other to form a substantially U-shape island. The island means an area that is physically and electrically separated from the other elements, and is used based on the same definition in the explanation hereinafter. On a predetermined portion of the upper surface of the gate insulating film **14**, the data line **3** is formed as illustrated in **FIG. 3B**. A connecting portion **3***a* with a large width is formed on a predetermined portion of the data line **3**.

[**0043**] On the upper surfaces of the gate insulating film **14**, the gate electrodes **15** and the data line **3**, an interlayer insulating film **16** is formed. As illustrated in **FIG. 3C, a** source electrode **17** and a drain electrode **18** are formed in an island shape. The source electrode **17** is connected to one n-type impurity high concentration region **13***d* of the polysilicone thin film **13** through a contact hole **19** provided to the interlayer insulating film **16** and the gate insulating film **14**.

[**0044**] One end of the drain electrode **18** is connected to the other n-type impurity high concentration region **13***d* of the polysilicone thin film **13** through a contact hole **20** provided to the interlayer insulating film **16** and the gate insulating film **14**. The other end of the drain electrode **18** is connected to the connecting portion **3***a* of the data line **3** through a contact hole **21** provided to the interlayer insulating film **16**.

[**0045**] As illustrated in **FIG. 3**C, the scanning line **2** is formed on a predetermined portion of the upper surface of the interlayer insulating film **16**. A connecting portion **2***a* formed on a predetermined portion of the scanning line **2** is connected to the common connecting portion **15***a* of the gate electrodes **15** through a contact hole **22** provided to the interlayer insulating film **16**. As illustrated in **FIGS. 2 and** 3C, the auxiliary capacitive electrode **6** is formed on a predetermined portion of the upper surface of the interlayer insulating film **16**. In this case, electrode portions **6***b* and **6***c* of the auxiliary capacitive electrode **6** are formed on the interlayer insulating film **16**, so as to cover the data lines **3**.

[**0046**] On the upper surfaces of the interlayer insulating film **16**, the source electrode **17** and the like, an overcoat film **23** is formed. On a predetermined portion of the upper surface of the overcoat film **23**, the pixel electrode **5** is formed. The pixel electrode **5** is connected to the source electrode **17** through a contact hole **24** provided to the overcoat film **23**.

[**0047**] Two divided gate electrodes **15** formed on the gate insulating film **14** cover the polysilicone thin film **13** to oppose to two channel regions **13***b* of the polysilicone thin film **13**, respectively. In this way, the thin film transistor **4** having the double gate structure is structured by the polysilicone thin film **13**, the gate insulating film **14**, the gate electrodes **15**, the source electrode **17**, and the drain electrode **18**.

[**0048**] An explanation will be next given of an example of a method for manufacturing the thin film transistor panel having the aforementioned structure. First of all, as illustrated in **FIG. 4**, on the upper surface of the glass substrate **1**, the first underlying insulating film **11** of silicon nitride, the second underlying insulating film **12** of silicon oxide, and an amorphous silicon thin film **31** are continuously formed by a plasma CVD (Chemical Vapor Deposition) method. Next, the amorphous silicon thin film **31** is crystallized by irradiation of excimer lasers to form a polysilicone thin film **32**.

[**0049**] Next, as illustrated in **FIG. 5**, on the upper surface of the polysilicone thin film **32**, there is formed resist pattern **33** having openings **33***a* formed on portions corresponding to the forming regions of the n-type impurity high concentration region **13***d* as illustrated in **FIG. 2**. Next, the resist pattern **33** is used as a mask and n-type impurities are injected threreonto with a high concentration. Thereafter, the resist pattern **33** is peeled from the polysilicone thin film **32**.

[**0050**] Next, the polysilicone thin film **32** is patterned to form the polysilicone thin film **13** on a predetermined portion of the upper surface of the second underlying insulating film **12** as illustrated in **FIG. 6**. Sequentially, on the upper surfaces of the second underlying insulating film **12** and the polysilicone thin film **13**, the gate insulating film **14** of silicon oxide is formed by a plasma CVD method. Next, on the upper surface of the gate insulating film **14**, a metallic film of Al and the like is formed by a sputtering method. Then, by patterning the formed metallic film, the gate electrodes **15** having the common connecting portion **15***a* and the data line **3** having the connecting portion **3***a*, as illustrated in **FIG. 3**B, are formed.

[**0051**] Next, as illustrated in **FIG. 7**, two gate electrodes **15** and the data line **3** are used as a mask and n-type impurities are injected with a low concentration. As a result, the n-type impurity low concentration region **13***a* is formed on a region of the polysilicone thin film **13**, which corresponds to a portion between two gate electrodes **15**. Furthermore, channel regions **13***b* each having an intrinsic region are formed on regions directly below two gate electrodes **15**. Moreover, n-type impurity low concentration regions **13***c* are formed at both sides of the channel regions **13***b*, and n-type impurity high concentration regions **13***d* are formed at both sides of the n-type impurity low concentration regions **13***c*. Next, in a nitrogen gas atmosphere, anneal processing is performed at temperature of about 500° C. for about one hour. As a result, the injected impurities are activated.

[**0052**] As illustrated in **FIG. 8**, on the upper surfaces of the gate insulating film **14**, the gate electrodes **15** and the data line **3**, the interlayer insulating film **16** of silicon nitride is formed by a plasma CVD method. Next, openings **19** and **20** are formed to the interlayer insulating film **16** and the gate insulating film **14**, so as to reach the high n-type impurity concentration regions **13***d* of the polysilicone thin film **13**. Moreover, an opening **21** is formed to the interlayer insulating film **16**, so as to reach the connecting portion **3***a* of the data line **3**. Furthermore, as illustrated in **FIGS. 3B and 3C**, an opening **22** is formed to the interlayer insulating film **16**, so as to reach the common connection portion **15***a* of two gate electrodes **15**. Next, an Al film and a Cr film (or Mo film) for ITO contact are successively formed in the openings **19**, **20**, **21** and **22** and on the upper surface of the interlayer insulating film **16** by a sputtering method. As a result, a metal film **34** is formed.

[**0053**] After that, by patterning the metal film **34**, the source electrode **17**, the drain electrode **18**, the scanning line **2** with the connecting portion **2***a*, and the auxiliary capacitive electrode **6** are respectively formed on predetermined portions of the upper surface of the interlayer insulating film **16**, as illustrated in **FIGS. 2 and 3**. Under this condition, the source electrode **17** is connected to one n-type impurity high concentration region **13***d* of the polysilicone thin film **13** through the contact hole **19**. Moreover, one end of the drain electrode **18** is connected to the other n-type impurity high concentration region **13***d* of the polysilicone thin film **13** through the contact hole **20**. Furthermore, the other end of the drain electrode **18** is connected to the connecting portion **3***a* of the data line **3** through the contact hole **21**. Also, the connecting portion **2***a* of the scanning line **2** is connected to the common connecting portion **15***a* of two gate electrodes **15** through the contact hole **22**.

[**0054**] Next, on the upper surfaces of the interlayer insulating film **16**, the source electrode **17** and the like, the overcoat film **23** of silicon nitride is formed by a plasma CVD method. Next, a contact hole **24** is formed on a predetermined portion of the overcoat film **23**, so as to reach the source electrode **17**. Sequentially, an ITO film is formed on the upper surface of the overcoat film **23** by a sputtering method. Then, the formed ITO film is patterned to form the pixel electrode **5** connected to the source electrode **17** through the contact hole **24**. Thus, the thin film transistor panel as illustrated in **FIGS. 1 and 2** can be obtained.

[**0055**] In the liquid crystal display device having the above-obtained thin film transistor panel, the electrode portions **6***b* and **6***c* of the auxiliary capacitive electrode **6** each having a larger width than that of the data line **3** are formed between the edge portions of the pixel electrodes **5** and the data lines **3**. For this reason, the electrode portions **6***b* and **6***c* can prevent the coupling capacitance from occurring between the edge portions of the pixel electrodes **5** and the data lines **3**. Accordingly, it is possible to prevent occurrence of vertical crosstalk and achieve a high display characteristic.

[**0056**] The aforementioned manufacturing method includes first to fifth processes. The first process forms the data line **3** and the island gate electrodes **15** on the gate insulating film **14**. The second process forms the contact holes **19** and **20** through the interlayer insulating film **16** and the gate insulating film **14**. The third process forms the scanning line **2**, the auxiliary capacitive electrode **6**, the island source electrode **17** and the island drain electrode **18** on the interlayer insulating film **16**. The fourth process forms the contact hole **24** to the overcoat film **23**. The fifth process forms the pixel electrode **5** on the overcoat film **23**. While, for example, a manufacturing method for the display device illustrated in **FIGS. 1 and 4** of the above-described Unexamined Japanese Patent Application KOKAI Publication No. H1-156725 includes first to fifth processes. The first process forms a scanning line and a gate electrode on a gate insulating film. The second process forms a contact hole passing through an interlayer insulating film and the gate insulating film, so as to reach one source and drain regions. The third process forms a data line on the interlayer insulating film. The fourth process forms a contact hole passing through an overcoat film, the interlayer insulating film and the gate insulating film, so as to reach the other source and drain regions. The fifth process forms a pixel electrode on the overcoat film. Accordingly, even if the gate electrode **15**, the source electrode **17** and the drain electrode **18** are formed in an island shape in the above-mentioned manufacturing method, the number of manufacturing processes does not increase.

[**0057**] (Second Embodiment)

[**0058**] **FIG. 9** is a plan view of a main part of a thin film transistor panel in a liquid crystal display device shown as respective layers being seen through according to a second embodiment of the present invention. In this case, the edge portion of each pixel electrode **5** is also hatched with oblique short solid lines for the purpose of clarifying **FIG. 9**. The point, which is largely different from the case shown in **FIGS. 1 and 2**, relates to a thin film transistor structure having a double gate structure. Though the detailed explanation is set forth below, in each pixel of the thin film transistor panel of the second embodiment, a polysilicone thin film is flat and U-shaped and a gate electrode is linearly formed to bridge the opposing portions of the U-shaped polysilicone thin film. Similar to the first embodiment, the gate electrode and a scanning line are connected to each other through a contact hole formed to an interlayer insulating film. However, in this case, the width of the scanning line can be set to the same or less than the width of the gate electrode. This makes it possible to improve the aperture ratio as compared with the double gate structure where the divided portions of the U-shaped gate electrode projects from the scanning line.

[**0059**] The specific structure of the thin film transistor panel in one pixel will be now explained. **FIG. 10** is a cross-sectional view taken on the line X-X of **FIG. 9**, **FIG. 11** is a cross-sectional view taken on the line XI-XI of **FIG. 9**, and **FIG. 12** is a cross sectional view taken on the line XII-XII of **FIG. 9**. The first and second underlying insulating films **11** and **12** are formed on the upper surface of the glass substrate **1**. The polysilicone thin film **13** is formed on a predetermined portion of the upper surface of the second underlying insulating film **12**. As illustrated in **FIG. 13**A, the polysilicone thin film **13** is substantially U-shaped and symmetrical with a vertical center line, and includes multiple gate (channel) regions. At a substantially central portion of each of a pair of side bars, the channel region **13***b* having an intrinsic region is formed. Moreover, the n-type impurity low concentration regions **13***c* are formed at both sides of the channel region **13***b*. Furthermore, the n-type impurity high concentration regions **13***d* are formed at both sides of the n-type impurity low concentration regions **13***c*.

[**0060**] On the upper surfaces of the second underlying insulating film **12** and the polysilicone thin film **13**, the gate insulating film **14** is formed. One linear gate electrode **15** is formed in an island shape on a predetermined portion of the upper surface of the gate insulting film **14**, so as to cover two channel regions **13***b* of the polysilicone thin film **13** as illustrated in **FIG. 13B**. In this case, connecting portions **15***b* are provided at both ends of the gate electrode **15**. On a predetermined portion of the upper surface of the gate insulating film **14**, the data line **3** is formed as illustrated in **FIG. 13B**. The connecting portion **3***a* with a large width is formed on a predetermined portion of the data line **3**.

[**0061**] On the upper surfaces of the gate insulating film **14**, the gate electrode **15** and the data line **3**, the interlayer insulating film **16** is formed. As illustrated in **FIG. 13**C, the source electrode **17** and the drain electrode **18** are formed on predetermined portions of the upper surface of the interlayer insulating film **16** in an island shape, respectively. The source electrode **17** is connected to one n-type impurity high concentration region **13***d* of the polysilicone thin film **13** through the contact hole **19** provided to the interlayer insulating film **16** and the gate insulating film **14**.

[**0062**] One end of the drain electrode **18** is connected to the other n-type impurity high concentration region **13***d* of the polysilicone thin film **13** through the contact hole **20** provided to the interlayer insulating film **16** and the gate insulating film **14**. The other end of the drain electrode **18** is connected to the connecting portion **3***a* of the data line **3** through the contact hole **21** provided to the interlayer insulating film **16**.

[**0063**] On a predetermined portion of the upper surface of the interlayer insulating film **16**, the scanning line **2** is formed as illustrated in **FIG. 13C**. In this case, the scanning line **2** has a narrow width portion **2***b* provided above a portion of the gate electrode **15**, which is sandwiched by the connecting portions **15***b*. The narrow width portion **2***b* is set to be narrower than the sandwiched portion. This structure is made to surely prevent the scanning line **2** from sticking out of the gate electrode **15** of lower layer in the width direction as seen from the plane, thereby an electric field is surely prevented from acting on the channel region. Both side portions of the narrow width portion **2***b* of the scanning line **2** are connected to the connecting portions **15***b* of the gate electrode **15** through the contact holes **22** provided to the interlayer insulating film **16**. Accordingly, the narrow width portion **2***b* of the scanning line **2** may be omitted. On a predetermined portion of the upper surface of the interlayer insulating film **16**, substantially the same auxiliary capacitive electrode **6** as the first embodiment is formed.

[**0064**] On the upper surfaces of the interlayer insulating film **16**, the source electrode **17** and the like, the overcoat film **23** is formed. On a predetermined portion of the upper surface of the overcoat film **23**, the pixel electrode **5** is formed. The pixel electrode **5** is connected to the source electrode **17** through the contact hole **24** provided to the overcoat film **23**.

[**0065**] In this way, the thin film transistor **4** having the double gate structure is structured by the polysilicone thin film **13** having two channel regions **13***b*, the gate insulating film **14**, the gate electrode **15**, the source electrode **17**, and the drain electrode **18**.

[**0066**] In addition, the thin film transistor panel manufacturing method of the second embodiment is substantially the same as the first embodiment, and the explanation is omitted. As mentioned above, in the thin film transistor panel of the second embodiment, the linear and island-shaped gate electrode **15** formed on the gate insulating film **14** and the scanning line **2** formed on the interlayer insulating film **16** are overlapped with each other as seen from the plane. This makes it possible to reduce the plane arranging space of the gate electrode **15** in the direction perpendicular to the scanning line **2**. As a result, a much higher aperture ratio can be achieved.

[**0067**] (Third Embodiment)

[**0068**] In order to increase an auxiliary capacitance that is formed of the auxiliary capacitive electrode **6** and the pixel electrode **5**, the following method can be used. Namely, in the process of forming the gate electrode **15** on the gate insulating film **14**, an auxiliary capacitive electrode of the lower layer is formed on a region overlapping with the polysilicone thin film **13** and the pixel electrode **5**, simultaneously, and the auxiliary capacitive electrode of the lower layer is connected to the auxiliary capacitive electrode **6** of the first and second embodiments. The third embodiment shows a thin film transistor panel in the above-manufactured liquid crystal display device. **FIG. 14** is a plan view of a main part of the thin film transistor panel in the liquid crystal display device shown as respective layers being seen through according to the third embodiment of the present invention, and **FIG. 15** is a cross-sectional view taken on the line XV-XV of **FIG. 14**. In this thin film transistor panel, on the interlayer insulating film **16**, there is formed an electrode portion **6***d* drawn from the electrode portion **6***a* of the auxiliary capacitive electrode **6** in a direction opposite to the drawing directions of electrode portions **6***b* and **6***c*, and corresponding to the lower side portion of the pixel electrode **5**. Moreover, on a region of the gate insulating film **14**, which corresponds to the forming regions of the electrode portion **6***d* and the source electrode **17**, an island electrode portion **6***e* is formed. The electrode portion **6***d* is connected to the electrode portion **6***e* through a contact hole provided to a predetermined portion of the interlayer insulating film **16**. The above-described structure is different from the structure shown in **FIGS. 1 and 2**.

[**0069**] In such a case, as auxiliary capacitances, there are further formed an auxiliary capacitance Cs**1** between the electrode portion **6***d* and the upper pixel electrode **5**, an auxiliary capacitance Cs**2** between the electrode portion **6***e* and the upper pixel electrode **5**, an auxiliary capacitance Cs**3** between the electrode portion **6***d* and the upper source electrode **17**, and an auxiliary capacitance Cs**4** between the electrode portion **6***e* and the lower n-type impurity high concentration region **13***d*. Accordingly, more auxiliary capacitances can be ensured.

[**0070**] (Fourth Embodiment)

[**0071**] **FIG. 16** is a cross-sectional view of a thin film transistor panel in a liquid crystal display device according to a fourth embodiment of the present invention, similar to **FIG. 15**. In this thin film transistor panel, the point different from the case shown in **FIG. 15** is that a relative thicker flatting film **26** formed of polyimide resin, epoxy resin or the like is used in place of the overcoat film **23** formed of silicon nitride. In this case, since the flatting film **26** is relatively thicker, a normal auxiliary capacitance Cs**0** between the auxiliary capacitive electrode **6** and the pixel electrode **5** shown in **FIG. 1** becomes small. However, since the auxiliary capacitances Cs**1**, Cs**2**, Cs**3**, and Cs**4** are formed in addition to this as mentioned above, necessary auxiliary capacitance can be fully ensured.

[**0072**] (Fifth Embodiment)

[**0073**] First to fourth embodiments showed the top gate type thin film transistor. However, the present invention can be applied to a bottom gate type thin film transistor. Moreover, if the auxiliary capacitive electrode is formed on only the portion overlapping with the data line, a much higher aperture ratio can be achieved. Fifth embodiment shows a thin film transistor panel in such an active matrix type liquid crystal display device. **FIG. 17** is a plan view of the thin film transistor panel shown as respective layers being seen through. This thin film transistor panel includes a glass substrate **101**. On the upper surface side of the glass substrate **101**, scanning lines **102** and data lines **103** are formed in such a manner as the manner set forth in the first embodiment. Then, in the vicinity of each intersection of scanning lines **102** and data lines **103**, a thin film transistor **104** and a pixel electrode **105** are formed. Moreover, auxiliary capacitive electrodes **106** are formed to be parallel with the data lines **103**, respectively.

[0074] In this case, right and left side portions of the pixel electrode **105** are overlapped with the auxiliary capacitive electrodes **106** arranged at the right and left sides of the pixel electrode **105**. Accordingly, a region, which is obtained by removing forming regions of the auxiliary capacitive electrodes **106** arranged at the right and left sides of the pixel electrode **105** and a forming region of the thin film transistor **104** from a forming region of the pixel electrode **105**, is used as a substantial pixel region. However, in order to prevent external light from being incident on the thin film transistors **104**, black masks are formed on portions, which correspond to at least the thin film transistors **104**, of a counter panel (not shown) provided to be opposite to the thin film transistor panel.

[0075] Each auxiliary capacitive electrode **106** is overlapped with the data line **103**. Moreover, though this is explained later, each of the auxiliary capacitive electrodes **106** is formed between the data line **103** and the pixel electrodes **105** in a thickness direction of the thin film transistor panel, namely, a vertical direction on paper of **FIG. 17**. Then, the width of each auxiliary capacitive electrode **106** (a length in a direction parallel to the scanning line **102**) is set to be wider than the width of the data line **103**. Accordingly, the data line **3** is entirely covered with the auxiliary capacitive electrode **106** not to oppose to the pixel electrodes **105** directly even if there is a positional shift in a direction parallel to the scanning line **102**.

[0076] Moreover, each auxiliary capacitive electrode **106** is formed over almost the entire area of the arranging region of the data line **103**. Thereby, even if the position of the auxiliary capacitive electrode **106** is shifted to the pixel electrode **105** in a direction perpendicular to the scanning line **102** in an alignment step, the auxiliary capacitive electrode **106** is overlapped with the pixel electrode **105** without fail. Accordingly, variations in the auxiliary capacitance caused by the positional shift are surely prevented.

[0077] Next, the specific structure of the thin film transistor panel will be explained. **FIG. 18** is a cross-sectional view taken on the line XVIII-XVIII of **FIG. 17**. On the upper surface of the glass substrate **101**, the scanning line **102** (**FIG. 17**) including a gate electrode **102***a* formed of chromium and molybdenum is formed. On the upper surfaces of the glass substrate **101**, the gate electrode **102***a* and the scanning line **102**, a gate insulating film **51** of silicon nitride is formed.

[0078] On the gate insulating film **51**, a semiconductor thin film **113** made of intrinsic amorphous silicon is formed so as to cover the gate electrode **102***a*. On a predetermined portion of the upper surface of the semiconductor thin film **113**, a channel protective film **52** made of silicon nitride is formed so as to overlap with the gate electrode **102***a*.

[0079] On the upper surface of the semiconductor thin film **113** and the both side portions of the upper surface of the channel protective film **52**, there are formed Ohmic contact layers **53** and **54** of n-type amorphous silicon. On the upper surfaces of the Ohmic contact layers **53** and **54**, there are formed a source electrode **57** and a drain electrode **58** of chromium and molybdenum, respectively.

[0080] Then, the thin film transistor **104** is formed by the gate electrode **102***a*, the gate insulating film **51**, the semiconductor thin film **113**, the channel protective film **52**, the Ohmic contact layers **53** and **54**, the source electrode **57** and the drain electrode **58**.

[0081] On the upper surface of the gate insulating film **51**, the data line **103** is formed. In this case, the data line **103** has a structure including three layers of intrinsic amorphous silicon **103***a, n*-type amorphous silicon **103***b* and a metallic layer **103***c* formed of chromium and molybdenum. Then, the intrinsic amorphous silicon **103***a*, the n-type amorphous silicon **103***b* and the metallic layer **103***c* are connected to the semiconductor thin film **113**, the Ohmic contact layer **54** and the drain electrode **58**, respectively.

[0082] On the upper surfaces of the gate insulating film **51**, the thin film transistor **104** and the data line **103**, there is formed an interlayer insulating film **59** of silicon nitride. On the upper surface of the interlayer insulating film **59**, the auxiliary capacitive electrode **106** of chromium and molybdenum is formed so as to cover the data line **103**.

[0083] On the upper surfaces of the interlayer insulating film **59** and the auxiliary capacitive electrode **106**, an overcoat film **123** of silicon nitride is formed. A contact hole **61** is formed to the interlayer insulating film **59** and the overcoat film **123**, so as to reach the source electrode **57**. On the upper surface of the overcoat film **123**, the pixel electrode **105** of transparent conductive material such as ITO or ZnO is formed so as to be connected to the source electrode **57** through the contact hole **61**.

[0084] Then, in the active matrix type liquid crystal display device including the above-structured thin film transistor panel, the auxiliary capacitive electrode **106** having a width larger than the data line **103** are formed between the data line **103** and the pixel electrodes **105**. For this reason, the auxiliary capacitive electrode **106** can prevent occurrence of coupling capacitance between the data line **103** and the pixel electrodes **105**. Accordingly, this makes it possible to prevent occurrence of vertical crosstalk and achieve a high display characteristic.

[0085] Moreover, as illustrated in **FIG. 17**, the vicinity of each intersection of the scanning lines **102** and data lines **103** can be shielded by the auxiliary capacitive electrode **106**. This makes it possible to largely increase the aperture ratio as compared with the case in which the corresponding vicinity is shielded by a black mask which is formed on the counter panel by a processing with relatively poor precision.

[0086] Moreover, as illustrated in **FIG. 17**, only the left and right side portions of the pixel electrode **105** are overlapped with the auxiliary capacitive electrodes **106** arranged at the right and left sides of the pixel electrode **105**. This makes it possible to largely increase the aperture ratio as compared with the case in which the U-shape auxiliary capacitive electrode having two extended portions extending along the right and left side portions of the pixel electrode **105** are overlapped with three side portions of the pixel electrode **105**.

[0087] (Sixth Embodiment)

[0088] **FIG. 19** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a sixth embodiment of the present invention, similar to **FIG. 17**. In **FIG. 19**, the point different form the case shown in **FIG. 17** is that the upper side portion of the pixel electrode **105** is extended and overlapped with the scanning line **102**. In this case, to surely prevent the upper side portion of the pixel electrode **105** from interfering with the thin film transistor (not shown) in the previous line after passing over the scanning line **102**, the width of the scanning line **102** is set to be larger than the case shown in **FIG. 17** to some degree.

[0089] In this way, according to the sixth embodiment, the upper side portion of the pixel electrode **105** is extended and overlapped with the scanning line **102**. This eliminates a gap (light leak portion), which exists between the upper side portion of the pixel electrode **105** and the scanning line **102** as shown in **FIG. 17**. Accordingly, there is no need to shield the gap by a black mask provided on the counter panel and the aperture ratio can be largely increased as compared with the case of shielding by the black mask.

[0090] Moreover, since the upper side portion of the pixel electrode **105** is extended and overlapped with the scanning line **102**, the electric field between the upper side portion of the pixel electrode **105** and the scanning line **102** more increases. As a result, the liquid crystal disposed between the upper side portion of the pixel electrode **105** and the counter panel is strongly restricted by off-potential of the scanning line **102** overlapping with the upper side portion of the pixel electrode **105**, so that disclination lessens as compared with the case shown in **FIG. 17**. This makes it possible to reduce the black mask, which is formed on the counter panel to hide disclination, to some degree and increase the aperture ratio.

[0091] (Seventh Embodiment)

[0092] **FIG. 20** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a seventh embodiment of the present invention, similar to **FIG. 19**. In **FIG. 20**, the auxiliary capacitive electrode **106** placed at the left side of the pixel electrode **105** has a first extending portion **106*a*** extending in parallel with the scanning line **102**. The first extending portion **106*a*** extends right from a portion in the vicinity of the thin film transistor **104**. At the upper side of the gate electrode **102*a*** of the thin film transistor **104**, the first extending portion **106*a*** is overlapped with the left portion of the lower side portion of the pixel electrode **105**. Moreover, the auxiliary capacitive electrode **106** placed at the right side of the pixel electrode **105** has a second extending portion **106*b*** extending in parallel with the scanning line **102**. The second extending portion **106*b*** extends left from a portion in the vicinity of the scanning line **102**. The second extending portion **106*b*** is overlapped with the right portion of the lower side portion of the pixel electrode **105**, the scanning line **102**, and the right portion of the upper side portion of the adjacent pixel electrode **105**A. The above-explained structure is different from the structure shown in **FIG. 19**. In this case, a connecting portion (namely, a contact hole **61** in **FIG. 18**) between the source electrode **57** of the thin film transistor **104** and the pixel electrode **105** is formed at a position that avoids the second extending portion **106*b***.

[0093] In this way, in the seventh embodiment, the first extending portion **106*a*** extended from the left auxiliary capacitive electrode **106** is placed between the gate electrode **102*a*** of the thin film transistor **104** and the left portion of the lower side portion of the pixel electrode **105**. Moreover, the second extending portion **106*b*** extended from the right auxiliary capacitive electrode **106** is placed between the right portion of the lower side portion of the pixel electrode **105** and the scanning line **102**. This makes it possible to reduce a coupling capacitance (Cgs) between the pixel electrode **105** and the gate electrode **102*a*** and between the pixel electrode **105** and the scanning line **102**. This means that variations in the pixel potential (field through voltage ΔV) influenced by variations of the coupling capacitance can be controlled with a small auxiliary capacitance at the time of AC drive. This enables to improve flicker that adversely affects the display quality and burning that adversely affects reliability.

[0094] Moreover, a gap between the right portion of the lower side portion of the pixel electrode **105** and the scanning line **102** is covered with the second extending portion **106*b*** to make it possible to eliminate a light leak from the gap. Accordingly, there is no need to shield the gap by a black mask provided on the counter panel and the aperture ratio can be largely increased as compared with the case of shielding by the black mask.

[0095] (Eighth Embodiment)

[0096] **FIG. 21** is a plan view of a thin film transistor panel shown as respective layers being seen through according to an eighth embodiment of the present invention, similar to **FIG. 1**. In **FIG. 21**, the auxiliary capacitive electrodes **106** at right and left sides of the pixel electrode **105** are formed together with connecting portions **106*c*** which are formed in the vicinity of the scanning lines **102**, so as to be entirely connected with each other via the connecting portions **106*c***. Each connecting portion **106*c*** is overlapped with the lower side portion of the pixel electrode **105** and the upper side portion of the adjacent pixel electrode **105**A. The above-explained structure is different from the structure shown in **FIG. 17**. In this case, a connecting portion (namely, the contact hole **61** in **FIG. 18**) between the source electrode **57** of the thin film transistor **104** and the pixel electrode **105** is formed at a position that avoids the connecting portion **106*c***.

[0097] In this way, in the eighth embodiment, each connecting portion **106*c*** is overlapped with the lower side portion of the pixel electrode **105** and the upper side portion of the adjacent pixel electrode **105**A. This makes it possible to cover all regions except the central portion (transparent pixel) of the pixel electrode **10S** with the auxiliary capacitive electrodes **106** including the connecting portions **106*c***. Accordingly, there is no need to provide a black mask for preventing a light leak on the counter panel and a considerably high aperture ratio can be achieved.

[0098] Moreover, in the thin film transistor **104** having the semiconductor thin film **113** (**FIG. 18**) formed of intrinsic amorphous silicon, the light leak easily occurs. However, since each thin film transistor **104** (except a part of the source electrode **57**) can be completely covered with the connecting portion **106*c***, considerably high light leak control can be obtained.

[0099] Furthermore, since the auxiliary capacitive electrodes **106** provided at right and left sides of the pixel electrode **105** are connected to each other by the connecting portions **106***c*, the auxiliary capacitive electrodes **106** including the connecting portions **106***c* are arrayed in a lattice. Accordingly, even if a break occurs anywhere in the auxiliary capacitive electrodes **106** including the connecting portions **106***c*, a current path can be ensured and a degree of risk that failure will occur by the break can be considerably reduced.

[0100] Moreover, in the case where the auxiliary capacitive electrodes **106** including the connecting portions **106***c* are arrayed in a lattice, the resistance value of the auxiliary capacitive electrodes **106** is small as compared with the case in which the auxiliary capacitive electrodes **106** are shaped stripe as illustrated in, for example, **FIG. 17**. This reduces a time constant, so that the liquid crystal responds quickly. In addition, though this is not illustrated, the auxiliary capacitive electrodes **106** are connected to counter electrodes formed on the opposing panel and driven in synchronization with the counter electrodes. Moreover, in order to correct jumping voltage ΔV at the time of AC drive, the counter electrodes are driven in synchronization with 1H signal or 1V signal. For this reason, the resistance value is reduced to lessen the time constant, so that the liquid crystal responds quickly.

[0101] (Ninth Embodiment)

[0102] **FIG. 22** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a ninth embodiment of the present invention, similar to **FIG. 21**. In **FIG. 22**, the point different from the case shown in **FIG. 21** is that the connecting portions **106***c* of the auxiliary capacitive electrodes **106** are formed to be overlapped with the scanning lines **102** and not to be overlapped with the pixel electrodes **105**. As a result, a part of the pixel electrode **105** directly opposes to the scanning line **102** via the insulating films. Namely, in **FIG. 22**, each of the connecting portions **106***c* of the auxiliary capacitive electrodes **106** is shaped to be overlapped with the upper portion of each scanning line **102**. Moreover, in each region where dots are written, the scanning line **102** opposes to the pixel electrode **105** via the gate insulating film **51**, the interlayer insulating film **59** and the overcoat film **123** **(FIG. 18)**. Namely, in each region where the dots are written, the connecting portion **106***c* of the auxiliary capacitive electrodes **106** is not provided between the scanning line **102** and the pixel electrode **105**.

[0103] In this way, according to the ninth embodiment, since the scanning line **102** is overlapped with only the part of the pixel electrode **105** via only the insulating films instead of the connecting portion **106***c* of the auxiliary capacitive electrode **106**, the electric field between the pixel electrode **105** and the scanning line **102** more increases. As a result, the liquid crystal disposed between the part of the pixel electrode **105** and the counter panel is strongly restricted by off-potential of the scanning line **102** overlapping with the upper side portion of the pixel electrode **105**, so that disclination lessens. This makes it possible to reduce the black mask, which is formed on the counter panel to hide disclination, to some degree and increase the aperture ratio.

[0104] (Tenth Embodiment)

[0105] **FIG. 23** is a plan view of a thin film transistor panel shown as respective layers being seen through according to a tenth embodiment of the present invention, similar to **FIG. 22**. In **FIG. 23**, the point different from the case shown in **FIG. 22** is that a transparent auxiliary capacitive electrode **106**A, which is formed of transparent conductive material such as ITO or ZnO, is provided as a lower conductive layer directly below each auxiliary capacitive electrode **106** which is formed on the interlayer insulating film **59** **(FIG. 18)** and includes the connecting portion **106***c*

[0106] In this case, in a region corresponding to the right and left side portions and the lower side portion of the pixel electrode **105**, the transparent auxiliary capacitive electrode **106**A is formed up to a slightly inner position than the auxiliary capacitive electrodes **106** including the coupling portions **106***c*. Moreover, the transparent auxiliary capacitive electrode **106**A is not formed on the connecting portion between the source electrode **57** of the thin film transistor **104** and the pixel electrode **105** (namely, contact hole **61** in **FIG. 18**) and the region corresponding to the vicinity thereof. Furthermore, the auxiliary capacitive electrode **106** including the connecting portions **106***c* is formed of shielding metal of chromium and molybdenum and the like that are electrically contactable with the transparent auxiliary capacitive electrode **106**A of transparent conductive material such as ITO or ZnO.

[0107] In this way, according to the tenth embodiment, in the region corresponding to the right and left side portions and the lower side portion of the pixel electrode **105**, the transparent auxiliary capacitive electrode **106**A is formed up to the slightly inner position than the auxiliary capacitive electrode **106** including the coupling portions **106***c*. For this reason, the auxiliary capacitive portion is also formed by an overlapping portion of a part of the transparent auxiliary capacitive electrode **106**A which is placed in the inner position than the auxiliary capacitive electrode **106** and the pixel electrode **105**. Moreover, since the transparent auxiliary capacitive electrode **106**A is formed of the transparent conductive material such as ITO or ZnO, no influence is exerted upon the aperture ratio. The size and shape of the transparent auxiliary capacitive electrode **106**A are appropriately selected to make it possible to adjust the auxiliary capacitance without exerting an influence upon the aperture ratio.

[0108] In addition, with reference to **FIG. 18**, it can be explained that the transparent auxiliary capacitive electrode **106**A may be formed on the upper surface of the interlayer insulating film **59** including the auxiliary capacitive electrode **106**. Moreover, the transparent auxiliary capacitive electrode **106**A may be formed on the upper surface of an upper interlayer insulating film (not shown) formed on the upper surfaces of the interlayer insulating film **59** and the auxiliary capacitive electrode **106**, so that the transparent auxiliary capacitive electrode **106**A is connected to the auxiliary capacitive electrode **106** through a contact hole formed to the upper interlayer insulating film. Furthermore, the transparent auxiliary capacitive electrode **106**A may be formed under the upper interlayer insulating film and the auxiliary capacitive electrode **106** may be formed on the upper interlayer insulting film, so that the transparent auxiliary capacitive electrode **106**A is connected to the auxiliary capacitive electrode **106** through the contact hole formed to the upper interlayer insulating film.

[0109] As explained above, according to the present invention, the part of the auxiliary capacitive electrode is formed between the pixel electrodes and the data line via the insulating films. This makes it possible to prevent occurrence of the coupling capacitance between the pixel electrodes and the data line. Accordingly, it is possible to prevent occurrence of the vertical crosstalk.

[0110] Various embodiments and changes may be made thereunto without departing from the broad spirit and scope of the invention. The above-described embodiments are intended to illustrate the present invention, not to limit the scope of the present invention. The scope of the present invention is shown by the attached claims rather than the embodiments. Various modifications made within the meaning of an equivalent of the claims of the invention and within the claims are to be regarded to be in the scope of the present invention.

[0111] This application is based on Japanese Patent Application No. 2003-61440 filed on Mar. 7, 2003 and Japanese Patent Application No. 2003-137232 filed on May 15, 2003 and including specification, claims, drawings and summary. The disclosure of the above Japanese Patent Application is incorporated herein by reference in its entirety.

What is claimed is:

1. A display device comprising:

a substrate;

a plurality of scanning lines formed in parallel with each other on said substrate in one direction

a plurality of data lines formed in parallel with each other on said substrate in orthogonal to said scanning lines;

a thin film transistor being formed in the vicinity of each intersection of said scanning lines and said data lines and having a semiconductor thin film, a gate electrode connected to one of said scanning lines, a source electrode, a drain electrode connected to one of said data lines;

pixel electrodes each connected to the source electrode of said thin film transistor;

auxiliary capacitive electrodes each having an overlap region that overlaps with said pixel electrodes and forming an auxiliary capacitance with said pixel electrodes;

a first insulating film arranged between said auxiliary capacitive electrodes and said data lines; and

a second insulting film arranged between said pixel electrodes and said auxiliary capacitive electrodes.

2. The display device according to claim 1, wherein the overlap region of each of said auxiliary capacitive electrodes has a larger width than the width of each of said data lines.

3. The display device according to claim 1, wherein the gate electrode and said data lines are formed on the same plane.

4. The display device according to claim 3, wherein said first insulating film is formed on the gate electrode and said data lines, and said scanning lines, the source electrode, the drain electrode, and said auxiliary capacitive electrodes are formed on said first insulating film.

5. The display device according to claim 1, wherein said thin film transistor includes a gate insulating film, and said gate electrode and said data lines are formed on the gate insulating film.

6. The display device according to claim 5, wherein the drain electrode is formed on said first insulating film, and connected to the semiconductor thin film through a contact hole formed to the gate insulating film and said first insulating film and connected to one of said data lines through a contact hole formed to said first insulating film.

7. The display device according to claim 5, wherein the source electrode is formed on said first insulating film, and connected to the semiconductor thin film through a contact hole formed to the gate insulating film and said first insulating film, and each of said pixel electrodes is connected to the source electrode through a contact hole formed to said second insulting film.

8. The display device according to claim 5, wherein the gate electrode is formed under each of said scanning lines.

9. The display device according to claim 8, wherein the width of the gate electrode is larger than the width of each of said scanning lines.

10. The display device according to claim 8, wherein the gate electrode comprises multiple gate electrodes which are arranged in a region corresponding to a portion between the source electrode and the drain electrode and connected to each other by a common connecting portion.

11. The display device according to claim 8, wherein the semiconductor thin film has a U shape, and the gate electrode is formed to cross multiple portions of the U-shape semiconductor thin film, seen from the plane.

12. The display device according to claim 5, further comprising a second auxiliary capacitive electrode formed on said gate insulating film to be overlapped with the semiconductor thin film.

13. The display device according to claim 5, further comprising a second auxiliary capacitive electrode formed on said gate insulating film to be overlapped with the source electrode.

14. The display device according to claim 5, further comprising a second auxiliary capacitive electrode formed on said gate insulating film to be overlapped with the semiconductor thin film and the source electrode.

15. The display device according to claim 14, wherein said second insulating film is formed of resin.

16. The display device according to claim 1, wherein part of each of said pixel electrodes is overlapped with said scanning lines adjacent to each of said pixel electrodes.

17. The display device according to claim 1, wherein said thin film transistor has a gate insulating film,

said semiconductor thin film and said data lines are formed on the gate insulating film,

the source electrode and the drain electrode are formed on said semiconductor thin film, and

said first insulating film is formed on said data lines, the source electrode, the drain electrode, and the gate insulating film in a region where said data lines, the source electrode, the drain electrode are not formed.

18. The display device according to claim 1, wherein an extending portion that is overlapped with at least the part of a gap between each of said pixel electrodes and the gate electrode of said thin film transistor is extended from each of said auxiliary capacitive electrodes.

19. The display device according to claim 1, wherein an extending portion that is overlapped with a gap between each of said pixel electrodes and each of said scanning lines, and is extended from each of said auxiliary capacitive electrodes.

20. The display device according to claim 1, further comprising a transparent auxiliary capacitive line being overlapped with at least the overlap region of each of said auxiliary capacitive electrodes and having a larger width than the width of each of said auxiliary capacitive electrodes.

21. The display device according to claim 1, wherein a connecting portion that connects said auxiliary capacitive electrodes to each other is formed between said auxiliary capacitive electrodes adjacent to other, and said auxiliary capacitive electrodes are arrayed in a lattice as a whole.

22. The display device according to claim 21, wherein said connecting portion is formed in a region including a gap between each of said pixel electrodes and each of said scanning lines and a region corresponding to the entirety of one of said scanning lines.

23. The display device according to claim 21, wherein said connecting portion is overlapped with the semiconductor thin film of said thin film transistor.

24. The display device according to claim 21, wherein one part of each of said scanning lines is overlapped with the connecting portion of said auxiliary capacitive electrodes and the other part is overlapped with an adjacent pixel electrode instead of being overlapped with the connecting portion.

* * * * *

专利名称(译)	具有辅助电容电极的液晶显示装置		
公开(公告)号	US20040174483A1	公开(公告)日	2004-09-09
申请号	US10/794276	申请日	2004-03-04
[标]申请(专利权)人(译)	中村YAYOI 石井弘光 SHIMOMAKI SHINICHI 渡边仁		
申请(专利权)人(译)	中村YAYOI 石井弘光 SHIMOMAKI SHINICHI 渡边仁		
当前申请(专利权)人(译)	中村YAYOI 石井弘光 SHIMOMAKI SHINICHI 渡边仁		
[标]发明人	NAKAMURA YAYOI ISHII HIROMITSU SHIMOMAKI SHINICHI WATANABE HITOSHI		
发明人	NAKAMURA, YAYOI ISHII, HIROMITSU SHIMOMAKI, SHINICHI WATANABE, HITOSHI		
IPC分类号	G02F1/1343 G02F1/136 G02F1/1362 G09F9/00 H01L29/786		
CPC分类号	G02F1/136209 G02F2201/40 G02F1/136213		
优先权	2003137232 2003-05-15 JP 2003061440 2003-03-07 JP		
外部链接	Espacenet USPTO		

摘要(译)

一种显示装置，包括：基板，在一个方向上在基板上彼此平行形成的多条扫描线，在基板上与扫描线正交地彼此平行形成的多条数据线，薄膜晶体管形成在扫描线和数据线的每个交叉点附近并具有半导体薄膜，连接到一条扫描线的栅电极，连接到一条扫描线的源电极，漏电极;每个像素电极连接到薄膜晶体管的源电极，每个辅助电容电极具有与像素电极重叠并与像素电极形成辅助电容的重叠区域，第一绝缘膜设置在辅助电容电极和数据线和布置在像素电极和辅助电容电极之间的第二绝缘膜。