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(54) DRIVING DEVICE AND A DRIVING METHOD FOR A DISPLAY DEVICE

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(57) ABSTRACT

Disclosed is a display device (e.g., a liquid crystal display), and an apparatus and a method for driving the display device. The LCD includes an LCD panel having a plurality of gate lines, a plurality of data lines insulated from and intersecting the gate lines, and a plurality of TFTs each having a gate electrode connected to one of the gate lines and a source electrode each connected to one of the data lines; a gate driver for sequentially supplying gate drive signals to the gate lines to turn the TFTs ON; and a data driver for dividing the data lines into a certain number of blocks, each block having a predetermined number of data lines, and applying image signals to the data lines in an (n)th block, and applying precharging voltages to the data lines in an (n+j)th block. The apparatus includes the gate driver and the data driver. The method includes the steps of sequentially supplying the gate drive signals to the gate lines to turn the TFTs ON; and applying the image signals to the data lines in an (n)th block, and applying precharging voltages to the data lines in an (n+j)th block.

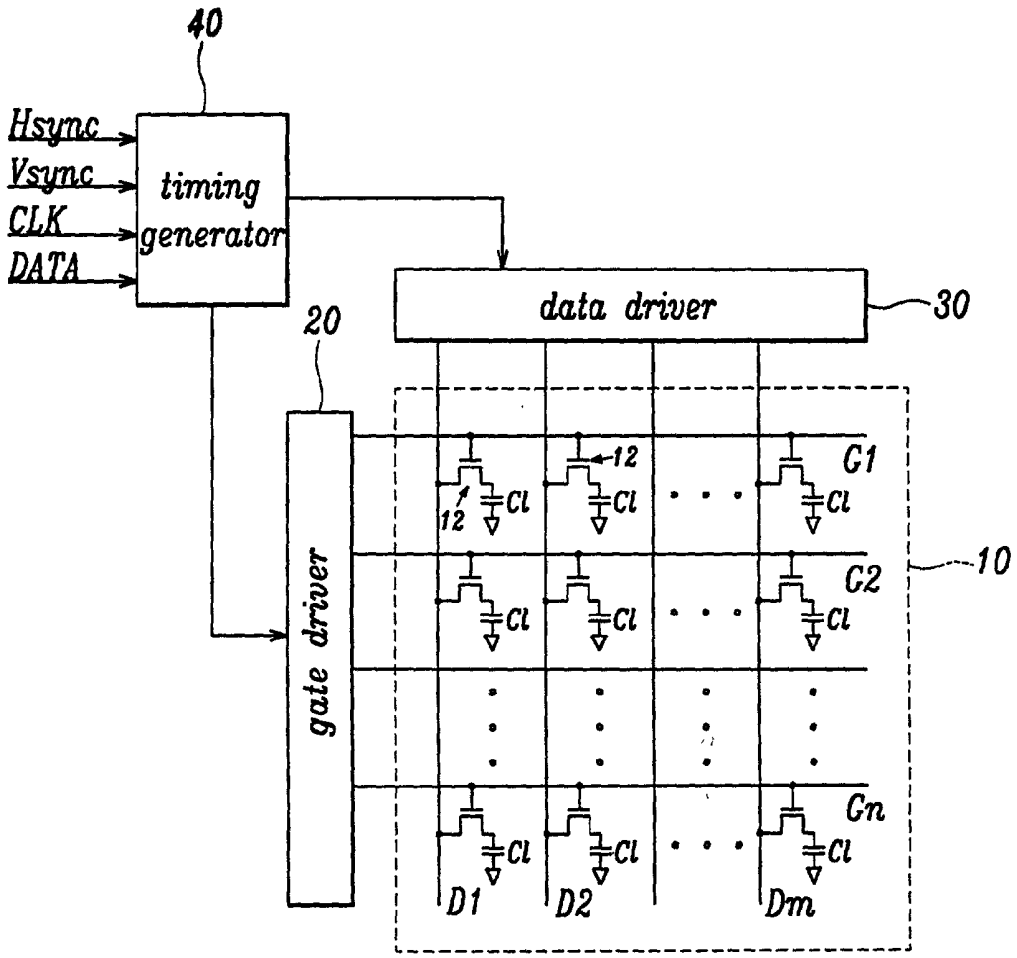


FIG. 1

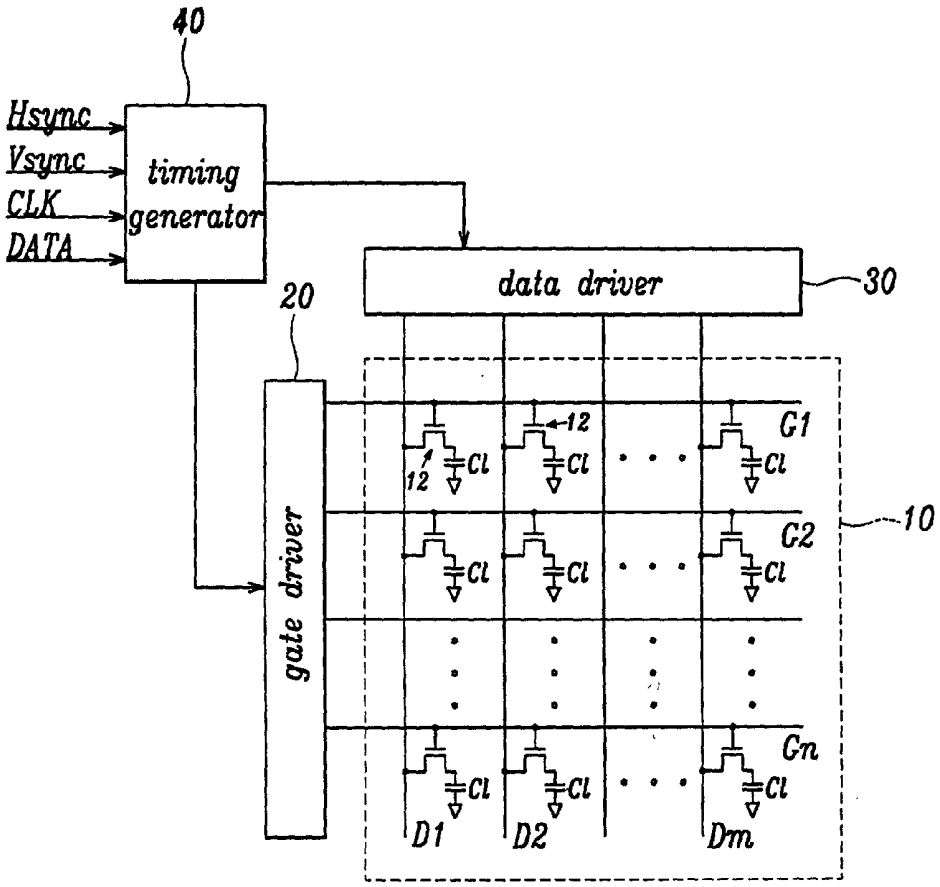


FIG. 2

(PRIOR ART)

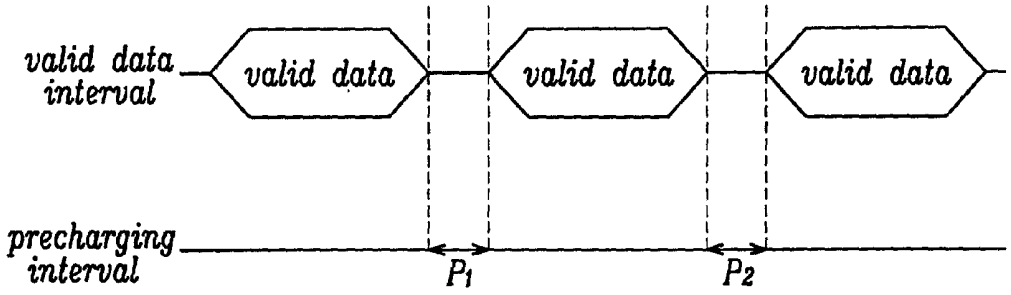


FIG.3

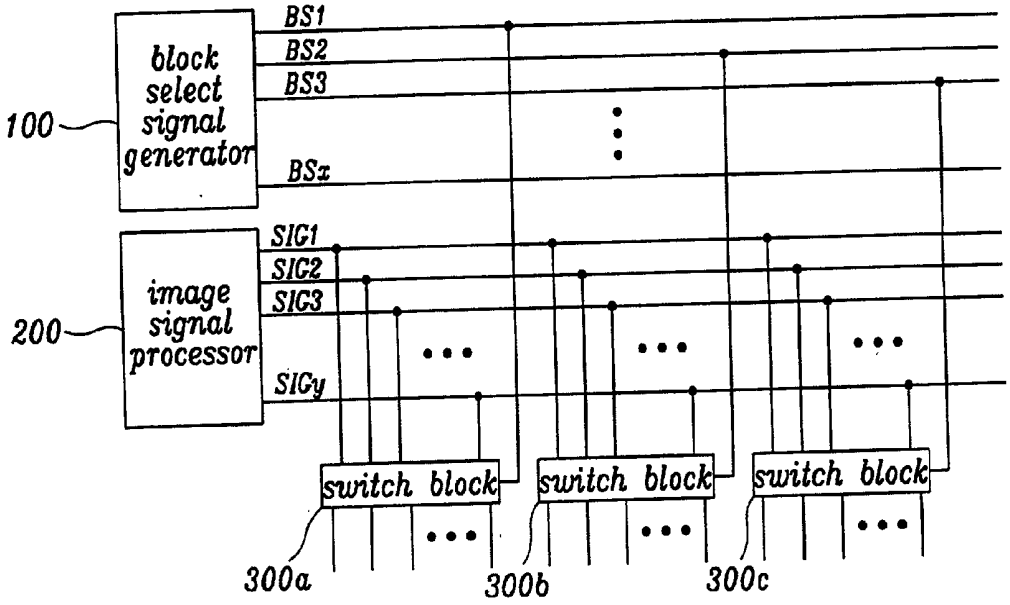

block select signal generator
100
BS1
BS2
BS3
BSx
image signal processor
200
SIC1
SIC2
SIC3
SICy
switch block
switch block
switch block
300a
300b
300c

FIG.4

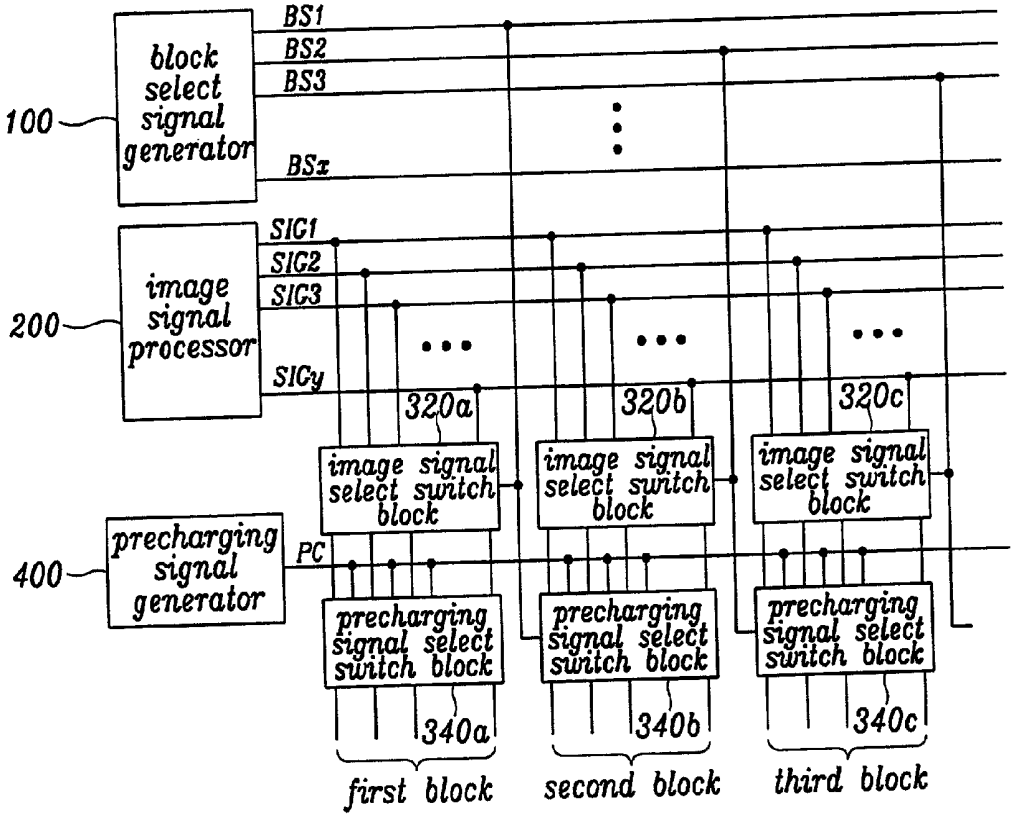

block select signal generator
100
BS1
BS2
BS3
BSx
image signal processor
200
SIC1
SIC2
SIC3
SICy
320a
320b
320c
image signal select switch block
image signal select switch block
image signal select switch block
precharging signal generator
400
PC
precharging signal select switch block
precharging signal select switch block
precharging signal select switch block
340a
340b
340c
first block
second block
third block

FIG.5

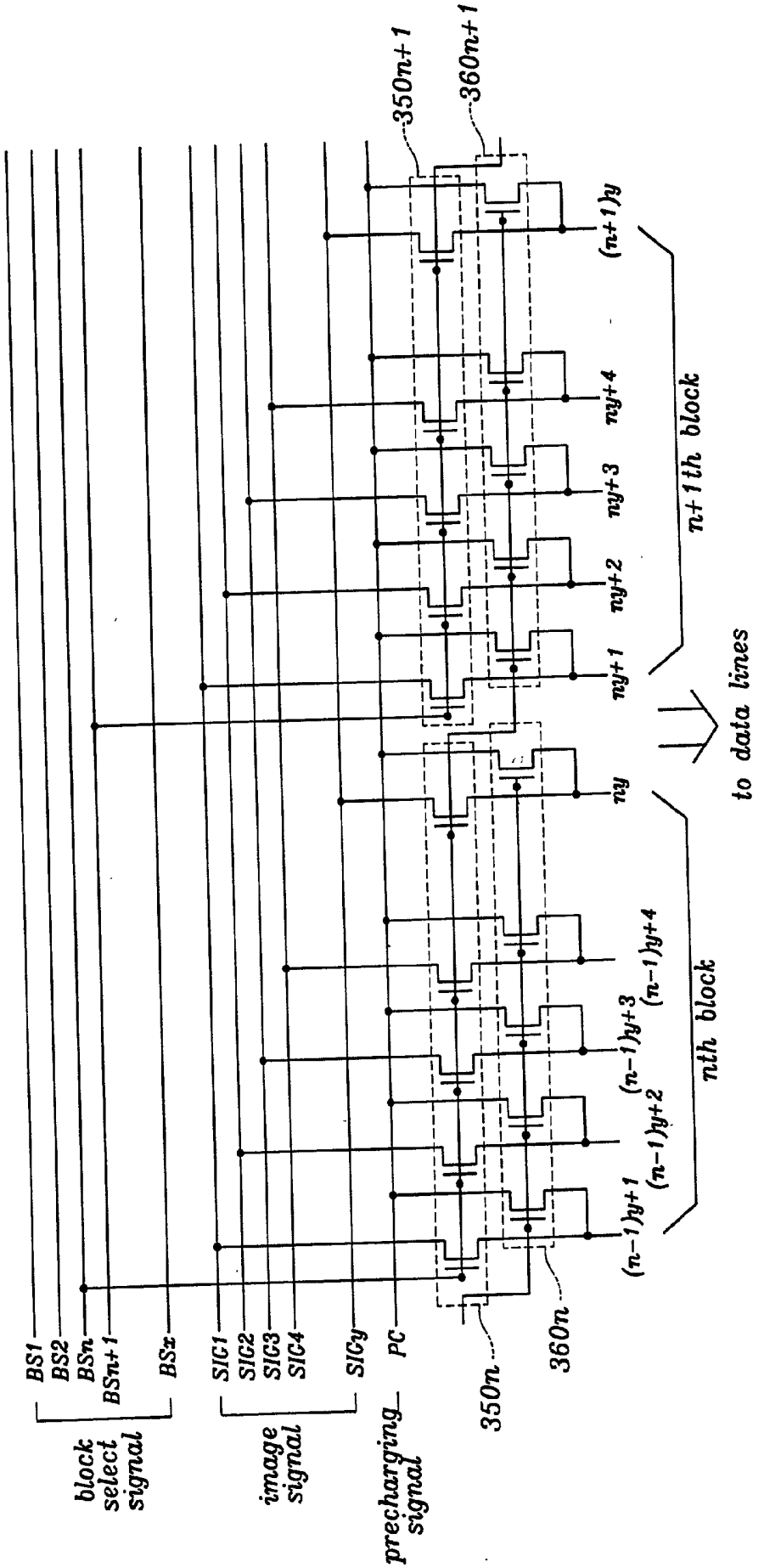

BS1
BS2
BSn
BSn+1
BSx
block select signal
SIG1
SIG2
SIG3
SIG4
SIGy
image signal
PC
precharging signal
350n
360n
350n+1
360n+1
(n-1)y+1
(n-1)y+2
(n-1)y+3
(n-1)y+4
ny
ny+1
ny+2
ny+3
ny+4
(n+1)y
nth block
n+1th block
to data lines

FIG.6a

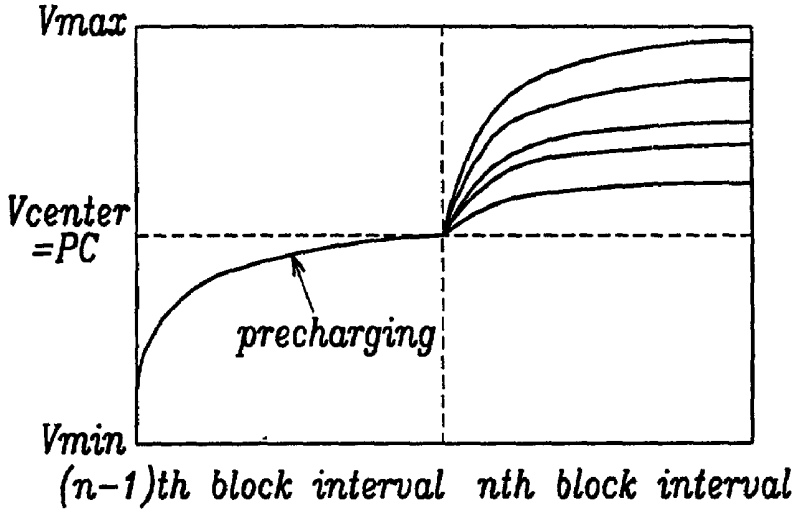

Vmax
Vcenter
=PC
precharging
Vmin
(n-1)th block interval
nth block interval

FIG.6b

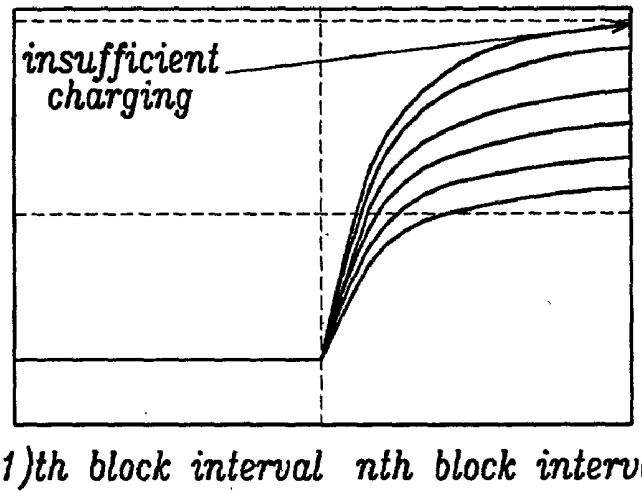

insufficient
charging
(n-1)th block interval
nth block interval

FIG.6c

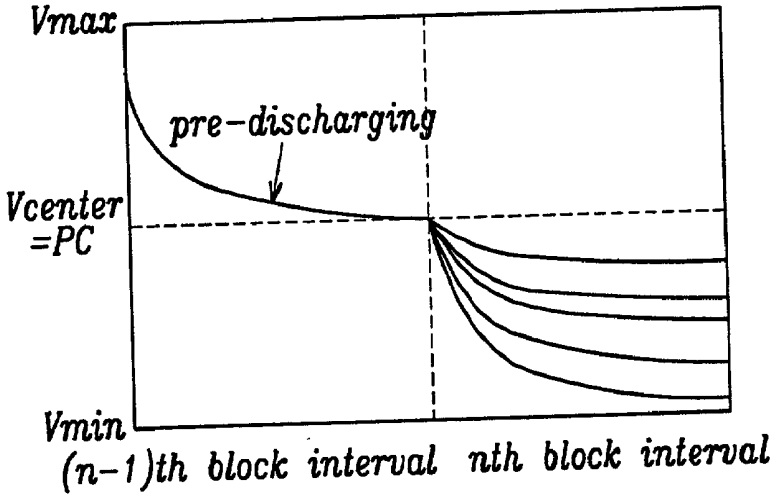

Vmax
pre-discharging
Vcenter
=PC
Vmin
(n-1)th block interval
nth block interval

FIG.6d

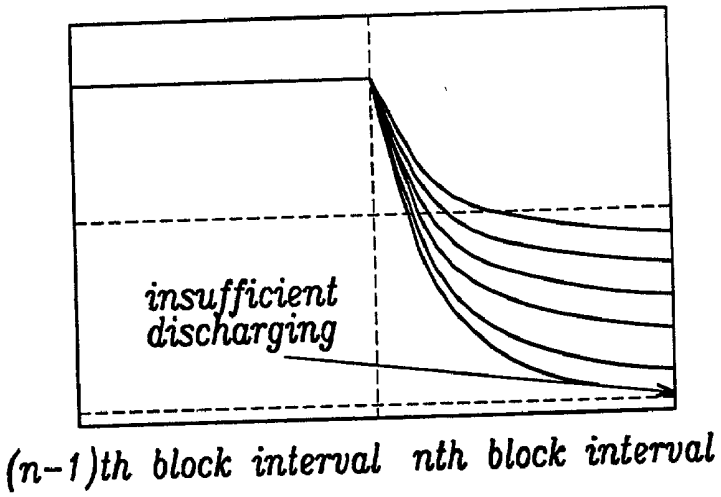

insufficient
discharging
(n-1)th block interval
nth block interval

FIG. 7

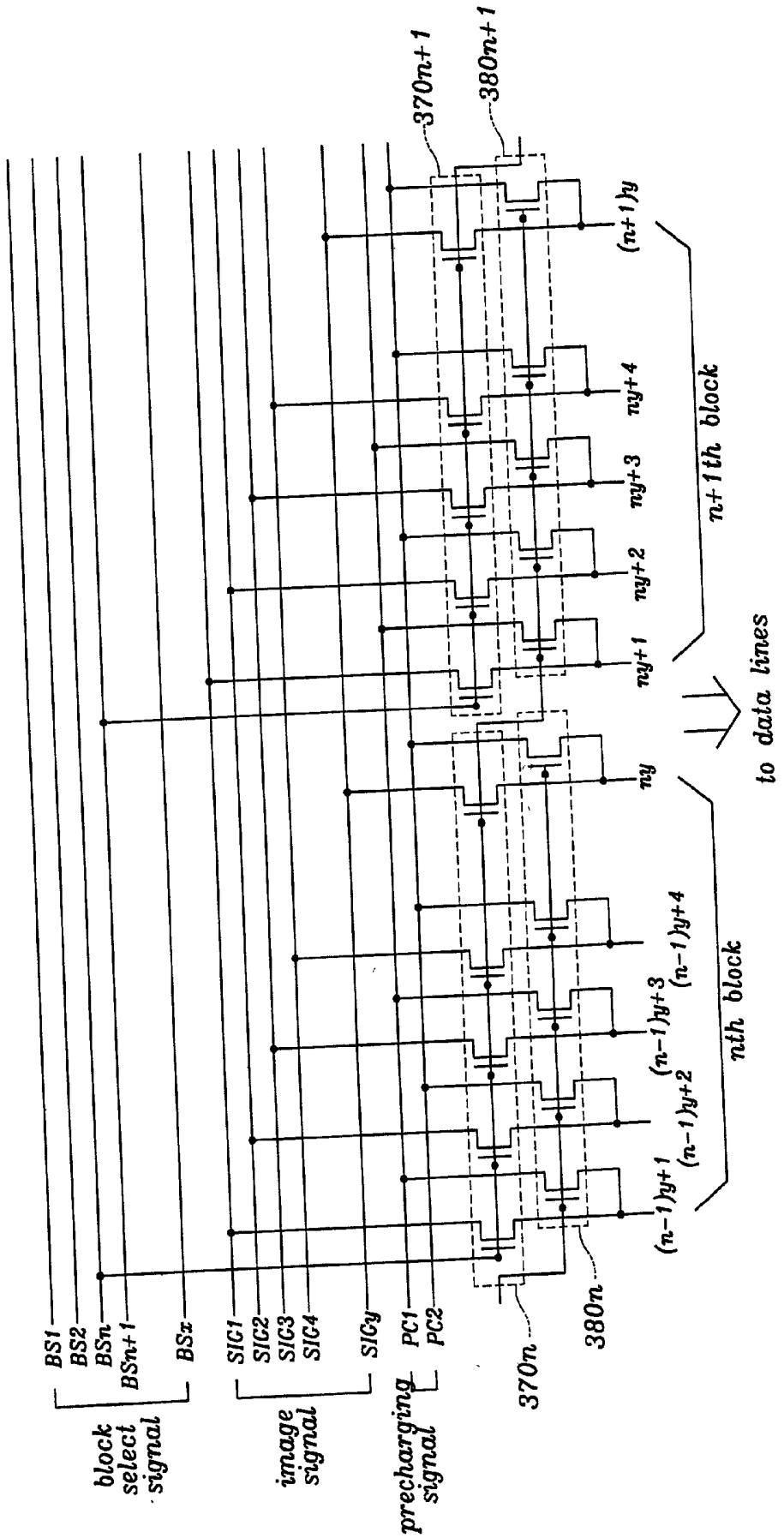

BS1
BS2
BSn
BSn+1
BSx
block select signal
SIG1
SIG2
SIG3
SIG4
image signal
SIGy
PC1
PC2
precharging signal
370n
380n
370n+1
380n+1
(n-1)y+1
(n-1)y+2
(n-1)y+3
(n-1)y+4
ny
ny+1
ny+2
ny+3
ny+4
(n+1)y
nth block
n+1th block
to data lines

FIG.8a

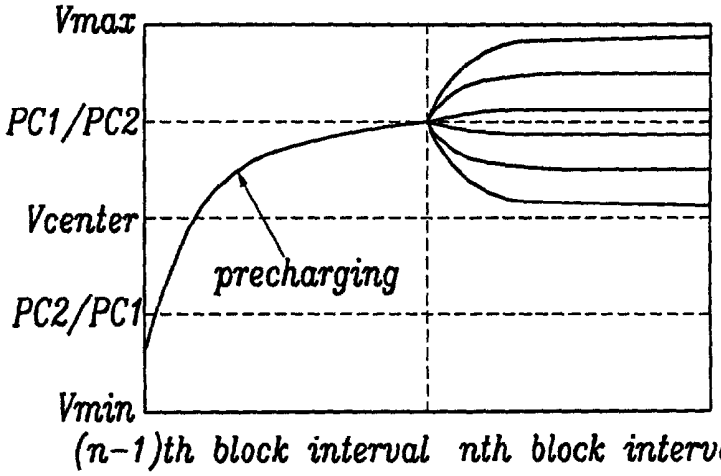


FIG.8b

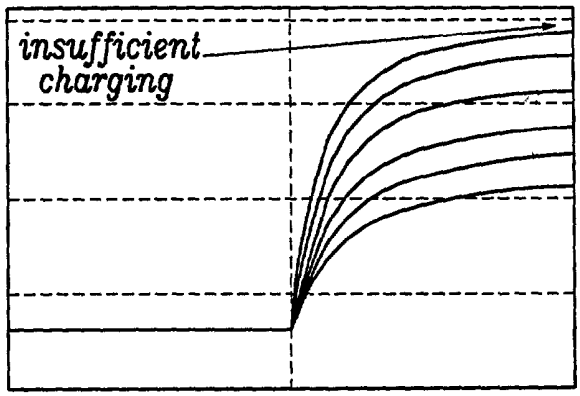
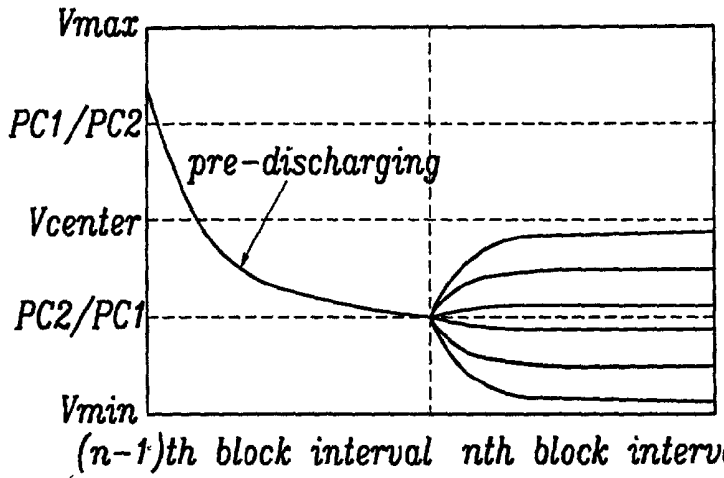
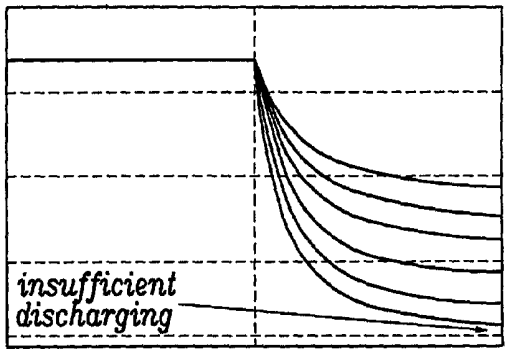


FIG.8c



8d


insufficient
discharging
(n-1)th block interval
nth block interval

8e

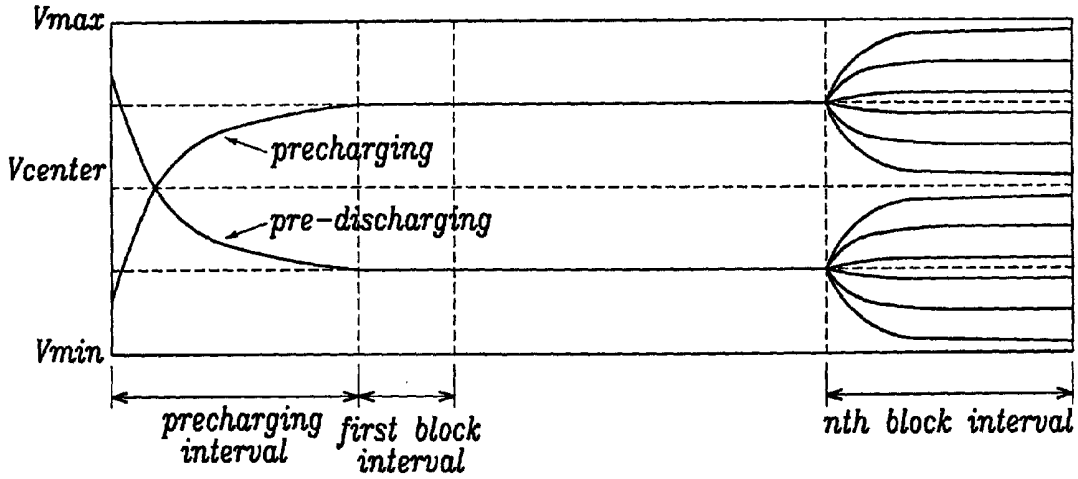

Vmax
Vcenter
Vmin
precharging
pre-discharging
precharging interval
first block interval
nth block interval

FIG.9

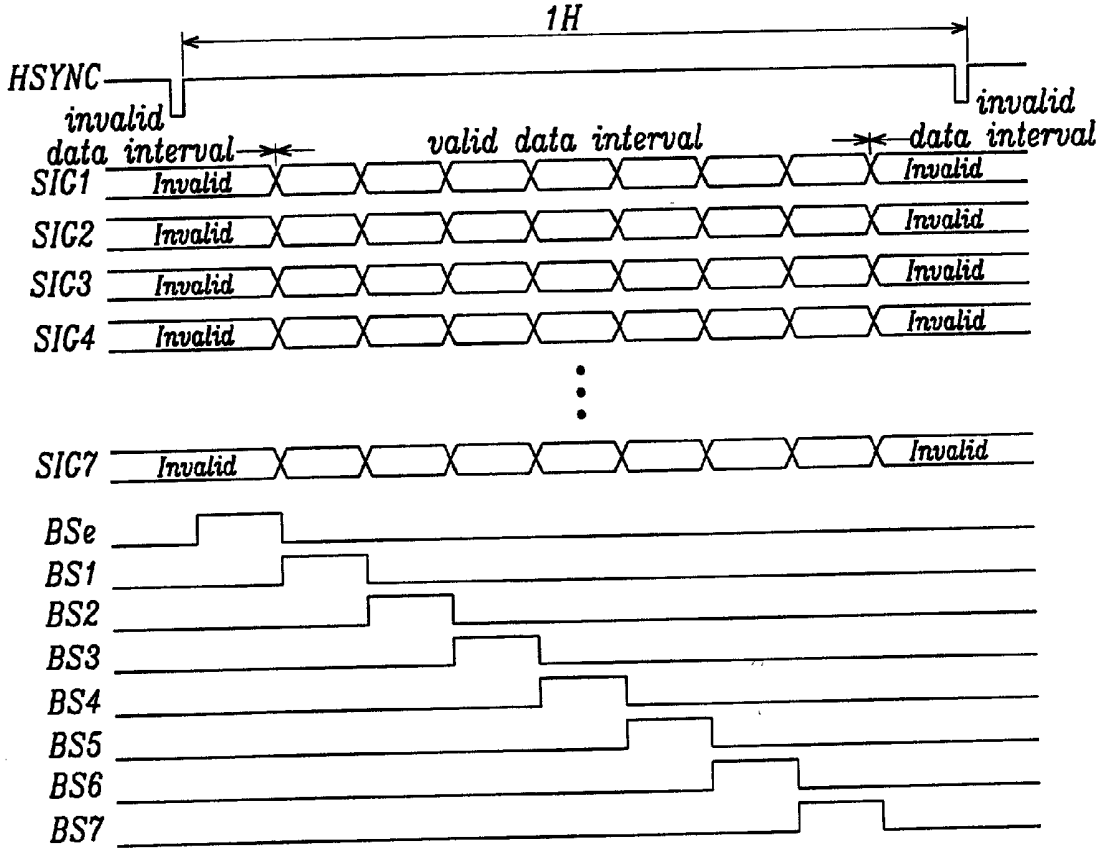

1H
HSYNC
invalid data interval
valid data interval
invalid data interval
SIC1
SIC2
SIC3
SIC4
SIC7
Invalid
BSe
BS1
BS2
BS3
BS4
BS5
BS6
BS7

FIG.10

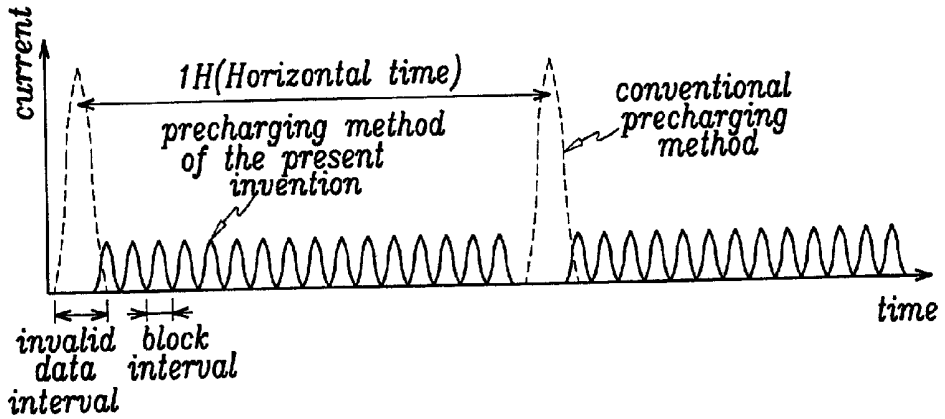
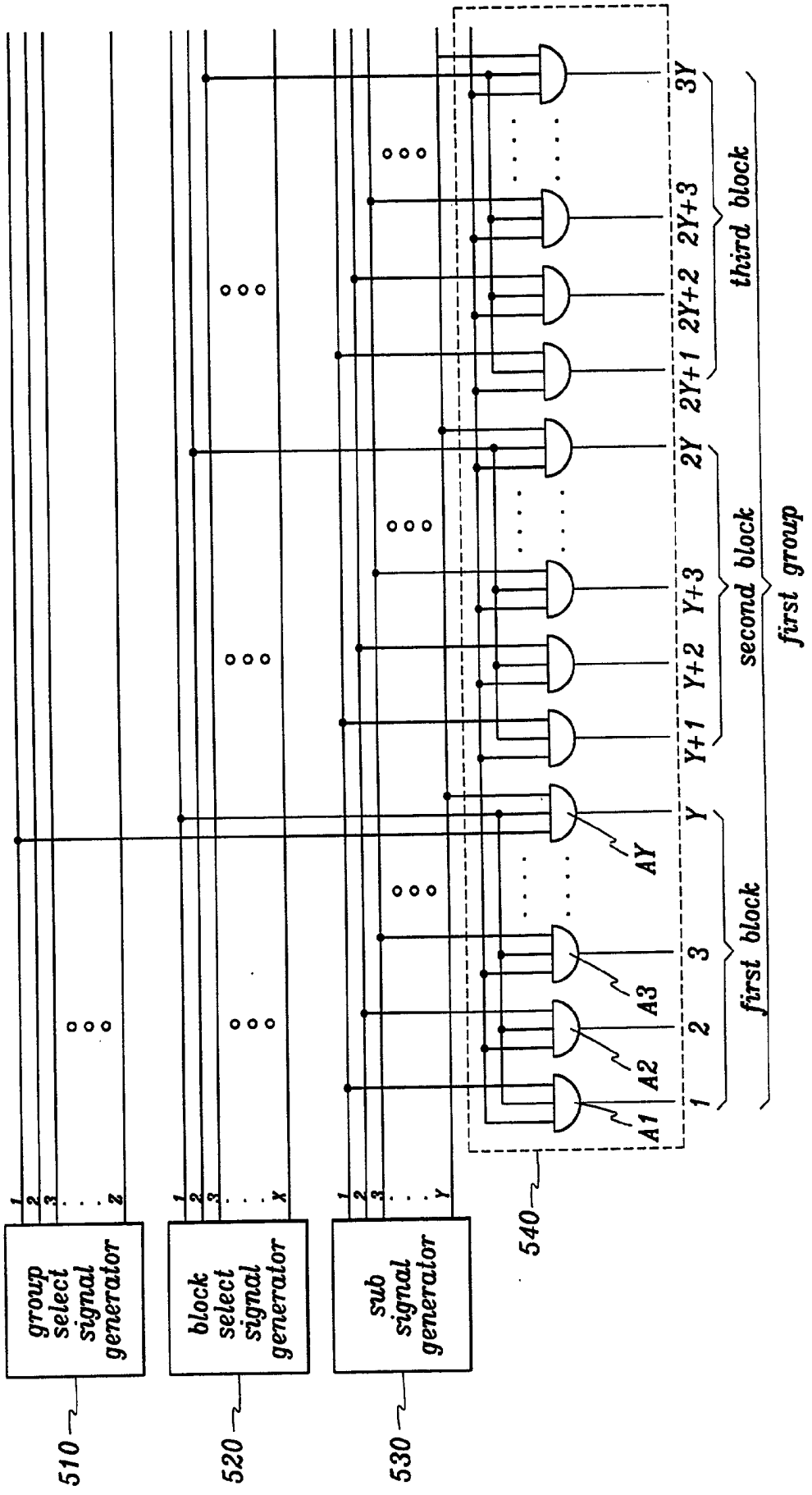

current
1H(Horizontal time)
precharging method of the present invention
conventional precharging method
time
invalid data interval
block interval

FIG. 11


group select signal generator
block select signal generator
sub signal generator
510
520
530
540
1
2
3
Z
X
Y
A1
A2
A3
AY
Y
Y+1
Y+2
Y+3
2Y
2Y+1
2Y+2
2Y+3
3Y
first block
second block
third block
first group

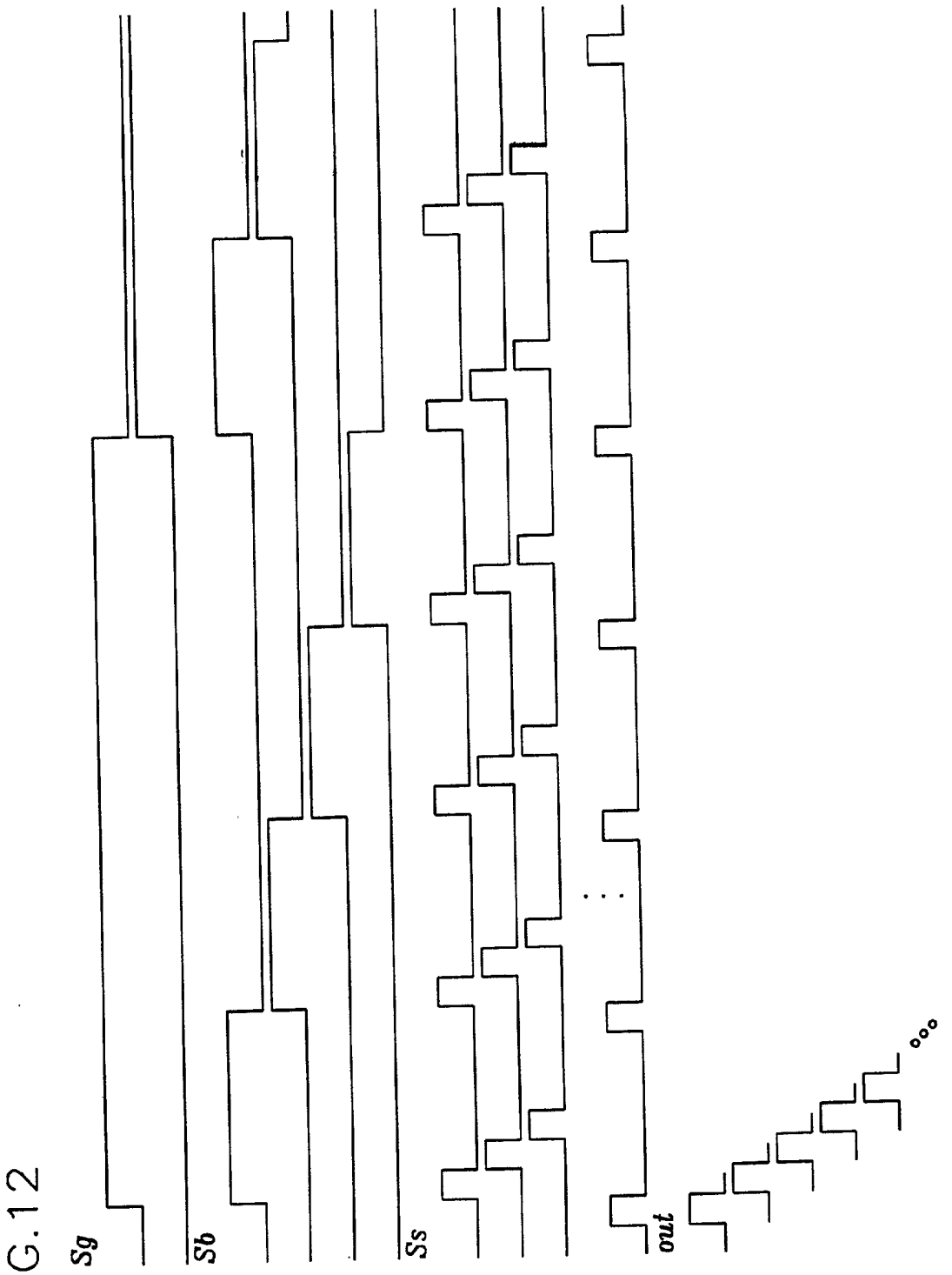
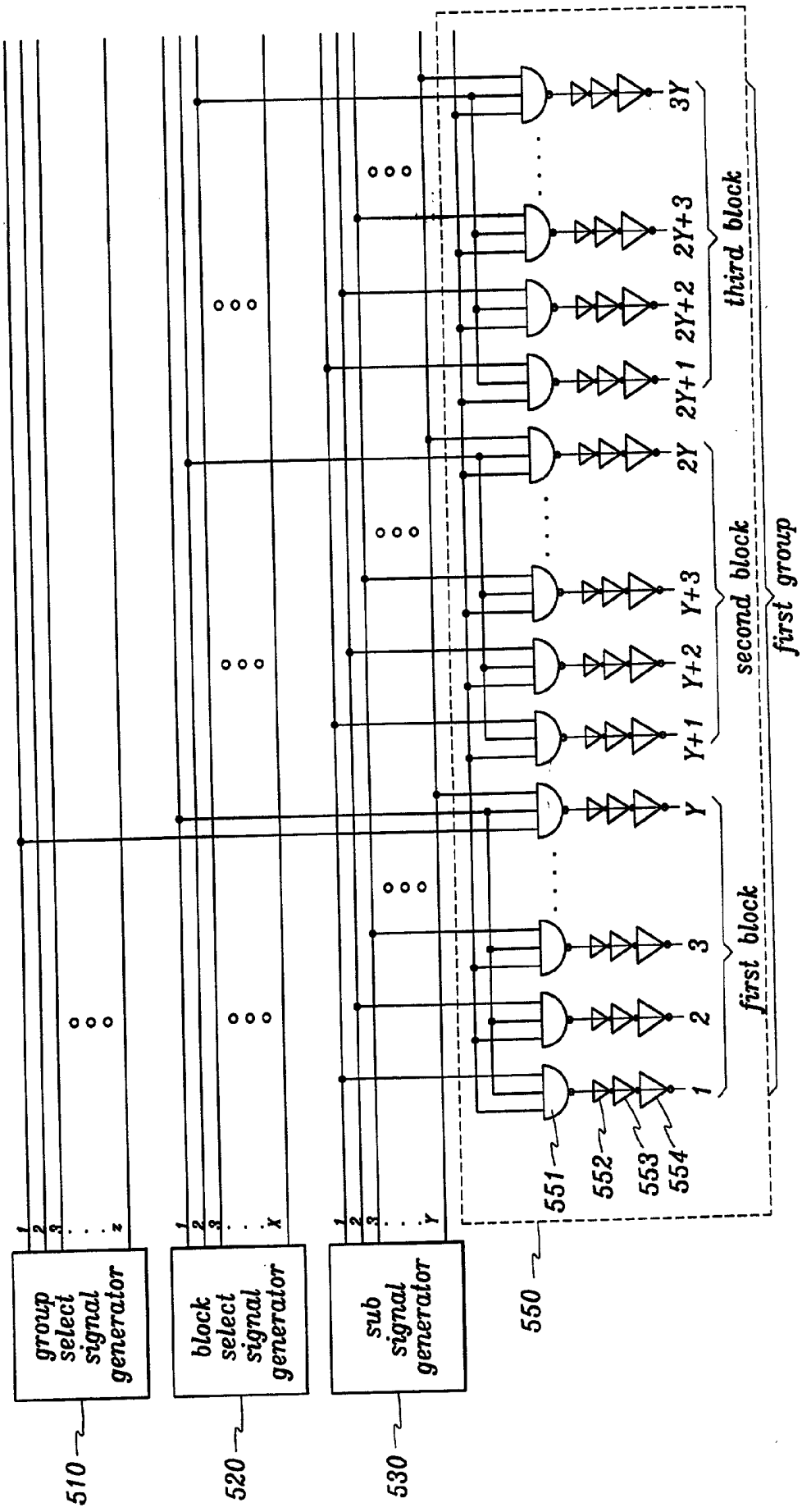


FIG. 12

FIG. 13


group select signal generator
block select signal generator
sub signal generator
510
520
530
550
551
552
553
554
first block
second block
third block
first group
1
2
3
Y
Y+1
Y+2
Y+3
2Y
2Y+1
2Y+2
2Y+3
3Y

DRIVING DEVICE AND A DRIVING METHOD FOR A DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to a display device, and an apparatus and method for driving the display device. More particularly, the present invention relates to a thin film transistor liquid crystal display (TFT-LCD), and an apparatus and method for driving the TFT-LCD.

[0003] (b) Description of the Related Art

[0004] TFT-LCDs apply an electric field to liquid crystal material having anisotropic dielectricity and injected between two substrates to form a liquid crystal layer. The two substrates are arranged substantially in parallel having a predetermined gap therebetween, and the amount of light permeating the substrates is controlled by the intensity of the electric field applied to the liquid crystal material. Because of the many advantages of the TFT-LCD—low power consumption, thin profile and low weight, high resolution and others—the CRT, which is presently the most widely used display configuration, is being replaced by this flat panel display technology in many areas.

[0005] **FIG. 1** shows a schematic view of a general TFT-LCD. The TFT-LCD includes an LCD panel **10**, a gate driver **20**, a data driver **30**, and a timing generator **40**. A plurality of gate lines G are formed on the LCD panel **10**, and a plurality of data lines D are formed insulated from and crossing the gate lines G.A TFT **12** is formed in each pixel defined by the crossing of gate lines G and the data lines D. A gate electrode, source electrode, and drain electrode of each TFT **12** are connected respectively to one of the gate lines G, one of the data lines D, and a pixel electrode (not shown). Liquid crystal material is injected between a substrate (TFT substrate) on which the above elements are formed and a substrate (common electrode substrate) on which are formed common electrodes. The two substrates and the liquid crystal material injected between the two substrates act as a capacitor Cl.

[0006] The gate driver **20** applies a gate ON/OFF voltage to the gate lines G to turn the TFTs ON or OFF. The gate ON voltage is applied sequentially to one of the gate lines G such that the TFTs connected to the gate lines G are turned ON in sequence. Further, the data driver **30** applies a gray voltage to the data lines D. Finally, the timing generator **40** receives from a graphic controller (not shown) a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a clock signal CLK, and a data signal DATA, and outputs a variety of timing control signals to the gate driver **20** and the data driver **30**.

[0007] The operation of the TFT-LCD structured as in the above will be described hereinafter.

[0008] The gate ON voltage is applied to the gate electrodes via the gate lines G such that the TFTs **12** are turned ON, after which the gray voltages, representing image signals, are applied to the source electrodes through the data lines D and then transmitted to the drain electrodes. As a result, the gray voltages are transmitted to the pixel electrodes, and electric fields are formed by a potential difference between the pixel electrodes and the common electrodes. An intensity of the electric field is controlled by the magnitude of the gray voltage, and the amount of light permeating the substrates is determined by this level of the electric field intensity.

[0009] As the size of the conventional TFT-LCD increases, the increased parasitic capacitance of the data lines prevents the gray voltages from sufficiently charged to the data lines. As a result, an inadequate gray voltage is transmitted to each of the pixels. To improve charge characteristics of the data lines, a method of precharging each data line to a predetermined voltage level is used in a conventional TFT-LCD.

[0010] In the conventional TFT-LCD, image data corresponding to an (n)th horizontal line (pixel line) are sampled and the sampled data are written on each of the data lines. When writing of the sampled (n)th data, image data corresponding to an (n+1)th horizontal line are sampled. Data lines are precharged in an interval between data writing times (data enable intervals) of the (n)th horizontal line and the (n+1)th horizontal line.

[0011] U.S. Pat. Nos. 5,426,447 and 5,510,807 disclose the above data line precharging methods. In these inventions, the data lines are precharged in an interval (i.e. invalid data interval) between the data enable interval of the (n)th horizontal line and the data enable interval of the (n+1)th horizontal line as described above. Also, a block addressing method is used in these inventions. In block addressing, a single pixel line is divided into blocks, each having many data lines, and each block is sequentially selected. For example, in a display device having 640 data lines, after the data lines are divided into 10 blocks each having 64 data lines, each block is selected within a single horizontal interval such that image data are written to the data lines within the selected block.

[0012] **FIG. 2** shows a diagram used to describe the conventional precharging method in which precharging is performed in the interval (i.e., the invalid data interval) between the data enable intervals of the (n)th horizontal line and the (n+1)th horizontal line. A valid data interval shown in **FIG. 2** refers to the interval during which sampled image data is written on one horizontal line. In the conventional precharging method, precharging is performed only between valid data intervals (data enable intervals). That is, precharging is performed during invalid data intervals P1 and P2. Accordingly, if the invalid data intervals P1 and P2 are not long enough, various problems may result.

[0013] Namely, in the conventional precharging method, since all the data lines must be precharged to a desired voltage level within the relatively short precharging interval, an extremely large amount of current is necessary for precharging, giving much stress to a current driving capability of the system. For example, in a color XGA display having 1024×3 (R,G,B) data lines, if a parasitic capacitance of each data line is 80pF, a large capacitance of 1024×3×80 pF=245.7 nF must be charged within a maximum allowable time of approximately 4.6μ sec to one horizontal line. Further, in the conventional precharging method, since precharging is performed in the intervals (invalid data intervals) between adjacent data enable intervals, if adjacent data intervals overlap without invalid data intervals, data lines can not be precharged.

[0014] On the other hand, a method is used in larger TFT-LCDs in which after gate blocks are selected, gate ON

signals are applied to each gate line within the selected block. Such a TFT-LCD structure is disclosed in U.S. Pat. Nos. 5,028,916, 4,714,921, and 5,426,447. However, these inventions require many bus lines in a gate driver structure, increasing a circuit area of the gate drivers and resulting in line open defects during the manufacture of the gate driver.

SUMMARY OF THE INVENTION

[0015] The present invention has been made in an effort to solve the above problems.

[0016] It is an object of the present invention to provide a display device, and an apparatus and a method for driving the display device that reduce a current level needed for precharging, allowing a high degree of margin for a precharging signal generator design, and making it possible to be applied to systems having a limited valid data interval.

[0017] It is another object of the present invention to provide a display device, and an apparatus and a method for driving the display device that reduce the number of required bus lines and a circuit area of a gate driver, thereby preventing line defects.

[0018] To achieve the above objects, the present invention provides a display device (e.g., a liquid crystal display), and an apparatus and a method for driving the display device. The LCD includes an LCD panel comprising a plurality of gate lines, a plurality of data lines insulated from and intersecting the gate lines, and a plurality of TFTs each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines; a gate driver for sequentially supplying gate drive signals to the gate lines to turn the TFTs ON; and a data driver that divides the data lines into an X-number of blocks, each block having a predetermined number of data lines, and that applies image signals to the data lines in an (n)th block and applies precharging voltages to the data lines in an (n+j)th block.

[0019] According to a feature of the present invention, the data driver includes a block select signal generator for generating block select signals to select one of the blocks; an image signal processor that generates the image signals for applying to the data lines in a selected block; a precharging signal generator that generates the precharging voltages for applying to the data lines in the selected block; an X-number of image signal select switch blocks for switching each of the image signals for application to one of the blocks; and an X-number of precharging select switch blocks for switching each of the precharging voltages for application to one of the blocks, wherein an (n)th block select signal simultaneously turns ON an (n)th image signal select switch block and an (n+j)th precharging signal select switch block.

[0020] According to another feature of the present invention, the precharging voltages are at a single voltage level.

[0021] According to yet another feature of the present invention, the precharging voltages have a center value between a maximum and a minimum value of the image signals.

[0022] According to still yet another feature of the present invention, an (n)th image signal select switch block among the X-number of select switch blocks comprises at least a Y-number of first MOS transistors having sources to which the image signals are applied, drains connected to the data lines, and gates to which the (n)th block select signal is applied; and wherein an (n)th precharging signal select switch block among the X-number of select switch blocks comprises at least a Y-number of second MOS transistors having sources to which the precharging voltages are applied, drains connected to the data lines, and gates to which an (n−j)th block select signal is applied.

[0023] According to still yet another feature of the present invention, the first and second MOS transistors are TFTs fabricated on a substrate of the LCD.

[0024] According to still yet another feature of the present invention, the TFTs are made of poly-crystal silicon or single-crystal silicon.

[0025] According to still yet another feature of the present invention, the precharging voltages each include a first precharging signal and a second precharging signal having a first voltage level and a second voltage level, respectively.

[0026] According to still yet another feature of the present invention, the first precharging signal has a predetermined value between a maximum and a center value of the image signals, and the second precharging signal has a predetermined value between a minimum value and a center value of the image signals.

[0027] According to still yet another feature of the present invention, an (n)th image signal select switch block among the X-number of select switch blocks comprises at least a Y-number of first MOS transistors having sources to which the image signals are applied, drains connected to the data lines, and gates to which the (n)th block select signal is applied; and wherein an (n)th precharging signal select switch block among the X-number of select switch blocks comprises at least a Y-number of second MOS transistors having sources to which the precharging voltages are applied, drains connected to the Y-number of data lines, and gates to which an (n−j)th block select signal is applied.

[0028] According to still yet another feature of the present invention, the first precharging signal is applied to the sources of the second MOS transistors connected to odd data lines, and the second precharging signal is applied to the sources of the second MOS transistors connected to even data lines.

[0029] The drive apparatus includes the gate driver and the data driver.

[0030] In another aspect, the drive apparatus is applied to a display device including a plurality of scanning lines and a plurality of data lines insulated from and intersecting the scanning lines, wherein the drive apparatus includes a scanning driver for sequentially supplying scanning signals to the scanning lines; and a data driver for dividing the data lines into an X-number of blocks, each block having a predetermined number of data lines, and applying image signals to the data lines in an (n)th block, and applying precharging voltages to the data lines in an (n+j)th block.

[0031] The method for driving an LCD includes the steps of sequentially supplying gate drive signals to the gate lines to turn the TFTs ON; and dividing the data lines into an X-number of blocks, each block having a predetermined number of data lines, and applying image signals to the data

lines in an (n)th block, and applying precharging voltages to the data lines in an (n+j)th block.

[0032] According to a feature of the method, j has a value of 1.

[0033] According to another feature of the method, if the image signals are applied to data lines in a last block of an (i)th pixel row, the precharging voltages are, at the same time, applied to data lines in a first block of an (i+1)th pixel row.

[0034] According to yet another feature of the method, a first block of an (i)th pixel row uses a separate first block precharging signal received externally.

[0035] In another aspect, the LCD includes an LCD panel including an R-number of gate lines, a plurality of data lines insulated from and intersecting the gate lines, and a plurality of TFTs each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines; a data driver for applying image signals to the data lines; and a gate driver for sequentially supplying gate drive signals to the gate lines to turn the TFTs ON, wherein the R-number of gate lines are divided into an X-number of blocks having a minimum Y-number of gate lines, and the X-number of blocks are divided into a minimum Z-number of groups connected to the gate driver.

[0036] The gate driver includes a group select signal generator for generating group select signals to select one of the Z-number of groups; a block select signal generator for generating block select signals to select one of the X-number of blocks; a sub-signal generator for generating sub-signals to select one of the Y-number of gate lines; and a gate array for receiving the group select signals, the block select signals, and the sub-signals, and outputting the gate drive signals.

[0037] According to another feature of the aspect, a gate array performs an AND operation of the group select signals, the block select signals, and the sub-signals.

[0038] According to yet another feature of the aspect, the gate array comprises a plurality of AND gates including input terminals connected to each of the group select signals, the block select signals, and the sub-signals, and output terminals each connected to one of the gate lines.

[0039] According to still yet another feature of the aspect, the gate array includes a plurality of NAND gates into which the group select signals, the block select signals, and the sub-signals are input; and a plurality of inverters for inverting output signals of the NAND gates and outputting the inverted signals to the gate lines.

[0040] According to still yet another feature of the aspect, the inverters include a first, second and third inverter connected to the NAND gates, of which a so current drive capacity increases from the first to the third inverter.

[0041] In another aspect, the drive apparatus is applied to a display device including an R-number of scanning lines transmitting scanning signals, and a plurality of data lines transmitting image signals, the drive apparatus including a data driver for applying image signals to data lines; and a scanning driver for sequentially supplying the scanning signals to the scanning lines such that the image signals applied to the data lines are displayed, wherein the R-number of scanning lines are divided into a plurality of blocks having a maximum Y-number of the scanning lines, and the blocks are divided into a Z-number of groups having a maximum X-number of blocks.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention:

[0043] **FIG. 1** is a schematic view of the conventional TFT-LCD;

[0044] **FIG. 2** shows a diagram used to describe a conventional precharging method in which precharging is performed in an interval between data enable intervals of an (n)th horizontal line and an (n+1)th horizontal line;

[0045] **FIG. 3** is a schematic view of a data driver used for block addressing;

[0046] **FIG. 4** is a schematic view of a data driver according to a preferred embodiment of the present invention;

[0047] **FIG. 5** is a detail view of image signal select switch blocks and precharging signal select switch blocks according to a first preferred embodiment of the present invention;

[0048] **FIGS. 6*a*-6*d*** are graphs used to describe effects of precharging according to the first preferred embodiment of the present invention;

[0049] **FIG. 7** is a detail view of image signal select switch blocks and precharging signal select switch blocks according to a second preferred embodiment of the present invention;

[0050] **FIGS. 8*a*-8*e*** are graphs used to describe effects of precharging according to the second preferred embodiment of the present invention;

[0051] **FIG. 9** is a timing chart of a method of separately applying external precharging signals of a first block according to a preferred embodiment of the present invention;

[0052] **FIG. 10** is a graph comparing current variations in a conventional precharging method and a precharging method of the present invention;

[0053] **FIG. 11** is a schematic view of a gate driver according to a preferred embodiment of the present invention;

[0054] **FIG. 12** is a waveform chart of signals of the gate driver shown in **FIG. 11**; and

[0055] **FIG. 13** is a schematic view of a gate driver according to a modified example of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0056] Preferred embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

[0057] **FIG. 3** shows a schematic view of a data driver used for block addressing. The data driver includes a block select signal generator **100**, an image signal processor **200**,

and switch blocks **300**. All data lines are divided into an x-number of blocks, and each block has a y-number of data lines.

[**0058**] The block select signal generator **100** outputs block select signals BS for selecting one of the blocks. Here, the block select signal BS**1** corresponds to a first block and is applied to the switch block **300***a,* the block select signal BS**2** corresponds to a second block and is applied to the switch block **300***b,* and the block select signal BS**3** corresponds to a third block and is applied to the switch block **300***c.* This pattern is repeated for all the block select signals BS and the x-number of switch blocks **300**. The switch block **300** receiving the block select signal BS of a high (or low) state is applied is turned ON. At this time, the block select signal generator **100** sequentially selects an x-number of blocks.

[**0059**] The image signal processor **200** writes image data SIG to the selected block. That is, the image data SIG output from the image signal processor **200** are written on data lines of the LCD panel through the switch blocks **300** that are turned ON by the block select signal generator **100**.

[**0060**] In the block addressing method, if R is a total number of the data lines, the number of the blocks X and the number of the data lines in each block Y must satisfy the following equation.

$$X*Y \geqq R \qquad \text{[Equation 1]}$$

[**0061**] For example, in an XGA display panel having 1024×3 (3072) data lines, a possible design may comprise 16 blocks each having 192 data lines. In this case, X*Y is exactly 3072, with no leftover data lines. Further, with the number of the data lines in each block Y set at 220 and the number of blocks X set at 14, Equation 1 can again be satisfied, but either the first or the last block must have fewer than 220 data lines.

[**0062**] A data driver according to a preferred embodiment of the present invention will be described hereinafter with reference to **FIG. 4**. The data driver includes a block select signal generator **100**, an image signal processor **200**, a precharging signal generator **400**, image signal select switch blocks **320**, and precharging signal select switch blocks **340**.

[**0063**] The block select signal generator **100** outputs block select signals BS to the image signal select switch blocks **320** and the precharging select switch blocks **340**. At this time, an (n)th block select signal BS is input to an (n)th image signal select switch block **320** and an (n+1)th precharging select switch block **340**. So, for example, the block select signal BS**1** is output to the image signal select switch block **320***a* and the precharging select switch block **340***b.*

[**0064**] The image signal processor **200** applies image signals SIG to the selected image signal select switch blocks **320** . That is, the image signals SIG output from the image signal processor **200** passes through the image signal select switch blocks **320**, which are turned ON by the block select signals BS of the block select signal generator **100**, to be applied to data lines of a LCD panel.

[**0065**] The precharging signal generator **400** applies precharging signals PC, having a predetermined voltage level, to the precharging signal select switch blocks **340**. The precharging signals PC pass through the precharging signal select switch blocks **340**, turned ON by the block select signals BS of the block select signal generator **100**, to be applied to the data lines of the LCD panel.

[**0066**] In the above described data driver, if a signal to select an (n)th block is applied, the signal is transmitted to an (n)th image signal select switch block **320** to which a Y-number of image signal lines are connected and also to an (n+1)th precharging signal select switch block **340** to which precharging lines are connected to turn these switch blocks **320** and **340** ON. As a result, the image signals SIG are transmitted to the data lines of the LCD panel connected to the (n)th image signal select switch block **320**, and the precharging signals PC are transmitted to the data lines of the LCD panel connected to the (n+1)th precharging signal select switch block **340** to precharge (or pre-discharge) these data lines connected to the (n+1)th precharging signal select switch block **340** to a predetermined voltage level. At this time, the predetermined voltage level to which the data lines are precharged (or pre-discharged) can be a level corresponding to a median value between the maximum image data and the minimum image data, or to two or more values closest to the image data to be written on the data lines.

[**0067**] As described above, in the data driver of the present invention, if the image signals SIG are transmitted to the data lines of the LCD panel connected to the (n)th image signal select switch block **320**, the data lines connected to the (n+1)th precharging signal select switch block **340** are precharged to a predetermined voltage level.

[**0068**] **FIG. 5** shows a detail view of an (n)th image signal select switch block **350***n* and an (n+1)th image signal select switch block **350**n+1, and an (n)th precharging signal select switch block **360***n* and an (n+1)th precharging signal select switch block **360***n*+1 according to a first preferred embodiment of the present invention. The image signal select switch blocks **350***n* and **350***n*+1, and the precharging signal select switch blocks **360***n* and **360**n+**1** are comprised of a plurality of MOS transistors.

[**0069**] With regard to the MOS transistors of the (n)th image signal select switch block **350***n,* sources of the MOS transistors are respectively connected to each of the image signals SIG**1**, SIG**2**, . . . , SIGy; gates of the MOS transistors are collectively connected to an (n)th block select signal BSn; and drains of the MOS transistors are respectively connected to each of the data lines of the LCD panel. Regarding the MOS transistors of the (n+1)th precharging signal select switch block **360***n*+1, sources of the MOS transistors are collectively connected to the precharging signal PC; gates of the MOS transistors are collectively connected to the (n)th block select signal BSn; and drains of the MOS transistors are respectively connected to each of the data lines of the LCD panel.

[**0070**] If the (n)th block select signal BSn becomes high, the transistors of both the (n)th image signal select switch block **350***n* and the (n+1)th precharging signal select switch block **360***n*+1 are turned ON. Accordingly, the image signals SIG**1**, SIG**2**, . . . , SIGY are transmitted to the data lines connected to the drains of the transistors of the (n)th image signal select switch block **350***n,* and the precharging signal PC is transmitted to the data lines connected to the drains of the transistors of the (n+1)th precharging signal select switch block **360***n*+1.

[0071] Effects of precharging (or pre-discharging) according to the first preferred embodiment of the present invention will be described hereinafter with reference to **FIGS. 6***a*-**6***d*.

[0072] **FIGS. 6***a* and **6***c* show the amount of change in the image signals SIG applied to the data lines during an (n)th block interval when the precharging/pre-discharging is performed at a center value Vcenter of a maximum value Vmax and a minimum value Vmin of the image signals SIG in an (n−1)th block interval. **FIGS. 6***b* and **6***d* show the amount of change in the image signals SIG applied to the data lines during an (n)th block interval when the precharging/pre-discharging is not performed during an (n−1)th block interval. As is shown by these drawings, the level of the resultant image signals SIG can be more fully realized to a desired level when precharging/pre-discharging than without precharging/pre-discharging.

[0073] **FIG. 7** shows a detail view of an (n)th image signal select switch block **370***n* and an (n+1)th image signal select switch block **370***n*+1, and an (n)th precharging signal select switch block **380***n* and an (n+1)th precharging signal select switch block **380***n*+1 according to a second preferred embodiment of the present invention. The image signal select switch blocks **370***n* and **370***n*+1, and the precharging signal select switch blocks **380***n* and **380***n*+1 are comprised of a plurality of MOS transistors.

[0074] With regard to the MOS transistors of the (n)th image signal select switch block **370***n*, sources of the MOS transistors are respectively connected to each of the image signals SIG**1**, SIG**2**, . . . , SIGy; gates of the MOS transistors are collectively connected to an (n)th block select signal BSn; and drains of the MOS transistors are respectively connected to each of the data lines of the LCD panel. Regarding the MOS transistors of the (n+1)th precharging signal select switch block **380***n*+1, sources of odd-number MOS transistors are collectively connected to a first precharging signal PC**1** while sources of even-number MOS transistors are collectively connected to a second precharging signal PC**2**. Further, gates of the MOS transistors of the (n+1)th precharging signal select switch block **380***n*+1 are collectively connected to the (n)th block select signal BSn, and drains of the MOS transistors are respectively connected to each of the data lines of the LCD panel.

[0075] In the above, it is preferable that the first precharging signal PC**1** has a value between a maximum value Vmax and a center value Vcenter of the image signals SIG (hereinafter referred to as a "positive value"), and the second precharging signal PC**2** has a value between a minimum value Vmin and the center value Vcenter of the image signals SIG (hereinafter referred to as a "negative value"). The values of the first and second precharging signals PC**1** and PC**2** change from a positive to a negative value in units of frames.

[0076] If the (n)th block select signal BSn is controlled to a high state, the transistors of both the (n)th image signal select switch block **370***n* and the (n+1)th precharging signal select switch block **380***n*+1 are turned ON. Accordingly, the image signals SIG**1**, SIG**2**, . . . SIGY are transmitted to the data lines connected to the drains of the transistors of the (n)th image signal select switch block **370***n*, and the precharging signals PC**1** and PC**2** are transmitted to the data lines connected to the drains of the transistors of the (n+1)th precharging signal select switch block **380***n*+1.

[0077] Effects of precharging (or pre-discharging) according to the second preferred embodiment of the present invention will be described hereinafter with reference to **FIGS. 8***a*-**8***e*.

[0078] **FIGS. 8***a* and **8***c* show the amount of change in the image signals SIG applied to the data lines during an (n)th block interval when precharging/pre-discharging is performed to the first precharging signal PC**1** (or the second precharging signal PC**2**) in an (n−1)th block interval. **FIGS. 8***b* and **8***d* show the amount of change in the image signals SIG applied to the data lines during an (n)th block interval when precharging/pre-discharging is not performed during an (n−1)th block interval . Further, **FIG. 8***e* shows the amount of change in image signals applied to data lines in the case where precharging/pre-discharging is performed according to the methods disclosed in U.S. Pat. Nos. 5,426,447 and 5,510,807.

[0079] In **FIG. 8***e*, all the data lines of an LCD panel are precharged in an interval before a first block is selected, and a value of this precharging is maintained until an (n)th block is selected and the image signals are applied to the data lines. However, as described previously, if the interval for precharging is short, a large current must be supplied to the data lines to perform precharging to a desired level.

[0080] Accordingly, as is shown by these drawings, the level of the resultant image signals SIG can be more fully realized to a desired level when precharging/pre-discharging the data lines, than without precharging/pre-discharging.

[0081] In the first and second embodiments of the present invention, the first block of pixel lines may use a final block select signal of a previous pixel line to perform precharging/pre-discharging, or a separate first block precharging signal may be generated and used.

[0082] **FIG. 9** shows a timing chart of a method of separately applying external precharging signals for a first block according to a preferred embodiment of the present invention. A single interval **1** H of a horizontal synchronization signal HSYNC includes invalid data intervals and valid data intervals. Block signals BS**1**, BS**2**, BS**3**, . . . , BS**7** respectively select a first block, a second block, a third block, . . . , a seventh block, the blocks applying image signals SIG**1**, SIG**2**, SIG**3**, SIG**7**, respectively. The block signals BS, as described above, are applied also to a subsequent block for precharging (or pre-discharging). The block select signals BS**1**, BS**2**, BS**3**,. . . , BS**7** are only in a high state in the valid data intervals. A block select signal BSe in **FIG. 9** is used to precharge the first block, and is in a high state in the invalid data intervals.

[0083] The select switch blocks shown in **FIGS. 5 and 7** can be fabricated into a single module (or chip) separated from the LCD panel and then be connected to the data lines of the LCD panel, or can be directly manufactured on the LCD panel substrate using the TFTs. In this case, polycrystal silicon or single-crystal silicon can be used as the TFTs. Further, in the embodiments of the present invention, described was the example of precharging (or pre-discharging) the data lines connected to the (n+1)th block when the image signals are applied to the (n)th block. However, it is also obvious that data lines connected to an (n+j)th block can be precharged (or pre-discharged). Here, j can be any positive integer such as 1, 2, 3, etc., with the resultant sum

being smaller than the total number of blocks. Since the structure and operation of data drivers meeting such requirements can be easily conceived by those in the art to which the present invention pertains, a description and drawings thereof will be omitted herein.

[0084] In addition, the first block of the pixel lines may use a (j−1)th previous select signal from the final block of the previous pixel line to perform precharging/pre-discharging, or a separate first block precharging signal can be generated and used.

[0085] In the precharging method of the preferred embodiments of the present invention described in the above, since the data lines are precharged a number of times (in each block interval), it is possible to reduce a required maximum current of the system when compared to the conventional method of precharging in the intervals between each horizontal line. For example, in a color XGA display having 3072 data lines, assuming that a parasitic capacitance of each data line is 80 pF, a total load of 245.76 nF (80 pF×3072) must be precharged. However, in preferred embodiments of the present invention, since the data lines are divided into 16 blocks and each block is sequentially precharged, a significantly smaller 15.36 nF load is used for precharging each block.

[0086] **FIG. 10** shows a graph comparing current variations in a conventional precharging method and a precharging method of the present invention. As shown in the drawing, although the total power consumption in the precharging signal generator is the same, a peak current value is smaller in the present invention. Therefore, it can provide lots of freedom in designing the layout of the precharging signal generator. Further, since it is possible to perform precharging also in the valid data intervals, rather than only in the invalid data intervals as in the conventional method, precharging can be effectively performed in systems where the invalid data intervals are short.

[0087] Although the present invention was described above in its application to a drive device of a TFT-LCD, it is to be understood that the invention is not limited to this application, and can cover various modifications and equivalent arrangements. For example, the present invention can be applied to all displays where it is advantageous to precharge data lines to which image signals are applied. Further, although the select switch blocks of **FIGS. 5 and 7** are realized through MOS transistors, it is also possible to use bipolar transistors, transmission gates, etc.

[0088] A gate driver according to a preferred embodiment of the present invention will be described hereinafter with reference to **FIG. 11**. The gate driver comprises a group select signal generator **510**, a block select signal generator **520**, a sub-signal generator **530**, and a gate array **540**. The gate array **540** includes a plurality of AND gates A1, A2, . . . AY . . . , each output terminal of the AND gates being connected to a gate line of the LCD panel. The gate array **540** is divided into a Z-number of gate groups, and each gate group is, in turn, divided into a maximum X-number of gate blocks. Further, each gate block has a maximum Y-number of AND gates.

[0089] The group select signal generator **510** outputs group select signals Sg for selecting one of the gate groups of the gate array **540**. The group select signals Sg are transmitted to each gate group through a Z-number of bus lines. The block select signal generator **520** outputs block select signals Sb for selecting one of the gate blocks of a gate group. The block select signals Sb are collectively transmitted to the gate blocks of each of the gate groups through an X-number of bus lines. The sub-signal generator **530** outputs sub-signals Ss for selecting one of the AND gates in a gate block. The sub-signals Ss are output to the AND gates of each of the gate blocks through a Y-number of bus lines.

[0090] Each AND gate of the gate array **540** receives the group select signals Sg, the block select signals Sb and the sub-signals Ss, and performs an AND operation of these signals. These output signals of the gate array **540** are output to the gate lines of the LCD panel.

[0091] **FIG. 12** shows a waveform chart of the signals of the gate driver shown in **FIG. 11**. In **FIG. 12**, there are shown waveforms of the group select signals Sg output by the group select signal generator **510**, the block select signals Sb output by the block select signal generator **520**, and the sub-signals Ss output by the sub-signal generator **530**. Also shown is a waveform of output signals coming out of the gate array **540**.

[0092] As shown in the drawing, in an interval where one group select signal Sg is in a high state, an X-number (**4** in **FIG. 12**) of the block select signals Sb sequentially changes temporarily into a high state then back to a low state. Also, in an interval where one block select signals Sb is in a high state, a Y-number of the sub-signals Ss sequentially changes temporarily into a high state then back to a low state.

[0093] Since the group select signals Sg, the block select signals Sb, and the sub-signals Ss are applied to input terminals of the AND gates of **FIG. 11**, the output terminals of the AND gates are sequentially controlled to high then low states as shown in **FIG. 12**. Output signals of the AND gates act as gate drive signals are applied to each of the gate lines of the LCD panel.

[0094] In the gate driver of the present invention described above, each of the AND gates of the gate array **540** is connected to one of R gate lines, and the gate lines are divided into a plurality of gate blocks having a maximum Y-number of gate lines and a plurality of the gate blocks are divided into a Z-number of gate groups having a maximum X-number of blocks, satisfying the following relation: $Z \times X \times Y \geqq R$.

[0095] For example, in an XGA display having 768 gate lines, all the gate lines are divided into 64 blocks each having 12 gate lines, and the 64 blocks are divided into 8 groups each having 8 blocks. In this case, Z is equal to 8, X is equal to 8, and Y is equal to 12. If the gate driver is structured in this manner, 28 bus lines are required (8+8+12) which is a significantly lower number of bus lines than required in the prior art. Further, in the case of a SXGA display having 1024 gate lines, or R=1024, and where the number of the elements are selected such that $Z \times X \times Y \geqq R$ is satisfied, the number of bus lines can be reduced. At this time, it is preferable that the selection of X, Y and Z is done such that the number of signal transmission lines (i.e., X+Y+Z) is minimized. Here, if the number of all the gate lines R is less than the product of the groups Z, the blocks X and the gate lines Y, the number of blocks (or gate lines) either in the first or last group must be adjusted to be less than the others.

[0096] It is to be understood that the gate driver is not limited to the structure and operation described above, and can cover various modifications and equivalent arrangements. For example, the AND gates of the gate array **540** shown in **FIG. 11** can be replaced by NAND gates **551** of a gate array **550** as shown in **FIG. 13**. Connected to the NAND gates **551** are inverters **552**, **553** and **554**. Here, the NAND gates **551** and the inverters **552**, **553** and **554** together act as AND gates. The use of the NAND gates **551** combined with the inverters **552**, **553** and **554** improves a current drive capability of the gate signals supplied to the gate lines. This is due to the incremental size of the inverters **552**, **553** and **554** connected to the NAND gates **551** such that the gate ON signals are able to be effectively transmitted to the gate lines.

[0097] The elements of the AND gates, the NAND gates and inverters shown in **FIGS. 11 and 13** can be manufactured using NMOS transistors, PMOS transistors, transmission gates, or a mixture thereof.

[0098] The gate drivers shown in **FIGS. 11 and 13** can be made into a single module (or chip) separated from the LCD panel then connected to the gate lines of the LCD panel, or can be directly manufactured on the LCD panel substrate using the TFTs. At this time, poly-crystal silicon or single-crystal silicon can be used as the TFTs. Further, it is also possible to use TFTs to directly manufacture only the gate arrays on the LCD panel substrate, while the remaining elements are made into an independent module.

[0099] In the above, although the gate driver has a structure in which the gate lines were divided into blocks, and the blocks were divided into groups, it is possible to further divide the groups into separate groups. If the groups are again divided, more select signal generators are needed to generate signals for the selection of the separate groups, and the AND gates of the gate array require more input pins.

[0100] Further, the gate driver of the present invention was described with its application to a TFT-LCD. However, the gate driver of the present invention can be used with other displays such as PDPs and FEDs in which image signals are applied to vertical lines, and scanning signals are applied to transmit the image signals sequentially to horizontal lines.

[0101] In the present invention described above, since the image signals are applied to the data line after precharging is performed in a previous block interval, a maximum current required for precharging is reduced, and precharging in a system having short invalid data intervals can be effectively realized. Further, since the group select signals, block select signals, and sub-signals are applied after the gate lines are divided into blocks and the blocks are divided into groups, the number of bus lines and the area of the circuit can be reduced, and line defects can be minimized.

[0102] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

What is claimed is:

1. A liquid crystal display (LCD) comprising:

an LCD panel including a plurality of gate lines, a plurality of data lines insulated from and intersecting the gate lines, and a plurality of TFTs each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines;

a gate driver for sequentially supplying gate drive signals to the gate lines to turn the TFTs ON; and

a data driver that groups the data lines into an X-number of blocks, each block having a predetermined number of data lines, and applies image signals to the data lines in an (n)th block, and precharging voltages to the data lines in the (n+j)th block.

2. The LCD of claim 1, wherein the data driver comprises:

a block select signal generator for generating block select signals to select one of the blocks;

an image signal processor that generates the image signals for the data lines in a selected block;

a precharging signal generator that generates the precharging voltages for the data lines in the selected block;

an X-number of image signal select switch blocks for switching each of the image signals for application to one of the blocks; and

an X-number of precharging select switch blocks for switching each of the precharging voltages for application to one of the blocks,

wherein an (n)th block select signal simultaneously turns ON an (n)th image signal select switch block and an (n+j)th precharging signal select switch block.

3. The LCD of claim 2, wherein the precharging voltages are at a single voltage level.

4. The LCD of claim 3, wherein the precharging voltages have a center value between a maximum value and a minimum value of the image signals.

5. The LCD of claim 3, wherein an (n)th image signal select switch block among the X-number select switch blocks comprises at least a Y-number of first MOS transistors having sources connected to the image signals, drains connected to the data lines, and gates connected to the (n)th block select signal; and

wherein an (n)th precharging signal select switch block among the X-number of select switch blocks comprises at least a Y-number of second MOS transistors having sources connected to the precharging voltages, drains connected to the data lines, and gates connected to the (n−j)th block select signal.

6. The LCD of claim 5, wherein the first and second MOS transistors are TFTs fabricated on a substrate of the LCD.

7. The LCD of claim 6, wherein the TFTs are made of poly-crystal silicon or single-crystal silicon.

8. The LCD of claim 2, wherein the precharging voltages include a first precharging signal and a second precharging signal having a first voltage level and a second voltage level, respectively.

9. The LCD of claim 8, wherein the first precharging signal has a predetermined value between a maximum and a center value of the image signals, and the second pre-

charging signal has a predetermined value between a minimum value and a center value of the image signals.

10. The LCD of claim 9, wherein the (n)th image signal select switch block among the X-number of select switch blocks comprises at least a Y-number of first MOS transistors having sources connected to the image signals, drains connected to the data lines, and gates connected to the (n)th block select signal; and

wherein an (n)th precharging signal select switch block among the X-number of select switch blocks comprises at least a Y-number of second MOS transistors having sources connected to the precharging voltages, drains connected to the data lines, and gates connected to the (n−j)th block select signal.

11. The LCD of claim 10, wherein the first precharging signal is applied to the sources of the second MOS transistors connected to odd data lines, and the second precharging signal is applied to the sources of the second MOS transistors connected to even data lines.

12. The LCD of claim 11, wherein the first and second MOS transistors are TFTs fabricated on a substrate of the LCD.

13. The LCD of claim 12, wherein the TFTs are made from poly-crystal silicon or single-crystal silicon.

14. A drive apparatus for a liquid crystal display (LCD), the LCD including a plurality of gate lines, a plurality of data lines insulated from and intersecting the gate lines, matrix-type pixels defined by the gate lines and the data lines, and a plurality of TFTs each provided in one of the pixels and each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines, wherein the apparatus comprises:

a gate driver for sequentially supplying gate drive signals to the gate lines to turn the TFTs ON; and

a data driver that groups the data lines into an X-number of blocks, each block having a predetermined number of data lines, and applies image signals to the data lines in an (n)th block, and precharging voltages to the data lines in the (n+j)th block.

15. The drive apparatus of claim 14, wherein the data driver comprises:

a block select signal generator for generating block select signals to select one of the blocks;

an image signal processor that generates the image signals for the data lines in the selected block;

a precharging signal generator that generates the precharging voltages for the data lines in the selected block;

X-number of image signal select switch blocks for switching each of the image signals for application to one of the blocks; and

X-number of precharging select switch blocks for switching each of the precharging voltages for application to one of the blocks,

wherein the (n)th block select signal simultaneously turns ON the (n)th image signal select switch block and the (n+j)th precharging signal select switch block.

16. The drive apparatus of claim 15, wherein j is 1.

17. The drive apparatus of claim 16, wherein a block select signal applied to a first precharging select switch block for precharging a first block uses a block select signal applied to a last image signal select switch block for applying the image signals to a last block.

18. The drive apparatus of claim 15, wherein a block select signal applied to a first precharging select switch block for precharging a first block uses a separate first block precharging signal.

19. The drive apparatus of claim 18, wherein the first block precharging signal is generated in an invalid data interval of a horizontal synchronous signal interval.

20. The drive apparatus of claim 15, wherein the precharging voltages are at a single voltage level.

21. The drive apparatus of claim 20, wherein the (n)th image signal select switch block among the X-number select switch blocks comprises at least a Y-number of first switches having a first terminal to which the image signals are applied, a second terminal connected to the data lines, and a third terminal to which the (n)th block select signal is applied;

wherein the (n)th precharging signal select switch block among the X-number of select switch blocks comprises at least a Y-number of second switches having a first terminal to which the precharging voltages are applied, a second terminal connected to the data lines, and a third terminal to which the (n−j)th block select signal is applied; and

wherein the first and the second switches apply the image signals and the precharging voltages, respectively applied to the first terminal of the first switching element and the first terminal of the second switching element, to the data lines according to the block select signals applied to the third terminals of the first and second switches.

22. The drive apparatus of claim 21, wherein the first and the second switches are MOS transistors having a source to which image signals and precharging voltages are respectively applied, a drain connected to data lines, and a gate to which the block select signals are applied.

23. The drive apparatus of claim 15, wherein the precharging voltages each include a first precharging signal and a second precharging signal having a first voltage level and a second voltage level, respectively.

24. The drive apparatus of claim 23, wherein magnitudes of the first and second precharging signals are changed in units of frames.

25. The drive apparatus of claim 23, wherein the (n)th image signal select switch block among the X-number select switch blocks comprises at least a Y-number of first switches having a first terminal to which the image signals are applied, a second terminal connected to the data lines, and a third terminal to which the (n)th block select signal is applied;

wherein the (n)th precharging signal select switch block among the X-number of select switch blocks comprises at least a Y-number of second switches having a first terminal to which the precharging voltages are applied, a second terminal connected to the data lines, and a third terminal to which the (n−j)th block select signal is applied; and

wherein the first and second switches apply the image signals and the precharging voltages, respectively applied to the first terminal of the first switches and the

first terminal of the second switches, to the data lines according to the block select signals applied to the third terminals of the first and second switches.

26. The drive apparatus of claim 25, wherein the first and second switches are MOS transistors having a source to which image signals and precharging voltages are respectively applied, a drain connected to the data lines, and a gate to which the block select signals are applied.

27. A drive apparatus for a display device, the display device including a plurality of scanning lines and a plurality of data lines intersecting the scanning lines, wherein the drive apparatus comprises:

a scanning driver for sequentially supplying scanning signals to the scanning lines; and

a data driver that groups the data lines into an X-number of blocks, each block having a predetermined number of data lines, and applies image signals to the data lines in an (n)th block and precharging voltages to the data lines in the (n+j)th block.

28. The drive apparatus of claim 27, wherein the data driver comprises:

a block select signal generator for generating block select signals to select one of the blocks;

an image signal processor that generates the image signals for the data lines in a selected block;

a precharging signal generator that generates the precharging voltages for application to the data lines in the selected block;

X-number of image signal select switch blocks for switching each of the image signals for application to one of the blocks; and

X-number of precharging select switch blocks for switching each of the precharging voltages for application to one of the blocks,

wherein the (n)th block select signal simultaneously turns ON the (n)th image signal select switch block and the (n+j)th precharging signal select switch block.

29. A method for driving a liquid crystal display (LCD), the LCD including a plurality of gate lines, a plurality of data lines insulated from and intersecting the gate lines, matrix-type pixels defined by the gate lines and the data lines, and a plurality of TFTs each provided in one of the pixels and each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines, a gate driver for applying gate drive signals to the gate lines and a data driver that groups the data lines into an X-number of blocks, each block having a predetermined number of data lines and applies image signals to the data lines in an (n)th block and precharging voltages to the data lines in the (n+j)th block, wherein the method comprises the steps of:

sequentially supplying gate drive signals to the gate lines to turn the TFTs ON; and

applying image signals to the data lines in the (n)th block and precharging voltages to the data lines in the (n+j)th block at the same time.

30. The method of claim 29, wherein j is 1.

31. The method of claim 30, wherein if the image signals are applied to data lines in a last block, the precharging voltages are, at the same time, applied to data lines in a first block.

32. The method of claim 29, wherein a first block uses a separate first block precharging signal received externally.

33. A liquid crystal display (LCD), comprising:

an LCD panel including an R-number of gate lines, a plurality of data lines insulated from and intersecting the gate lines, and a plurality of TFTs each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines;

a data driver for applying image signals to the data lines; and

a gate driver for sequentially supplying gate drive signals to the gate lines to turn the TFTs ON,

wherein the R-number of gate lines are grouped into an X-number of blocks having a minimum Y-number of gate lines, and the X-number of blocks are grouped into a minimum Z-number of groups connected to the gate driver.

34. The LCD of claim 33, wherein the gate driver comprises:

a group select signal generator for generating group select signals to select one of the Z-number of groups;

a block select signal generator for generating block select signals to select one of the X-number of blocks;

a sub-signal generator for generating sub-signals to select one of the Y-number of gate lines; and

a gate array for receiving the group select signals, the block select signals, and the sub-signals, and outputting the gate drive signals.

35. The LCD of claim 34, wherein the gate array performs an AND operation of the group select signals, the block select signals, and the sub-signals.

36. The LCD of claim 35, wherein the gate array comprises a plurality of AND gates including input terminals connected to each of the group select signals, the block select signals, and the sub-signals, and output terminals each connected to one of the gate lines.

37. The LCD of claim 35, wherein the gate array comprises:

a plurality of NAND gates into which the group select signals, the block select signals, and the sub-signals are input; and

a plurality of inverters for inverting output signals of the NAND gates and outputting the inverted signals to the gate lines.

38. The LCD of claim 37, wherein the inverters comprise a first, second and third inverter connected to the NAND gates, and a current drive capacity increments from the first to the third inverter.

39. The LCD of claim 34, wherein X, Y and Z satisfy the condition of $X \times Y \times Z \geqq R$,minimizing the sum of X, Y and Z.

40. The LCD of claim 39, wherein, when $X \times Y \times Z > R$, either a first group or a last group of the Z-number of groups has fewer gate lines than the other groups.

41. The LCD of claim 34, wherein the gate driver is made of TFTs formed on a substrate of the LCD panel.

42. The LCD of claim 34, wherein the gate array is made of TFTs formed on a substrate of the LCD panel.

43. The LCD of claim 33, wherein the Z-number of groups are divided into a V-number of separate groups, each of the separate groups having a maximum of W groups; and V, W, X and Y meet the condition of $V \times W \times X \times Y \geqq R$, minimizing the sum of V, W, X and Y.

44. A drive apparatus for a display device, the display device including an R-number of scanning lines transmitting scanning signals and a plurality of data lines transmitting image signals, comprising:

a data driver for applying image signals to data lines; and

a scanning driver for sequentially supplying the scanning signals to the scanning lines such that the image signals applied to the data lines are displayed;

wherein the R-number of scanning lines are grouped into a plurality of blocks having a maximum Y-number of the scanning lines, and the blocks are grouped into a Z-number of groups having a maximum X-number of blocks.

45. The drive apparatus of claim 44, wherein the scanning driver comprises:

a group select signal generator for generating group select signals to select one of the Z-number of groups;

a block select signal generator for generating block select signals to select one of the X-number of blocks;

a sub-signal generator for generating sub-signals to select one of the Y-number of gate lines; and

a gate array for receiving the group select signals, the block select signals, and the sub-signals, and outputting the scanning signals.

46. The LCD of claim 45, wherein the gate array performs an AND operation of the group select signals, the block select signals, and the sub-signals.

47. The LCD of claim 45, wherein X, Y and Z satisfy the condition of $X \times Y \times Z \geqq R$, minimizing the sum of X, Y and Z.

48. A method for driving an LCD, the LCD including an R-number of gate lines grouped into a plurality of blocks having a maximum Y-number of the gate lines, the blocks being grouped into a Z-number of groups having a maximum X-number of blocks, a plurality of data lines insulated from and intersecting the gate lines, and a plurality of TFTs each having a gate electrode connected to one of the gate lines and a source electrode connected to one of the data lines, wherein the method comprises the steps of:

selecting one of the groups;

selecting one of the blocks in a selected group; and

selecting one of the gate lines in a selected block and applying a gate signal to a selected gate line to turn on the TFTs.

49. The method of claim 48, wherein X, Y and Z satisfy the condition of $X \times Y \times Z \geqq R$. minimizing the sum of X, Y and Z.

50. The method of claim 49, wherein, when $X \times Y \times Z > R$, either a first group or a last group of the Z-number of groups has less gate lines than the other groups.

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摘要(译)

公开了一种显示装置（例如，液晶显示器），以及用于驱动该显示装置的装置和方法。 LCD包括具有多条栅极线的LCD面板，与栅极线绝缘并交叉的多条数据线，以及多个TFT，每个TFT具有连接到栅极线之一的栅电极和连接到栅极线的源电极。其中一条数据线;栅极驱动器，用于顺序地向栅极线提供栅极驱动信号以使TFT导通;数据驱动器，用于将数据线分成一定数量的块，每个块具有预定数量的数据线，并将图像信号施加到第（n）块中的数据线，并将预充电电压施加到数据线在第（n + j）块中。该装置包括栅极驱动器和数据驱动器。该方法包括以下步骤：将栅极驱动信号顺序提供给栅极线以使TFT导通;将图像信号施加到第（n）块中的数据线，并将预充电电压施加到第（n + j）块中的数据线。