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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE SAME**

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None
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(57) **ABSTRACT**

A liquid crystal display device is provided in which the aperture ratio can be increased in a pixel including a thin film transistor in which an oxide semiconductor is used. In the liquid crystal display device, the thin film transistor including a gate electrode, a gate insulating layer and an oxide semiconductor layer which are provided so as to overlap with the gate electrode, and a source electrode and a drain electrode which overlap part of the oxide semiconductor layer is provided between a signal line and a pixel electrode which are provided in a pixel portion. The off-current of the thin film transistor is 1×10^{-13} A or less. A potential can be held only by a liquid crystal capacitor, without a capacitor which is parallel to a liquid crystal element, and a capacitor connected to the pixel electrode is not formed in the pixel portion.

16 Claims, 19 Drawing Sheets

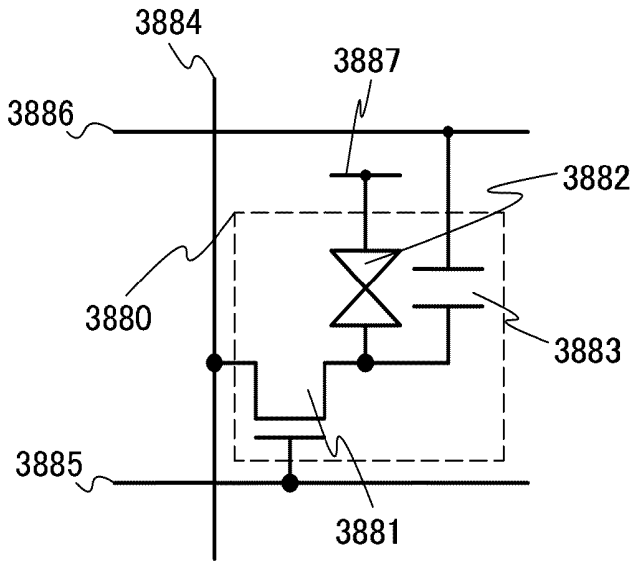

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FIG. 1A

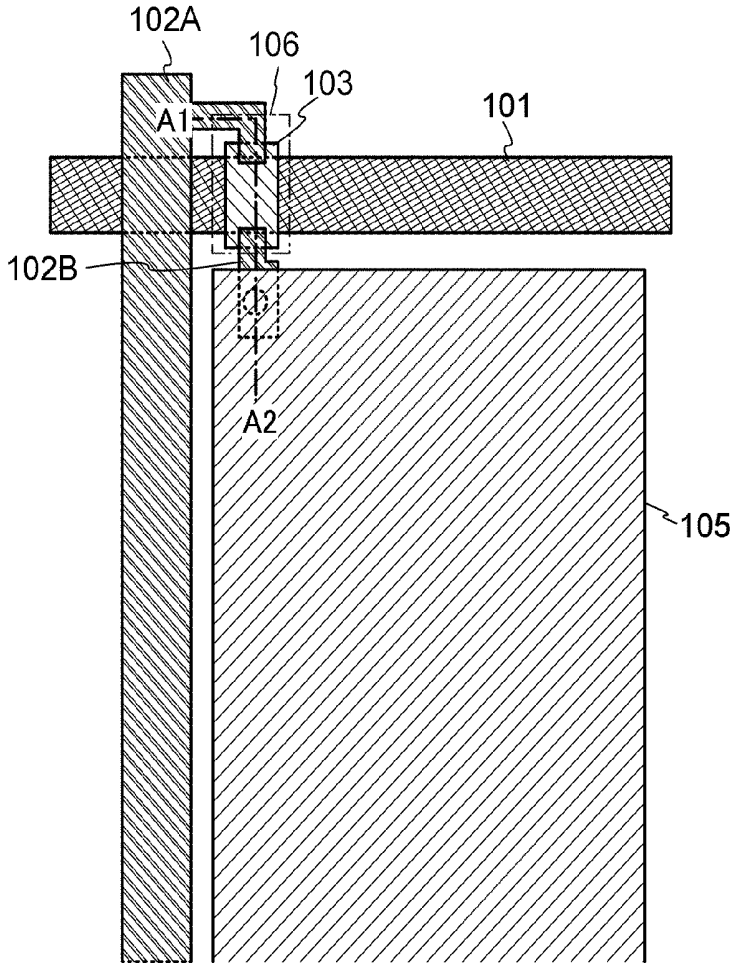

102A
106
103
101
A1
102B
A2
105

FIG. 1B

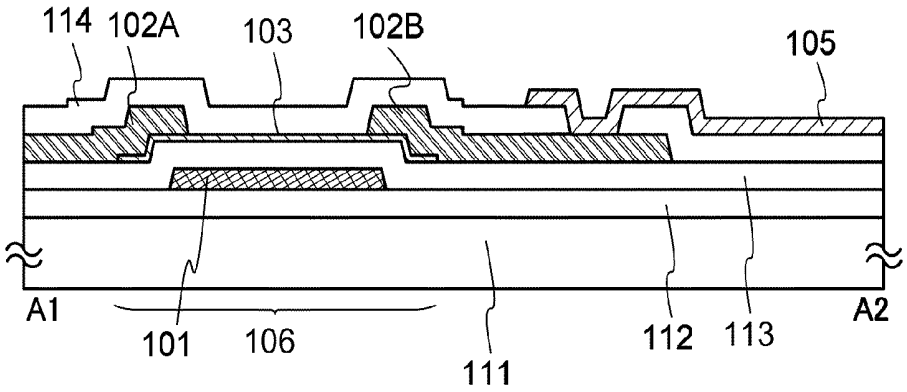

114
102A
103
102B
105
A1
101
106
111
112
113
A2

FIG. 2A

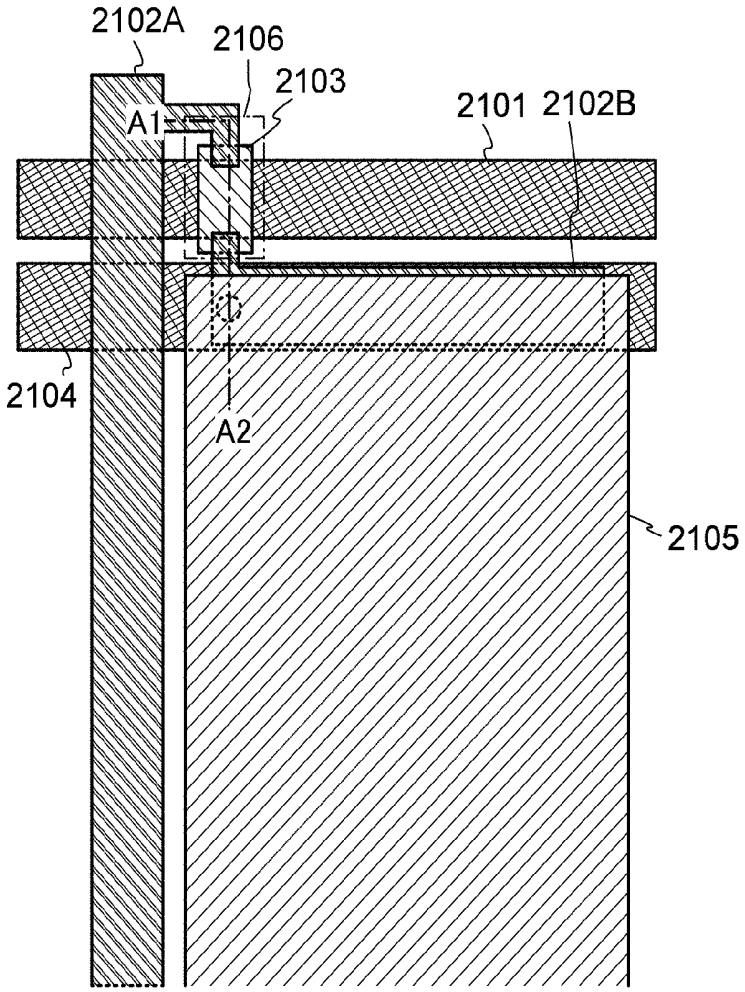

2102A
2106
2103
A1
2101
2102B
2104
A2
2105

FIG. 2B

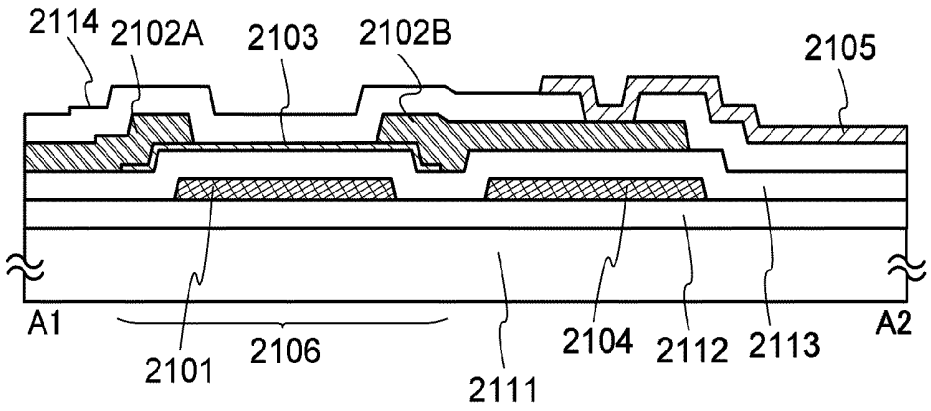

2114
2102A
2103
2102B
2105
A1
2101
2106
2111
2104
2112
2113
A2

FIG. 3A

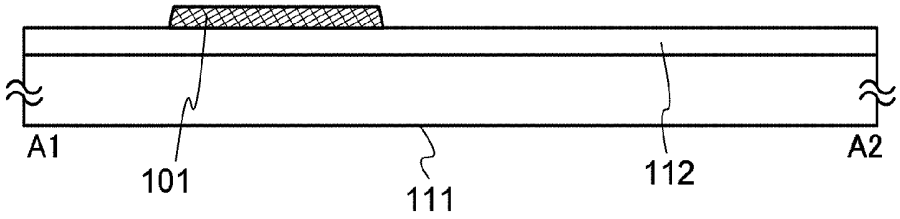


FIG. 3B

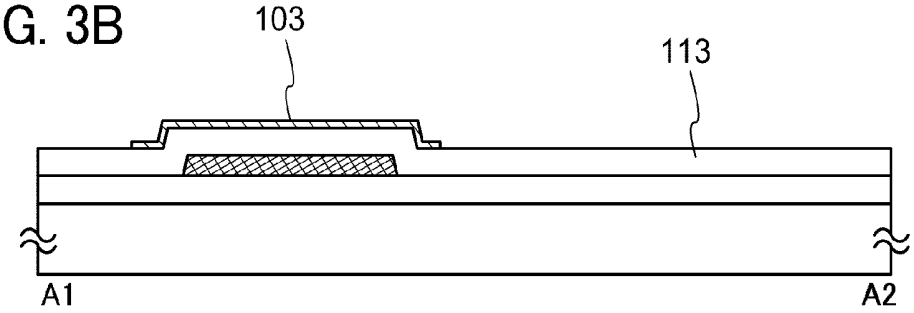


FIG. 3C

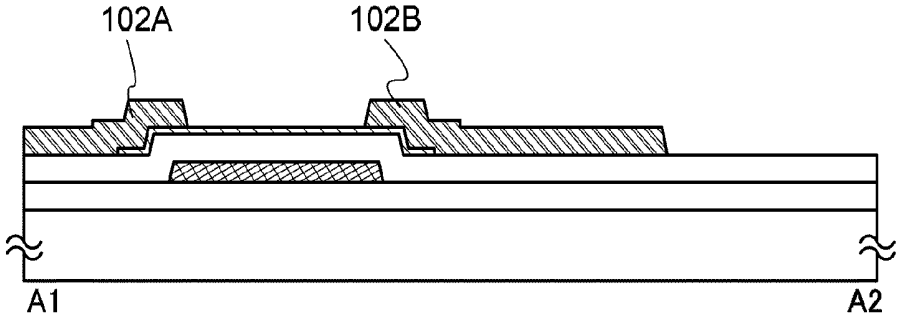


FIG. 3D

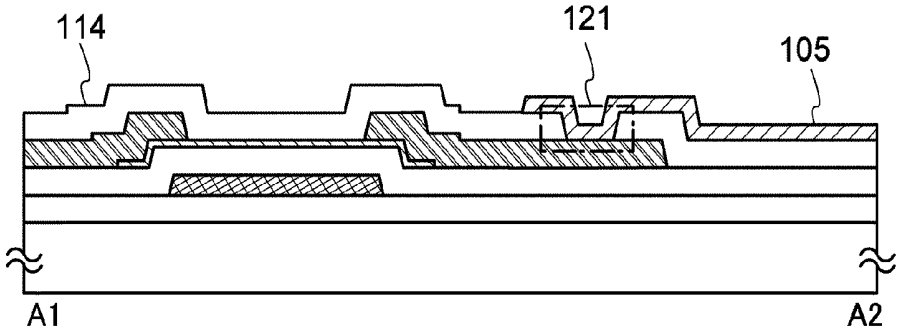


FIG. 4

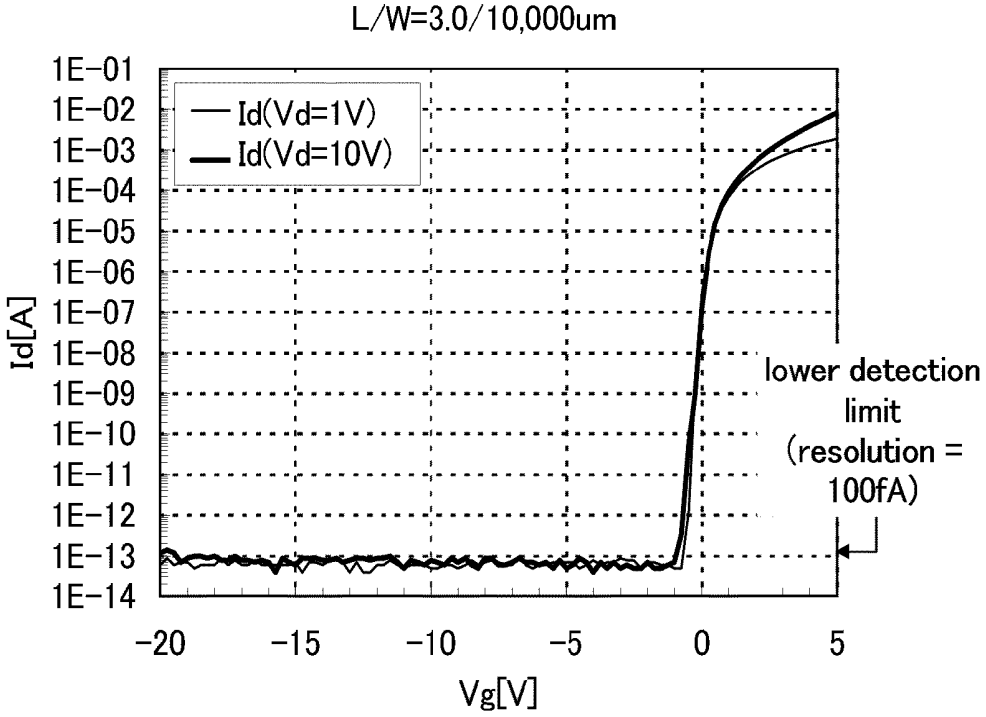

L/W=3.0/10,000um
Id(Vd=1V)
Id(Vd=10V)
Id[A]
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E-14
-20
-15
-10
-5
0
5
Vg[V]
lower detection limit (resolution = 100fA)

FIG. 5A

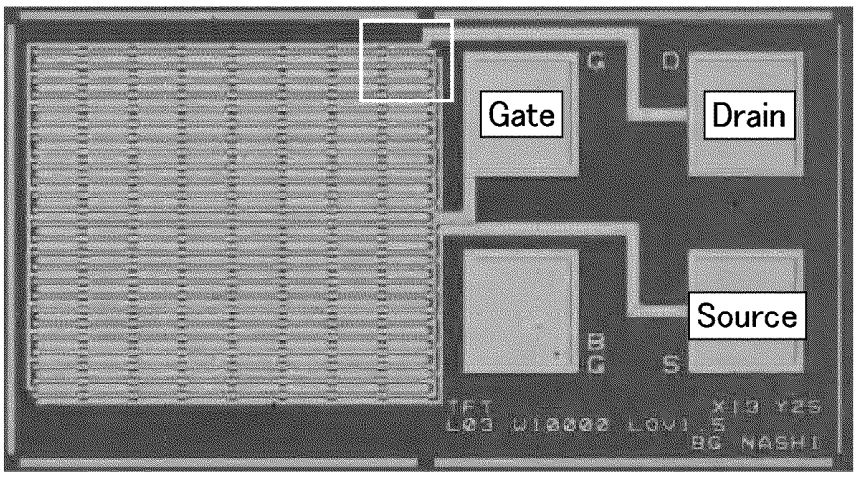

G
D
Gate
Drain
Source
B
G
S
TFT
L03 W10002 L0v1 S
X10 Y25
BC NASHI

FIG. 5B

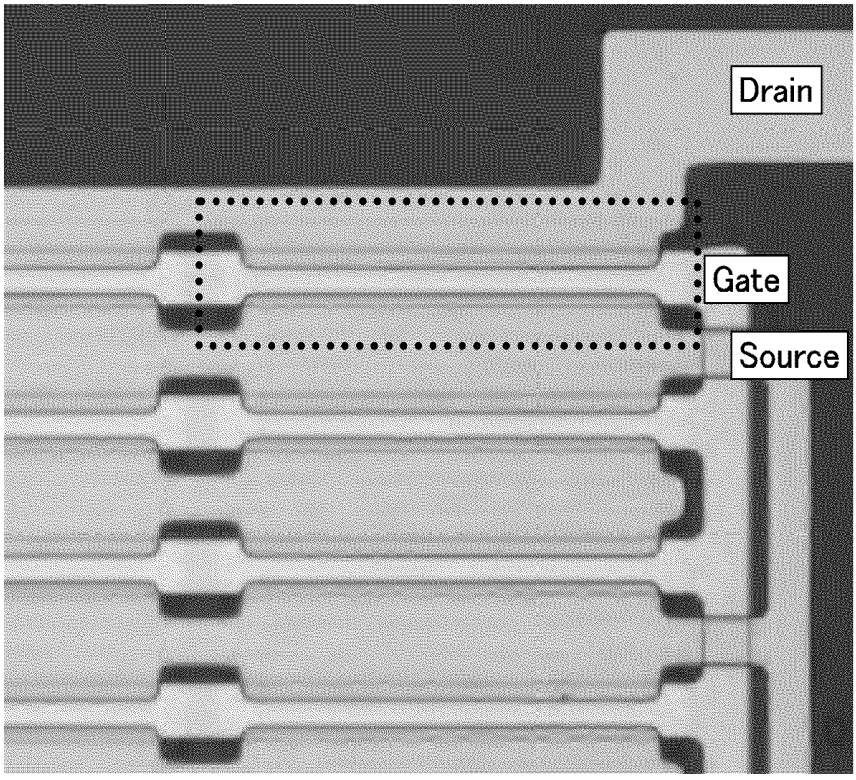

Drain
Gate
Source

FIG. 6A

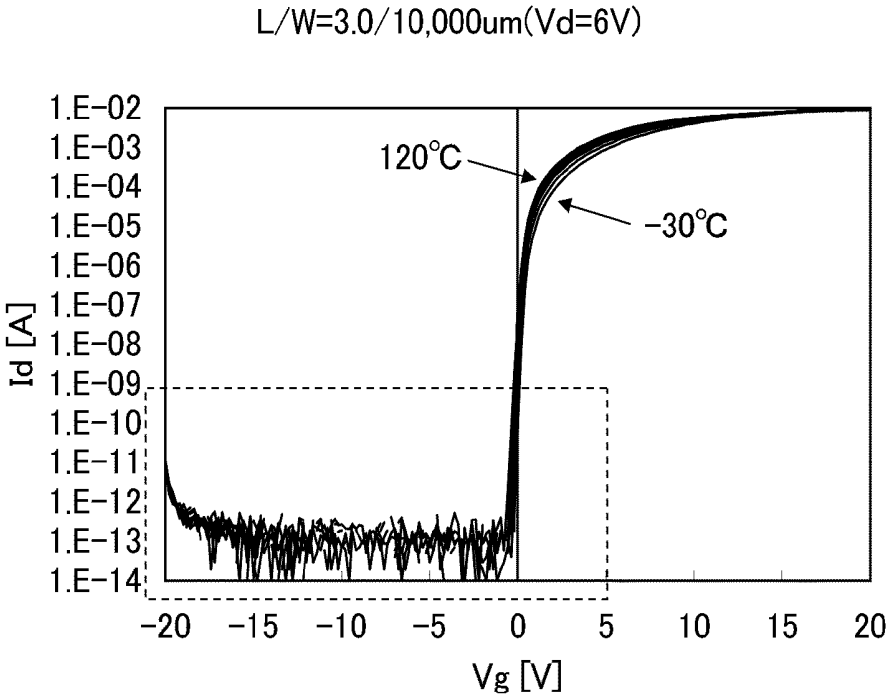

L/W=3.0/10,000um(Vd=6V)
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
Id [A]
120°C
-30°C
-20
-15
-10
-5
0
5
10
15
20
Vg [V]

FIG. 6B

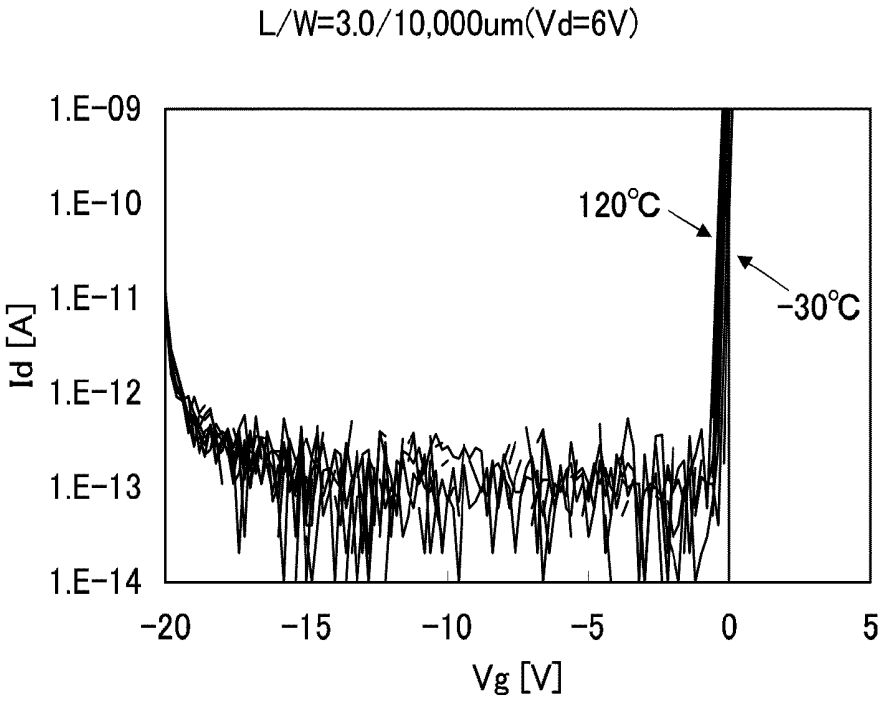

L/W=3.0/10,000um(Vd=6V)
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
Id [A]
120°C
-30°C
-20
-15
-10
-5
0
5
Vg [V]

FIG. 7

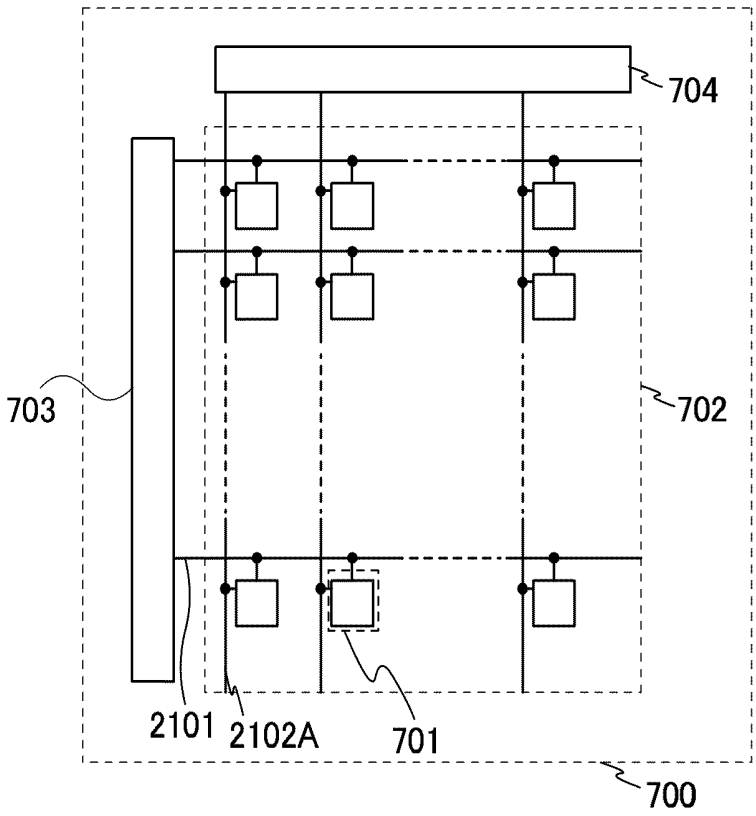


FIG. 8

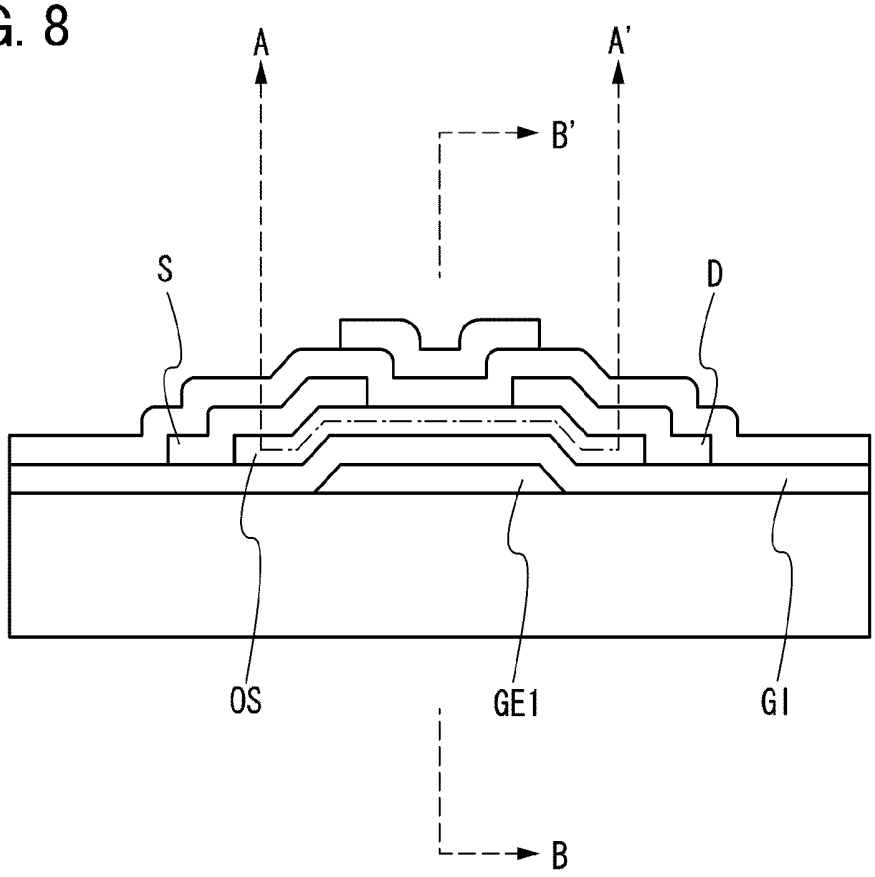


FIG. 9A

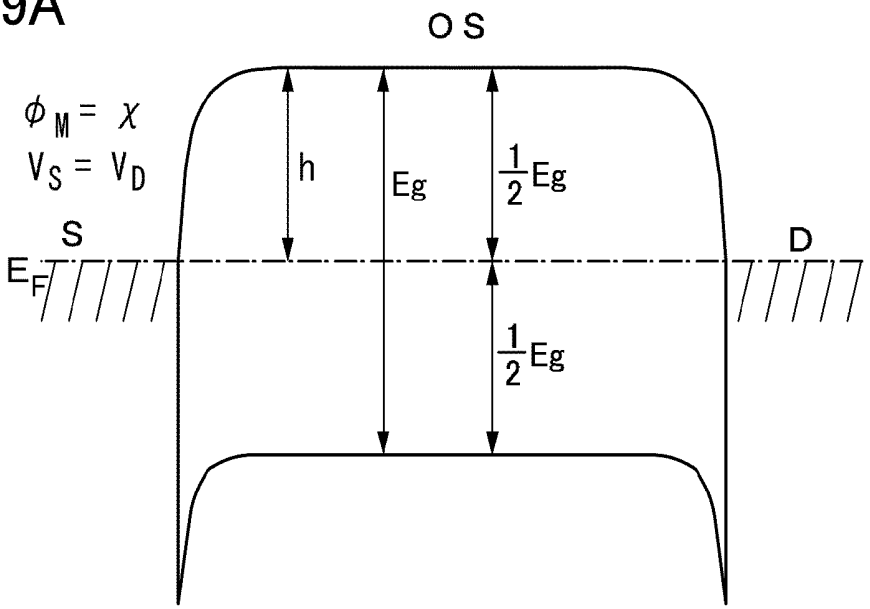

OS
$\phi_M = \chi$
$V_S = V_D$
h
Eg
$\frac{1}{2}$Eg
S
D
E_F
$\frac{1}{2}$Eg

FIG. 9B

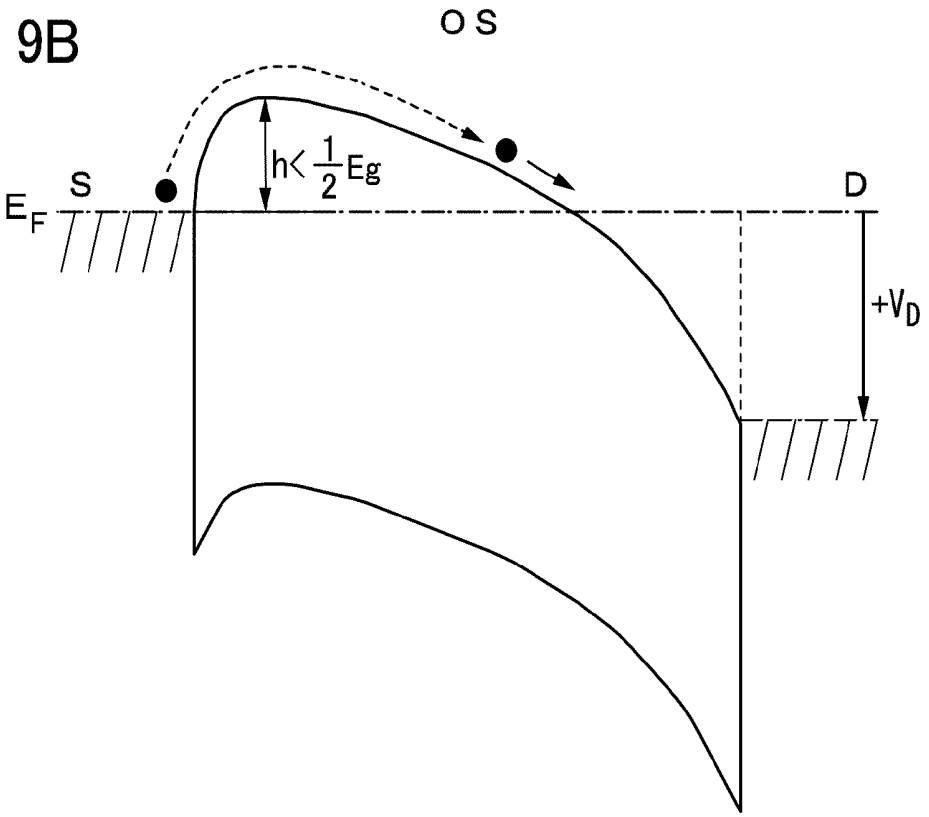

OS
$h < \frac{1}{2}$Eg
S
D
E_F
$+V_D$

FIG. 10A

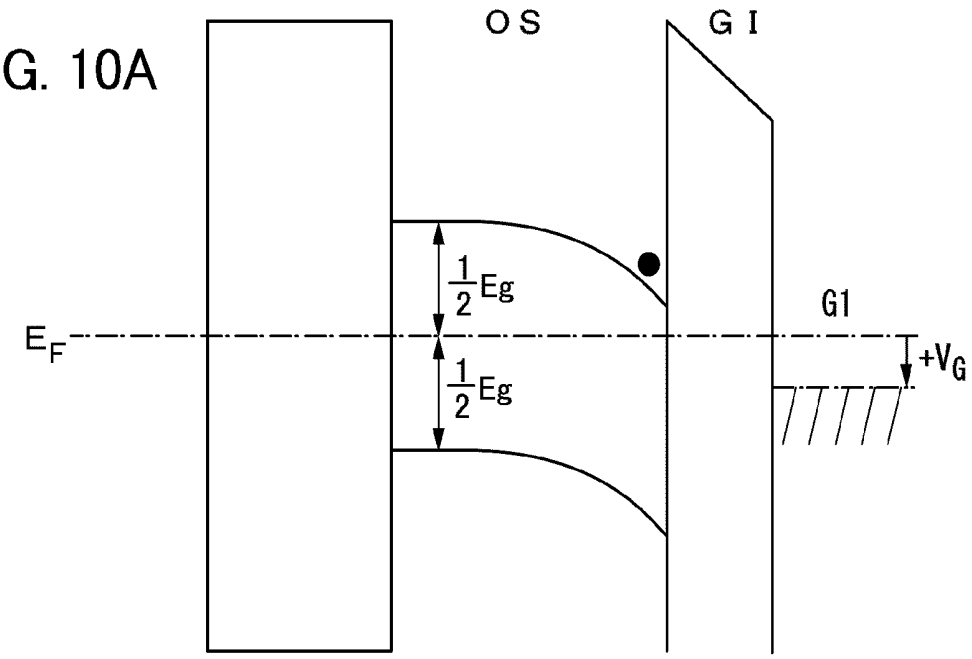


FIG. 10B

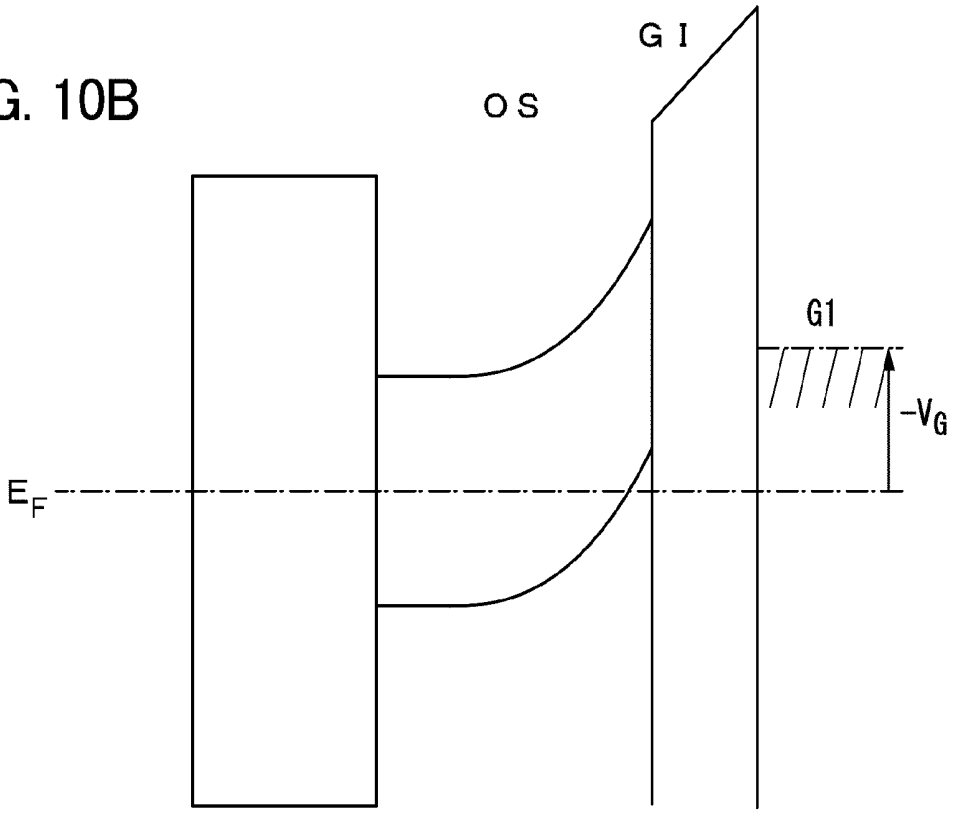


FIG. 11

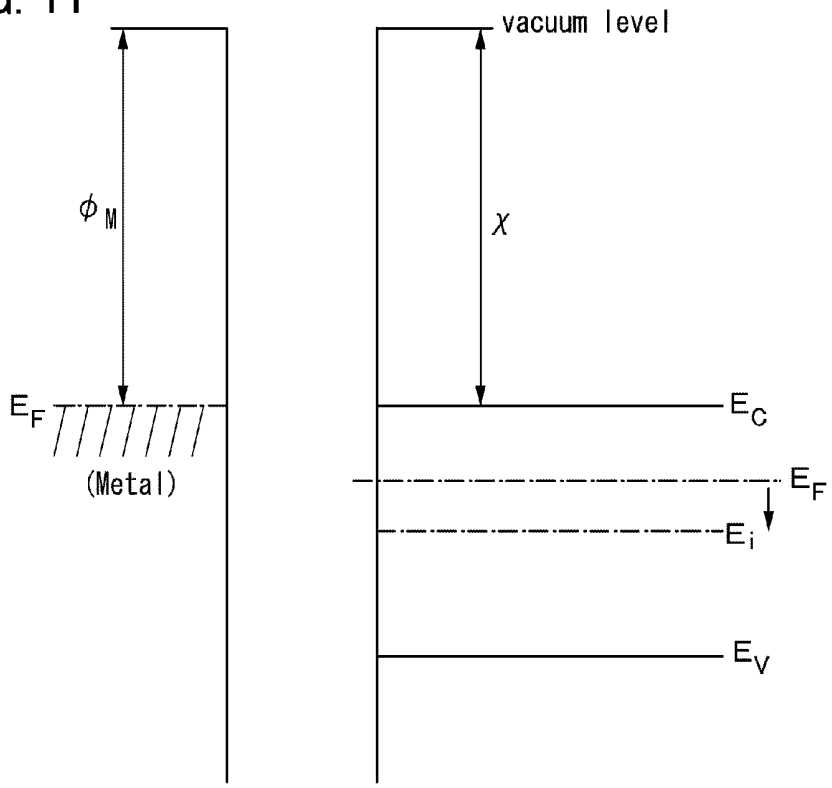


FIG. 12A

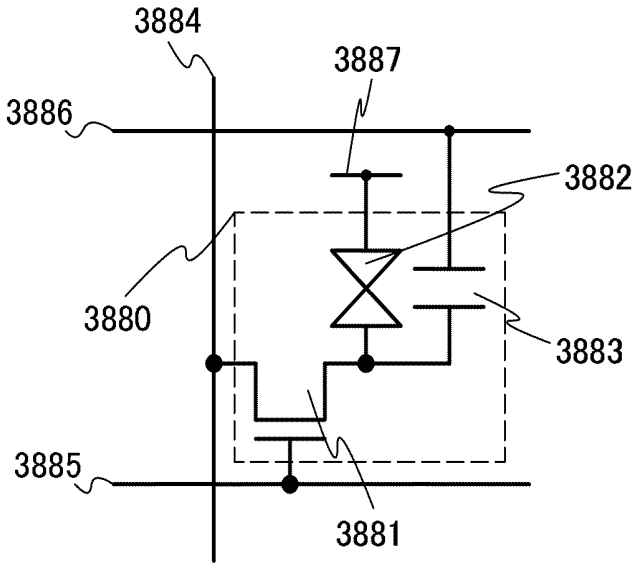


FIG. 12B

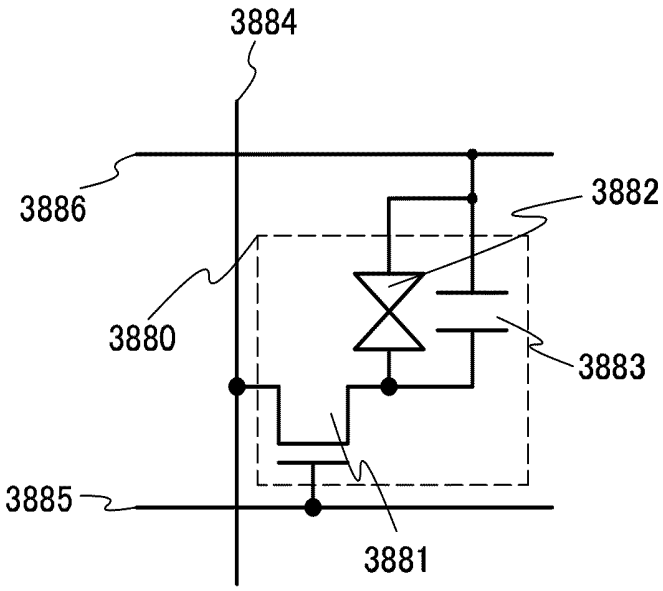


FIG. 13A

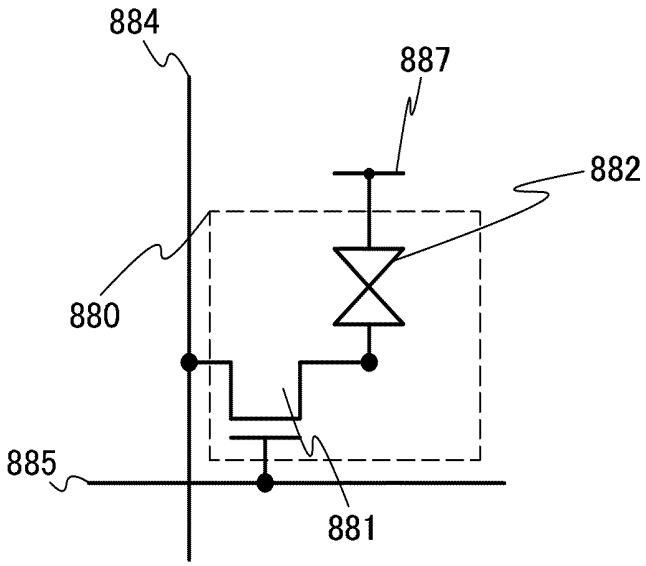


FIG. 13B

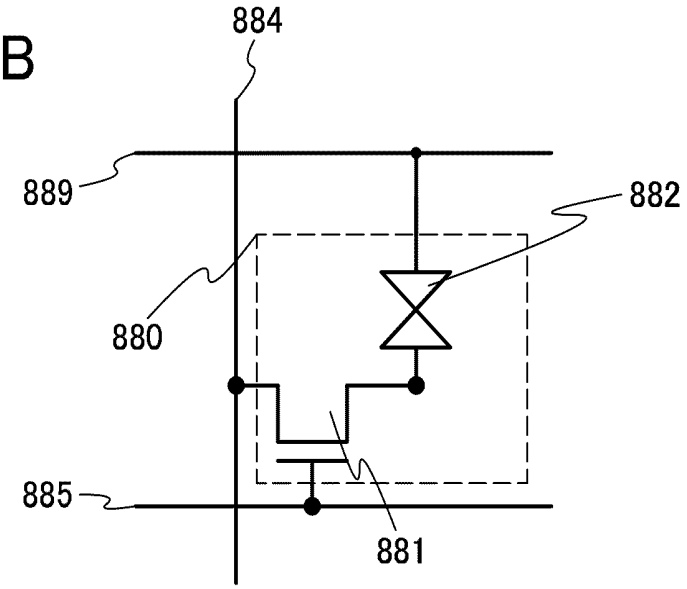


FIG. 14A

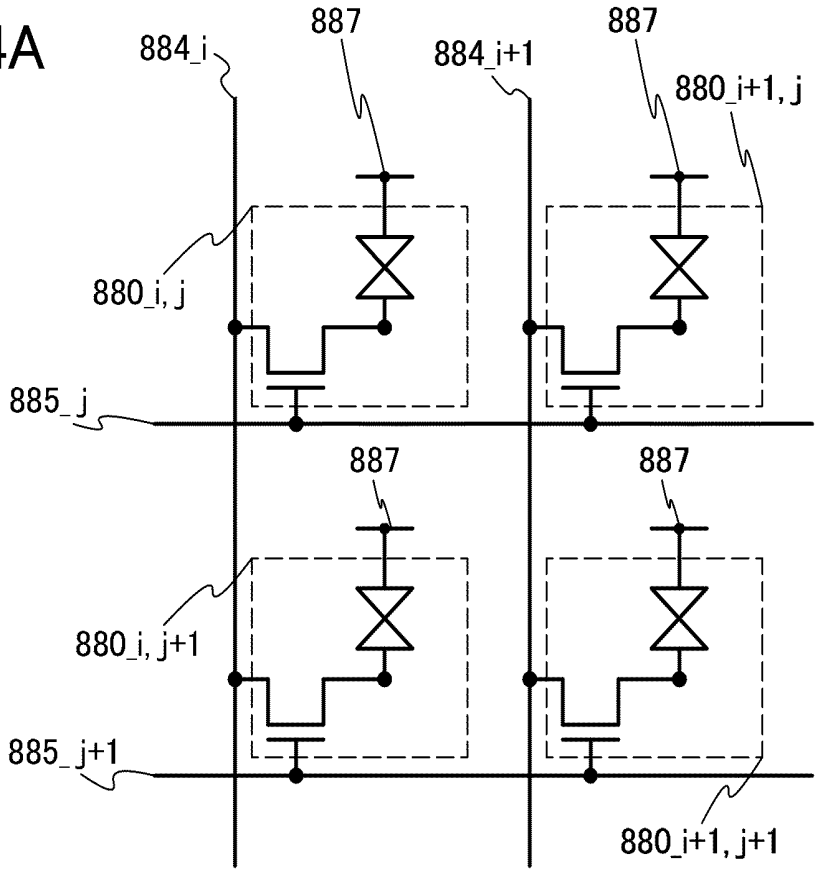


FIG. 14B

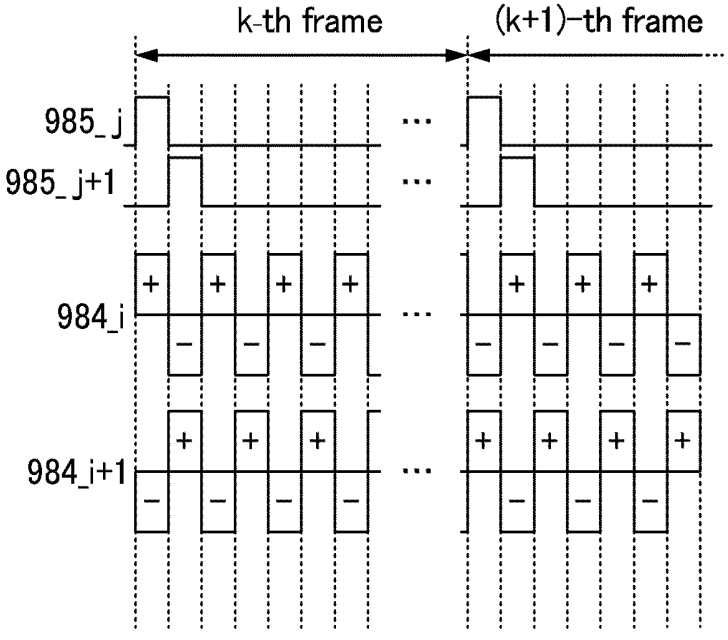


FIG. 15A

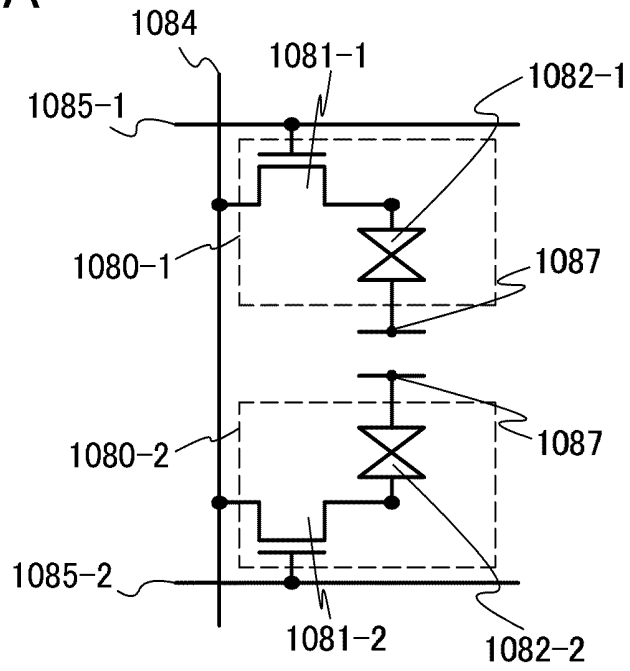


FIG. 15B

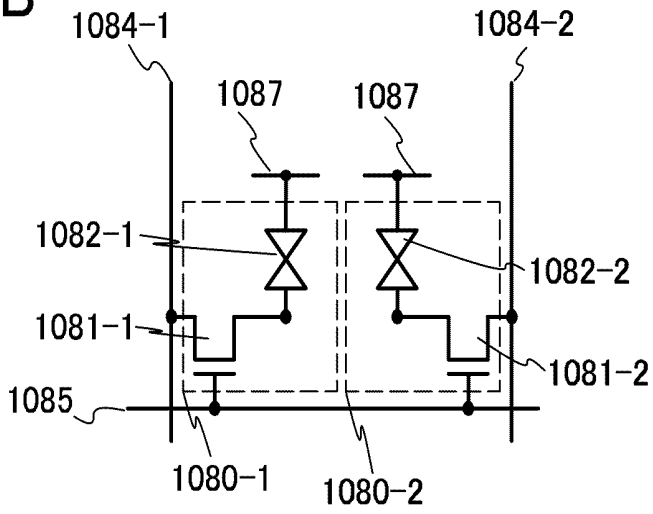


FIG. 16A

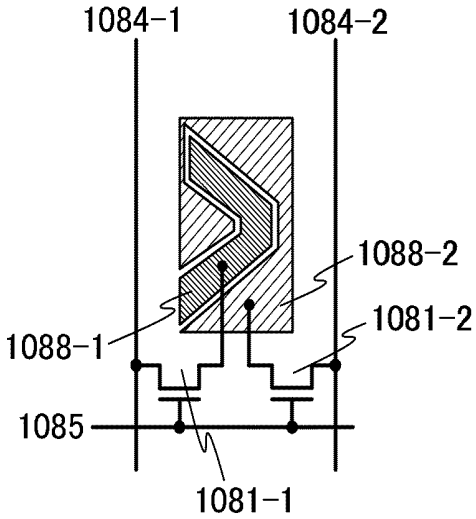


FIG. 16B

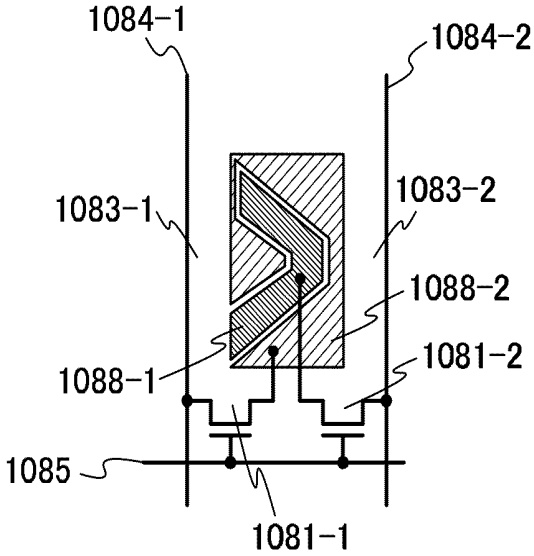


FIG. 17A

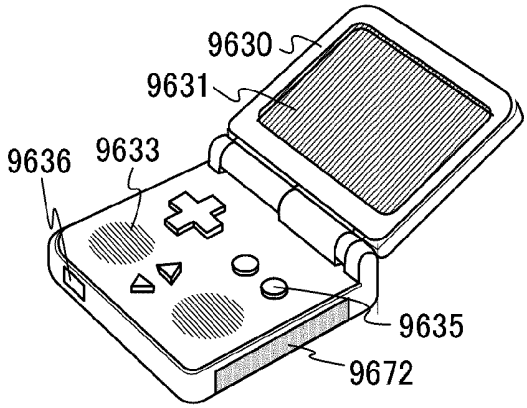


FIG. 17B

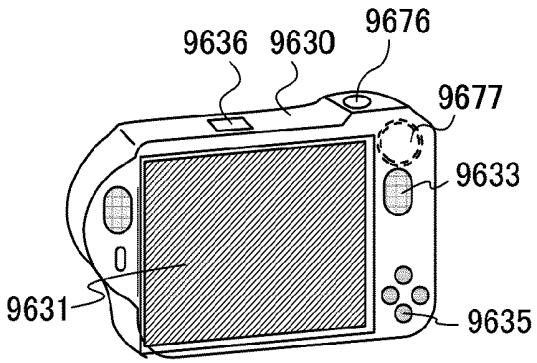


FIG. 17C

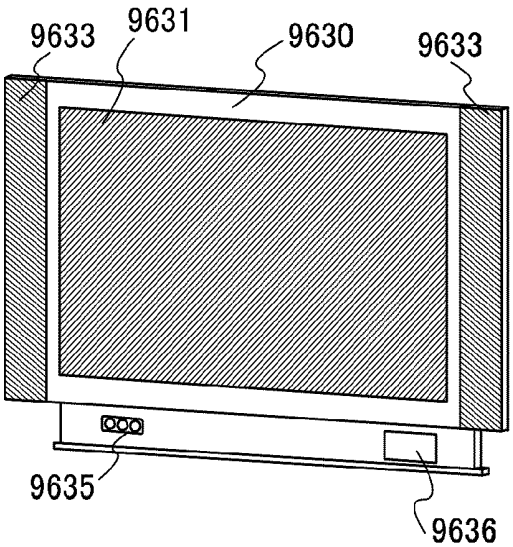


FIG. 18A

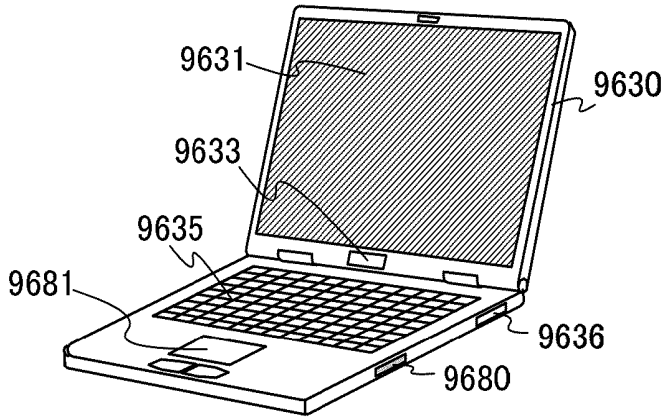


FIG. 18B

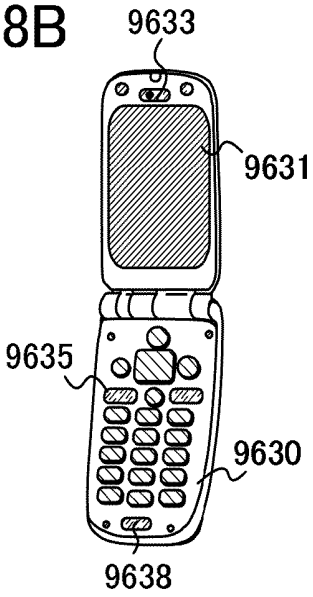


FIG. 18C

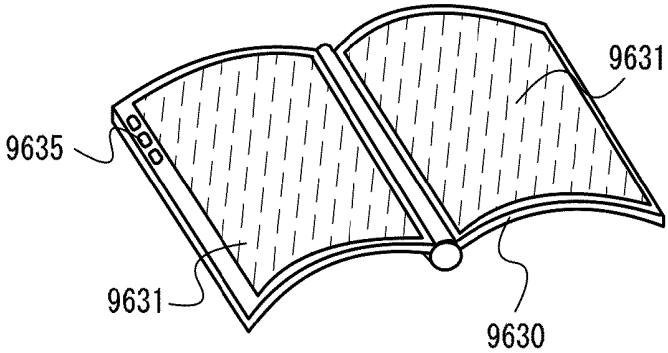
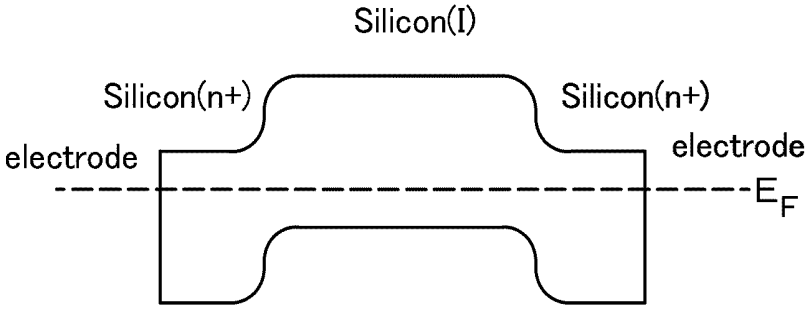


FIG. 19



LIQUID CRYSTAL DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE SAME

TECHNICAL FIELD

One embodiment of the present invention relates to a semiconductor device including a field-effect transistor using an oxide semiconductor.

In this specification, a semiconductor device means all types of devices which can function by utilizing semiconductor characteristics, and an electro-optical device such as a liquid crystal display device, a semiconductor circuit, and an electronic device are all semiconductor devices.

BACKGROUND ART

A technique for forming thin film transistors using a semiconductor thin film formed over a substrate having an insulating surface has attracted attention. The thin film transistors are used for display devices typified by liquid crystal televisions. A silicon-based semiconductor material is known as a material for a thin semiconductor film applicable to a thin film transistor. As another material, an oxide semiconductor has attracted attention.

As a material for the oxide semiconductor, zinc oxide and a material containing zinc oxide as its component are known. Further, a thin film transistor formed using an amorphous oxide (oxide semiconductor) having an electron carrier concentration of less than $10^{18}/cm^3$ is disclosed (Patent Documents 1 to 3).

REFERENCE

Patent Document

[Patent Document 1] Japanese Published Patent Application No. 2006-165527

[Patent Document 2] Japanese Published Patent Application No. 2006-165528

[Patent Document 3] Japanese Published Patent Application No. 2006-165529

DISCLOSURE OF INVENTION

However, a difference from a stoichiometric composition of an oxide semiconductor film occurs in the formation process, which becomes a problem in some cases. For example, in the case where oxygen in a film is excess or deficient, or the case where hydrogen contained as an impurity becomes an electron donor, electrical conductivity changes.

Even when having an electron carrier concentration of less than $10^{18}/cm^3$, an oxide semiconductor is a substantially n-type oxide semiconductor, and an on-off ratio of the thin film transistor disclosed in the Patent Documents is only about 10^3. Such a low on-off ratio of the thin film transistor is due to large off-current.

It is an object of one embodiment of the present invention to provide a display device including a thin film transistor having stable electric characteristics (e.g., an off-current is extremely reduced).

One embodiment of the present invention is a liquid crystal display device including a thin film transistor in which a channel region is formed using an oxide semiconductor which is an intrinsic or substantially intrinsic semiconductor obtained by removal of impurities serving as

electron donors (donors) in the oxide semiconductor and which has a larger energy gap than a silicon semiconductor.

That is, one embodiment of the present invention is a liquid crystal display device including a thin film transistor in which a channel region is formed using an oxide semiconductor film. Hydrogen or an OH bond contained in the oxide semiconductor is extremely reduced so that hydrogen is contained at $5\times10^{19}/cm^3$ or less, preferably $5\times10^{18}/cm^3$ or less, more preferably $5\times10^{17}/cm^3$ or less in the oxide semiconductor, and the carrier concentration of the oxide semiconductor film is set to $5\times10^{14}/cm^3$ or less, preferably $5\times10^{12}/cm^3$ or less.

The energy gap of the oxide semiconductor is 2 eV or more, preferably 2.5 eV or more, more preferably 3 eV or more and an impurity such as hydrogen which forms a donor is extremely reduced so that the carrier concentration is $1\times10^{14}/cm^3$ or less, preferably $1\times10^{12}/cm^3$ or less.

When such a highly purified oxide semiconductor is used for a channel formation region of a thin film transistor, even in the case where the channel width is 10 mm and the drain voltage is 10 V, the oxide semiconductor operates so that the drain current is 1×10^{-13}A or less at a gate voltage of −5 V to 20 V.

One embodiment of the present invention disclosed in this specification is a liquid crystal display device. In the liquid crystal display device, a thin film transistor including a gate electrode, a gate insulating layer which is provided so as to overlap the gate electrode, an oxide semiconductor layer which is provided so as to overlap the gate electrode with the gate insulating layer interposed therebetween, and a source electrode and a drain electrode which are provided so as to overlap part of the oxide semiconductor layer is provided between a signal line and a pixel electrode which are provided in a pixel portion. An auxiliary capacitor which is electrically connected to the pixel electrode is not formed.

Another embodiment of the present invention disclosed in this specification is a liquid crystal display device. In the liquid crystal display device, a thin film transistor includes a gate electrode, a gate insulating layer which is provided so as to overlap the gate electrode, an oxide semiconductor layer which is provided so as to overlap the gate electrode with the gate insulating layer interposed therebetween, and a source electrode and a drain electrode which are provided so as to overlap part of the oxide semiconductor layer. The thin film transistor is provided between a signal line and a pixel electrode which are each provided in a plurality of subpixels in one pixel. An auxiliary capacitor which is electrically connected to the pixel electrode is not formed.

Note that an auxiliary capacitor refers to a capacitor which is intentionally provided, and parasitic capacitance which is not intentionally provided may be formed.

According to one embodiment of the present invention, a capacitor to hold a signal voltage applied to a pixel is not necessarily provided because the off-current is reduced to 1×10^{-13} A or less. That is, since an auxiliary capacitor is not necessarily provided in each pixel, the aperture ratio can be improved. In addition, a pixel using a thin film transistor according to one embodiment of the present invention can be kept in a certain state (a state where a video signal is written) and thus stable operation can be performed even in the case where a still image is displayed.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. **1**A and **1**B are a top view and a cross-sectional view of a liquid crystal display device.

FIGS. **2**A and **2**B are a top view and a cross-sectional view of a liquid crystal display device.

FIGS. **3**A to **3**D are cross-sectional views illustrating a method for manufacturing a liquid crystal display device.

FIG. **4** shows Vg-Id characteristics of a thin film transistor in which an oxide semiconductor is used.

FIGS. **5**A and **5**B are photographs of a thin film transistor in which an oxide semiconductor is used.

FIGS. **6**A and **6**B show Vg-Id characteristics (temperature characteristics) of a thin film transistor in which an oxide semiconductor is used.

FIG. **7** illustrates a liquid crystal display device.

FIG. **8** is a longitudinal sectional view of a thin film transistor having an inverted staggered structure in which an oxide semiconductor is used.

FIGS. **9**A and **9**B are energy band diagrams (schematic diagrams) along an A-A' section illustrated in FIG. **8**.

FIGS. **10**A and **10**B are energy band diagrams (schematic diagrams) along a B-B' section illustrated in FIG. **8**; FIG. **10**A illustrates a state in which a positive voltage ($+V_G$) is applied to a gate (G**1**) and FIG. **10**B illustrates a state in which a negative voltage ($-V_G$) is applied to the gate (G**1**).

FIG. **11** shows a relation between the vacuum level and the work function of a metal (ϕ_M) and a relation between the vacuum level and the electron affinity (χ) of an oxide semiconductor.

FIGS. **12**A and **12**B each illustrate a liquid crystal display device.

FIGS. **13**A and **13**B each illustrate a liquid crystal display device.

FIGS. **14**A and **14**B illustrate a liquid crystal display device.

FIGS. **15**A and **15**B each illustrate a liquid crystal display device.

FIGS. **16**A and **16**B each illustrate a liquid crystal display device.

FIGS. **17**A to **17**C each illustrate an electronic device.

FIGS. **18**A to **18**C each illustrate an electronic device.

FIG. **19** illustrates a band structure between a source and a drain of a silicon MOS transistor.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will be described in detail with reference to the accompanying drawings. The present invention is not limited to the following description, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not to be construed as being limited to the content of the embodiments included herein. Note that in the structures of the present invention described below, the same reference numerals are used for the same portions and portions having similar functions in different drawings, and the description thereof is not repeated.

Note that the size, the thickness of a layer, or a region of each structure illustrated in drawings in this specification is exaggerated for simplicity in some cases. Therefore, embodiments of the present invention are not limited to such scales.

Note that the terms such as "first", "second", and "third" used in this specification are used in order to avoid confusion of structural elements and do not mean limitation of the number of the structural elements. Therefore, for example, the term "first" can be replaced with the term "second", "third", or the like as appropriate.

Embodiment 1

An example is described below in which a pixel of a liquid crystal display device is formed using a thin film transistor according to one embodiment of the present invention. In this embodiment, in a liquid crystal display device, a thin film transistor included in a pixel and an electrode (also referred to as a pixel electrode) connected to the thin film transistor will be shown and described as an example. Note that a pixel includes elements provided in each pixel of a display device, for example, a thin film transistor, an electrode functioning as a pixel electrode, a wiring for supplying an electric signal to the element, and the like. Note that a pixel may include a color filter or the like. For example, in a color display device including color elements of R, G, and B, a minimum unit of an image is composed of three pixels of an R pixel, a G pixel, and a B pixel.

Note that when it is described that "A and B are connected", the case where A and B are electrically connected to each other, and the case where A and B are directly connected to each other are included therein. Here, A and B are each an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, a layer, or the like).

A storage capacitance is a combination of a capacitance of a liquid crystal element and a capacitance of a capacitor which is provided separately. The former is referred to as a liquid crystal capacitance and the latter is referred to as an auxiliary capacitance for distinction.

First, as an example of a pixel portion in a conventional liquid crystal display device, a top view is illustrated in FIG. **2**A. A thin film transistor illustrated in FIG. **2**A has a kind of bottom-gate structure called an inverted staggered structure in which a wiring layer serving as a source electrode and a drain electrode is provided over an oxide semiconductor layer overlapped with a gate electrode.

A pixel portion illustrated in FIG. **2**A includes a first wiring **2101** functioning as a scan line, a second wiring **2102**A functioning as a signal line, an oxide semiconductor layer **2103**, a capacitor line **2104**, and a pixel electrode **2105**. Moreover, the pixel portion in FIG. **2**A includes a third wiring **2102**B for electrically connecting the oxide semiconductor layer **2103** and the pixel electrode **2105**.

The first wiring **2101** also functions as a gate electrode of a thin film transistor **2106**.

The second wiring **2102**A also functions as one of a source electrode and a drain electrode of the thin film transistor **2106** and one electrode of a capacitor.

The third wiring **2102**B also functions as the other of the source electrode and the drain electrode of the thin film transistor **2106**.

The capacitor line **2104** functions as the other electrode of the capacitor. Note that the first wiring **2101** and the capacitor line **2104** are formed in the same layer, and the second wiring **2102**A and the third wiring **2102**B are formed in the same layer. In addition, the third wiring **2102**B and the capacitor line **2104** partly overlap with each other to form an auxiliary capacitor (a capacitor) of a liquid crystal element. The oxide semiconductor layer **2103** included in the thin film transistor **2106** is provided over the first wiring **2101** with a gate insulating film **2113** (not illustrated) therebetween.

FIG. **2**B illustrates a cross-sectional structure along chain line A**1**-A**2** in FIG. **2**A.

In the cross-sectional structure illustrated in FIG. **2**B, the first wiring **2101** serving as the gate electrode and the capacitor line **2104** are provided over a substrate **2111** with a base film **2112** therebetween. The gate insulating film **2113** is provided so as to cover the first wiring **2101** and the capacitor line **2104**. The oxide semiconductor layer **2103** is provided over the gate insulating film **2113**. Further, the second wiring **2102**A and the third wiring **2102**B are provided over the oxide semiconductor layer **2103**, and an oxide insulating layer **2114** functioning as a passivation film is provided thereover. An opening portion is formed in the oxide insulating layer **2114**. The pixel electrode **2105** and the third wiring **2102**B are connected to each other in the opening portion. A capacitor is formed by the third wiring **2102**B and the capacitor line **2104**, using the gate insulating film **2113** as a dielectric.

Note that the pixel illustrated in FIGS. **2**A and **2**B corresponds to one of a plurality of pixels **701** arranged in a matrix over a substrate **700** as illustrated in FIG. **7**. FIG. **7** illustrates a structure in which a pixel portion **702**, a scan line driver circuit **703**, and a signal line driver circuit **704** are placed over the substrate **700**. Whether the pixels **701** are in a selected state or in a non-selected state is determined per row in accordance with a scan signal supplied from the first wiring **101** connected to the scan line driver circuit **703**. The pixel **701** selected by the scan signal is supplied with a video voltage (also referred to as an image signal, a video signal, or video data) from the wiring **2102**A connected to the signal line driver circuit **704**.

FIG. **7** illustrates the structure in which the scan line driver circuit **703** and the signal line driver circuit **704** are provided over the substrate **700**; alternatively, one of the scan line driver circuit **703** and the signal line driver circuit **704** may be provided over the substrate **700**. Only the pixel portion **702** may be provided over the substrate **700**.

FIG. **7** illustrates an example in which the plurality of pixels **701** is arranged in a matrix (in stripe) in the pixel portion **702**. Note that the pixels **701** are not necessarily arranged in a matrix and may be arranged in a delta pattern or Bayer arrangement. As a display method of the pixel portion **702**, a progressive method or an interlace method can be employed. Note that color elements controlled in the pixel for color display are not limited to three colors of R (red), G (green), and B (blue), and for example, RGBW (W corresponds to white), or RGB added with one or more of yellow, cyan, magenta, and the like may be employed. Further, the size of display regions may be different between dots of color elements.

In FIG. **7**, the first wirings **2101** and the second wirings **2102**A are formed in accordance with the number of pixels in the row direction and column direction. Note that the numbers of the first wirings **2101** and the second wirings **2102**A may be increased depending on the number of subpixels included in one pixel or the number of transistors in the pixel. The pixels **701** may be driven with the first wiring **2101** and the second wiring **2102**A shared with some pixels.

Note that in FIG. **2**A, the second wiring **2102**A is rectangular; alternatively, the second wiring **2102**A may surround the third wiring **2102**B (specifically, the second wiring **2102**A may be in a U-shape or C-shape) so that the area of a region where carriers move is increased to increase the amount of current flowing.

Note that a thin film transistor is an element having at least three terminals of a gate, a drain, and a source. The thin film transistor has a channel region between a drain region and a source region, and current can flow through the drain region, the channel region, and the source region. Here, since the source and the drain of the transistor may interchange depending on the structure, the operating condition, and the like of the transistor, it is difficult to define which is a source or a drain. Therefore, a region functioning as a source or a drain is not called the source or the drain in some cases. In such a case, for example, one of the source and the drain is referred to as a first terminal, a first electrode, or a first region and the other of the source and the drain is referred to as a second terminal, a second electrode, or a second region in some cases.

Next, an example of a structure of a pixel portion according to one embodiment of the present invention is illustrated in FIGS. **1**A and **1**B. FIG. **1**A illustrates a structure in which a capacitor (an auxiliary capacitor) is omitted from the structure of the pixel portion of the conventional example in FIG. **2**A. Therefore, a capacitor line is not necessary, and the third wiring **102**B does not function as an electrode of the capacitor. The third wiring **102**B serves a wiring connected to only a pixel electrode **105** as the source electrode or the drain electrode, which leads to reduction in area. Thus, the aperture ratio can be significantly increased.

Note that an example of a structure of a pixel portion in which a capacitor is omitted, which is one embodiment of the present invention, can have the same structure (except a capacitor) as the above-described conventional example. Although a transistor having an inverted staggered structure is described as an example, a transistor having another structure such as a bottom contact structure or a top gate structure may be used.

In order to omit a capacitor from a pixel portion as described above, the potential of the pixel needs to be held only by a charged liquid crystal element for a certain period. To realize this, the off-current of a thin film transistor needs to be sufficiently reduced. One example of a manufacturing method of a thin film transistor to achieve these characteristics is described with reference to FIGS. **3**A to **3**D.

A glass substrate can be used as the light-transmitting substrate **111**. A base film **112** is provided over the substrate **111** in order to prevent diffusion of impurities from the substrate **111** or improve adhesion between the substrate **111** and elements provided over the substrate **111**. Note that the base film **112** is not necessarily provided.

Next, a conductive layer is formed over the base film **112**. After that, a first photolithography step is performed so that a resist mask is formed and unnecessary portions are removed by etching, whereby the first wiring **101** is formed. At this time, etching is preferably performed so that edges of the first wiring **101** are tapered. FIG. **3**A is a cross-sectional view at this stage.

The first wiring **101** is preferably formed using a low-resistance conductive material such as aluminum or copper. Since the use of aluminum alone has disadvantages such as low heat resistance and a tendency to be corroded, aluminum is preferably used in combination with a conductive material having heat resistance. As the conductive material having heat resistance, it is possible to use an element selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium; an alloy containing any of these elements as its component; an alloy containing a combination of any of these elements; or a nitride containing any of these elements as its component.

Note that the wirings and the like included in the thin film transistor can be formed by an inkjet method or a printing method. Since the wirings and the like can be manufactured

without using a photomask, a layout of the transistor can be changed easily. Further, it is not necessary to use a resist, so that material cost is reduced and the number of steps can be reduced. In addition, a resist mask and the like can also be formed by an inkjet method or a printing method. Since a resist mask can be formed only over intended portions by an inkjet method or a printing method, cost can be reduced.

A resist mask having regions with a plurality of thicknesses (typically, two kinds of thicknesses) may be formed using a multi-tone mask to form wirings and the like.

Then, an insulating film (hereinafter referred to as a gate insulating film **113**) is formed over the first wiring **101**.

In this embodiment, the gate insulating film **113** is formed using a high-density plasma CVD apparatus in which a microwave (2.45 GHz) is used. Here, a high-density plasma CVD apparatus refers to an apparatus which can realize a plasma density higher than or equal to $1\times10^{11}/cm^3$. For example, plasma is generated by applying a microwave power higher than or equal to 3 kW and lower than or equal to 6 kW so that an insulating film is formed.

A monosilane gas (SiH_4), nitrous oxide (N_2O), and a rare gas are introduced into a chamber as a source gas to generate high-density plasma at a pressure higher than or equal to 10 Pa and lower than or equal to 30 Pa so that an insulating film is formed over a substrate. After that, the supply of a monosilane gas is stopped, and nitrous oxide (N_2O) and a rare gas are introduced without exposure to the air, so that plasma treatment may be performed on a surface of the insulating film. The plasma treatment performed on the surface of the insulating film by introducing nitrous oxide (N_2O) and a rare gas is performed at least after the insulating film is formed. The insulating film formed through the above process procedure has a small thickness, and reliability can be ensured even when it has a thickness less than 100 nm, for example.

In forming the gate insulating film **113**, the flow ratio of a monosilane gas (SiH_4) to nitrous oxide (N_2O) which are introduced into the chamber is in the range of 1:10 to 1:200. In addition, as a rare gas which is introduced into the chamber, helium, argon, krypton, xenon, or the like can be used. In particular, argon, which is inexpensive, is preferably used.

Further, the insulating film formed using the high-density plasma CVD apparatus has excellent step coverage and the thickness thereof can be controlled precisely.

The insulating film formed through the above process procedure is greatly different from the insulating film formed using a conventional parallel plate PCVD apparatus. The etching rate of the insulating film formed through the above process procedure is lower than that of the insulating film formed using the conventional parallel plate PCVD apparatus by 10% or more or 20% or more in the case where the etching rates with the same etchant are compared to each other. Thus, it can be said that the insulating film formed using the high-density plasma CVD apparatus is a dense film.

In this embodiment, a silicon oxynitride film (also referred to as SiO_xN_y, where $x>y>0$) with a thickness of 100 nm formed using the high-density plasma CVD apparatus is used as the gate insulating film **113**.

As another formation method of the gate insulating film **113**, a sputtering method may be employed. It is needless to say that the gate insulating film **113** is not limited to such a silicon oxide film and may be formed with a single-layer structure or a layered structure of another insulating film such as a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or a tantalum oxide film.

Note that before the deposition of an oxide semiconductor, dust attached to a surface of the gate insulating film **113** is preferably removed by reverse sputtering in which argon is used as a sputtering gas. Note that as a sputtering gas, nitrogen, helium, or the like may be used instead of argon. Alternatively, argon to which oxygen, hydrogen, N_2O, Cl_2, CF_4, or the like is added may be used as a sputtering gas.

Next, an oxide semiconductor film is formed over the gate insulating film **113**. The field-effect mobility of a transistor in which an oxide semiconductor is used for a semiconductor layer can be higher than that of a transistor in which amorphous silicon is used for a semiconductor layer. Note that examples of the oxide semiconductor are zinc oxide (ZnO), tin oxide (SnO_2), and the like. Moreover, In, Ga, or the like can be added to ZnO.

For the oxide semiconductor film, a thin film represented by the chemical formula, $InMO_3(ZnO)_m$ ($m>0$) can be used. Note that M denotes one metal element or a plurality of metal elements selected from Ga, Al, Mn, and Co. Specifically, M may be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like.

As the oxide semiconductor film, the following oxide semiconductors can also be used: a four-component metal oxide such as an In—Sn—Ga—Zn—O-based oxide semiconductor; a three-component metal oxide such as an In—Ga—Zn—O-based oxide semiconductor, an In—Sn—Zn—O-based oxide semiconductor, an In—Al—Zn—O-based oxide semiconductor, a Sn—Ga—Zn—O-based oxide semiconductor, an Al—Ga—Zn—O-based oxide semiconductor, and a Sn—Al—Zn—O-based oxide semiconductor; a two-component metal oxide such as an In—Zn—O-based oxide semiconductor, a Sn—Zn—O-based oxide semiconductor, an Al—Zn—O-based oxide semiconductor, a Zn—Mg—O-based oxide semiconductor, a Sn—Mg—O-based oxide semiconductor, an In—Mg—O-based oxide semiconductor, an In—Ga—O-based oxide semiconductor; an In—O-based oxide semiconductor; a Sn—O-based oxide semiconductor; and a Zn—O-based oxide semiconductor. Further, SiO_2 may be contained in the above oxide semiconductor. Here, an In—Ga—Zn—O-based oxide semiconductor means an oxide including indium (In), gallium (Ga), and zinc (Zn), and there is no particular limitation on the stoichiometric proportion. Further, the In—Ga—Zn—O-based oxide semiconductor may contain an element other than In, Ga, and Zn. Furthermore, it is preferable that the energy gap of the oxide semiconductor is 2 eV or more, preferably 2.5 eV or more, more preferably 3 eV or more.

An In—Ga—Zn—O-based film is used as the oxide semiconductor. Here, a target in which In_2O_3, Ga_2O_3, and ZnO are contained at a molar ratio of 1:1:1 or 1:1:2 is used, and deposition is performed by a sputtering method. The oxide semiconductor is deposited under the following conditions: the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct current (DC) power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the proportion of the oxygen flow is 100%). Note that a pulsed direct current (DC) power supply is preferably used because powder substances (also referred to as particles or dust) generated in film deposition can be reduced and the film thickness can be uniform.

In this case, the oxide semiconductor film is preferably formed while remaining moisture in the treatment chamber is removed, in order to prevent hydrogen, hydroxyl group, or moisture from being contained in the oxide semiconductor film.

In order to remove remaining moisture in the treatment chamber, an entrapment vacuum pump is preferably used.

For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. The evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide semiconductor film formed in the deposition chamber can be reduced.

Next, a second photolithography step is performed so that a resist mask is formed and unnecessary portions are removed by etching, whereby the oxide semiconductor layer **103** is formed. The first heat treatment for the oxide semiconductor layer may be performed on the oxide semiconductor film that has not yet been processed into the island-shaped oxide semiconductor layer. FIG. **3**B is a cross-sectional view at this stage.

Next, the oxide semiconductor layer is subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400° C. and lower than or equal to 750° C., preferably higher than or equal to 425° C. and lower than or equal to 750° C. Note that the heat treatment may be performed for one hour or shorter when the temperature of the heat treatment is 425° C. or higher; the heat treatment is preferably performed for one hour or longer when the temperature is lower than 425° C. Here, the substrate is introduced into an electric furnace, which is one of heat treatment apparatuses, and heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere. Then, the oxide semiconductor layer is not exposed to air, and a high-purity oxygen gas, a high-purity N_2O gas, or an ultra-dry air (having a dew point of lower than or equal to −40° C., preferably lower than or equal to −60° C.) is introduced into the same furnace and cooling is performed. At this time, it is preferable that water, hydrogen, and the like be not contained in the gas introduced. Alternatively, the purity of the gas which is introduced into the heat treatment apparatus is preferably 6N (99.9999%) or more preferably 7N (99.99999%) or more (that is, the impurity concentration in the gas is 1 ppm or less, or preferably 0.1 ppm or less).

Note that in this specification, heat treatment in the atmosphere of an inert gas such as nitrogen or a rare gas is referred to as heat treatment for dehydration or dehydrogenation. In this specification, dehydrogenation does not indicate elimination of only H_2 by heat treatment. For convenience, elimination of H, OH, and the like is called dehydration or dehydrogenation.

The heat treatment apparatus is not limited to an electric furnace. For example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. Further, the LRTA apparatus may have not only a lamp but also a device for heating an object to be processed by heat conduction or heat radiation from a heater such as a resistance heater. GRTA is a method of heat treatment using a high-temperature gas. As the gas, an inert gas that hardly reacts with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used. The heat treatment may be performed using such an RTA method at higher than or equal to 600° C. and lower than or equal to 750° C. for several minutes.

Further, after the first heat treatment for dehydration or dehydrogenation, heat treatment may be performed at 200° C. to 400° C. inclusive, preferably 200° C. to 300° C. inclusive, in an atmosphere of an oxygen gas or an N_2O gas.

When the oxide semiconductor layer is subjected to heat treatment at 400° C. to 750° C. inclusive, the dehydration or dehydrogenation of the oxide semiconductor layer can be achieved; thus, water (H_2O) can be prevented from being contained again in the oxide semiconductor layer later. At the same time of the dehydration or dehydrogenation, an i-type oxide semiconductor layer is changed into an oxygen-deficient oxide semiconductor layer, i.e., an n-type (e.g., n^--type and n^+-type) oxide semiconductor layer. When an oxide insulating film which is in contact with the n-type oxide semiconductor layer is formed, the oxide semiconductor layer is brought into an oxygen-excess state. Accordingly, the oxide semiconductor layer becomes an i-type oxide semiconductor layer again so as to have high resistance. The threshold voltage of the transistor using such an oxide semiconductor layer is positive, so that the transistor shows so-called normally-off characteristics. It is preferable for a transistor used in a semiconductor device such as a display device that the gate voltage be a positive threshold voltage that is as close to 0 V as possible. In an active matrix display device, electric characteristics of a transistor included in a circuit are important and the performance of the display device depends on the electrical characteristics. In particular, the threshold voltage of the transistor is important. If the threshold voltage of the transistor is negative, the transistor has so-called normally-on characteristics, that is, current flows between a source electrode and a drain electrode even when the gate voltage is 0 V, so that it is difficult to control the circuit formed using the transistor. In the case of a transistor where the threshold voltage is positive but an absolute value of the threshold voltage is large, the transistor cannot perform a switching operation in some cases because driving voltage is not high enough. In the case of an n-channel transistor, it is preferable that a channel be formed and drain current begin to flow after a positive gate voltage is applied. A transistor in which a channel is not formed unless driving voltage is raised and a transistor in which a channel is formed and drain current flows even when a negative voltage is applied are unsuitable for a transistor used in a circuit.

In the first heat treatment, water, hydrogen, and the like are not preferably contained in nitrogen or a rare gas such as helium, neon, or argon. It is preferable that the purity of nitrogen or the rare gas such as helium, neon, or argon which is introduced into a heat treatment apparatus be set to be 6N (99.9999%) or higher, preferably 7N (99.99999%) or higher.

Here, the oxide semiconductor that is made to be an intrinsic oxide semiconductor or a substantially intrinsic oxide semiconductor (the oxide semiconductor that is highly purified) by removal of impurities such as hydrogen is extremely sensitive to an interface state and an interface electric charge; thus, an interface between the oxide semiconductor and the gate insulating film is important. Therefore, the gate insulating film (GI) that is in contact with the highly-purified oxide semiconductor needs to have higher quality.

For example, by the above-described high-density plasma CVD method using a microwave (2.45 GHz), an insulating film which is dense, has high withstand voltage, and has high quality can be formed. The highly-purified oxide semiconductor and the high-quality gate insulating film are in close contact with each other, whereby the interface state density can be reduced to obtain favorable interface characteristics.

Needless to say, another film formation method such as a sputtering method or a plasma CVD method can be employed as long as the method enables formation of a good-quality insulating film as a gate insulating film. Further, an insulating film whose film quality and characteristic of an interface between the insulating film and an oxide semiconductor are improved by heat treatment which is performed after formation of the insulating film may be formed as a gate insulating film. In any case, any insulating film may be used as long as the insulating film has characteristics of enabling reduction in interface state density of an interface between the insulating film and an oxide semiconductor and formation of a favorable interface as well as having favorable film quality as a gate insulating film.

Further, when an oxide semiconductor containing many impurities is subjected to a gate bias-temperature stress test (BT test) for 12 hours under conditions that the temperature is 85° C. and the voltage applied to the gate is 2×10^6 V/cm, a bond between the impurity and a main component of the oxide semiconductor is cleaved by a high electric field (B: bias) and a high temperature (T: temperature), and a generated dangling bond induces drift of threshold voltage (V_{th}). In contrast, the present invention makes it possible to obtain a thin film transistor which is stable to a BT test by removal of impurities in an oxide semiconductor, especially hydrogen, water, and the like as much as possible to obtain a favorable characteristic of an interface between the oxide semiconductor film and a gate insulating film as described above.

Then, a conductive film is formed from a metal material over the oxide semiconductor film by a sputtering method or a vacuum evaporation method. Examples of a material for the conductive film are an element selected from aluminum, chromium, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of the above elements as its component; and an alloy containing a combination of any of the above elements. Further, in the case where heat treatment is performed at 200° C. to 600° C. inclusive, the conductive film preferably has sufficient heat resistance to withstand heat treatment performed in this temperature range. Since the use of Al alone brings disadvantages such as low heat resistance and a tendency to be corroded, aluminum is used in combination with a conductive material having heat resistance. As such a conductive material having heat resistance, any of the following materials can be used: an element selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium; an alloy containing any of these above elements as its component; an alloy containing a combination of any of these elements; and a nitride containing any of these elements as its component.

Here, the conductive film has a single-layer structure of a titanium film. The conductive film may have a two-layer structure, and a titanium film may be stacked over an aluminum film. Alternatively, the conductive film may have a three-layer structure in which a titanium film, an aluminum film containing neodymium (an Al—Nd film), and a titanium film are stacked in this order. Further alternatively, the conductive film may have a single-layer structure of an aluminum film containing silicon.

Next, a third photolithography step is performed so that a resist mask is formed and unnecessary portions are removed by etching, whereby the second wiring **102**A and the third wiring **102**B made of the conductive film are formed. Wet etching or dry etching is employed as an etching method at this time. For example, when a conductive film of titanium is etched with wet etching using an ammonia peroxide mixture (hydrogen peroxide water at 31 wt %:ammonia water at 28 wt %:water=5:2:2), the oxide semiconductor layer **103** can be left while the second wiring **102**A and the third wiring **102**B are selectively etched. FIG. **3**C is a cross-sectional view at this stage.

An exposed region of the oxide semiconductor layer is sometimes etched in the third photolithography step depending on the etching conditions. In this case, the thickness of the oxide semiconductor layer **103** in a region between the second wiring **102**A and the third wiring **102**B is smaller than that of the oxide semiconductor layer over the first wiring **101** in a region overlapping the second wiring **102**A or the third wiring **102**B.

Then, the oxide insulating layer **114** is formed over the gate insulating film **113**, the oxide semiconductor layer **103**, the second wiring **102**A, and the third wiring **102**B. At this stage, part of the oxide semiconductor layer **103** is in contact with the oxide insulating layer **114**.

The oxide insulating layer **114** can be formed to a thickness of at least 1 nm by a method with which impurities such as water and hydrogen are not mixed into the oxide insulating layer as appropriate. In this embodiment, a silicon oxide film is formed by a sputtering method as the oxide insulating layer. The substrate temperature in film deposition is higher than or equal to room temperature and lower than or equal to 300° C., and is 100° C. in this embodiment. The silicon oxide film can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas (typically, argon) and oxygen. As a target for deposition, a silicon oxide target or a silicon target can be used. For example, with the use of a silicon target, a silicon oxide film can be formed by a sputtering method in an atmosphere of oxygen and a rare gas. As the oxide insulating layer which is formed in contact with the oxide semiconductor layer which is changed into an oxygen-deficient type and has low resistance, an inorganic insulating film that does not include impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of these impurities from the outside is used. Specifically, a silicon oxide film, a silicon nitride oxide film, an aluminum oxide film, or an aluminum oxynitride film is used. Note that a target for deposition which is doped with phosphorus (P) or boron (B) is used, so that an oxide insulating layer to which phosphorus (P) or boron (B) is added can be formed.

In this embodiment, the oxide insulating layer **114** is formed by a pulsed DC sputtering method using a columnar polycrystalline silicon target doped with boron that has a purity of 6N and a resistivity of 0.01 Ωcm in the following conditions: the distance between the substrate and the target (T-S distance) is 89 mm, the pressure is 0.4 Pa, the direct-current (DC) power is 6 kW, and the atmosphere is an oxygen atmosphere (the oxygen flow rate is 100%). The thickness thereof is 300 nm.

Note that the oxide insulating layer **114** is provided on and in contact with a region serving as the channel formation region of the oxide semiconductor layer and also functions as a channel protective layer.

In this case, the oxide insulating layer **114** is preferably formed while remaining moisture in the treatment chamber is removed, in order to prevent hydrogen, hydroxyl group, or moisture from being contained in the oxide semiconductor layer **103** and the oxide insulating layer **114**.

In order to remove remaining moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. The evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the

cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide insulating layer **114** formed in the deposition chamber can be reduced.

Next, second heat treatment (preferably at 200° C. to 400° C. inclusive, for example, 250° C. to 350° C. inclusive) is performed in an inert gas atmosphere. For example, the second heat treatment is performed at 250° C. for one hour in a nitrogen atmosphere. By the second heat treatment, heat is applied while part of the oxide semiconductor layer **103** is in contact with the oxide insulating layer **114**.

When the second heat treatment is performed while the oxide semiconductor layer **103** which is changed into an oxygen-deficient type at the same time as elimination of hydrogen and the resistance of which is reduced by the first heat treatment is in contact with the oxide insulating layer **114**, a region that is in contact with the oxide insulating layer **114** is brought into an oxygen-excess state. Thus, the oxide semiconductor layer **103** is changed into a high-resistance (i-type) oxide semiconductor layer in the depth direction from the region that is in contact with the oxide insulating layer **114**.

Further, the heat treatment may be performed at 100° C. to 200° C. inclusive for one hour to 30 hours inclusive in the air. For example, the heat treatment is performed at 150° C. for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature of 100° C. to 200° C. inclusive and then decreased to room temperature. Further, this heat treatment may be performed before formation of the oxide insulating film under a reduced pressure. Under the reduced pressure, the heat treatment time can be shortened. With such heat treatment, hydrogen is introduced from the oxide semiconductor layer to the oxide insulating layer; thus, a normally-off thin film transistor can be obtained. Therefore, reliability of the semiconductor device can be improved.

Then, an opening portion **121** is formed in the oxide insulating layer **114** through a fourth photolithography step and an etching step, and a light-transmitting conductive film is formed. The light-transmitting conductive film is formed using indium oxide (In_2O_3), indium tin oxide (In_2O_3—SnO_2, hereinafter abbreviated as ITO), or the like by a sputtering method, a vacuum evaporation method, or the like. Alternatively, an Al—Zn—O-based film containing nitrogen, that is, an Al—Zn—O—N-based film, a Zn—O-based film containing nitrogen, or a Sn—Zn—O-based film containing nitrogen may be used. Note that the composition ratio (atomic %) of zinc in the Al—Zn—O—N-based film is less than or equal to 47 atomic % and is higher than that of aluminum in the film; the composition ratio (atomic %) of aluminum in the film is higher than that of nitrogen in the film. Such a material is etched with a hydrochloric acid-based solution. However, since a residue is easily generated particularly in etching ITO, indium zinc oxide (In_2O_3—ZnO) may be used to improve etching processability.

Note that the unit of the percentage of components in the light-transmitting conductive film is atomic percent (atomic %), and the percentage of components is evaluated by analysis using an electron probe X-ray microanalyzer (EPMA).

Next, a fifth photolithography step is performed so that a resist mask is formed and unnecessary portions are removed by etching, thereby forming the pixel electrode **105**. FIG. **3**D is a cross-sectional view at this stage.

In such a manner, the pixel including the thin film transistor **106** with low off-current can be manufactured. Moreover, the pixels are arranged in a matrix to form a pixel portion, whereby one of substrates for manufacturing an active-matrix liquid crystal display device can be obtained. In this specification, such a substrate is referred to as an active-matrix substrate for convenience.

Note that in an active-matrix liquid crystal display device, pixel electrodes arranged in a matrix are driven so that a display pattern is formed on a screen. Specifically, voltage is applied between a selected pixel electrode and a counter electrode corresponding to the pixel electrode, so that a liquid crystal layer provided between the pixel electrode and the counter electrode is optically modulated and this optical modulation is recognized as a display pattern by an observer. A display element such as a liquid crystal element is provided over the pixel electrode **105**.

As described above, the structure described in this embodiment, in which a capacitor is omitted, makes it possible to increase the aperture ratio of a pixel including a thin film transistor in which an oxide semiconductor is used. Thus, a liquid crystal display device can include a high definition display portion.

This embodiment can be implemented in combination with any of the structures described in the other embodiments as appropriate.

Embodiment 2

According to one embodiment of the present invention, impurities to be donors (or acceptors) of carriers in an oxide semiconductor are reduced to a very low level, whereby the oxide semiconductor is made to be intrinsic or substantially intrinsic, and the oxide semiconductor is used for a thin film transistor. In this embodiment, measured values of off-current using a test element group (also referred to as a TEG) will be described below.

FIG. **4** shows initial characteristics of a thin film transistor with L/W=3 μm/10000 μm in which 200 thin film transistors each with L/W=3 μm/50 μm are connected in parallel. In addition, a top view is shown in FIG. **5**A and a partially enlarged top view thereof is show in FIG. **5**B. The region enclosed by a dotted line in FIG. **5**B is a thin film transistor of one stage with L/W=3 μm/50 μm and Lov=1.5 μm. In order to measure initial characteristics of the thin film transistor, the changing characteristics of the source-drain current (hereinafter referred to as a drain current or Id), i.e., Vg-Id characteristics, were measured, under the conditions where the substrate temperature was set to room temperature, the voltage between source and drain (hereinafter, a drain voltage or Vd) was set to 10 V, and the voltage between source and gate (hereinafter, a gate voltage or Vg) was changed from −20 V to +20 V. Note that FIG. **4** shows Vg in the range of from −20 V to +5 V.

As shown in FIG. **4**, the thin film transistor having a channel width W of 10000 μm has an off-current of 1×10^{-13} A or less at Vd of 1 V and 10 V, which is less than or equal to the resolution (100 fA) of a measurement device (a semiconductor parameter analyzer, Agilent 4156C manufactured by Agilent Technologies Inc.).

A method for manufacturing the thin film transistor used for the measurement is described.

First, a silicon nitride film was formed as a base layer over a glass substrate by a CVD method, and a silicon oxynitride film was formed over the silicon nitride film. A tungsten

layer was formed as a gate electrode layer over the silicon oxynitride film by a sputtering method. Here, the gate electrode layer was formed by selectively etching the tungsten layer.

Then, a silicon oxynitride film having a thickness of 100 nm was formed as a gate insulating layer over the gate electrode layer by a CVD method.

Then, an oxide semiconductor film having a thickness of 50 nm was formed over the gate insulating layer by a sputtering method using an In—Ga—Zn—O-based metal oxide target (at a molar ratio of In_2O_3:Ga_2O_3:ZnO=1:1:2). Here, an island-shaped oxide semiconductor layer was formed by selectively etching the oxide semiconductor film.

Then, first heat treatment was performed on the oxide semiconductor layer in a nitrogen atmosphere in a clean oven at 450° C. for 1 hour.

Then, a titanium layer (having a thickness of 150 nm) was formed as a source electrode layer and a drain electrode layer over the oxide semiconductor layer by a sputtering method. Here, the source electrode layer and the drain electrode layer were formed by selectively etching the titanium layer such that 200 thin film transistors each having a channel length L of 3 μm and a channel width W of 50 μm were connected in parallel to obtain a thin film transistor with L/W=3 μm/10000 μm.

Then, a silicon oxide film having a thickness of 300 nm was formed as a protective insulating layer in contact with the oxide semiconductor layer by a reactive sputtering method. Opening portions were formed over the gate electrode layer, the source electrode layer, and the drain electrode layer by selectively etching the silicon oxide film. After that, second heat treatment was performed in a nitrogen atmosphere at 250° C. for 1 hour.

Then, heat treatment was performed at 150° C. for 10 hours before the measurement of Vg-Id characteristics.

Through the above process, a bottom-gate thin film transistor was manufactured.

The reason why the off-current of the thin film transistor is approximately 1×10^{-13} A as shown in FIG. **4** is that the concentration of hydrogen in the oxide semiconductor layer could be sufficiently reduced in the above manufacturing process. The concentration of hydrogen in the oxide semiconductor layer is 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, more preferably 5×10^{17} atoms/cm^3 or less. Note that the concentration of hydrogen in the oxide semiconductor layer was measured by secondary ion mass spectrometry (SIMS).

Although the example of using an In—Ga—Zn—O-based oxide semiconductor is described, this embodiment is not particularly limited thereto. As another oxide semiconductor material, a four-component metal oxide film such as an In—Sn—Ga—Zn—O film; a three-component metal oxide film such as an In—Ga—Zn—O film, an In—Sn—Zn—O film, an In—Al—Zn—O film, a Sn—Ga—Zn—O film, an Al—Ga—Zn—O film, or a Sn—Al—Zn—O film; or a two-component metal oxide film such as an In—Zn—O film, a Sn—Zn—O film, an Al—Zn—O film, a Zn—Mg—O film, a Sn—Mg—O film, or an In—Mg—O film; an In—O film, a Sn—O film, or a Zn—O film can be used for the oxide semiconductor film. Furthermore, as an oxide semiconductor material, an In—Al—Zn—O-based oxide semiconductor mixed with AlO_x of 2.5 wt % to 10 wt % or an In—Zn—O-based oxide semiconductor mixed with SiO_x of 2.5 wt % to 10 wt % can be used.

The carrier concentration of the oxide semiconductor layer which is measured by a carrier measurement device is preferably less than or equal to 1.45×10^{10}/cm^3, which is intrinsic carrier concentration of silicon. Specifically, the carrier concentration is 5×10^{14}/cm^3 or less, preferably 5×10^{12}/cm^3 or less. In other words, the carrier concentration of the oxide semiconductor layer can be made as close to zero as possible.

The thin film transistor can also have a channel length L of 10 nm to 1000 nm inclusive, which enables an increase in circuit operation speed, and the off-current is extremely small, which enables a further reduction in power consumption.

In addition, in circuit design, the oxide semiconductor layer can be regarded as an insulator when the thin film transistor is in an off state.

After that, the temperature characteristics of off-current of the thin film transistor manufactured in this embodiment were evaluated. Temperature characteristics are important in considering the environmental resistance, maintenance of performance, or the like of an end product in which the thin film transistor is used. It is to be understood that a smaller amount of change is more preferable, which increases the degree of freedom for product designing.

For the temperature characteristics, the Vg-Id characteristics were obtained using a constant-temperature chamber under the conditions where substrates provided with thin film transistors were kept at respective constant temperatures of −30° C., 0° C., 25° C., 40° C., 60° C., 80° C., 100° C., and 120° C., the drain voltage was set to 6 V, and the gate voltage was changed from −20 V to +20V.

FIG. **6**A shows Vg-Id characteristics measured at the above temperatures and superimposed on one another, and FIG. **6**B shows an enlarged view of a range of off-current enclosed by a dotted line in FIG. **6**A. The rightmost curve indicated by an arrow in the diagram is a curve obtained at −30° C.; the leftmost curve is a curve obtained at 120° C.; and curves obtained at the other temperatures are located therebetween. The temperature dependence of on-currents can hardly be observed. On the other hand, as clearly shown also in the enlarged view of FIG. **6**B, the off-currents are less than or equal to 1×10^{-12} A, which is near the resolution of the measurement device, at all temperatures except in the vicinity of a gate voltage of 20 V, and the temperature dependence thereof is not observed. In other words, even at a high temperature of 120° C., the off-current is kept less than or equal to 1×10^{-12} A, and given that the channel width W is 10000 μm, it can be seen that the off-current is significantly small.

A thin film transistor including a purified oxide semiconductor (purified OS) shows almost no dependence of off-current on temperature. It can be said that an oxide semiconductor does not show temperature dependence when purified because the conductivity type becomes extremely close to an intrinsic type and the Fermi level is located in the middle of the forbidden band, as illustrated in the energy band diagram of FIG. **9**A. This also results from the fact that the oxide semiconductor has an energy gap of 3 eV or more and includes very few thermally excited carriers. In addition, the source region and the drain region are in a degenerated state, which is also a factor for showing no temperature dependence. The thin film transistor is mainly operated with carriers which are injected from the degenerated source region to the oxide semiconductor, and the above characteristics (independence of off-current on temperature) can be explained by independence of carrier concentration on temperature. Further, this extremely low off-current will be described with reference to energy band diagrams below.

FIG. **8** is a longitudinal sectional view of an inverted staggered thin film transistor in which an oxide semicon-

ductor is used. An oxide semiconductor layer (OS) is provided over a gate electrode (GE1) with a gate insulating film (GI) therebetween, and a source electrode (S) and a drain electrode (D) are provided thereover.

FIGS. **9**A and **9**B are energy band diagrams (schematic diagrams) along an A-A' section illustrated in FIG. **8**. FIG. **9**A shows a case where the source and the drain have voltage of the same potential (V_D=0 V). FIG. **9**B shows a case where positive potential is applied to the drain (V_D>0 V) whereas positive potential is not applied to the source.

FIGS. **10**A and **10**B are energy band diagrams (schematic diagrams) along a B-B' section illustrated in FIG. **8**. FIG. **10**A shows a state where positive potential ($+V_G$) is applied to a gate (G**1**), that is, a case where the thin film transistor is in an on state where carriers (electrons) flow between the source and the drain. FIG. **10**B shows a state where negative potential ($-V_G$) is applied to the gate (G**1**), that is, a case where the thin film transistor is in an off state (where minority carriers do not flow).

FIG. **11** shows relation between the vacuum level and the work function of a metal (ϕ_M) and relation between the vacuum level and the electron affinity (χ) of an oxide semiconductor.

At normal temperature, electrons in the metal degenerate and the Fermi level is positioned in the conduction band. On the other hand, a conventional oxide semiconductor is generally of n-type, and the Fermi level (E_F) in that case is positioned closer to the conduction band and is away from the intrinsic Fermi level (E_i) that is located in the middle of the band gap. Note that it is known that some hydrogen in the oxide semiconductor form a donor and might be a factor that causes an oxide semiconductor to be an n-type oxide semiconductor.

In contrast, the oxide semiconductor according to the present invention is an oxide semiconductor that is made to be an intrinsic (i-type) semiconductor or made to be as close to an intrinsic semiconductor as possible by being highly purified not by addition of an impurity but by removal of hydrogen that is an n-type impurity so that as few impurities, which are not main components of the oxide semiconductor, as possible are contained. In other words, the oxide semiconductor according to the present invention has a feature in that it is made to be an i-type (intrinsic) semiconductor or made to be close thereto by being highly purified by removal of impurities such as hydrogen or water as much as possible. As a result, the Fermi level (E_F) can be at the same level as the intrinsic Fermi level (E_i).

It is said that the electron affinity (χ) of an oxide semiconductor is 4.3 eV in the case where the band gap (Eg) thereof is 3.15 eV. The work function of titanium used for forming the source and drain electrodes is substantially equal to the electron affinity (χ) of the oxide semiconductor. In the case where titanium is used for the source and drain electrodes, the Schottky electron barrier is not formed at an interface between the metal and the oxide semiconductor.

In other words, an energy band diagram (a schematic diagram) like FIG. **9**A is obtained in the case where a metal and an oxide semiconductor are in contact with each other when the work function of the metal (ϕ_M) and the electron affinity (χ) of the oxide semiconductor are substantially equal.

In FIG. **9**B, a black circle (•) represents an electron. When positive potential is applied to the drain, the electron is injected into the oxide semiconductor over the barrier (h) and flows toward the drain. In that case, the height of the barrier (h) changes depending on the gate voltage and the drain voltage. In the case where positive drain voltage is applied, the height of the barrier (h) is smaller than the height of the barrier (h) in FIG. **9**A of the case where no voltage is applied; that is, the height of the barrier (h) is smaller than half of the band gap (Eg).

In this case, as shown in FIG. **9**A, the electron moves along the lowest part of the oxide semiconductor, which is energetically stable, at an interface between the gate insulating film and the highly-purified oxide semiconductor.

In FIG. **9**B, when negative potential (reverse bias) is applied to the gate (G**1**), the number of holes that are minority carriers is substantially zero; thus, the current value becomes a value as close to zero as possible.

For example, even when the thin film transistor has a channel width W of 1×10^4 μm and a channel length of 3 μm, an off-current of 10^{-13} A or less and a subthreshold value (S value) of 0.1 V/dec. (the thickness of the gate insulating film: 100 nm) can be obtained.

FIG. **19** is a band structure of a transistor formed using a silicon semiconductor. The intrinsic carrier concentration of a silicon semiconductor is $1.45\times10^{10}/cm^3$ (300 K) and carriers exist even at room temperature. This means that thermally excited carriers exist even at room temperature. A silicon wafer to which an impurity such as phosphorus or boron is added is used practically. Therefore, in practice, $1\times10^{14}/cm^3$ or more carriers exist in a silicon semiconductor, and the carriers contribute to conduction between the source and the drain. Furthermore, the band gap of a silicon semiconductor is 1.12 eV, and thus the off-current of a transistor including a silicon semiconductor significantly changes depending on temperature.

Therefore, not by simply using an oxide semiconductor having a wide band gap for a transistor but by highly purifying the oxide semiconductor such that an impurity other than a main component can be prevented from being contained therein as much as possible so that the carrier concentration becomes $1\times10^{14}/cm^3$ or less, preferably $1\times10^{12}/cm^3$ or less, carriers to be thermally excited at a practical operation temperature can be eliminated, and the transistor can operate only with carriers that are injected from the source side. This makes it possible to decrease the off-current to 1×10^{-13} A or less and to obtain a transistor whose off-current hardly changes with a change in temperature and which is capable of extremely stable operation.

In the case where a memory circuit (memory element) or the like is manufactured using a thin film transistor having such an extremely small off-current, there is very little leakage. Therefore, memory data can be stored for a longer period of time. Similarly in a liquid crystal display device and the like, leakage from a storage capacitor through a thin film transistor can be suppressed; therefore, a potential of a pixel can be held only by a liquid crystal capacitor, without an auxiliary capacitor.

This embodiment can be implemented in combination with any of the structures described in the other embodiments as appropriate.

Embodiment 3

In this embodiment, a structure and operation of a pixel that can be applied to a liquid crystal display device will be described.

FIG. **12**A illustrates an example of a pixel configuration that can be applied to a liquid crystal display device. A pixel **3880** includes a transistor **3881**, a liquid crystal element **3882**, and a capacitor **3883**. A gate of the transistor **3881** is electrically connected to a wiring **3885**. A first terminal of the transistor **3881** is electrically connected to a wiring **3884**.

A second terminal of the transistor **3881** is electrically connected to a first terminal of the liquid crystal element **3882**. A second terminal of the liquid crystal element **3882** is electrically connected to a wiring **3887**. A first terminal of the capacitor **3883** is electrically connected to the first terminal of the liquid crystal element **3882**. A second terminal of the capacitor **3883** is electrically connected to a wiring **3886**.

The wiring **3884** can function as a signal line. The signal line is a wiring for transmitting a signal voltage, which is input from the outside of the pixel, to the pixel **3880**. The wiring **3885** can function as a scan line. The scan line is a wiring for controlling on/off of the transistor **3881**. The wiring **3886** can function as a capacitor line. The capacitor line is a wiring for applying a predetermined voltage to the second terminal of the capacitor **3883**. The transistor **3881** can function as a switch. The capacitor **3883** can function as an auxiliary capacitor. The capacitor is an auxiliary capacitor with which the signal voltage continues to be applied to the liquid crystal element **3882** even when the switch is off. The wiring **3887** can function as a counter electrode. The counter electrode is a wiring for applying a predetermined voltage to the second terminal of the liquid crystal element **3882**. Note that a function of each wiring is not limited to the above, and each wiring can have a variety of functions. For example, by changing a voltage applied to the capacitor line, a voltage applied to the liquid crystal element can be adjusted.

FIG. **12**B illustrates another example of a pixel configuration that can be applied to a liquid crystal display device. The example of the pixel configuration in FIG. **12**B is the same as that in FIG. **12**A, except that the wiring **3887** is omitted and the second terminal of the liquid crystal element **3882** and the second terminal of the capacitor **3883** are electrically connected to each other. The example of the pixel configuration in FIG. **12**B can be applied particularly to the case of using a liquid crystal element with a horizontal electric field mode (including an IPS mode and FFS mode). This is because in the horizontal electric field mode liquid crystal element, the second terminal of the liquid crystal element **3882** and the second terminal of the capacitor **3883** can be formed over one substrate, and thus it is easy to electrically connect the second terminal of the liquid crystal element **3882** and the second terminal of the capacitor **3883**. With the pixel configuration in FIG. **12**B, the wiring **3887** can be omitted, whereby a manufacturing process can be simplified and manufacturing cost can be reduced.

Here, a pixel portion including the thin film transistor described in Embodiment 1 is illustrated in FIGS. **13**A and **13**B. FIG. **13**A illustrates a structure in which the capacitor **3883** is omitted from the structure illustrated in FIG. **12**A. In addition, FIG. **13**B is a structure in which the capacitor **3883** is omitted from the structure illustrated in FIG. **12**B, and the second terminal of the liquid crystal element is connected to a common wiring **889**. As described in Embodiment 2, when a thin film transistor with sufficiently low off-current is used, a potential can be held only by a liquid crystal capacitor, without a capacitor (an auxiliary capacitor) which is parallel to a liquid crystal element. Needless to say, a capacitor may be provided similarly to the above-described comparative example, and the size thereof can be reduced. Further, a capacitance of an auxiliary capacitor which is smaller than a capacitance of a liquid crystal element may be formed. In this embodiment, a pixel configuration in which a capacitor is omitted is described below.

FIG. **14**A illustrates a circuit configuration in the case where a plurality of pixels with the structure illustrated in FIG. **13**A is arranged in a matrix. FIG. **14**A is a circuit diagram illustrating four pixels among a plurality of pixels included in the display portion. A pixel placed in an i-th column and a j-th row (i and j are each a natural number) is represented as a pixel **880**_*i,j*, and a wiring **884**_*i* and a wiring **885**_*j* are electrically connected to the pixel **880**_*i, j*. Similarly, a pixel **880**_*i*+1, j is electrically connected to a wiring **884**_*i*+1 and the wiring **885**_*j*. Similarly, a pixel **880**_*i, j*+1 is electrically connected to the wiring **884**_*i* and a wiring **885**_*j*+1. Similarly, a pixel **880**_*i*+1, j+1 is electrically connected to the wiring **884**_*i*+1 and the wiring **885**_*j*+1. Note that each of the wirings can be shared with a plurality of pixels in the same column or the same row. In the pixel configuration in FIG. **14**A, the wiring **887** is a counter electrode. Since the counter electrode is common to all the pixels, the wiring **887** is not indicated by the natural number i or j. Further, since the pixel configuration in FIG. **13**B can also be used, the wiring **887** is not essential even in a structure where the wiring **887** is provided, and the wiring **887** can be omitted when another wiring serves as the wiring **887**, for example.

The pixel configuration in FIG. **14**A can be driven by a variety of methods. In particular, when the pixels are driven by a method called alternating-current driving, degradation (burn-in) of the liquid crystal element can be suppressed. FIG. **14**B is a timing chart of voltages applied to each wiring in the pixel configuration in FIG. **14**A in the case where dot inversion driving which is a kind of alternating-current driving is performed. By the dot inversion driving, flickers seen when the alternating-current driving is performed can be suppressed. Note that FIG. **14**B illustrates a signal **985**_*j* input to the wiring **885**_*j*, a signal **985**_*j*+1 input to the wiring **885**_*j*+1, a signal **984**_*i* input to the wiring **884**_*i*, and a signal **984**_*i*+1 input to the wiring **884**_*i*+1.

In the pixel configuration in FIG. **14**A, a switch in a pixel electrically connected to the wiring **885**_*j* is brought into a selection state (an on state) in a j-th gate selection period in one frame period, and brought into a non-selection state (an off state) in the other periods. Then, a (j+1)-th gate selection period is provided after the j-th gate selection period. By performing sequential scanning in this manner, all the pixels are sequentially selected in one frame period. In the timing chart in FIG. **14**B, the switch in the pixel is brought into a selection state when the voltage is set to high level, and the switch is brought into a non-selection state when the voltage is set to low level.

In the timing chart in FIG. **14**B, in the j-th gate selection period in a k-th frame (k is a natural number), a positive signal voltage is applied to the wiring **884**_*i* used as a signal line, and a negative signal voltage is applied to the wiring **884**_*i*+1. Then, in the (j+1)-th gate selection period in the k-th frame, a negative signal voltage is applied to the wiring **884**_*i*, and a positive signal voltage is applied to the wiring **884**_*i*+1. After that, signals whose polarity is reversed in each gate selection period are alternately supplied to each of the signal lines. Thus, in the k-th frame, the positive signal voltage is applied to the pixel **880***i, j* and the pixel **880**_*i*+1, j+1, and the negative signal voltage is applied to the pixel **880**_*i*+1, j and the pixel **880**_*i, j*+1. Then, in a (k+1)-th frame, a signal voltage whose polarity is opposite to that of the signal voltage written in the k-th frame is written to each pixel. Thus, in the (k+1)-th frame, the positive signal voltage is applied to the pixel **880**_*i*+1, j and the pixel **880**_*i, j*+1, and the negative signal voltage is applied to the pixel **880**_*i, j* and the pixel **880**_*i*+1, j+1. The dot inversion driving is a driving method in which signal voltages whose polarity is different between adjacent pixels are applied in one frame and the polarity of the signal voltage for one pixel is

reversed in each frame as described above. By the dot inversion driving, flickers seen when the entire or part of an image to be displayed is uniform can be reduced while degradation of the liquid crystal element is suppressed. Although only the polarity of the signal voltages for the wirings **884** is shown in the timing chart, the signal voltages can actually have a variety of values in the polarity shown. Here, the case where the polarity is reversed per dot (per pixel) is described; the polarity can be reversed per a plurality of pixels without limitation to the above. For example, when the polarity of signal voltages to be written is reversed per two gate selection periods, power consumed by writing the signal voltages can be reduced. Alternatively, the polarity can be reversed per column (source line inversion) or per row (gate line inversion).

In this case, so-called overdriving may be performed in which an overdrive voltage is applied to the pixel portion and the response speed of the liquid crystal element is increased to suppress blur. Thus, when a moving image is displayed, the movement thereof can be displayed clearly.

Specifically, in the case where a capacitor which is parallel to a liquid crystal element is not provided as in one embodiment of the present invention, there are cases where after writing data to the pixel, dielectric constant is changed in accordance with a change in a state of liquid crystal and a capacitance of the liquid crystal itself is changed, whereby a potential held by the pixel is changed; therefore, overdriving is an effective driving method.

Next, a pixel configuration and a driving method that are preferably used particularly by a liquid crystal element with a vertical alignment (VA) mode typified by an MVA mode or a PVA mode will be described. The VA mode has advantages that a rubbing process is not necessary in manufacturing, the amount of light leakage is small in displaying black images, the level of drive voltage is low, and the like; however, the VA mode has a problem in that the quality of images deteriorates when a screen is viewed from an angle (i.e., the viewing angle is small). In order to increase the viewing angle in the VA mode, a pixel configuration in which one pixel includes a plurality of subpixels as illustrated in FIGS. **15**A and **15**B is effective. Pixel configurations illustrated in FIGS. **15**A and **15**B are examples of the case where a pixel includes two subpixels (a first subpixel **1080-1** and a second subpixel **1080-2**). Note that the number of subpixels in one pixel is not limited to two and can be other numbers. As the number of subpixels becomes larger, the viewing angle can be further increased. A plurality of subpixels can have the same circuit configuration. Here, the case is described in which all the subpixels have the circuit configuration in FIG. **13**A. The first subpixel **1080-1** includes a transistor **1081-1** and a liquid crystal element **1082-1**. The connection relation is the same as that in the circuit configuration in FIG. **13**A. Similarly, the second subpixel **1080-2** includes a transistor **1081-2** and a liquid crystal element **1082-2**. The connection relation is the same as that in the circuit configuration in FIG. **13**A.

The pixel configuration in FIG. **15**A includes, for two subpixels included in one pixel, two wirings **1085** (a wiring **1085-1** and a wiring **1085-2**) used as scan lines and one wiring **1084** used as a signal line. When the signal line is shared with two subpixels in such a manner, the aperture ratio can be increased. Further, a signal line driver circuit can be simplified, so that manufacturing cost can be reduced. Moreover, the number of connections between a liquid crystal panel and a driver circuit IC can be reduced, so that the yield can be increased. The pixel configuration in FIG. **15**B includes, for two subpixels included in one pixel, one wiring **1085** used as a scan line and two wirings **1084** (a wiring **1084-1** and a wiring **1084-2**) used as signal lines. When the scan line is shared with two subpixels in such a manner, the aperture ratio can be increased. Further, the total number of scan lines can be reduced, so that one gate line selection period per pixel can be sufficiently long even in a high-definition liquid crystal panel, and an appropriate signal voltage can be written to each pixel.

FIGS. **16**A and **16**B each schematically illustrate an example of electrical connection of elements in the case where the liquid crystal element in the pixel configuration in FIG. **15**B is replaced with the shape of a pixel electrode. In FIG. **16**A, a first pixel electrode **1088-1** corresponds to a first terminal of the liquid crystal element **1082-1** in FIG. **15**B, and a second pixel electrode **1088-2** corresponds to a first terminal of the liquid crystal element **1082-2** in FIG. **15**B. That is, the first pixel electrode **1088-1** is electrically connected to one of a source and a drain of the transistor **1081-1**, and the second pixel electrode **1088-2** is electrically connected to one of a source and a drain of the transistor **1081-2**. In FIG. **16**B, the connection relation between the pixel electrode and the transistor is opposite to that in FIG. **16**A. That is, the first pixel electrode **1088-1** is electrically connected to one of the source and the drain of the transistor **1081-2**, and the second pixel electrode **1088-2** is electrically connected to one of the source and the drain of the transistor **1081-1**. Although not illustrated, each pixel electrode is connected to a counter electrode through liquid crystal to form a liquid crystal element.

Next, an estimate of how much the aperture ratio of each pixel in a liquid crystal display device is increased by using a thin film transistor including an oxide semiconductor layer according to one embodiment of the present invention is shown.

Parameters for estimating the aperture ratio of a pixel are as follows: the leakage current of the thin film transistor including the oxide semiconductor layer is 1×10^{-13} (A), the panel size is 3.4 inches, the grayscale to be expressed is 256 gray levels, a voltage input is 10 V, and one frame for display is 1/60 second. Moreover, a gate insulating film has a dielectric constant of 3.7 (F/m) and a thickness of 1×10^{-7} (m).

First, the area of a capacitor and the aperture ratio in the case where the above-described parameters apply to a panel (referred to as a first panel) in which the number of pixels is 540×RGB×960 are estimated. The size of the pixel in the panel is 26 (μm)×78 (μm), that is, 2.03×10^{-9} (m^2). The area other than a region occupied by a wiring and a thin film transistor is 1.43×10^{-9} (m^2), and the area of the region occupied by the wiring and the thin film transistor is 6.00×10^{-10} (m^2).

In the first panel, a minimum necessary capacitance of an auxiliary capacitor is 4.25×10^{-14} (F) in a pixel having a thin film transistor including an oxide semiconductor layer. In this case, the area necessary for the capacitor is 1.30×10^{10} (m^2); the capacitor accounts for 6.4% of the area of the pixel and the aperture ratio is 64.0%.

In addition, the area of a capacitor and the aperture ratio in the case where the above-described parameters apply to a panel (referred to as a second panel) in which the number of pixels is 480×RGB×640 are estimated. The size of a pixel in the panel is 36 (μm)×108 (μm), that is, 3.89×10^{-9} (m^2). The area excluding a region occupied by a wiring and a thin film transistor is 3.29×10^{-9} (m^2), and the area of the region occupied by the wiring and the thin film transistor is 6.00×10^{-10} (m^2).

In the second panel, a minimum necessary capacitance of an auxiliary capacitor is 4.25×10^{-14} (F) in a pixel having a

thin film transistor including an oxide semiconductor layer. In this case, the area necessary for the capacitor is 1.30×10^{-10} (m^2); the capacitor accounts for 3.3% of the area of the pixel and the aperture ratio is 81.2%.

When a thin film transistor including an oxide semiconductor layer according to one embodiment of the present invention is used for the first panel and the second panel, a capacitor line can be reduced and the region occupied by the pixel electrode **105** can be increased. The calculated aperture ratio in the first panel is 70.4% and that in the second panel is 84.5%; therefore, it is found that the aperture ratio is significantly increased by omitting a capacitor.

By a combination of the pixel in this embodiment with the structure in Embodiment 1 or 2, the aperture ratio can be increased when the pixel including a thin film transistor in which an oxide semiconductor is used is formed.

This embodiment can be implemented in combination with any of the structures described in the other embodiments as appropriate.

Embodiment 4

In this embodiment, an example of an electronic device including the liquid crystal display device described in any of Embodiments 1 to 3 will be described.

FIG. **17**A illustrates a portable game machine that can include a housing **9630**, a display portion **9631**, speakers **9633**, operation keys **9635**, a connection terminal **9636**, a recording medium reading portion **9672**, and the like. The portable game machine in FIG. **17**A can have a function of reading a program or data stored in the recording medium to display it on the display portion, a function of sharing information with another portable game machine by wireless communication, and the like. Note that the portable game machine in FIG. **17**A can have a variety of functions without being limited to the above.

FIG. **17**B illustrates a digital camera that can include the housing **9630**, the display portion **9631**, the speakers **9633**, the operation keys **9635**, the connection terminal **9636**, a shutter button **9676**, an image receiving portion **9677**, and the like. The digital camera having a television reception function in FIG. **17**B can have various functions such as a function of photographing a still image and/or a moving image; a function of automatically or manually correcting the photographed image; a function of obtaining various kinds of information through an antenna; a function of storing the photographed image or the information obtained through the antenna; and a function of displaying the photographed image or the information obtained through the antenna on the display portion. Note that the digital camera having the television reception function in FIG. **17**B can have a variety of functions without being limited to the above.

FIG. **17**C illustrates a television set that can include the housing **9630**, the display portion **9631**, the speakers **9633**, the operation keys **9635**, the connection terminal **9636**, and the like. The television set in FIG. **17**C can have a function of converting an electric wave for television into an image signal, a function of converting the image signal into a signal suitable for display, a function of converting a frame frequency of the image signal, and the like. Note that the television set in FIG. **17**C can have a variety of functions without being limited to the above.

FIG. **18**A illustrates a computer that can include the housing **9630**, the display portion **9631**, the speaker **9633**, the operation keys **9635**, the connection terminal **9636**, a pointing device **9681**, an external connection port **9680**, and the like. The computer in FIG. **18**A can have a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion, a function of controlling processing by a variety of software (programs), a communication function such as wireless communication or wired communication, a function of being connected to various computer networks with the communication function, a function of transmitting or receiving a variety of data with the communication function, and the like. Note that the computer in FIG. **18**A is not limited to having these functions and can have a variety of functions.

FIG. **18**B illustrates a mobile phone that can include the housing **9630**, the display portion **9631**, the speaker **9633**, the operation keys **9635**, a microphone **9638**, and the like. The mobile phone in FIG. **18**B can have a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion; a function of displaying a calendar, a date, the time, or the like on the display portion; a function of operating or editing the information displayed on the display portion; a function of controlling processing by various kinds of software (programs); and the like. Note that the functions of the mobile phone in FIG. **18**B are not limited to those described above, and the mobile phone can have various functions.

FIG. **18**C illustrates an electronic paper terminal (also referred to as an eBook or an e-book reader) that can include the housing **9630**, the display portion **9631**, the operation keys **9635**, and the like. The electronic paper in FIG. **18**C can have a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion; a function of displaying a calendar, a date, the time, or the like on the display portion; a function of operating or editing the information displayed on the display portion; a function of controlling processing by various kinds of software (programs); and the like. Note that the electronic paper in FIG. **18**C can have a variety of functions without being limited to the above.

The electronic devices described in this embodiment each can include a liquid crystal display device in which the aperture ratio of a plurality of pixels included in the display portion can be increased.

This embodiment can be implemented in combination with any of the structures described in the other embodiments as appropriate.

This application is based on Japanese Patent Application serial no. 2009-242787 filed with Japan Patent Office on Oct. 21, 2009, the entire contents of which are hereby incorporated by reference.

EXPLANATION OF REFERENCE

101: wiring, **102**A: wiring, **102**B: wiring, **103**: oxide semiconductor layer, **105**: pixel electrode, **106**: thin film transistor, **111**: substrate, **112**: base film, **113**: gate insulating film, **114**: oxide insulating layer, **121**: opening portion, **700**: substrate, **701**: pixel, **702**: pixel portion, **703**: scan line drive circuit, **704**: signal line drive circuit, **880**: pixel, **884**: wiring, **885**: wiring, **887**: wiring, **889**: common wiring, **984**: signal, **985**: signal, **1080**: subpixel, **1081**: transistor, **1082**: liquid crystal element, **1084**: wiring, **1085**: wiring, **1088**: pixel electrode, **2101**: wiring, **2102**A: wiring, **2102**B: wiring, **2103**: oxide semiconductor layer, **2104**: capacitor line, **2105**: pixel electrode, **2106**: thin film transistor, **2111**: substrate, **2112**: base film, **2113**: gate insulating film, **2114**: oxide insulating layer, **3880**: pixel, **3881**: transistor, **3882**: liquid crystal element, **3883**: capacitor, **3884**: wiring, **3885**: wiring,

3886: wiring, **3887**: wiring, **9630**: housing, **9631**: display portion, **9633**: speaker, **9635**: operation key, **9636**: connection terminal, **9638**: microphone, **9672**: recording medium insert reading portion, **9676**: shutter button, **9677**: image receiving portion, **9680**: external connection port, and **9681**: pointing device.

The invention claimed is:

1. A liquid crystal display device comprising:
- a transistor;
- a liquid crystal element electrically connected to the transistor; and
- an auxiliary capacitor electrically connected to the transistor and the liquid crystal element,
- wherein a channel formation region of the transistor is in an intrinsic or substantially intrinsic oxide semiconductor layer,
- wherein the liquid crystal element is provided in a pixel,
- wherein a capacitance of the auxiliary capacitor is smaller than a capacitance of the liquid crystal element,
- wherein the transistor has electric characteristics such that an off-current flowing through a region serving as the channel formation region is 1×10^{-12} A or less under a condition at which a temperature is 120° C., and
- wherein a voltage between a source and a drain of the transistor is **6** V at the condition.

2. A liquid crystal display device according to claim **1**, wherein the intrinsic or substantially intrinsic oxide semiconductor layer has a hydrogen concentration of $5\times10^{19}/cm^3$ or less and a carrier concentration of $5\times10^{14}/cm^3$ or less.

3. A liquid crystal display device according to claim **1**, wherein the liquid crystal element is provided in a subpixel included in the pixel.

4. A liquid crystal display device according to claim **1**,
- wherein the transistor further comprises:
- a gate electrode;
- a gate insulating layer overlapping with the gate electrode; and
- a source electrode and a drain electrode in contact with part of the intrinsic or substantially intrinsic oxide semiconductor layer,
- wherein the intrinsic or substantially intrinsic oxide semiconductor layer overlaps with the gate electrode.

5. An electronic device comprising the liquid crystal display device according to claim **1**.

6. A liquid crystal display device comprising:
- a transistor comprising:
  - a gate electrode;
  - a gate insulating layer over the gate electrode; and
  - an intrinsic or substantially intrinsic oxide semiconductor layer over the gate electrode; and
- an insulating layer over and in contact with the intrinsic or substantially intrinsic oxide semiconductor layer;
- a liquid crystal element electrically connected to the transistor; and
- an auxiliary capacitor electrically connected to the transistor and the liquid crystal element,
- wherein the liquid crystal element is provided in a pixel,
- wherein a capacitance of the auxiliary capacitor is smaller than a capacitance of the liquid crystal element,
- wherein the transistor has electric characteristics such that an off-current flowing through a region serving as a channel formation region is 1×10^{-12}A or less under a condition at which a temperature is 120° C., and
- wherein a voltage between a source and a drain of the transistor is **6** V at the condition.

7. A liquid crystal display device according to claim **6**, wherein the intrinsic or substantially intrinsic oxide semiconductor layer has a hydrogen concentration of $5\times10^{19}/cm^3$ or less and a carrier concentration of $5\times10^{14}/cm^3$ or less.

8. A liquid crystal display device according to claim **6**, wherein the liquid crystal element is provided in a subpixel included in the pixel.

9. An electronic device comprising the liquid crystal display device according to claim **6**.

10. A liquid crystal display device comprising:
- a transistor comprising:
  - a gate electrode;
  - an intrinsic or substantially intrinsic oxide semiconductor layer; and
  - a gate insulating layer between the gate electrode and the intrinsic or substantially intrinsic oxide semiconductor layer;
- a liquid crystal element electrically connected to the transistor; and
- an auxiliary capacitor electrically connected to the transistor and the liquid crystal element,
- wherein the liquid crystal element is provided in a pixel,
- wherein a capacitance of the auxiliary capacitor is smaller than a capacitance of the liquid crystal element,
- wherein the transistor has electric characteristics such that an off-current flowing through a region serving as a channel formation region is 1×10^{-12} A or less under a condition at which a temperature is 120° C., and
- wherein a voltage between a source and a drain of the transistor is **6** V at the condition.

11. A liquid crystal display device according to claim **10**, wherein the intrinsic or substantially intrinsic oxide semiconductor layer has a hydrogen concentration of $5\times10^{19}/cm^3$ or less and a carrier concentration of $5\times10^{14}/cm^3$ or less.

12. A liquid crystal display device according to claim **10**, wherein the liquid crystal element is provided in a subpixel included in the pixel.

13. An electronic device comprising the liquid crystal display device according to claim **10**.

14. A liquid crystal display device comprising:
- a liquid crystal panel; and
- a driver circuit IC,
- the liquid crystal panel comprising:
  - a first wiring;
  - a second wiring;
  - a transistor;
  - a liquid crystal element; and
  - a capacitor,
- wherein a gate of the transistor is electrically connected to the first wiring,
- wherein one of a source and a drain of the transistor is electrically connected to the second wiring,
- wherein the other of the source and the drain of the transistor is electrically connected to the liquid crystal element and the capacitor,
- wherein a channel formation region of the transistor is in an intrinsic or substantially intrinsic oxide semiconductor layer,
- wherein a capacitance of the capacitor is smaller than a capacitance of the liquid crystal element, and
- wherein the transistor has electric characteristics such that an off-current flowing through a region serving as the channel formation region is 1×10^{-12}A or less under a condition at which a temperature is 120° C.

15. A liquid crystal display device according to claim **14**,
- wherein the oxide semiconductor layer is provided so as to overlap the gate with a gate insulating layer interposed therebetween.

16. An electronic device comprising the liquid crystal display device according to claim 14.

* * * * *

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摘要(译)

提供一种液晶显示装置，其中可以在包括其中使用氧化物半导体的薄膜晶体管的像素中增加孔径比。在液晶显示装置中，薄膜晶体管包括栅电极，栅极绝缘层和氧化物半导体层，它们设置成与栅电极重叠，以及源电极和漏电极，它们与栅电极重叠。氧化物半导体层设置在设置在像素部分中的信号线和像素电极之间。薄膜晶体管的截止电流为1×10 -13 A或更小。只有液晶电容器才能保持电位，而没有与液晶元件平行的电容器，并且在像素部分中没有形成连接到像素电极的电容器。