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(54) LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **G02F 1/1343**

(52) **U.S. Cl.** **349/139**

(57) **ABSTRACT**

A method of manufacturing a liquid crystal display device is intended to decrease the number of manufacturing steps. The liquid crystal display device is arranged so that in each pixel area provided on a liquid-crystal-side surface of one of a pair of substrates disposed to oppose each other with a liquid crystal interposed therebetween, a signal from a drain line is applied to a pixel electrode via a drain electrode and a source electrode which are formed in a layer overlying a semiconductor layer of a thin film transistor, by the supply of a scanning signal from a gate electrode which is positioned as an underlying layer with respect to the semiconductor layer. The method of manufacturing such liquid crystal display device includes the steps of: forming a stacked structure in which the semiconductor layer and a first conductive layer are sequentially stacked in the same pattern, in both an area for forming the drain signal and an area for forming the thin film transistor; and after forming a second conductive layer, by using the same mask, providing separation between the drain electrode and the source electrode of the thin film transistor and also forming the pixel electrode connected to the source electrode.

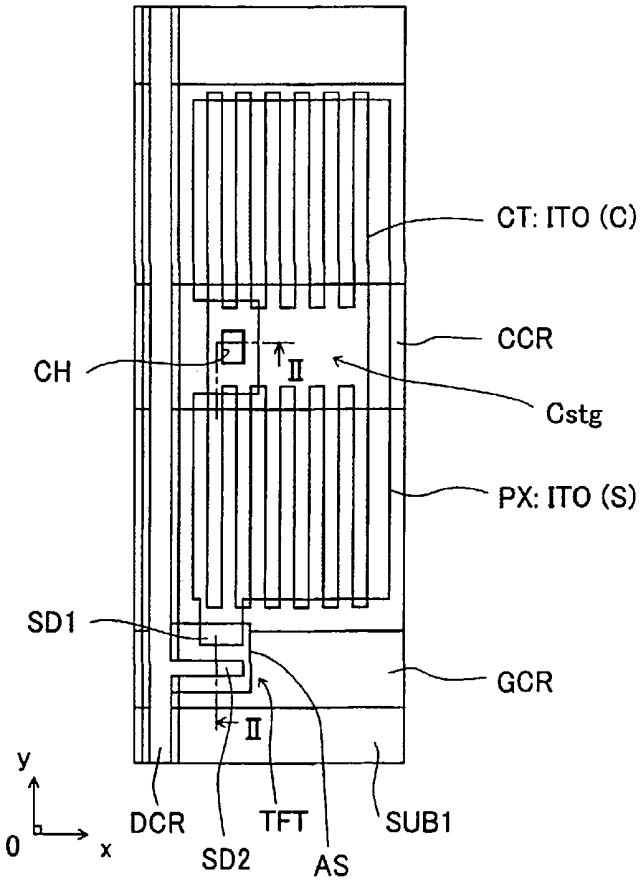


FIG. 1

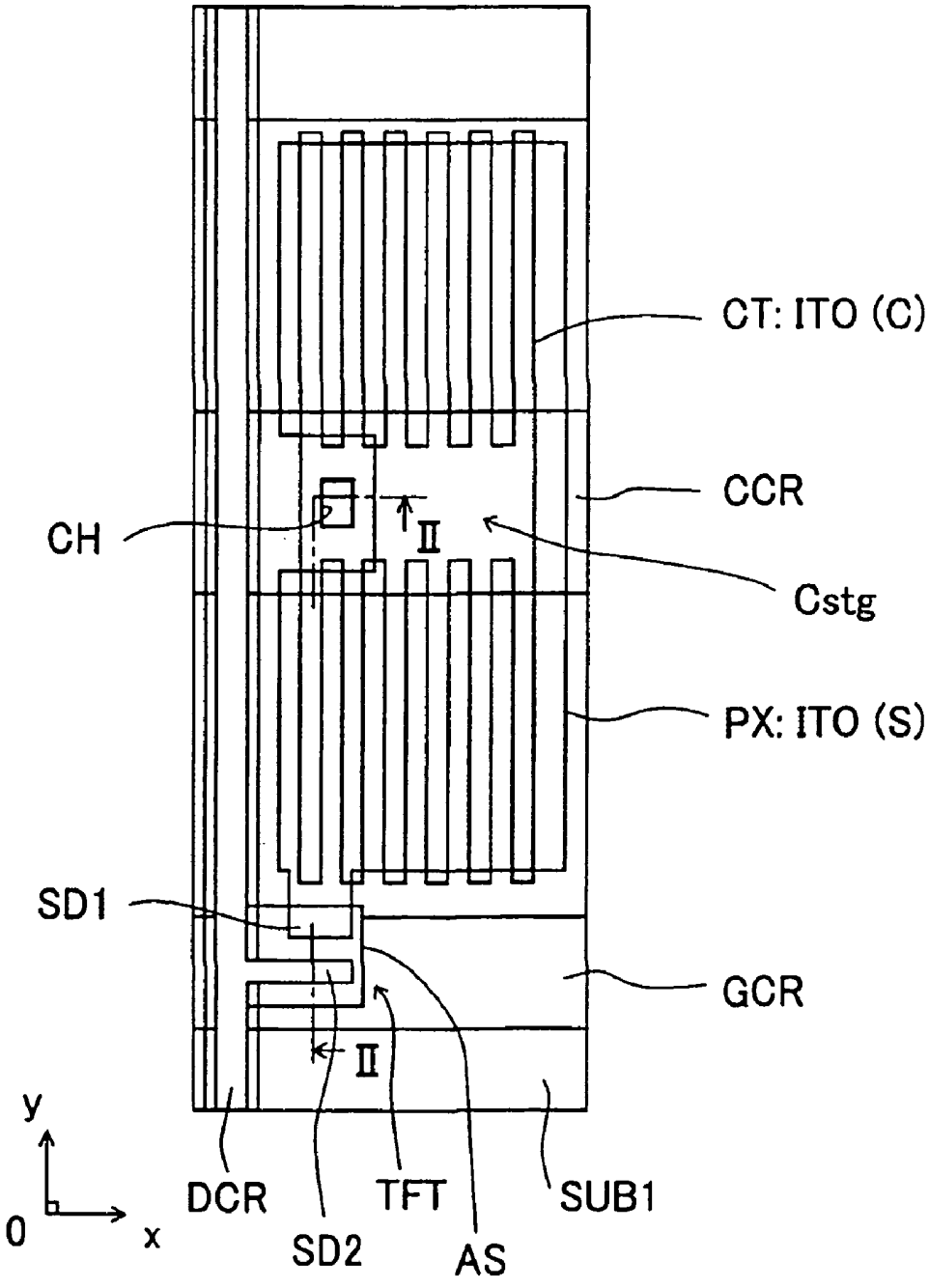
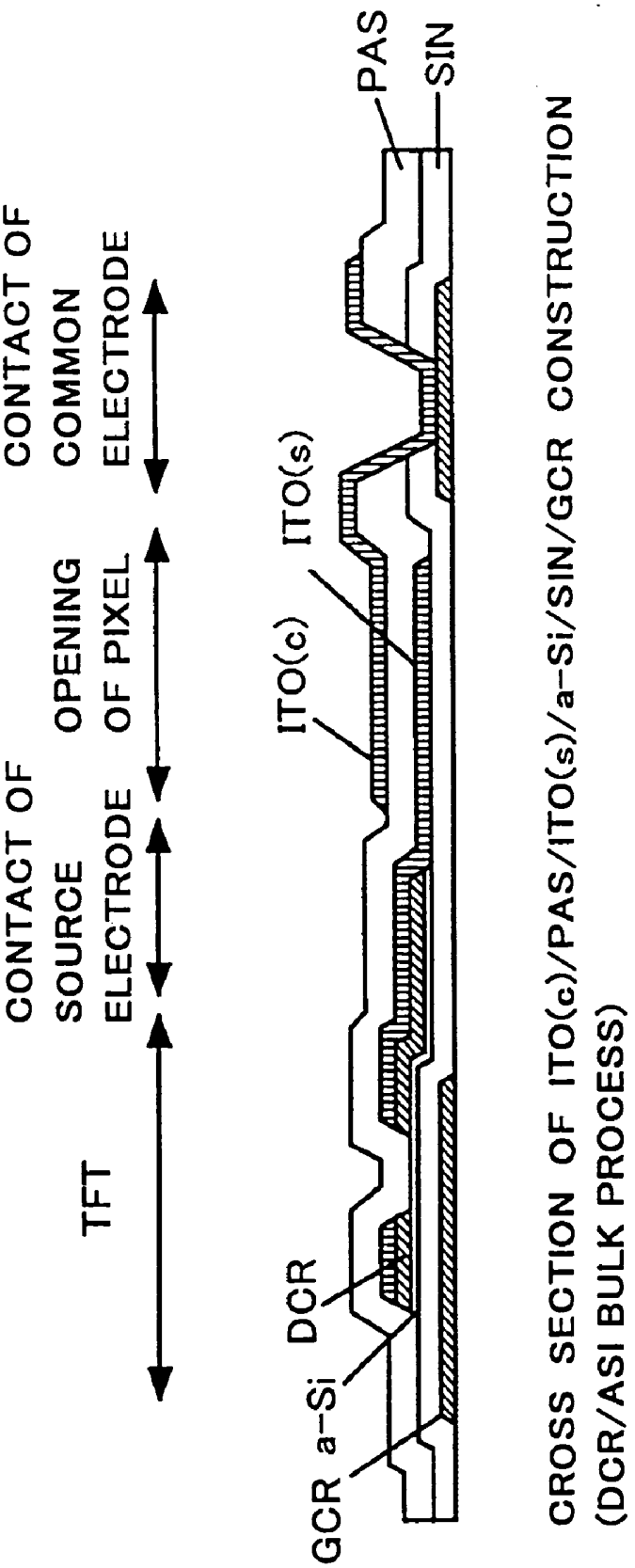
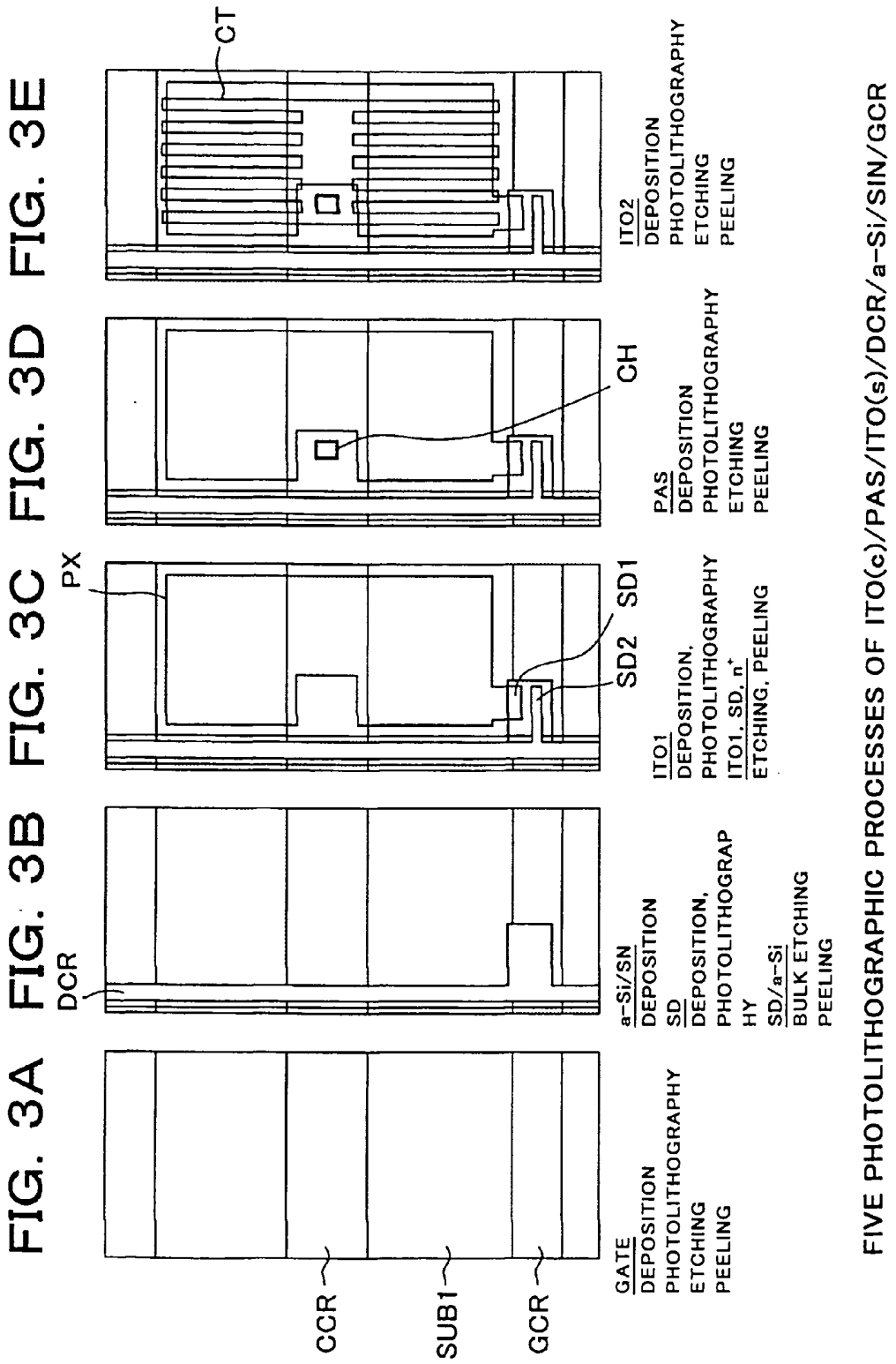
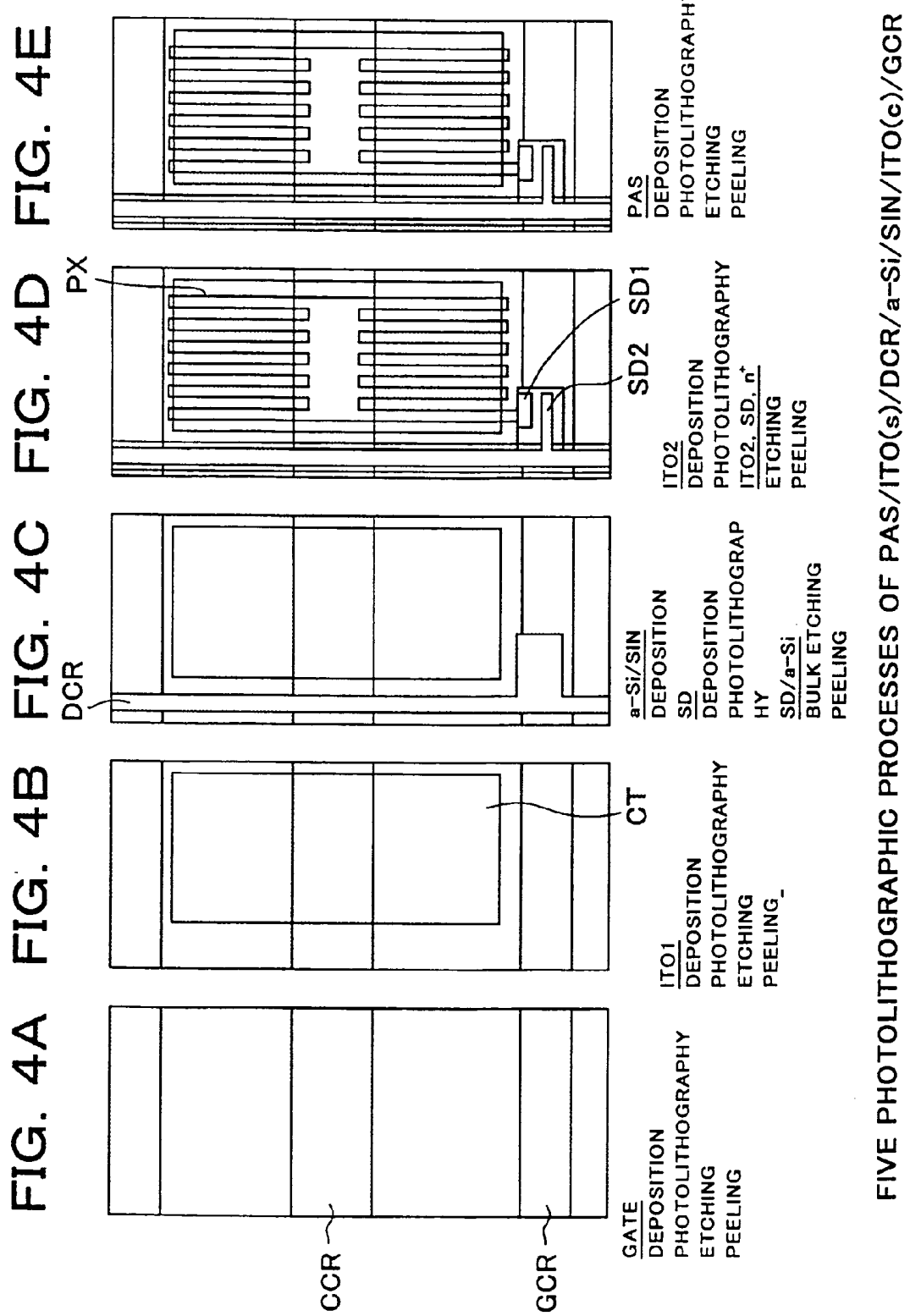


FIG. 2


CONTACT OF COMMON ELECTRODE
OPENING OF PIXEL
CONTACT OF SOURCE ELECTRODE
TFT
PAS
SIN
ITO(s)
ITO(c)
DCR
GCR a-Si
CROSS SECTION OF ITO(c)/PAS/ITO(s)/a-Si/SIN/GCR CONSTRUCTION
(DCR/ASI BULK PROCESS)



FIVE PHOTOLITHOGRAPHIC PROCESSES OF ITO(c)/PAS/ITO(s)/DCR/a-Si/SIN/GCR



FIVE PHOTOLITHOGRAPHIC PROCESSES OF PAS/ITO(s)/DCR/a-Si/SIN/ITO(c)/GCR

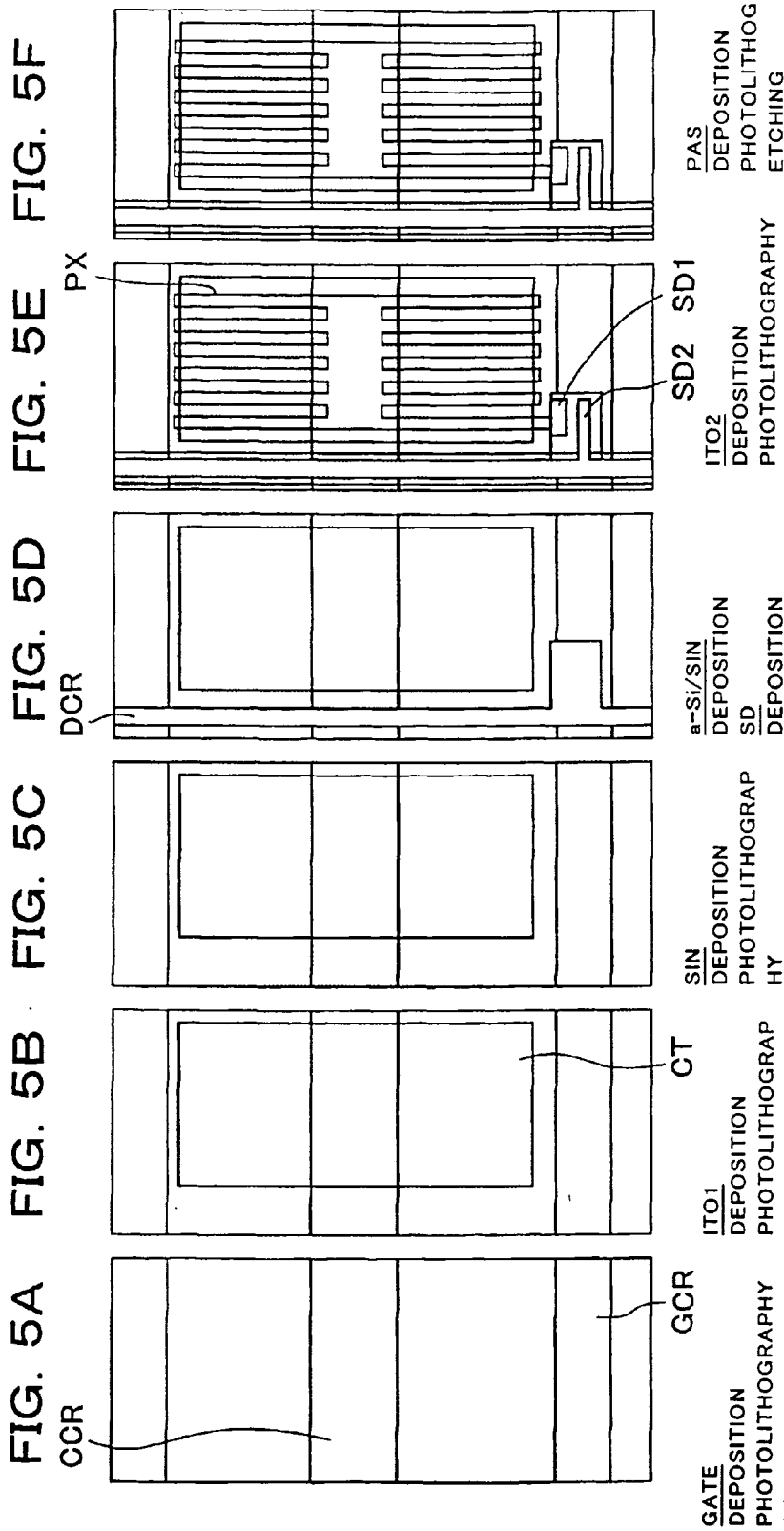
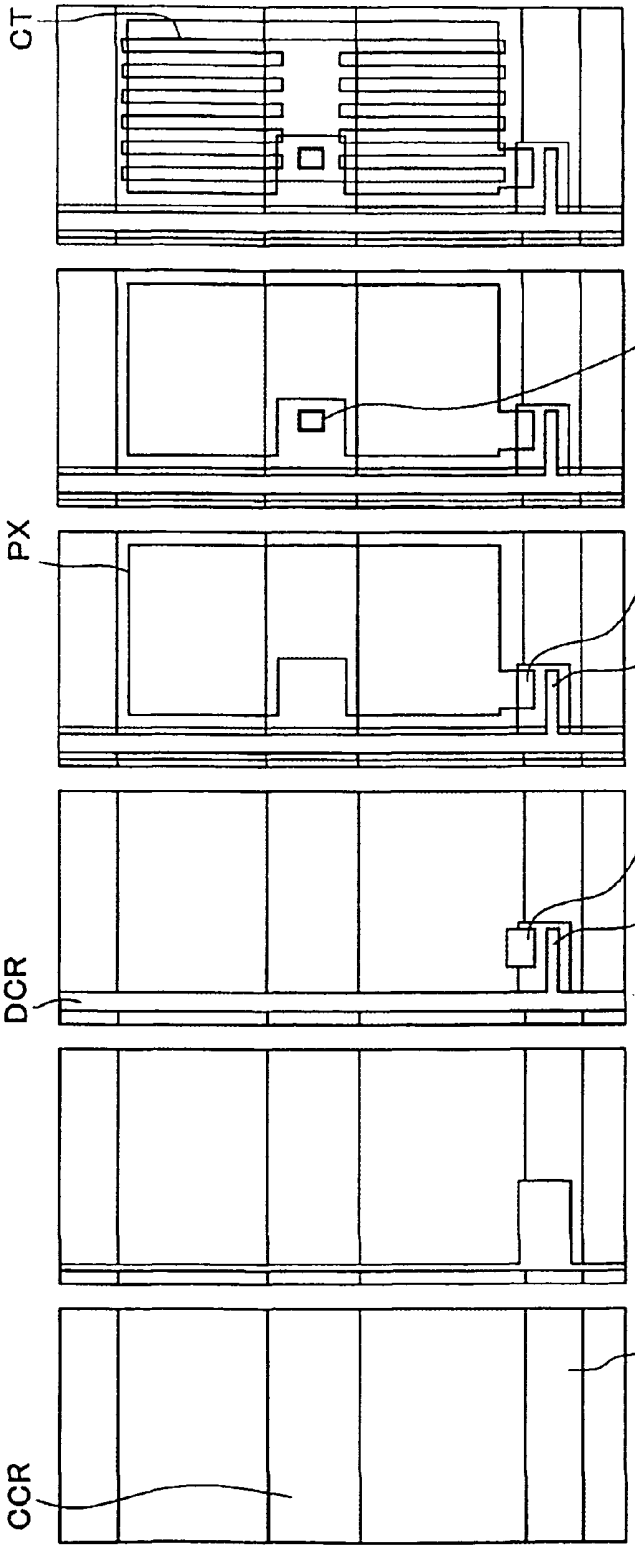
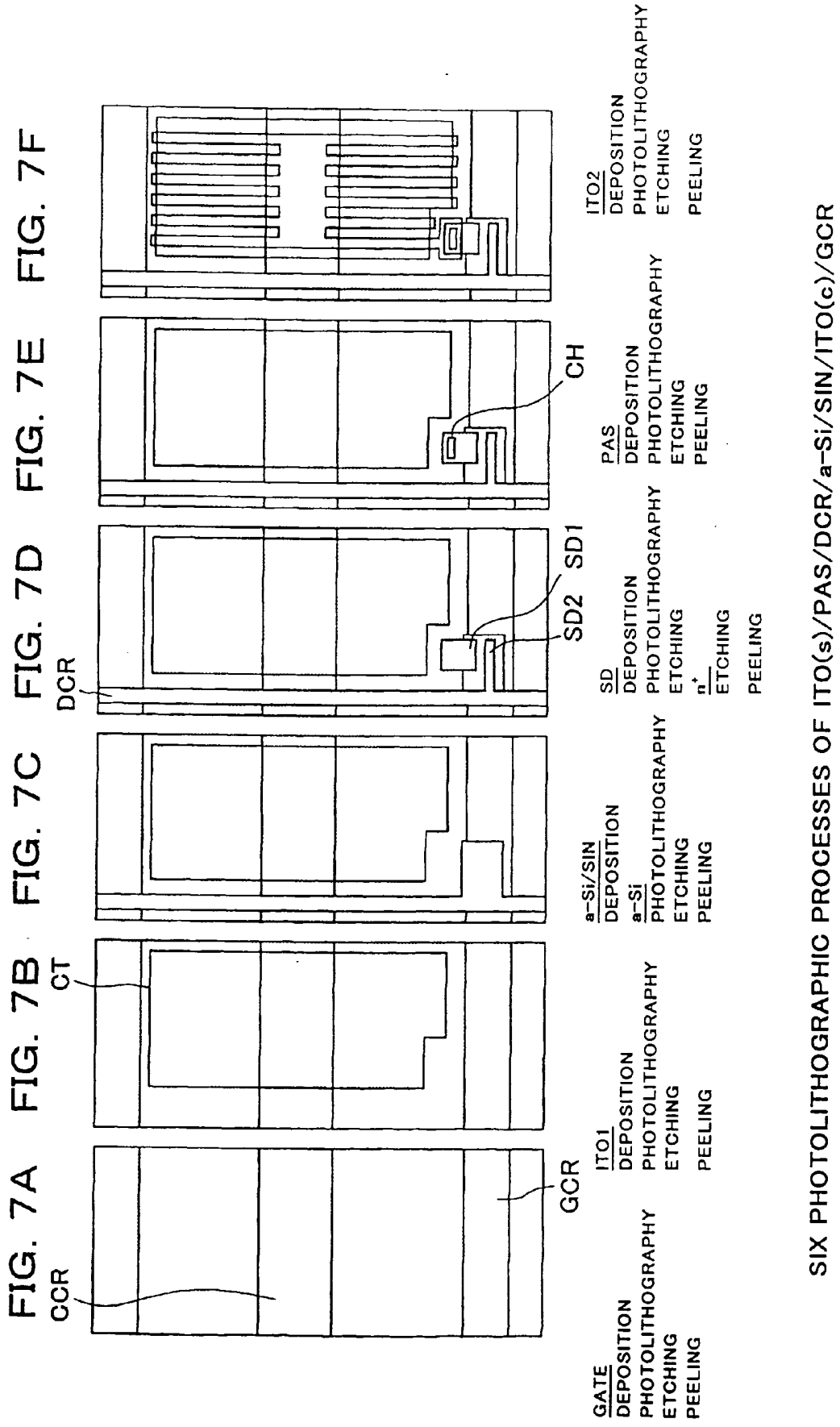


FIG. 5A
FIG. 5B
FIG. 5C
FIG. 5D
FIG. 5E
FIG. 5F
CCR
GCR
CT
DCR
PX
SD1
SD2
GATE
DEPOSITION
PHOTOLITHOGRAPHY
ETCHING
PEELING
ITO1
DEPOSITION
PHOTOLITHOGRAP
HY
ETCHING
PEELING
SIN
DEPOSITION
PHOTOLITHOGRAP
HY
ETCHING
PEELING
a-Si/SIN
DEPOSITION
SD
DEPOSITION
PHOTOLITHOGRAPHY
SD/a-Si
BULK ETCHING
PEELING
ITO2
DEPOSITION
PHOTOLITHOGRAPHY
ITO2, SD, n+
ETCHING
PEELING
PAS
DEPOSITION
PHOTOLITHOGRAPHY
ETCHING
PEELING
SIX PHOTOLITHOGRAPHIC PROCESSES OF PAS/ITO(s)/DCR/a-Si/SIN/ITO(c)/GCR



FIVE PHOTOLITHOGRAPHIC PROCESSES OF ITO(g)/PAS/ITO(s)/DCR/a-Si/SIN/GCR



SIX PHOTOLITHOGRAPHIC PROCESSES OF ITO(s)/PAS/DCR/a-Si/SIN/ITO(c)/GCR

FIG. 8

NO.	LAYER STRUCTURE	NUMBER OF TIMES OF PHOTOLITHOGRAPHY	MEANS FOR REDUCING NUMBER OF TIMES OF PHOTOLITHOGRAPHY	REMARKS
1	ITO(s)/PAS/ITO(c)/DCR/a-Si/SIN/GCR	5	DCR/ASI BULK PROCESS, PAS/SIN BULK PROCESS	
2		6	DCR/ASI BULK PROCESS (ADDITION OF SIN PHOTOLITHOGRAPHY OF NO.1)	
3		6	PAS/SIN BULK PROCESS (ADDITION OF AS PHOTOLITHOGRAPHY OF NO.1)	
4	ITO(c)/PAS/ITO(s)/DCR/a-Si/SIN/GCR	5	DCR/ASI BULK PROCESS, PAS/SIN BULK PROCESS	FIG. 2
5		6	DCR/ASI BULK PROCESS (ADDITION OF SIN PHOTOLITHOGRAPHY OF NO.4)	
6		6	PAS/SIN BULK PROCESS (ADDITION OF AS PHOTOLITHOGRAPHY OF NO.4)	FIG. 5
7	ITO(s)/PAS/DCR/ITO(c)/a-Si/SIN/GCR	6	PAS/SIN BULK PROCESS	
8	ITO(c)/PAS/DCR/ITO(c)/a-Si/SIN/GCR	6	PAS/SIN BULK PROCESS	
9	ITO(s)/PAS/DCR/a-Si/ITO(c)/SIN/GCR	6	PAS/SIN BULK PROCESS	
10	ITO(c)/PAS/DCR/a-Si/ITO(s)/SIN/GCR	6	PAS/SIN BULK PROCESS	
11	ITO(s)/PAS/DCR/a-Si/SIN/ITO(c)/GCR	6	PAS/SIN BULK PROCESS	FIG. 6
12	ITO(s)/PAS/DCR/a-Si/SIN/GCR/ITO(c)	6	PAS/SIN BULK PROCESS	
13	PAS/ITO(s)/DCR/a-Si/SIN/ITO(c)/GCR	5	DCR/ASI BULK PROCESS, PAS/SIN BULK PROCESS (ONLY PERIPHERY)	FIG. 3
14		6	DCR/ASI BULK PROCESS (ADDITION OF SIN PHOTOLITHOGRAPHY OF NO.13)	FIG. 4
15		6	PAS/SIN BULK PROCESS (ADDITION OF ASI PHOTOLITHOGRAPHY OF NO.13)	
16	PAS/DCR/ITO(s)/a-Si/SIN/ITO(c)/GCR	6	PAS/SIN BULK PROCESS (ONLY PERIPHERY)	
17	PAS/DCR/a-Si/ITO(s)/SIN/ITO(c)/GCR	6	PAS/SIN BULK PROCESS (ONLY PERIPHERY)	
18	PAS/ITO(s)/DCR/a-Si/SIN/GCR/ITO(c)	5	DCR/ASI BULK PROCESS, PAS/SIN BULK PROCESS (ONLY PERIPHERY)	
19		6	DCR/ASI BULK PROCESS (ADDITION OF SIN PHOTOLITHOGRAPHY OF NO.18)	
20		6	PAS/SIN BULK PROCESS (ADDITION OF ASI PHOTOLITHOGRAPHY OF NO.18)	
21	PAS/DCR/ITO(s)/a-Si/SIN/GCR/ITO(c)	6	PAS/SIN BULK PROCESS (ONLY PERIPHERY)	
22	PAS/DCR/a-Si/ITO(s)/SIN/GCR/ITO(c)	6	PAS/SIN BULK PROCESS (ONLY PERIPHERY)	

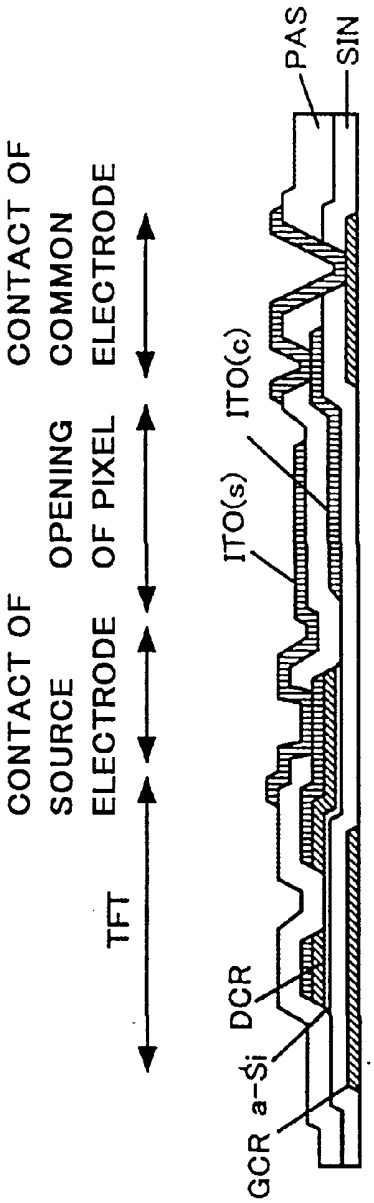


FIG. 9

CROSS SECTION OF ITO(s)/PAS/ITO(c)/DCR/a-Si/SIN/GCR CONSTRUCTION (DCR/ASI BULK PROCESS) CORRESPONDING NOS. 1 AND 2

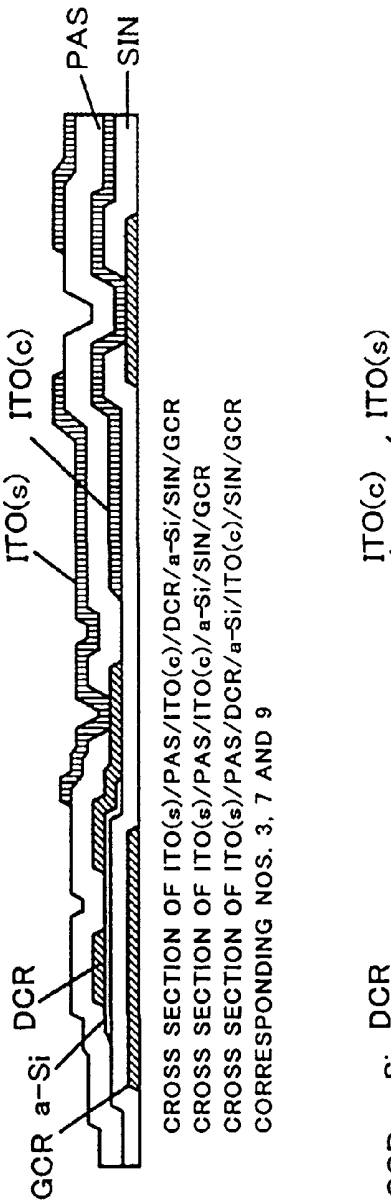


FIG. 10

CROSS SECTION OF ITO(s)/PAS/ITO(c)/DCR/a-Si/SIN/GCR
CROSS SECTION OF ITO(s)/PAS/ITO(c)/a-Si/SIN/GCR
CROSS SECTION OF ITO(s)/PAS/DCR/a-Si/ITO(c)/SIN/GCR
CORRESPONDING NOS. 3, 7 AND 9

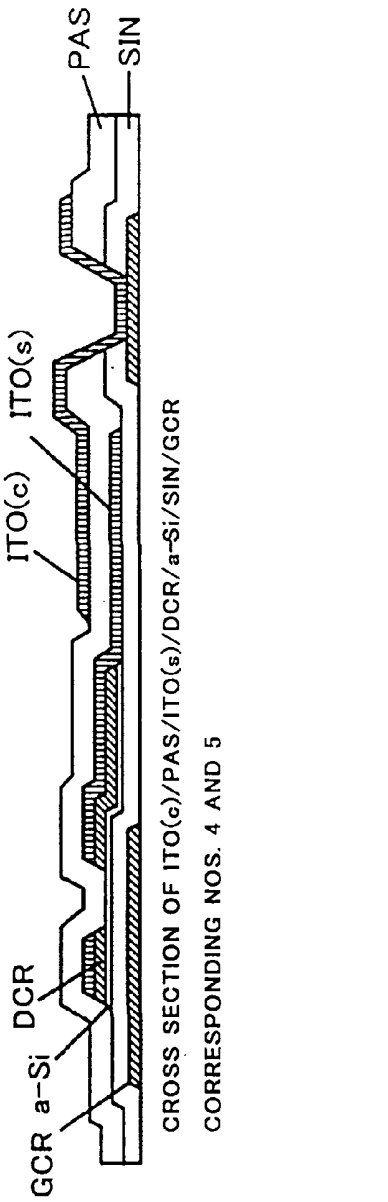


FIG. 11

CROSS SECTION OF ITO(c)/PAS/ITO(s)/DCR/a-Si/SIN/GCR
CORRESPONDING NOS. 4 AND 5

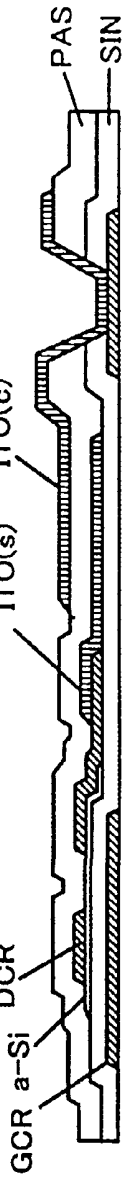


FIG. 12

CROSS SECTION OF ITO(c)/PAS/ITO(s)/DCR/a-Si/SIN/GCR
CORRESPONDING NO. 6

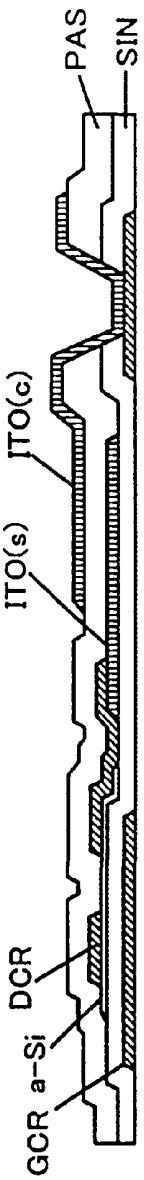


FIG. 13

CROSS SECTION OF ITO(c)/PAS/DCR/ITO(s)/a-Si/SIN/GCR
CROSS SECTION OF ITO(c)/PAS/DCR/a-Si/ITO(s)/SIN/GCR
CORRESPONDING NOS. 8 AND 10

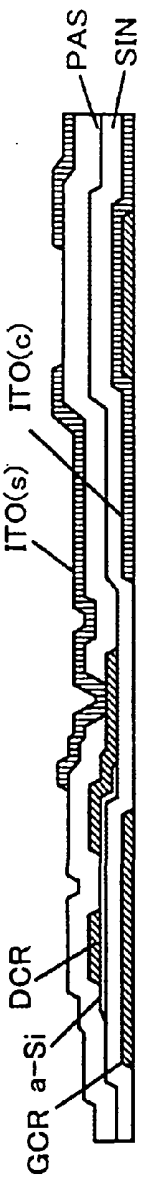


FIG. 14

CROSS SECTION OF ITO(s)/PAS/DCR/a-Si/SIN/ITO(c)/GCR
CORRESPONDING NO. 11

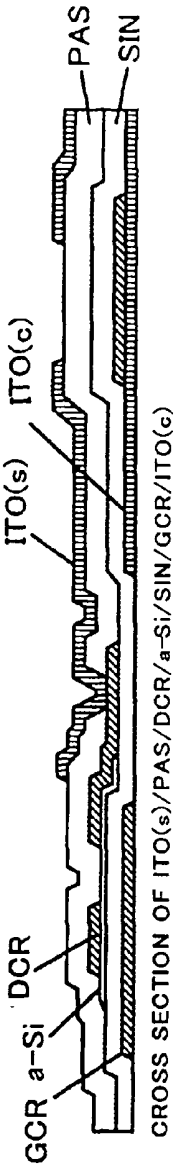


FIG. 15

CROSS SECTION OF ITO(s)/PAS/DCR/a-Si/SIN/GCR/ITO(c)
CORRESPONDING NO. 12

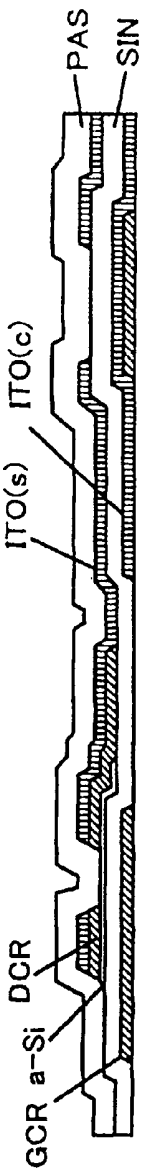


FIG. 16

CROSS SECTION OF PAS/ITO(s)/DCR/a-Si/SIN/ITO(c)/GCR
CONSTRUCTION (DCR/ASI BULK PROCESS)
CORRESPONDING NOS. 13 AND 14

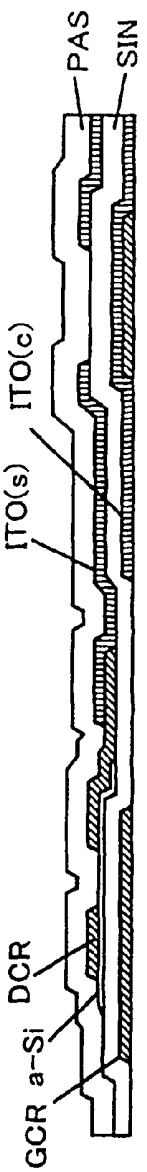


FIG. 17

CROSS SECTION OF PAS/ITO(s)/DCR/a-Si/SIN/ITO(c)/GCR
CORRESPONDING NO. 15

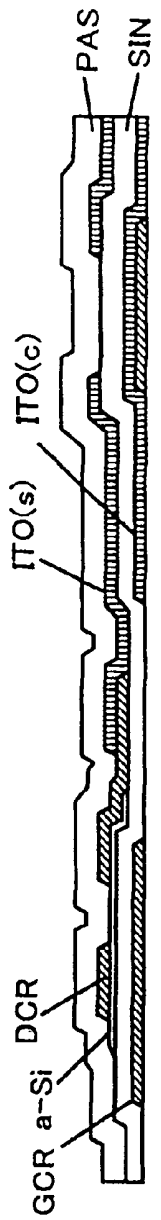


FIG. 18

CROSS SECTION OF PAS/DCR/ITO(s)/a-Si/SIN/ITO(c)/GCR
CROSS SECTION OF PAS/DCR/a-Si/ITO(s)/SIN/ITO(c)/GCR
CORRESPONDING NOS. 16 AND 17

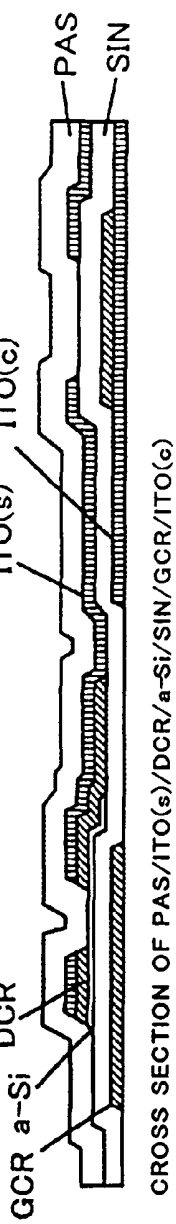


FIG. 19

CROSS SECTION OF PAS/ITO(s)/DCR/a-Si/SIN/GCR/ITO(c)
CONSTRUCTION (DCR/ASI BULK PROCESS)
CORRESPONDING NOS. 18 AND 19

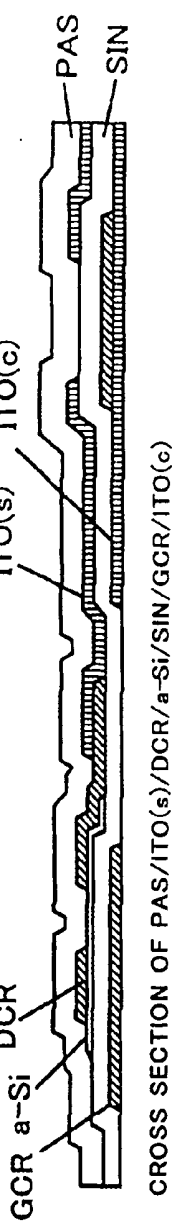
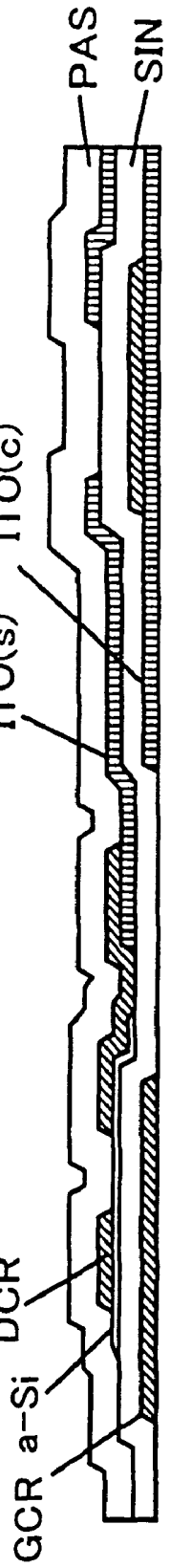


FIG. 20

CROSS SECTION OF PAS/ITO(s)/DCR/a-Si/SIN/GCR/ITO(c)
CORRESPONDING NO. 20

FIG. 21



CROSS SECTION OF PAS/DCR/a-Si/ITO(s)/SIN/GCR/ITO(c)
CORRESPONDING NOS. 21 AND 22

LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] The present application is a Continuation Application of Ser. No. 10/388,834, filed Mar. 14, 2003, which is a Continuation Application of Ser. No. 09/764,197, filed Jan. 16, 2001, which is related to and claims priority to Japanese Patent Application No. 2000-009179, filed on Jan. 18, 2000, all of which are herein incorporated by reference in their entirety for all purposes.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a method of manufacturing a liquid crystal display device and, more particularly, to a method of manufacturing a liquid crystal display device called In-Plane Switching Mode.

[0003] A liquid crystal display device which is called "IPS mode (In-Plane Switching Mode)" has a construction in which a pixel electrode and a counter electrode which causes an electric field (a lateral electric field) parallel to transparent substrates to be generated between the counter electrode and the pixel electrode are formed in each pixel on the liquid-crystal-side surface of one of the transparent substrates disposed to oppose each other with a liquid crystal interposed therebetween.

[0004] The in-plane switching mode of liquid crystal display device is constructed so that the amount of light to be transmitted through the area between the pixel electrode and the counter electrode is controlled by the driving of the liquid crystal to which the electric field is applied.

[0005] Such a liquid crystal display device is known as a type which is superior in so-called wide viewing angle characteristics which enable a displayed picture to remain unchanged even when its display surface is observed from an oblique direction.

[0006] The pixel electrode and the counter electrode have so far been formed of a conductive layer which does not transmit light therethrough.

[0007] In recent years, a liquid crystal display device constructed in the following manner has been known: a counter electrode made of a transparent electrode is formed over the entire area of each pixel area except the periphery thereof, and stripe-shaped pixel electrodes made of transparent electrodes disposed to be extended in one direction and to be juxtaposed in a direction transverse to the one direction are formed over the counter electrode with an insulating film interposed therebetween.

[0008] The liquid crystal display device having this construction causes a lateral electric field to be generated between each pixel electrode and the corresponding counter electrode, and is still superior in wide viewing angle characteristics and is greatly improved in aperture ratio.

[0009] Incidentally, this art is described, for example, in SID (Society for Information Display) 99 DIGEST: pp. 202-205, or Japanese Patent Laid-Open No. 202356/1999. However, in the case where such in-plane switch mode is applied to an active matrix type of liquid crystal display device, the number of manufacturing steps, particularly, since the number of times of repetition of selective etching using a photolithographic technique reaches seven, it has been desired to decrease the number.

[0010] Since such a series of photolithographic techniques employs different photomasks for its respective photolithographic cycles, the positional deviation of the photomasks precludes the formation of a high-resolution pixel structure, and a complicated process cannot be avoided.

SUMMARY OF THE INVENTION

[0011] The present invention has been made on the basis of the above-described circumstances, and provides a liquid crystal display device which can be reduced in the number of manufacturing steps.

[0012] A representative aspect of the invention disclosed in the present application will be described below in brief.

[0013] According to the present invention, there is provided a method of manufacturing a liquid crystal display device in which, in each pixel area provided on a liquid-crystal-side surface of one of a pair of substrates disposed to oppose each other with a liquid crystal interposed therebetween, a signal from a drain line is applied to a pixel electrode via a drain electrode and a source electrode which are formed in a layer overlying a semiconductor layer of a thin film transistor, by supply of a scanning signal from a gate electrode which is positioned as an underlying layer with respect to the semiconductor layer,

[0014] the manufacturing method comprising the steps of:

[0015] forming a stacked structure in which the semiconductor layer and a first conductive layer are sequentially stacked in the same pattern; and

[0016] after forming a second conductive layer over the stacked structure, by using the same mask, providing separation between the drain electrode and the source electrode of the thin film transistor and also forming the pixel electrode connected to the source electrode.

[0017] In the method of manufacturing the liquid crystal display device constructed in this manner, the formation of the semiconductor layer of the thin film transistor, the formation of the drain line (the drain electrode and the source electrode) and the formation of the pixel electrode can be completed in two steps each, whereby it is possible to reduce the number of manufacturing steps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The invention will become more readily appreciated and understood from the following detailed description of preferred embodiments of the invention when taken in conjunction with the accompanying drawings, in which:

[0019] **FIG. 1** is a plan view showing one embodiment of a pixel area of a liquid crystal display device according to the present invention;

[0020] **FIG. 2** is a cross-sectional view taken along line II-II of **FIG. 1**;

[0021] **FIG. 3** is a process diagram showing one embodiment of a method of manufacturing the liquid crystal display device according to the present invention;

[0022] **FIG. 4** is a process diagram showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention;

[0023] **FIG. 5** is a process diagram showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention;

[0024] **FIG. 6** is a process diagram showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention;

[0025] **FIG. 7** is a process diagram showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention;

[0026] **FIG. 8** is a table showing in list form other embodiments of the method of manufacturing the liquid crystal display device according to the present invention (inclusive of the above-described embodiments);

[0027] **FIG. 9** is a cross-sectional view showing one embodiment of the layer structure of a pixel area of a liquid crystal display device formed by the manufacturing method according to the present invention;

[0028] **FIG. 10** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0029] **FIG. 11** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0030] **FIG. 12** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0031] **FIG. 13** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0032] **FIG. 14** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0033] **FIG. 15** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0034] **FIG. 16** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0035] **FIG. 17** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0036] **FIG. 18** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0037] **FIG. 19** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention;

[0038] **FIG. 20** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention; and

[0039] **FIG. 21** is a cross-sectional view showing another embodiment of the layer structure of the pixel area of the liquid crystal display device formed by the manufacturing method according to the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

[0040] Preferred embodiments of a method of manufacturing a liquid crystal display device according to the present invention will be described below with reference to the accompanying drawings.

[0041] [Embodiment 1]

[0042] Construction of Pixel

[0043] **FIG. 1** is a plan view showing one pixel of a liquid crystal display device to which the present invention is applied. **FIG. 2** is a cross-sectional view taken along line II-II of **FIG. 1**.

[0044] In **FIG. 1**, there is shown a transparent substrate SUB1. This transparent substrate SUB1 is a so-called TFT substrate which is disposed to oppose a transparent substrate which is called a color filter substrate (not shown) with a liquid crystal interposed therebetween.

[0045] Gate lines GCR are formed over the liquid-crystal side surface of the transparent substrate SUB1 in such a manner as to be extended in the x-direction of **FIG. 1** and to be juxtaposed in the y-direction of **FIG. 1**, while a counter voltage signal line CCR is formed over the same liquid-crystal side surface in such a manner as to be extended in the x-direction of **FIG. 1** between each of the gate lines GCR. Each of the signal lines GCR and CCR is formed of the same metal layer, for example, a Cr layer.

[0046] An insulating film GI made of, for example, a silicon nitride film (SiN) is formed over the surface of the transparent substrate SUB1 in such a manner as to cover all of the signal lines GCR and CCR.

[0047] This insulating film GI has the function of an interlayer insulating film for insulating drain lines DCR (to be described later) from the gate lines GCR and the counter voltage signal lines CCR. The insulating film GI also has the function of a gate insulating film in each area in which a thin film transistor TFT which will be described below is formed, as well as the function of a dielectric film in each area in which a capacitance element Cstg which will be described below is formed.

[0048] As shown in the bottom left portion of **FIG. 1**, the thin film transistor TFT is formed over a portion of the gate line GCR of the pixel area, and a semiconductor layer AS is formed on the insulating film GI. This semiconductor layer AS is made of, for example, amorphous silicon (a-Si), and a high-concentration impurity layer which is doped with, for

example, phosphorus (P) to serve as a contact layer is formed on the surface of the semiconductor layer AS.

[0049] Incidentally, this semiconductor layer AS is connected to that of the thin film transistor TFT, and is also formed in the area in which the drain line DCR which will be described later is formed in order to strengthen the function of an interlayer insulating film for insulating the drain line DCR from the gate line GCR and the counter voltage signal line CCR.

[0050] A drain electrode SD2 and a source electrode SD1 are formed on the upper surface of the semiconductor layer AS in the area in which the thin film transistor TFT is formed, whereby an inverted staggered structure MIS transistor is formed which uses a portion of the gate line GCR as its gate electrode. The drain electrode SD2 is formed integrally with the drain line DCR which will be described later.

[0051] Specifically, the drain line DCR which is disposed to be extended in the y-direction of **FIG. 1** is formed of, for example, Cr, and a portion of the drain line DCR is formed to be extended to the semiconductor layer AS lying in the area in which the thin film transistor TFT is formed, whereby the drain electrode SD2 is formed.

[0052] The source electrode SD1 which is formed to oppose the drain electrode SD2 is formed by extending a portion of a pixel electrode PX which is formed in nearly the whole area of the central portion of the pixel area that excludes the peripheral narrow portion thereof.

[0053] Incidentally, in this embodiment, the same metal layer as the drain line DCR is formed to be interposed between the pixel electrode PX and the semiconductor layer AS (refer to **FIG. 2**). This pixel electrode PX is formed of, for example, a transparent conductive film made of ITO (Indium-Tin-Oxide), and is formed to avoid a portion of an area superposed on the counter voltage signal line CCR. This portion serves as a location which provides connection between a counter electrode CT and the counter voltage signal line CCR.

[0054] A protective film PAS which is made of, for example, a silicon nitride film (SiN) is formed over the whole area of the surface processed in this manner, and a contact hole CH is formed in the protective film PAS. The contact hole CH exposes a portion of the area of the counter voltage signal line CCR on which the pixel electrode PX is not superposed.

[0055] In addition, the counter electrode CT is formed on the surface of the protective film PAS. This counter electrode CT is made of, for example, a transparent conductive film made of ITO (Indium-Tin-Oxide), and is connected to the counter voltage signal line CCR through the contact hole CH.

[0056] The counter electrode CT is constructed of multiple stripe-shaped electrodes formed to be extended in the y-direction of **FIG. 1** and to be juxtaposed in the x-direction of **FIG. 1**, and the portion of the counter electrode CT that is superposed on the counter voltage signal line CCR has a wide-area portion connected to the counter voltage signal line CCR.

[0057] The capacitance element Cstg is formed in this portion, and owing to the storage capacitance Cstg, the picture signal supplied from the drain line DCR through the thin film transistor TFT is stored in the pixel electrode PX for a long time when the thin-film transistor TFT is turned off.

[0058] Manufacturing Method

[0059] **FIGS. 3A** to **3**E are process diagrams showing one example of a method of manufacturing the liquid crystal display device shown in **FIG. 1**.

[0060] Step **1** (**FIG. 3A**)

[0061] The transparent substrate SUB1 is prepared, and a metal film made of, example, Cr is formed over the entire liquid-crystal-side surface of the transparent substrate SUB1. The metal film is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0062] Thus, the gate line GCR which is extended in the x-direction below the pixel area and the counter voltage signal line CCR which is extended in the x-direction in the central portion of the pixel area are formed over the surface of the transparent substrate SUB1.

[0063] Step **2** (**FIG. 3B**)

[0064] The insulating film GI made of, for example, a silicon nitride film (SiN) and the semiconductor layer AS made of amorphous silicon (a-Si) are sequentially formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0065] Incidentally, a contact layer doped with an impurity made of, for example, phosphorus (P) is formed on the surface of the semiconductor layer AS. In addition, a metal film made of, for example, Cr is formed over the entire surface of the transparent substrate SUB1.

[0066] Then, the metal film and the underlying semiconductor layer AS are formed into a predetermined pattern by a selective etching method using a photolithographic technique. The metal film and the semiconductor layer AS are etched in bulk into the same pattern.

[0067] Thus, the drain electrode SD2 and the source electrode SD1 which are integrally connected to each other are formed together with the drain line DCR (the semiconductor layer AS is formed in the same pattern below the drain electrode SD2 and the source electrode SD1).

[0068] Step **3** (**FIG. 3C**)

[0069] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1.

[0070] Then, the transparent conductive film and the metal film are formed into a predetermined pattern by a selective etching method using a photolithographic technique. The mask used for this photolithographic technique has a pattern including the drain line DCR, the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT, and the pixel electrode PX. These lines and electrodes can be formed with one mask because they are not formed in the state of being superposed on one another.

[0071] Specifically, a disconnection-preventing signal line to be superposed on the drain line DCR and the pixel electrode PX are formed by the selective etching of the

transparent conductive film by the use of the mask (during this time, the transparent conductive film is etched along the patterns of the source electrode SD1 and the drain electrode SD2 of the thin film transistor TFT to be connected to the pixel electrode PX). Then, the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT are formed by the selective etching of the metal film that underlies the transparent conductive film.

[0072] After that, the contact layer on the surface of the semiconductor layer AS is etched by using the same mask. In this step, the drain line DCR (as well as the drain electrode SD2) is formed as part of a stacked structure in which the metal layer and the transparent conductive film and the drain line DCR are stacked in that order. Owing to this step, the disconnection-preventing signal line is formed in the state of being superposed on the drain line DCR, whereby it is possible to greatly decrease the probability that disconnection occurs in the drain line DCR.

[0073] Incidentally, the pixel electrode PX needs to be formed in a pattern which partly includes an area which is not superposed on the counter voltage signal line CCR. This portion is intended to provide connection between the counter voltage signal line CCR and the counter electrode CT which will be formed in a later step.

[0074] Step **4** (**FIG. 3D**)

[0075] The protective film PAS made of, for example, a silicon nitride film (SiN) is formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0076] Then, the contact hole CH is formed in the area in which the pixel electrode PX is not formed above the counter voltage signal line CCR, by a selective etching method using a photolithographic technique.

[0077] At the same time, openings in which to expose the terminals of the drain line DCR, the gate line GCR and the counter voltage signal line CCR are also formed in a portion except the pixel area.

[0078] Step **5** (**FIG. 3E**)

[0079] A transparent conductive film made of, for example, ITO is formed over the entire surface of the transparent substrate SUB1 processed in this manner, and the transparent conductive film is formed into a predetermined pattern by a selective etching method using a photolithographic technique, whereby the counter electrode CT is formed.

[0080] The counter electrode CT is formed to be superposed on the pixel electrode PX, and is formed of multiple stripe-shaped electrodes formed to be extended in the y-direction of **FIG. 3E** and to be juxtaposed in the x-direction of **FIG. 3E**.

[0081] Then, each of the stripe-shaped electrodes is connected to the others so that the area of the portion of the counter electrode CT that is superposed on the counter voltage signal line CCR is increased (for the purpose of forming the capacitance element cstg), and the counter electrode CT is connected to the counter voltage signal line CCR through the contact hole CH formed in the protective film PAS.

[0082] The method of manufacturing the liquid crystal display device constructed in this manner is completed by repeating five times the selective etching method using the photolithographic technique. Accordingly, it is possible to reduce the number of steps of the manufacturing process.

[0083] [Embodiment 2]

[0084] **FIGS. 4A** to **4E** are process diagrams showing another embodiment of the liquid crystal display device according to the present invention.

[0085] Step **1** (**FIG. 4A**)

[0086] The transparent substrate SUB1 is prepared, and a metal film made of, example, Cr is formed over the entire liquid-crystal-side surface of the transparent substrate SUB1.

[0087] Thus, the gate line GCR and the counter voltage signal line CCR are formed.

[0088] Step **2** (**FIG. 4B**)

[0089] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1, and then the transparent conductive film is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0090] Thus, the counter electrode CT connected to the counter voltage signal line CCR is formed over the central portion of the pixel area that excludes the peripheral narrow portion thereof.

[0091] Step **3** (**FIG. 4C**)

[0092] The insulating film GI made of, for example, a silicon nitride film (SiN) and the semiconductor layer AS made of amorphous silicon (a-Si) are sequentially formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0093] Incidentally, a contact layer doped with an impurity made of, for example, phosphorus (P) is formed on the surface of the semiconductor layer AS. In addition, a metal film made of, for example, Cr is formed over the entire surface of the transparent substrate SUB1.

[0094] Then, the metal film and the underlying semiconductor layer AS are formed into a predetermined pattern by a selective etching method using a photolithographic technique. The metal film and the semiconductor layer AS are etched in bulk into the same pattern.

[0095] Thus, the drain electrode SD2 and the source electrode SD1 which are integrally connected to each other are formed together with the drain line DCR (the semiconductor layer AS is formed in the same pattern below the drain electrode SD2 and the source electrode SD1).

[0096] Step **4** (**FIG. 4D**)

[0097] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1.

[0098] Then, the transparent conductive film and the metal film are formed into a predetermined pattern by a selective etching method using a photolithographic technique. The mask used for this photolithographic technique has a pattern including the drain line DCR, the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT, and

the pixel electrode PX. These lines and electrodes can be formed with one mask because they are not formed in the state of being superposed on one another.

[0099] Specifically, a disconnection-preventing signal line to be superposed on the drain line DCR and the pixel electrode PX are formed by the selective etching of the transparent conductive film by the use of the mask (during this time, the transparent conductive film is etched along the patterns of the source electrode SD1 and the drain electrode SD2 of the thin film transistor TFT to be connected to the pixel electrode PX). Then, the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT are formed by the selective etching of the metal film that underlies the transparent conductive film.

[0100] The pixel electrode PX is formed of multiple stripe-shaped electrodes formed to be extended in the y-direction of **FIG. 4D** and to be juxtaposed in the x-direction of **FIG. 4D**, and the portion of the pixel electrode PX that is superposed on the counter voltage signal line CCR has a comparatively large area. At this portion, the capacitance element Cstg is formed.

[0101] After that, the contact layer on the surface of the semiconductor layer AS is etched by using the same mask.

[0102] Step **5** (**FIG. 4E**)

[0103] The protective film PAS made of, for example, a silicon nitride film (SiN) is formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0104] Then, openings for exposing the terminals of the drain line DCR, the gate line GCR and the counter voltage signal line CCR are formed in a portion except the pixel area by a selective etching method using a photolithographic technique.

[0105] The method of manufacturing the liquid crystal display device constructed in this manner is completed by repeating five times the selective etching method using the photolithographic technique, whereby it is possible to reduce the number of steps of the manufacturing process.

[0106] [Embodiment 3]

[0107] **FIGS. 5A** to **5**F are process diagrams showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention.

[0108] Step **1** (**FIG. 5A**)

[0109] The transparent substrate SUB1 is prepared, and a metal film made of, example, Cr is formed over the entire liquid-crystal-side surface of the transparent substrate SUB1, and the metal film is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0110] Thus, the gate line GCR and the counter voltage signal line CCR are formed.

[0111] Step **2** (**FIG. 5B**)

[0112] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1, and then the transparent conductive film is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0113] Thus, the counter electrode CT connected to the counter voltage signal line CCR is formed over the central portion of the pixel area that excludes the peripheral narrow portion thereof.

[0114] Step **3** (**FIG. 5C**)

[0115] An insulating film made of, for example, a silicon nitride film (SiN) is formed over the entire surface of the transparent substrate SUB1.

[0116] After that, openings for exposing the terminals of the gate line GCR and the counter voltage signal line CCR are formed in a portion except the pixel area by a selective etching method using a photolithographic technique.

[0117] Step **4** (**FIG. 5C**)

[0118] The insulating film GI made of, for example, a silicon nitride film (SiN) and the semiconductor layer AS made of amorphous silicon (a-Si) are sequentially formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0119] Incidentally, a contact layer doped with an impurity made of, for example, phosphorus (P) is formed on the surface of the semiconductor layer AS. In addition, a metal film made of, for example, Cr is formed over the entire surface of the transparent substrate SUB1.

[0120] Then, the metal film and the underlying semiconductor layer AS are formed into a predetermined pattern by a selective etching method using a photolithographic technique. The metal film and the semiconductor layer AS are etched in bulk into the same pattern.

[0121] Thus, the drain electrode SD2 and the source electrode SD1 which are connected to each other are formed together with the drain line DCR (the semiconductor layer AS is formed in the same pattern below the drain electrode SD2 and the source electrode SD1).

[0122] Step **5** (**FIG. 5E**)

[0123] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1.

[0124] Then, the transparent conductive film and the metal film are formed into a predetermined pattern by a selective etching method using a photolithographic technique. The mask used for this photolithographic technique has a pattern including the drain line DCR, the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT, and the pixel electrode PX.

[0125] Specifically, the drain line DCR and the pixel electrode PX are formed by the selective etching of the transparent conductive film using the mask (in this case, etching is effected along the patterns of the source electrode SD1 and the drain electrode SD2 to be connected to the pixel electrode PX), and the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT are formed by the selective etching of the metal film which underlies the transparent conductive film.

[0126] After that, the contact layer on the surface of the semiconductor layer AS is etched by using the same mask.

[0127] Step **6** (**FIG. 5F**)

[0128] The protective film PAS made of, for example, a silicon nitride film (SiN) is formed over the entire surface of the transparent substrate SUB**1** processed in this manner.

[0129] Then, openings for exposing the terminals of the drain line DCR, the gate line GCR and the counter voltage signal line CCR are formed in a portion except the pixel area by a selective etching method using a photolithographic technique.

[0130] The method of manufacturing the liquid crystal display device constructed in this manner is completed by repeating five times the selective etching method using the photolithographic technique, whereby it is possible to reduce the number of steps of the manufacturing process.

[0131] [Embodiment 4]

[0132] **FIGS. 6A** to **6**F are process diagrams showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention.

[0133] Step **1** (**FIG. 6A**)

[0134] The transparent substrate SUB**1** is prepared, and a metal film made of, example, Cr is formed over the entire liquid-crystal-side surface of the transparent substrate SUB**1**, and the metal film is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0135] Thus, the gate line GCR and the counter voltage signal line CCR are formed.

[0136] Step **2** (**FIG. 6B**)

[0137] The insulating film GI made of, for example, a silicon nitride film (SiN) and the semiconductor layer AS made of amorphous silicon (a-Si) are sequentially formed over the entire surface of the transparent substrate SUB**1** processed in this manner.

[0138] Incidentally, a high-concentration impurity layer for formation of a contact layer doped with an impurity made of, for example, phosphorus (P) is formed on the surface of the semiconductor layer AS.

[0139] Then, the semiconductor layer AS is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0140] Thus, the semiconductor layer AS is left in an area in which to form the thin film transistor TFT and in an area in which to form the drain line DCR.

[0141] The reason why the semiconductor layer AS is allowed to remain in the area in which to form the drain line DCR is to improve the function of an interlayer insulating film for insulating the drain line DCR (to be formed later) from the gate line GCR and the counter voltage signal line CCR.

[0142] Step **3** (**FIG. 6C**)

[0143] A metal film made of for example, Cr is formed over the entire surface of the transparent substrate SUB**1**.

[0144] Then, the metal film is formed into a predetermined pattern by a selective etching method using a photolithographic technique, thereby forming the drain line DCR and the drain electrode SD**2** and the source electrode SD**1** of the thin film transistor TFT.

[0145] Step **4** (**FIG. 6D**)

[0146] A transparent conductive film made of for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB**1**.

[0147] Then, the transparent conductive film is formed into a predetermined pattern by a selective etching method using a photolithographic technique, thereby forming the pixel electrode PX and a disconnection-preventing signal line.

[0148] The pixel electrode PX is formed to be connected to the source electrode SD**1** of the thin film transistor TFT. Excepting a part of the portion of the pixel electrode PX that is superposed on the counter voltage signal line CCR, the pixel electrode PX is formed over the entire area of the central portion of the pixel area that excludes the peripheral narrow portion thereof, and the disconnection-preventing signal line is formed to be superposed on the drain line DCR.

[0149] After that, the high-concentration impurity layer formed on the surface of the semiconductor layer AS is etched by using as a mask the drain electrode SD**2** and the source electrode SD**1** of the thin film transistor TFT.

[0150] Step **5** (**FIG. 6E**)

[0151] The protective film PAS made of, for example, a silicon nitride film (SiN) is formed over the entire surface of the transparent substrate SUB**1** processed in this manner.

[0152] The contact hole CH which exposes a portion of the area of the counter voltage signal line CCR over which the pixel electrode PX is not formed is formed in the protective film PAS by a selective etching method using a photolithographic technique.

[0153] At the same time, openings for exposing the terminals of the drain line DCR, the gate line GCR and the counter voltage signal line CCR are formed in a portion except the pixel area.

[0154] Step **6** (**FIG. 6F**)

[0155] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB**1**.

[0156] Then, the transparent conductive film is formed into a predetermined pattern by a selective etching method using a photolithographic technique, thereby forming the counter electrode CT.

[0157] The counter electrode CT is formed to be connected to the counter voltage signal line CCR through the contact hole CH and to be superposed on the pixel electrode PX. The counter electrode CT is formed of multiple stripe-shaped electrodes disposed to be extended in the y-direction of **FIG. 6F** and to be juxtaposed in the x-direction of **FIG. 6F**.

[0158] The method of manufacturing the liquid crystal display device constructed in this manner is completed by repeating five times the selective etching method using the

photolithographic technique, whereby it is possible to reduce the number of steps of the manufacturing process.

[0159] [Embodiment 5]

[0160] **FIGS. 7A** to **7F** are process diagrams showing another embodiment of the method of manufacturing the liquid crystal display device according to the present invention.

[0161] Step **1** (**FIG. 7A**)

[0162] The transparent substrate SUB1 is prepared, and a metal film made of, example, Cr is formed over the entire liquid-crystal-side surface of the transparent substrate SUB1, and the metal film is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0163] Thus, the gate line GCR and the counter voltage signal line CCR are formed.

[0164] Step **2** (**FIG. 7B**)

[0165] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1.

[0166] Then, the transparent conductive film and the metal film are formed into a predetermined pattern by a selective etching method using a photolithographic technique, thereby forming the counter electrode CT connected to the counter voltage signal line CCR.

[0167] Step **3** (**FIG. 7C**)

[0168] The insulating film GI made of, for example, a silicon nitride film (SiN) and the semiconductor layer AS made of amorphous silicon (a-Si) are sequentially formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0169] Incidentally, a high-concentration impurity layer for formation of a contact layer doped with an impurity made of, for example, phosphorus (P) is formed on the surface of the semiconductor layer AS.

[0170] Then, the semiconductor layer AS is formed into a predetermined pattern by a selective etching method using a photolithographic technique.

[0171] Step **4** (**FIG. 7D**)

[0172] In addition, a metal film made of, example, Cr is formed over the entire liquid-crystal-side surface of the transparent substrate SUB1.

[0173] Then, the metal film is formed into a predetermined pattern by a selective etching method using a photolithographic technique, thereby forming the drain line DCR and the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT.

[0174] After that, the high-concentration impurity layer formed on the surface of the semiconductor layer AS is etched by using as a mask the drain electrode SD2 and the source electrode SD1 of the thin film transistor TFT.

[0175] Step **5** (**FIG. 7E**)

[0176] The protective film PAS made of, for example, a silicon nitride film (SiN) is formed over the entire surface of the transparent substrate SUB1 processed in this manner.

[0177] The contact hole CH which exposes a portion of the source electrode SD1 of the thin film transistor TFT is formed in the protective film PAS by a selective etching method using a photolithographic technique.

[0178] At the same time, openings for exposing the terminals of the drain line DCR, the gate line GCR and the counter voltage signal line CCR are formed in a portion except the pixel area.

[0179] Step **6** (**FIG. 7F**)

[0180] A transparent conductive film made of, for example, ITO (Indium-Tin-Oxide) is formed over the entire surface of the transparent substrate SUB1.

[0181] Then, the transparent conductive film is formed into a predetermined pattern by a selective etching method using a photolithographic technique, thereby forming the pixel electrode PX.

[0182] The pixel electrode PX is formed to be connected to the source electrode SD1 of the thin film transistor TFT through the contact hole CH and to be superposed on the counter electrode CT.

[0183] Then, the pixel electrode PX is formed of multiple stripe-shaped electrodes disposed to be extended in the y-direction of **FIG. 7F** and to be juxtaposed in the x-direction of **FIG. 7F**.

[0184] [Other Embodiments]

[0185] Although the above-described embodiments have been referred to as representative examples, there are various other embodiments. Such various other embodiments as well as the above-described embodiments are listed in **FIG. 8**

[0186] The table of **FIG. 8** shows in list form layer structures each formed by the method of manufacturing the liquid crystal display device according to the present invention, the number of times of repetition of selective etching using a photolithographic technique, which selective etching is utilized for the manufacturing of each of the layer structures (the number of times of repetition of photolithography), and characteristic means which contributes to a reduction in the number of times of repetition of photolithography (means for reducing the number of times of repetition of photolithography).

[0187] In the table, the term "DCR/ASI bulk process" signifies the process of sequentially stacking the insulating film GI, the semiconductor layer AS and the metal layer and effecting selective etching of the metal layer and the underlying semiconductor layer AS in accordance with the same pattern and, at the same time, forming the drain electrode SD2 and the source electrode SD1 in an integrally interconnected state over the semiconductor layer AS in the area in which to form the thin film transistor TFT.

[0188] As described previously, the separation between the drain electrode SD2 and the source electrode SD1 can be effected by selective etching which is performed when the pixel electrode PX is being formed at a later step.

[0189] The term "PAS/SIN bulk process" signifies the process of forming the insulating film GI and further the protective film PAS thereon and then sequentially effecting selective etching of the protective film PAS and the insu-

lating film GI in each of areas in which to form the respective terminals of the signal lines, and, at the same time, forming openings such as contact holes in the protective film PAS if such openings need to be formed.

[0190] In **FIG. 8**, the respective manufacturing methods are denoted by No. **1** to No. **22**, and the manufacturing methods No. **4**, No. **6**, No. **11**, No. **13** and No. **14** correspond to the above-described Embodiments 1 to 5 shown in **FIGS. 3, 6, 7, 4** and **5**.

[0191] The respective layer structures of the pixel areas formed by the individual manufacturing methods are shown in FIGS. **9** to **21**. The number or numbers shown in each of the figures indicate the layer structure formed by the manufacturing method or methods denoted by the corresponding one or ones of the numbers shown in **FIG. 8**.

[0192] Incidentally, each of FIGS. **9** to **21** shows a cross-sectional view of the same portion of the pixel shown in **FIG. 1**.

[0193] As is apparent from the foregoing description, in accordance with the method of manufacturing the liquid crystal display device according to the present invention, it is possible to reduce the number of manufacturing steps.

What is claimed is:

1. A liquid crystal display device comprising:

a pair of opposing substrates, at least one of said pair of opposing substrates being transparent;

a plurality of pixel electrodes and a plurality of counter electrodes formed on one of the substrates, wherein the counter electrodes are arranged at a layer lower than that of the pixel electrodes with at least an insulating layer disposed therebetween; and

a connecting member arranged at a layer higher than that of the counter electrodes, the connecting member electrically connected to one of the counter electrodes and to a counter voltage signal line that is spaced apart from the counter electrodes.

2. A liquid crystal display device according to claim 1, wherein the connecting member is formed on the insulation layer, the device further comprising a first contact hole which connects the connecting member and one of the counter electrodes; and a second contact hole different from the first contact hole which connects the connecting member and the counter voltage signal line.

3. A liquid crystal display device according to claim 2, wherein the connecting member is disposed on the same layer as that of the pixel electrodes.

4. A liquid crystal display device according to claim 3, wherein the counter electrode and the pixel electrodes each is a transparent conductor material.

5. A liquid crystal display device according to claim 3, wherein the transparent conductor material is ITO (indium-ton-oxide).

6. A liquid crystal display device comprising:

a pair of opposing substrates, at least one of said pair of opposing substrates being transparent;

a plurality of pixel regions, each pixel region defined by a pixel electrode and a thin film transistor; and

three contact holes formed in each pixel region,

wherein a first of the three contact holes connects the pixel electrode and the thin film transistor, and a second and a third of the three contact holes each is connected to a common electrode.

7. A liquid crystal display device according to claim 6, further comprising a member disposed in the same layer as that of the pixel electrodes and spaced apart from the pixel electrodes, the member in contact with the common electrode at the second and third contact holes.

8. A liquid crystal display device according to claim 7, wherein the pixel electrode and the member each is transparent conductor material.

9. A liquid crystal display device according to claim 8, wherein the transparent conductor material is ITO.

10. A liquid crystal display device according to claim 8, wherein the common electrode is arranged at lower layer than that of the pixel electrode having at least an insulating layer disposed therebetween.

11. A liquid crystal display device according to claim 7, wherein both ends of the member connect with the common electrode through a contact hole.

12. A liquid crystal display device according to claim 11, wherein length of the member is less than the length of the pixel electrode.

13. A liquid crystal display device comprising:

a pair of opposing substrates, at least one of said pair of opposing substrates being transparent;

a pixel electrode and a thin film transistor formed in a pixel region;

a first conductive member and a second conductive member separated from the first conductive member, the first conductive member and the pixel electrode overlapping in a region with an insulating layer therebetween; and

a connecting member which connects the first conductive member and the second conductive member.

14. A liquid crystal display device according to claim 13, further comprising two contact holes in a pixel region to connect the conductive member.

15. A liquid crystal display device according to claim 14, wherein the connecting member is in the same layer as that of the pixel electrode.

16. A liquid crystal display device according to claim 15, wherein the first conductive member and the second conductive member each is absent any connection to a gate line and to a drain line.

17. A liquid crystal display device according to claim 16, wherein length of the connecting member is less than that of the pixel electrode.

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专利名称(译)	液晶显示器及其制造方法		
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摘要(译)

制造液晶显示装置的方法旨在减少制造步骤的数量。液晶显示装置被布置成使得在设置为彼此相对的一对基板中的一个基板的液晶侧表面上的每个像素区域中插入液晶，来自漏极线的信号被应用于像素电极，通过漏电极和源电极，形成在覆盖薄膜晶体管的半导体层的层中，通过从栅电极提供扫描信号，该栅电极相对于半导体定位为下层层。制造这种液晶显示装置的方法包括以下步骤：在用于形成漏极信号的区域和用于形成的区域中形成堆叠结构，其中半导体层和第一导电层以相同的图案顺序堆叠薄膜晶体管;在形成第二导电层之后，通过使用相同的掩模，在薄膜晶体管的漏电极和源电极之间提供分离，并且还形成连接到源电极的像素电极。