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(54) ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE AND THE FABRICATION METHOD OF THE SAME

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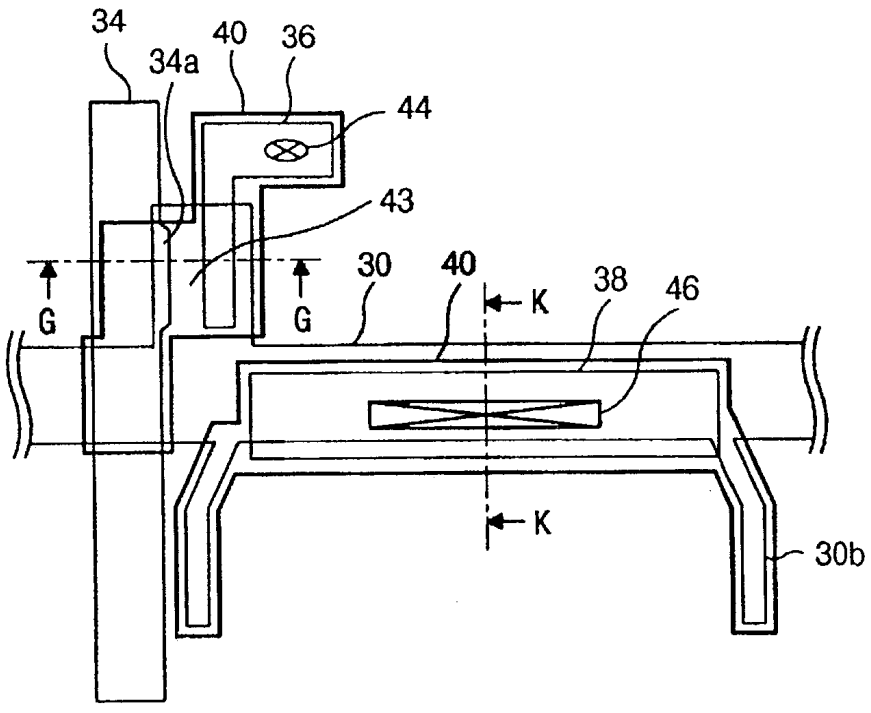
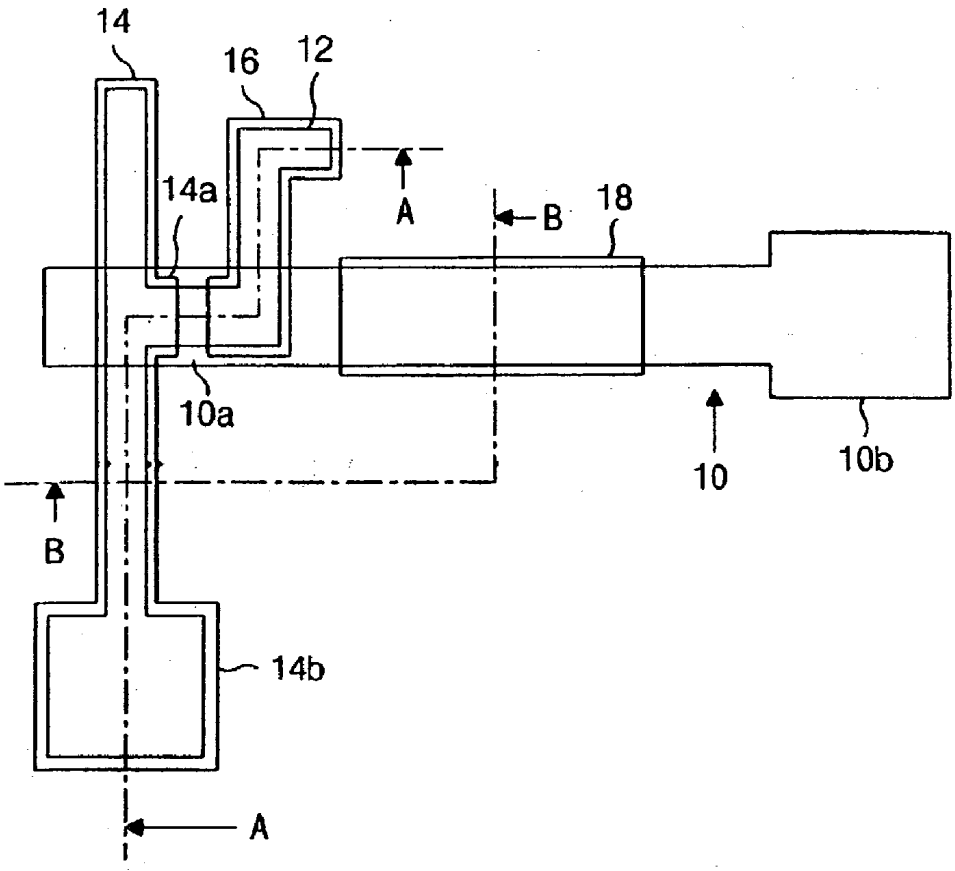
(57) **ABSTRACT**

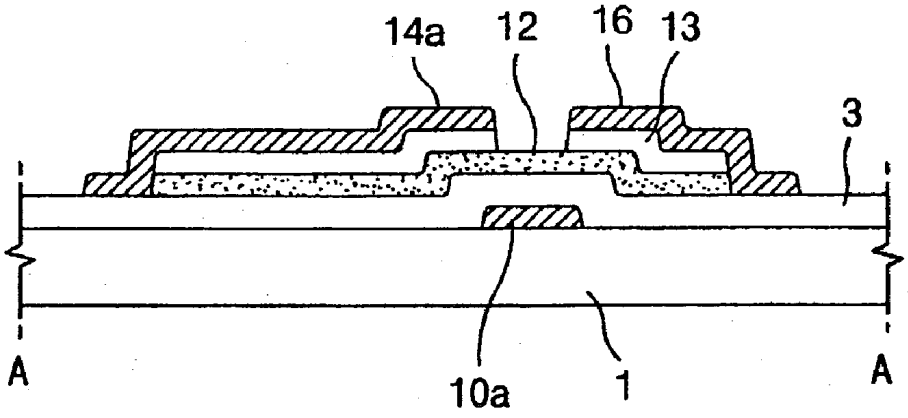
The present invention discloses a four-mask method of manufacturing an array substrate of a liquid crystal display device and the liquid crystal display device having the same array substrate. The method includes forming a plurality of gate lines, gate electrodes and gate extension lines by depositing a first metallic material on a substrate and patterning the first metallic material with a first mask, the gate extension lines extending toward the opposite direction of the gate electrodes; forming a first insulating layer on the whole surface having gate lines, gate electrodes, and gate extension lines; forming a plurality of data lines, source electrodes, drain electrodes, and capacitor electrodes over the gate lines by depositing a semiconductor layer, an ohmic contact layer and a second metallic material sequentially on the first insulating layer, and patterning the second metallic material and the ohmic contact layer with a second mask; forming a passivation layer and a plurality of first and second contact holes by depositing a second insulating layer on the data lines, the source electrodes, the drain electrodes and the capacitor electrodes, and patterning the second insulating layer with a third mask, the first contact holes exposing a portion of the drain electrode, the second contact holes exposing a portion of the capacitor electrodes; and forming a plurality of pixel electrodes by depositing a transparent conductive layer on the passivation layer, and patterning the transparent conductive layer by a fourth mask, the pixel electrodes contacting the drain electrodes through the first contact holes and contacting the capacitor electrodes through the second contact holes.





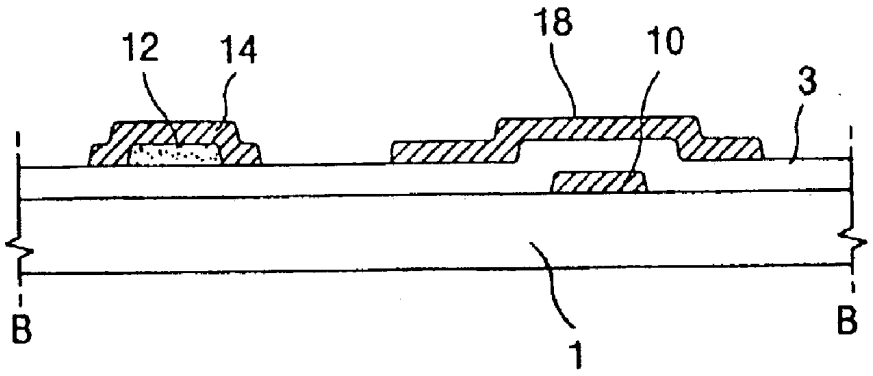
(related art)

FIG. 1



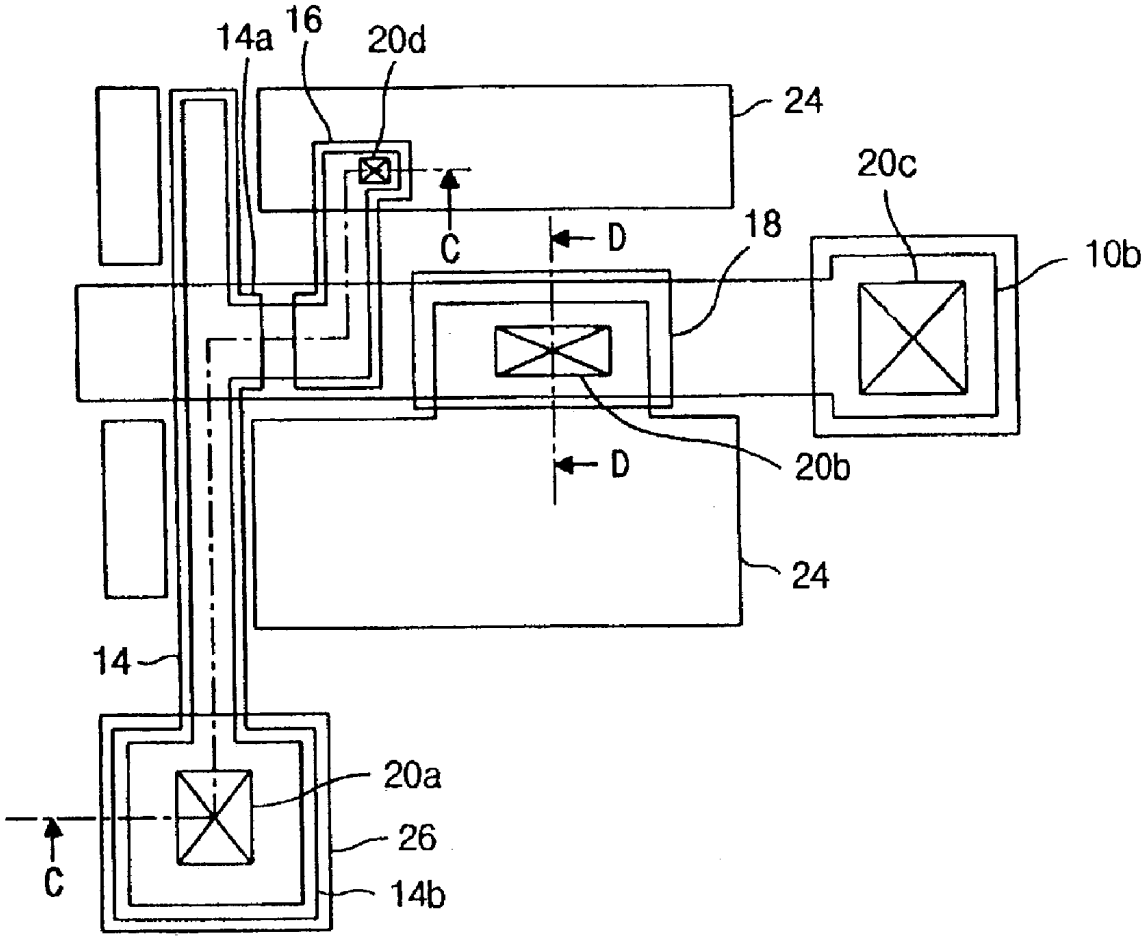
(related art)

FIG. 2A



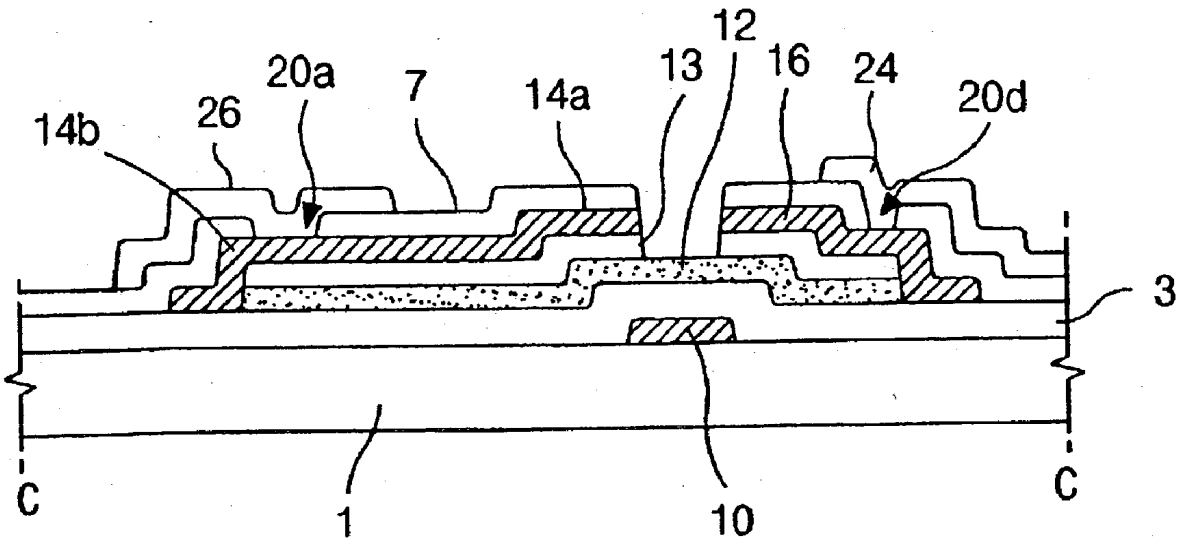
(related art)

FIG. 2B



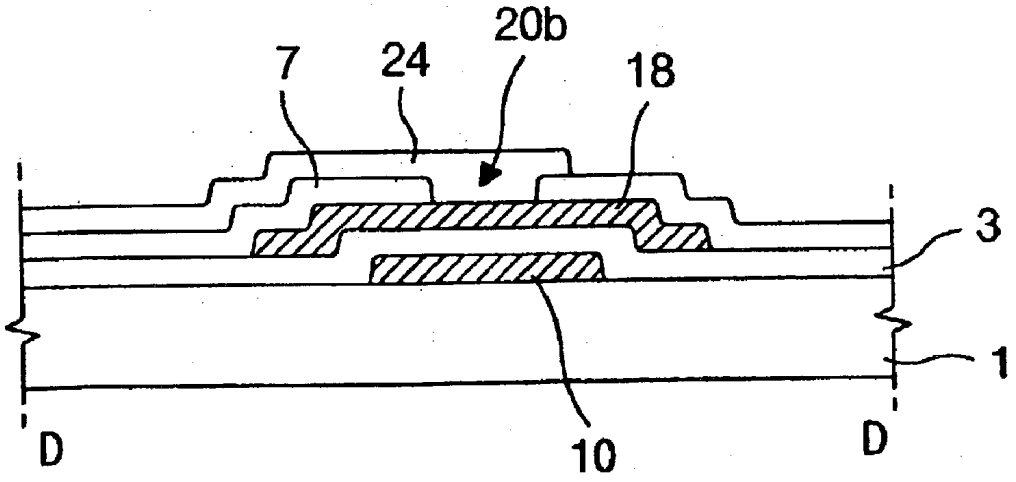
(related art)

FIG. 3



(related art)

FIG. 4A



(related art)

FIG. 4B

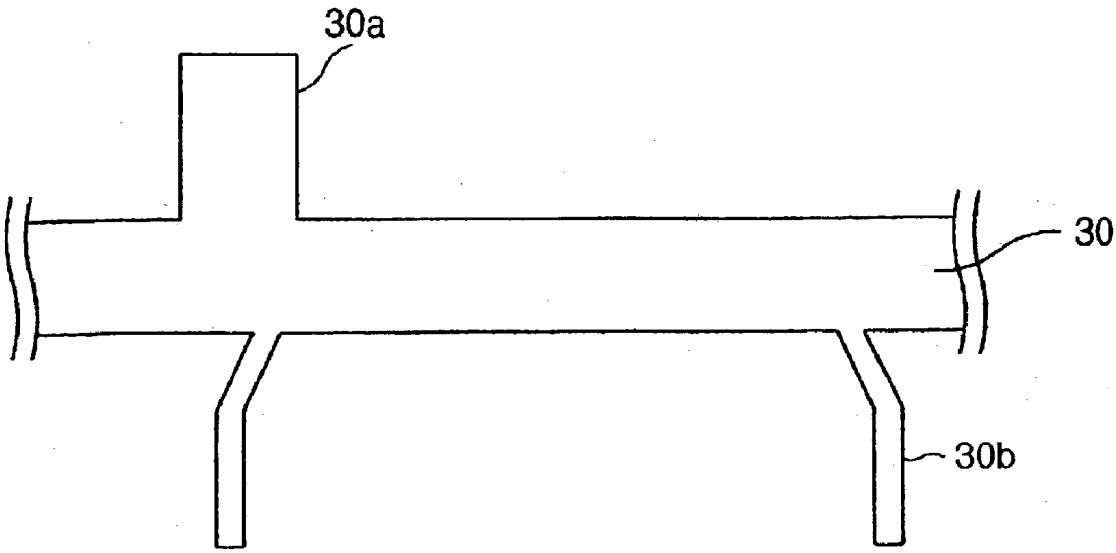


FIG. 5A

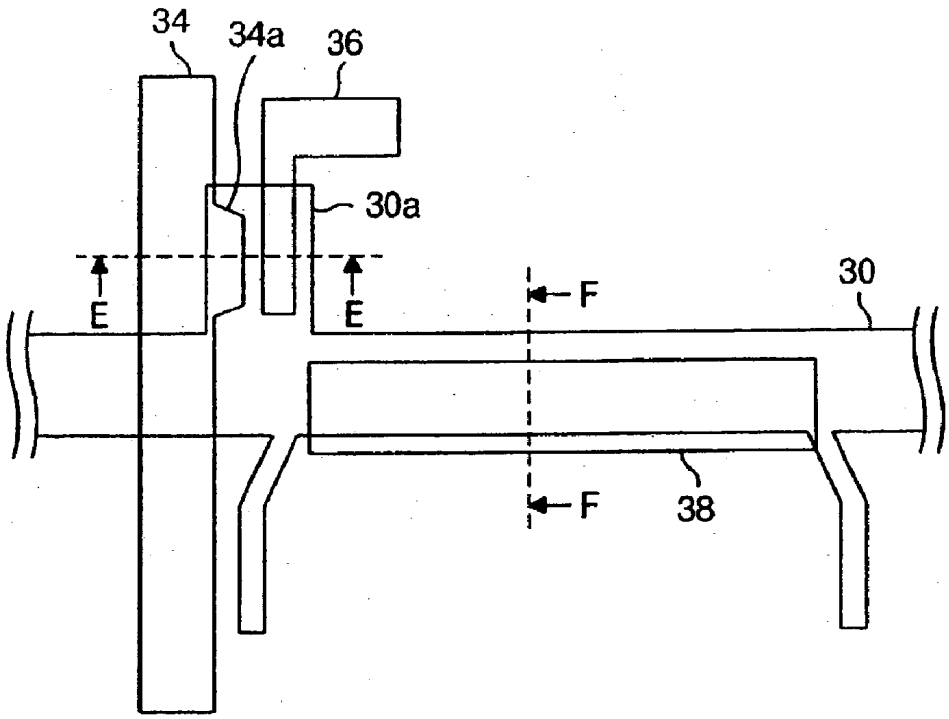


FIG. 5B

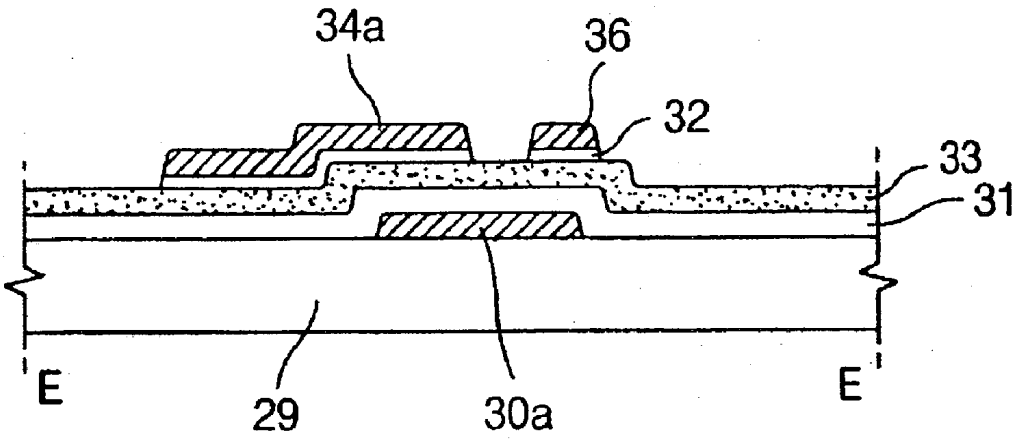


FIG. 6A

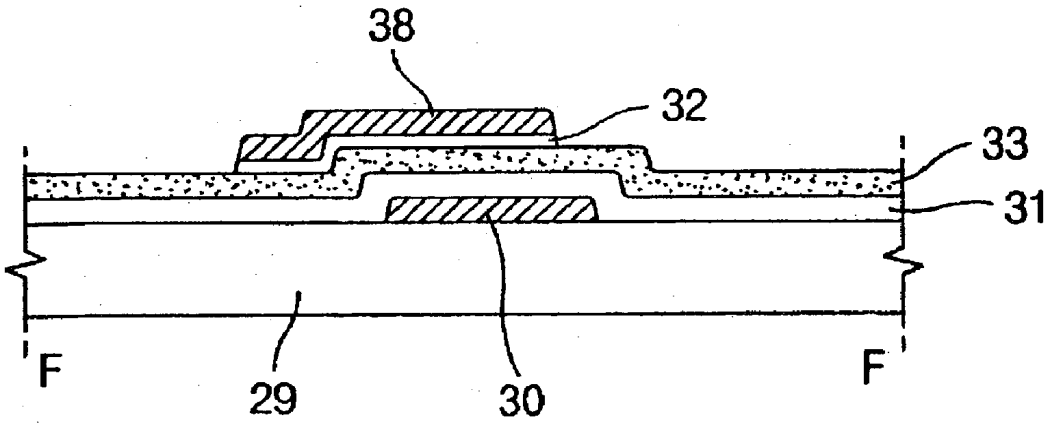


FIG. 6B

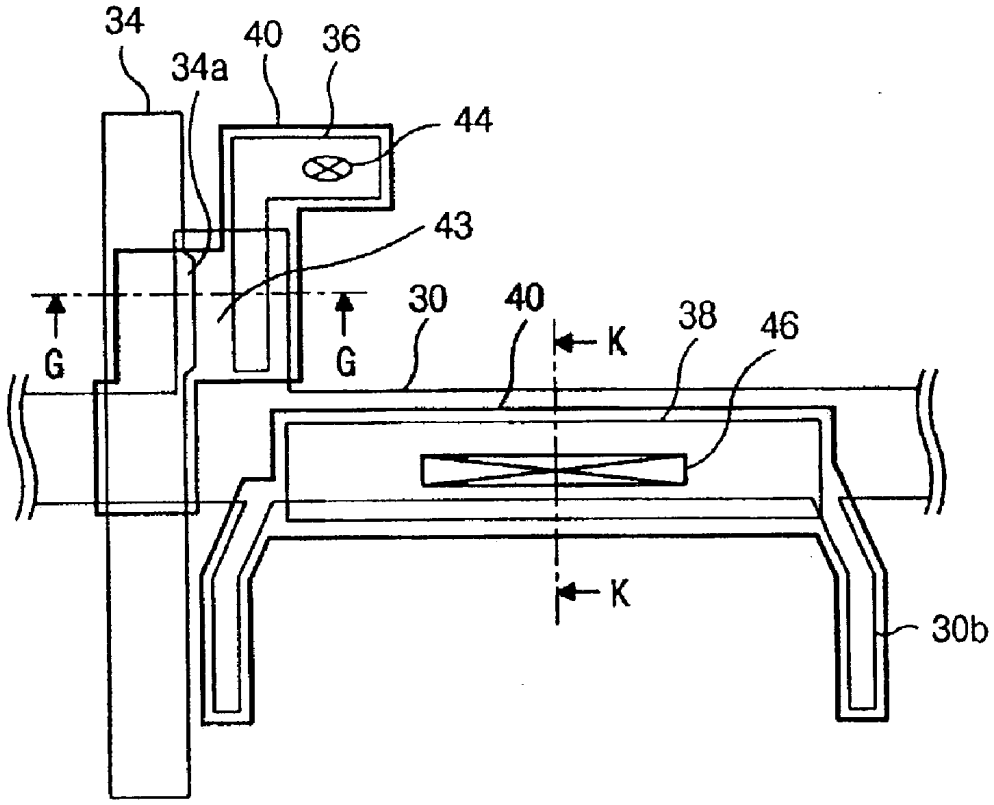

34
34a
40
36
44
43
G
G
30
40
K
38
46
K
30b

FIG. 7

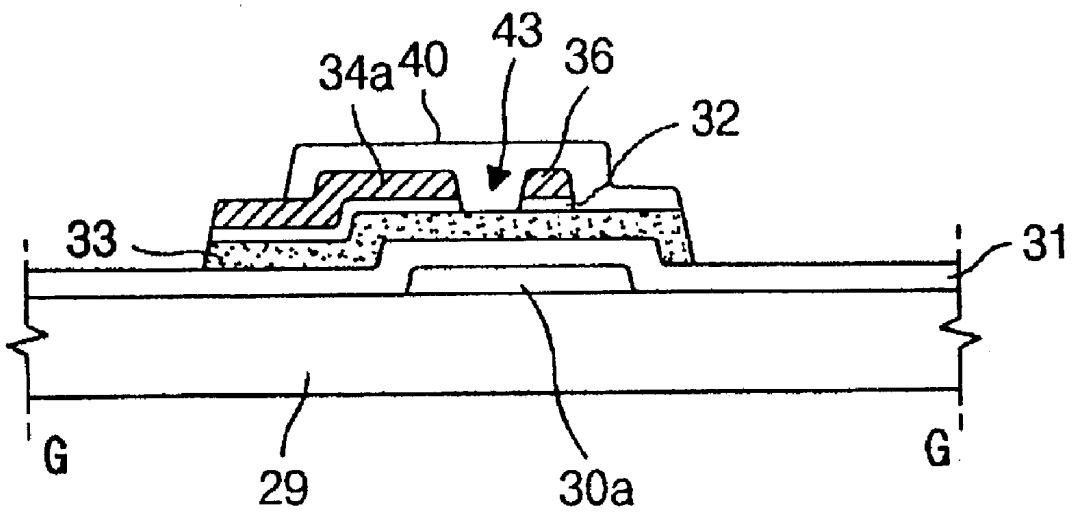

43
34a
40
36
32
33
31
G
29
30a
G

FIG. 8A

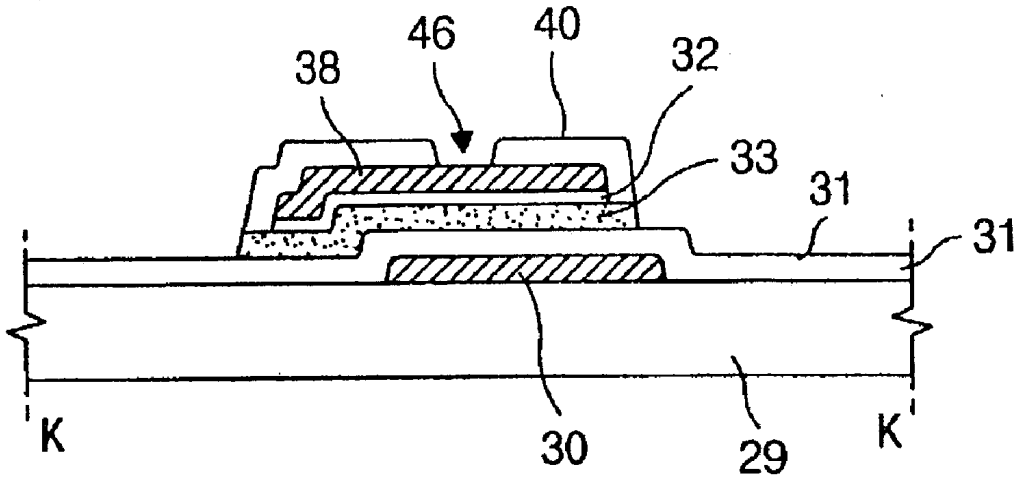

46
40
38
32
33
31
31
K
30
29
K

FIG. 8B

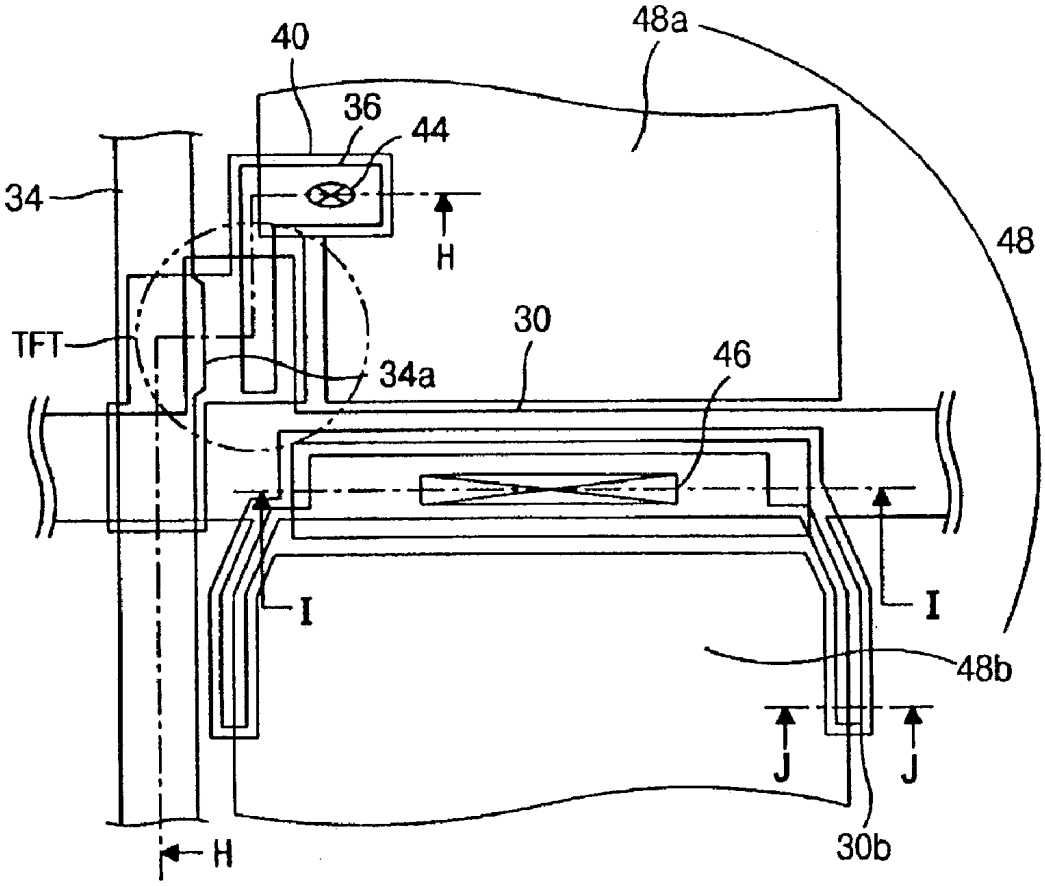

40
48a
36
44
34
H
48
TFT
30
34a
46
I
I
48b
J
J
H
30b

FIG. 9

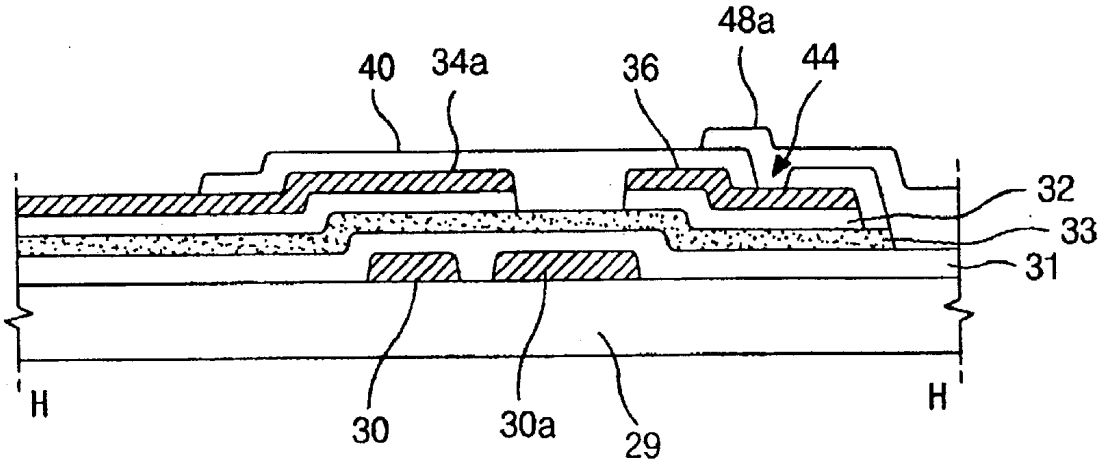


FIG. 10A

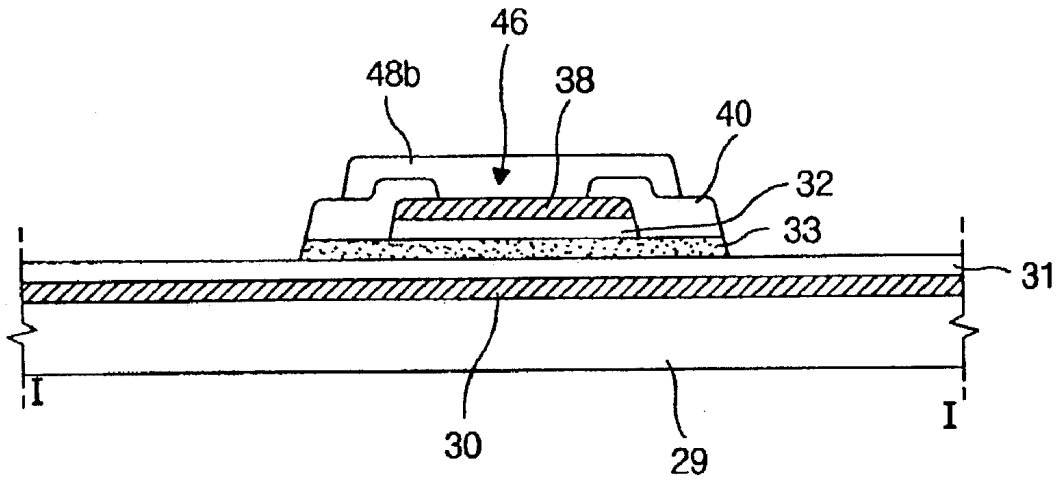


FIG. 10B

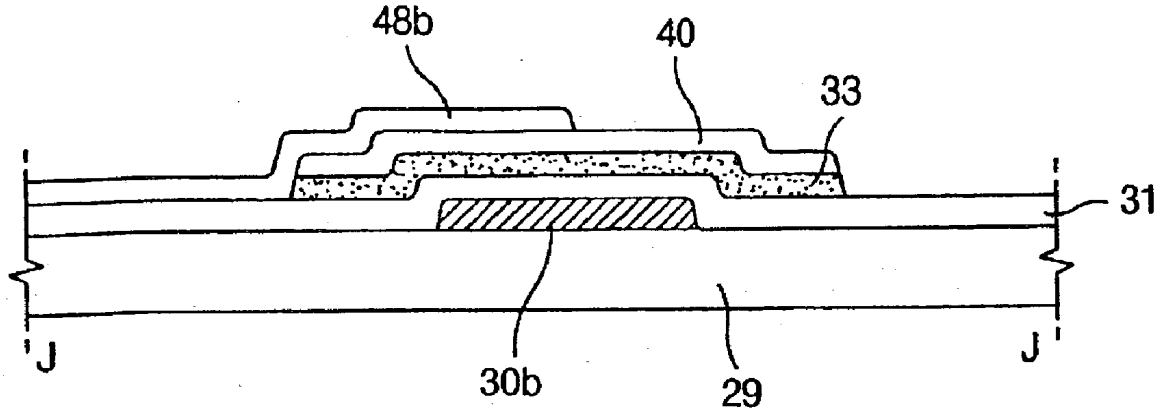


FIG. 10C

ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE AND THE FABRICATION METHOD OF THE SAME

[0001] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

CROSS REFERENCE

[0002] This application claims the benefit of Korean Patent Application No. 1999-0038016, filed on Sep. 8, 1999, under 35 U.S.C. §119, the entirety of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] The present invention relates to a liquid crystal display (LCD) device and a method of fabricating the LCD device, and more particularly, to an array substrate having thin film transistors for the liquid crystal display device and the method of fabricating the array substrate.

[0005] 2. Description of Related Art

[0006] Recently, according to a rapid development in a thin-film-transistor addressed liquid crystal display device (TFT/LCD, hereinafter noted simply as a liquid crystal display device), various portable electric appliances adopt the liquid crystal display device due to its advantage in a light weight and a wide applicability. Thus, an improved manufacturing process technology of the liquid crystal display device becomes required for a cheaper production cost and a higher productivity.

[0007] The liquid crystal display device manufacturing process requires repeated steps of depositing and patterning of various layers. The patterning step adopts a photolithography mask step including a light exposing with a mask. Since one cycle of the photolithography step is facilitated with one mask, the number of masks used in the fabrication process is a critical factor in determining the number of patterning steps. Namely, the production cost substantially depends on the number of masks used in the manufacturing process.

[0008] Now, referring to the attached drawings, a conventional array substrate of the liquid crystal display device manufactured by a conventional method is explained in detail. For convenience of explanation, the attached drawings of plan views do not illustrate insulating layers interposed between metal films, but the insulating layers are shown in the cross-sectional views.

[0009] In **FIGS. 1, 2A** and 2B, on a transparent insulating substrate **1**, a gate line **10** is horizontally formed with a data line **14** formed perpendicular to the gate line **10**. Near a cross point between the gate and data lines **10** and **14**, a portion of the gate line **10** is protruded as a gate electrode **10***a*, and, at one end of the gate line **10**, a gate pad **10***b* is positioned. Further, near the cross point between the gate and data lines **10** and **14**, a source electrode **14***a* is protruded from the data line **14**, and, spaced apart from the source electrode **14***a*, a drain electrode **16** is formed. Also at one end of the data line **14**, a data pad **14***b* is positioned.

[0010] Herein, in the same layer of the data line **14**, between the drain electrode **16** and the gate pad **10***b*, a capacitor electrode **18** of the same material as the data line **14** is formed in shape of an island. The capacitor electrode **18** overlaps a corresponding portion of the gate line **10** so that the capacitor electrode **18** makes a storage capacitor together with the corresponding overlapped portion of the gate line **10**.

[0011] **FIGS. 2A and 2B** illustrate cross-sections taken along lines "A-A" and "B-B" of **FIG. 1**, respectively. As shown in **FIGS. 2A and 2B**, a conductive metal layer is deposited on a surface of the substrate **1**, and patterned with a first mask so as to form the gate line **10** including the gate electrode **10***a* and the gate pad **10***b*.

[0012] On the whole surface including the gate lines of the substrate **1**, an insulating material, a semiconductor material, and a doped semiconductor material are sequentially deposited, and patterned with a second mask so as to form a first insulating layer **3**, a semiconductor layer **12**, and an ohmic contact layer **13**.

[0013] Next, another conductive metallic material is deposited on the whole surface including the ohmic contact layer **13** of the substrate **1**, and thereafter the metal layer and the ohmic contact layer **13** are patterned with a third mask so that the source, drain and capacitor electrodes **14***a*, **16** and **18** are formed. At this point, between the source and drain electrodes **14***a* and **16**, a back channel is opened so as to expose a portion of the semiconductor layer **12**.

[0014] **FIGS. 3, 4A** and 4B illustrate a completed array substrate for the liquid crystal display device.

[0015] On the whole surface including the patterned metal layer of **FIG. 2, a** second insulating layer **7** shown in **FIGS. 4A and 4B** is deposited, and patterned with a fourth mask so as to form a first to a fourth contact holes **20***a*, **20***b*, **20***c*, and **20***d*. The first contact hole **20***a* exposes a portion of the data pad **14***b*; the second contact hole **20***b* exposes a portion of the capacitor electrode **18**; the third contact hole **20***c* exposes a portion of the gate pad **10***b*; and the fourth contact hole **20***d* exposes a portion of the drain electrode **16**. Via the data and gate pads **14***b* and **16**, an outer circuit transmits data and gate signals, respectively.

[0016] On the whole surface including the second insulating layer **7**, an indium tin oxide (ITO) layer is deposited and patterned so as to form a pixel electrode **24** and a data pad terminal **26**; the data pad terminal contacts with the data pad **14***b* through the first contact hole **20***a*.

[0017] Further, a portion of the pixel electrode **24** is electrically connected with the capacitor electrode **18** through the second contact hole **20***b*; another portion of the pixel electrode **24** is electrically connected with the drain electrode **16** through the fourth contact hole **20***d*.

[0018] At this point, the capacitor electrode **18**, electrically connected with the pixel electrode **24** through the second contact hole **20***b* of **FIG. 3**, plays a role of an electrode of the storage capacitor; the overlapped portion of the gate line **10** under the capacitor electrode **18** plays a role of the other electrode of the storage capacitor.

[0019] Since the above-described conventional method of manufacturing the array substrate of the liquid crystal display device employs too many masks, the method has a disadvantage of too many-repeated photolithography steps, which results in high production cost and inferiority percentage.

SUMMARY OF THE INVENTION

[0020] In view of the foregoing and other problems of the conventional manufacturing method of the liquid crystal display device, it is an object of the present invention to provide a relatively low cost manufacturing method of the array substrate for the liquid crystal display device.

[0021] It is another object of the present invention to provide an improved array substrate for the liquid crystal display device manufactured by the above-mentioned method.

[0022] To achieve the above-mentioned objects, the present invention provides a four-mask method of manufacturing an array substrate of a liquid crystal display device and an array substrate fabricated by the method. The method includes forming a plurality of gate lines, gate electrodes and gate extension lines by depositing a first metallic material on a substrate and patterning the first metallic material with a first mask, the gate extension lines extending toward the opposite direction of the gate electrodes; forming a first insulating layer on the whole surface having gate lines, gate electrodes, and gate extension lines; forming a plurality of data lines, source electrodes, drain electrodes, and capacitor electrodes over the gate lines by depositing a semiconductor layer, an ohmic contact layer and a second metallic material sequentially on the first insulating layer, and patterning the second metallic material and the ohmic contact layer with a second mask; forming a passivation layer and a plurality of first and second contact holes by depositing a second insulating layer on the data lines, the source electrodes, the drain electrodes and the capacitor electrodes, and patterning the second insulating layer with a third mask, the first contact holes exposing a portion of the drain electrode, the second contact holes exposing a portion of the capacitor electrodes; and forming a plurality of pixel electrodes by depositing a transparent conductive layer on the passivation layer, and patterning the transparent conductive layer by a fourth mask, the pixel electrodes contacting the drain electrodes through the first contact holes and contacting the capacitor electrodes through the second contact holes.

[0023] The foregoing and other objectives of the present invention will become more apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

[0025] **FIG. 1** is a schematic plan view illustrating source and drain electrodes formed on an array substrate according to a conventional manufacturing method;

[0026] **FIG. 2A** is a cross-sectional view taken along the line "A-A" of **FIG. 1**;

[0027] **FIG. 2B** is a cross-sectional view taken along the line "B-B" of **FIG. 1**;

[0028] **FIG. 3** is a plan view illustrating a completed array substrate according to the conventional manufacturing method;

[0029] **FIG. 4A** is a cross-sectional view taken along the line "C-C" of **FIG. 3**;

[0030] **FIG. 4B** is a cross-sectional view taken along the line "D-D" of **FIG. 3**;

[0031] **FIG. 5A** is a plan view illustrating an array substrate formed by a first mask according to an embodiment of the present invention;

[0032] **FIG. 5B** is a plan view illustrating an array substrate formed by a second mask according to an embodiment of the present invention;

[0033] **FIG. 6A** is a cross-sectional view taken along the line "E-E" of **FIG. 5B**;

[0034] **FIG. 6B** is a cross-sectional view taken along the line "F-F" of **FIG. 5B**;

[0035] **FIG. 7** is a plan view illustrating an array substrate formed by a third mask according to an embodiment of the present invention;

[0036] **FIG. 8A** is a cross-sectional view taken along the line "G-G" of **FIG. 7**;

[0037] **FIG. 8B** is a cross-sectional view taken along the line "K-K" of **FIG. 7**;

[0038] **FIG. 9** is a plan view illustrating an array substrate formed by a fourth mask according to an embodiment of the present invention;

[0039] **FIG. 10A** is a cross-sectional view taken along the line "H-H" of **FIG. 9**;

[0040] **FIG. 10B** is a cross-sectional view taken along the line "I-I" of **FIG. 9**; and

[0041] **FIG. 10C** is a cross-sectional view taken along the line "J-J" of **FIG. 9**.

DETAILED DESCRIPTION OF PREFFERED EMBODIMENTS

[0042] Referring now to the drawings, and more particularly to **FIGS. 5A** to **10**C, a preferred embodiment of the present invention will be described.

[0043] **FIG. 5A** illustrates a gate line formed with a first mask according to the preferred embodiment of the present invention.

[0044] In order to form the gate line **30** including a gate electrode **30***a* which is perpendicularly extended from a portion of the gate line **30**, a first metallic material is deposited on a surface of a substrate (shown in **FIG. 6A**), and patterned by the first mask. The gate line **30** also has a couple of gate extension lines **30***b* spaced apart from each

other and extended toward an opposite direction of the gate electrode **30***a*, and each of the gate extension lines **30***b* is formed near corresponding data line **34** and extended substantially parallel to the data line **34**. The gate extension lines **30***b* serve to expand the capacity of a storage capacitor, which will be explained later in detail. Between the gate extension lines **30***b*, a pixel electrode will be located in a later step. The first metallic material is selected from a group consisting of molybdenum (Mo) and Chromium (Cr).

[**0045**] On the whole surface having the above-mentioned gate line **30** of the substrate, a first insulating material (not shown) is deposited. The first insulating material is made of silicon nitride (SiNx) or silicon oxide (SiO2); especially silicon nitride is widely used for the first insulating material.

[**0046**] Next, as shown in **FIGS. 5B, 6A** and 6B, a semiconductor material, a doped semiconductor material and a second metallic material are sequentially deposited on the first insulating layer **31** of the substrate **29**; the doped semiconductor layer and the second metal film are patterned with a second mask so as to form a data line **34**, a source electrode **34***a*, a drain electrode **36**, a capacitor electrode **38**, a semiconductor layer **33**, and an ohmic contact layer **32**. The second metallic material is selected from a group consisting of molybdenum (Mo), and chromium (Cr); the semiconductor material is an amorphous silicon; and the doped semiconductor material is a doped amorphous silicon.

[**0047**] In **FIG. 5**B, the data line **34** is arranged perpendicular to the gate line **30**; the source electrode **34***a* is protruded from the data line **34** near the cross point between the gate and data lines **30** and **34**; the drain electrode **36**, in the shape of an island, is formed spaced apart from the source electrode **34***a*. The source and the drain electrodes **34***a* and **36** overlap a portion of the gate electrode **30***a*; and a capacitor electrode **38**, in the shape of another island longitudinally parallel to the gate line **30**, is formed spaced apart from the data line **34**, and overlaps a portion of the gate line **30**.

[**0048**] Referring to **FIGS. 6A and 6B**, a more detailed description about the above-mentioned structure will be followed; **FIGS. 6A and 6B** illustrate cross-sections taken along lines "E-E" and "F-F" of **FIG. 5**B, respectively.

[**0049**] As mentioned previously, on the insulating layer **31**, the semiconductor material, the doped semiconductor material, and the second metallic material are sequentially deposited; the doped semiconductor layer and the second metal film are patterned with the second mask.

[**0050**] In the conventional five-mask method of manufacturing the conventional liquid crystal display device, after the semiconductor layer and the doped semiconductor layer are patterned with the conventional second mask, the second metallic material is deposited, and patterned with the conventional third mask. But, in the four-mask method of manufacturing the liquid crystal display device according to the embodiment of the present invention, all of the semiconductor material, the doped semiconductor material, and the second metallic material are sequentially deposited, and thereafter the doped semiconductor layer and the second metal film are patterned with the second mask. The semiconductor layer will be patterned with another mask in a later step.

[**0051**] Accordingly, since the conventional second mask is excluded, the number of masks decreases by one.

[**0052**] **FIGS. 7, 8A** and 8B illustrate the array substrate formed just after a third mask step.

[**0053**] A second insulating material is deposited over the whole surface including the patterned second metal film, and patterned with the third mask so as to form a passivation film **40**, and first and second contact holes **44** and **46**.

[**0054**] For the sake of protection, the passivation film **40** covers a portion of the gate line **30**, the gate extension lines **30***b*, the source and drain electrodes **34***a* and **36**, a portion of the data line **34**, the capacitor electrode **38**, and a back channel **43** that is defined between the source and drain electrodes **34***a* and **36**.

[**0055**] The first and the second contact holes **44** and **46** expose a portion of the drain and the source electrodes **36** and **38**, respectively.

[**0056**] **FIGS. 9, 10A**, **10**B and **10**C illustrate the array substrate formed just after a fourth mask step.

[**0057**] As shown in **FIG. 9, a** transparent conductive material is deposited on the whole surface including the passivation layer **40**, and patterned with the fourth mask so as to form a pixel electrode **48** that is electrically connected with the drain electrode **36** through the first contact hole **44**, and with the capacitor electrode **38** through the second contact hole **46**. The pixel electrode **48** partially overlaps the gate extension lines **30***b*. The array substrate of the invention is for an active matrix type liquid crystal display, and thus the first and second pixel electrodes **48***a* and **48***b* are shown. In **FIG. 9**, The second pixel electrode **48***b*, which is not electrically connected with the "TFT", overlaps the gate line **30** included in the "TFT" as in the conventional art.

[**0058**] As shown in **FIG. 10**A, the first pixel electrode **48***a* contacts with the drain electrode **36** through the first contact hole **44**.

[**0059**] The pixel electrode **48** not only applies an electric field to the liquid crystal but also plays a role of an electrode of the storage capacitor. That is to say, the second pixel electrode **48***b* is electrically connected with the capacitor electrode **38** that plays the role of one electrode of the storage capacitor. The storage-electrode-overlapping portion of the gate line **30** plays the role of the other electrode of the storage capacitor.

[**0060**] **FIGS. 10B and 10C** illustrate the two different cross-sections of the storage capacitor. As shown in **FIG. 10**1B, at the capacitor electrode **38**, the transparent conductive material of the second pixel electrode **48***b* fills the second contact hole **46** so as to connect the capacitor electrode **38** and the pixel electrode **48***b* electrically. On the substrate **1**, the gate line **30**, the first insulating layer **31**, the semiconductor layer **33**, the ohmic contact layer **32**, the capacitor electrode **38**, the passivation film **40**, and the pixel electrode **48** are formed sequentially.

[**0061**] Comparing with the conventional storage capacitor, since the semiconductor layer **31** is not patterned before this fourth mask step, and the ohmic contact layer **32** is patterned together with the capacitor electrode **38**, portions of the semiconductor layer **31** and the ohmic contact layer **32** are included in the storage capacitor according to the embodiment of the present invention. The elongated vertical distance between the storage-electrode-overlapping portion of the gate electrode **30** and the capacitor electrode **38**

decreases the capacity of the storage capacitor. But, since an expanded portion of the storage capacitor including the gate extension lines **30***b*, the corresponding covering portion of the passivation layer **40**, and the corresponding overlapping portion of the second pixel electrode **48***b* compensates for the decrease in the capacity of the storage capacitor, the total capacity of the storage capacitor increases so as to improve the display quality of the liquid crystal display device.

[**0062**] **FIG. 10C** shows the cross-sectional structure of the expanded portion of the storage capacitor.

[**0063**] As shown in **FIG. 10**C, on the substrate **1**, the gate-extension line **30***b*, the first insulating layer **31**, the semiconductor layer **33**, the passivation film **40**, and the second pixel electrode portion **48***b* are formed sequentially.

What is claimed is:

1. A method of fabricating an array substrate for an active matrix type liquid crystal display device, the method comprising:

a) forming a plurality of gate lines and gate electrodes by depositing a first metallic material on a substrate and patterning the first metallic material with a first mask;

b) forming a first insulating layer on the whole surface having gate lines and gate electrodes;

c) forming a plurality of data lines, source electrodes, drain electrodes, and capacitor electrodes over the gate lines by depositing a semiconductor layer, an ohmic contact layer and a second metallic material sequentially on the first insulating layer, and patterning the second metallic material and the ohmic contact layer with a second mask;

d) forming a passivation layer and a plurality of first and second contact holes by depositing a second insulating, layer on the data lines, the source electrodes, the drain electrodes and the capacitor electrodes, and patterning the second

insulating layer with a third mask, the first contact holes exposing a portion of the drain electrode, the second contact holes exposing a portion of the capacitor electrodes; and

e) forming a plurality of pixel electrodes by depositing a transparent conductive layer on the passivation layer, and patterning the transparent conductive layer by a fourth mask, the pixel electrodes contacting the drain electrodes through the first contact holes and contacting the capacitor electrodes through the second contact holes.

2. The method according to claim 1, wherein, in patterning with the first mask, a plurality of gate extension lines extended from the gate lines substantially parallel to the data lines are further formed, in patterning with the third mask, the passivation layer covers the extension lines, and the pixel electrodes overlap the gate extension lines.

3. The method according to claim 1, wherein the transparent conductive layer is selected from a group consisting of indium tin oxide and indium zinc oxide.

4. The method according to claim 1, wherein the semiconductor layer is an amorphous silicon layer.

5. An array substrate for a liquid crystal display device, the array substrate manufactured by the method according to claim 1.

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专利名称(译)	用于液晶显示装置的阵列基板及其制造方法		
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摘要(译)

本发明公开了一种制造液晶显示装置的阵列基板的四掩模方法和具有该阵列基板的液晶显示装置。该方法包括通过在基板上沉积第一金属材料并用第一掩模图案化第一金属材料来形成多条栅极线，栅电极和栅极延伸线，栅极延伸线朝向栅电极的相反方向延伸;在整个表面上形成具有栅极线，栅极和栅极延伸线的第一绝缘层;通过在第一层上依次沉积半导体层，欧姆接触层和第二金属材料，在栅极线上形成多条数据线，源电极，漏电极和电容器电极绝缘层，并用第二掩模图案化第二金属材料和欧姆接触层;通过在数据线，源电极，漏电极和电容器电极上沉积第二绝缘层，并用第三掩模图案化第二绝缘层，形成钝化层和多个第一和第二接触孔，第一接触孔暴露出一部分漏电极，第二接触孔暴露出一部分电容电极;通过在所述钝化层上沉积透明导电层，并通过第四掩模对所述透明导电层进行图案化，形成多个像素电极，所述像素电极通过所述第一接触孔与所述漏电极接触，并通过所述第二接触孔与所述电容电极接触接触孔。