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Nakamura et al.

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(45) **Date of Patent: Feb. 5, 2013**

(54) **LIQUID CRYSTAL DISPLAY DEVICE**

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(73) Assignee: **Casio Computer Co., Ltd.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 741 days.

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(22) Filed: **Mar. 19, 2009**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
G09G 3/36 (2006.01)
G02F 1/133 (2006.01)
G02F 1/1343 (2006.01)

(52) **U.S. Cl.** **345/87**; 349/34; 349/143; 345/89; 345/98

(58) **Field of Classification Search** 345/84, 345/87, 89, 98–100, 211; 349/34, 38, 43, 349/48, 89, 114, 143, 129, 139; 257/72; 330/255; 365/205
See application file for complete search history.

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Assistant Examiner — Lin Li
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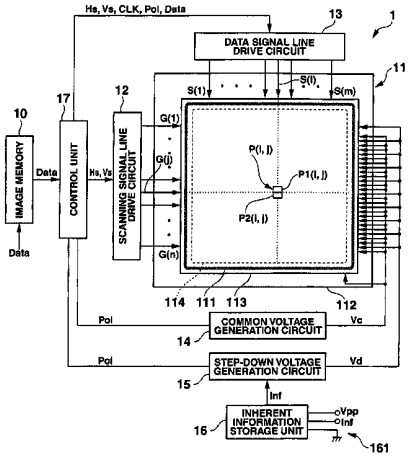
(57) **ABSTRACT**

A liquid crystal display device with multiple pixels includes a first sub-pixel including, a first liquid crystal capacitance between a common electrode and a first pixel electrode, and a first auxiliary capacitance between the first pixel electrode and a first auxiliary capacitance electrode; a second sub-pixel including, a second liquid crystal capacitance between the common electrode and a second pixel electrode, a second auxiliary capacitance between the second pixel electrode and a second auxiliary capacitance electrode, and a step-down capacitance between the second pixel electrode and a step-down capacitance electrode; a first voltage application unit for applying a common first voltage to the common electrode, the first auxiliary capacitance electrode, and the second auxiliary capacitance electrode; and a second voltage application unit for applying a second voltage, which is different from the first voltage, to the step-down capacitance electrode.

14 Claims, 17 Drawing Sheets



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JP	2007-156379	A	6/2007
JP	2007/065832	*	8/2007
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WO	PCT/JP2007/065832	*	8/2007
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FIG.1

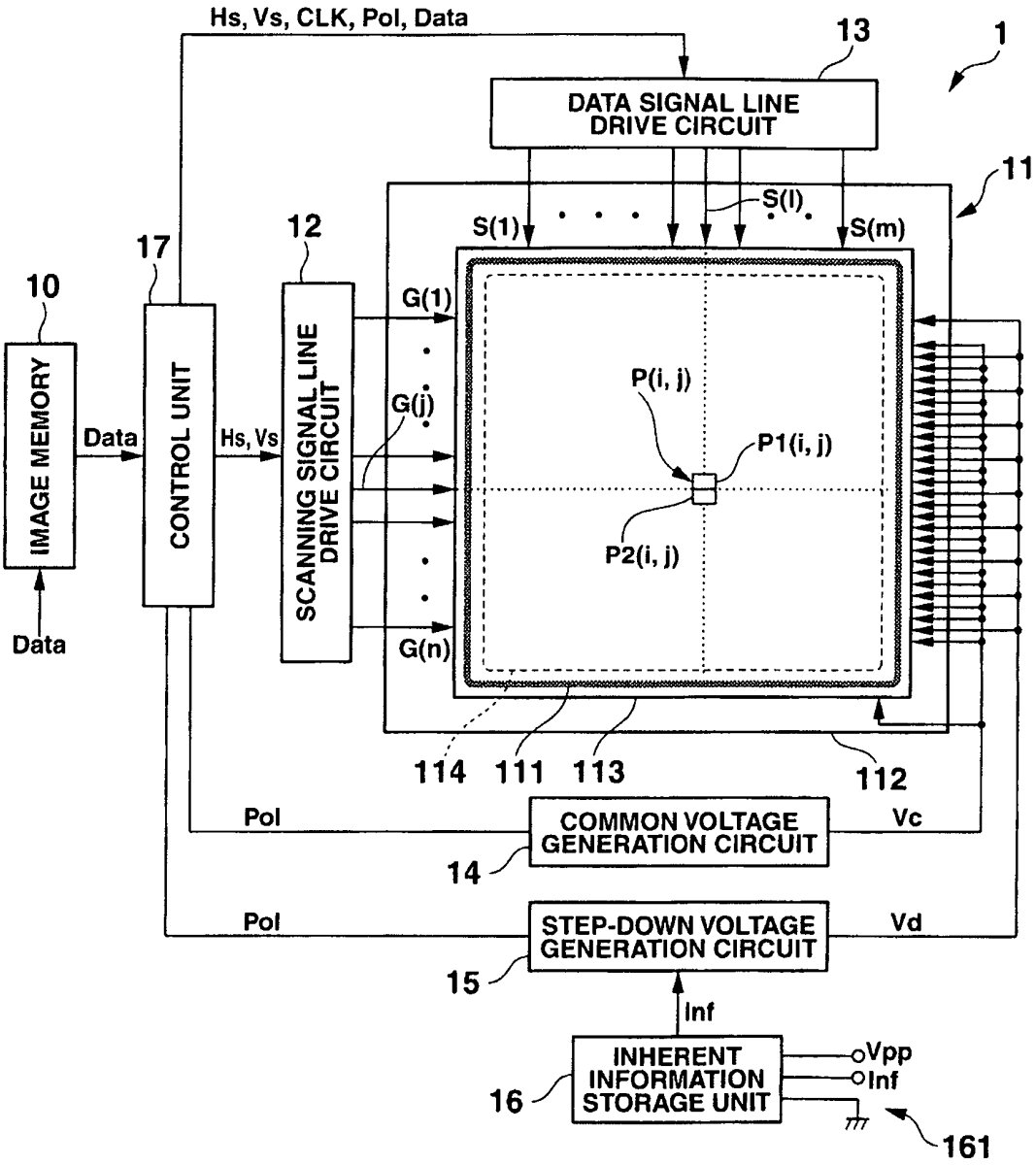

Hs, Vs, CLK, Pol, Data
13
1
DATA SIGNAL LINE DRIVE CIRCUIT
11
S(1)
S(l)
S(m)
12
17
10
G(1)
G(j)
G(n)
P(i, j)
P1(i, j)
P2(i, j)
IMAGE MEMORY
Data
CONTROL UNIT
Hs, Vs
SCANNING SIGNAL LINE DRIVE CIRCUIT
Data
114
111
113
112
Pol
COMMON VOLTAGE GENERATION CIRCUIT
Vc
14
Pol
STEP-DOWN VOLTAGE GENERATION CIRCUIT
Vd
15
Inf
INHERENT INFORMATION STORAGE UNIT
Vpp
Inf
16
161

FIG.2

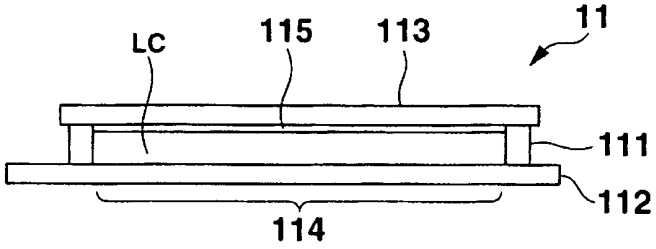

LC
115
113
11
111
112
114

FIG.3

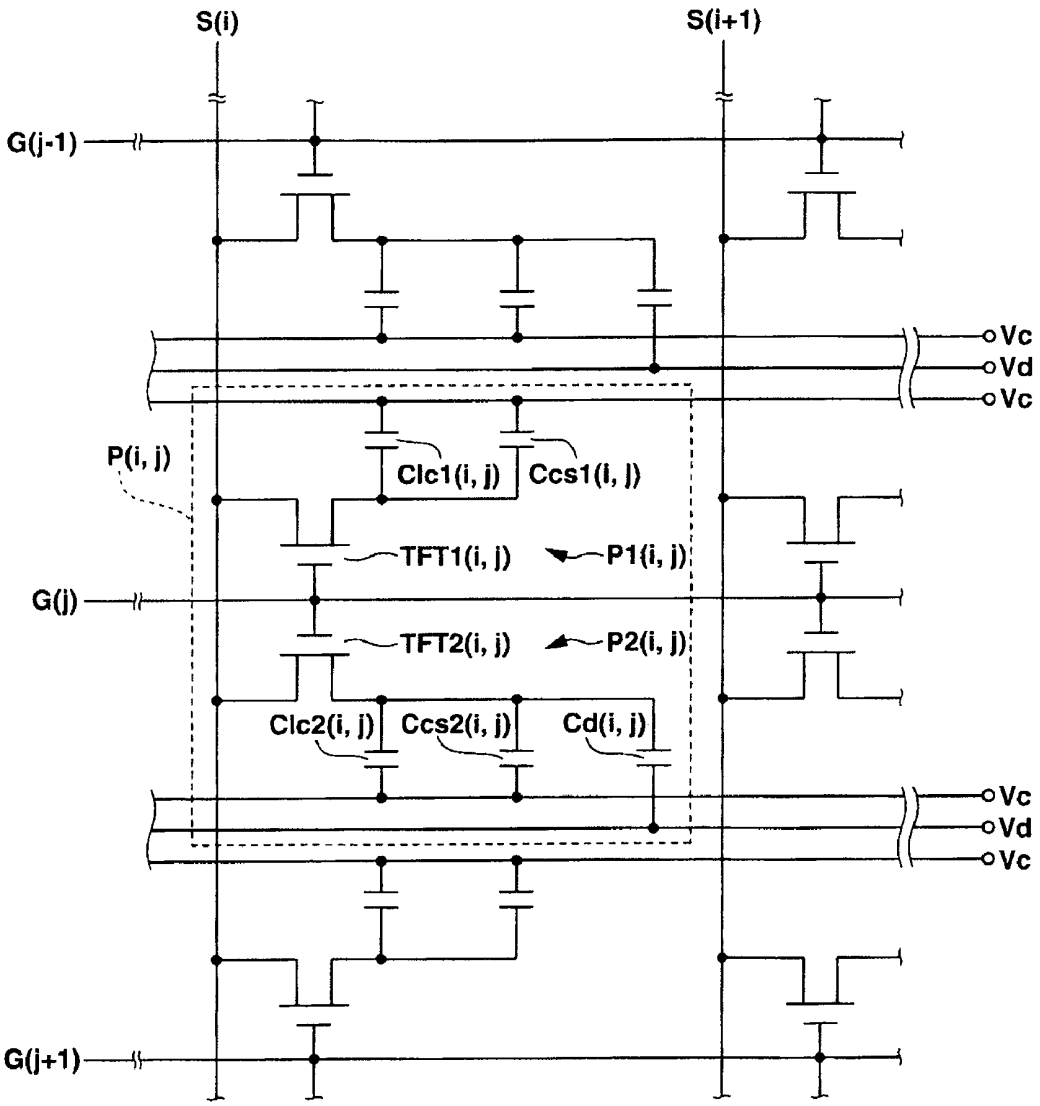

S(i)
S(i+1)
G(j-1)
Vc
Vd
Vc
P(i, j)
Clc1(i, j)
Ccs1(i, j)
TFT1(i, j)
P1(i, j)
G(j)
TFT2(i, j)
P2(i, j)
Clc2(i, j)
Ccs2(i, j)
Cd(i, j)
Vc
Vd
Vc
G(j+1)

FIG.4

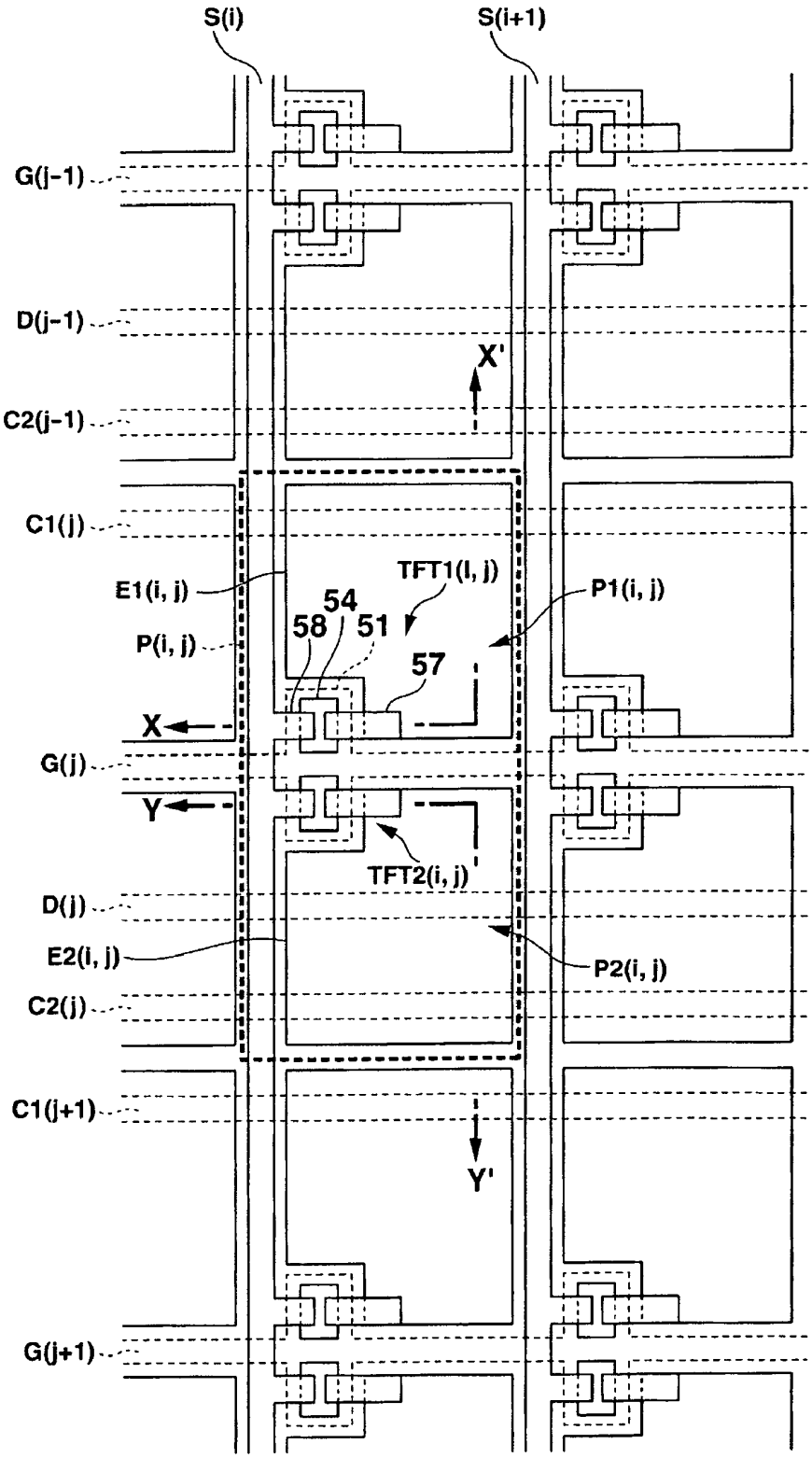

S(i)
S(i+1)
G(j-1)
D(j-1)
X'
C2(j-1)
C1(j)
E1(i, j)
TFT1(I, j)
P1(i, j)
54
58
51
P(i, j)
57
X
G(j)
Y
TFT2(i, j)
D(j)
E2(i, j)
P2(i, j)
C2(j)
C1(j+1)
Y'
G(j+1)

FIG.5A

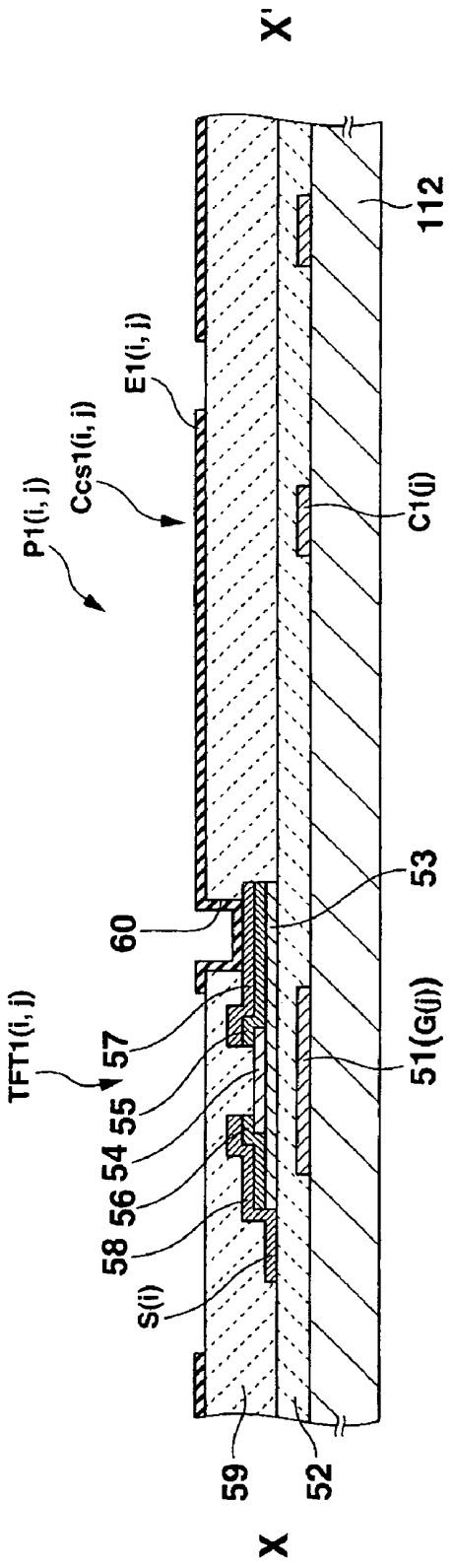

X
X'
P1(i, j)
Ccs1(i, j)
E1(i, j)
C1(j)
112
60
53
TFT1(i, j)
57
55
54
56
58
S(i)
51(G(j))
59
52

FIG.5B

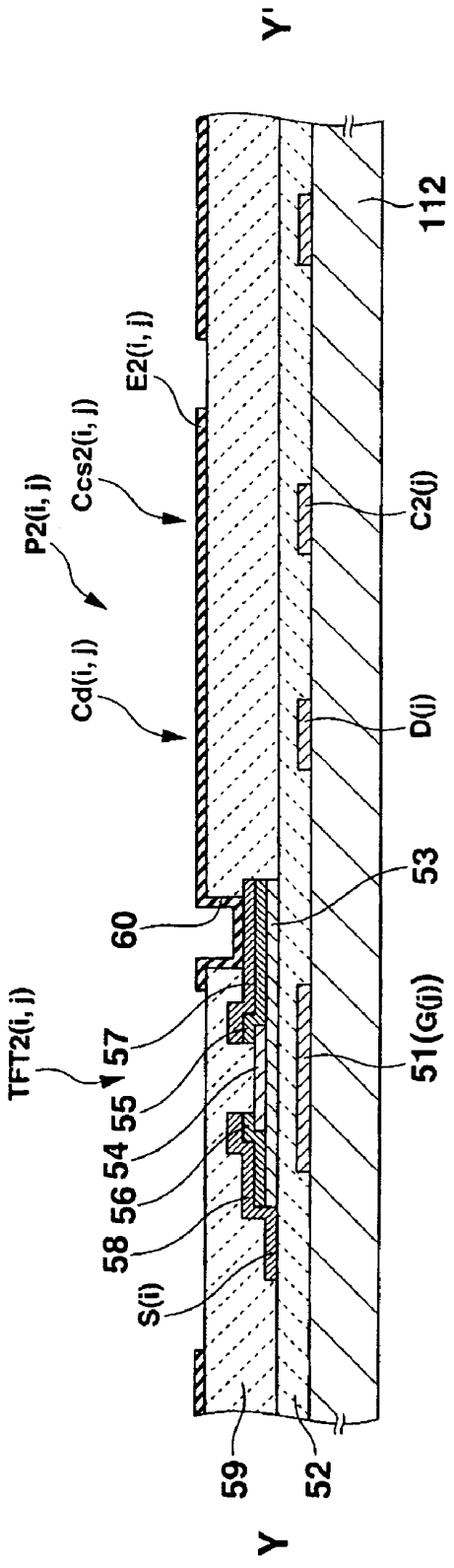

Y
Y'
P2(i, j)
Ccs2(i, j)
E2(i, j)
C2(j)
Cd(i, j)
D(j)
112
60
53
TFT2(i, j)
57
55
54
56
58
S(i)
51(G(j))
59
52

FIG.6

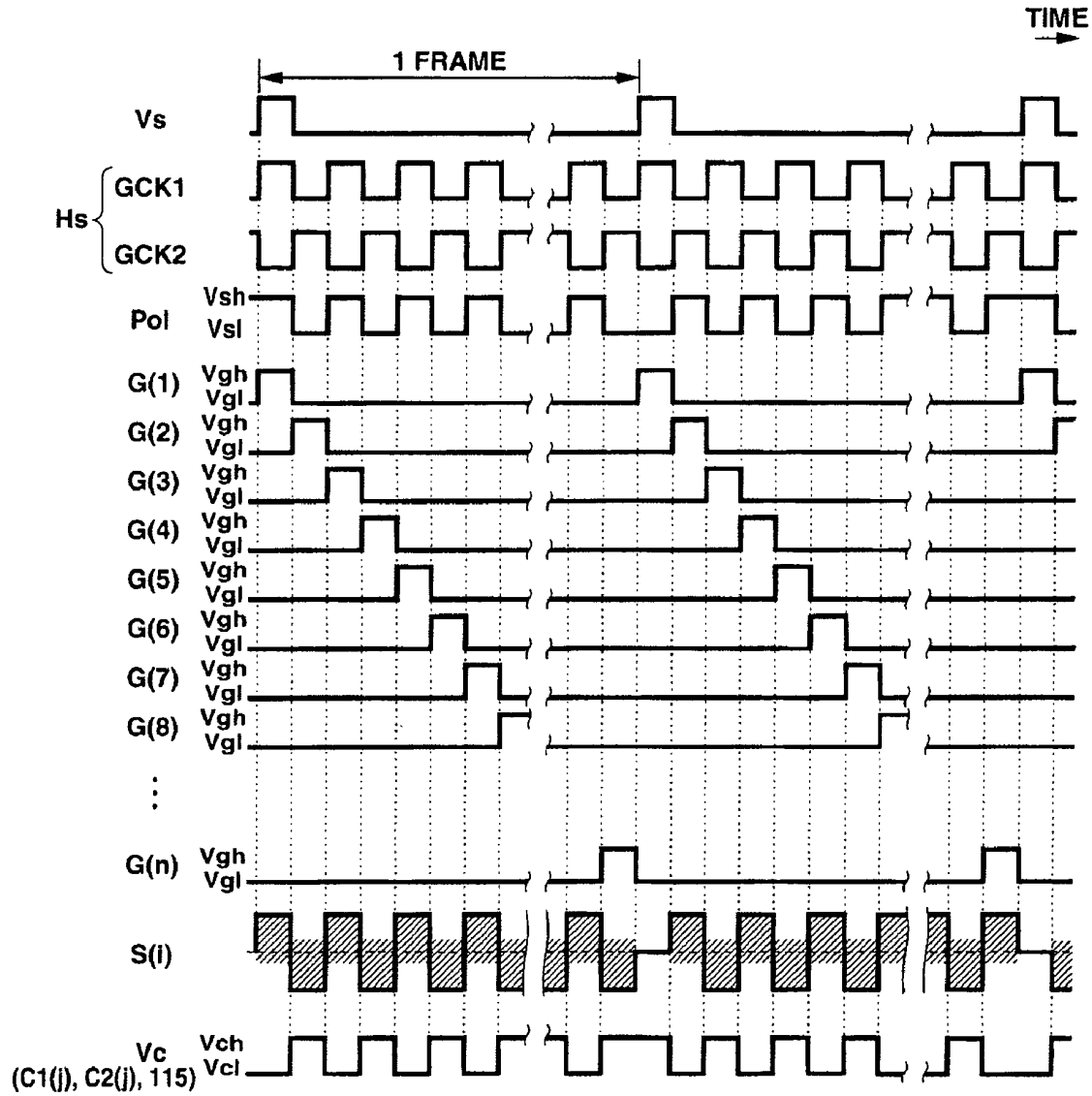

TIME
1 FRAME
Vs
Hs
GCK1
GCK2
Pol
Vsh
Vsl
G(1)
G(2)
G(3)
G(4)
G(5)
G(6)
G(7)
G(8)
G(n)
Vgh
Vgl
S(i)
Vc
(C1(j), C2(j), 115)
Vch
Vcl

FIG.7

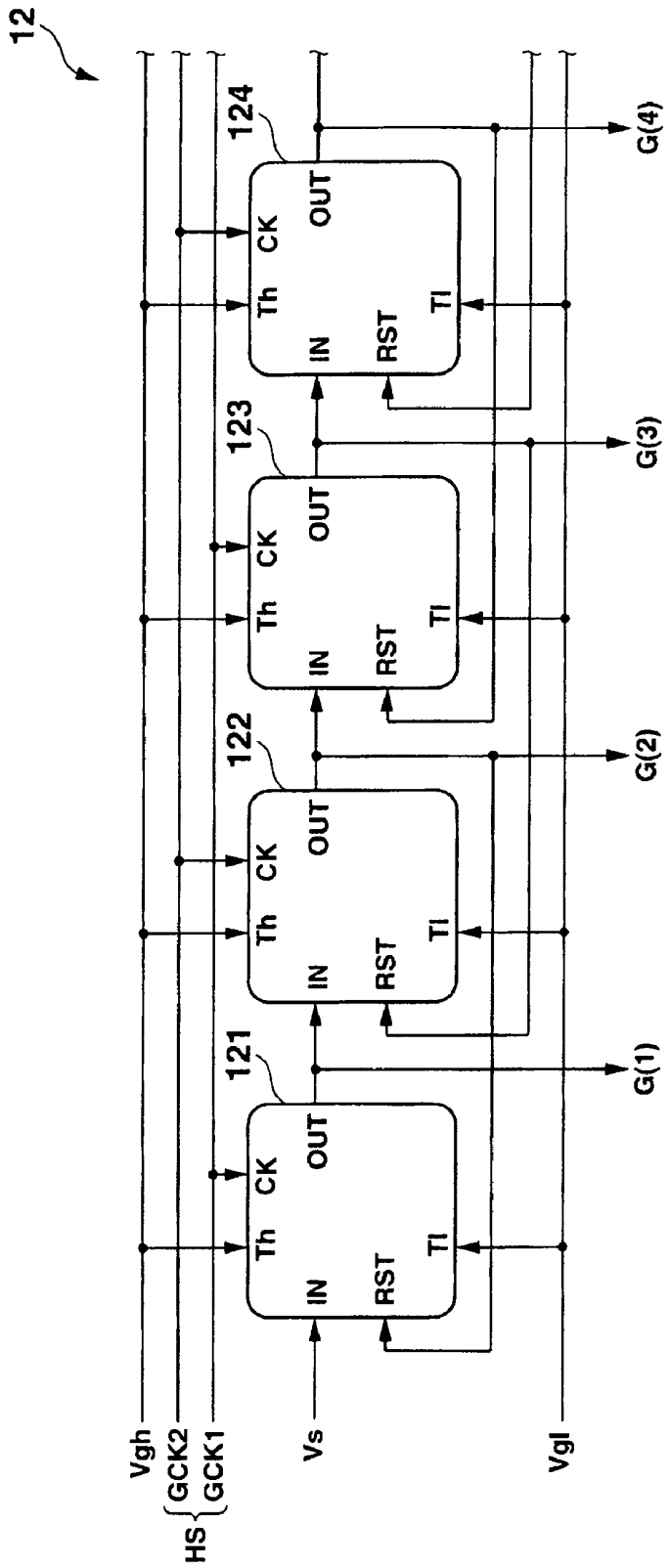

12
124
123
122
121
CK
OUT
Th
Tl
IN
RST
G(4)
G(3)
G(2)
G(1)
Vgh
GCK2
GCK1
HS
Vs
Vgl

FIG.8

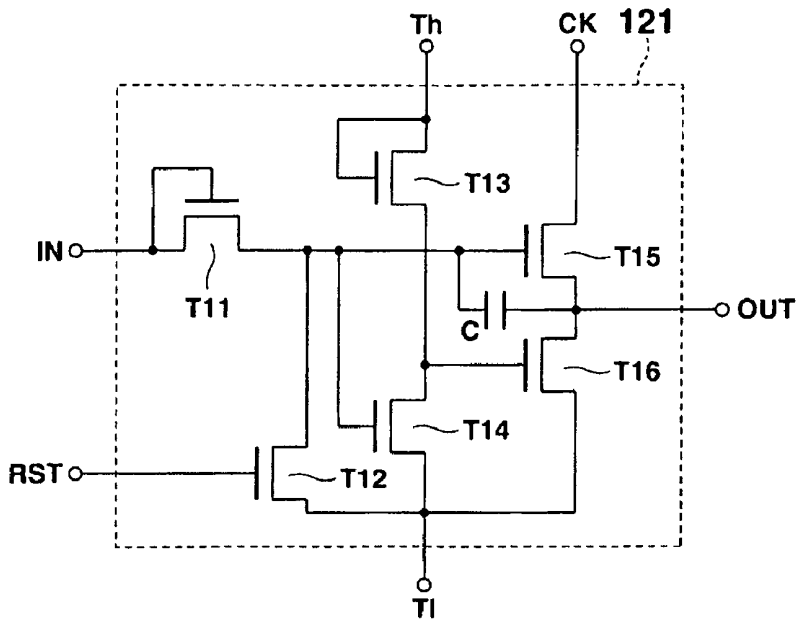

Th
CK
121
T13
IN
T11
T15
OUT
C
T16
T14
RST
T12
TI

FIG.9

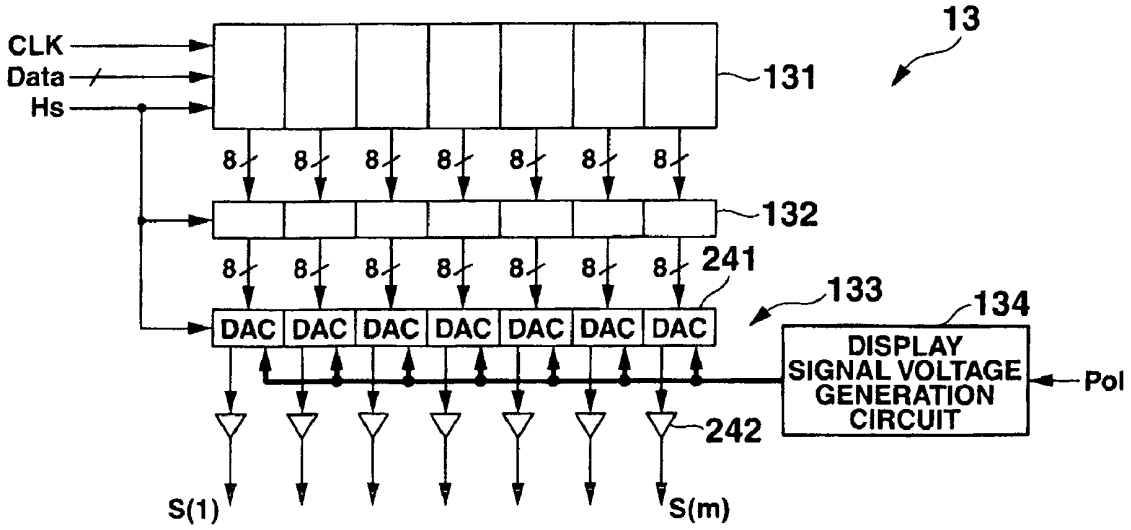

13
CLK
Data
Hs
131
8
132
241
133
134
DAC
DISPLAY SIGNAL VOLTAGE GENERATION CIRCUIT
Pol
242
S(1)
S(m)

FIG.10

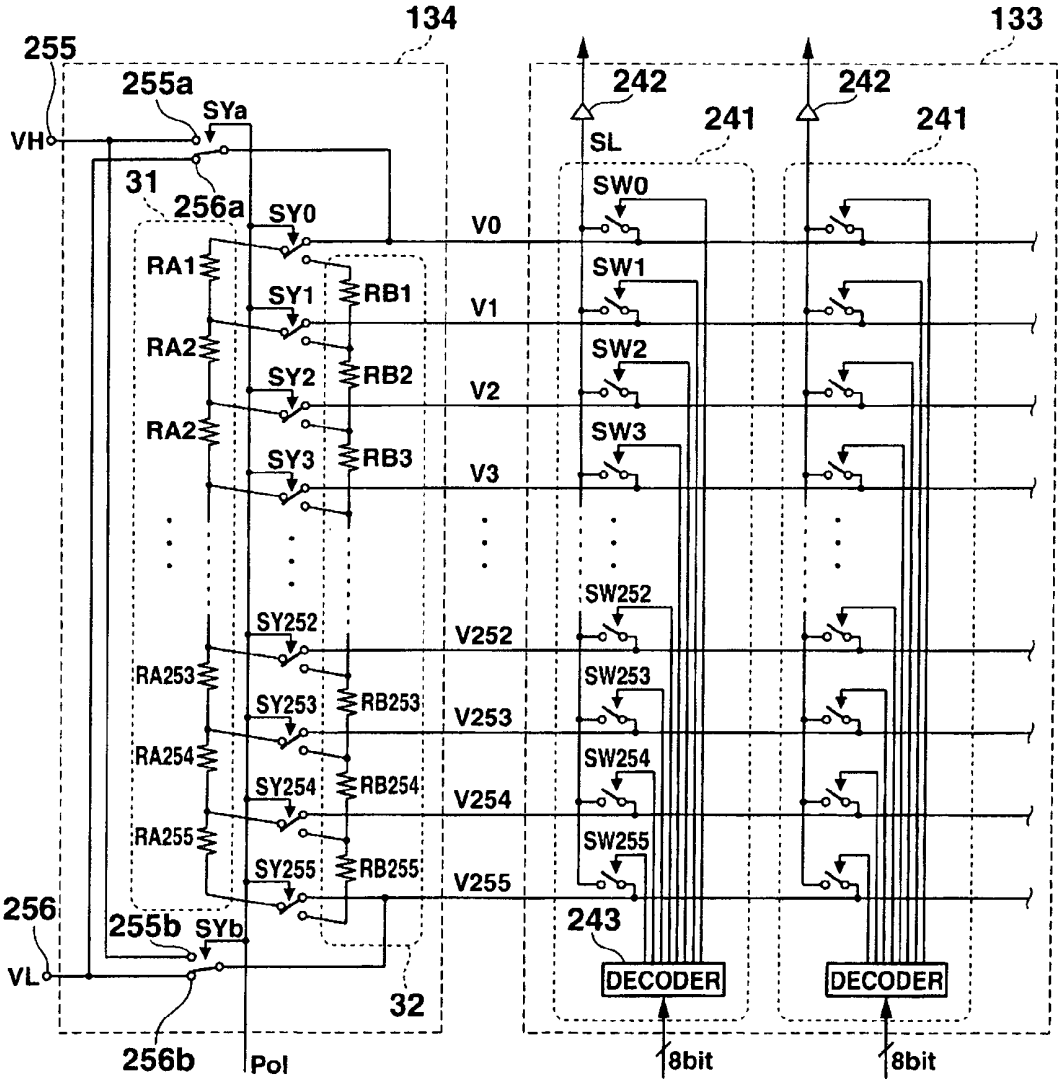

134
133
255
255a
SYa
VH
31
256a
SY0
V0
RA1
SY1
RB1
V1
RA2
SY2
RB2
V2
RA2
SY3
RB3
V3
SY252
V252
RA253
SY253
RB253
V253
RA254
SY254
RB254
V254
RA255
SY255
RB255
V255
256
255b
SYb
VL
32
256b
Pol
242
241
SL
SW0
SW1
SW2
SW3
SW252
SW253
SW254
SW255
243
DECODER
8bit

FIG.11

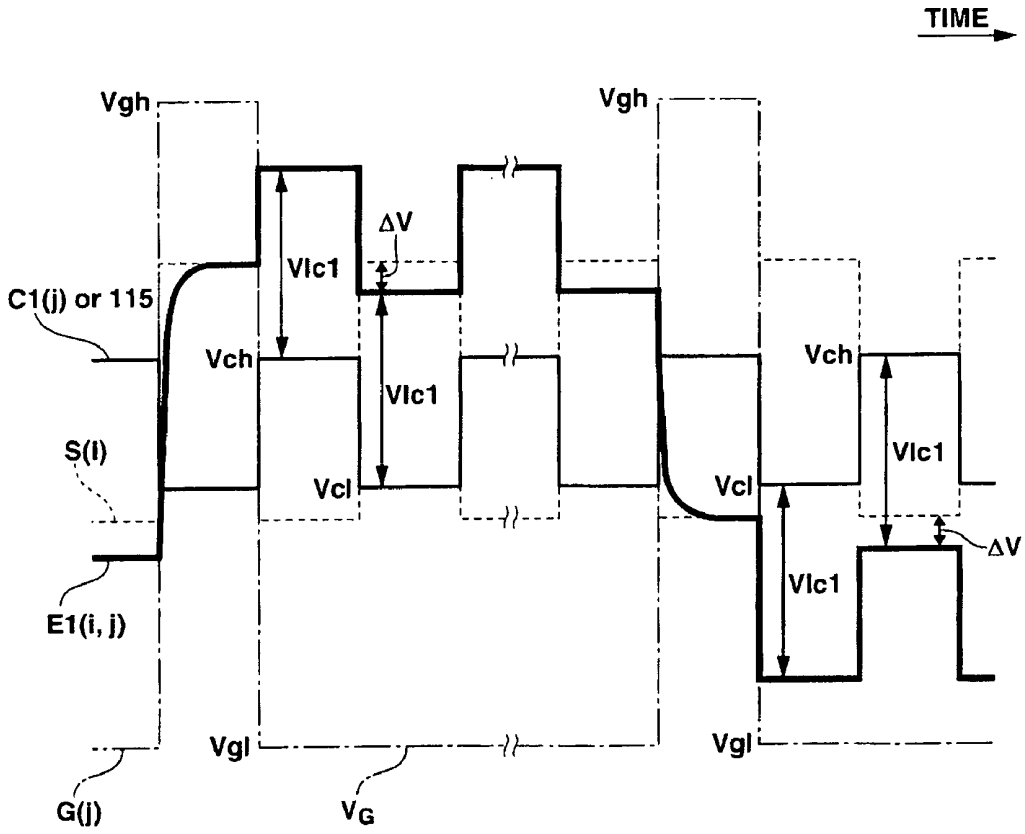

TIME
Vgh
Vgh
ΔV
Vlc1
C1(j) or 115
Vch
Vch
Vlc1
S(l)
Vlc1
Vcl
Vcl
ΔV
Vlc1
E1(i, j)
Vgl
Vgl
G(j)
VG

FIG.12

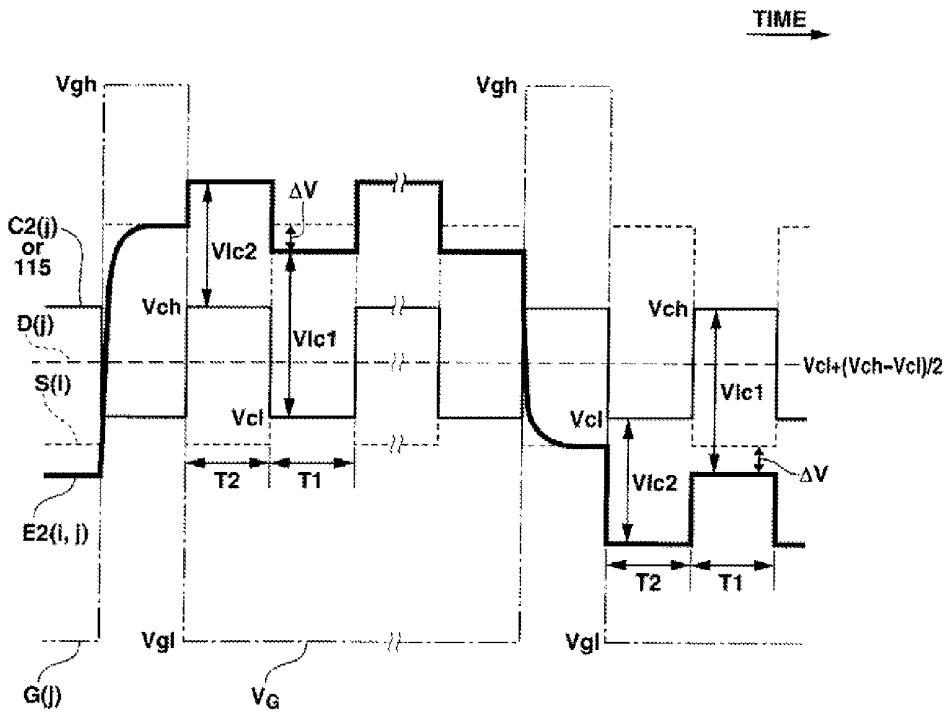

TIME
Vgh
Vgh
ΔV
C2(j) or 115
Vlc2
Vch
Vch
D(j)
Vlc1
Vcl+(Vch-Vcl)/2
S(l)
Vlc1
Vcl
Vcl
ΔV
T2
T1
Vlc2
E2(i, j)
T2
T1
Vgl
Vgl
G(j)
VG

FIG.13

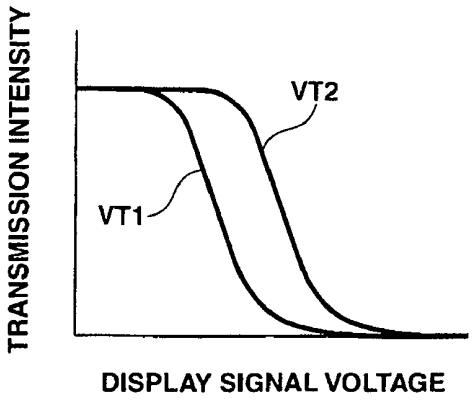


FIG.14A

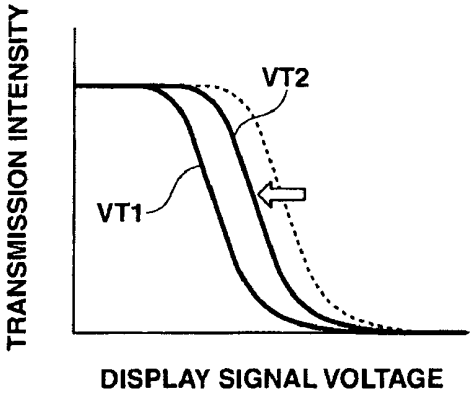


FIG.14B

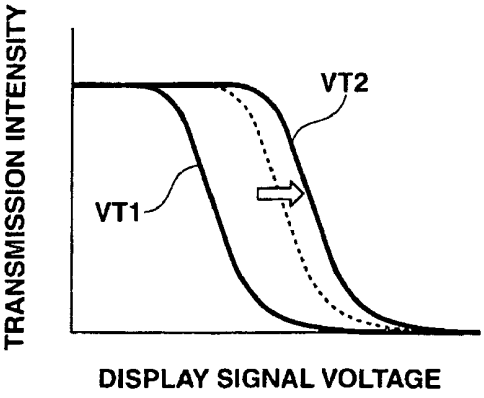


FIG.15A

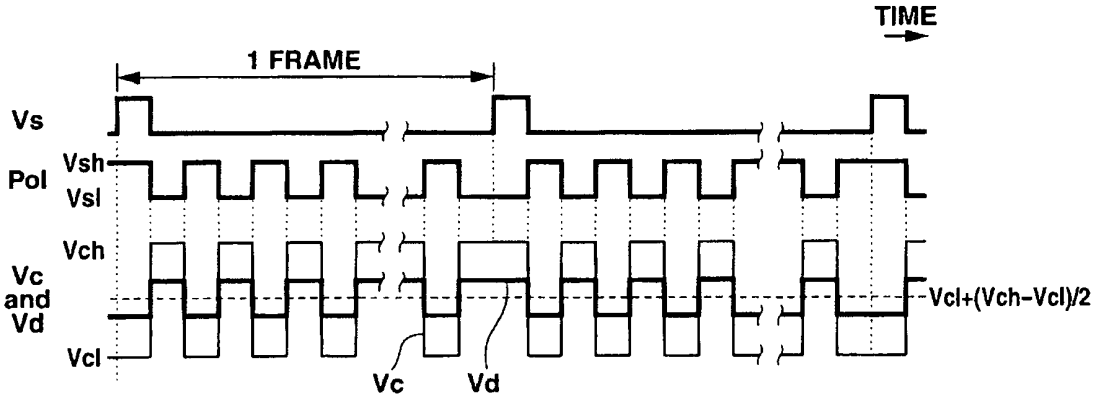


FIG.15B

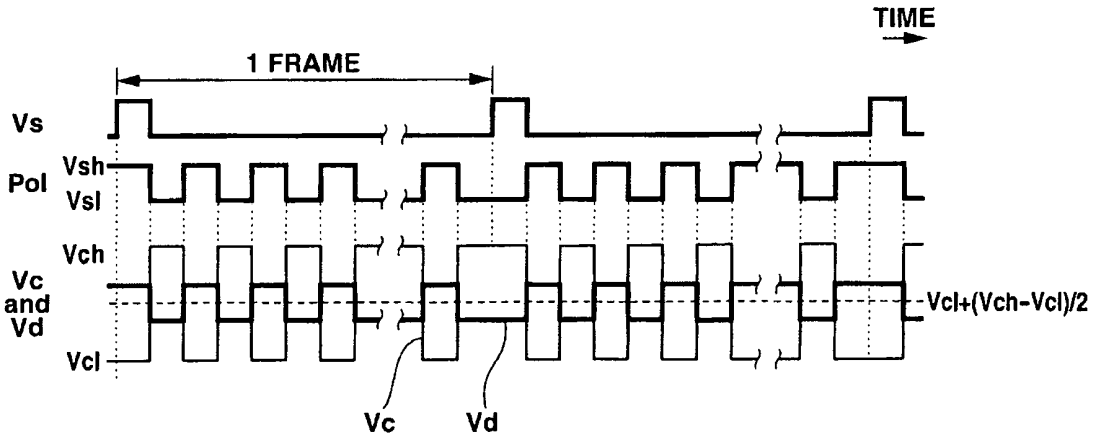


FIG.16

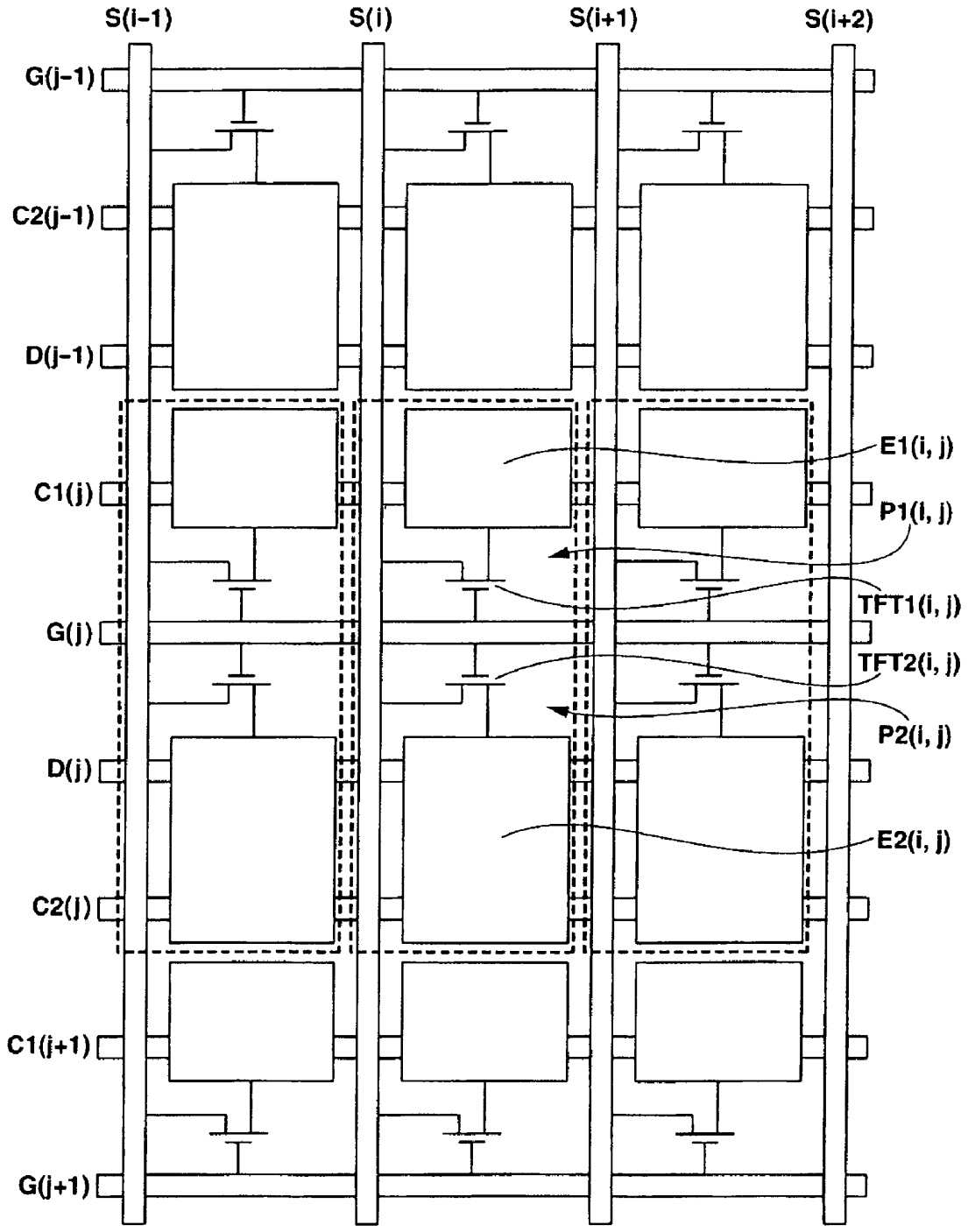

S(i-1)
S(i)
S(i+1)
S(i+2)
G(j-1)
C2(j-1)
D(j-1)
C1(j)
G(j)
D(j)
C2(j)
C1(j+1)
G(j+1)
E1(i, j)
P1(i, j)
TFT1(i, j)
TFT2(i, j)
P2(i, j)
E2(i, j)

FIG.17

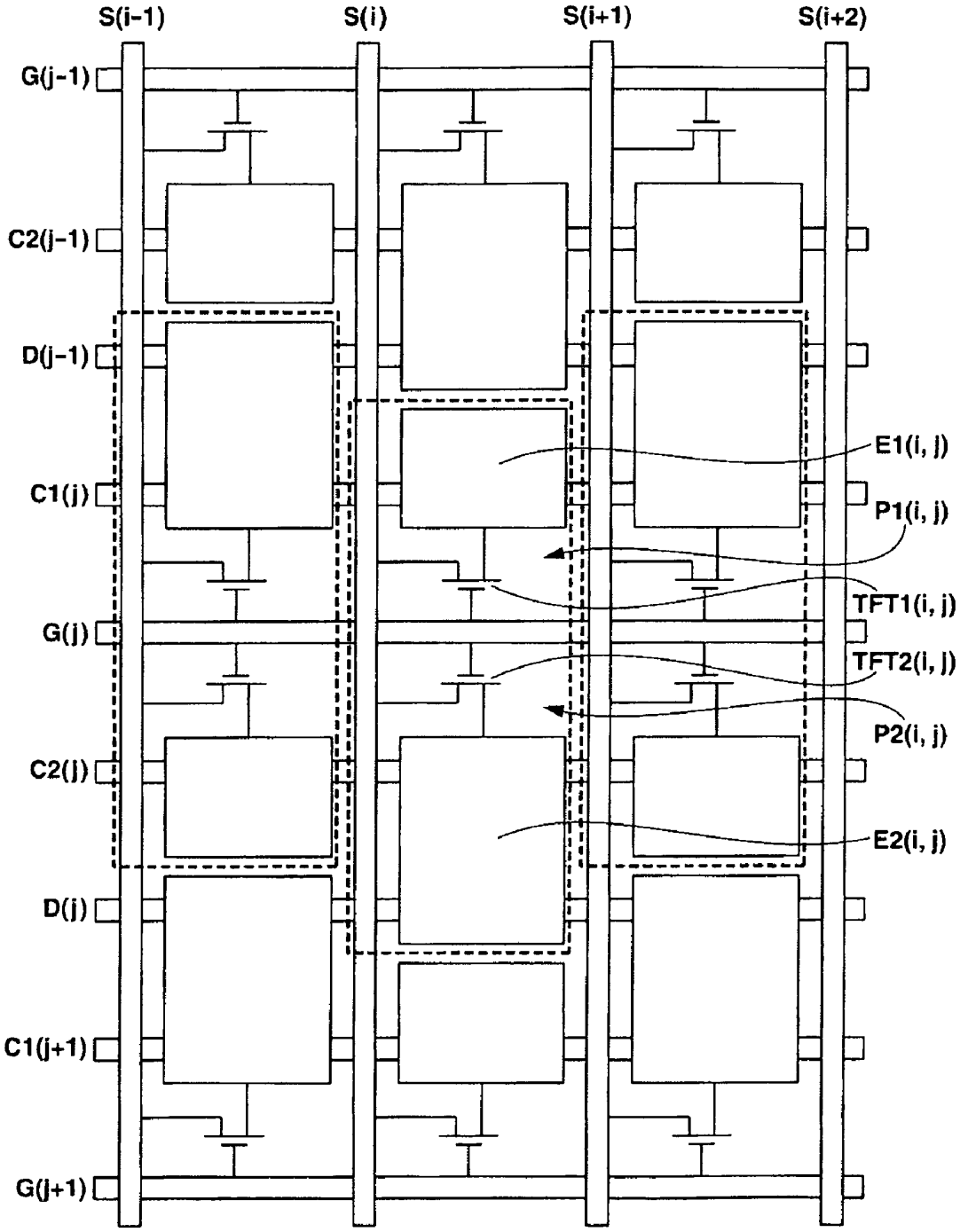

S(i-1)
S(i)
S(i+1)
S(i+2)
G(j-1)
C2(j-1)
D(j-1)
C1(j)
G(j)
C2(j)
D(j)
C1(j+1)
G(j+1)
E1(i, j)
P1(i, j)
TFT1(i, j)
TFT2(i, j)
P2(i, j)
E2(i, j)

FIG.18

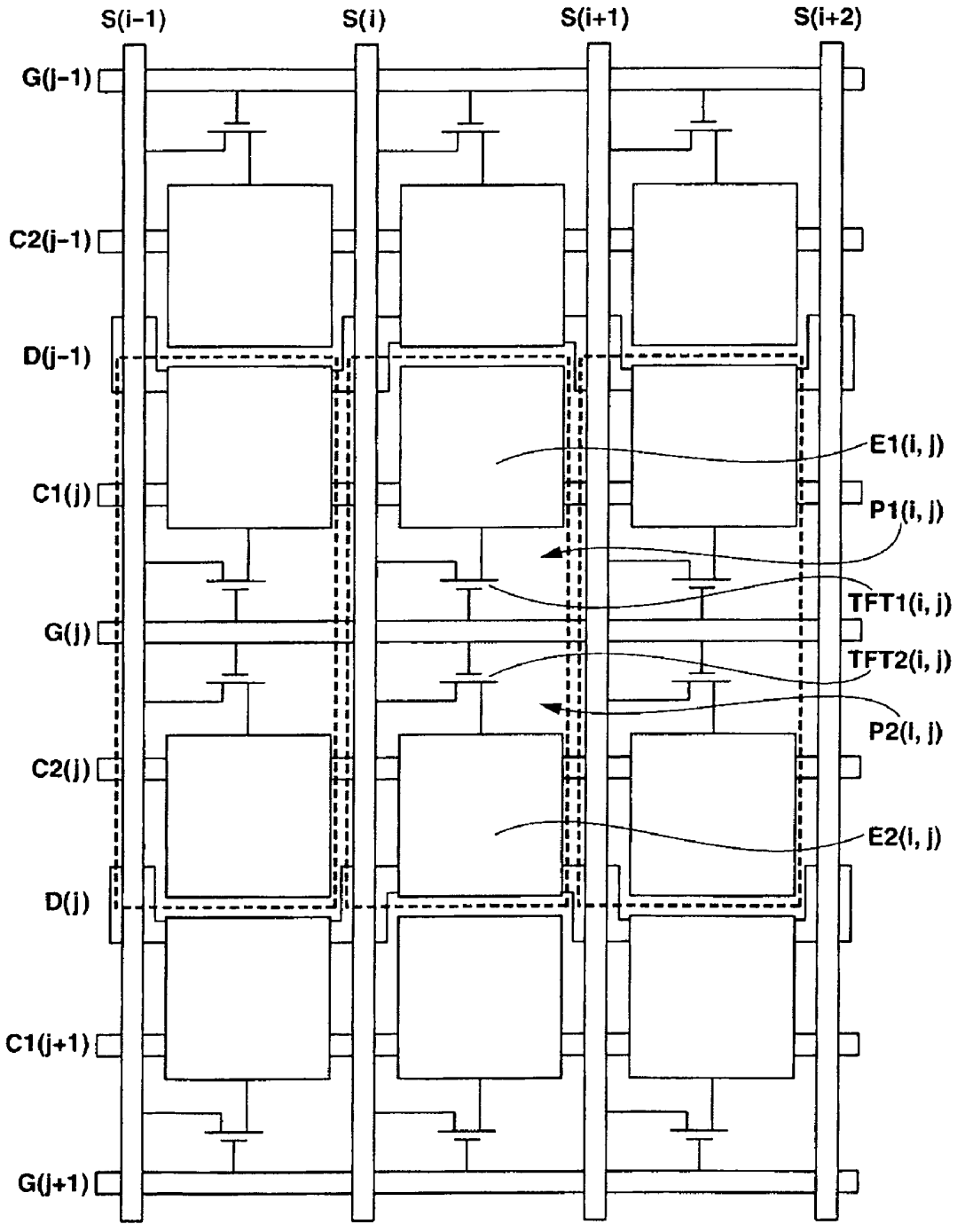

S(i-1)
S(i)
S(i+1)
S(i+2)
G(j-1)
C2(j-1)
D(j-1)
C1(j)
G(j)
C2(j)
D(j)
C1(j+1)
G(j+1)
E1(i, j)
P1(i, j)
TFT1(i, j)
TFT2(i, j)
P2(i, j)
E2(i, j)

FIG.19

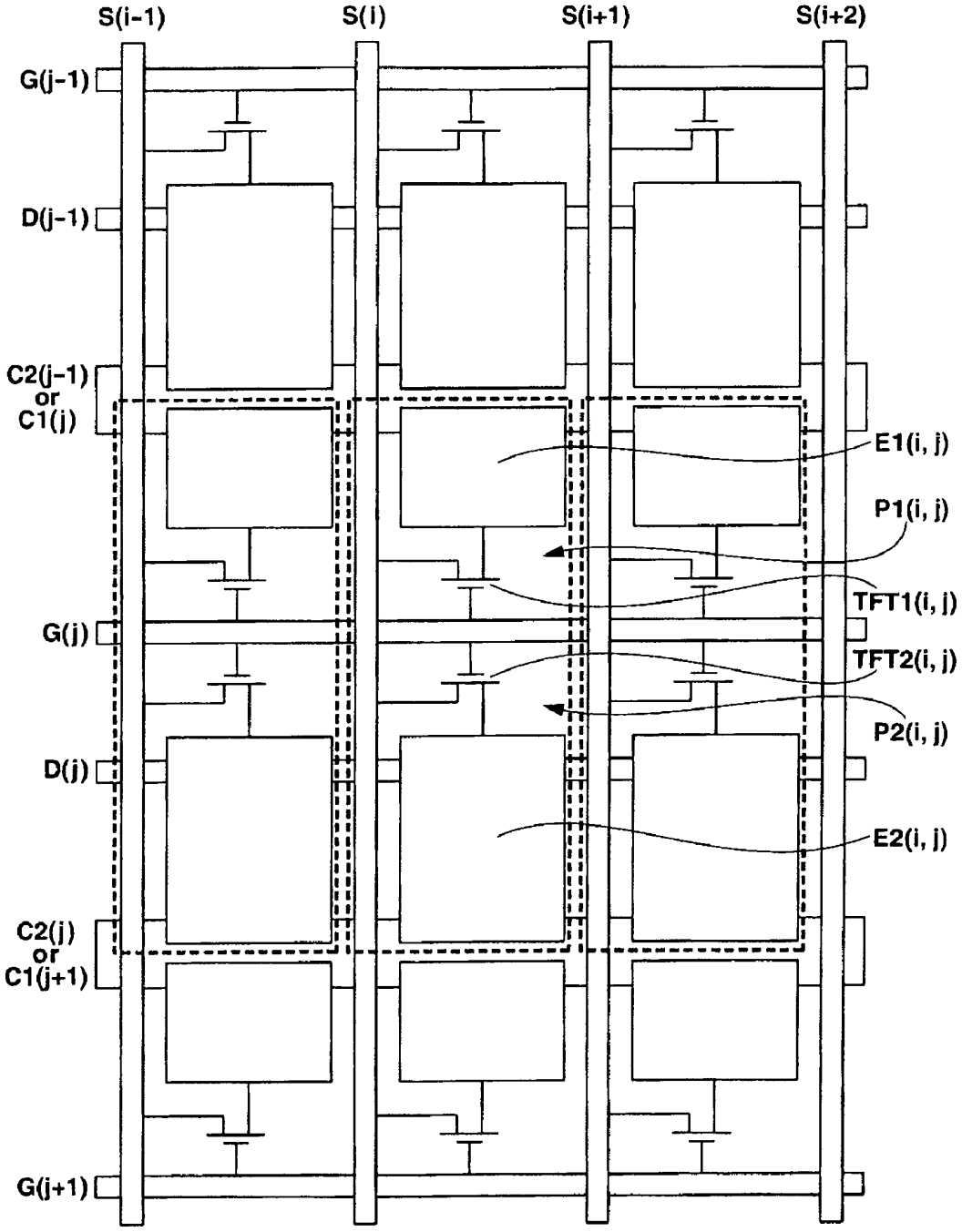
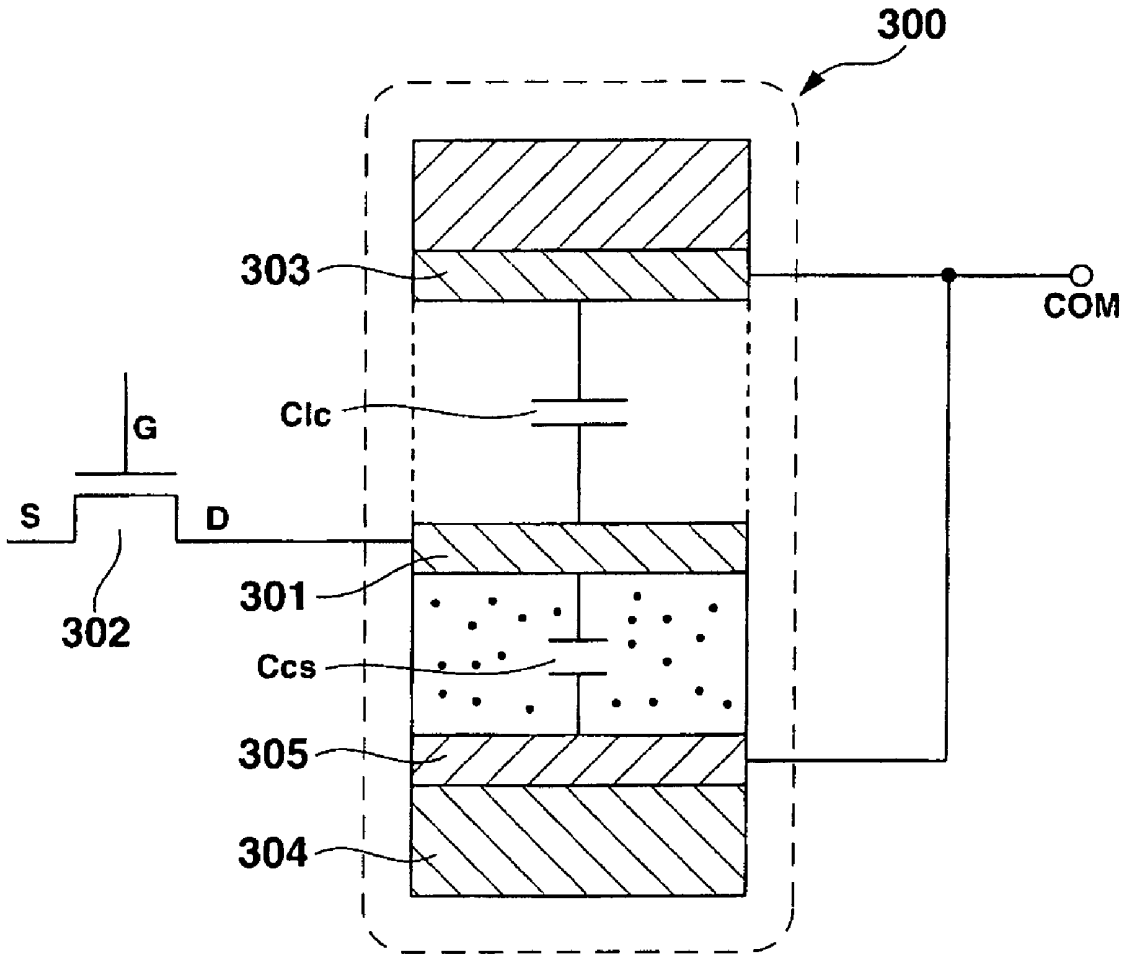

S(i-1)
S(i)
S(i+1)
S(i+2)
G(j-1)
D(j-1)
C2(j-1)
or
C1(j)
G(j)
D(j)
C2(j)
or
C1(j+1)
G(j+1)
E1(i, j)
P1(i, j)
TFT1(i, j)
TFT2(i, j)
P2(i, j)
E2(i, j)

FIG.20



LIQUID CRYSTAL DISPLAY DEVICE

This application claims the benefit of Japanese Application No. JP 2008-094421 filed, in Japan on Mar. 31, 2008, which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a liquid crystal display device having pixels equipped with first sub-pixels and second sub-pixels whose pixel electrodes are separated from each other.

2. Description of the Related Art

With conventional liquid crystal display devices, a voltage is applied to a liquid crystal through switching devices such as thin film transistors (TFT) and others disposed in pixels.

FIG. **20** is a view schematically showing a pixel **300** of a conventional liquid crystal display device. A pixel electrode (Pix) **301** is charged to a source potential via a transistor **302**. A common voltage (Vcom) is applied to a common electrode (COM) **303**, and the potential difference between the common electrode **303** and the pixel electrode **301** is applied to the liquid crystal as a voltage (Vlc). In this case, the liquid crystal sandwiched by the common electrode **303** and the pixel electrode **301** forms a liquid crystal capacitance Clc, whereas a solid dielectric material sandwiched by the pixel electrode **301** and an auxiliary capacitance line **305** forms an auxiliary capacitance Ccs.

The auxiliary capacitance Ccs is formed in parallel with the liquid crystal capacitance Clc. At the same time, since the auxiliary capacitance line **305** is connected in a way that allows the same potential as the common electrode **303** to be applied, the potential fluctuation that occur at the pixel electrode **301** due to a gate potential fluctuation or the leak current at off state of the transistor **302** is reduced. To prevent an image burn-in and electrolysis of the liquid crystal, the liquid crystal display device is ac-driven that the polarity of the voltage is applied to the liquid crystal to be switched at specified intervals.

There is a well-known technique, for example, that a pixel of a liquid crystal device is divided into multiple regions and different voltages are applied to each region to decrease the dependence of display status on viewing angles, as disclosed by Japanese Patent Laid Open Applications, JP H7-028091A (1995) and JP H8-015723A (1996).

Specifically, JP H7-028091A discloses a liquid crystal display device that a TFT is connected to any one of the divided pixel electrodes, and effective voltages at various levels are applied to multiple regions within the pixels of the liquid crystal by applying the voltage to the pixel electrode connected to the TFT to other pixel electrodes via a capacitance formed between the relevant pixel electrode.

JP H8-015723A discloses an active matrix liquid crystal display that its common electrode is disposed opposite to a pixel electrode connected to a TFT and is divided into multiple regions. By applying different voltages to each region, effective voltages at various levels are applied to the liquid crystal of a plural region in a pixel.

However, in the liquid crystal display device disclosed by JP H7-028091A, if the capacitances formed between the pixel electrode connected to the TFT and other pixel electrodes vary due to the difference in thickness of dielectric material (insulation film) for example, a problem arises that the viewing-angle dependences vary among plural liquid crystal display device from device.

On the other hand, in the active matrix liquid crystal display disclosed by JP H8-015723A, since electrode patterning on the pixel size level must be performed on both substrates constituting a liquid crystal panel, it increases the number of manufacturing processes. Furthermore, since high laminating accuracy is required in laminating two substrates, thus inducing a problem that the yielding was lowered.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is directed to provide a liquid crystal display device whose viewing-angle dependence, which varies from device to device, can be corrected easily without increasing the number of manufacturing processes, and even after liquid crystal panels have been manufactured, thus solving the problems of conventional liquid crystal display devices.

One of the preferable embodiments of the present invention provides a liquid crystal display device with multiple pixels provided therein, comprising: multiple pixel electrodes arranged in a horizontal direction and a vertical direction, the pixel electrode including a first sub-pixel electrode and a second sub-pixel electrode disposed adjacent to the first sub-pixel electrode; a common electrode disposed opposite to the multiple pixel electrodes; plural scanning signal lines extending in the horizontal direction; a first liquid crystal capacitance formed with a liquid crystal sandwiched between the common electrode and the first sub-pixel electrode; a first auxiliary capacitance formed with a solid dielectric material sandwiched between the first sub-pixel electrode and a first auxiliary capacitance line extending in the horizontal direction; a second liquid crystal capacitance formed with the liquid crystal sandwiched between the common electrode and the second sub-pixel electrode; a second auxiliary capacitance formed with a solid dielectric material sandwiched between the second sub-pixel electrode and a second auxiliary capacitance line extending in the horizontal direction; a step-down capacitance formed with a solid dielectric material sandwiched between the second sub-pixel electrode and a step-down capacitance line, the step-down capacitance line being different from any one of the plural scanning signal lines and from the second auxiliary capacitance line, and extending in the horizontal direction; a first voltage application means for applying a common first voltage to the common electrode, the first auxiliary capacitance line, and to the second auxiliary capacitance line; and a second voltage application means for applying a second voltage, which is different from a voltage applied to the scanning signal line and from the first voltage, to the step-down capacitance line, wherein the first voltage is a rectangular AC voltage that oscillates at a specified amplitude, and the second voltage is a rectangular AC voltage whose amplitude is smaller than the specified amplitude of the first voltage.

In another aspect, the present invention provides a liquid crystal display device with multiple pixels provided therein, comprising: multiple pixel electrodes arranged in a horizontal direction and a vertical direction, said pixel electrode includes a first sub-pixel electrode and a second sub-pixel electrode disposed adjacent to said first sub-pixel electrode; a common electrode disposed opposite to said plural pixel electrodes; multiple scanning signal lines extending in the horizontal direction; and a first voltage application means and a second voltage application means both for applying voltage, wherein: the first sub-pixel electrode is disposed opposite to the common electrode via a liquid crystal layer, and is disposed opposite to a first auxiliary capacitance line extending in the horizontal direction via an insulating layer, the second

sub-pixel electrode is disposed opposite to the common electrode via the liquid crystal layer, and is disposed opposite to a second auxiliary capacitance line extending in the horizontal direction via the insulating layer, and further, the second sub-pixel electrode is disposed opposite to a step-down capacitance line via the insulating layer, the step-down capacitance line being different from any one of the multiple scanning signal lines and from the second auxiliary capacitance line, and extending in the horizontal direction, the first voltage application means applies a common first voltage to the common line, the first auxiliary capacitance line, and to the second auxiliary capacitance line, and the second voltage application means applies a second voltage, which is different from a voltage applied to the scanning signal line and from the first voltage, to the step-down capacitance line, wherein the first voltage is a rectangular AC voltage that oscillates at a specified amplitude, and the second voltage is a rectangular AC voltage whose amplitude is smaller than the specified amplitude of the first voltage.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings:

FIG. **1** is a block diagram illustrating a structure of a liquid crystal display device according to an embodiment of the present invention;

FIG. **2** is a drawing illustrating a cross-sectional area of a liquid crystal display device according to an embodiment of the present invention;

FIG. **3** is a drawing illustrating an equivalent circuit of a pixel;

FIG. **4** is a magnified plan view of a pixel;

FIG. **5**A is a cross-sectional view of the pixel in FIG. **4** taken along a line X-X';

FIG. **5**B is a cross-sectional view of the pixel in FIG. **4** taken along a line Y-Y';

FIG. **6** is a chart illustrating scanning signals and a common voltage;

FIG. **7** is a block diagram illustrating a configuration of a scanning signal line drive circuit;

FIG. **8** is a block diagram illustrating a configuration of a holding circuit;

FIG. **9** is a block diagram illustrating a configuration of a data signal line drive circuit;

FIG. **10** is a block diagram illustrating a configuration of a display signal voltage generation circuit;

FIG. **11** is a drawing illustrating a voltage to be applied to the liquid crystal at a first sub-pixel;

FIG. **12** is a drawing illustrating a voltage to be applied to the liquid crystal at a second sub-pixel;

FIG. **13** is a drawing illustrating the relationship between display signal voltage and transmission intensity in each pixel;

FIG. **14**A is a drawing illustrating the relationship between display signal voltage and transmission intensity in each pixel, with the step-down voltage oscillated in a way that allows the potential difference from the common voltage to be decreased;

FIG. **14**B is a drawing illustrating the relationship between display signal voltage and transmission intensity in each pixel, with the step-down voltage oscillated in a way that allows the potential difference from the common voltage to be increased;

FIG. **15**A is a drawing illustrating the relationship between common voltage and step-down voltage, with the step-down voltage oscillated in a way that allows the potential difference from the common voltage to be decreased;

FIG. **15**B is a drawing illustrating the relationship between the common voltage and step-down voltage, with the step-down voltage oscillated in a way that allows the potential difference from the common voltage to be increased;

FIG. **16** is a partially magnified plan view illustrating a first example of the layout of first and second sub-pixels in a pixel;

FIG. **17** is a partially magnified plan view illustrating a second example of the layout of first and second sub-pixels in a pixel;

FIG. **18** is a partially magnified plan view illustrating a part of a third example of the layout of first and second sub-pixels in a pixel;

FIG. **19** is a partially magnified plan vie illustrating a part of a fourth example of the layout of first and second sub-pixels in a pixel; and

FIG. **20** is a drawing schematically illustrating a structure of a pixel of a conventional liquid crystal display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, various embodiments of the present invention will be described in detail with reference to the figures in which like reference characters are used to designate like or corresponding components.

As shown in FIG. **1**, a liquid crystal display device **1** according to the present invention comprises, for example, an image memory **10** for temporarily storing image data input from outside, a display panel **11** for displaying an image based on the image data stored in the image memory **10**, a scanning signal line drive circuit **12** for scanning signal lines of the display panel **11**, a data signal line drive circuit **13** for providing a display signal voltage to the data signal lines of the display panel **11** based on an image data, a common voltage generation circuit **14** for applying a specified voltage to a common electrode and auxiliary capacitance lines of the display panel **11**, a step-down voltage generation circuit **15** for applying voltage for decreasing pixel voltage to step-down capacitance lines of the display panel **11**, an inherent information storage unit **16** in which a value of the voltage to be applied by the step-down voltage generation circuit **15** has been stored, and a control unit **17** that outputs various control signals to synchronize each drive unit, whose operation will be described in detail later.

As shown in FIG. **2**, the display panel **11** is comprised of a pair of substrates **112** and **113** which are disposed opposite to each other and adhered with a sealing agent **111**, and a liquid crystal LC is sandwiched between the substrates **112** and **113**. One of the substrates **112** comprises multiple scanning signal lines extending in the horizontal direction ("n" scanning signal lines, for example), multiple auxiliary capacitance lines also extending in the horizontal direction ("n×2" auxiliary capacitance lines, for example), step-down capacitance lines also extending in the horizontal direction ("n" step-down capacitance lines, for example), and multiple data signal lines extending in the vertical direction ("m" data signal lines, for example) and a pixel P (i, j) as shown in FIGS. **3** and **4** is disposed on the substrate **112** adjacent at each intersections of a scanning signal line G (j) and a data signal line S (i) (i=1, 2, 3, . . . m, and j=1, 2, 3, . . . n). A common electrode **115** having a common electric potential at each pixel P (i, j) is disposed on the substrate **112** that faces substrate **112**. For example, a transparent electrode is disposed on a surface of the substrate **113** opposing to substrate **112** to cover the entire surface.

At each pixel P (i, j), a first sub-pixel P**1** (i, j) and a second sub-pixel P**2** (i, j) are disposed.

At the first sub-pixel P1 (i, j), a first pixel electrode E1 (i, j) and a TFT1 (i, j) as a first switching device, etc. are disposed. The first pixel electrode E1 (i, j) is connected to a drain electrode of TFT1 (i, j), the data signal line S (i) is connected to a source electrode of TFT1 (i, j), and a scanning signal line G (j) is connected to a gate electrode of TFT1 (i, j). A first liquid crystal capacitance Clc1 (i, j) is formed by the common electrode **115**, the first pixel electrode E1 (i, j), and the liquid crystal filled between them. An auxiliary capacitance line C1 (j) is disposed on the lower side of a first pixel electrode E1 (i, j) via a solid dielectric material so that a first auxiliary capacitance Ccs1 (i, j) is formed by the first pixel electrode E1 (i, j), the dielectric material, and the auxiliary capacitance line C1 (j).

Meanwhile, in the second sub-pixel P2 (i, j), a second pixel electrode E2 (i, j) separated from the first pixel electrode E1 (i, j), TFT2 (i, j) as a second switching device etc. are disposed. The second pixel electrode E2 (i, j) is connected to a drain electrode of TFT2 (i, j), the data signal line S (i) is connected to the source electrode of TFT2 (i, j), and the scanning signal line G (j) is connected to a gate electrode of TFT2 (i, j). A second liquid crystal capacitance Clc2 (i, j) is formed by the common electrode **115**, the second pixel electrode E2 (i, j), and the liquid crystal filled between them. An auxiliary capacitance line C2 (j) and a step-down capacitance line D (j) are disposed on the lower side of the second pixel electrode E2 (i, j) via a solid dielectric material. A second auxiliary capacitance Ccs2 (i, j) is formed by the second pixel electrode E2 (i, j), the dielectric material, and the auxiliary capacitance line C2 (j). Also, a step-down capacitance Cd (i, j) is formed by the second pixel electrode E2 (i, j), the dielectric material, and the step-down capacitance line D (j).

Each pixel P (i, j) is configured to allow display status to be controlled by changing the orientation of the liquid crystal disposed between the pixel electrode and the common electrode **115** of each sub-pixel, P1 (i, j) and P2 (i, j), based on the potential difference between the pixel electrode and the common electrode **115**.

The common electrode **115** and the auxiliary capacitance lines C1 (j) and C2 (j) are electrically connected outside the display area **114**, which allows an applying a common voltage Vc. A step-down voltage Vd, which is different from the common voltage Vc, is applied to the step-down capacitance lines D (j).

Hereinafter, specific configuration of the cross-sectional area of each pixel P (i, j) will be described by referring to FIGS. **5**A and **5**B. The scanning signal line G (j) including a gate electrode **51** is disposed on one of the substrates **112**. The auxiliary capacitance lines C1 (j) and C2 (j) and step-down capacitance line D (j) are disposed on the same layer as the scanning signal line G (j). In other words, the scanning signal line G (j), auxiliary capacitance lines C1 (j) and C2 (j), and step-down capacitance line D (j) are formed at a same time. A gate insulating film **52** is disposed on the whole surfaces of these lines. An intrinsic amorphous silicon semiconducting thin film **53** is disposed on the gate insulating film **52**. A channel protective film **54** is disposed on the upper surface of approximately center of semiconducting thin film **53**. An n-type amorphous silicon contact layers **55** and **56** are disposed on both sides of the channel protective film **54** and the semiconducting film **53** covering the upper face of the channel protective film **54** on both sides.

A drain electrode **57** is disposed on an upper face of one of the contact layers **55**. The data signal line S (i) including a source electrode **58** is disposed on an upper face of the other contact layer **56** and an upper face of the gate insulating film **52**.

Thus, the TFT1 (i, j) is included by the gate electrode **51**, the gate insulating film **52**, the semiconducting thin film **53**, the channel protective film **54**, the contact layers **55** and **56**, the drain electrode **57**, and the source electrode **58**. TFT2 (i, j) is configured as same as the TFT1 (i, j).

A planarizing film **59** made of an insulating material is disposed over the entire surface of the gate insulating film **52** including TFT1 (i, j), TFT2 (i, j), etc. A contact hole **60** is formed in the specified portion of the planarizing film **59** corresponding to the drain electrode **57**. The pixel electrodes E1 (i, j) and E2 (i, j) both of which are consisting of ITO are disposed on the specified portions of the planarizing film **59**. The pixel electrodes E1 (i, j) and E2 (i, j) are connected to the drain electrodes **57** of the relevant TFT via the contact hole **60**.

A portion of the auxiliary capacitance line C1 (j) that overlaps with the first pixel electrode E1 (i, j) serves as an auxiliary capacitance electrode. This overlapping portion forms the first auxiliary capacitance Ccs1 (i, j) as described previously. Meanwhile, a portion of the auxiliary capacitance line C2 (j) that overlaps with the second pixel electrode E2 (i, j) serves as an auxiliary capacitance electrode. As described previously, this overlapping area forms the second auxiliary capacitance Ccs2 (i, j). Furthermore, a portion of the step-down capacitance line D (j) that overlaps with the second pixel electrode E2 (i, j) serves as a step-down capacitance electrode. This overlapping portion forms a step-down capacitance Cd (i, j) as described previously. Each pixel P (i, j) is configured to ensure that a size of the first auxiliary capacitance Ccs1 (i, j) is equal to that of the second auxiliary capacitance Ccs2 (i, j).

As shown in FIG. **6**, the scanning signal line drive circuit **12** outputs scanning signals to each scanning signal line G (j) according to vertical synchronizing signal Vs output from a control unit **17** and horizontal synchronizing signal Hs based on a first gate clock signals GCK1 and a second gate clock signals GCK2. The first gate clock signals GCK1 and the second gate clock signals GCK2 are rectangular signals having an opposite phase to each other.

As shown in FIG. **7**, the main part of the scanning signal line drive circuit **12** is roughly configured with holding circuits **121**, **122**, **123**, **124**, . . . connected in series of the number equivalent to the number of the scanning signal lines ("n" stages). Each holding circuit **121**, etc. comprise: an input terminal IN, an output terminal OUT, a reset terminal RST, a clock signal input terminal CK, a high potential power input terminal Th, and a low potential power input terminal Tl. The vertical synchronizing signal Vs is supplied to the input terminal IN of the holding circuit **121** as the first stage input signal. The output signals from the holding circuit in the previous stage are supplied to the input terminal IN of the holding circuit in the second and subsequent stages. The output signals from the holding circuit in the next stage are supplied to the reset terminal RST of each holding circuit. Here, separate reset signals END or the output signals from the holding circuit **121** in the first stage may be supplied to the reset terminal RST of the holding circuit in the final stage (not shown, "y"th stage, for example).

Furthermore, the first gate clock signal GCK1 is supplied to clock signal input terminals CK of the holding circuit in the odd-numbered stages. The second gate clock signal GCK2 having opposite phase to the first gate clock signal GCK1 is supplied to the clock signal input terminals CK of the holding circuit in the even-numbered stages. A predetermined high voltage Vgh is supplied to the high-potential power input terminal Th of each holding circuits, whereas a predeter-

mined low voltage Vgl is supplied to the low-potential power input terminal Tl of each holding circuits.

As shown in FIG. **8**, each holding circuit **121**, **122**, **123**, **124**, . . . is provided with six MOS type Field Effect Transistors (hereinafter referred to as MOS transistors) T**11** to T**16** and a capacitance C.

As shown in FIG. **6**, such scanning signal line drive circuit **12** starts scanning in the relevant frame in response to the vertical synchronizing signal Vs, and performs voltage output, which is based on the first gate clock signals GCK**1** and the second gate clock signals GCK**2**, from a low-level voltage Vgl to a high-level voltage Vgh for a specified period of time starting from the scanning signal line in each of the first stage G (**1**) up to final stage G (n).

Specifically, the scanning signal line drive circuit **12** sequentially sets TFT**1** (i, j) and TFT**2** (i, j) corresponding to the relevant scanning signal line G (j) to ON, and writes the display signal voltage that is output to the data signal line S (i) at that time to the first sub-pixel P**1** (i, j) and the second sub-pixel P**2** (i, j).

The data signal line drive circuit **13** outputs display signal voltage corresponding to each data signal line S (i) disposed on the display panel **11** at predetermined timing according to the horizontal synchronizing signal Hs, the vertical synchronizing signal Vs, the image data Data, a reference clock signal CLK, and a polarity reversal signal Pol among of which output from the control unit **17**.

As shown in FIG. **9**, the functional block of the data signal line drive circuit **13** comprises sampling memories **131**, data latch units **132**, D/A conversion circuits (DAC) **133**, and a display signal voltage generation circuit **134**.

The sampling memories **131** have data storage areas as many as the number of data signal lines S (i). In synchronization with the horizontal synchronizing signal Hs output from the control unit **17** and the reference clock signal CLK, the sampling memory **131** fetches image data corresponding to each pixel from the image memory **10** sequentially, starting from the data corresponding to the scanning signal line in the previous stage, in units of image data corresponding to the pixel for one scanning signal line (image data for one horizontal period). Specifically, each sampling memory **131** fetches image data corresponding to the relevant scanning signal line, and stores each of the image data fetched in the data storage area corresponding to the relevant scanning signal line S (i). In this case, the image data includes gradation levels to be displayed in each pixel. This gradation levels are displayed by each pixel as 8-bit digital data, for example. This 8-bit digital data is stored in each data storage area.

The image data of one horizontal period fetched by the sampling memory **131** is transferred from the sampling memory **131** to the data latch unit **132** in response to a request from the data latch unit **132** in the subsequent stage. After a completion of transferring the image data to the data latch unit **132**, the sampling memory **131** starts to fetch the image data corresponding to the scanning signal line of the next row for the next horizontal period. This is performed in synchronization with horizontal synchronizing signal Hs.

The data latch units **132** obtain image data for one horizontal period collectively from the sampling memories **131** according to horizontal synchronizing signal Hs, and output the obtained image data to the D/A conversion circuits **133** in the subsequent stage.

The D/A conversion circuit **133** comprises multiple DAC units **241** and output amplification circuits **242**. The display signal voltage supplied from the display signal voltage generation circuit **134** is selected by the DAC units **241**, which allows each image data output from the data latch units **132** to be converted into display signal voltages as corresponding analog signals, and then output to the data signal lines S (i) via the output amplification circuits **242**.

At this time, the D/A conversion circuits **133** convert digital image data output from the data latch units **132** into an analog display signal voltage, in response to the polarity reversal signals Pol output from the control unit **17**. Specifically, when the polarity reversal signal Pol is in high state Vsh, the D/A conversion circuits **133** perform D/A conversion to allow the image data output from the data latch units **132** to become display signal voltage having positive polarity. On the contrary, when the polarity reversal signal Pol is in low state Vsl, the D/A conversion circuits **133** perform D/A conversion to allow the image data output from the data latch units **132** to become display signal voltage having negative polarity. In other words, the D/A conversion circuits **133** perform D/A conversion to allow the voltage applied to the liquid crystal to have positive polarity when the polarity reversal signal Pol is in high state Vsh, and allow the voltage applied to the liquid crystal to have negative polarity when the polarity reversal signal Pol is in low state Vsl.

As shown in FIG. **10**, the display signal voltage generation circuit **134** comprises: a pair of ladder resistors **31** and **32**, multiple switches SY**0**, SY**1**, . . . , SY**255**, and switches SYa and SYb etc.. Each pair of ladder resistors **31** and **32** divides the voltage between terminal **255** (voltage VH) and terminal **256** (voltage VL) using multiple resistors suitable for the bit count p of the image data (8 bits in the embodiment of the present invention). The multiple switches SY**0**, SY**1**, . . . , SY**255** serves for selecting a desired ladder resistor of the pair. The switches SYa and SYb serve for switching the polarity of the voltage to be applied to the ladder resistors in response to the ladder resistor selected. The display signal voltage generation circuit **134** selects desired ladder resistors by the operation of each switch SY**0**, SY**1**, . . . , SY**255** based on the polarity reversal signal Pol output from the control unit **17**. At the same time, the display signal voltage generation circuit **134** switches the polarity of the voltage to be applied to the ladder resistors by the operation of the switches SYa and SYb, and applies each voltage divided by the ladder resistors to the voltage application lines V**0**, V**1**, . . . , V**255** as display signal voltage at a corresponding gradation level.

Specifically, when the polarity reversal signal Pol from the control unit **17** is at high level Vsh, the ladder resistor **31** is selected by the operation of each switch SY**0**, SY**1**, . . . , SY**255**. In addition, when the terminal **255***a* (voltage VH) and the terminal **256***b* (voltage VL) are selected by the operation of the switches SYa and SYb, the voltage between the terminals **255***a* (voltage VH) and **256***b* (voltage VL) is divided by multiple resistors RA**1**, RA**2**, . . . , RA**254** suitable for the bit count of the image data (8 bits in the embodiment of the present invention). Each voltage is applied to the voltage application lines V**0**, V**1**, . . . , V**255** as display signal voltage that allows a voltage having positive polarity to be applied to the liquid crystal, for example.

When the polarity reversal signal Pol from the control unit **17** is at low level Vsl, the ladder resistor **32** is selected by the operation of each switch SY**0**, SY**1**, . . . , SY**255**. In addition, when the terminals **256***a* (voltage VL) and **255***b* (voltage VH) are selected by the operation of the switches SYa and SYb, the voltage between the terminals **256***a* (voltage VL) and the terminal **255***b* (voltage VH) is divided by multiple resistors RB**1**, RB**2**, . . . , RB**254** suitable for the bit count of the image data (8 bits in the embodiment of the present invention), and each voltage is applied to voltage application lines V**0**,

V1, . . . , V255 as display signal voltage that allows a voltage having negative polarity to be applied to the liquid crystal, for example.

Each DAC unit **241** comprises: a decoder **243** and, selector switches SW0, SW1, . . . , SW255 which are connected to voltage application lines V0, V1, . . . , V255. In the decoder **243**, input the image data output from the data latch units **132** are decoded and output data signals that satisfy the number of gradation levels (i.e. bit count). Each selector switch SW0, SW1, . . . , SW255 is set to ON/OFF according to the data signals output from the decoder **243**. The selected voltage application lines V0, V1, . . . , V255 and a voltage output line SL are connected, and the display signal voltage which is applied to the selected voltage application lines V0, V1, . . . , V255 is supplied to the voltage output line SL. The display signal voltage applied to the voltage output line SL is then supplied to the data signal lines S (i) via the output amplification circuit **242**.

The common voltage generation circuit **14** applies identical common voltage Vc to the common electrode **115** and each auxiliary capacitance line C1 (j) and C2 (j) according to the polarity reversal signal Pol output from the control unit **17**. When the polarity reversal signal Pol is at a high level Vsh, the first common voltage Vcl is applied so as to allow a voltage having positive polarity to be applied to the liquid crystal. When the polarity reversal signal Pol is at a low level Vsl, the second common voltage Vch is applied so as to allow a voltage having negative polarity to be applied to the liquid crystal. In other words, the common voltage generation circuit **14** applies rectangular AC voltage to the common electrode **115** and each auxiliary capacitance line C1 (j) and C2 (j).

The control unit **17** outputs the polarity reversal signal Pol to allow the voltage to be applied to the liquid crystal to have opposite polarities between adjacent pixels (pixels adjacent to each other in the pixel row direction), and furthermore to allow the voltage to be applied to the liquid crystal to have opposite polarities by each frame.

Thus, the voltage Vlc1 as shown in FIG. **11** is applied to the liquid crystal in the first sub-pixel P1 (i, j) of each pixel P (i, j) over an approximately entire period in one flame. In FIG. **11**, ΔV shows a pull-in voltage that is generated when write of display signal voltage into a pixel is completed due to the effect of parasitic capacitance between scanning signal lines and pixel electrodes. It is desirable that a center of amplitude of the common voltage Vc is set to a value shifting the center of amplitude of the display signal voltage by ΔV in the direction of generation of ΔV.

The step-down voltage generation circuit **15** applies a step-down voltage Vd to the step-down capacitance lines D (j) based on the polarity reversal signal Pol output from the control unit **17** and the inherent information Inf stored in the inherent information storage unit **16**. A step-down voltage Vd may be a center voltage of the common voltage Vc, i.e. Vcl+(Vch−Vcl)/2. A step-down voltage Vd may be a center voltage of the common voltage Vc, i.e. Vcl+(Vch−Vcl)/2, and this voltage value changes in synchronization with the polarity reversal signal Pol.

Specifically, the step-down voltage generation circuit **15** applies voltage to the step-down capacitance lines D (j) so that a potential fluctuation at the second pixel electrode E2 (i, j) is reduced to be smaller than a potential fluctuation at the common electrode **115** by step-down capacitance Cd (i, j) which is formed between the second pixel electrode E2 (i, j) and the step-down capacitance line D (j).

Therefore, this allows that voltage Vlc1 and Vlc2 as shown in FIG. **12** are applied to the liquid crystal at the second sub-pixel P2 (i, j) of each pixel P (i, j), thus ensuring that the mean voltage, i.e. (Vlc1+Vlc2)/2, applied to the liquid crystal during one frame is smaller than the voltage Vlc1 applied to the liquid crystal at the first sub-pixel P1 (i, j).

In other words, during the period T1, in which the potential of the common electrode **115** is equivalent to the potential of the relevant common electrode **115** at the time when display signal voltage is written into the second pixel electrode E2 (i, j) via TFT2 (i, j), the voltage applied to the liquid crystal at the second sub-pixel P2 (i, j) is equal to the voltage Vlc1 applied to the liquid crystal at the first sub-pixel P1 (i, j). Meanwhile, during the period T2, in which the potential of the common electrode **115** is not equivalent to the potential of the relevant common electrode **115** at the time when display signal voltage is written into the second pixel electrode E2 (i, j) via TFT **2** (i, j), the voltage, expressed as Vlc2, applied to the liquid crystal at the second sub-pixel P2 (i, j) is smaller than the voltage Vlc1 applied to the liquid crystal at the first sub-pixel P1 (i, j).

Consequently, as shown in FIG. **13**, a curve VT2, which represents a relationship between a display signal voltage and a transmission intensity at the second sub-pixels P2 (i, j) can be shifted to with respect to a curve VT1, which represents a relationship between a display signal voltage and a transmission intensity at the first sub-pixels P1 (i, j). Therefore, multiple relationships between display signal voltage and transmission intensity at each display pixel P (i, j) can be obtained, and thus the degree of dependence on viewing angles in the liquid crystal display device **1** can be improved.

The difference ΔVlc between voltages Vlc1 and Vlc2 can be found for example by using the following equations (1) to (4)

$$\Delta Vlc=(A-B)/R \tag{1}$$

$$A=\{Clc2(i,j)+Ccs2(i,j)\}\times Vcl \tag{2}$$

$$B=\{Clc2(i,j)+Ccs2(i,j)\}\times Vch \tag{3}$$

$$R=Clc2(i,j)+Ccs2(i,j)+Cd. \tag{4}$$

To bring the curve VT2, which represents the relationship between the display signal voltage and transmission intensity at the second sub-pixels P2 (i, j), relatively close to VT1, which represents the relationship between the display signal voltage and transmission intensity at the first sub-pixels P1 (i, j), the step-down voltage Vd as shown in FIG. **14**A may be oscillated as shown in FIG. **15**A to be in phase with the common voltage Vc output from the common voltage generation circuit **14**, thus minimizing the potential difference from the common voltage Vc.

On the contrary, to bring the curve VT2, which represents the relationship between the display signal voltage and transmission intensity at the second sub-pixels P2 (i, j), relatively away from VT1, which represents the relationship between the display signal voltage and transmission intensity at the first sub-pixels P1 (i, j), the step-down voltage Vd as shown in FIG. **15**B may be oscillated to be in opposite phase with the common voltage Vc output from the common voltage generation circuit **14**, thus maximizing the potential difference from the common voltage Vc.

According to the present embodiment, since the relationship between the display signal voltage and transmission intensity can be shifted easily by adjusting the step-down voltage Vd applied to the step-down capacitance lines D (j), the viewing-angle dependence of the liquid crystal display can be improved by simple circuit configuration. Furthermore, the degree of viewing-angle dependence of it can be adjusted.

For example, after a display panel **11** has been manufactured, differences of viewing-angle dependence among a plural display panel **11** can be minimized by followings configurations. The inherent information storage unit **16** is made to store the value of step-down voltage Vd which can be controlled to the similar extent as the control of viewing-angle dependence of other display panels **11** as the inherent information Inf. And a step-down voltage generation circuit **15** is configured to apply step-down voltage Vd having an amplitude based on the inherent information Inf stored in the relevant inherent information storage unit **16** to the step-down capacitance line D (j).

In addition, since the step-down voltage generation circuit **15** needs to adjust the amplitude of step-down voltage Vd only, a simple step-down voltage generation circuit **15** can be configured. If sub-pixels have different data signal lines, and different display signal voltages are applied to each sub-pixel via corresponding data signal lines and TFTs, for example, multiple display signal voltage generation circuits relatively large in size are required to apply different display signal voltages to each sub-pixel as described above. However, according to the embodiment of the present invention, it does not need complex configuration, and the viewing-angle dependence can be adjusted with a simpler circuit configuration compared with configuration mentioned above. Moreover, since the common electrode **115** need not be separated for each region within a display pixel, the number of manufacturing processes does not increase.

In addition, since display signal voltage is applied directly to the pixel electrodes of each sub-pixel via corresponding TFTs in the present embodiment, the voltage is applied to the liquid crystal more stably compared with the one in which voltage is applied to the pixel electrodes only via capacitances.

Meanwhile, an EEPROM (Electrically Erasable Programmable Read Only Memory), which is one of nonvolatile memories, can be used for an inherent information storage unit **16**. The EEPROM has the state that no information has been written in it i.e. "white" state at the start of manufacturing of a display device **1**. After the completion of manufacturing of liquid crystal display device **1**, predetermined information can be stored in the inherent information storage unit **16** by connecting a system device for writing in an EEPROM to a signal terminal for writing **161** in accordance with the finishing state of the relevant liquid crystal display device **1**.

It is preferable to set the writing voltage Vpp into the inherent information storage unit **16** at a level higher than the reference supply voltage Vcc to be input to the power control circuit for the relevant liquid crystal display device **1** so that the information stored in the inherent information storage unit **16** can be prevented to be erased carelessly by the influence of the reference supply voltage Vcc.

The above embodiment explains a case that the shape and the area of the first pixel electrodes E**1** (i, j) in the first sub-pixels P**1** (i, j) are the same as those of the second pixel electrodes E**2** (i, j) of the second sub-pixels P**2** (i, j). Hereinafter, a typical modification of the layout of the first sub-pixels P**1** (i, j) and the second sub-pixels P**2** (i, j) in display pixels P (i, j) will be described.

FIG. **16** is a partially magnified plan view showing the first example of the layout of first and second sub-pixels in pixels P (i, j). As shown in FIG. **16**, a shape and an area of a first pixel electrode E**1** (i, j) and a second pixel electrode E**2** (i, j) may differ. In this case, however, the size and shape of each of the first sub-pixels P**1** (i, j) are identical, and the size and shape of each of the second sub-pixels P**2** (i, j) are also identical. Consequently, two sub-pixels, the first sub-pixel P**1** (i, j) disposed on the side of the previous row of the scanning line G (j), namely on the side of the j−1 row, and the second sub-pixel P**2** (i, j) disposed on the side of the following row of the scanning line G (j), namely on the side of the j+1 row, constitute a pixel pattern. This pixel pattern is disposed on all of the intersections between each row and column. The region enclosed in the broken line represents pixels for one row and three columns. The first sub-pixels P**1** (i, j) are disposed on the upper side of the scanning line G (j) via the first switching devices TFT**1** (i, j). The second sub-pixels P**2** (i, j) are disposed on the lower side of the scanning line G (j) via the second switching devices TFT**2** (i, j).

In FIG. **16**, each of the first sub-pixels P**1** (i, j) is disposed adjacent to the second sub-pixels P**2** (i, j), which are disposed on the lower side of the scanning line G (j−1) of the pixels P (i, j) in the previous row. Each of the second sub-pixels P**2** (i, j) is disposed adjacent to the first sub-pixels P**1** (i, j), which are disposed on the upper side of the scanning line G (j+1) of the pixels P (i, j) in the following row, namely on the upper side of the scanning line G (j+1) of the following row.

The auxiliary capacitance line C**1** (j) for the first sub-pixel P**1** (i, j) is disposed on the upper side of the scanning line G (j) in parallel to the scanning line G (j).

The auxiliary capacitance line C**2** (j) for the second sub-pixel P**2** (i, j) is disposed on the lower side of the scanning line G (j) in parallel to the scanning line G (j). The step-down capacitance line D (j) of the second sub-pixel P**2** (i, j) is disposed on the upper side of the auxiliary capacitance line C**2** (j) in parallel to the scanning line G (j).

The above embodiment is a case that the step-down capacitance line D (j) is disposed on the upper side of the auxiliary capacitance line C**2** (j) in the second sub-pixels P**2** (i, j) closer to the scanning line G (j). Unlike the embodiment in FIG. **16**, the auxiliary capacitance line C**2** (j) may be disposed on the upper side of the step-down capacitance line D (j) closer to the scanning line G (j).

The above embodiment is a case that the layout of the first sub-pixels P**1** (i, j) and the second sub-pixels P**2** (i, j) is identical between the pixels adjacent to each other in the direction of the length of the scanning signal lines G (j) and step-down capacitance lines D (j). However, as shown in FIGS. **17** and **18** later, the layout of the first sub-pixels P**1** (i, j) and the second sub-pixels P**2** (i, j) may be reversed between the pixels adjacent to each other in the direction of the length of the scanning signal lines G (j) and step-down capacitance lines D (j).

FIG. **17** is a partially magnified plan view showing the second example of the layout of first and second sub-pixels in pixels P (i, j). As shown in FIG. **17**, a pixel P (i, j) comprises a first sub-pixel P**1** (i, j), which has smaller area, and a second sub-pixel P**2** (i, j), which has larger area. The layout of the pixels in the same column as the pixel P (i, j), the layout of P (i, j−1) and P (i, j+1) for example, is identical to that of the pixel P (i, j). Meanwhile, the layout of the pixels in the same row as the pixel P (i, j), the layout of P (i−1, j) and P (i+1, j) for example, is reversed from that of the pixel P (i, j). Specifically, in P (i−1, j) and P (i+1, j), the second sub-pixels P**2** (i−1, j) are disposed on the upper side of the scanning line G (j) via the second switching device TFT**2** (i−1, j). While, the first sub-pixels P**1** (i−1, j) are disposed on the lower side of the scanning lien G (j) via the first switching device TFT**1** (i−1, j).

The auxiliary capacitance line C**1** (j) for the first sub-pixel P**1** (i, j) and the auxiliary capacitance line C**2** (j) for the second sub-pixels P**2** (i−1, j) and P**2** (i+1, j), which are disposed on other columns that are adjacent to column j, are formed to be a common line, and this common line is arranged in parallel to the scanning line G (j).

The auxiliary capacitance line C2 (j) for the second sub-pixel P2 (i, j) and the auxiliary capacitance lines C1 (j) for the first sub-pixels P1 (i−1, j) and P1 (i+1, j) disposed on other columns that are adjacent to column j are formed to be a common line, and this common line is arranged in parallel to the scanning line G (j).

The step-down capacitance line D (j) for the second sub-pixel P2 (i, j) and the step-down capacitance lines D (j) for the second sub-pixel P2 (i−1, j) and P2 (i+1, j) disposed on other columns that are adjacent to column j are formed to be a common line, and this common line is arranged in parallel to the scanning line G (j).

FIG. **18** is a partially magnified plan view showing the third example of the layout of first and second sub-pixels in pixels P (i, j). As shown in FIG. **18**, the pixel layout is the same as that shown in FIG. **17**, except that an area of the first sub-pixels P1 (i, j) and that of the second sub-pixels P2 (i, j) are approximately the same, and that the interconnection wiring of the step-down capacitance line D (j) is different in the second sub-pixel P2 (i, j).

The step-down capacitance line D (j) for the second sub-pixel P2 (i, j) includes the step-down capacitance line D (j+1), which is in the columns at left and right (columns i−1 and i+1) and in the following row as well as the interconnection wiring portion for the following row of the scanning line G (j). In FIG. **18**, the interconnection wiring portion is in the shape of a staggered clamp. Consequently, the step-down capacitance line D (j) of the second sub-pixel P2 (i, j) extends along the second sub-pixel P2 (i, j) of the relevant row and the second sub-pixel P2 (i, j+1) of the following row alternately in the shape of polygonal line in the direction of the scanning line **21** and in the shape of waves by column.

The above embodiment is a case that two auxiliary capacitance lines are disposed for each pixel P (i, j). However, as shown in FIG. **19** later, an auxiliary capacitance line can be shared by sub-pixels.

FIG. **19** is a partially magnified plan view showing the fourth example of the layout of first and second sub-pixels in pixels P (i, j). The pixel **15** in FIG. **19** differs from the pixel **15** in FIG. **16** in that the auxiliary capacitance line C1 (j) for the first sub-pixel P1 (i, j) and the auxiliary capacitance line C2 (j−1) for the second sub-pixel P2 (i, j−1) disposed on the side of the scanning line G (j−1) of the previous row are formed to be a common line.

Similarly, the auxiliary capacitance line C2 (j) for the second sub-pixel P2 (i, j) disposed on the subsequent row of the scanning line G (j) and the auxiliary capacitance line C1 (j+1) for the first sub-pixel P1 (i, j+1) disposed on the side of the subsequent row of the scanning line G (j), namely scanning line G (j+1), are formed to be a common interconnection wiring, and this common interconnection wiring is disposed in parallel to the scanning line G (j).

The electrode and interconnection wiring structures described above simplifies mask patterns for fabrication of auxiliary capacitance lines C1 and C2, thus reducing cost.

According to the pixel layouts as shown in FIGS. **16**, **17**, **18**, and **19**, it is preferable that two regions having different relationships between display signal voltage and transmission intensity can be disposed so as to realize a higher uniformity.

The present invention allows the difference in viewing-angle dependence between liquid crystal panels to be corrected easily without increasing the number of manufacturing processes even after the manufacturing is completed.

Various modifications and variations can be made in the present invention within the scope of the appended claims, not limited to the above embodiments, and it is not without saying that those variations are also included in the scope of the present invention.

What is claimed is:

1. A liquid crystal display device with multiple pixels provided therein, comprising:

multiple pixel electrodes arranged in a horizontal direction and a vertical direction, said pixel electrode including a first sub-pixel electrode and a second sub-pixel electrode disposed adjacent to said first sub-pixel electrode;

a common electrode disposed opposite to said multiple pixel electrodes;

plural scanning signal lines extending in the horizontal direction;

a first liquid crystal capacitance formed with a liquid crystal sandwiched between said common electrode and said first sub-pixel electrode;

a first auxiliary capacitance formed with a solid dielectric material sandwiched between said first sub-pixel electrode and a first auxiliary capacitance line extending in the horizontal direction;

a second liquid crystal capacitance formed with said liquid crystal sandwiched between said common electrode and said second sub-pixel electrode;

a second auxiliary capacitance formed with a solid dielectric material sandwiched between said second sub-pixel electrode and a second auxiliary capacitance line extending in the horizontal direction;

a step-down capacitance formed with a solid dielectric material sandwiched between said second sub-pixel electrode and a step-down capacitance line, said step-down capacitance line being different from any one of said plural scanning signal lines and from said second auxiliary capacitance line, and extending in the horizontal direction;

a first voltage application means for applying a common first voltage to said common electrode, said first auxiliary capacitance line, and to said second auxiliary capacitance line; and

a second voltage application means for applying a second voltage, which is different from a voltage applied to said scanning signal line and from said first voltage, to said step-down capacitance line,

wherein said first voltage is a rectangular AC voltage that oscillates at a specified amplitude, and

said second voltage is a rectangular AC voltage whose amplitude is smaller than said specified amplitude of said first voltage.

2. The liquid crystal display device as set forth in claim **1**, wherein said rectangular AC voltage as said first voltage is in phase with said rectangular AC voltage as said second voltage.

3. The liquid crystal display device as set forth in claim **1**, wherein said rectangular AC voltage as said first voltage is in opposite phase with respect to said rectangular AC voltage as said second voltage.

4. The liquid crystal display device as set forth in claim **1**, further comprising:

multiple data signal lines extending in the vertical direction;

a first switching device connected to said first sub-pixel electrode; and

a second switching device connected to said second sub-pixel electrode,

wherein said first and said second switching devices are connected to the same data signal lines and the same scanning signal lines.

5. The liquid crystal display device as set forth in claim 4, wherein said step-down capacitance line is disposed on the same layer as said scanning signal lines.

6. The liquid crystal display device as set forth in claim 4, wherein said first sub-pixel electrode and said second sub-pixel electrode are disposed in different directions with respect to said scanning signal lines.

7. The liquid crystal display device as set forth in claim 1, wherein an area of said first sub-pixel electrode is identical to an area of said second sub-pixel electrode.

8. The liquid crystal display device as set forth in claim 1, wherein an area of said first sub-pixel electrode is not identical to an area of said second sub-pixel electrode.

9. The liquid crystal display device as set forth in claim 1, wherein said first auxiliary capacitance line, said second auxiliary capacitance line, and said step-down capacitance line are disposed on the same layer.

10. A liquid crystal display device with multiple pixels provided therein, comprising:

multiple pixel electrodes arranged in a horizontal direction and a vertical direction, said pixel electrode includes a first sub-pixel electrode and a second sub-pixel electrode disposed adjacent to said first sub-pixel electrode;

a common electrode disposed opposite to said plural pixel electrodes;

multiple scanning signal lines extending in the horizontal direction; and

a first voltage application means and a second voltage application means both for applying voltage,

wherein:

said first sub-pixel electrode is disposed opposite to said common electrode via a liquid crystal layer, and is disposed opposite to a first auxiliary capacitance line extending in the horizontal direction via an insulating layer,

said second sub-pixel electrode is disposed opposite to said common electrode via said liquid crystal layer, and is disposed opposite to a second auxiliary capacitance line extending in the horizontal direction via said insulating layer, and further, said second sub-pixel electrode is disposed opposite to a step-down capacitance line via said insulating layer, said step-down capacitance line being different from any one of said multiple scanning signal lines and from said second auxiliary capacitance line, and extending in the horizontal direction,

said first voltage application means applies a common first voltage to said common line, said first auxiliary capacitance line, and to said second auxiliary capacitance line, and

said second voltage application means applies a second voltage, which is different from a voltage applied to said scanning signal line and from said first voltage, to said step-down capacitance line,

wherein said first voltage is a rectangular AC voltage that oscillates at a specified amplitude, and

said second voltage is a rectangular AC voltage whose amplitude is smaller than said specified amplitude of said first voltage.

11. The liquid crystal display device as set forth in claim 10, wherein said rectangular AC voltage as said first voltage is in phase with said rectangular AC voltage as said second voltage.

12. The liquid crystal display device as set forth in claim 10, wherein said rectangular AC voltage as said first voltage is in opposite phase with said rectangular AC voltage as said second voltage.

13. The liquid crystal display device as set forth in claim 10, further comprising:

multiple data signal lines extending in the vertical direction;

a first switching device connected to said first sub-pixel electrode;

a second switching device connected to said second sub-pixel electrode,

wherein said first and said second switching devices are connected to the same data signal lines and the same scanning signal lines.

14. The liquid crystal display device as set forth in claim 13, wherein said step-down capacitance line is formed on the same layer as the scanning signal lines.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US8368626	公开(公告)日	2013-02-05
申请号	US12/407771	申请日	2009-03-19
[标]申请(专利权)人(译)	卡西欧计算机株式会社		
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IPC分类号	G09G3/36 G02F1/133 G02F1/1343		
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摘要(译)

一种具有多个像素的液晶显示装置，包括：第一子像素，包括：公共电极和第一像素电极之间的第一液晶电容;以及第一像素电极和第一辅助电容电极之间的第一辅助电容;第二子像素，包括：公共电极和第二像素电极之间的第二液晶电容，第二像素电极和第二辅助电容电极之间的第二辅助电容，以及第二像素电极和第二像素电极之间的降压电容。降压电容电极;第一电压施加单元，用于将公共第一电压施加到公共电极，第一辅助电容电极和第二辅助电容电极;第二电压施加单元，用于将与第一电压不同的第二电压施加到降压电容电极。