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(54) IN PLANE FRINGE FIELD SWITCHING MODE LCD REALIZING HIGH SCREEN QUALITY

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(57) **ABSTRACT**

Disclosed is an IP-FFS mode LCD realizing high screen quality by preventing a lowering of transmittance. The IP-FFS mode LCD comprises: a transparent insulating substrate; a plurality of gate bus lines and data bus lines cross-arranged on the substrate; a plurality of common bus lines arranged to be parallel with the gate bus line; a thin film transistor arranged at the intersection of the gate bus line and the data bus line; a counter electrode arranged in each unit pixel, including a first body arranged on the edge of one side of unit pixel to be parallel with the data bus line and a plurality of first branches, the end of one side being in contact with the first body, wherein the first branches have a predetermined angle symmetric with respect to the common bus line; and a pixel electrode arranged in each unit pixel, including a second body arranged on the lower part of the other end of the first branch on the other edge of the unit pixel, being parallel with the data bus line and a plurality of second branches, the other end being in contact with the second body and the one end being extended to the upper part of the first branch, wherein the second branches are arranged on the same layer with the first branches, forming parallel between the first branches.

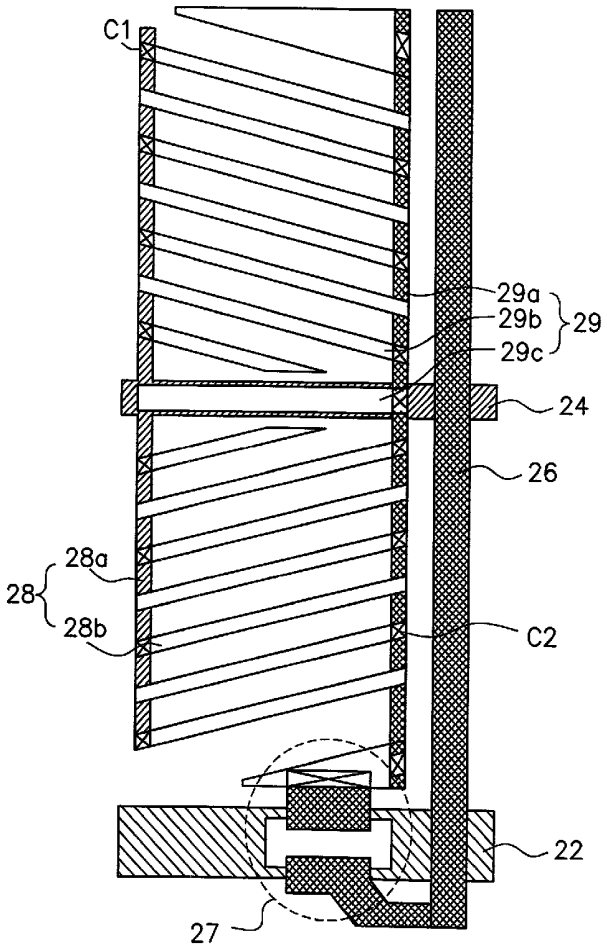


FIG. 1

(PRIOR ART)

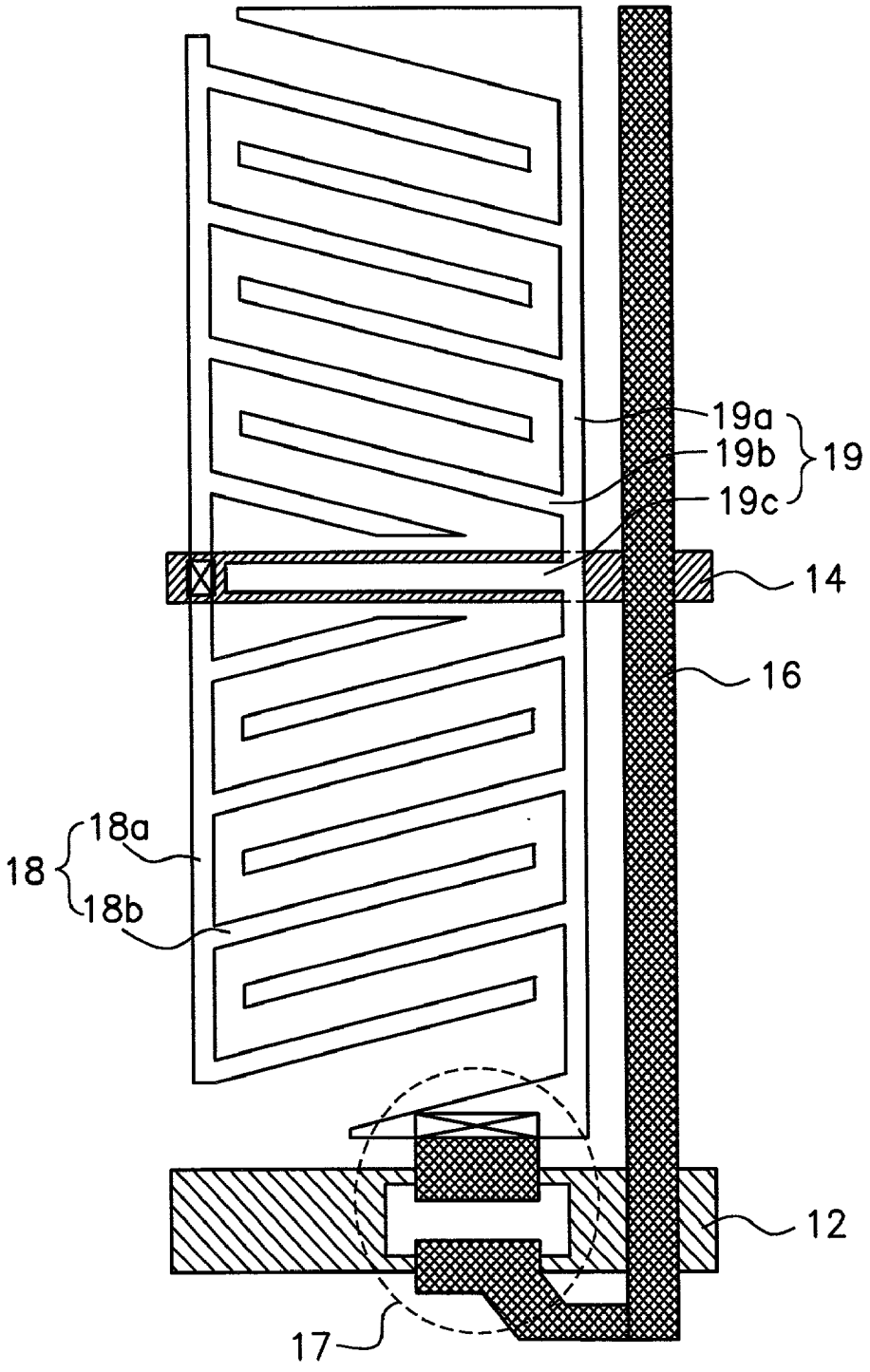


FIG.2

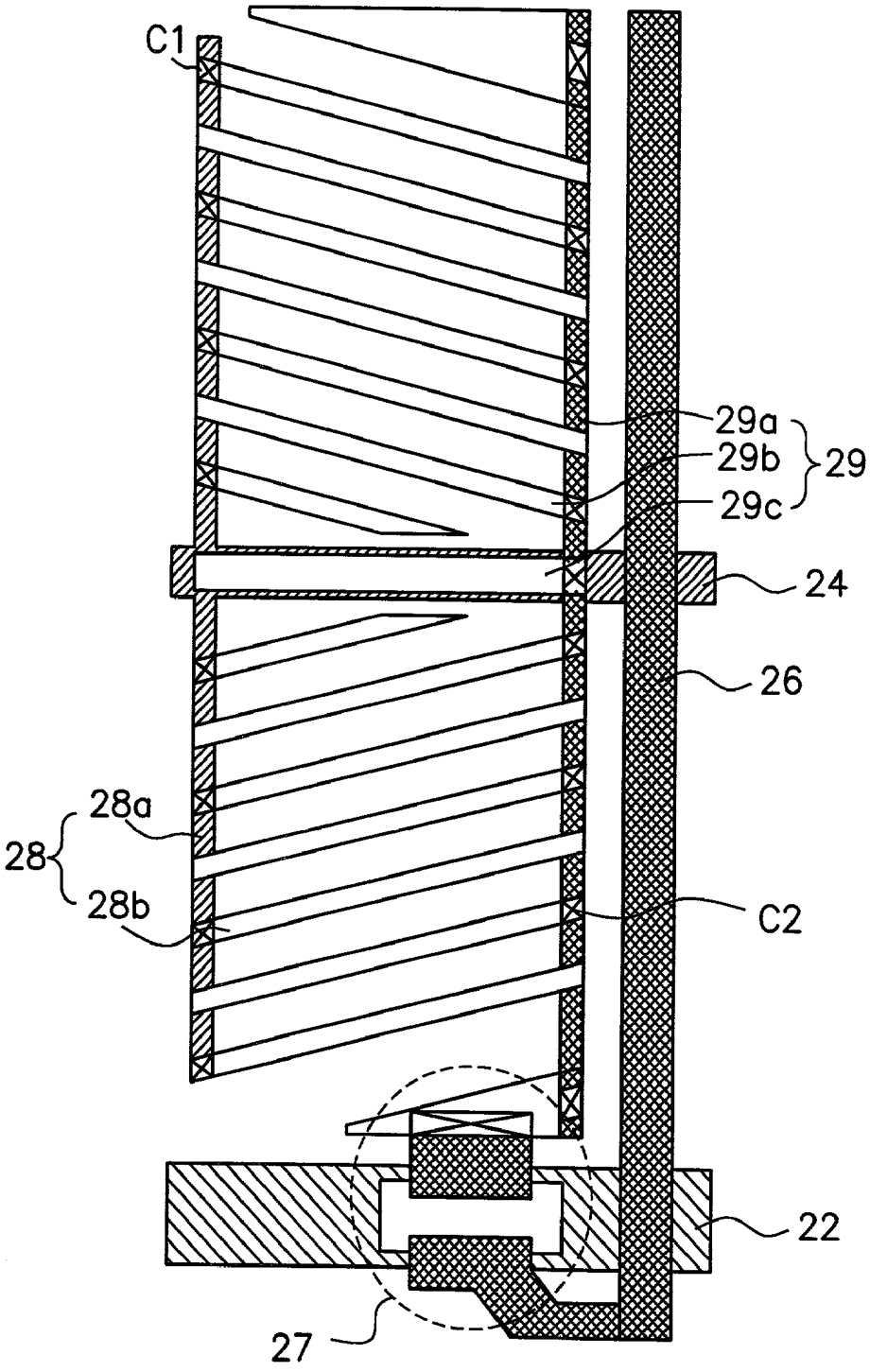
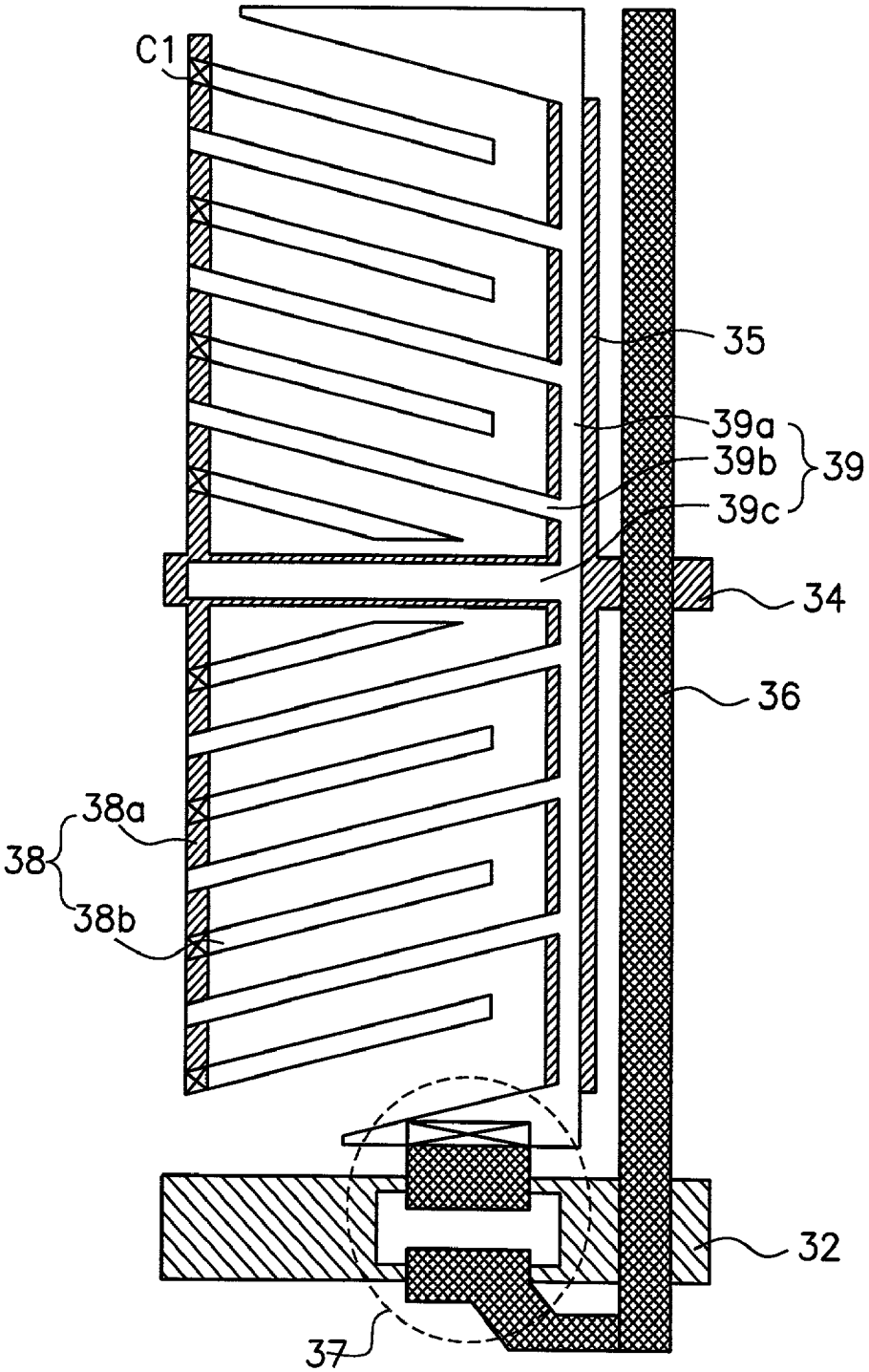


FIG.3



IN PLANE FRINGE FIELD SWITCHING MODE LCD REALIZING HIGH SCREEN QUALITY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a Liquid Crystal Display (hereinafter, referred to as LCD) and, more particularly, to an In Plane Fringe Field Switching Mode LCD wherein a counter electrode and a pixel electrode are formed on the same layer.

[0003] 2. Description of the Prior Art

[0004] In TN (Twisted Nematic) mode LCD, liquid crystal molecules are twisted in 90° by the voltage applied to a counter electrode on an upper substrate and a pixel electrode on a lower substrate, thereby realizing display. The TN mode LCD has advantages that it is easy to drive and the fabrication process is simple. However, it also has disadvantages that viewing angle is narrow and response time is slow, thereby there are limitations in its application.

[0005] Therefore, In Plane Switching (hereinafter, referred to as IPS) mode LCD has been proposed to solve the problem of the TN mode. The IPS mode LCD has advantages of wide viewing angle and rapid response time, however, it has disadvantages of low aperture ratio and transmittance due to the fact that counter and pixel electrodes are made of opaque metals.

[0006] In order to overcome low aperture ratio and transmittance of the IPS mode LCD, a Fringe Field Switching (hereinafter, referred to as FFS) mode LCD has been proposed by the present applicant. In the FFS mode LCD, the counter electrode and the pixel electrode are made of transparent metals, for example, ITO and the distance between the counter electrode and the pixel electrode is narrower than a cell gap, thereby realizing high brightness and wide viewing angle.

[0007] And, the present applicant also has proposed an In Plane Fringe-Field Switching (hereinafter, referred to as IP-FFS) mode LCD realizing high screen quality by arranging the counter and pixel electrodes on the same layer.

[0008] **FIG. 1** is a plan view showing the electrode structure of conventional IP-FFS mode LCD.

[0009] Referring to **FIG. 1, a** gate bus line **12** and a data bus line **16** are cross-arranged. A thin film transistor **17** is arranged at the intersection of the gate bus line **12** and the data bus line **16**, as a switch. A common bus line **14** is arranged on the center of unit pixel defined by the gate bus line **12** and the data bus line **16**, being parallel with the gate bus line **12**.

[0010] A counter electrode **18** and a pixel electrode **19** are formed on the same layer by ITO patterning, respectively including bodies **18***a*, **19***a* and a plurality of branches **18***b*, **19***b*, **19***c*. The branches of counter electrode and pixel electrode **18***b*, **19***b* are alternately arranged, having a predetermined angle symmetric with respect to the common bus line **14**. The counter electrode **18** is in contact with the common bus line **14**. The pixel electrode **19** is in contact with the thin film transistor **17**, further including a center branch **19***c* on the upper part of common bus line **14**, being parallel with the common bus line. The center branch **19***c* is formed in order to form storage capacitance.

[0011] In the IP-FFS mode LCD, the counter electrode and the pixel electrode are arranged on the same layer by ITO patterning, thereby having advantages in afterimages and cost reduction, compared with FFS mode LCD wherein the counter electrode has a plate structure and the pixel electrode has a slit structure, arranged on the different layers. And, in the IP-FFS mode LCD, the counter electrode and the pixel electrode are arranged in the unit pixel to form two domains, thereby preventing color shift generation.

[0012] As a result, the IP-FFS mode LCD has advantages in afterimages and cost reduction, compared with the FFS mode LCD, thereby realizing high screen quality.

[0013] However, in the IP-FFS mode LCD, a short may be generated between the counter electrode and the pixel electrode since they are formed on the same layer. In order to prevent the short generation, branches of counter electrode and pixel electrode are arranged with a distance of over 3 μm. The body of counter electrode also maintains the same distance with the branch end of pixel electrode and the body of pixel electrode maintains the same distance, over 3 μm, with the branch end of counter electrode.

[0014] When the body of counter electrode and the branch end of pixel electrode, and the body of pixel electrode and the branch end of counter electrode are arranged with a good distance, electric fields are formed between each body and branch end. The direction of electric field corresponds to initial arrangement of rubbed liquid crystal molecules. Therefore, liquid crystal molecules are not twisted in the regions between the body of each electrode and the branch end thereof, thereby lowering transmittance of the IP-FFS mode LCD.

SUMMARY OF THE INVENTION

[0015] Therefore, an object of the present invention is to provide an IP-FFS mode LCD capable of realizing high screen quality by preventing lowering of transmittance.

[0016] In order to accomplish the above-mentioned object, the present IP-FFS mode LCD comprises: a transparent insulating substrate; a plurality of gate bus lines and data bus lines cross-arranged on the substrate to define a unit pixel; a plurality of common bus lines arranged on the center of unit pixels to be parallel with the gate bus line; a thin film transistor arranged at the intersection of the gate bus line and the data bus line; a counter electrode arranged in each unit pixel, including a first body arranged to be parallel with the data bus line on the edge of one side of the unit pixel and a plurality of first branches, the end of one side being in contact with the first body wherein the first branches are made of ITO and arranged having a predetermined angle symmetric with respect to the common bus line; and a pixel electrode arranged in each pixel to be in contact with the thin film transistor, including a second body arranged to be parallel with the data bus line on the lower part of the other end of the first branch and a plurality of second branches, the end thereof being in contact with the second body and the other end is extended to the upper part of first branch wherein the second branches are made of ITO and arranged on the same layer of the first branches, to be parallel with each other between the first branches.

[0017] And, the IP-FFS mode LCD of the present embodiment further comprises a gate insulating layer interposed between the gate bus line and the data bus line and a protective layer between the data bus line and first and second branches of counter and pixel electrodes.

[0018] According to the present embodiment, the first body of counter electrode is formed in a built-in type with the common bus line and the second body of the pixel electrode is arranged on the same layer with the data bus line. And, the first branch of counter electrode is in contact with the first body by a first contact hole passing through the protective layer and the gate insulating layer, and the second branch of pixel electrode is in contact with the second body by a second contact hole passing through the protective layer. Moreover, the pixel electrode further comprises a center branch arranged on the upper part of common bus line to form storage capacitance.

[0019] According to another embodiment of the present invention, the IP-FFS mode LCD includes a transparent insulating substrate; a plurality of gate bus lines and data bus lines cross-arranged on the substrate to define a unit pixel; a plurality of common bus lines arranged on the central part of unit pixels to be parallel with the gate bus line, having a storage capacitance electrode arranged adjacent to the data bus line in unit pixel and parallel therewith; a thin film transistor arranged at the intersection of the gate bus line and the data bus line; a counter electrode arranged in each unit pixel, including a first body arranged on one edge of unit pixel to be parallel with the data bus line and a plurality of first branches, the end of one side being in contact with the first body and the end of other side being separated from the storage capacitance electrode, wherein the first branches are made of ITO and arranged having a predetermined angle symmetric with respect to the common bus line; and a pixel electrode arranged in each unit pixel to be in contact with the thin film transistor, including a second body arranged on the edge of other side of unit pixel to be parallel with the data bus line and overlap with the storage capacitance electrode and a plurality of second branches extended from the second body to the upper part of first body, wherein the second branches are made of ITO and arranged on the same layer with the first branches, forming parallel between the first branches.

[0020] And, the IP-FFS mode LCD of the present embodiment further comprises a gate insulating layer interposed between the gate bus line and the data bus line and a protective layer between the data bus line and the first and the second branches of counter and pixel electrodes.

[0021] According to the present embodiment, the first body of counter electrode is formed in built-in type with the common bus line and second body of pixel electrode is formed in built-in type with the second branch through ITO patterning. And, the first branch of counter electrode is in contact with the first body by a contact hole passing through the protective layer and the gate insulating layer. Moreover, the pixel electrode further comprises a center branch arranged on the upper part of common bus line to form storage capacitance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The objects and features of the invention may be understood with reference to the following detailed description of an illustrative embodiment of the invention, taken together with the accompanying drawings.

[0023] **FIG. 1** is a plan view showing an electrode structure of conventional IP-FFS mode LCD.

[0024] **FIG. 2** is a plan view showing an IP-FFS mode LCD according to an embodiment of the present invention.

[0025] **FIG. 3** is a plan view showing an IP-FFS mode LCD according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Referring to **FIG. 2, a** plurality of gate bus lines **22** and data bus lines **26** are cross-arranged on a transparent insulating substrate, desirably, on a glass substrate (not illustrated) . A gate insulating layer (not illustrated) is interposed between the gate bus line **22** and the data bus line **26**. A common bus line **24** is arranged on a center part of unit pixel defined by the gate bus line **22** and the data bus line **26**, being parallel with the gate bus line **22**. A thin film transistor **27** is arranged at the intersection of the gate bus line **22** and the data bus line **26**, as a switching device. A counter electrode **28** and a pixel electrode **29** are arranged in each unit pixel, respectively including bodies **28***a*, **29***a* and a plurality of branches **28***b*, **29***b*, **29***c*. A protective layer (not illustrated) is interposed between the data bus line **26** and the branches **28***b*, **29***b*, **29***c* of counter electrode **28** and pixel electrode **29**.

[0027] The body of counter electrode is arranged on the edge of one side of unit pixel to be parallel with the data bus line **26**. The body **28***a* of counter electrode is formed at the same time with the gate bus line **22** and the common bus line **24**, in a built-in type with the common bus line **24**. The branches **28***b* of counter electrode are formed on the protective layer through ITO patterning and arranged having a predetermined angle symmetric with respect to the common bus line **24**. In the branches **28***b* of counter electrode, the end of one side is in contact with the body **28***a* and the end of the other side is arranged on the upper part of body **29***a* of pixel electrode. The body **28***a* and the branch **28***b* of counter electrode maintain a contact C1 by a first contact hole (not illustrated) passing through the protective layer and the gate insulating layer.

[0028] The body **29***a* of pixel electrode is arranged on the edge of the other side of unit pixel to be parallel with the data bus line **26**. The body **29***a* of the pixel electrode is formed on the gate insulating layer at the same time with the data bus line **26**. The branches **29***b*, **29***c* of pixel electrode are formed on the same layer with the branches **28***b* of the counter electrode, that is, on the protective layer, through ITO patterning and arranged between branches **28***b* of adjacent counter electrode to be parallel therewith.

[0029] The pixel electrode **29** further includes a center branch **29***c* arranged on the upper part of common bus line **24**, being parallel therewith, to form storage capacitance. The body **29***a* and the branches **29***b*, **29***c* of the pixel electrode maintain contact C2 by a second contact hole (not illustrated) passing through the protective layer.

[0030] The bodies **28***a*, **29***a* of the counter and the pixel electrodes are formed to have a predetermined width, desir-

ably, 6 μm. The branches **28***b*, **29***b*, **29***c* of the counter and pixel electrodes also have a predetermined width, desirably, less than 8 μm and the center branch **29***c* of pixel electrode has a width of approximately 8 μm to have storage capacitance. The branches **28***b*, **29***b* of counter and pixel electrodes are arranged with a distance of less than 10 μm, more desirably, 3~10 μm.

[**0031**] Although it is not shown in the drawings, a lower substrate having the above structure are combined with an upper substrate having a color filter, with a liquid crystal layer interposed, thereby completing IP-FFS mode LCD. The horizontal alignment layers are attached to inner sides of each substrate and polarizing plates are attached to outer sides thereof.

[**0032**] According to the present invention, the body of counter electrode is arranged on the substrate having a common bus line and the body of pixel electrode is arranged on a gate insulating layer having a data bus line. Therefore, it is possible to extend the branches of counter and pixel electrodes arranged on the protective layer to the upper part of bodies of pixel and counter electrodes, respectively.

[**0033**] As a result, in the IP-FFS mode LCD of the present invention, the initial arrangement of rubbed liquid crystal molecules has a predetermined angle with the direction of electric field in the regions between the body of counter electrode and the branch end of pixel electrode and between the body of pixel electrode and branch end of counter electrode. Therefore, liquid crystal molecules are twisted by electric field in the regions, thereby realizing high screen quality without lowering of transmittance.

[**0034**] **FIG. 3** is a plan view showing IP-FFS mode LCD according to another embodiment of the present invention. The elements have the same structures with those in the above-mentioned embodiment. The following explanation is focused on the points different from the above embodiment.

[**0035**] The present embodiment is similar to the former one in that a counter electrode **38** is formed in a built-in type with a common bus line **34**, branches **38***a* are formed on a protective layer through ITO patterning, and the body **38***a* and the branches **38***b* maintain contact C1 by a contact hole passing through the protective layer and the gate insulating layer.

[**0036**] The pixel electrode **39** comprises a body **39***a* and branches **39***b*, **39***c*, being in contact with a thin film transistor **37**. However, the body and the branches **39***a*, **39***b*, **39***c* are formed on the protective layer in a built-in type through ITO patterning.

[**0037**] And, a storage capacitance electrode **35** is additionally formed on the lower part of body **39***a* of pixel electrode to form storage capacitance, being parallel with the data bus line **36**. The storage capacitance electrode **35** is formed at the same time with the gate bus line **32** and the common bus line **34**, overlapping with the body **39***a* of pixel electrode with the gate insulating layer and the protective layer interposed, thereby forming additional storage capacitance.

[**0038**] According to the present embodiment, the IP-FFS mode LCD has increased storage capacitance, compared with the former embodiments. Therefore, the transmittance is slightly decreased, however, it is possible to prevent lowering of screen quality by the storage capacitance.

[**0039**] That is, the IP-FFS mode LCD has a very small amount of storage capacitance, compared with that in FFS mode LCD. This is because the IP-FFS mode LCD can obtain storage capacitance only by overlap of common bus line and center branch of pixel electrode. On the other hand, the FFS mode LCD can obtain storage capacitance by overlap of counter electrode having plate structure and pixel electrode having slit structure. The storage capacitance is essential element to accomplish improvement of screen quality, thereby causing lowering of screen quality when the storage capacitance is decreased below a predetermined level.

[**0040**] In the IP-FFS mode LCD of the above embodiment, storage capacitance is formed between the common bus line and center branch of pixel electrode, and additionally, it is also formed between the storage capacitance electrode and the body of pixel electrode, thereby it is possible to obtain storage capacitance to a desired level. Therefore, the liquid crystal molecules are not twisted in the region between the body of pixel electrode and the branch end of counter electrode, thereby lowering the transmittance, compared with the former embodiments. However, it is possible to prevent lowering of screen quality due to storage capacitance.

[**0041**] As described above, the present invention can improve transmittance and thereby, accomplish high screen quality LCD since the counter electrode and the pixel electrode respectively comprise bodies and branches and each branch end is extended to the upper part of the other body. And, it has an advantage in obtaining storage capacitance by additionally forming storage capacitance electrode.

[**0042**] Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is

1. An IP-FFS mode LCD comprising:

a transparent insulating substrate;

a plurality of gate bus lines and data bus lines cross-arranged on the substrate, to define a unit pixel;

a plurality of common bus lines arranged on the center part of unit pixels, being parallel with the gate bus line;

a thin film transistor arranged at the intersection of the gate bus line and the data bus line;

a counter electrode arranged in each unit pixel, including a first body arranged on the edge of one side of unit pixel to be parallel with the data bus line and a plurality of first branches, the end of one side being in contact with the first body, wherein the first branches are made of ITO and arranged having a predetermined angle symmetric with respect to the common bus line; and

a pixel electrode arranged in each unit pixel to be in contact with the thin film transistor, including a second body arranged on the lower part of the other end of the first branch on the other edge of the unit pixel, being

parallel with the data bus line and a plurality of second branches, the other end being in contact with the second body and the one end being extended to the upper part of the first branch, wherein the second branches are made of ITO and arranged on the same layer with the first branches, forming parallel between the first branches.

2. The IP-FFS mode LCD according to claim 1, further comprising a gate insulating layer interposed between the gate bus line and the data bus line and a protective layer between the data bus line and first and second branches of the counter and pixel electrodes.

3. The IP-FFS mode LCD according to claim 1, wherein the first body of the counter electrode is formed in a built-in type with the common bus line.

4. The IP-FFS mode LCD according to claim 1, wherein the second body of the pixel electrode is arranged on the same layer with the data bus line.

5. The IP-FFS mode LCD according to claim 2, wherein the first branch of the counter electrode is in contact with the first body by a first contact hole passing through the protective layer and the gate insulating layer.

6. The IP-FFS mode LCD according to claim 2, wherein the second branch of the pixel electrode is in contact with the second body by a second contact hole passing through the protective layer.

7. The IP-FFS mode LCD according to claim 1, wherein the pixel electrode further comprises a center branch arranged on the upper part of the common bus line to form storage capacitance.

8. An IP-FFS mode LCD comprising:

a transparent insulating layer;

a plurality of gate bus lines and data bus lines cross-arranged on the substrate, to define a unit pixel;

a plurality of common bus lines arranged on the center part of unit pixels, being parallel with the gate bus line and having a storage capacitance electrode arranged in the unit pixel, adjacent to the data bus line and parallel therewith;

a thin film transistor arranged at the intersection of the gate bus line and the data bus line;

a counter electrode arranged in the unit pixel, including a first body arranged on the edge of one side of the unit pixel to be parallel with the data bus line and a plurality of first branches, the end of one side being in contact with the first body and the end of the other side being separated from the storage capacitance electrode, wherein the first branches are made of ITO, having a predetermined angle symmetric with respect to the common bus line; and

a pixel electrode arranged in each unit pixel to be in contact with the thin film transistor, including a second body arranged on the edge of the other side of unit pixel to be parallel with the data bus line and overlap with the storage capacitance electrode and a plurality of second branches extended from the second body to the upper part of the first body, wherein the second branches are made of ITO and arranged on the same layer with the first branches, forming parallel between the first branches.

9. The IP-FFS mode LCD according to claim 8, further comprising a gate insulating layer interposed between the gate bus line and the data bus line and a protective layer between the data bus line and the first and the second branches of counter and pixel electrodes.

10. The IP-FFS mode LCD according to claim 8, wherein the first body of counter electrode is formed in a built-in type with the common bus line.

11. The IP-FFS mode LCD according to claim 8, wherein the second body of pixel electrode is formed in a built-in type with the second branches through ITO patterning.

12. The IP-FFS mode LCD according to claim 9, wherein the first branch of counter electrode is in contact with the first body by a contact hole passing through the protective layer and the gate insulating layer.

13. The IP-FFS mode LCD according to claim 8, wherein the pixel electrode further comprises a center branch arranged on the upper part of the common bus line to form storage capacitance.

* * * * *

专利名称(译)	在平面边缘场切换模式LCD中实现高屏幕质量		
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摘要(译)

公开了一种IP-FFS模式LCD，其通过防止透射率降低来实现高屏幕质量。IP-FFS模式LCD包括：透明绝缘基板;多个栅极总线和数据总线交叉排列在基板上;多条公共总线设置成与栅极总线平行;薄膜晶体管，设置在栅极总线和数据总线的交叉点上;布置在每个单元像素中的对电极，包括布置在单元像素的一侧的边缘上的第一主体，以与数据总线和多个第一分支平行，一侧的一端与第一主体接触，其中第一分支具有相对于公共总线对称的预定角度;布置在每个单元像素中的像素电极，包括布置在单位像素的另一边缘上的第一分支的另一端的下部的第二主体，与数据总线和多个第二分支平行，另一端与第二主体接触，一端延伸到第一分支的上部，其中第二分支与第一分支布置在同一层上，在第一分支之间平行形成。