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(57) **ABSTRACT**

(51) **Int. Cl.⁷** **G09G 3/36**

Provided is a liquid crystal display device capable of independently adjusting gradation for each of RGB. A control circuit outputs a clock signal, an image signal for each of RGB, and an adding circuit control signal. A gradation voltage generation circuit outputs a gradation voltage. A color correction voltage for each of RGB is generated in a color correction voltage generation circuit based on an input signal for color correction. A signal electrode drive circuit receives the clock signal, a control signal, the image signal, the adding circuit control signal, the gradation voltage, and the color correction voltage. A gradation voltage corresponding to a gradation value of the image signal for each of RGB is selected from the gradation voltage. The color correction voltage for each of RGB is added to the gradation voltage, then a sub-pixel data signal is generated and sent to a liquid crystal panel.

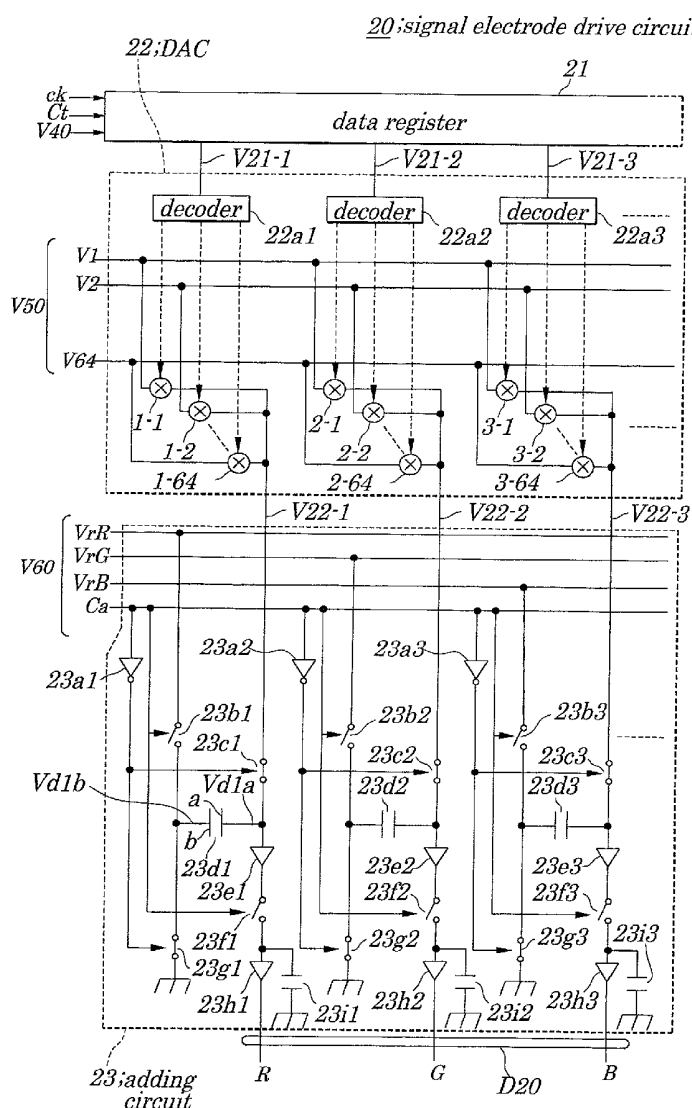


FIG. 1

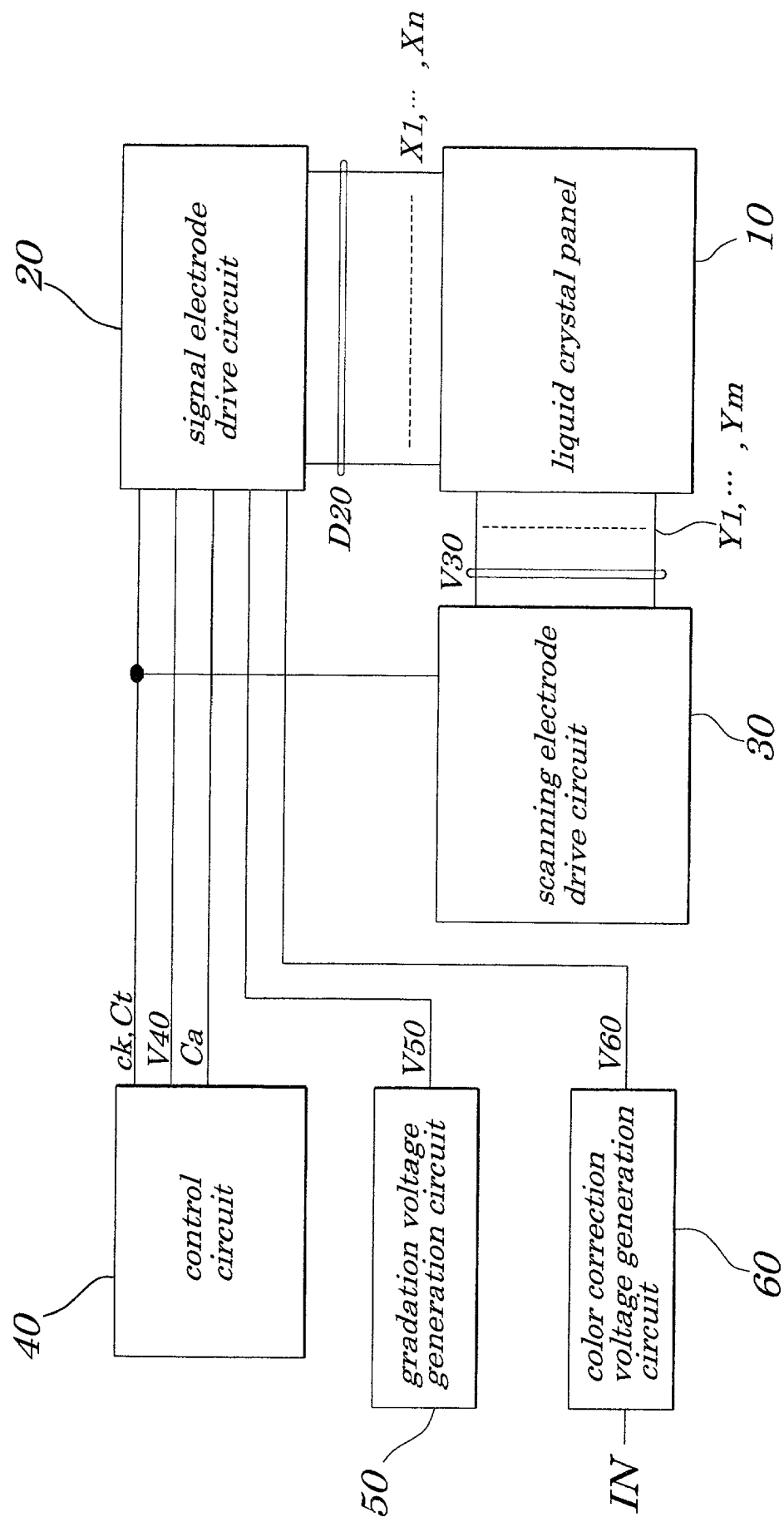


FIG. 2

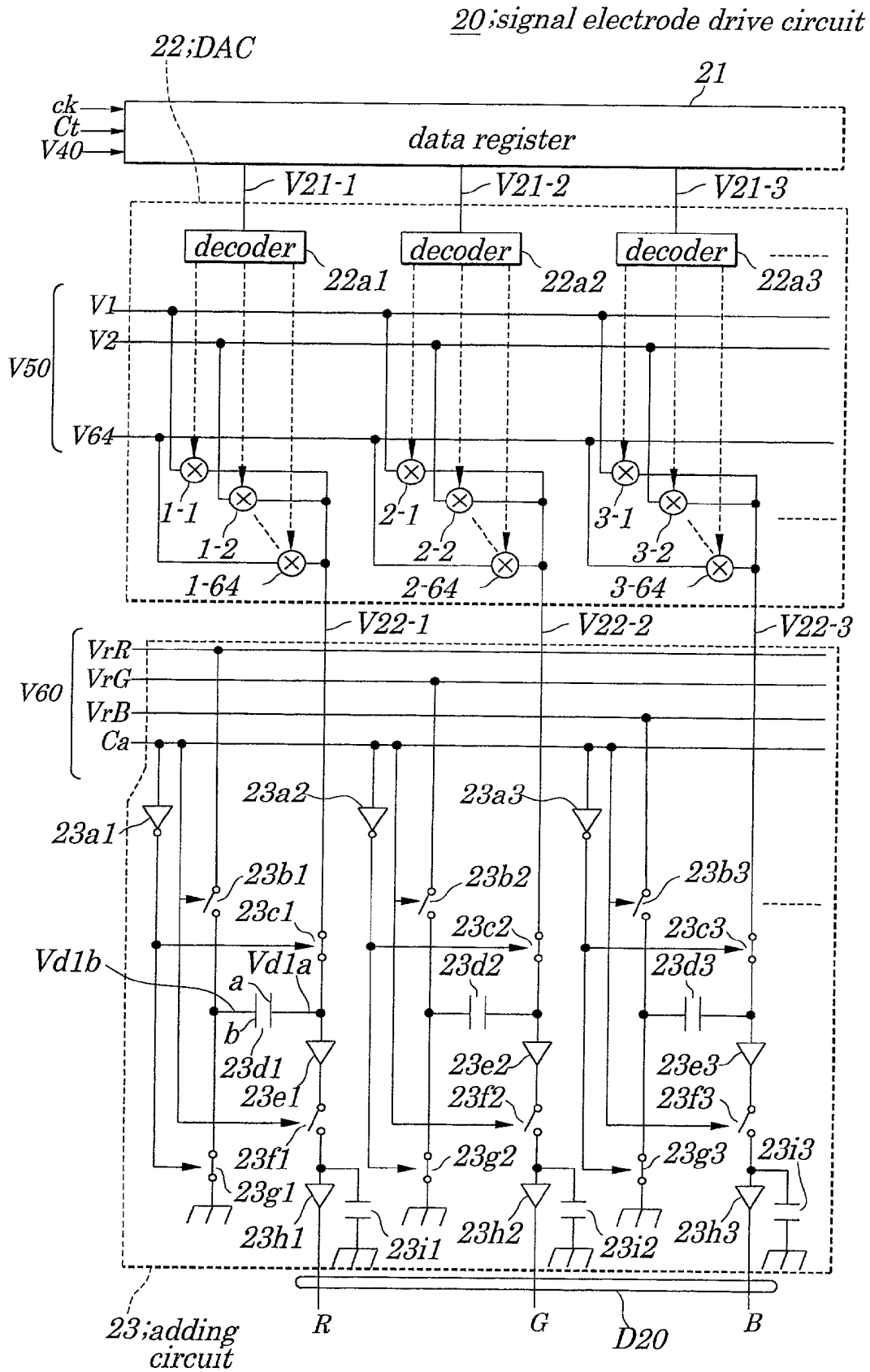


FIG. 3

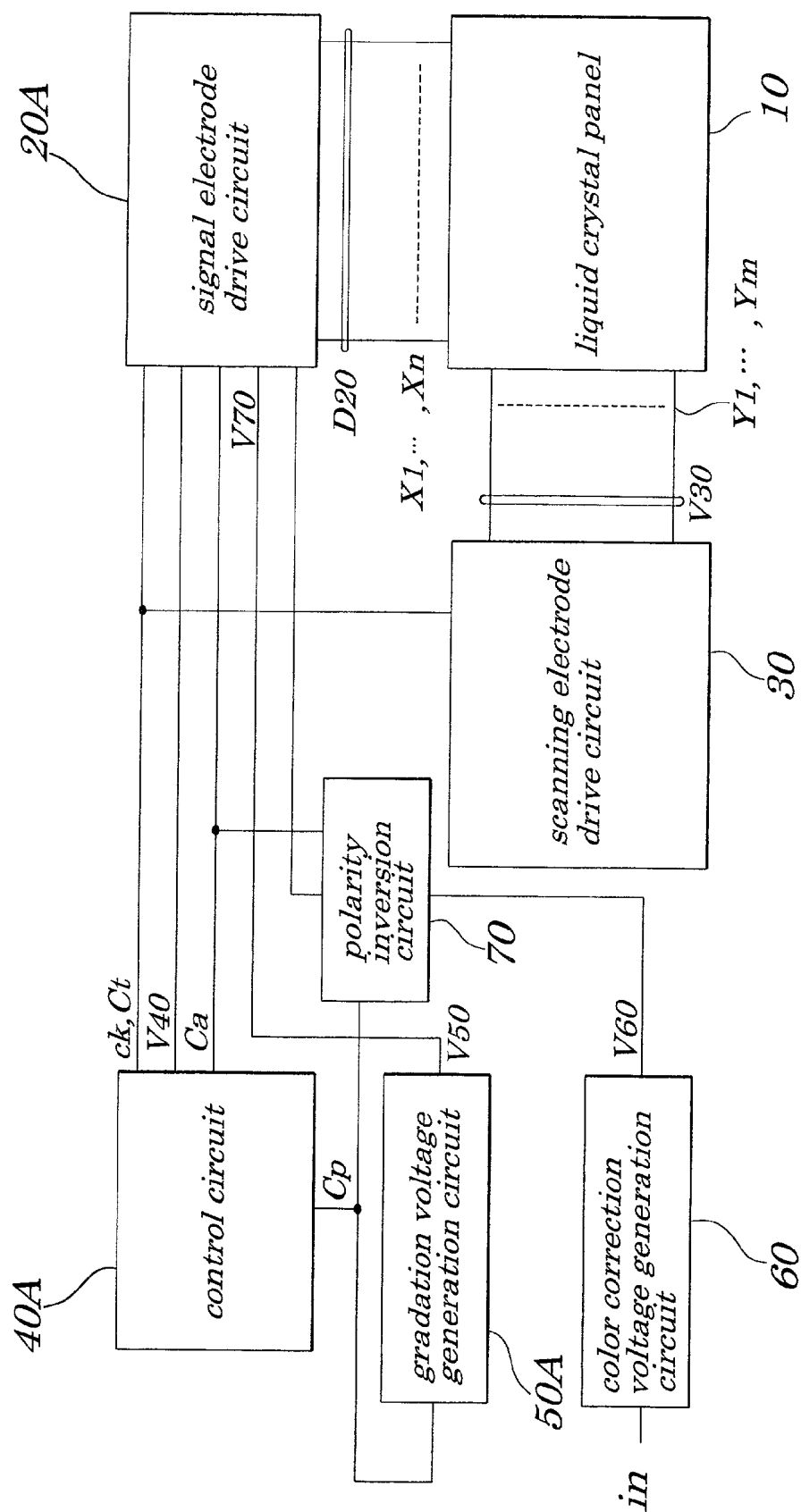


FIG. 4

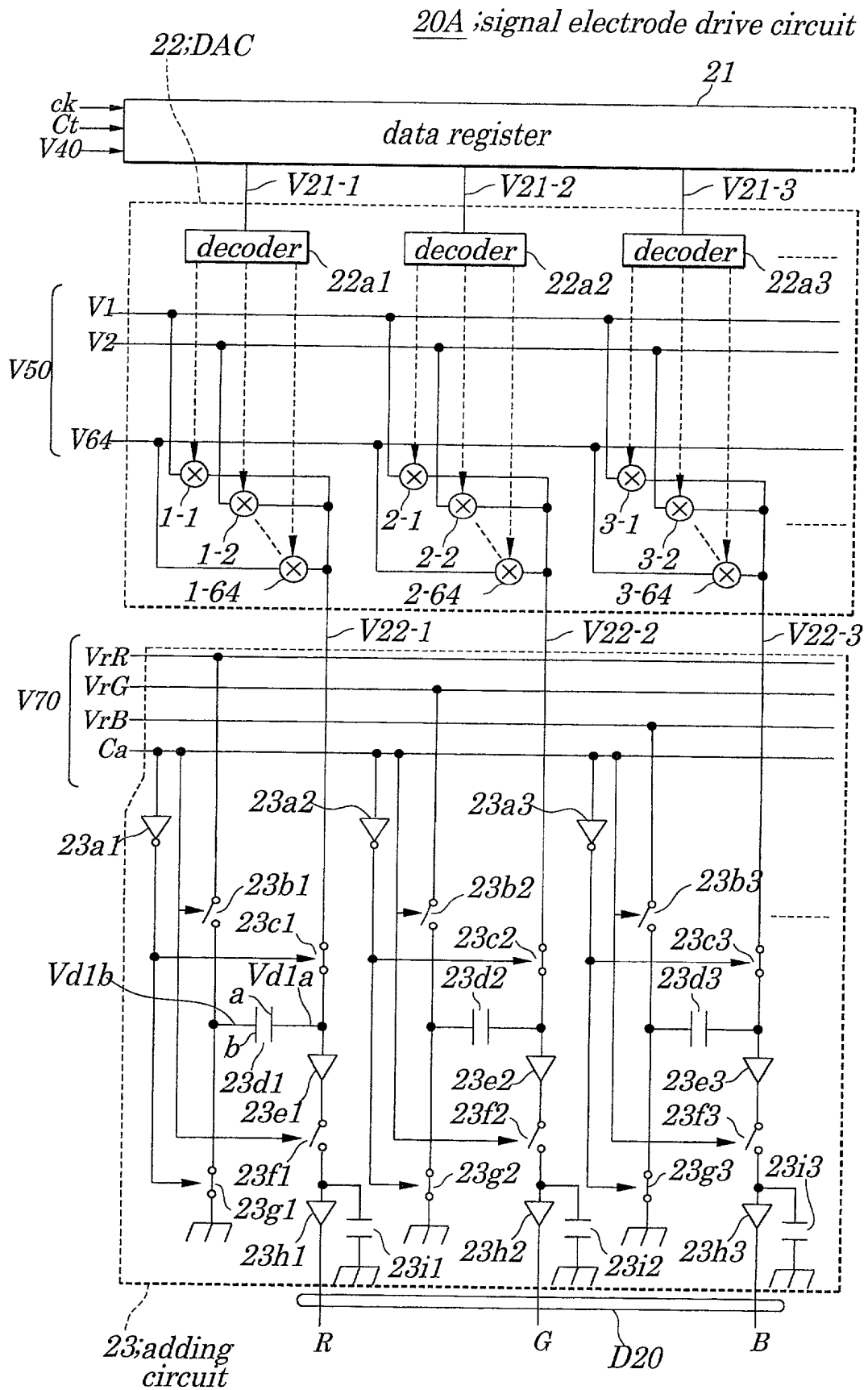


FIG.5

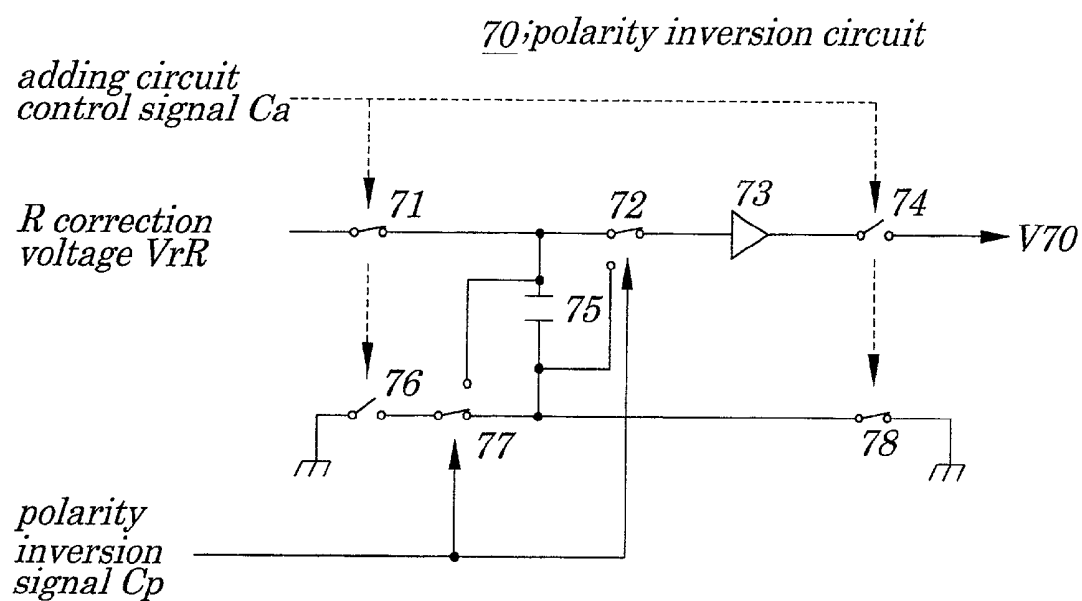


FIG.6

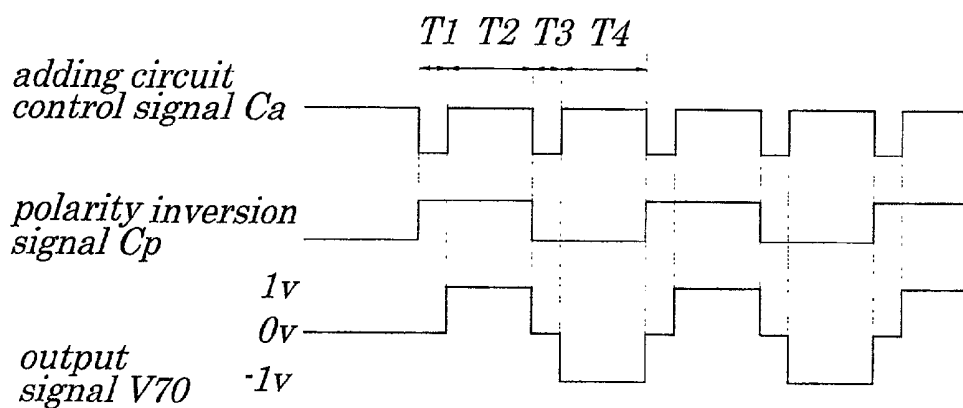


FIG. 7

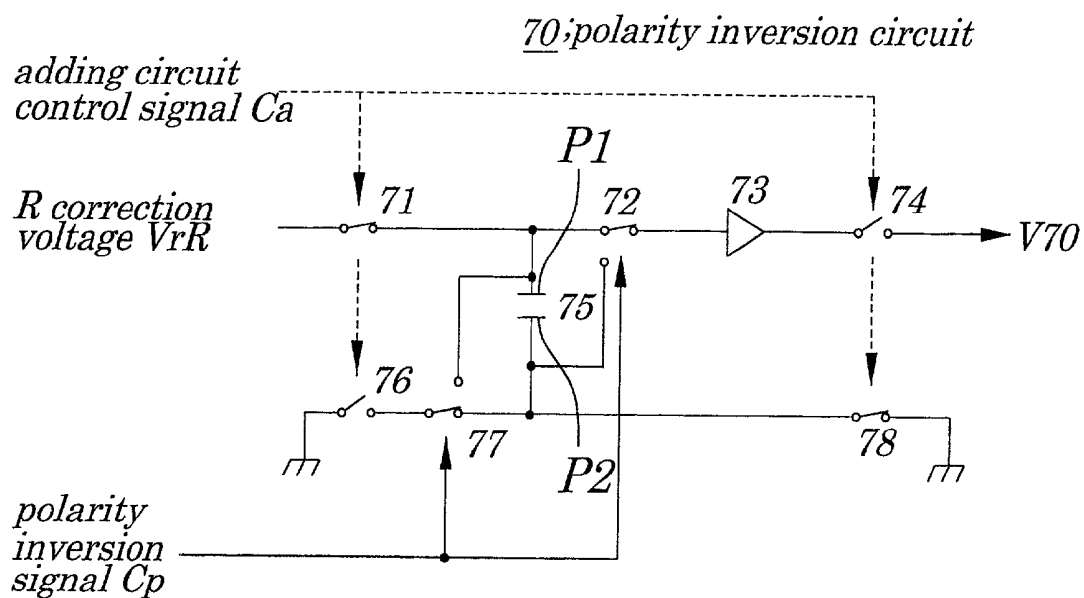


FIG. 8

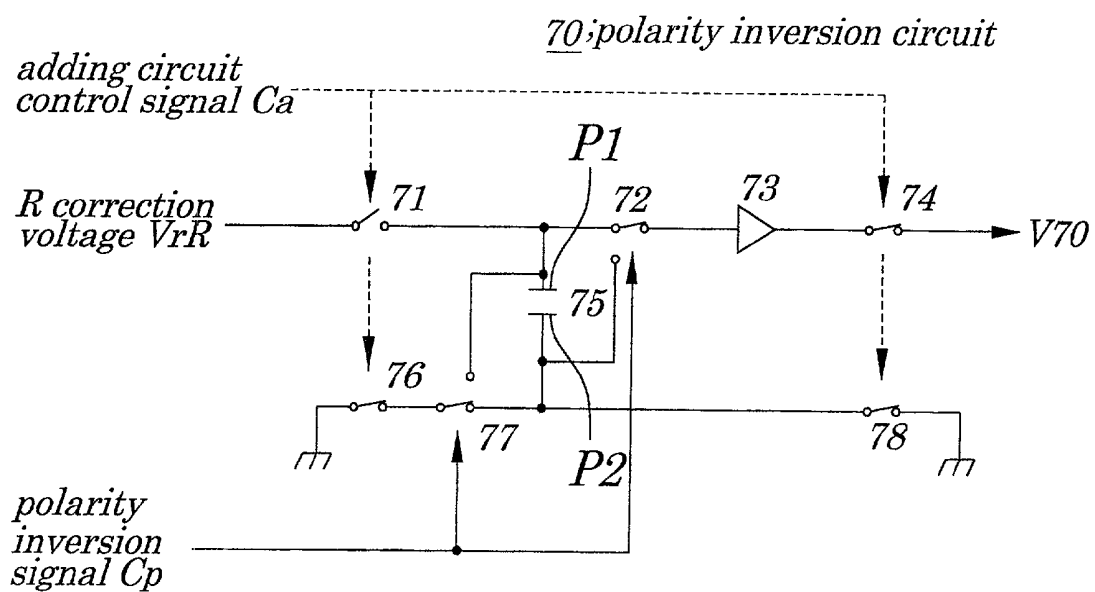


FIG. 9

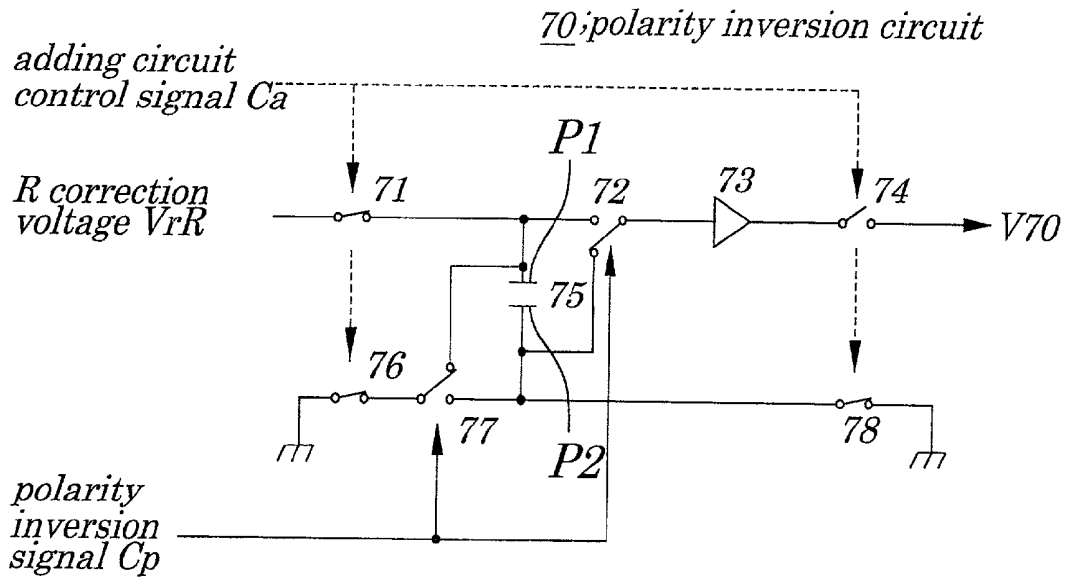


FIG. 10

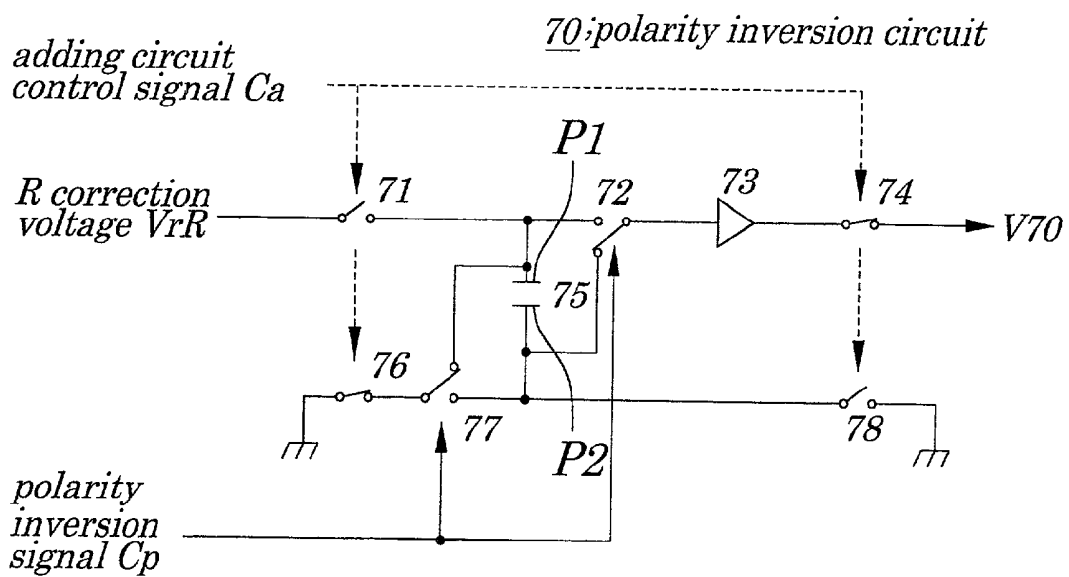


FIG. 11

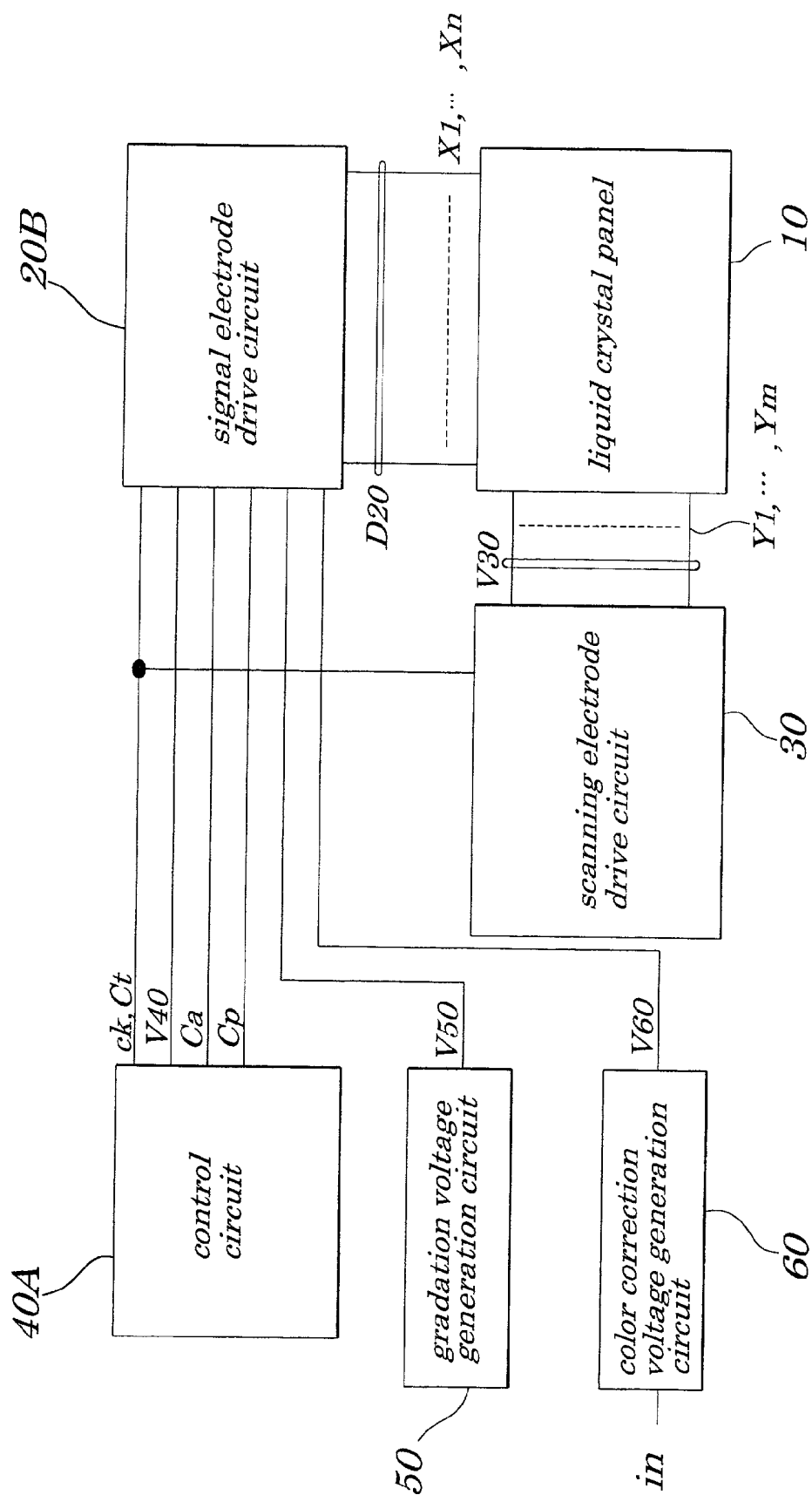


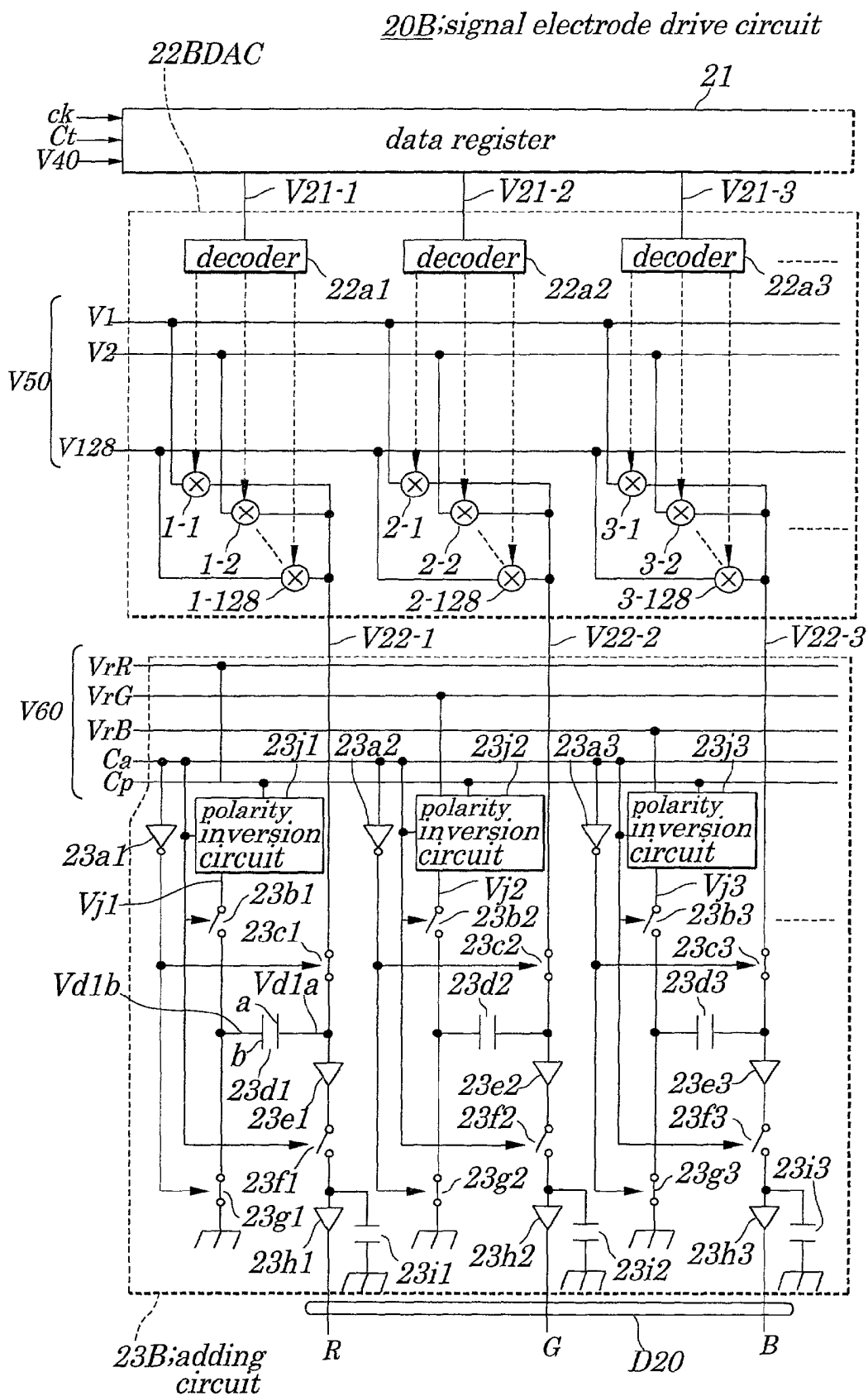
FIG. 12

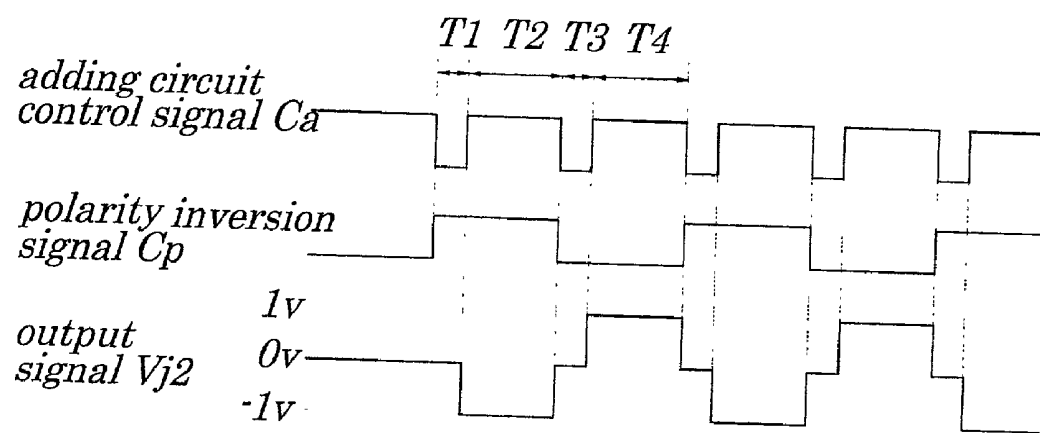
FIG. 13

FIG. 14

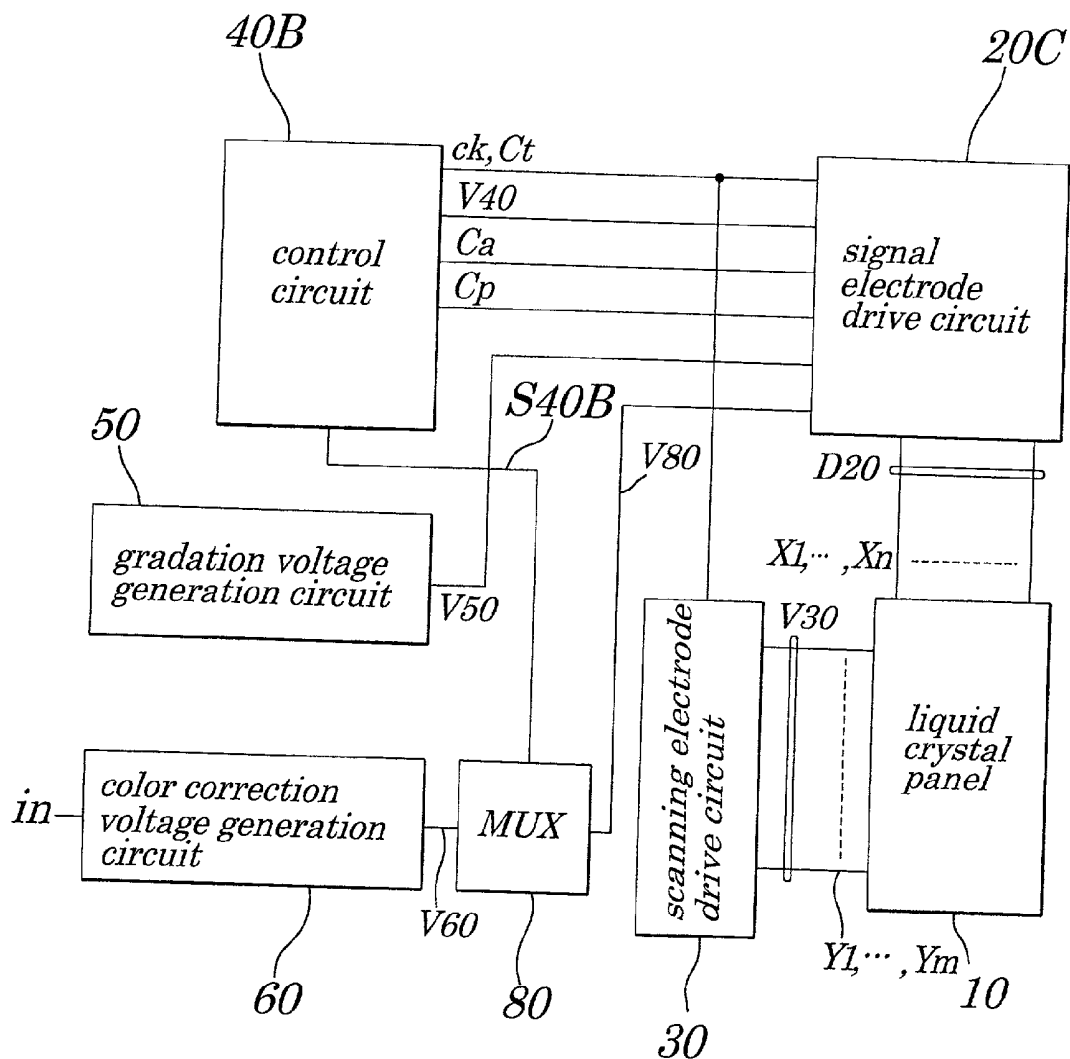


FIG. 15

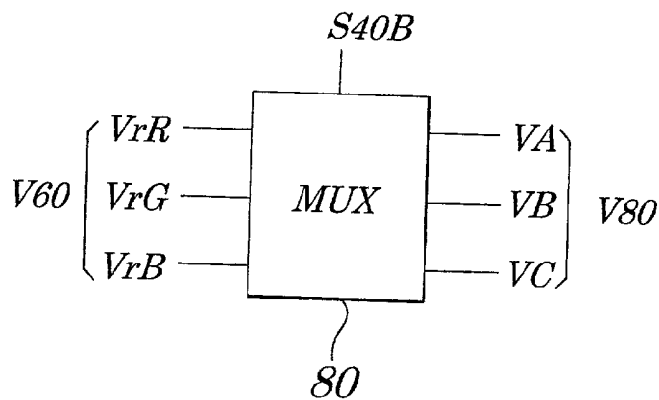


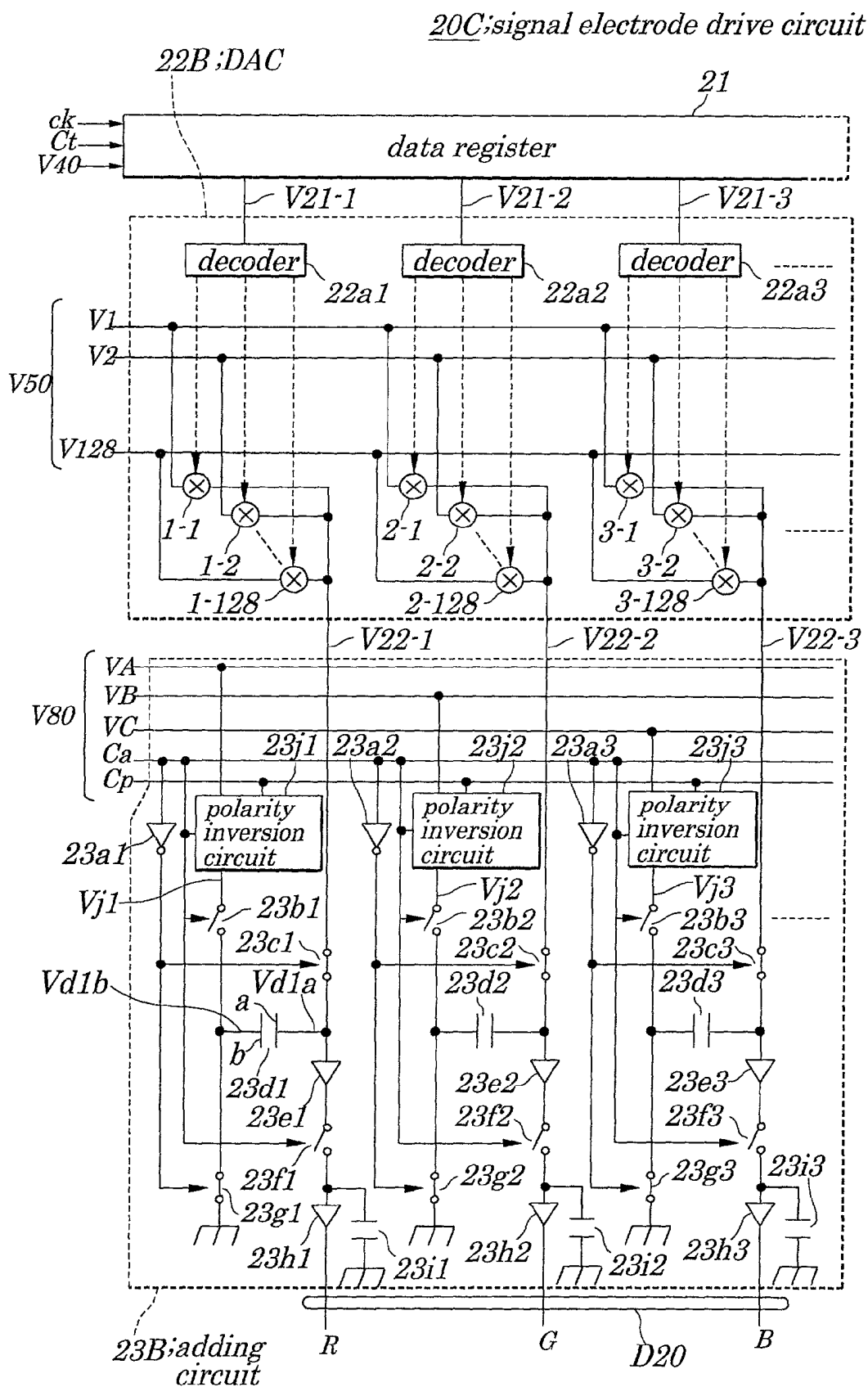
FIG. 16

FIG. 17

<i>control signal S40B</i>	<i>vertical-stripe type</i>			<i>mosaic type</i>			<i>horizontal- stripe type</i>		
<i>horizontal line</i>	Y_i	Y_{i+1}	Y_{i+2}	Y_i	Y_{i+1}	Y_{i+2}	Y_i	Y_{i+1}	Y_{i+2}
<i>VA</i>	<i>R</i>	<i>R</i>	<i>R</i>	<i>R</i>	<i>B</i>	<i>G</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>VB</i>	<i>G</i>	<i>G</i>	<i>G</i>	<i>G</i>	<i>R</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>VC</i>	<i>B</i>	<i>B</i>	<i>B</i>	<i>B</i>	<i>G</i>	<i>R</i>	<i>R</i>	<i>G</i>	<i>B</i>

FIG. 18(PRIOR ART)

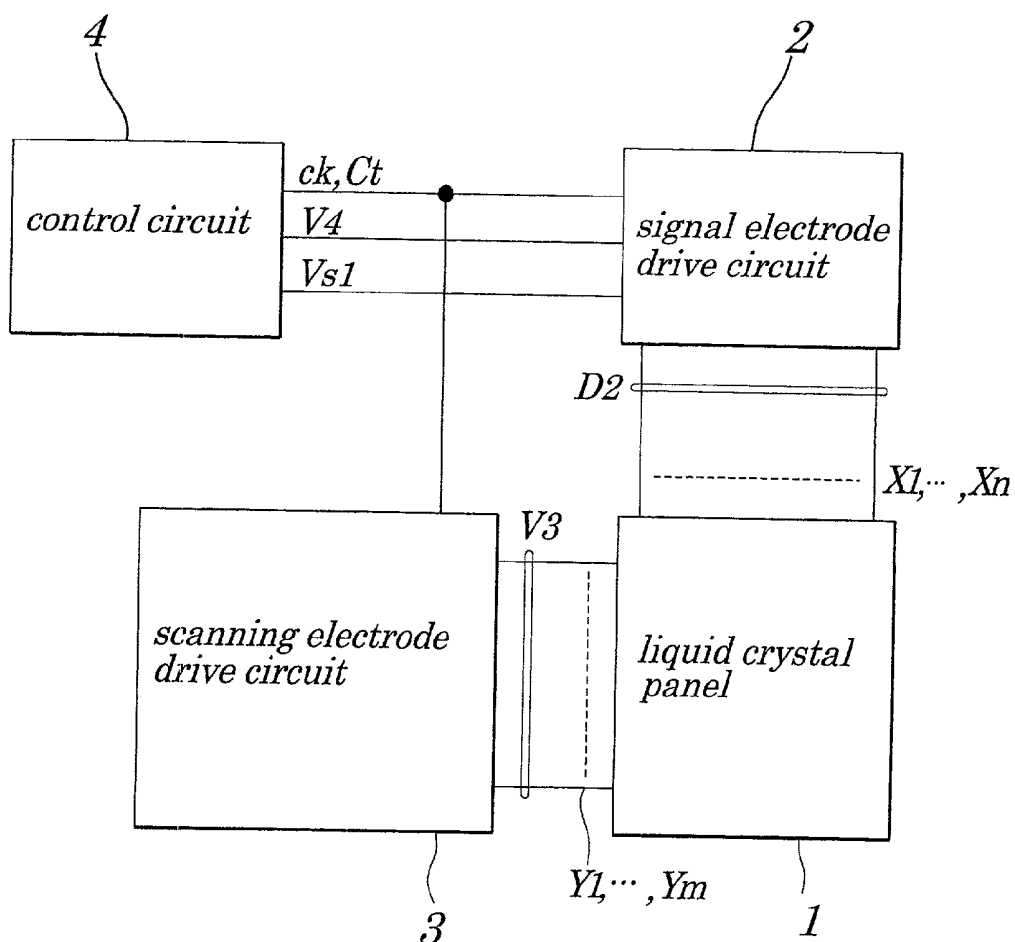


FIG. 19A(PRIOR ART)

<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>

vertical stripe

FIG. 19B(PRIOR ART)

<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>
<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>
<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>
<i>B</i>	<i>R</i>	<i>G</i>	<i>B</i>	<i>R</i>	<i>G</i>

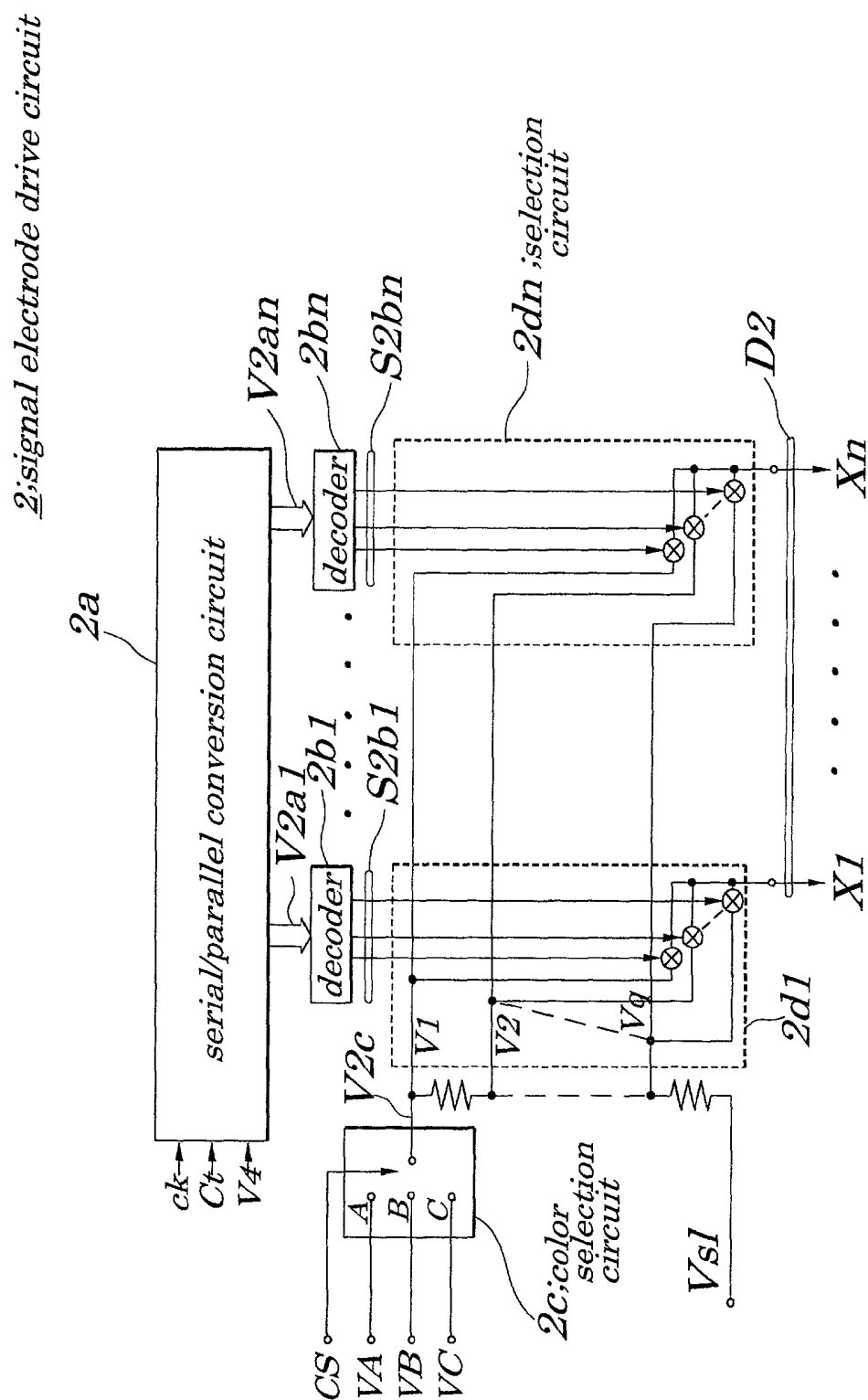
mosaic

FIG. 19C(PRIOR ART)

<i>R</i>	<i>B</i>	<i>G</i>	<i>R</i>	
	<i>G</i>	<i>R</i>	<i>B</i>	<i>G</i>
<i>R</i>	<i>B</i>	<i>G</i>	<i>R</i>	
	<i>G</i>	<i>R</i>	<i>B</i>	<i>G</i>
<i>R</i>	<i>B</i>	<i>G</i>	<i>R</i>	

triangle

FIG. 20(PRIOR ART)



LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display device for color displaying. For example, the present invention relates to the liquid crystal display device for the color displaying with a liquid crystal panel having color filters of a vertical-stripe type, a mosaic type or a like built therein, and capable of adjusting white balance of a display screen thereof.

[0003] The present application claims priority of Japanese Patent Application No.2000-160804 filed on May 30, 2000, which is hereby incorporated by reference.

[0004] 2. Description of the Related Art

[0005] As shown in **FIG. 18**, a conventional liquid crystal display device includes: a liquid crystal panel **1**, a signal electrode drive circuit **2**, a scanning electrode drive circuit **3**, and a control circuit **4**. The liquid crystal panel **1** includes color filters where a pixel is divided into sub-pixels of three primary colors of RGB (Red, Green, Blue). The liquid crystal panel **1** also includes: a plurality of data signal lines X_1, \dots, X_n for receiving a sub-pixel data signal **D2** corresponding to the sub-pixels of RGB, a plurality of scanning signal lines Y_1, \dots, Y_m for receiving a scanning signal **V3**, and a plurality of sub-pixel regions provided at points where each of the data signal lines X_1, \dots, X_n and each of the scanning signal lines Y_1, \dots, Y_m intersect. The sub-pixel data signal **D2** is supplied to sub-pixel regions selected from the plurality of sub-pixel regions by a scanning signal **V3**, and thus a color image corresponding to the sub-pixel data signal **D2** is displayed.

[0006] The signal electrode drive circuit **2** receives a clock signal ck , a control signal Ct , an image signal **V4** for each of RGB, and a central voltage $Vs1$, generates the sub-pixel data signal **D2** by selecting a gradation voltage corresponding to a gradation value of the image signal **V4** for each of RGB, and sends the sub-pixel data signal **D2** to each of the data signal lines X_1, \dots, X_n of the liquid crystal panel **1**. The scanning electrode drive circuit **3** sends the scanning signal **V3** to each of the scanning signal lines Y_1, \dots, Y_m of the liquid crystal panel **1** synchronously with the clock signal ck . The control circuit **4** outputs the clock signal ck , the control signal Ct , the image signal **V4**, and the central voltage $Vs1$.

[0007] **FIGS. 19(a), 19(b), and 19(c)** are exemplary views showing the above-mentioned color filters used in the liquid crystal panel **1**.

[0008] The color filter of a vertical-stripe type shown in **FIG. 19(a)** is suitable for displaying characters, drawings, and the like. The color filters of a mosaic type and a triangle type shown in **FIG. 19(b), and 19(c)** are ones where the three primary colors of RGB are arranged in a delta state such as stacked-up bricks, which are suitable for displaying moving images such as television (that is, picture data displaying). There is also a horizontal-stripe type color filter. In the horizontal-stripe type color filter, a horizontal line is constituted of pixels of one of the RGB colors, and a line in the vertical direction is constituted of pixels of the three primary colors of RGB.

[0009] Adjustment of white balance of a display screen is generally performed by limiting a range of a gradation value of an image signal for each of RGB to be used. For example, in the case where the gradation value of each of RGB is represented by 8-bit data, the gradation value could take values in a range of from 0 to 256. In adjusting the white balance, however, top and bottom of the gradation value of a particular color are cut. For example, regarding the gradation value for R, 0 to 4 and 251 to 255 are cut, and thus the gradation value of 5 to 25 is used. In addition, regarding the gradation value for G and the gradation value for B, 0 to 255 is used.

[0010] In adjusting the white balance, as a method of adjusting the gradation voltage for each of RGB without adjustment of the gradation value for each of RGB, there exists a method described in Japanese Patent Laid-open No. Hei4-60583 gazette (hereinafter, referred to as a literature), for example.

[0011] **FIG. 20** is a circuit diagram showing an electrical configuration of the signal electrode drive circuit **2** described in the foregoing literature.

[0012] The signal electrode drive circuit **2** includes: a serial/parallel conversion circuit **2a**, decoders $2b1, \dots, 2bn$, a color selection circuit **2c**, and selection circuits $2d1, \dots, 2dn$. The serial/parallel conversion circuit **2a** receives the clock signal ck , the control signal Ct and the image signal **V4**, and outputs gradation values $V2a1, \dots, V2an$ for each of RGB of the image signal **V4**. The decoders $2b1, \dots, 2bn$ decode the gradation values $V2a1, \dots, V2an$, and output selection signals $S2b1, \dots, S2bn$ corresponding to the gradation values $V2a1, \dots, V2an$. The color selection circuit **2c** selects voltages V_A, V_B , and V_C for adjusting the gradation voltage for each of RGB, which are supplied to selected terminals A to C, for every horizontal line period of an image of the liquid crystal panel **1** (**FIG. 18**) based on a color selection signal CS , and outputs a voltage $V2c$. The selection circuits $2d1, \dots, 2dn$ receive drive voltages $V1, \dots, Vq$ generated by a voltage dividing resistor connected between the voltage $V2c$ and the central voltage $Vs1$, select drive voltages corresponding to the selection signals $S2b1, \dots, S2bn$ from the drive voltages $V1, \dots, Vq$, and output a sub-pixel data signal **D2**.

[0013] In the liquid crystal display device, the control circuit **4** outputs the clock signal ck , the control signal Ct , the image signal **V4**, the color selection signal CS and the central voltage $Vs1$. Another control circuit (not shown) outputs the color selection signal CS . The clock signal ck , the control signal Ct , the image signal **V4** for each of RGB and the central voltage $Vs1$ are input to the signal electrode drive circuit **2**. Then, gradation voltages corresponding to the gradation value of the image signal **V4** for each of RGB are selected, and the sub-pixel data signal **D2** is generated, which is sent to each of data signal lines X_1, \dots, X_n of the liquid crystal panel **1**.

[0014] In this case, the clock signal ck , the control signal Ct , and the image signal **V4** are input to the serial/parallel conversion circuit **2a**, from which the gradation values $V2a1, \dots, V2an$ of the image signal **V4** for each of RGB are output. The gradation values $V2a1, \dots, V2an$ are input to the decoders $2b1, \dots, 2bn$ and decoded, from which selection signals $S2b1, \dots, S2bn$ are output. The voltages V_A, V_B , and V_C supplied to selected terminals A, B, and C

are selected for every horizontal line period of the image of the liquid crystal panel 1 in the color selection circuit 2c based on the color selection signal CS, and the voltage V2c is output from the color selection circuit 2c. The drive voltages V1, . . . , Vq are input to the selection circuits 2d1, . . . , 2dn, and the drive voltage selected based on the selection signals S2b1, . . . , S2bn is output as the sub-pixel data signal D2 from the selection circuits 2d1, . . . , 2dn.

[0015] In addition, the clock signal ck is input to the scanning electrode drive circuit 3, the scanning signal V3 is generated synchronously with the clock signal ck, and the scanning signal V3 is sent to each of the scanning signal lines Y1, . . . , Ym of the liquid crystal panel 1. In the liquid crystal panel 1, the sub-pixel data signal D2 is supplied to the sub-pixel region selected by the scanning signal V3, and color image corresponding to the sub-pixel data signal D2 is displayed. Herein, voltages VA, VB, and VC are adjusted and input in accordance with the color of the color image on the liquid crystal panel 1, and thus the white balance of the color image is adjusted.

[0016] However, in the foregoing conventional general adjustment of the white balance, the use of the gradation value is limited in a particular color. Accordingly, there is a drawback in that combinations of the gradation of RGB, that is, kinds of display colors, are reduced. Moreover, in the method according to the foregoing literature, there is a problem in that the color filter of the liquid crystal panel 1 is limited to the horizontal-stripe type, and it can not deal with the color filters of the vertical stripe type, the mosaic type and the triangle type shown in FIG. 18.

SUMMARY OF THE INVENTION

[0017] In view of the above, it is an object of the present invention to provide a liquid crystal display device, in which a color correction voltage for each of RGB is generated, a liquid crystal drive voltage (that is, sub-pixel data signal) is independently generated for each of RGB, and a color image is displayed on a liquid crystal panel, and which can deal with various kinds of color filters.

[0018] To solve the above-described problems, according to a first aspect of the present invention, there is provided a liquid crystal display device including a liquid crystal panel for displaying a color image, wherein a color correction voltage generation circuit is provided for generating a color correction voltage for each of RGB based on a given input signal for color correction, and the color correction voltage of each of RGB is added to a gradation voltage of an image signal for each of RGB respectively, then the added voltages are supplied to the liquid crystal panel.

[0019] According to a second aspect of the present invention, there is provided a liquid crystal display device, including:

[0020] a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of RGB, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of the data signal lines and each of the scanning signal lines intersect, and the liquid crystal panel displaying a color image corresponding to the sub-pixel data signal by supplying the sub-pixel data signal

to a sub-pixel region selected by the scanning signal among the plurality of sub-pixel regions;

[0021] a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to the sub-pixel data signal;

[0022] a color correction voltage generation circuit for generating a color correction voltage for each of RGB based on a given input signal for color correction;

[0023] a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for each of RGB from each gradation voltage, adding the color correction voltage for each of RGB respectively to the gradation voltage to generate the sub-pixel data signal, and sending the sub-pixel data signal to each data signal line of the liquid crystal panel;

[0024] a scanning signal circuit for sending the scanning signal to each scanning signal line of the liquid crystal panel synchronously with a clock signal; and

[0025] a control circuit for outputting the clock signal and the image signal for each of RGB.

[0026] According to a third aspect of the present invention, there is provided a liquid crystal display device, including:

[0027] a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of RGB, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of the data signal lines and each of the scanning signal lines intersect, and the liquid crystal panel displaying a color image corresponding to the sub-pixel data signal by supplying the sub-pixel data signal to a sub-pixel region selected by the scanning signal among the plurality of sub-pixel regions;

[0028] a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to the sub-pixel data signal, inverting a polarity of the gradation voltage in one frame period based on a polarity inversion signal, and outputting the gradation voltage with the inverted polarity;

[0029] a color correction voltage generation circuit for generating a color correction voltage for each of RGB based on a given input signal for color correction, inverting a polarity of the color correction voltage in one frame period based on the polarity inversion signal, and outputting the color correction voltage with the inverted polarity;

[0030] a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for each of RGB from each gradation voltage, adding the color correction voltage for each of RGB respectively to the gradation voltage to generate the sub-pixel data signal, and sending the sub-pixel data signal to each data signal line of the liquid crystal panel;

[0031] a scanning signal circuit for sending the scanning signal to each scanning signal line of the liquid crystal panel synchronously with a clock signal; and

[0032] a control circuit for outputting the clock signal and the image signal for each of RGB.

[0033] According to a fourth aspect of the present invention, there is provided a liquid crystal display device, including:

[0034] a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of RGB, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of the data signal lines and each of the scanning signal lines intersect, and the liquid crystal panel displaying a color image corresponding to the sub-pixel data signal by supplying the sub-pixel data signal to a sub-pixel region selected by the scanning signal among the plurality of sub-pixel regions;

[0035] a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to the sub-pixel data signal, inverting a polarity of the gradation voltage in a specified number of horizontal line periods based on a polarity inversion signal, and outputting the gradation voltage with the inverted polarity;

[0036] a color correction voltage generation circuit for generating a color correction voltage for each of RGB based on a given input signal for color correction;

[0037] a polarity inversion circuit for inverting a polarity of the color correction voltage for each of RGB in a specified number of horizontal line periods based on the polarity inversion signal, and outputting the color correction voltage with the inverted polarity;

[0038] a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for each of RGB from each gradation voltage, adding the color correction voltage for each of RGB respectively to the gradation voltage to generate the sub-pixel data signal, and sending the sub-pixel data signal to each data signal line of the liquid crystal panel;

[0039] a scanning signal circuit for sending the scanning signal to each scanning signal line of the liquid crystal panel synchronously with a clock signal; and

[0040] a control circuit for outputting the clock signal, the image signal for each of RGB, and the polarity inversion signal.

[0041] According to a fifth aspect of the present invention, there is provided a liquid crystal display device, including:

[0042] a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of RGB, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of the data signal lines and each of the scanning signal lines intersect, and the liquid crystal panel displaying a color image corresponding to the sub-pixel data signal by supplying the sub-pixel data signal to a sub-pixel region selected by the scanning signal among the plurality of sub-pixel regions;

[0043] a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to the sub-pixel data signal;

[0044] a color correction voltage generation circuit for generating a color correction voltage for each of RGB based on a given input signal for color correction;

[0045] a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for each of RGB from each gradation voltage, inverting the color correction voltage for each of RGB at each sub-pixel based on a polarity inversion signal and adding the color correction voltage with the inverted polarity to the gradation voltage to generate the sub-pixel data signal, and sending the sub-pixel data signal to each data signal line of the liquid crystal panel;

[0046] a scanning signal circuit for sending the scanning signal to each scanning signal line of the liquid crystal panel synchronously with a clock signal; and

[0047] a control circuit for outputting the clock signal, the image signal for each of RGB, and the polarity inversion signal.

[0048] According to a sixth aspect of the present invention, there is provided a liquid crystal display device, including:

[0049] a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of RGB, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of the data signal lines and each of the scanning signal lines intersect, and the liquid crystal panel displaying a color image corresponding to the sub-pixel data signal by supplying the sub-pixel data signal to a sub-pixel region selected by the scanning signal among the plurality of sub-pixel regions;

[0050] a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to the sub-pixel data signal;

[0051] a color correction voltage generation circuit for generating a color correction voltage for each of RGB based on a given input signal for color correction;

[0052] a multiplexer for selecting and outputting the color correction voltage for each of RGB in accordance with an arrangement of RGB color filters in a horizontal direction of the sub-pixels on the liquid crystal panel, based on a control signal;

[0053] a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for each of RGB from each gradation voltage, adding the color correction voltage for each of RGB output from the multiplexer respectively to the gradation voltage to generate the sub-pixel data signal, and sending the sub-pixel data signal to each data signal line of the liquid crystal panel;

[0054] a scanning signal circuit for sending the scanning signal to each scanning signal line of the liquid crystal panel synchronously with a clock signal; and

[0055] a control circuit for outputting the clock signal, the image signal for each of RGB, and the control signal.

[0056] With the above configurations, the color correction voltage for each of RGB is added to the gradation voltage for each of RGB. Accordingly, the sub-pixel data signal can be controlled and adjusted independently for each of RGB. Therefore, the white balance can be adjusted without reducing the number of the gradation values. Furthermore, the control circuit for outputting the control signal correspond-

ing to the arrangement of RGB of the sub-pixel and the MUX for selecting and outputting the color correction voltage for each of RGB in accordance with the arrangement of RGB of the sub-pixel of the liquid crystal panel are provided, based on the control signal. Accordingly, the present invention can cope with various color filters.

BRIEF DESCRIPTION OF THE DRAWINGS

[0057] Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

[0058] **FIG. 1** is a block diagram showing an electrical configuration of a liquid crystal display device according to a first embodiment of the present invention;

[0059] **FIG. 2** is a circuit diagram showing an electrical configuration of a signal electrode drive circuit **20** shown in **FIG. 1**;

[0060] **FIG. 3** is a block diagram showing an electrical configuration of a liquid crystal display device according to a second embodiment of the present invention;

[0061] **FIG. 4** is a circuit diagram showing an electrical configuration of a signal electrode drive circuit **20A** in **FIG. 3**;

[0062] **FIG. 5** is a circuit diagram showing an electrical configuration of a circuit for inverting polarity of a color correction voltage **V60** of an R component in a polarity inversion circuit **70** in **FIG. 3**;

[0063] **FIG. 6** is a timing chart showing an operation of the polarity inversion circuit **70**;

[0064] **FIG. 7** is a circuit diagram showing a state of the polarity inversion circuit **70** based on **FIG. 6**;

[0065] **FIG. 8** is another circuit diagram showing a state of the polarity inversion circuit **70** based on **FIG. 6**;

[0066] **FIG. 9** is another circuit diagram showing a state of the polarity inversion circuit **70** based on **FIG. 6**;

[0067] **FIG. 10** is still another circuit diagram showing a state of the polarity inversion circuit **70** based on **FIG. 6**;

[0068] **FIG. 11** is a block diagram showing an electrical configuration of a liquid crystal display device according to a third embodiment of the present invention;

[0069] **FIG. 12** is a circuit diagram showing an electrical configuration of a signal electrode drive circuit **20B** in **FIG. 11**;

[0070] **FIG. 13** is a timing chart showing an operation of a polarity inversion circuit **23j (2k)** in **FIG. 12**;

[0071] **FIG. 14** is a block diagram showing an electrical configuration of a liquid crystal display device according to a fourth embodiment of the present invention;

[0072] **FIG. 15** is a configuration diagram of a MUX **80** in **FIG. 14**;

[0073] **FIG. 16** is a circuit diagram showing an electrical configuration of a signal electrode drive circuit **20C** in **FIG. 14**;

[0074] **FIG. 17** is a graph explaining an operation of the MUX **80**;

[0075] **FIG. 18** is a block diagram showing an electrical configuration of a conventional liquid crystal device;

[0076] **FIGS. 19(a), 19(b), and 19(c)** are exemplary diagrams showing-examples of color filters; and

[0077] **FIG. 20** is a circuit diagram showing an electrical configuration of a signal electrode drive circuit **2** described in a literature.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0078] In driving methods of a liquid crystal display device, there are basic driving methods such as a frame inversion drive, a line inversion drive, and a dot inversion drive. Voltages higher (positive polarity) and lower (negative polarity) than a common voltage (0V) are supplied to the liquid crystal panel as drive voltages, and the liquid crystal panel is driven by an alternating voltage. The drive voltage is generated by allowing a few kinds of gradation voltages generated in the gradation voltage generation circuit to be divided into fragments by a resistor in the signal electrode drive circuit. For example, ten kinds of gradation voltages are generated in the gradation voltage generation circuit, and the gradation voltages are divided by the resistor in the signal electrode drive circuit to generate 128 kinds of gradation voltages. This time, in the case of the dot inversion drive, since the gradation voltages are divided into 64 kinds of gradation voltages above the common voltage and 64 kinds of gradation voltages below the common voltage, the signal electrode drive circuit generates the drive voltage with 64 gradations. In the frame inversion drive and the line inversion drive, either the gradation voltage of positive polarity or the gradation voltage of negative polarity is input to the signal electrode drive circuit. In the dot inversion drive, the gradation voltages of the both polarities are input to the signal electrode drive circuit.

[0079] Best modes for carrying out the present invention will be described in further detail using various embodiments with reference to the accompanying drawings.

First Embodiment

[0080] **FIG. 1** is a block diagram showing an electrical configuration of a liquid crystal display device according to a first embodiment of the present invention.

[0081] The liquid crystal display device of this embodiment, as shown in **FIG. 1**, includes: a liquid crystal panel **10**; a display signal circuit (for example, a signal electrode drive circuit **20**); a scanning signal circuit (for example, a scanning electrode drive circuit **30**); a control circuit **40**; a gradation voltage generation circuit **50**; and a color correction voltage generation circuit **60**. The liquid crystal panel **10** has color filters where pixels are divided into sub-pixels of three primary colors of RGB. The liquid crystal panel **10** also includes: a plurality of data signal lines **X1, . . . , Xn** for receiving a sub-pixel data signal **D20** corresponding to the sub-pixels of RGB; a plurality of scanning signal lines **Y1, . . . , Ym** for receiving a scanning signal **V30**; and a plurality of sub-pixel regions provided at points where each of the data signal lines **X1, . . . , Xn** and each of the scanning signal lines **Y1, . . . , Ym** intersect. The sub-pixel data signal

D20 is supplied to sub-pixel regions selected from the plurality of sub-pixel regions by the scanning signal V30, and thus a color image corresponding to the sub-pixel data signal D20 is displayed.

[0082] The signal electrode drive circuit 20 receives a clock signal ck, a control signal Ct, an image signal V40 for each of RGB, an adding circuit control signal Ca, a plurality of gradation voltages V50, and a color correction voltage V60, selects a gradation voltage corresponding to a gradation value of the image signal V40 for each of RGB from each gradation voltage V50, adds the color correction voltage V60 for each of RGB to the gradation voltage to generate the sub-pixel data signal D20, and sends the sub-pixel data signal D20 to each of the data signal lines X1, . . . , Xn of the liquid crystal panel 10. The scanning electrode drive circuit 30 sends the scanning signal V30 to each of the scanning signal lines Y1, . . . , Ym of the liquid crystal panel 10 synchronously with the clock signal ck.

[0083] The control circuit 40 outputs the clock signal ck, the image signal V40 for each of RGB, and the adding circuit control signal Ca. The gradation voltage generation circuit 50 generates a plurality of the gradation voltages V50 (for example, V1, . . . , VQ) for giving gradation to the sub-pixel data signal D20. The color correction voltage generation circuit 60 generates the color correction voltage V60 for each of RGB based on a given input signal "IN" for color correction.

[0084] FIG. 2 is a circuit diagram showing an electrical configuration of the signal electrode drive circuit 20 in FIG. 1.

[0085] The signal electrode drive circuit 20 includes: a data register 21; a digital/analog converter (hereinafter, referred to as DAC 22); and an adding circuit 23. The data register 21 receives the clock signal ck, the control signal Ct, and the image signal V40, and outputs gradation values V21-1, V21-2, . . . , V21-n of the image signal V40 for each of RGB. The DAC 22 includes: decoders 22a1, 22a2, . . . , 22an; and selection switches 1-1, 1-2, . . . , 1-64, 2-1, 2-2, . . . , 2-64, . . . , n-1, n-2, . . . , n-64, divides the gradation voltages V50 (V1, . . . , VQ) by a voltage dividing resistor circuit (not shown) to generate the gradation voltages V1, . . . , V64, selects the gradation voltages V22-1, V22-2, . . . , V22-n corresponding to the gradation values V21-1, V21-2, . . . , V21-n of the image signal V40 for each of RGB from the gradation voltages V1, . . . , V64, and outputs the gradation voltages.

[0086] The adding circuit 23 includes: inverters 23a1, 23a2, . . . , 23an; switches 23b1, 23b2, . . . , 23bn; switches 23c1, 23c2, . . . , 23cn; capacitors 23d1, 23d2, . . . , 23dn; buffers 23e1, 23e2, . . . , 23en; switches 23f1, 23f2, . . . , 23fn; switches 23g1, 23g2, . . . , 23gn; buffers 23h1, 23h2, . . . , 23hn; and capacitors 23i1, 23i2, . . . , 23in. The adding circuit 23 adds the color correction voltage V60 (for example, VrR, VrG, VrB) to the gradation voltages V22-1, V22-2, . . . , V22-n based on the adding circuit control signal Ca, and outputs the sub-pixel data signal D20.

[0087] Next, an operation of the liquid crystal display device of this embodiment will be described.

[0088] The control circuit 40 outputs the clock signal ck, the image signal V40 for each of RGB and the adding circuit control signal Ca. The gradation voltage generation circuit

50 outputs a plurality of the gradation voltages V50 (V1, . . . , VQ). The color correction voltage generation circuit 60 generates the color correction voltage V60 for each of RGB based on, for example, the input signal "IN" for color correction given by a user or a like.

[0089] The signal electrode drive circuit 20 receives the clock signal ck, the control signal Ct, the image signal V40, the adding circuit control signal Ca, the gradation voltage V50, and the color correction voltage V60, selects the gradation voltage V50 corresponding to the gradation value of the image signal V40 for each of RGB from the gradation voltage V50, adds the color correction voltage V60 for each of RGB to the gradation voltage V50, and generates the sub-pixel data signal D20. The sub-pixel data signal D20 is sent to each of the data signal lines X1, . . . , Xn of the liquid crystal panel 10.

[0090] In this case, data register 21 receives the clock signal ck, the control signal Ct, and the image signal V40, and outputs the gradation values V21-1, V21-2, . . . , V21-n of the image signal V40 for each of RGB. The DAC 22 receives the gradation values V21-1, V21-2, . . . , V21-n, selects the gradation voltages V22-1, V22-2, . . . , V22-n corresponding to the gradation values V21-1, V21-2, . . . , V21-n from the gradation voltages V1, . . . , V64, and outputs the gradation voltages. The adding circuit 23 receives the gradation voltages V22-1, V22-2, . . . , V22-n, adds the color correction voltage V60 (VrR, VrG, VrB) based on the adding circuit control signal Ca, and outputs the sub-pixel data signal D20.

[0091] In the adding circuit 23, in accordance with the adding circuit control signal Ca, the switch 23b1 and the switch 23f1 become in an OFF state when the switch 23c1 and the switch 23g1 are in an ON state, and the switch 23b1 and the switch 23f1 become in an ON state when the switch 23c1 and the switch 23g1 are in an OFF state. The adding circuit control signal Ca changes its theory level from a low level (hereinafter, referred to as L) to a high level (hereinafter, referred to as H) in one horizontal period. When the switch 23c1 and the switch 23g1 are in an ON state and the switch 23b1 and the switch 23f1 are in an OFF state, a voltage Vd1a of an electrode "a" of the capacitor 23d1 connected to an input side of the buffer 23e1 becomes an equal value as the gradation voltage V22-1. Next, when the switch 23c1 and the switch 23g1 are in an OFF state and the switch 23b1 and the switch 23f1 are in an ON state, a voltage Vd1b of an electrode "b" of the capacitor 23d1 becomes the color correction voltage VrR. Accordingly, the voltage Vd1a of the electrode "a" becomes as follows:

[0092] $Vd1a = \text{gradation voltage (V22-1)} + \text{color correction voltage (VrR)}$. The voltage Vd1a is output as the sub-pixel data signal D20 of R component via the buffer 23h1. The sub-pixel data signals D20 of G component and B component are output in the same manner.

[0093] The scanning electrode drive circuit 30 receives the clock signal ck, generates the scanning signal V30 synchronously with the clock signal ck, and sends the scanning signal V30 to each of the scanning signal lines Y1, . . . , Ym of the liquid crystal panel 10. In the liquid crystal panel 10, the sub-pixel data signal D20 is supplied to a sub-pixel region selected by the scanning signal V30, and a color image corresponding to the sub-pixel data signal D20 is displayed.

[0094] As described above, since the first embodiment is designed such that the color correction voltage V60 for each of RGB (VrR, VrG, VrB) is added to the gradation voltages V22-1, V22-2, . . . , V22-n, the sub-pixel data signal D20 is controlled and adjusted independently for each of RGB. Therefore, adjustment of the white balance is enabled without reducing the number of the gradation values of the color image.

Second Embodiment

[0095] FIG. 3 is a block diagram showing an electrical configuration of a liquid crystal display device of a line inversion driving method according to the second embodiment of the present invention. Common reference numerals are given to elements common to elements of FIG. 1 showing the first embodiment.

[0096] In the liquid crystal display device, a signal electrode drive circuit 20A, a control circuit 40A and a gradation voltage generation circuit 50A having a different configuration are provided instead of a signal electrode drive circuit 20, a control circuit 40 and a gradation voltage generation circuit 50 shown in FIG. 1, and further, a polarity inversion circuit 70 is also provided. The signal electrode drive circuit 20A is designed to receive a color correction voltage V70 instead of a color correction voltage V60 (FIG. 1) input to the signal electrode drive circuit 20 (FIG. 1). The control circuit 40A has a function to output a polarity inversion signal Cp in addition to the function of the control circuit 40 (FIG. 1). The gradation voltage generation circuit 50A inverts and outputs a polarity of a gradation voltage V50, for example, in one horizontal line period, based on the polarity inversion signal Cp. The polarity inversion circuit 70 inverts a polarity of a color correction voltage V60 for each of RGB in one horizontal line period based on the polarity inversion signal Cp, and outputs the color correction voltage V70. Other parts of the configuration are approximately the same as that of FIG. 1; and therefore their description has been omitted.

[0097] FIG. 4 is a circuit diagram showing an electrical configuration of the signal electrode drive circuit 20A in FIG. 3.

[0098] As shown in FIG. 4, the signal electrode drive circuit 20A has a same electrical configuration as that of a signal electrode drive circuit 20 shown in FIG. 2. However, the signal electrode drive circuit 20A is different from the signal electrode drive circuit 20 in that the color correction voltage V70 is input to an adding circuit 23 instead of the color correction voltage V60.

[0099] FIG. 5 is a circuit diagram showing an electrical configuration of a circuit for inverting polarity of the color correction voltage V60 of an R component (of RGB) in the polarity inversion circuit 70 of FIG. 3.

[0100] The polarity inversion circuit 70 includes: a switch 71, a switch 72, a buffer 73, a switch 74, a capacitor 75, a switch 76, switch 77 and a switch 78. Circuits for inverting polarity of the color correction voltage V60 of a G component (of RGB) and a B component (of RGB) have the same configuration.

[0101] FIG. 6 is a timing chart showing an operation of the polarity inversion circuit 70. FIG. 7, FIG. 8, FIG. 9 and

FIG. 10 are circuit diagrams respectively showing a state of the polarity inversion circuit 70 based on FIG. 6.

[0102] In the operation of the liquid crystal display device of the embodiment, the following point is different from the above-described first embodiment. Specifically, polarity of the color correction voltage V60 for each of RGB is inverted by the polarity inversion circuit 70 in one horizontal line period based on an adding circuit control signal Ca and a polarity inversion signal Cp, and added to gradation voltages V22-1, V22-2, . . . , V22-n respectively, and thus a sub-pixel data signal D20 (FIG. 4) is generated.

[0103] In this case, at a time T1 of FIG. 6, the adding circuit control signal Ca is "L" (Low) and the polarity inversion signal Cp is "H" (High), and thus the polarity inversion circuit 70 is in a state shown in FIG. 7. Here, a potential of an electrode P1 of the capacitor 75 is R correction voltage VrR (for example, 1V). At a time T2, the adding circuit control signal Ca is "H" and the polarity inversion signal Cp is "H", and thus the polarity inversion circuit 70 is in a state shown in FIG. 8. Here, a potential of the electrode P1 (that is, 1V) of the capacitor 75 is output as the color correction voltage V70 (that is, 1V) via the switch 72, the buffer 73, and the switch 74. At a time T3, the adding circuit control signal Ca is "L" and the polarity inversion signal Cp is "L", and thus the polarity inversion circuit 70 is in a state shown in FIG. 9. Here, the color correction voltage V70 is 0V. At a time T4, the adding circuit control signal Ca is "H" and the polarity inversion signal Cp is "L", and thus the polarity inversion circuit 70 is in a state shown in FIG. 10. Here, the potential of the electrode P2 of the capacitor 75 (that is, -1V) is output as the color correction voltage V70 (that is, -1V) via the switch 72, the buffer 73 and the switch 74.

[0104] As described above, since the second embodiment is designed such that the color correction voltage V60 for each of RGB (VrR, VrG, VrB) is inverted in one horizontal line period and added to the gradation voltages V22-1, V22-2, . . . , V22-n as the color correction voltage V70, the sub-pixel data signal D20 is controlled and adjusted independently for each of RGB. Therefore, similarly to the first embodiment, adjustment of white balance is enabled without reducing the number of a gradation value of a color image.

Third Embodiment

[0105] FIG. 11 is a block diagram showing an electrical configuration of a liquid crystal display device of a dot inversion driving method according to the third embodiment of the present invention. Common reference numerals are given to elements common to elements of FIG. 1 showing the first embodiment and elements of FIG. 2 showing the second embodiment and therefore details of them are omitted.

[0106] In the liquid crystal display device, a signal electrode drive circuit 20B of a different configuration is provided instead of a signal electrode drive circuit 20 shown in FIG. 1. Moreover, the control circuit 40A identical to that of FIG. 3 is provided instead of a control circuit 40 shown in FIG. 1. The signal electrode drive circuit 20B selects a gradation voltage corresponding to a gradation value of an image signal V40 for each of RGB from a gradation voltage V50, inverts a polarity of a color correction voltage V60 for each of RGB based on an adding circuit control signal Ca

and a polarity inversion signal Cp. Then, the color correction voltage V60 for each of RGB with inverted polarity is respectively added to the gradation voltage to generate a sub-pixel data signal D20, and the sub-pixel data signal D20 is sent to each of data signal lines X1, . . . , Xn of the liquid crystal panel. Other parts of the configuration are the same as that of FIG. 1 and their description has been omitted.

[0107] FIG. 12 is a circuit diagram showing an electrical configuration of the signal electrode drive circuit 20B in FIG. 11. Common reference numerals are given to elements common to elements of FIG. 2 showing the first embodiment.

[0108] In signal electrode drive circuit 20B, DAC 22B, and adding circuit 23B having a different configuration are provided instead of a DAC 22 and an adding circuit 23 in FIG. 2. The DAC 22B includes: decoders 22a1, 22a2, . . . , 22an; and selection switches 1-1, 1-2, . . . , 1-128, 2-1, 2-2, . . . , 2-128, . . . , n-1, n-2, . . . , n-128, divides gradation voltages V50 (V1, . . . , VQ) by a voltage dividing resistor circuit (not shown) to generate gradation voltages V1, . . . , V128, selects gradation voltages V22-1, V22-2, . . . , V22-n corresponding to the gradation values V21-1, V21-2, . . . , V21-n of an image signal V40 for each of RGB from the gradation voltages V1, . . . , V128, and outputs selected gradation voltages. As the gradation voltages V50 (V1, . . . , VQ), a voltage of positive polarity and a voltage of negative polarity are supplied, where 0V is a common voltage.

[0109] In the adding circuit 23B, polarity inversion circuits 23j1, 23j2, . . . , 23jn are added to the adding circuit 23. Among them, polarity inversion circuits 23j[2k+1] (where k=0, 1, 2, . . .) in odd numbers have a configuration same as FIG. 5 showing the second embodiment, invert a polarity of a color correction voltage V60 for each of RGB at each sub-pixel based on an adding circuit control signal Ca and a polarity inversion signal Cp, and output an output signal Vj[2k+1] (where k=0, 1, 2, . . .). Polarity inversion circuits 23j[2k] (where k=1, 2, . . .) in even numbers are constituted such that an ON/OFF operation of a switch 72 and a switch 77 in FIG. 5 is made to be opposite to that of the polarity inversion circuits 23j[2k+1]. Other parts of the configuration are approximately same as that of FIG. 2.

[0110] FIG. 13 is a timing chart showing an operation of the polarity inversion circuit 23j[2k] in FIG. 12.

[0111] In an operation of the liquid crystal display device of the embodiment, the following point is different from the above-described second embodiment. That is, as shown in FIG. 13, operation of the polarity inversion circuit 23j[2k] at a time T2 and a time T4 is opposite to operation of polarity inversion circuits 23j[2k+1] shown in FIG. 5. Thus, output voltage Vj2 in antiphase to an output voltage V70 of a polarity inversion circuit 70 is output. Therefore, polarity of the color correction voltage V60 for each of RGB is inverted for each sub-pixel based on the adding circuit control signal Ca and the polarity inversion signal Cp, added to the gradation voltages V22-1, V22-2, . . . , V22-n respectively, and the sub-pixel data signal D20 is generated.

[0112] As described above, since the third embodiment is designed such that the color correction voltage V60 for each of RGB (VrR, VrG, VrB) is inverted at each sub-pixel and added to the gradation voltages V22-1, V22-2, . . . , V22-n, the sub-pixel data signal D20 is controlled and adjusted

independently for each of RGB. Therefore, similarly to the first embodiment, adjustment of white balance is enabled without reducing the number of gradation values of a color image.

Fourth Embodiment

[0113] The foregoing first, second and third embodiments are described as the liquid crystal display device using the color filter of the vertical stripe type shown in FIG. 18(a). This embodiment is the one that deals with the color filters of the mosaic type, the horizontal stripe type and the like in which the arrangement of the color filters of RGB is repeated at every horizontal line.

[0114] FIG. 14 is a block diagram showing an electrical configuration of the liquid crystal display device, which is a fourth embodiment of the present invention. Common reference numerals are given to elements common to elements of FIG. 11 showing the third embodiment.

[0115] In the liquid crystal display device of the fourth embodiment, a control circuit 40B and a signal electrode drive circuit 20C having a different configuration are provided instead of a control circuit 40A and a signal electrode drive circuit 20B in FIG. 11. In addition, a multiplexer (hereinafter, referred to as a MUX) 80 is provided. The control circuit 40B has a configuration where the control circuit 40B has a function to output a control signal S40B (FIG. 15) corresponding to an arrangement of RGB of sub-pixels of the liquid crystal panel 10 in addition to a function of the control circuit 40A. The MUX 80, as shown in FIG. 15, selects a color correction voltage V60 for each RGB (VrR, VrG, VrB), based on the control signal S40B so as to correspond to an arrangement of RGB of the sub-pixels of the liquid crystal panel 10, and outputs color correction voltage V80 (VA, VB, VC) to the signal electrode drive circuit 20C. Other parts of the configuration are the same as that of FIG. 11.

[0116] FIG. 16 is a circuit diagram showing an electrical configuration of the signal electrode drive circuit 20C in FIG. 14.

[0117] Although the signal electrode drive circuit 20C, as shown in FIG. 14, is the electrical configuration similar to the signal electrode drive circuit 20B, it is different in a point where the color correction voltage V80 is input to an adding circuit 23B.

[0118] FIG. 17 is a graph explaining an operation of the MUX 80.

[0119] The operation of the liquid crystal display device of FIG. 14 will be described with reference to FIG. 17.

[0120] In the liquid crystal display device, the control signal S40B corresponding to the arrangement of RGB of each color filter is output from the control circuit 40B even in a case where the color filters of the liquid crystal panel 10 are not only of the vertical-stripe type, the mosaic type and the triangle type but also in the horizontal-stripe type. The control signal S40B is input to the MUX 80, the color correction voltage V80 for each of RGB is selected from the MUX 80 so as to correspond to the arrangement of RGB of the color filter and the selected color correction voltage V80 is output to the signal electrode drive circuit 20C.

[0121] In this case, as shown in FIG. 17, when the control signal S40B corresponds to the color filter of the vertical-stripe type, the color correction voltage V60 (VA, VB, VC) corresponding to the vertical-stripe type is output from the MUX 80 and sent to the signal electrode drive circuit 20C. When the control signal S40B corresponds to the color filter of the mosaic type, the color correction voltage V60 (VA, VB, VC) corresponding to the mosaic type is output from the MUX 80 and sent to the signal electrode drive circuit 20C. When the control signal S40B corresponds to the color filter of the horizontal-stripe type, the color correction voltage V60 (VA, VB, VC) corresponding to the horizontal-stripe type is output from the MUX 80 and sent to the signal electrode drive circuit 20C. Thereafter, operation similar to the third embodiment is performed.

[0122] As described above, in the fourth embodiment, the control circuit 40B for outputting the control signal S40B corresponding to the arrangement of RGB of the sub-pixel and the MUX 80 for selecting and outputting the color correction voltage V60 of each of RGB so as to correspond to the arrangement of RGB of the sub-pixel of the liquid crystal panel 10, based on the control signal S40B are provided. Accordingly, in addition to the advantages of the third embodiment, the fourth embodiment can be applied to various color filters.

[0123] It is apparent that the present invention is not limited to the above embodiments but may be changed and modified without departing from the scope and spirit of the invention.

[0124] For example, the color filters are not limited to the three colors of RGB, but may be four colors (for example, including cyan or a like) for example. Moreover, the polarity inversion of the color correction voltage is not limited to the inversion in one horizontal line period, but may be the inversion in two horizontal line periods. Further, the control circuit 40B and the MUX 80 in FIG. 14 showing the fourth embodiment may be provided in FIG. 1, FIG. 3 or FIG. 11 showing other embodiments.

What is claimed is:

1. A liquid crystal display device having a liquid crystal panel for displaying a color image, wherein:

a color correction voltage generation circuit is provided for generating a color correction voltage for each of red, green, and blue based on a given input signal for color correction, and

said color correction voltage for each of said red, green, and blue is added to a gradation voltage of an image signal for said each of said red, green, and blue respectively, and the added voltages are supplied to said liquid crystal panel.

2. A liquid crystal display device, comprising:

a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of red, green, and blue, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of said data signal lines and each of said scanning signal lines intersect, and said liquid crystal panel displaying a color image corresponding to said sub-pixel data signal by supplying said sub-pixel data signal to a sub-pixel region selected by said scanning signal among said plurality of sub-pixel regions;

a gradation voltage generation circuit for generating a plurality of a gradation voltages to give gradation to said sub-pixel data signal;

a color correction voltage generation circuit for generating a color correction voltage for each of said red, green, and blue based on a given signal for color correction;

a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for said each of said red, green, and blue from said each gradation voltage, adding said color correction voltage for said each of said red, green, and blue respectively to said gradation voltage to generate said sub-pixel data signal, and sending said sub-pixel data signal to said each data signal line of said liquid crystal panel;

a scanning signal circuit for sending said scanning signal to said each scanning signal line of said liquid crystal panel synchronously with a clock signal; and

a control circuit for outputting said clock signal and said image signal for said each of said red, green, and blue.

3. A liquid crystal display device, comprising:

a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of said red, green, and blue, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of said data signal lines and each of said scanning signal lines intersect, and said liquid crystal panel displaying a color image corresponding to said sub-pixel data signal by supplying said sub-pixel data signal to a sub-pixel region selected by said scanning signal among said plurality of sub-pixel regions;

a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to said sub-pixel data signal, inverting a polarity of said gradation voltage in one frame period based on a polarity inversion signal, and outputting said gradation voltage with said inverted polarity;

a color correction voltage generation circuit for generating a color correction voltage for each of said red, green, and blue based on a given input signal for color correction, inverting a polarity of said color correction voltage in one frame period based on said polarity inversion signal, and outputting said color correction voltage with said inverted polarity;

a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for said each of said red, green, and blue from said each gradation voltage, adding said color correction voltage for said each of said red, green, and blue respectively to said gradation voltage to generate said sub-pixel data signal, and sending said sub-pixel data signal to said each data signal line of said liquid crystal panel;

a scanning signal circuit for sending said scanning signal to said each scanning signal line of said liquid crystal panel synchronous with a clock signal; and

a control circuit for outputting said clock signal and said image signal for said each of said red, green, and blue.

4. A liquid crystal display device, comprising:

a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a

sub-pixel where a pixel is divided into three primary colors of said red, green, and blue, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of said data signal lines and each of said scanning signal lines intersect, and said liquid crystal panel displaying a color image corresponding to said sub-pixel data signal by supplying said sub-pixel data signal to a sub-pixel region selected by said scanning signal among said plurality of sub-pixel regions;

- a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to said sub-pixel data signal, inverting a polarity of said gradation voltage in a specified number of horizontal line periods based on a polarity inversion signal, and outputting said gradation voltage with said inverted polarity;
- a color correction voltage generation circuit for generating a color correction voltage for said each of said red, green, and blue based on a given input signal for color correction;
- a polarity inversion circuit for inverting a polarity of said color correction voltage for said each of said red, green, and blue in a specified number of horizontal line periods based on said polarity inversion signal, and outputting said color correction voltage with said inverted polarity;
- a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for said each of said red, green, and blue from said each gradation voltage, adding said color correction voltage for said each of said red, green, and blue respectively to said gradation voltage to generate said sub-pixel data signal, and sending said sub-pixel data signal to said each data signal line of said liquid crystal panel;
- a scanning signal circuit for sending said scanning signal to said each scanning signal line of said liquid crystal panel synchronously with a clock signal; and
- a control circuit for outputting said clock signal, said image signal for said each of said red, green, and blue and said polarity inversion signal.

5. A liquid crystal display device, comprising:

- a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of said red, green, and blue, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of said data signal lines and each of said scanning signal lines intersect, and said liquid crystal panel displaying a color image corresponding to said sub-pixel data signal by supplying said sub-pixel data signal to a sub-pixel region selected by said scanning signal among said plurality of sub-pixel regions;
- a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to said pixel data signal;
- a color correction voltage generation circuit for generating a color correction voltage for each of said red, green, and blue based on a given input signal for color correction;

a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for said each of said red, green, and blue from said each gradation voltage, inverting said color correction voltage for said each of said red, green, and blue at said each sub-pixel based on a polarity inversion signal and adding said color correction voltage with said inverted polarity to said gradation voltage to generate said sub-pixel data signal, and sending said sub-pixel data signal to said each data signal line of said liquid crystal panel;

a scanning signal circuit for sending said scanning signal to said each scanning signal line of said liquid crystal panel synchronously with a clock signal; and

a control circuit for outputting said clock signal, said image signal for said each of said red, green, and blue and said polarity inversion signal.

6. A liquid crystal display device, comprising:

a liquid crystal panel having a plurality of data signal lines for receiving a sub-pixel data signal corresponding to a sub-pixel where a pixel is divided into three primary colors of said red, green, and blue, a plurality of scanning signal lines for receiving a scanning signal, and a plurality of sub-pixel regions provided at points where each of said data signal lines and each of said scanning signal lines intersect, and said liquid crystal panel displaying a color image corresponding to said sub-pixel data signal by supplying said sub-pixel data signal to a sub-pixel region selected by said scanning signal among said plurality of sub-pixel regions;

a gradation voltage generation circuit for generating a plurality of gradation voltages to give gradation to said sub-pixel data signal;

a color correction voltage generation circuit for generating a color correction voltage for said each of said red, green, and blue based on a given input signal for color correction;

a multiplexer for selecting and outputting said color correction voltage for said each of said red, green, and blue in accordance with an arrangement of said red, green, and blue color filters in a horizontal direction of said sub-pixels on said liquid crystal panel, based on a control signal;

a display signal circuit for selecting a gradation voltage corresponding to a gradation value of an image signal for said each of said red, green, and blue from each gradation voltage, adding said color correction voltage for said each of said red, green, and blue output from said multiplexer respectively to said gradation voltage to generate said sub-pixel data signal, and sending said sub-pixel data signal to said each data signal line of said liquid crystal panel;

a scanning signal circuit for sending said scanning signal to said each scanning signal line of said liquid crystal panel synchronously with a clock signal; and

a control circuit for outputting said clock signal, said image signal for said each of said red, green, and blue and said control signal.

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专利名称(译)	液晶显示装置		
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摘要(译)

本发明提供一种能够对RGB中的每一个独立地调整灰度的液晶显示装置。控制电路输出时钟信号，RGB中的每一个的图像信号和加法电路控制信号。灰度电压产生电路输出灰度电压。基于用于颜色校正的输入信号，在颜色校正电压产生电路中产生RGB中的每一个的颜色校正电压。信号电极驱动电路接收时钟信号，控制信号，图像信号，加法电路控制信号，灰度电压和颜色校正电压。从灰度电压中选择对应于每个RGB的图像信号的灰度值的灰度电压。将RGB中的每一个的颜色校正电压加到灰度电压，然后产生子像素数据信号并将其发送到液晶面板。

