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CHO et al.(10) **Pub. No.: US 2011/0102694 A1**(43) **Pub. Date: May 5, 2011**(54) **MOTHER SUBSTRATE FOR LIQUID
CRYSTAL DISPLAY AND MANUFACTURING
METHOD THEREOF****Publication Classification**(51) **Int. Cl.**
G02F 1/1343 (2006.01)
H01L 21/28 (2006.01)(76) **Inventors:** **Ilman CHO**, Buk-gu (KR);
Yongmin Kim, Seongbuk-gu (KR)(52) **U.S. Cl. 349/39; 438/34; 257/E21.158**(21) **Appl. No.: 12/907,534**(22) **Filed: Oct. 19, 2010**(57) **ABSTRACT**(30) **Foreign Application Priority Data**

Oct. 30, 2009 (KR) 10-2009-0104372

A mother substrate for a liquid crystal display comprises a plurality of active matrix arrays, test lines connected to the active matrix arrays, test pads connected to the test lines, and connection lines connecting test lines to each other.

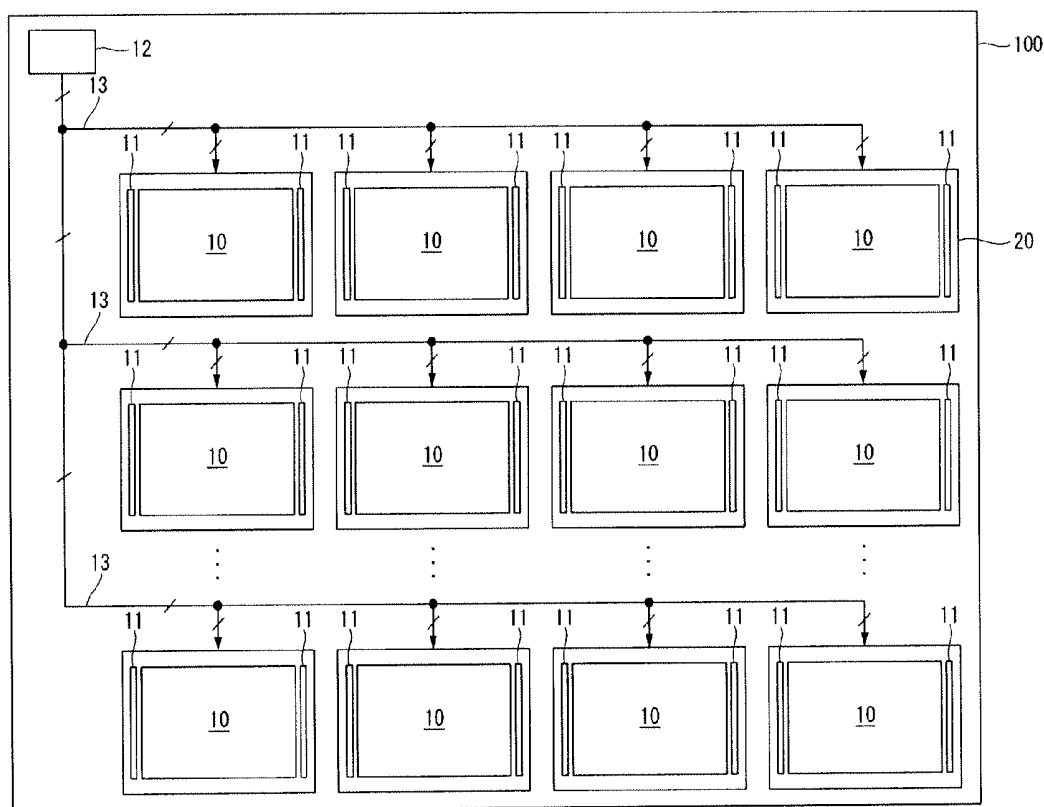


FIG. 1
(RELATED ART)

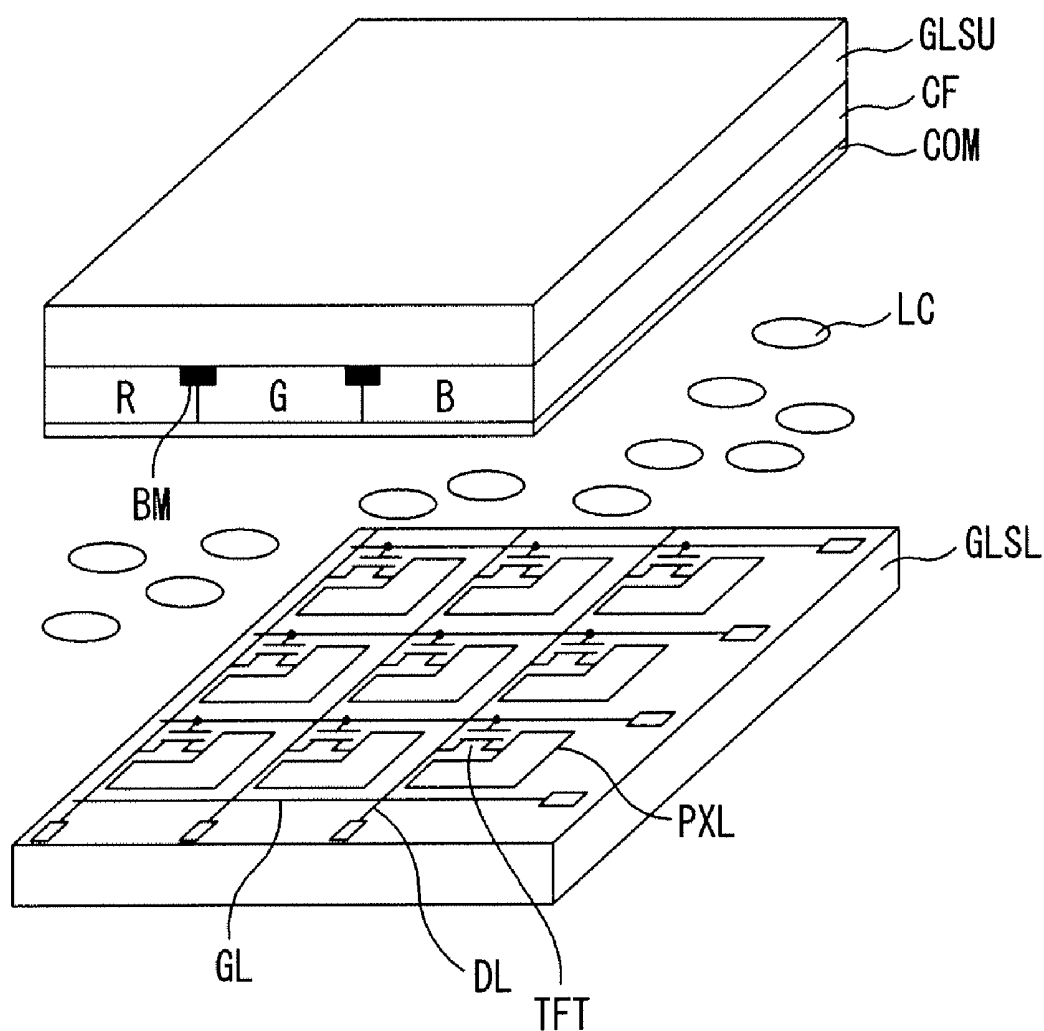


FIG. 2

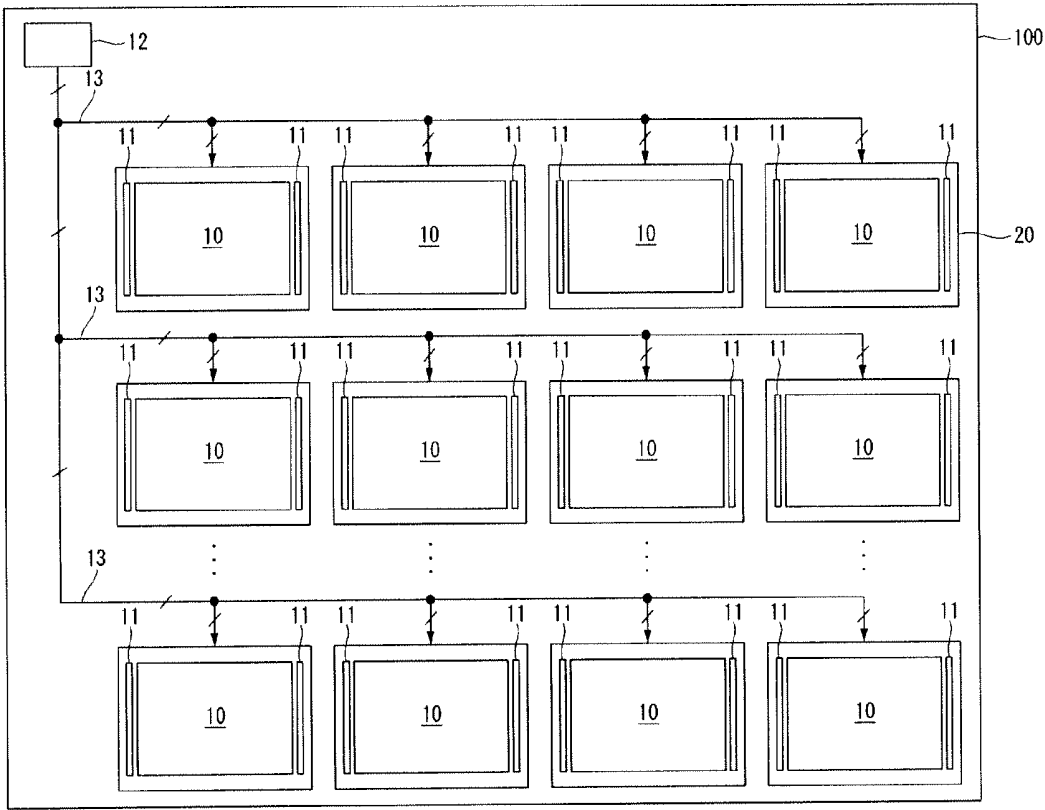


FIG. 3

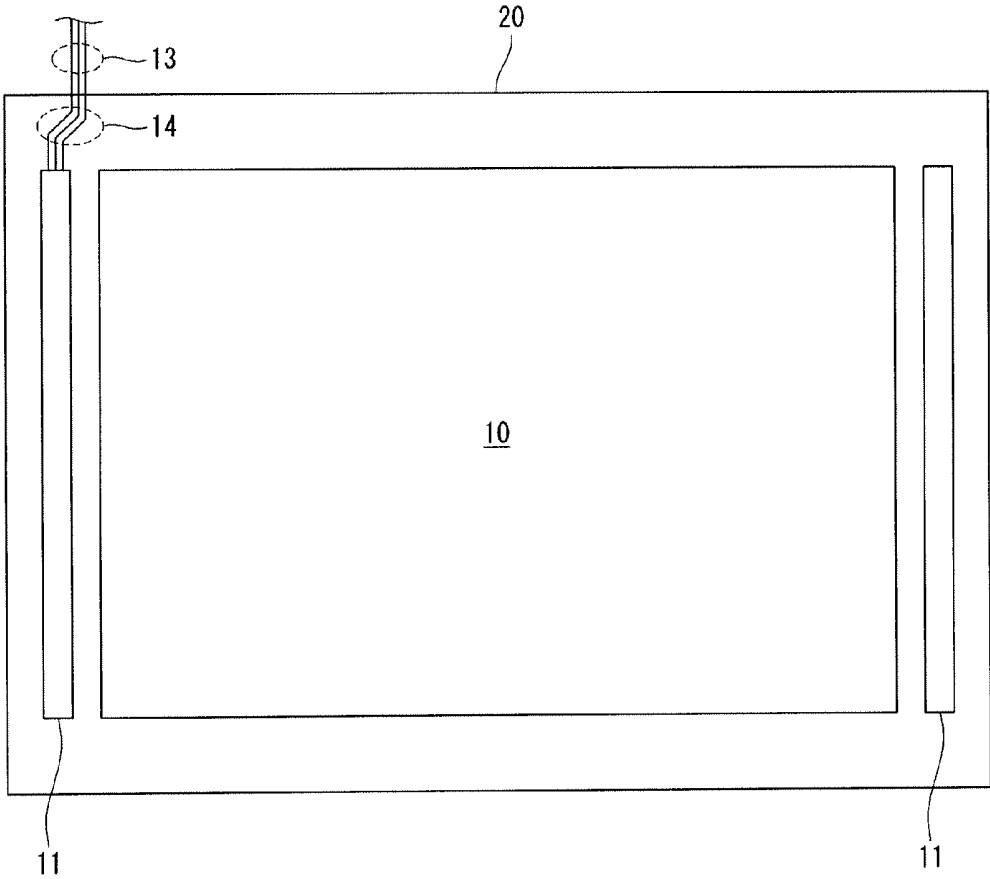


FIG. 4

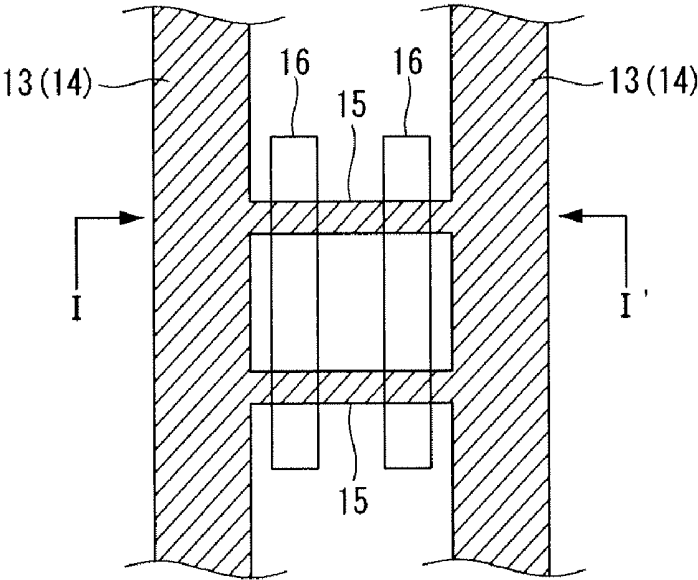


FIG. 5

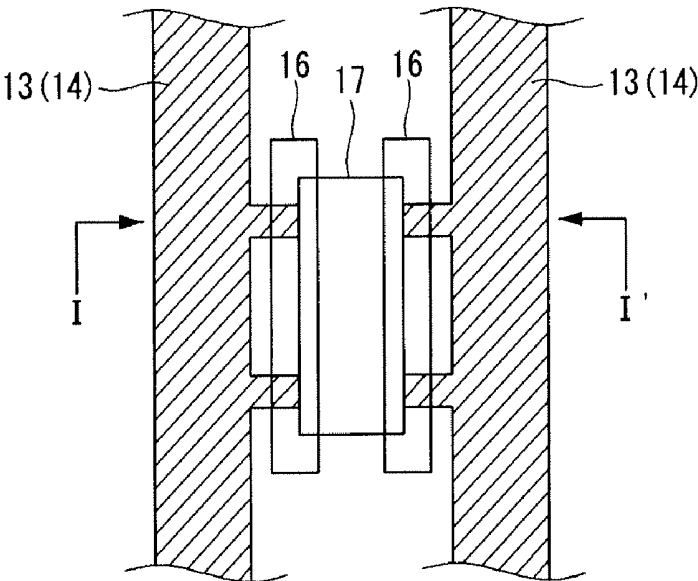


FIG. 6

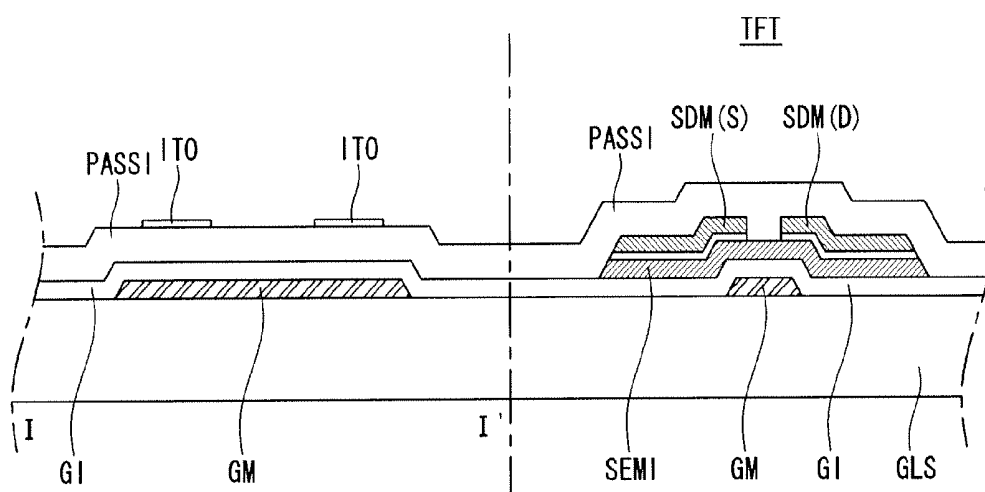


FIG. 7

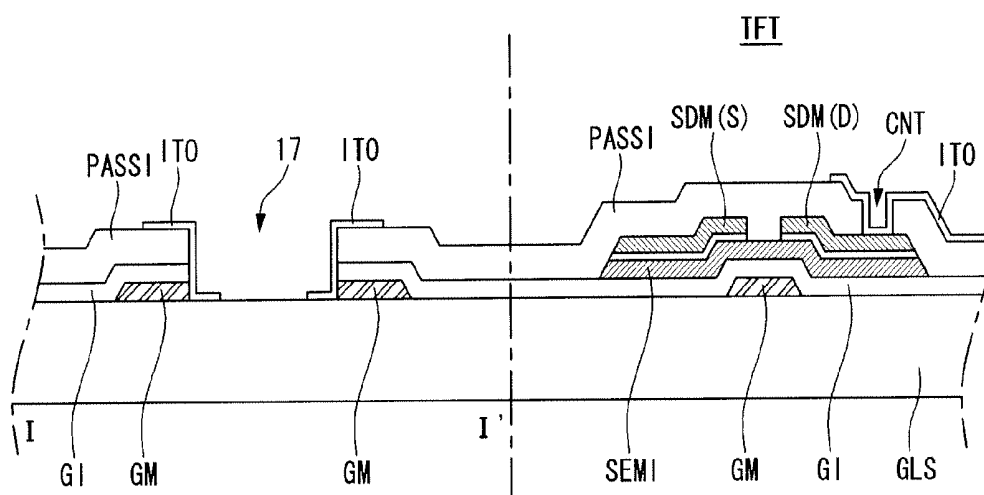


FIG. 8

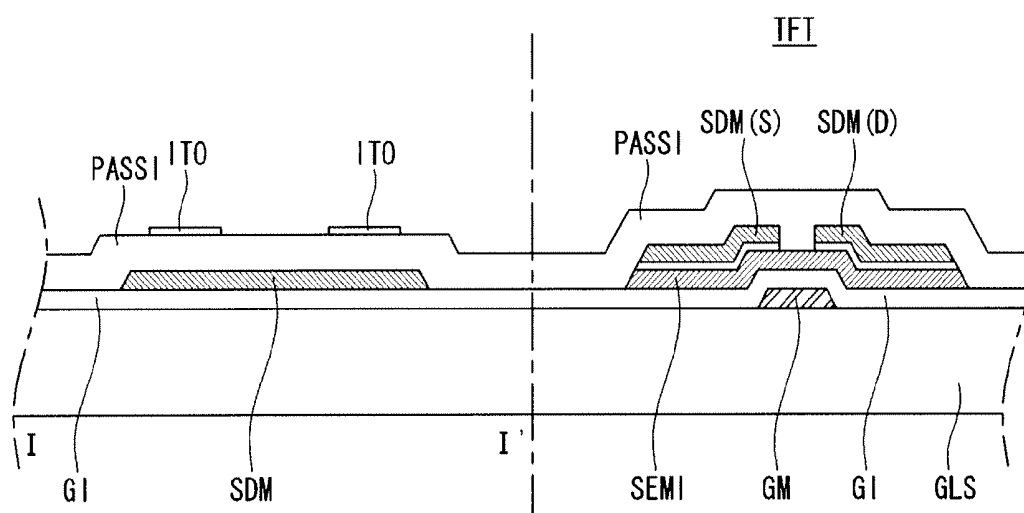
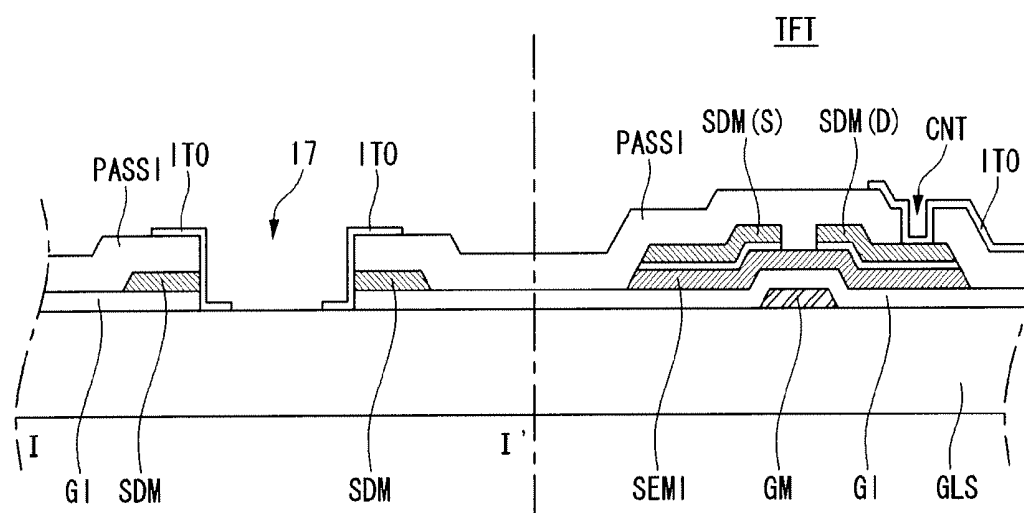


FIG. 9



**MOTHER SUBSTRATE FOR LIQUID
CRYSTAL DISPLAY AND MANUFACTURING
METHOD THEREOF**

[0001] This application claims the benefit of Korea Patent Application No. 10-2009-0104372 filed on Oct. 30, 2009, the entire contents of which is incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This document relates to a mother substrate provided with a plurality of active matrix arrays and a manufacturing method thereof.

[0004] 2. Related Art

[0005] A liquid crystal display ("LCD") has been widely applied due to its lightweight, thin profile, lower power consumption driving, and so on. Such an LCD has been employed as a portable computer such as a notebook PC, an office automation device, an audio/video device, an indoor/outdoor advertisement display device or the like.

[0006] Referring to FIG. 1, a lower glass substrate GLSL of the active matrix LCD is provided with data lines DL and gate lines GL intersecting each other. At the intersections of the data lines DL and the gate lines GL, TFTs (thin film transistors) and pixel electrodes, which are connected to each other, are arranged in a matrix. An upper glass substrate GLSU is provided with black matrices BM, color filters CF, and common electrodes COM. A lower polarizer is attached to a light incidence plane of the lower glass substrate GLSL, and an upper polarizer, having the light absorption axis perpendicular to the light absorption axis of the lower polarizer, is attached to a light emission plane of the upper glass substrate GLSU. In addition, alignment layers are formed having contact with a liquid crystal layer LC between the lower glass substrate GLSL and the upper glass substrate GLSU.

[0007] In order to increase productivity of the LCD, a plurality of active matrix arrays are formed on a large-sized mother substrate together, and thereafter the active matrix arrays are divided into each other through a scribing process and a grinding process.

[0008] In the course of thin film patterning on the mother substrate, static electricity is generated during the deposition process, the etching process, and so forth. If line materials formed on the mother substrate are metals with low resistance, the static electricity is easily applied to the active matrix arrays via the line materials. The static electricity deteriorates characteristics of elements in the active matrix arrays or causes dielectric breakdown.

SUMMARY OF THE INVENTION

[0009] Embodiments of this document provide a mother substrate of a liquid crystal display and a manufacturing method thereof, capable of blocking static electricity generated during manufacturing of the mother substrate.

[0010] According to an exemplary embodiment of this document, there is provided a mother substrate for a liquid crystal display, comprises a plurality of active matrix arrays; test lines connected to the active matrix arrays; test pads connected to the test lines; and first connection lines connecting test lines to each other.

[0011] Each of the active matrix arrays may comprise a TFT array including data lines, gate lines intersecting the data lines, TFTs connected to the data lines and the gate lines, pixel electrodes connected to the TFTs, and storage capacitors connected to the pixel electrodes; a driving circuit unit sequentially supplying gate pulses to the gate lines; and LOG lines connecting the test lines to the driving circuit unit.

[0012] Each of the active matrix arrays may further comprise second connection lines connecting the LOG lines to each other.

[0013] According to an exemplary embodiment of this document, there is provided a method of manufacturing a mother substrate of a liquid crystal display, comprising forming a plurality of active matrix arrays, test lines connected to the active matrix arrays, test pads connected to the test lines, and first connection lines connecting the test lines to each other on the mother substrate, respectively; forming a passivation layer covering the plurality of active matrix arrays, the test lines, the test pad, and the connection lines on the mother substrate; and forming a first open hole disconnecting the first connection lines during an etching process of the passivation layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0015] FIG. 1 is a perspective view schematically illustrating an LCD;

[0016] FIG. 2 is a plan view illustrating a mother substrate of an LCD according to an embodiment of this document;

[0017] FIG. 3 is an enlarged plan view illustrating the active matrix array shown in FIG. 2;

[0018] FIG. 4 is a plan view illustrating connection lines formed between test lines, and between LOG lines.

[0019] FIG. 5 is a plan view illustrating connection lines removed during an etching process of a passivation layer;

[0020] FIG. 6 is a sectional view taken along the line I-I' in FIG. 4 and shows an example where the connection lines are formed of gate metal patterns;

[0021] FIG. 7 is a sectional view taken along the line I-I' in FIG. 5 and shows disconnection of the connection lines shown in FIG. 6;

[0022] FIG. 8 is a sectional view taken along the line I-I' in FIG. 4 and shows an example where the connection lines are formed of source/drain metal patterns; and

[0023] FIG. 9 is a sectional view taken along the line I-I' and shows disconnection of the connection lines shown in FIG. 8.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Hereinafter, embodiments of this document will be described in detail with reference to the accompanying drawings. Like reference numerals designate like elements throughout the specification. In the following description, when a detailed description of well-known functions or configurations related to this document is determined to unnecessarily cloud a gist of the present invention, the detailed description thereof will be omitted.

[0025] The LCD according to this document may be implemented, when classified by LC modes, by a TN (twisted

nematic) mode, a VA (vertical alignment) mode, an IPS (in plane switching) mode, an FFS (fringe field switching) mode, or the like. In view of a structure, the LCD according to this document may be implemented by any other type, for example, such as a transmissive LCD, a transfective LCD, a reflective LCD, or the like. The transmissive LCD and the transfective LCD require a backlight unit. The backlight unit may be implemented by a direct type backlight unit or an edge type backlight unit.

[0026] According to this document, during manufacturing the LCD, a plurality of active matrix arrays is formed together on a mother substrate **100** as shown in FIG. 2.

[0027] In FIGS. 2 and 3, the mother substrate **100** is provided with a plurality of active matrix arrays **20**, a test pad **12**, and test lines **13**.

[0028] Each of the active matrix arrays **20** is provided with a TFT array **10**, a driving circuit unit **11** for driving the TFT array **10**, and LOG (line on glass) lines **14**. The TFT array **10** is provided with data lines, gate lines intersecting the data lines, TFTs connected to the data lines and the gate lines, pixel electrodes connected to the TFTs, storage capacitors connected to the pixel electrodes, and so forth. The driving circuit unit **11** comprises gate driving circuits for sequentially gate pulses to the gate lines. The LOG lines **14** connect the test lines **13** to the driving circuit unit **11**.

[0029] The test pads **12** have contact with a probe of an external test jig and supplies a test signal and a driving power output from the test jig to the test lines **13**. The test pad is formed at one edge of the mother substrate **100**.

[0030] The test lines **13** are formed between the test pad **12** and the LOG lines **14**, and transmit the test signal and the driving power from the test pad to the LOG lines **14**.

[0031] A thin film patterning process of the mother substrate **100** includes a plurality of deposition and etching processes, thereby forming thin film patterns in the TFT array **10**, the driving circuit unit **11** for driving the TFT array **10**, the LOG lines **14**, the test pad **12**, and the test lines **13**.

[0032] In order to block static electricity generated during the deposition process and the etching process, in this document, connection lines **15** are formed between the test lines **13** so as to be connected to each other. Also, in this document, the connection lines **15** are formed between the LOG lines **14** so as to be connected to each other. Static electricity is dispersed through the connection lines **15** and thereby static electricity flowing towards the driving circuit unit **11** can be blocked. The connection lines **15** do not comprise diodes or transistor elements, but comprises only metal line patterns.

[0033] The connection lines **15** may be formed of gate line patterns and/or source/drain metal patterns. Thus, there is no need for a separate process for forming the connection lines **15**.

[0034] The connection lines **15** are removed by an open hole which is formed during an etching process of a passivation layer as shown in FIG. 5. Transparent conductive patterns **16** are formed at both edges of the open hole **17**. The transparent conductive patterns **16** prevent remaining metals of the connection lines **15** from being exposed to air and thus the metals being oxidized. After the connection lines **15** are removed, the probe of the test jig has contact with the test pad **12**. When the test jig has contact with the test pad **12**, the active matrix arrays are all inspected at the same time. Following the inspection, the active matrix arrays are individually separated from each other through a scribing process and a grinding process.

[0035] The mother substrate **100** in this document can be manufactured using the two-mask process, the three-mask process, or the four-mask process in the related art. An embodiment of a method of manufacturing the mother substrate **100** will be described by exemplifying the four-mask process. Of course, the mother substrate **100** may be manufactured using the two-mask process or the three-mask process.

[0036] FIG. 6 is a sectional view illustrating an example where the connection lines **15** is formed of a gate metal pattern. FIG. 7 is a sectional view illustrating disconnection of the connection lines **15** shown in FIG. 6.

[0037] Referring to FIGS. 6 and 7, in a manufacturing method of the mother substrate according to a first embodiment, a gate metal layer is formed on the mother substrate **100** using a deposition method such as sputtering. The gate metal may be selected from an aluminum (Al) based metal including aluminum/neodymium (AlNd), molybdenum (Mo), copper (Cu), chrome (Cr), tantalum (Ta), titanium (Ti), or the like.

[0038] The gate metal layer is patterned during a first photolithography process. The gate lines, gate electrodes and gate pads of the TFTs connected to the gate lines, in the TFT array **10**, and the like are formed of the gate metal pattern GM. Along with the gate metal pattern GM in the TFT array **10**, the gate metal pattern of the driving circuit unit **11**, and the gate metal pattern GM of the test lines **12** and the connection lines **15** are formed.

[0039] Next, a gate insulating layer GI, a semiconductor layer, and a source/drain metal layer are consecutively deposited to cover the gate metal patterns GM. The gate insulating layer GI may be made of an inorganic insulating material such as silicon oxide (SiO_x) or silicon nitride (SiN_x). The source/drain metal may be selected from molybdenum (Mo), titanium (Ti), tantalum (Ta), molybdenum alloy, copper (Cu), or the like. The semiconductor layer and the source/drain metal layer are patterned together during a second photolithography process. The semiconductor pattern SEMI includes an amorphous silicon layer doped with no impurities and an ohmic contact layer doped with impurities. The data lines and the source/drain electrodes SDM(S) and SDM(D) in the TFT array **10**, and data pads are formed of source/drain metal pattern. Along with the source/drain metal pattern in the TFT array **10**, the source/drain metal pattern of the driving circuit unit **11** and the source/drain metal pattern of the test lines **12** are formed.

[0040] Subsequently, a passivation layer PASSI covering the active matrix array **20**, the test pad **12**, and the test lines is deposited on the mother substrate **100**. The passivation layer PASSI may be made of inorganic insulating material the same as the gate insulating layer GI, acryl based organic compound with a small dielectric constant, or organic insulating material such as BCB (bebzocyclobutane) and PFCB (perfluorocyclobutane).

[0041] Next, the passivation layer PASSI is etched during a third photolithography process. During the third photolithography process, as shown in FIG. 7, a contact hole CNT for exposing a portion of the drain electrode SDM(D) of the TFT of the active matrix array **20**, the open hole **17** for disconnecting the gate metal pattern GM of the connection lines **15**, and contact holes for exposing the gate metal pattern and the source/drain metal pattern of the test pad **12** are formed together.

[0042] Thereafter, a transparent conductive layer covering the passivation layer PASSI is deposited and then the transparent conductive layer is patterned during a fourth photolithography process. The transparent conductive layer may be made of indium tin oxide (ITO), tin oxide (TO), indium tin zinc oxide (ITZO), or indium zinc oxide (IZO). The transparent conductive layer pattern comprises the pixel electrodes of the active matrix array 20, top electrodes of the gate pads and the data pads, a top electrode of the test pad 12, and top electrodes covering the edges of the open hole 17.

[0043] FIG. 8 is a sectional view illustrating an example where the connection lines 15 are formed of the source/drain metal patterns. FIG. 9 is a sectional view illustrating disconnection of the connection lines 15 shown in FIG. 8.

[0044] Referring to FIGS. 8 and 9, in a manufacturing method of a mother substrate according to a second embodiment of this document, the connection lines 15 are formed of the source/drain metal patterns SDM, and the connection lines 15 are disconnected during the etching process of the passivation layer PASSI. The order of the manufacturing processes is substantially the same as in the above-described first embodiment.

[0045] As described above, in this document, the test lines on the mother substrate are connected to each other using the connection lines, and the connection lines are disconnected during the etching process of the passivation layer, thereby blocking static electricity generated during the deposition process, the etching process, and so forth, by using the connection lines.

[0046] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

1. A mother substrate for a liquid crystal display, comprising:

- a plurality of active matrix arrays;
- test lines connected to the active matrix arrays;
- test pads connected to the test lines; and
- first connection lines connecting test lines to each other.

2. The mother substrate of claim 1, wherein each of the active matrix arrays comprises:

- a TFT array including data lines, gate lines intersecting the data lines, TFTs connected to the data lines and the gate

- lines, pixel electrodes connected to the TFTs, and storage capacitors connected to the pixel electrodes;
- a driving circuit unit sequentially supplying gate pulses to the gate lines; and

LOG lines connecting the test lines to the driving circuit unit.

3. The mother substrate of claim 2, wherein each of the active matrix arrays further comprises second connection lines connecting the LOG lines to each other.

4. A method of manufacturing a mother substrate of a liquid crystal display, comprising:

- forming a plurality of active matrix arrays, test lines connected to the active matrix arrays, test pads connected to the test lines, and first connection lines connecting the test lines to each other on the mother substrate, respectively;

forming a passivation layer covering the plurality of active matrix arrays, the test lines, the test pad, and the connection lines on the mother substrate; and

forming a first open hole disconnecting the first connection lines during an etching process of the passivation layer.

5. The method of claim 4, further comprising forming transparent conductive patterns on edges of the first open hole.

6. The method of claim 5, wherein each of the active matrix arrays comprises:

- a TFT array including data lines formed of source/drain metal patterns, gate lines intersecting the data lines and formed of gate metal patterns, TFTs connected to the data lines and the gate lines, pixel electrodes connected to the TFTs, and storage capacitors connected to the pixel electrodes;

a driving circuit unit sequentially supplying gate pulses to the gate lines; and

LOG lines connecting the test lines to the driving circuit unit.

7. The method of claim 6, wherein the step of forming of the first connection lines on the mother substrate comprises forming second connection lines connecting the LOG lines to each other.

8. The method of claim 7, wherein the step of forming of the first open hole comprises

- forming a second open hole disconnecting the second connection lines during the etching process of the passivation layer.

9. The method of claim 8, wherein the first and second connection lines are formed of the source/drain metal patterns.

10. The method of claim 8, wherein the first and second connection lines are formed of the gate metal patterns.

* * * * *

专利名称(译)	用于液晶显示器的母基板及其制造方法		
公开(公告)号	US20110102694A1	公开(公告)日	2011-05-05
申请号	US12/907534	申请日	2010-10-19
[标]申请(专利权)人(译)	CHO ILMAN KIM王永民		
申请(专利权)人(译)	CHO ILMAN KIM王永民		
当前申请(专利权)人(译)	CHO ILMAN KIM王永民		
[标]发明人	CHO ILMAN KIM YONGMIN		
发明人	CHO, ILMAN KIM, YONGMIN		
IPC分类号	G02F1/1343 H01L21/28		
CPC分类号	H01L27/124		
优先权	1020090104372 2009-10-30 KR		
其他公开文献	US8339565		
外部链接	Espacenet USPTO		

摘要(译)

用于液晶显示器的母基板包括多个有源矩阵阵列，连接到有源矩阵阵列的测试线，连接到测试线的测试焊盘，以及将测试线彼此连接的连接线。

