



US 20080062103A1

(19) **United States**(12) **Patent Application Publication**
YOU(10) **Pub. No.: US 2008/0062103 A1**(43) **Pub. Date: Mar. 13, 2008**(54) **DISPLAY PANEL, DISPLAY DEVICE HAVING
THE DISPLAY PANEL AND METHOD OF
OPERATING THE DISPLAY DEVICE****Publication Classification**(51) **Int. Cl.**
G09G 3/36 (2006.01)(52) **U.S. Cl.** **345/89; 345/87**(57) **ABSTRACT**(76) **Inventor: Bong-Hyun YOU, Yongin-si (KR)**

Correspondence Address:
MACPHERSON KWOK CHEN & HEID LLP
2033 GATEWAY PLACE, SUITE 400
SAN JOSE, CA 95110

(21) **Appl. No.: 11/850,419**(22) **Filed: Sep. 5, 2007**(30) **Foreign Application Priority Data**

Sep. 7, 2006 (KR) 2006-85949

A display panel includes a first switching element, a liquid crystal capacitor and a second switching element. The first switching element receives a gate signal and a data signal. The liquid crystal capacitor is connected to the first switching element, and charged with an initial pixel voltage corresponding to the data signal. The second switching element operates in response to a compensation gate signal applied from a compensation gate line. The compensation capacitor is connected to the second switching element to reduce the liquid crystal capacitor's voltage to a value below the initial pixel voltage when the second switching element is turned on. Accordingly, motion blur can be reduced or eliminated.

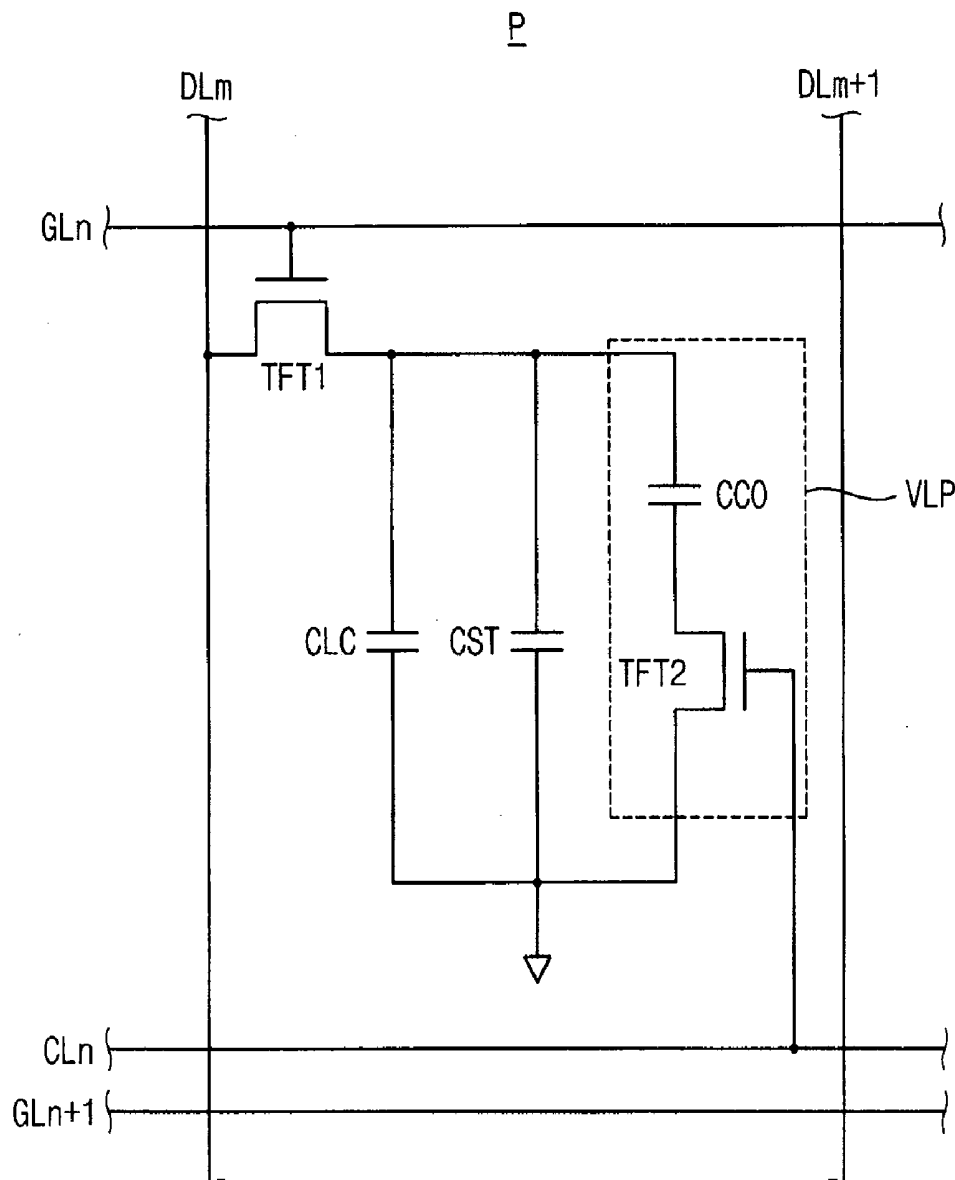


FIG. 1

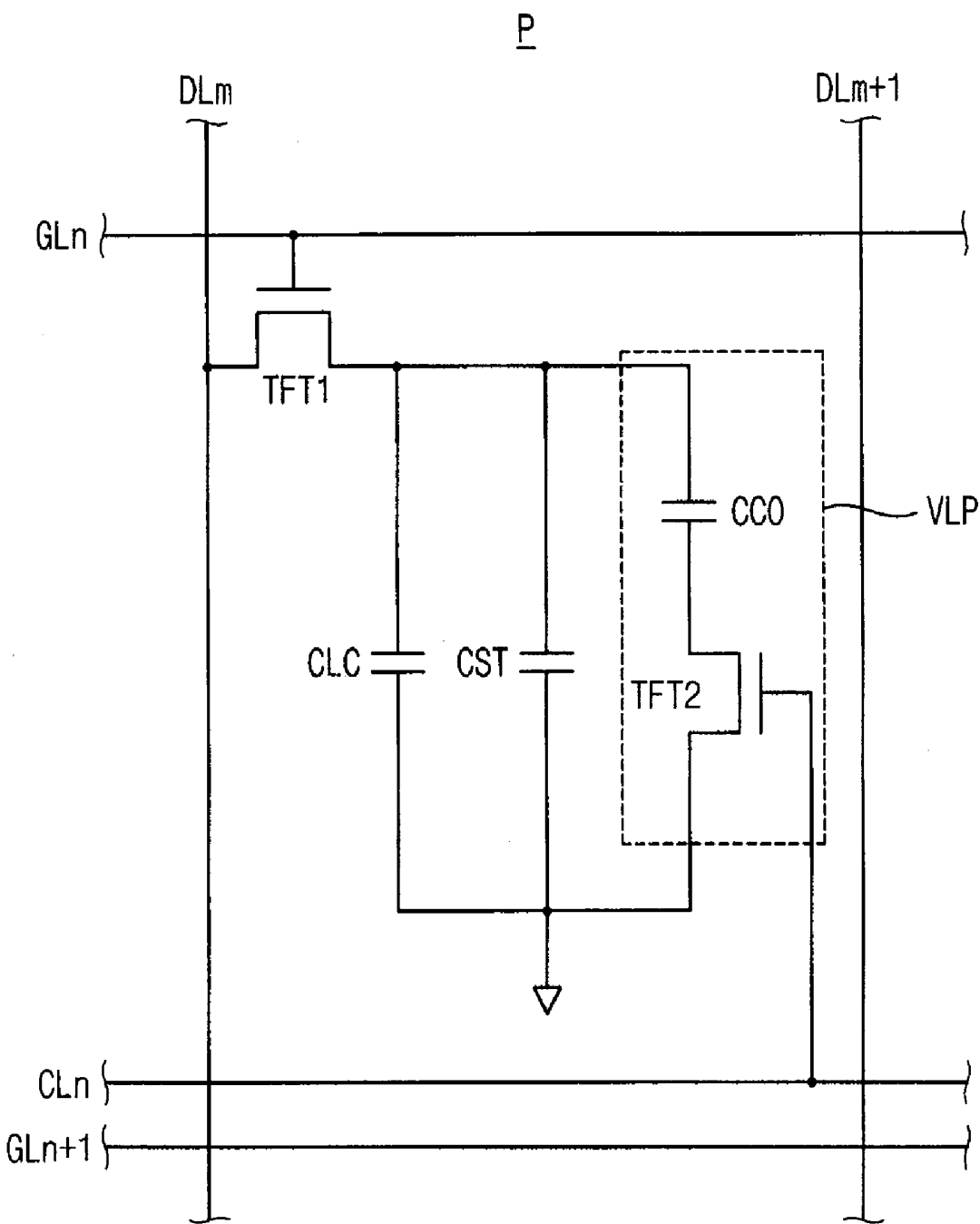


FIG. 2

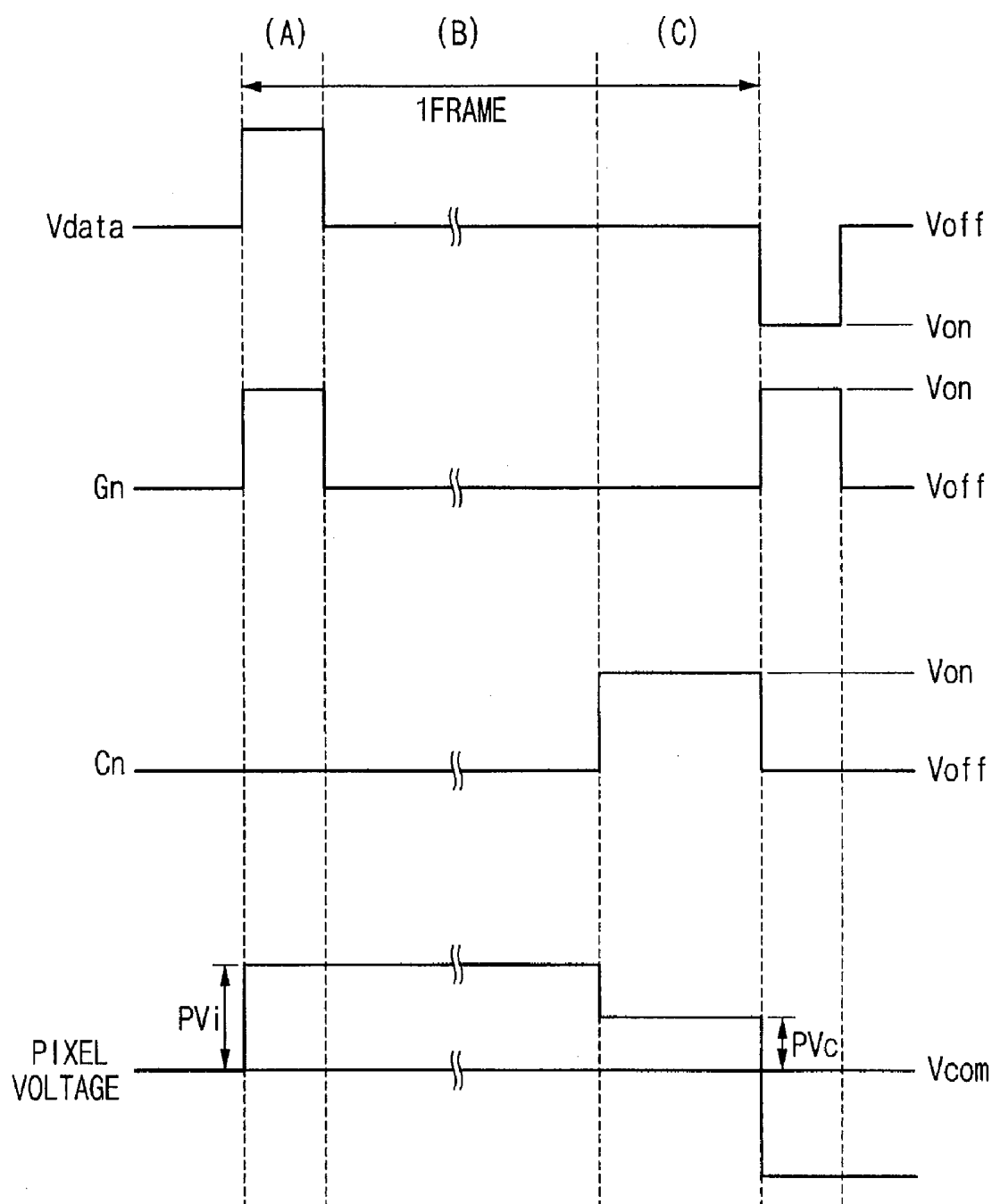


FIG. 3C

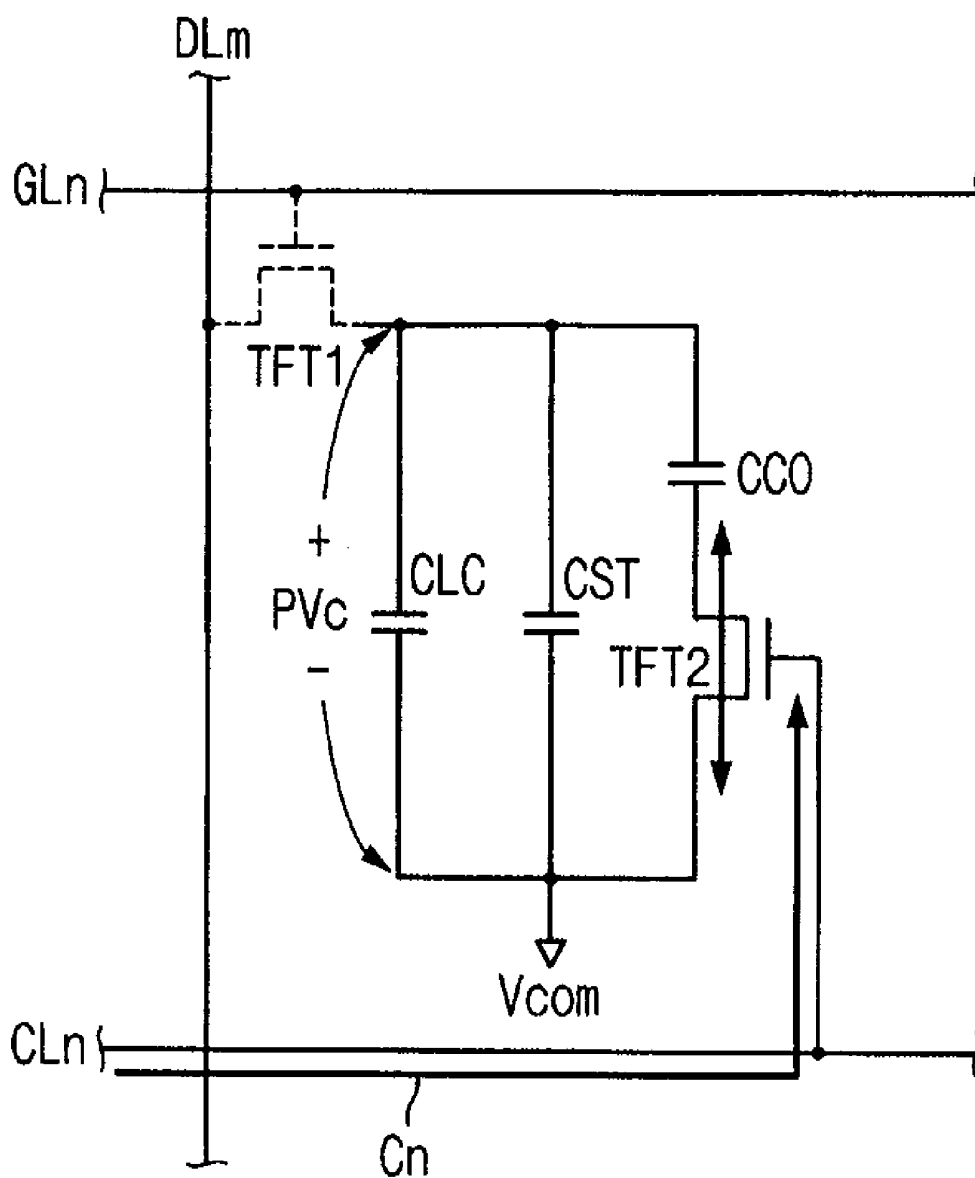


FIG. 5

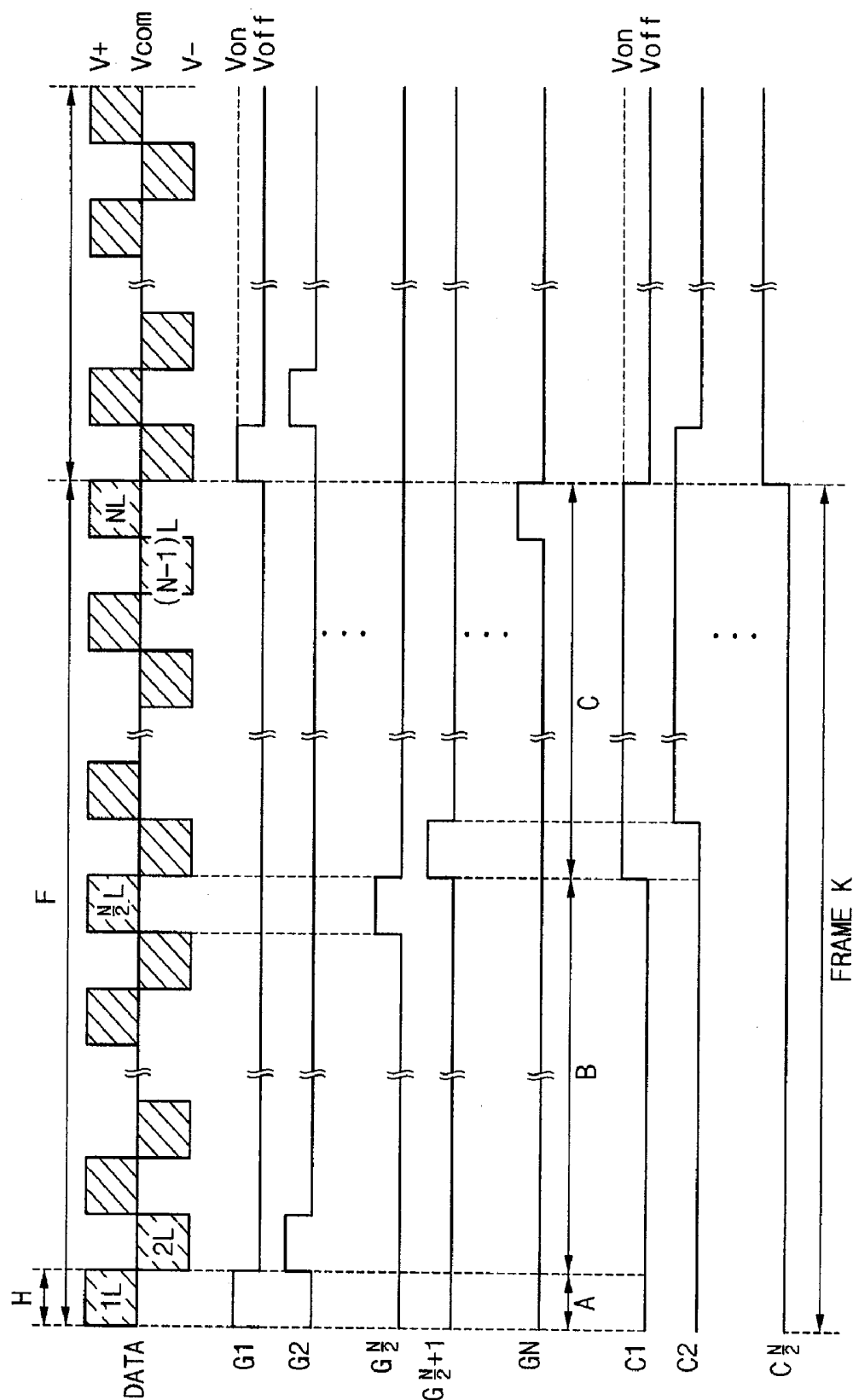


FIG. 6A

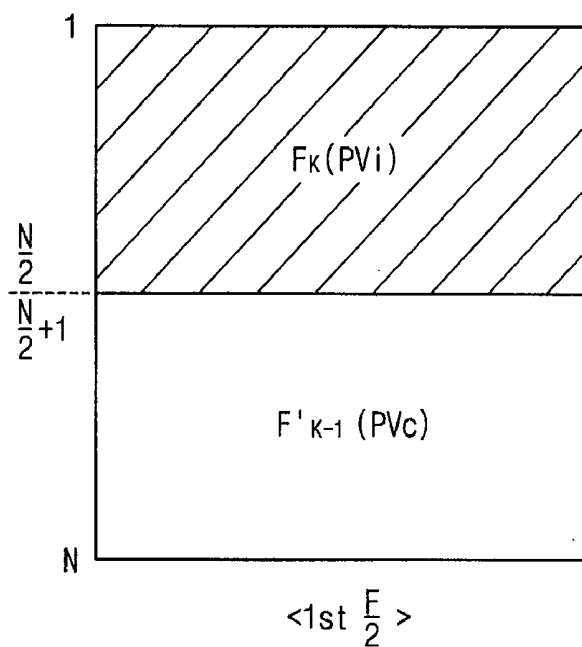
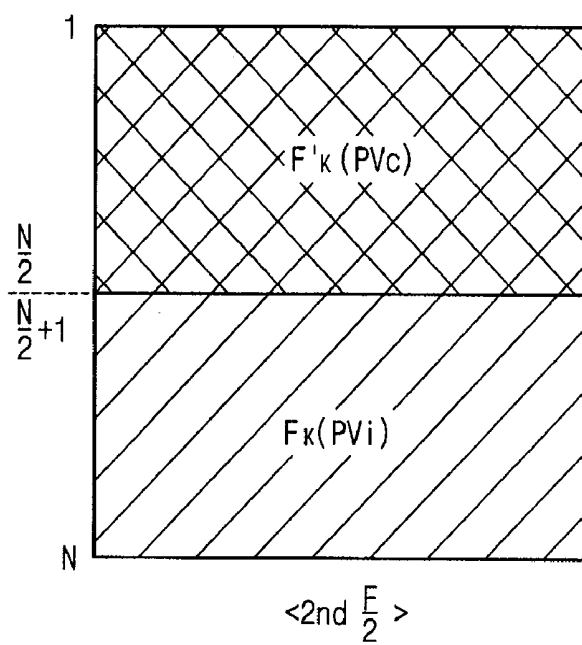


FIG. 6B



DISPLAY PANEL, DISPLAY DEVICE HAVING THE DISPLAY PANEL AND METHOD OF OPERATING THE DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Korean Patent Application No. 2006-85949 filed on Sep. 7, 2006, the contents of which are herein incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a display panel, a display device having the display panel, and a method of operating the display device. More particularly, the present invention relates to a display panel capable of improving the display quality of a moving image, to a display device having such a display panel, and to a method of operating the display device.

[0004] 2. Description of the Related Art

[0005] Generally, a liquid crystal display (LCD) device includes a display panel (i.e., an LCD panel) and a backlight providing the LCD panel with light. The LCD panel includes an array substrate and an opposite substrate facing each other, and a liquid crystal layer interposed between the two substrates. The LCD device displays images in a sample-and-hold manner, as opposed to a cathode ray tube (CRT) device that displays images as an impulse device. Accordingly, motion blur may occur when displaying a high-speed moving image on the LCD. The motion blur occurs because the image of the preceding frame remains on the display for some time while the next frame is being readied. To solve the motion blur problem, the LCD can be overdriven, i.e., driven with higher voltages to improve the liquid crystal's response speed. However, the motion blur may still be present in spite of the improved response speed.

SUMMARY

[0006] Some embodiments of the present invention obviate the above problems to provide a display panel having a pixel structure capable of improving the display quality of a moving image.

[0007] The present invention also provides a display device having the display panel.

[0008] The present invention also provides a method of operating a display device.

[0009] In a display device according to an exemplary embodiment of the present invention and achieve the above-mentioned purpose, a display panel comprises: a first switching element for receiving a gate signal from a gate line and for receiving a data signal from a data line; a liquid crystal capacitor connected to the first switching element, for being charged with an initial pixel voltage corresponding to the data signal; and a voltage lowering part that lowers a voltage of the liquid crystal capacitor to lower a luminance of an image pixel in response to a compensation gate signal provided by a compensation gate line.

[0010] A display device according to an exemplary embodiment of the present invention comprises a display panel comprising: a first switching element including two first input terminals and a first output terminal, the two first input terminals being connected to a gate line and a data line

respectively; a liquid crystal capacitor including a driving electrode and a common electrode, the driving electrode being connected to the first output terminal of the first switching element; a compensation capacitor connected in parallel with the liquid crystal capacitor; a second switching element including two second input terminals and a second output terminal, the two second input terminals being connected to the compensation capacitor and a compensation gate line respectively, and the second output terminal being connected to the common electrode of the liquid crystal capacitor; a source driving block for outputting a data signal to the data line; a gate driving block for outputting a gate signal to the gate line; a compensation gate driving block for outputting a compensation gate signal to the compensation gate line with a delay relative to the gate signal.

[0011] Some embodiments of the present invention provide a method of driving a display device including a display panel comprising a first switching element including two first input terminals connected respectively to a gate line and a data line, a liquid crystal capacitor including a driving electrode connected to a first output terminal of the first switching element, a compensation capacitor connected in parallel with the liquid crystal capacitor, and a second switching element including two second input terminals connected respectively to the compensation capacitor and a compensation gate line and including a second output terminal connected to a common electrode of the liquid crystal capacitor, the method comprising: outputting a data signal to the data line; outputting a gate signal to the gate line; and outputting a compensation gate signal to the compensation gate line with a delay relative to the gate signal.

[0012] In some embodiments, motion blur can be reduced or eliminated via reducing the liquid crystal capacitor's voltage from an initial pixel voltage value to a compensation pixel voltage value in response to a compensation gate signal applied to a compensation gate line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other features and advantages of some embodiments of the present invention will become more apparent in view of detailed description of exemplary embodiments thereof with reference to the accompanying drawings, in which:

[0014] FIG. 1 is a circuit diagram of a display panel according to an exemplary embodiment of the present invention;

[0015] FIG. 2 is a timing diagram showing input signals of the circuit of FIG. 1;

[0016] FIGS. 3A, 3B and 3C are schematic diagrams illustrating the operation shown in the timing diagram of FIG. 2;

[0017] FIG. 4 is a block diagram of a display device according to an exemplary embodiment of the present invention;

[0018] FIG. 5 is a timing diagram illustrating operation of a display device according to an exemplary embodiment of the present invention; and

[0019] FIGS. 6A and 6B are schematic diagrams of images displayed on a display panel operated as in FIG. 5.

DESCRIPTION OF SOME EMBODIMENTS

[0020] Some embodiments of the present invention will now be described with reference to the accompanying

drawings. The invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth in this section; rather, these embodiments are provided to make this disclosure thorough and complete, and to fully convey the scope of the invention to those skilled in the art. It will be understood that when an element is referred to as being “on” or “onto” another element, it may be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present. Like reference numerals refer to similar or identical elements throughout.

[0021] FIG. 1 is a circuit diagram of a display panel according to an exemplary embodiment of the present invention. The display panel includes a plurality of pixel structures. For example, the pixel structure may be defined by a plurality of data lines and a plurality of gate lines arranged transversely to the data lines. The area of each pixel structure ‘P’ is defined by adjacent m-th and m+1-th data lines D_m, D_{m+1} and adjacent n-th and n+1-th gate lines G_n, G_{n+1}. An n-th compensation gate line passes through this area. The n-th compensation gate line CL_n is parallel to the n-th gate line G_n.

[0022] The pixel structure ‘P’ includes a first switching element TFT1, a liquid crystal capacitor CLC, a storage capacitor CST and a voltage lowering part VLP.

[0023] The first switching element TFT1 includes two first input terminals connected to the n-th gate line G_n and the m-th data line D_m respectively, and a first output terminal connected to a first driving electrode of the liquid crystal capacitor CLC.

[0024] The first input terminals of the first switching element TFT1 may be a first gate electrode and a first source electrode. The first output terminal of the first switching element TFT1 includes a first drain electrode. The first gate electrode is connected to the n-th gate line G_n, and the first source electrode is connected to the m-th data line D_m. The first drain electrode is connected to the first driving electrode (“pixel electrode”) of the liquid crystal capacitor CLC, to a driving electrode (“second driving electrode”) of the storage capacitor CST, and to a driving electrode (“third driving electrode”) of the compensation capacitor CCO.

[0025] The liquid crystal capacitor CLC includes the first driving electrode (“pixel electrode”) connected to the first drain electrode, a first common electrode facing the pixel electrode, and a liquid crystal layer (not shown) interposed between the pixel electrode and the first common electrode.

[0026] The storage capacitor CST includes a second driving electrode (hereinafter, “storage electrode”) and a second common electrode facing the storage electrode.

[0027] The compensation capacitor CCO includes the third driving electrode (hereinafter “compensation electrode”) and a third common electrode facing the compensation electrode. The third common electrode is connected to the second switching element TFT2.

[0028] The voltage lowering part VLP includes a compensation capacitor CCO and a second switching element TFT2.

[0029] The second switching element TFT2 includes two second input terminals connected to the compensation capacitor CCO and the n-th compensation gate line CL_n respectively, and a second output terminal connected to the first common electrode of the liquid crystal capacitor CLC. For example, the second input terminals of the second switching element TFT2 may be a second gate electrode and

a second source electrode. The second output terminal of the second switching element TFT2 includes a second drain electrode. The second gate electrode is connected to the n-th compensation gate line CL_n, and the second source electrode is connected to the third common electrode of the compensation capacitor CCO. The second drain electrode is connected to the first common electrode.

[0030] FIG. 2 is a timing diagram showing input signals for the circuit of FIG. 1. FIGS. 3A, 3B and 3C explain the operation according to the timing of FIG. 2.

[0031] Referring to FIGS. 2 and 3A, an initial pixel voltage P_{Vi} charges the liquid crystal capacitor CLC and the storage capacitor CST in a first portion ‘A’ of a frame period 1FRAME (the frame period 1FRAME in FIG. 3A is shown as the period between the rising edges of gate signal G_n). This is done as follows in some embodiments. Gate signal G_n, which is a gate-on voltage V_{on}, is applied to the n-th gate line G_n. As a result, the gate signal G_n is applied to the first gate electrode of the first switching element TFT1 to turn on the first switching element TFT1. When the first switching element TFT1 turns on, a data voltage V_{data} provided on the m-th data line D_m is applied to the liquid crystal capacitor CLC and the storage capacitor CST.

[0032] Compensation gate signal C_n is not applied to the n-th compensation gate line CL_n at this time. Rather, a gate-off voltage V_{off} is applied to the n-th compensation gate line CL_n. Accordingly, the second switching element TFT2 is off, and the compensation capacitor CCO’s electrode electrically connected to the second switching element TFT2 is in a floating state.

[0033] Due to the data voltage V_{data} and a common voltage V_{com} applied to the liquid crystal capacitor CLC and the storage capacitor CST, the two capacitors store an electric charge corresponding to the voltage difference between the data voltage V_{data} and the common voltage V_{com}. This voltage difference is shown as the initial pixel voltage P_{Vi}.

[0034] Referring to FIGS. 2 and 3B, the initial pixel voltage P_{Vi} is maintained on the liquid crystal capacitor CLC and the storage capacitor CST during a second portion ‘B’ of the frame period 1FRAME. More particularly, at the end of the first portion ‘A’ of the frame period 1FRAME, the gate-off voltage V_{off} is applied to the n-th gate line G_n to turn off the first switching element TFT1. Also, the n-th compensation gate line CL_n is kept at the gate-off voltage V_{off} to keep the second switching element TFT2 off. Therefore, the initial pixel voltage P_{Vi} provided in the first portion ‘A’ of the frame period 1FRAME is maintained on the liquid crystal capacitor CLC and the storage capacitor CST.

[0035] Referring to FIGS. 2 and 3C, the voltage on the liquid crystal capacitor CLC and the storage capacitor CST decreases in a third portion ‘C’ of the frame period 1FRAME. In one example, the n-th gate line G_n is kept at the gate-off voltage V_{off} to keep the first switching element TFT1 off. In contrast, the n-th compensation gate line CL_n is driven with the compensation gate signal C_n equal to the gate-on voltage V_{on}. The compensation gate signal C_n is thus applied to the second gate electrode of the second switching element TFT2 through the n-th compensation gate line CL_n to turn on the second switching element TFT2. When the second switching element TFT2 turns on, the compensation capacitor CCO becomes connected in parallel with the liquid crystal capacitor CLC and the storage capacitor CST. Accordingly, some of the charge stored on the

liquid crystal capacitor CLC and the storage capacitor CST flows to the compensation capacitor CCO. Consequently, the voltage on the liquid crystal capacitor CLC and the storage capacitor CST decreases from the initial pixel voltage value PV_i to a compensation pixel voltage value PV_c when the second switching element TFT2 is turned on.

[0036] Therefore, the pixel structure 'P' is charged to the initial pixel voltage PV_i in the first and second portions 'A' and 'B' of the frame period 1FRAME, and to the compensation pixel voltage PV_c proportional to the initial pixel voltage PV_i in the third portion 'C' of the frame period 1FRAME.

[0037] FIG. 4 is a block diagram of a display device according to another exemplary embodiment of the present invention. The display device of FIG. 4 includes a timing control block 110, a voltage generating block 120, a memory block 130, a display panel 140, a source driving block 150, a gate driving block 160 and a compensation gate driving block 170.

[0038] The timing control block 110 generates a driving control signal 111 based on a primary control signal 101 received from an external graphics controller (not shown), and controls the operation of the display device using the driving control signal 111.

[0039] The voltage generating block 120 generates operating voltages for operating the display device. The operating voltages may include voltage V_{com} provided to the display panel 140, a reference gradation voltage V_{ref} provided to the source driving block 150, and gate on/off voltages V_{on} and V_{off} that are provided to the gate driving block 160 and the compensation gate driving block 170.

[0040] The memory block 130 stores and provides data received by the display device. The data are written to, and read out from, the memory block 130 at predetermined equal intervals of time (equal to a frame period for example) under the control of the timing control block 110.

[0041] The display panel 140 includes a plurality of data lines $DL_1, \dots, DL_M$, a plurality of gate lines $GL_1, \dots, GL_N$, and a plurality of compensation gate lines $CL_1, \dots, CL_N$ parallel to the gate lines $GL_1, \dots, GL_N$.

[0042] The display panel 140 includes a plurality of pixel structures 'P'. Each pixel structure 'P' is as in FIG. 1. The pixel structure 'P' includes a first switching element TFT1, a liquid crystal capacitor CLC, a storage capacitor CST, a compensation capacitor CCO and a second switching element TFT2. Further description of the pixel structure 'P' is given above in connection with FIG. 1 and will not be repeated.

[0043] The source driving block 150 converts the data signals read out from the memory block 130 to analog data voltages under the control of the driving control signal 111, and outputs the analog data voltages to the data lines $DL_1, \dots, DL_M$.

[0044] The gate driving block 160 generates a gate signal from the gate on/off voltages V_{on} and V_{off} . The gate driving block 160 sequentially outputs the gate signal to the gate lines $GL_1, \dots, GL_N$.

[0045] The compensation gate driving block 170 operates with a delay relative to the gate driving block 160. The compensation gate driving block 170 generates a compensation gate signal from the gate on/off voltages V_{on} and V_{off} . The compensation gate driving block 170 sequentially outputs the compensation gate signal to the compensation gate lines $CL_1, \dots, CL_N$.

[0046] FIG. 5 is a timing diagram illustrating the operation of the display device of FIG. 4 according to an exemplary embodiment of the present invention.

[0047] Referring to FIGS. 4 and 5, the timing control block 110 receives primary control signal 101 and data 102, generates the driving control signal 111 based on the received primary control signal 101, and stores the received data in the memory block 130 at regular intervals of time each of which is equal to a frame period.

[0048] The timing control block 110 reads out the data for one horizontal line of pixels from the memory block 130 at regular intervals of time each of which is equal to a horizontal period, and outputs the data to the source driving block 150. The source driving block 150 converts the data for one horizontal line to analog data voltages, and outputs the analog data voltages to the data lines $DL_1, \dots, DL_M$ of the display panel 140 during a horizontal period 'H' [DATA].

[0049] The gate driving block 160 generates gate signals $G_1, \dots, G_N$ that have a first pulse width of a predefined length, possibly equal to one horizontal period 'H'. In FIG. 5, the time of generating the signal G_1 is shown as a first portion 'A' of a frame period 'F' which begins at the rising edge of the gate signal G_1 . Generally, each gate signal G_i is generated during a first portion 'A' of a frame period which starts at the rising edge of the gate signal G_i . The gate signals are generated from the gate on/off voltages V_{on} and V_{off} . The gate driving block 160 outputs the gate signals $G_1, \dots, G_N$ to the respective gate lines $GL_1, \dots, GL_N$.

[0050] In synchronization with the gate signals output from the gate driving block 160, the compensation gate driving block 170 outputs a first compensation gate signal $C1$ beginning at the end of a second portion 'B' of the frame period 'F'. The second portion 'B' begins at the end of the first portion 'A'.

[0051] The compensation gate driving block 170 generates compensation gate signals $C_1, \dots, C_N$ from the gate on/off voltages V_{on} and V_{off} , and sequentially outputs the compensation gate signals $C_1, \dots, C_N$ to the compensation gate lines $CL_1, \dots, CL_N$ at the start of the respective first portions 'A' of the respective frame periods 'F' which start at the rising edges of the respective gate signals $G_1, \dots, G_N$. Each of the compensation gate signals $C_1, \dots, C_N$ has a second pulse width equal in length to a third portion 'C' of the respective frame period 'F'. The second pulse width is longer than the first pulse width 'A'. In each third portion 'C', darker-than-normal image is displayed on the corresponding horizontal line to eliminate a motion blur that could be caused by a moving image displayed on the display panel 140. Therefore, the brightness of the moving image displayed in the display panel 140 can be controlled by adjusting the length of the third portions 'C'.

[0052] In the example of FIG. 5, the combined length of the first and second pulse widths 'A' and 'B' is $N/2 \cdot H$. The data driven by the source driving block 150 are shown as "1L" for the first horizontal period 'H' in a frame display (i.e. for the first line of pixels, corresponding to the gate line $G1$), "2L" for the second horizontal period 'H', and so on. Thus, the source driving block 150 outputs line data voltages 1L to the data lines $DL_1, \dots, DL_M$ in the first horizontal period 'H', data voltages 2L in the second horizontal period 'H', and so on. Data voltages NL are output in the N-th horizontal period H, where N is the total number of pixel rows of the display device 140.

[0053] The gate driving block **160** sequentially outputs the gate signals $G_1, \dots, G_N$ for the respective line data voltages $1L, 2L, \dots, NL$ output from the source driving block **150**. In the first $N/2$ horizontal periods 'H', the gate driving block **160** sequentially outputs the gate signals $G_1, \dots, G_{N/2}$ on the respective $N/2$ gate lines. Accordingly, the first to $N/2$ -th horizontal lines of pixels are charged with the initial pixel voltages corresponding to line data voltages $1L, 2L, \dots, (N/2)L$. In particular, the first switching elements TFT1 of the pixel structures are turned on in response to the gate signals, and thus the liquid crystal capacitors CLC are charged with the initial pixel voltages corresponding to the respective line data voltages $1L, 2L, \dots, (N/2)L$.

[0054] When the gate signal for the line $(N/2)+1$ is output from the gate driving block **160**, the compensation gate driving block **170** outputs the first compensation gate signal C1 on the first compensation gate line CL1. Until then, the voltages on the first horizontal line were the initial pixel voltages, which charged the line in response to the first gate signal G1 during the second portion 'B' of the corresponding frame period. When the first compensation gate signal C1 is applied to the first compensation gate line CL1, the voltages on the first horizontal line decrease from the initial pixel voltages to the compensation pixel voltages in response to the first compensation gate signal C1.

[0055] The voltages on the first horizontal line are maintained at the compensation pixel voltage levels during the third portion 'C' of the frame period corresponding to the first horizontal line. The length of each time interval 'C' (each third portion of the frame period corresponding to a line) is equal to the second pulse width, which is the pulse width of the first compensation gate signal C1.

[0056] If the second pulse width 'C' is lengthened, the compensation pixel voltage is maintained longer, so the brightness of the image on the display panel **140** decreases. To the contrary, when the second pulse width 'C' is shortened, the compensation pixel voltage is maintained for a shorter time, so the brightness of the image on the display panel **140** increases. Therefore, the brightness can be controlled by adjusting the second pulse width 'C'.

[0057] As shown in FIG. 5, the compensation gate driving block **170** sequentially outputs the first to the $N/2$ -th compensation gate signals $C_1, \dots, C_{N/2}$ in synchronization with the $(N/2)+1$ -st to the N -th gate signals $G_{(N/2)+1}, \dots, G_N$ that are sequentially output from the gate driving block **160**. Thus, the initial pixel voltages charging the first to $N/2$ -th horizontal lines are each maintained for a time 'B' which is the length of one second portion 'B' of a frame period, and then the initial pixel voltages decrease line after line to the compensation pixel voltages in response to the first to $N/2$ -th compensation gate signals $C_1, \dots, C_{N/2}$. The compensation pixel voltages are maintained for each line for a time equal to the second pulse width 'C'.

[0058] Thus, the compensation capacitor CCO reduces the initial pixel voltage charging the respective liquid crystal capacitor CLC to the compensation pixel voltage during the third portion 'C' of a relevant frame period, i.e. when the corresponding second switching element TFT2 of the pixel structure is turned on by the respective compensation gate signal.

[0059] FIGS. 6A and 6B are schematic diagrams of images displayed on a display panel operated as in FIG. 5.

[0060] Referring to FIGS. 5 and 6A, during the first half "1st F/2" of frame period "FRAME K" starting on the rising

edge of the gate signal G1 for a frame K, the first $N/2$ -th horizontal lines $1, \dots, N/2$ of the display panel **140** are charged to the initial pixel voltages PV_i corresponding to the K-th frame's data. Accordingly, the upper half of the display panel **140** displays the K-th frame's normal image F_K . At this time, the bottom $N/2$ horizontal lines $(N/2)+1, \dots, N$ are still charged with the compensation pixel voltages PV_c corresponding to the data of frame (K-1). Accordingly, the lower half of the display panel **140** displays the compensation image F'_{K-1} of frame (K-1).

[0061] Referring to FIGS. 5 and 6B, during the second half "2nd F/2" of the K-th frame period "FRAME K", the compensation gate driving block **170** operates to reduce the voltages on the first $N/2$ horizontal lines $1, \dots, N/2$ from the initial pixel voltage values PV_i to the compensation pixel voltages PV_c. Accordingly, the upper half of the display panel **140** displays the compensation image F'_K for the K-th frame.

[0062] On the other hand, the last $N/2$ horizontal lines $(N/2)+1, \dots, N$ are charged to the initial pixel voltages PV_i corresponding to the K-th frame's data. Accordingly, the lower half of the display panel **140** displays the normal image F_K for the K-th frame.

[0063] The brightness of the compensation image F'_K is lower than that of the normal image F_K . If the compensation image F'_K is displayed longer, the brightness of the image displayed on the display panel **140** is lower. Accordingly, the brightness of the image displayed on the display panel **140** may be controlled by adjusting the length of the period when the compensation image F'_K is displayed.

[0064] The ratio of the period when the normal image F_K is displayed to the period when the compensation image F'_K is displayed is 1:1 in some embodiments, and lower and higher ratios can also be used.

[0065] As described above, in some embodiments of the present invention, a pixel structure includes a compensation gate line and a switching element that is to be turned on by a compensation gate signal applied to the compensation gate line, so that an initial pixel voltage charging the pixel structure is lowered to a compensation pixel voltage to eliminate a motion blur.

[0066] Thus, a slight modification of the conventional pixel structure (i.e. addition of the compensation line) makes it possible to easily reduce or eliminate the motion blur of a moving image. Some embodiments of the present invention achieve motion blur improvement at lower frequencies than prior art. For example, in some embodiments of the present invention, a 60 Hz (Hertz) operation provides motion blur compensation comparable to the motion blur compensation achieved at 120 Hz and higher frequencies in prior art.

[0067] Although exemplary embodiments of the present invention have been described, it is understood that the present invention should not be limited to these exemplary embodiments but various changes and modifications can be made by one of ordinary skill in the art within the spirit and scope of the present invention. The invention is defined by the appended claims.

What is claimed is:

1. A display panel comprising:

a first switching element for receiving a gate signal from a gate line and for receiving a data signal from a data line;

- a liquid crystal capacitor connected to the first switching element, for being charged with an initial pixel voltage corresponding to the data signal; and
- a voltage lowering part that lowers a voltage of the liquid crystal capacitor to lower a luminance of an image pixel in response to a compensation gate signal provided by a compensation gate line.
2. The display panel of claim 1, wherein the image luminance lowering part comprises:
- a second switching element responsive to the compensation gate signal; and
 - a compensation capacitor connected to the second switching element, for reducing the liquid crystal capacitor's voltage when the second switching element is turned on.
3. The display panel of claim 2, wherein the first switching element comprises:
- a first gate electrode electrically connected to the gate line;
 - a first source electrode electrically connected to the data line; and
 - a first drain electrode electrically connected to driving electrodes of the liquid crystal capacitor and the compensation capacitor.
4. The display panel of claim 3, wherein the second switching element comprises:
- a second gate electrode electrically connected to the compensation gate line;
 - a second source electrode electrically connected to a common electrode of the compensation capacitor; and
 - a second drain electrode electrically connected to a common electrode of the liquid crystal capacitor.
5. The display panel of claim 4, wherein the second drain electrode of the second switching element is connected with a common electrode of a storage capacitor whose driving electrode is connected to the driving electrode of the liquid crystal capacitor.
6. A display device comprising:
- a display panel comprising:
 - a first switching element including two first input terminals and a first output terminal, the two first input terminals being connected to a gate line and a data line respectively;
 - a liquid crystal capacitor including a driving electrode and a common electrode, the driving electrode being connected to the first output terminal of the first switching element; and
 - a voltage lowering part that lowers a voltage of the liquid crystal capacitor to lower a luminance of an image pixel in response to a compensation gate signal provided by a compensation gate line;
 - a source driving block for outputting a data signal to the data line;
 - a gate driving block for outputting a gate signal to the gate line; and
 - a compensation gate driving block for outputting a compensation gate signal to the compensation gate line with a delay relative to the gate signal.
7. The display device of claim 6, wherein the voltage lowering part comprises:
- a compensation capacitor connected in parallel with the liquid crystal capacitor; and
 - a second switching element including two second input terminals and a second output terminal, the two second input terminals being connected to the compensation gate line and a common electrode of the liquid crystal capacitor respectively, and the second output terminal being connected to the common electrode of the liquid crystal capacitor.
8. The display device of claim 7, wherein the gate driving block outputs the gate signal to the gate line during a first portion of a frame period.
9. The display device of claim 8, wherein the first portion of the frame period is a horizontal period (1H).
10. The display device of claim 8, wherein the first switching element charges the liquid crystal capacitor with an initial pixel voltage during the first portion of the frame period in response to the gate signal.
11. The display device of claim 8, wherein the display panel further comprises a storage capacitor connected to one of the first output terminals of the first switching element, wherein the storage capacitor is connected in parallel with the liquid crystal capacitor.
12. The display device of claim 11, wherein the liquid crystal capacitor is charged with an initial voltage during the first portion of the frame period, and the storage capacitor maintains the initial voltage during a second portion of the frame period, the second portion of the frame period corresponding to a period between the gate signal and the compensation gate signal.
13. The display device of claim 12, wherein the compensation gate driving block outputs the compensation gate signal to the compensation gate line during a third portion of the frame period.
14. The display device of claim 13, wherein the liquid crystal capacitor is charged with an initial pixel voltage during the first portion of the frame period, and the compensation capacitor lowers the liquid crystal capacitor's voltage from the initial pixel voltage to a compensation pixel voltage during the third portion of the frame period when the second switching element is turned on in response to the compensation gate signal.
15. A method of driving a display device including a display panel comprising a first switching element including two first input terminals connected respectively to a gate line and a data line, a liquid crystal capacitor including a driving electrode connected to a first output terminal of the first switching element, a compensation capacitor connected in parallel with the liquid crystal capacitor, and a second switching element including two second input terminals connected respectively to the compensation capacitor and a compensation gate line and including a second output terminal connected to a common electrode of the liquid crystal capacitor, the method comprising:
- outputting a data signal to the data line;
 - outputting a gate signal to the gate line; and
 - outputting a compensation gate signal to the compensation gate line with a delay relative to the gate signal.
16. The method of claim 15, wherein the gate signal is output during a first portion of a frame period.
17. The method of claim 16, wherein the first portion of the frame period is a horizontal period (1H).
18. The method of claim 16, wherein outputting the gate signal includes:
- turning on the first switching element in response to the gate signal; and
 - charging the liquid crystal capacitor with an initial pixel voltage corresponding to the data signal when the first switching element is turned on.

19. The method of claim **18**, further comprising maintaining the initial pixel voltage for a predefined length of time after ceasing to output the gate signal.

20. The method of claim **19**, wherein the compensation gate signal is output for a predefined length of time during the frame period.

21. The method of claim **20**, wherein outputting the compensation gate signal includes:

turning on the second switching element in response to the compensation gate signal; and
reducing the initial pixel voltage to a compensation pixel voltage using the compensation capacitor when the second switching element is turned on.

* * * * *

专利名称(译)	显示面板，具有显示面板的显示设备和操作显示设备的方法		
公开(公告)号	US20080062103A1	公开(公告)日	2008-03-13
申请号	US11/850419	申请日	2007-09-05
[标]申请(专利权)人(译)	你BONG HYUN		
申请(专利权)人(译)	YOU BONG-HYUN		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	YOU BONG HYUN		
发明人	YOU, BONG-HYUN		
IPC分类号	G09G3/36		
CPC分类号	G09G3/2018 G09G2320/0261 G09G2300/0876 G09G3/3659		
优先权	1020060085949 2006-09-07 KR		
其他公开文献	US8009133		
外部链接	Espacenet USPTO		

摘要(译)

显示面板包括第一开关元件，液晶电容器和第二开关元件。第一开关元件接收栅极信号和数据信号。液晶电容器连接到第一开关元件，并且用对应于数据信号的初始像素电压充电。第二开关元件响应于从补偿栅极线施加的补偿栅极信号而操作。补偿电容器连接到第二开关元件，以在第二开关元件导通时将液晶电容器的电压降低到低于初始像素电压的值。因此，可以减少或消除运动模糊。

