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(54) LIQUID CRYSTAL DISPLAY AND THIN FILM TRANSISTOR ARRAY PANEL THEREFOR

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(57) **ABSTRACT**

A liquid crystal display includes a first substrate including a first electrode and a second electrode formed thereon, a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, and at least one cutout formed in the third electrode, wherein the at least one cutout is aligned with a space between the first and second electrodes.

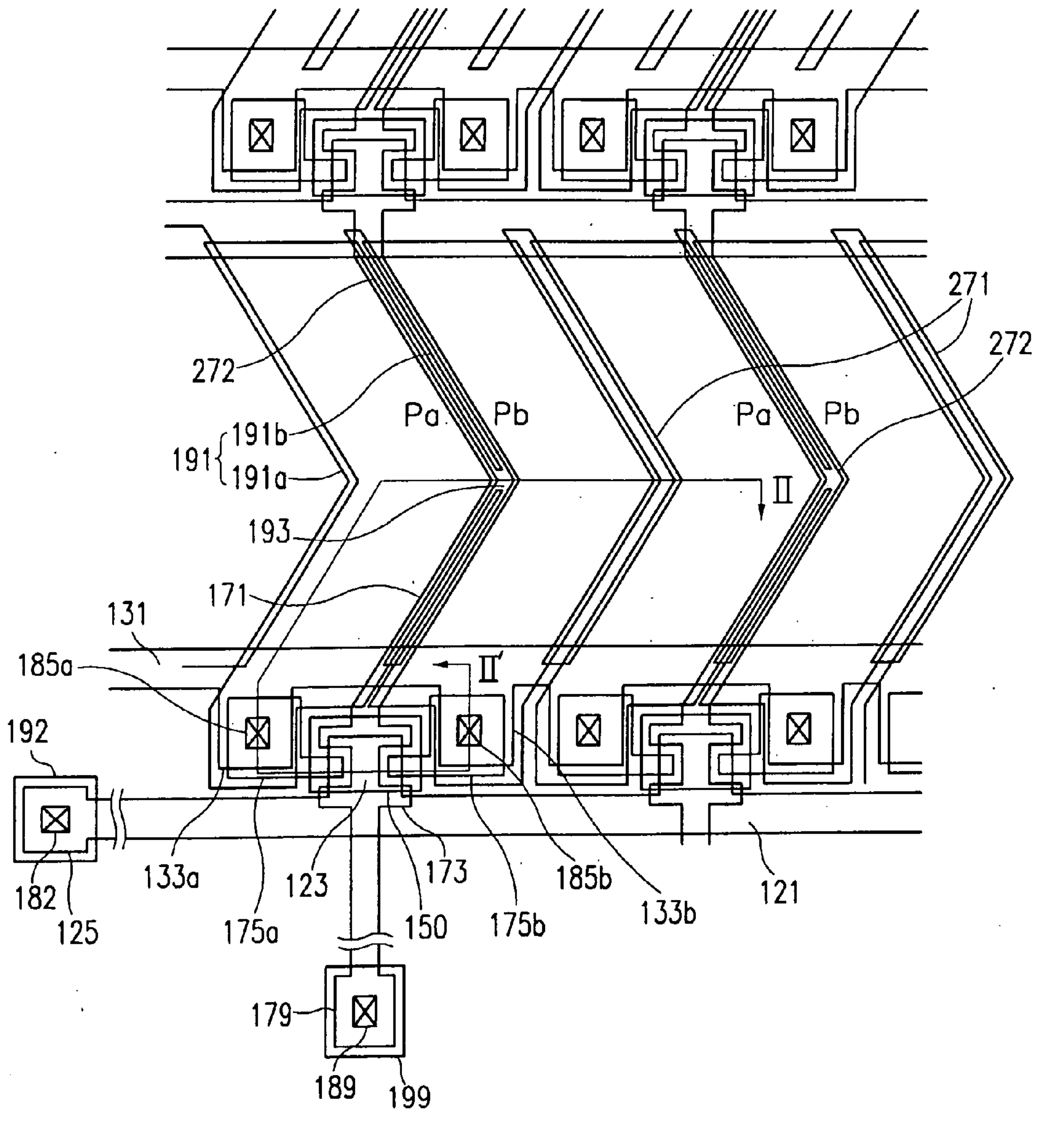


FIG.1

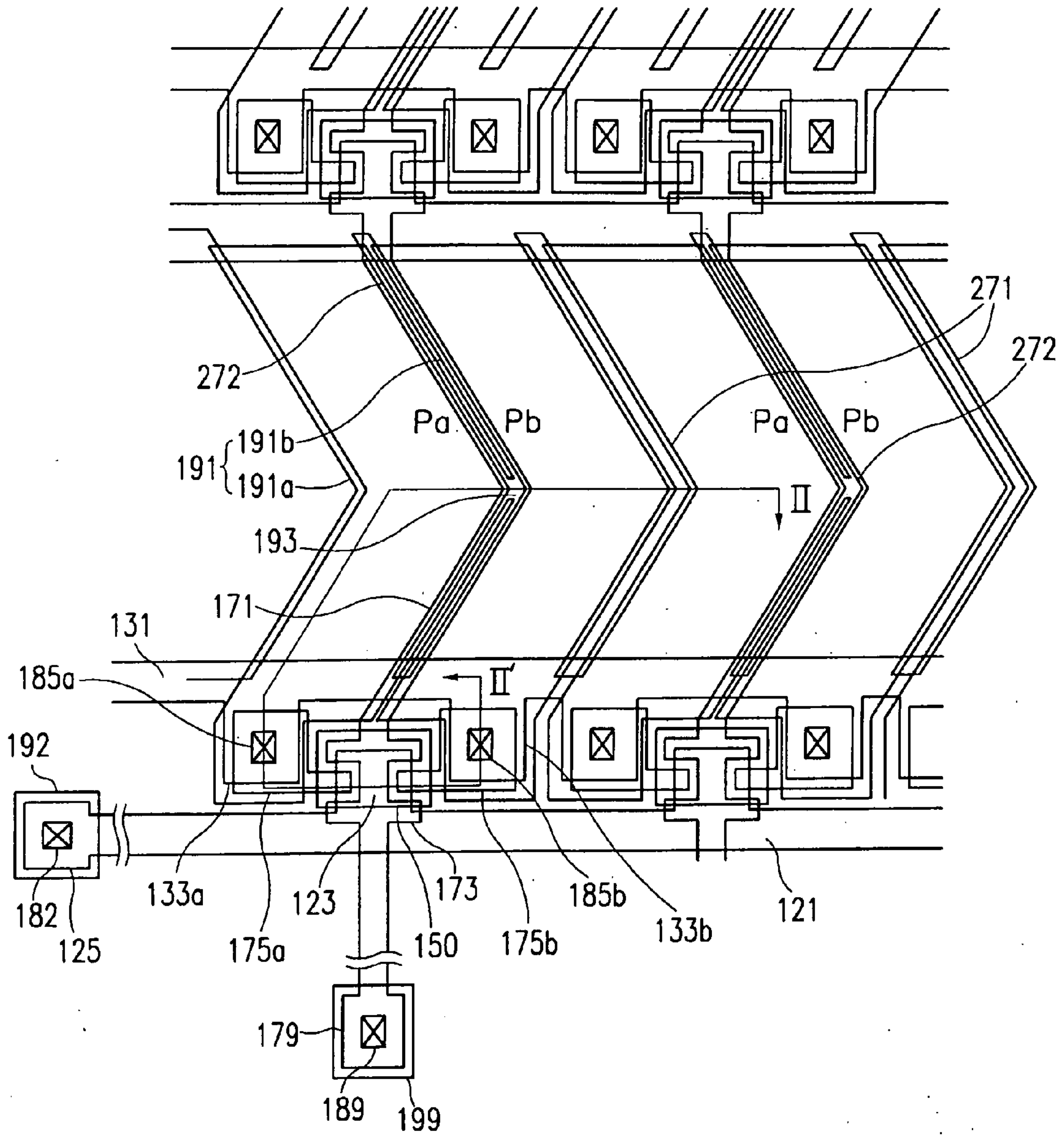
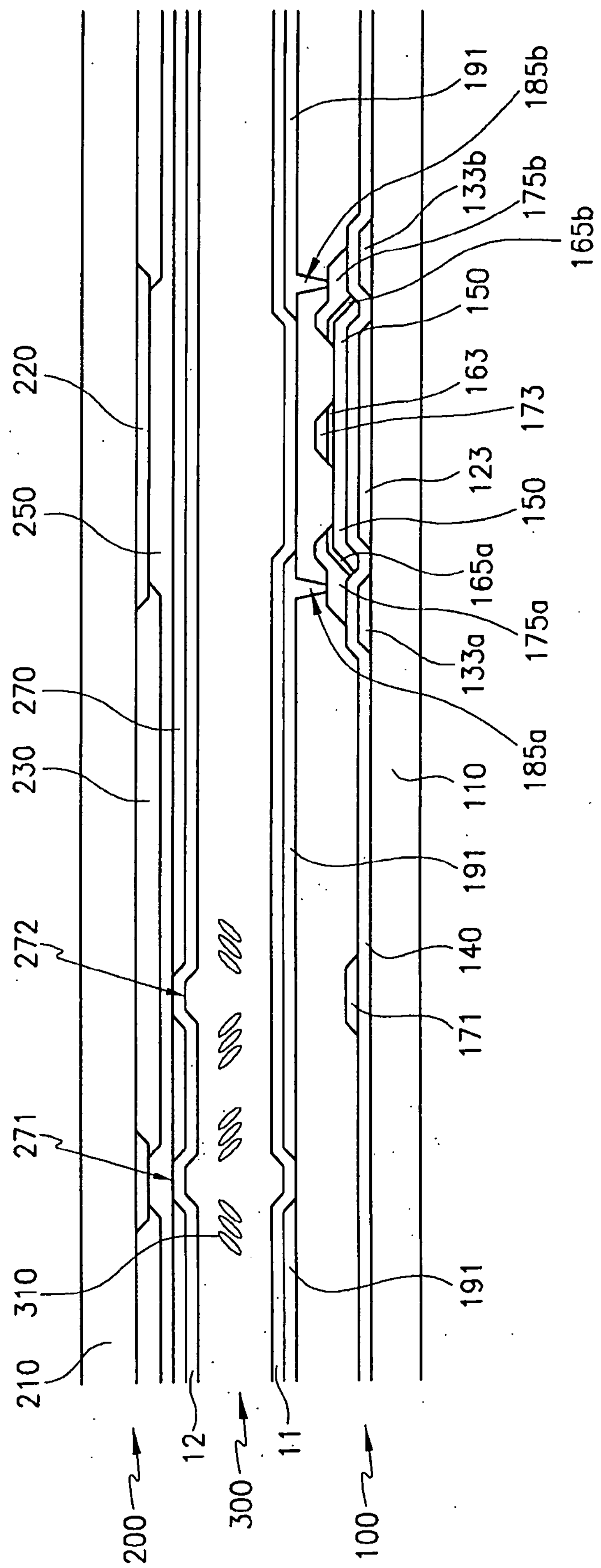

272
191b
191
191a
193
171
131
185a
192
182
125
133a
175a
123
150
173
175b
185b
133b
121
179
189
199
Pa
Pb
271
272
Pa
Pb
II
II'

FIG.2



210
310
271
272
230
270
250
220
200
12
300
11
100
191
140
171
191
110
185a
133a
175a
165a
150
123
173
163
150
165b
175b
133b
185b
191

FIG.3

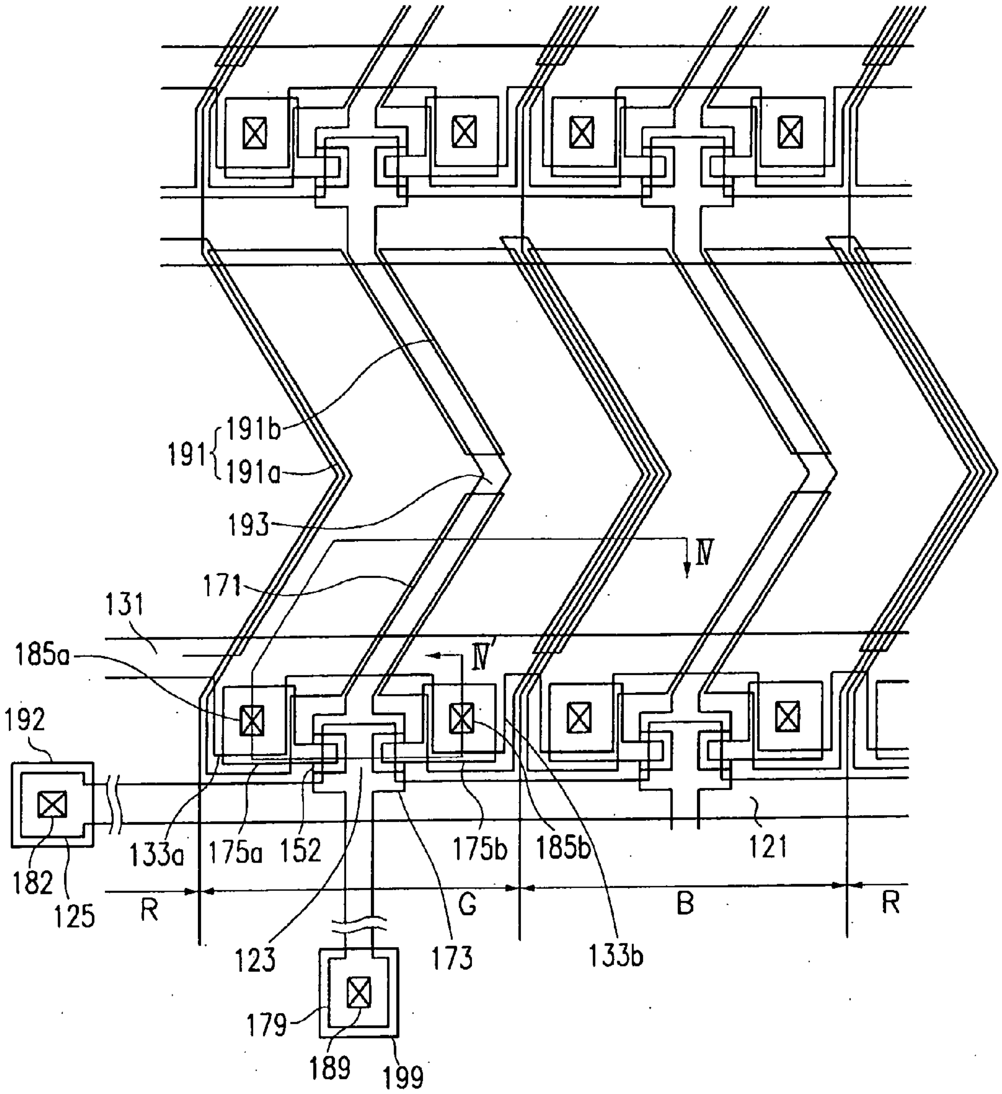
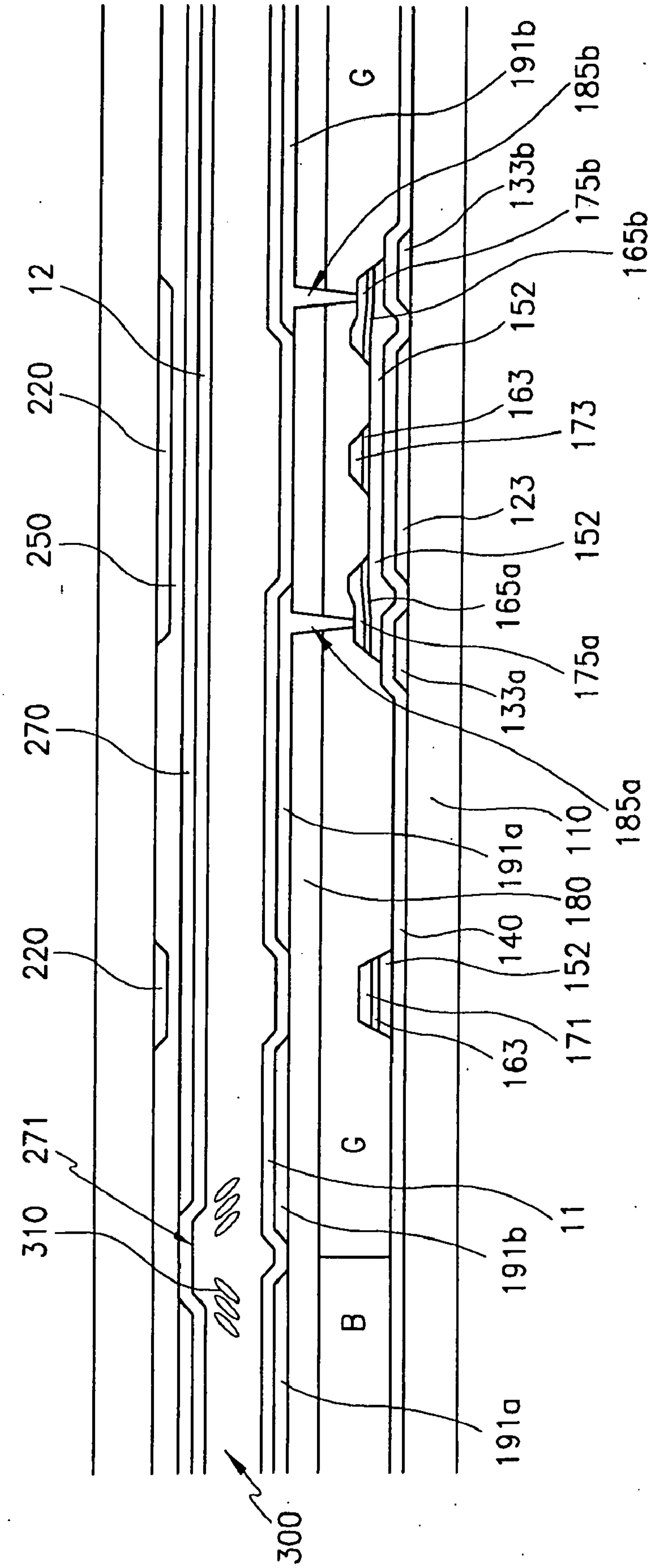

191
191b
191a
193
171
131
IV
IV'
185a
192
182
125
133a
175a
152
175b
185b
121
R
G
B
R
123
173
133b
179
189
199

FIG. 4


12
220
250
270
220
310
271
300
G
191b
185b
133b
175b
165b
152
163
173
123
152
165a
175a
133a
185a
110
191a
180
140
152
171
163
G
11
191b
B
191a

LIQUID CRYSTAL DISPLAY AND THIN FILM TRANSISTOR ARRAY PANEL THEREFOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Divisional of U.S. application Ser. No. 10/780,335, filed on Feb. 17, 2004, the disclosure of which is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Technical Field

[0003] The present disclosure relates to a liquid crystal display and a thin film transistor array panel therefor.

[0004] 2. Discussion of the Related Art

[0005] A liquid crystal display (LCD) is one of the most widely used flat panel displays. LCDs are used in notebook or laptop computers, desktop computer monitors and televisions. LCDs are lightweight and occupy less space than conventional cathode ray tube (CRT) displays.

[0006] The general structure of an LCD consists of a liquid crystal (LC) layer that is positioned between pair of panels including field generating electrodes and polarizers. The LC layer is subject to an electric field generated by the electrodes and variations in the field strength change the molecular orientation of the LC layer. For example, upon application of an electric field, the molecules of the LC layer change their orientation and polarize light passing through the LC layer. Appropriately positioned polarized filters block the polarized light, creating dark areas that can represent desired images.

[0007] One measure of LCD quality is viewing angle (i.e., the available area when viewing the LCD in which minimum contrast can be seen). Various techniques for enlarging the viewing angle have been suggested, including a technique utilizing a vertically aligned LC layer and providing cutouts or protrusions at pixel electrodes. However, cutouts and the protrusions reduce the aperture ratio (i.e., ratio between the actual size of a sub-pixel and the area of the sub-pixel that can transmit light). To increase aperture ratio, it has been suggested that the size of the pixel electrodes be maximized. However, maximization of the size of the pixel electrodes results in a close distance between the pixel electrodes, causing strong lateral electric fields between the pixel electrodes. The strong electric fields cause unwanted altering of the orientation of the LC molecules, yielding textures and light leakage and deteriorating display characteristics.

[0008] Another issue arises with the photo etching processes performed to form various patterns on the panels of the LCD. When a backplane for LCDs is too large to use an exposure mask, the entire exposure (e.g., irradiation of a resist) is accomplished by repeating a divisional exposure. This is called a step-and-repeat process and a single exposure area or field is called a shot. One characteristic associated with the step-and-repeat process is that the shots may be misaligned due to transition, rotation, distortion, etc., which are generated during light exposure. Accordingly, parasitic capacitances generated between wires and pixel electrodes differ depending on the shots in which they are located. These capacitance differences cause a brightness difference between the shots, which is recognized at the pixels located at a boundary between the shots. As a result, a stitch defect is generated on the screen of the LCD due to the brightness discontinuity between the shots.

[0009] Therefore, there exists a need in the art for an LCD panel and cutout configuration that allows for increased viewing angle without causing an unwanted reduction in aperture ratio and distortion of the orientation of the LC layer. There also exists a need for an LCD panel configuration that minimizes or eliminates parasitic capacitance differences between shots and corresponding brightness discontinuity.

SUMMARY OF THE INVENTION

[0010] A liquid crystal display, in accordance with an embodiment of the present invention, includes a first substrate including a first electrode and a second electrode formed thereon, a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, and at least one cutout formed in the third electrode, wherein the at least one cutout is aligned with a space between the first and second electrodes.

[0011] The first electrode may be a first pixel electrode, the second electrode may be a second pixel electrode and the third electrode may be a common electrode. The gap may include a liquid crystal layer configured for housing liquid crystal molecules, and the at least one cutout may include a first edge aligned parallel to an edge of the first electrode and a second edge aligned parallel to an edge of the second electrode. A component of an electric field generated between the third and the first and second electrodes for causing a change in tilt direction of the liquid crystal molecules may align at least one of perpendicular to the first edge of the cutout, perpendicular to the second edge of the cutout, perpendicular to the edge of the first electrode and perpendicular to the edge of the second electrode. The at least one cutout may have a width within the range of about 9 to about 12 microns.

[0012] The liquid crystal display may further include a plurality of data lines for transmitting data voltages formed on the first substrate, and at least one other cutout formed in the third electrode, wherein the at least one other cutout is aligned with at least one data line of the plurality of data lines.

[0013] An electric field, due to a voltage difference between the first electrode and the second electrode, may be generated between the first and second electrodes, and a direction of the electric field may be at least one of perpendicular to the first edge of the at least one cutout and perpendicular to the second edge of the at least one cutout. A voltage having an opposite polarity with respect to a voltage applied to the third electrode may be applied to one of the first electrode and the second electrode

[0014] The liquid crystal display may further include at least one gate electrode formed on the first substrate, and at least two transistors formed on the first substrate and symmetrically disposed about the at least one gate electrode for creating a non-varying parasitic capacitance between the at least one gate electrode and at least two drain electrodes of the at least two transistors across a plurality of shots of the first substrate. A pair of the symmetrically disposed transistors may include the at least one gate electrode, at least one source electrode, the at least two drain electrodes and at least one semiconductor island. The liquid crystal display may further include a plurality of data lines for transmitting data voltages formed on the first substrate, wherein the first and second electrodes are symmetrically disposed about at least one data line of the plurality of data lines for creating a non-varying parasitic capacitance between the first and second electrodes and the at least one data line across a plurality of shots of the first substrate.

[0015] The liquid crystal display may further include a plurality of gate lines for transmitting gate signals formed on the first substrate, a plurality of storage electrode lines for transmitting at least one predetermined voltage formed on the first substrate, and a plurality of data lines for transmitting data voltages formed on the first substrate. At least one of the first electrode and the second electrode may be positioned in an area enclosed by the plurality of gate lines, the plurality of storage electrode lines and the plurality of data lines, and may overlap at least one data line of the plurality of data lines. The plurality of data lines may intersect the plurality of gate lines and the plurality of storage lines. Each data line of the plurality of data lines may be curved and include a plurality of pairs of oblique portions connected to each other to form a chevron. Opposite ends of the oblique portions may be connected to respective longitudinal portions that cross over gate electrodes. A length of each pair of the oblique portions may be about one to about nine times a length of a longitudinal portion. At least one of the plurality of gate lines, the plurality of storage electrode lines and the plurality of data lines may include tapered sides, wherein an incline angle of the tapered sides with respect to a horizontal surface of the first substrate is within the range of about 30 to about 80 degrees. At least one of the plurality of gate lines, the plurality of storage electrode lines and the plurality of data lines includes a lower film and an upper film, wherein the upper film includes one of aluminum and an aluminum alloy and the lower film includes one of chromium, molybdenum and a molybdenum alloy.

[0016] The liquid crystal display may further include a plurality of storage electrodes formed on the first substrate, and a plurality of drain electrodes formed on the first substrate, wherein at least one pair of drain electrodes of the plurality of drain electrodes overlaps at least one pair of storage electrodes of the plurality of storage electrodes. The first electrode and the second electrode may be respectively connected to a first drain electrode and a second drain electrode of the plurality of drain electrodes, and the first electrode and the second electrode may receive data voltages from the first drain electrode and the second drain electrode, respectively. The liquid crystal display may also include a plurality of color filters formed on one of the first substrate and the second substrate, wherein two adjacent color filters of the plurality of color filters overlap each other.

[0017] The liquid crystal display may further include a gate insulating layer formed on the first substrate, a plurality of semiconductor islands formed on the gate insulating layer, a plurality of ohmic contacts formed on the semiconductor islands, a plurality of data lines for transmitting data voltages formed on at least one of the ohmic contacts and the gate insulating layer, and a plurality of drain electrodes formed on the ohmic contacts, wherein the semiconductor islands have essentially the same planar shapes as at least one of the data lines, the drain electrodes and the ohmic contacts. The data lines, the drain electrodes, the semiconductor islands and the ohmic contacts may be simultaneously formed using one photolithography process.

[0018] Another liquid crystal display, in accordance with an embodiment of the present invention, includes a first substrate including a first electrode and a second electrode formed thereon, a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, at least one gate electrode formed on the first substrate, and at least two transistors formed on the first substrate and symmetrically disposed about the at least one gate electrode.

[0019] The first electrode may be a first pixel electrode, the second electrode may be a second pixel electrode and the third electrode may be a common electrode. A pair of the symmetrically disposed transistors may include the at least one gate electrode, at least one source electrode, at least two drain electrodes and at least one semiconductor island. A plurality of data lines for transmitting data voltages may be formed on the first substrate, wherein the first and second electrodes are symmetrically disposed about at least one data line of the plurality of data lines.

[0020] At least one cutout may be formed in the third electrode, wherein the at least one cutout includes a first edge aligned parallel to an edge of the first electrode and a second edge aligned parallel to an edge of the second electrode. The at least one cutout may be aligned with a space between the first and second electrodes. A component of an electric field generated between the third and the first and second electrodes for causing a change in tilt direction of liquid crystal molecules may align at least one of perpendicular to the first edge of the cutout, perpendicular to the second edge of the cutout, perpendicular to the edge of the first electrode and perpendicular to the edge of the second electrode. The at least one cutout may have width within the range of about 9 to about 12 microns. An electric field may be generated between the first and second electrodes, and a direction of the electric field may be at least one of perpendicular to the first edge of the at least one cutout and perpendicular to the second edge of the at least one cutout.

[0021] The liquid crystal display may further include a plurality of data lines for transmitting data voltages formed on the first substrate, and at least one cutout formed in the third electrode, wherein the at least one cutout is aligned with the at least one data line. A voltage having an opposite polarity with respect to a voltage applied to the third electrode may be applied to one of the first electrode and the second electrode. An electric field, due to a voltage difference between the first electrode and the second electrode, may be generated between the first electrode and the second electrode.

[0022] Another liquid crystal display, in accordance with an embodiment of the present invention, includes a first substrate including a first pixel electrode and a second pixel electrode formed thereon. And a second substrate including a common electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, and a voltage having an opposite polarity with respect to a voltage applied to the common electrode is applied to one of the first pixel electrode and the second pixel electrode to generate an electric field between the first pixel electrode and the second pixel electrode having a direction which coincides with a component of an electric field generated between the common electrode and the first and second pixel electrodes.

[0023] Another liquid crystal display, in accordance with an embodiment of the present invention, includes a first substrate including a first electrode and a second electrode formed thereon, a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, and at least one cutout formed in the third electrode, wherein the at least one cutout includes a first edge aligned parallel to an edge of the first electrode and a second edge aligned parallel to an edge of the second electrode.

[0024] Another liquid crystal display, in accordance with an embodiment of the present invention, includes a first substrate including a first electrode and a second electrode formed thereon, a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, and a plurality of data lines for transmitting data voltages formed on the first substrate, wherein the first and second electrodes are symmetrically disposed about at least one data line of the plurality of data lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Preferred embodiments of the invention can be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings in which:

[0026] **FIG. 1** is a layout view of an LCD according to an embodiment of the present invention;

[0027] **FIG. 2** is a sectional view of the LCD shown in **FIG. 1** taken along the line II-II';

[0028] **FIG. 3** is a layout view of an LCD according to another embodiment of the present invention; and

[0029] **FIG. 4** is a sectional view of the LCD shown in **FIG. 3** taken along the line IV-VI'.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0030] Preferred embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein.

[0031] **FIG. 1** is a layout view of an LCD according to an embodiment of the present invention, and **FIG. 2** is a sectional view of the LCD shown in **FIG. 1** taken along the line II-II'.

[0032] As shown in **FIG. 2**, an LCD according to an embodiment of the present invention includes a TFT array panel **100**, a common electrode panel **200**, and an LC layer **300** interposed between the panels **100** and **200** and containing a plurality of LC molecules **310** aligned in the vertical direction with respect to the surfaces of the panels **100** and **200**.

[0033] Referring to **FIGS. 1 and 2**, a plurality of gate lines **121** and a plurality of storage electrode lines **131** are formed on an insulating substrate **110**. The gate lines **121** are separated from each other and extend substantially in a transverse direction. The gate lines **121** transmit gate signals and a plurality of projections of each gate line **121** form a plurality of gate electrodes **123**.

[0034] Each storage electrode line **131** extends substantially in the transverse direction and includes a plurality of projections forming a plurality of pairs of storage electrodes **133*a*** and **133*b***. The storage electrodes **133*a*** and **133*b*** have a shape of rectangle (or diamond) and are located close to the gate electrodes **123**. The storage electrode lines **131** are supplied with a predetermined voltage such as a common voltage, which is applied to a common electrode **270** on the common electrode panel **200** of the LCD.

[0035] The gate lines **121** and the storage electrode lines **131** may have a multi-layered structure including two films having different physical characteristics, a lower film (not shown) and an upper film (not shown). The upper film is preferably made of a metal having a low resistivity, for example, an aluminum (Al) containing metal such as Al or an Al alloy, for reducing signal delay or voltage drop in the gate lines **121** and the storage electrode lines **131**. The lower film is preferably made of a material such as chromium (Cr), molybdenum (Mo) or a Mo alloy, which has good contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). A preferred combination of the lower film material and the upper film material is Cr and an aluminum-neodymium (Al—Nd) alloy, respectively.

[0036] The sides of the gate lines **121** and the storage electrode lines **131** are tapered, and the angle of incline of the sides with respect to a surface of the substrate **110** ranges from about 30 to about 80 degrees.

[0037] A gate insulating layer **140** preferably made of silicon nitride (SiNx) is formed on the gate lines **121** and the storage electrode lines **131**.

[0038] A plurality of semiconductor islands **150** preferably made of hydrogenated amorphous silicon (a-Si) or polysilicon (p-Si) are formed on the gate insulating layer **140**. Each semiconductor island **150** is located opposite a gate electrode **123**.

[0039] A plurality of ohmic contact islands **163**, **165*a*** and **165*b*** preferably made of silicide or n+ hydrogenated a-Si heavily doped with an n-type impurity are formed on the semiconductor islands **150**.

[0040] The sides of the semiconductor islands **150** and the ohmic contacts **163**, **165*a*** and **165*b*** are tapered, and the incline angles thereof with respect to the substrate **110** are preferably in a range between about 30 to about 80 degrees.

[0041] As shown in **FIG. 1**, a plurality of data lines **171** for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines **121** and the storage electrode lines **131**. Each data line **171** is curved repeatedly and includes a plurality of pairs of oblique portions and a plurality of longitudinal portions. A pair of oblique portions are connected to each other to form a chevron and opposite ends of the pair of oblique portions are connected to respective longitudinal portions. The oblique portions of the data lines **171** form an angle of about 45 degrees with the gate lines **121**, and the longitudinal portions cross over the gate electrodes **123**. The length of a pair of oblique portions is about one to about nine times the length of a longitudinal portion, that is, it occupies about 50 to about 90 percent of the total length of the pair of oblique portions plus the longitudinal portion.

[0042] As shown in **FIG. 2**, the plurality of data lines **171** and a plurality of pairs of drain electrodes **175***a* and **175***b* are separated from each other and formed on the ohmic contacts **163**, **165***a* and **165***b* and the gate insulating layer **140**.

[0043] The pair of drain electrodes **175***a* and **175***b* are opposite each other with respect to a longitudinal portion of a data line **171**. Each longitudinal portion of the data lines **171** includes a plurality of projections such that the longitudinal portion including the projections forms a source electrode **173** partly enclosing the drain electrodes **175***a* and **175***b*. The source electrode **173** is formed on the ohmic contact **163**. The drain electrodes **175***a* and **175***b* are formed on the ohmic contacts **165***a* and **165***b*, respectively.

[0044] The ohmic contacts **163**, **165***a* and **165***b* are interposed only between the underlying semiconductor islands **150** and the overlying data lines **171** and the overlying source and drain electrodes **173**, **175***a* and **175***b* and reduce the contact resistance between the underlying and overlying elements. Each drain electrode **175***a* or **175***b* includes an expansion overlapping a storage electrode **133***a* or **133***b*.

[0045] Each set of a gate electrode **123**, a source electrode **173**, a pair of drain electrodes **175***a* and **175***b*, and a semiconductor island **150** form a pair of TFTs. The pair of TFTs includes channels formed in the semiconductor island **150** disposed between the source electrode **173** and the drain electrodes **175***a* and **175***b*, respectively.

[0046] Like the gate lines **121** and the storage electrode lines **131**, the data lines **171** and the drain electrodes **175***a* and **175***b* may also include a lower film (not shown) preferably made of Mo, Mo alloy or Cr and an upper film (not shown) located thereon, preferably made of an Al containing metal. Further, the data lines **171** and the drain electrodes **175***a* and **175***b* also have tapered sides, with incline angles ranging from about 30 to about 80 degrees.

[0047] A passivation layer **180** is formed on the data lines **171**, the drain electrodes **175***a* and **175***b*, and exposed portions of the semiconductor islands **150** which are not covered by the data lines **171** and the drain electrodes **175***a* and **175***b*. The passivation layer **180** is preferably made of a flat photosensitive organic material and low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), or an inorganic material such as silicon nitride and silicon oxide. The passivation layer **180** may have a double-layered structure including a lower inorganic film and an upper organic film.

[0048] The passivation layer **180** has a plurality of contact holes **185***a*, **185***b* and **189** exposing the drain electrodes **175***a* and **175***b* and end portions **179** of the data lines **171**, respectively. The passivation layer **180** and the gate insulating layer **140** have a plurality of contact holes **182** exposing end portions **125** of the gate lines **121**. The contact holes **182**, **185***a*, **185***b* and **189** can have various shapes, such as a polygon or circle. The area of each contact hole **182** or **189** is preferably greater than or equal to 0.5 mm×15 μm and not larger than 2 mm×60 μm. The sidewalls of the contact holes **182**, **185***a*, **185***b* and **189** are inclined with an angle of about 30 to about 85 degrees or have stepwise profiles.

[0049] A plurality of pairs of pixel electrodes **191***a* and **191***b* and a plurality of contact assistants **192** and **199**, which are preferably made of ITO, IZO or Cr, are formed on the passivation layer **180**.

[0050] Each pixel electrode **191***a* or **191***b* is located substantially in an area enclosed by the data lines **171**, the gate lines **121**, and the storage electrode lines **131** and forms a chevron. A pair of pixel electrodes **191***a* and **191***b* are connected to each other through a connection **193** and form a pair of subpixel areas Pa and Pb.

[0051] The pixel electrodes **191***a* and **191***b* are physically and electrically connected to the drain electrodes **175***a* and **175***b* through the contact holes **185***a* and **185***b* such that the pixel electrodes **191***a* and **191***b* receive the data voltages from the drain electrodes **175***a* and **175***b*. The pixel electrodes **191***a* and **191***b* supplied with the data voltages generate electric fields in cooperation with the common electrode **270**, which reorient liquid crystal molecules disposed therebetween.

[0052] A pixel electrode **191***a* or **191***b* and a common electrode form a capacitor called a "liquid crystal capacitor," which stores applied voltages after turn-off of the TFT. An additional capacitor called a "storage capacitor," which is connected in parallel to the liquid crystal capacitor, is provided for enhancing the voltage storing capacity. The storage capacitor is implemented by overlapping the pixel electrodes **191** with the storage electrode lines **131**. The capacitance of a storage capacitor, (i.e., the storage capacitance) is increased by providing the projections at the storage electrode lines **131** forming the storage electrodes **133***a* and **133***b*, elongating the drain electrodes **175***a* and **175***b* connected to the pixel electrodes **191***a* and **191***b*, and providing the expansions at the drain electrodes **175***a* and **175***b* overlapping the storage electrodes **133***a* and **133***b* of the storage electrode lines **131**. These design elements decrease the distance between the terminals and increase the overlapping areas, resulting in an increase of the storage capacitance. The pixel electrodes **191***a* and **191***b* also may overlap the data lines **171** to increase aperture ratio.

[0053] The contact assistants **192** and **199** are connected to the exposed end portions **125** of the gate lines **121** and the exposed end portions **179** of the data lines **171** through the contact holes **182** and **189**, respectively. The contact assistants **192** and **199** are not required, but are preferred to protect the exposed portions **125** and **179** and to complement the adhesiveness of the exposed portions **125** and **179** and external devices.

[0054] An alignment layer **11** is formed on the pixel electrodes **191***a* and **191***b*, the contact assistants **192** and **199**, and the passivation layer **180**.

[0055] With respect to the common electrode panel **200**, a black matrix **220** for preventing light leakage is formed on an insulating substrate **210** such as transparent glass. The black matrix **220** includes a plurality of openings facing the pixel electrodes **191***a* and **191***b* and having substantially the same shape as the pixel electrodes **191***a* and **191***b*.

[0056] A plurality of red, green and blue color filters **230** are formed with a substantial portion thereof in the openings of the black matrix **220** and an overcoat **250** is formed on the color filters **230**.

[0057] A common electrode **270** preferably made of transparent conductive material such as ITO and IZO is formed on the overcoat **250**. The common electrode **270** has a plurality of cutouts **271** and **272**. Each cutout **271** is aligned with a gap between a pair of pixel electrodes **191***a* and **191***b* and has two main edges parallel to the two opposite edges of the pair of pixel electrodes **191***a* and **191***b*. As shown, the cutouts **271** may overlap the edges of the pixel electrodes **191***a* and **191***b*. The cutouts **271** are provided for controlling the tilt directions of the LC molecules in the LC layer **300** and preferably have a width in a range between about 9 to about 12 microns. End portions of the cutouts **271** may have various shapes. The cutouts **272** are aligned with the data lines **171** and are provided for reducing the delay of the data voltages flowing in the data lines **171**. The delay is generated by the parasitic capacitance formed by the overlap of the common electrode **270** and the data lines **171**. The cutouts **272** are also used for controlling the tilt directions of the LC molecules of the LC layer **300**.

[0058] A homogeneous or homeotropic alignment layer **12** is coated on the common electrode **270**.

[0059] A pair of polarizers (not shown) are provided on the outer surfaces of the panels **100** and **200** such that their transmissive axes are crossed and one of the transmissive axes is parallel to the gate lines **121**.

[0060] The LCD may further include at least one retardation film (e.g., an optical element that produces, for example, full, half or quarter wave phase changes of polarized light) for compensating for the retardation of the LC layer **300**.

[0061] The LC molecules in the LC layer **300** are aligned such that their long axes are vertical to the surfaces of the panels **100** and **200**. The liquid crystal layer **300** has negative dielectric anisotropy.

[0062] Upon application of a common voltage to the common electrode **270** and a data voltage to the pixel electrodes **191***a* and **191***b*, a primary electric field substantially perpendicular to the surfaces of the panels **100** and **200** is generated. The LC molecules tend to change their orientations in response to the electric field such that their long axes are perpendicular to the field direction.

[0063] The cutouts **271** of the common electrode **270** and the edges of the pixel electrodes **191***a* and **191***b* distort the primary electric field to have a horizontal component which determines the tilt directions of the LC molecules. The horizontal component of the primary electric field adopts four different orientations, thereby forming four domains in the LC layer **300** with different LC molecule tilt directions. The horizontal component is perpendicular to the first and second edges of the cutouts **271**, perpendicular to the edge of the pixel electrode **191***a* and perpendicular to the edge of the pixel electrode **191***b*. Accordingly, four domains having different tilt directions are formed in the LC layer **300**. The cutouts **271** may be substituted with a plurality of protrusions formed on the common electrode **270** since the tilt directions of the LC molecules also can be controlled by a plurality of protrusions (not shown).

[0064] The directions of a secondary electric field due to the voltage difference between the pixel electrodes **191***a* and **191***b* are perpendicular to each of the edges of the cutouts **271**. Accordingly, the field direction of the secondary electric field coincides with that of the horizontal component of the primary electric field. Consequently, the secondary electric field between the pixel electrodes **191***a* and **191***b* enhances the tilt directions of the LC molecules.

[0065] Since the LCD performs inversion (i.e., inverting the polarity of an applied voltage) such as dot inversion, column inversion, etc., a secondary electric field that enhances the tilt directions of the LC molecules is attained by supplying an adjacent pixel electrode with a data voltage having opposite polarity with respect to the common voltage. As a result, a direction of the secondary electric field generated between adjacent pixel electrodes is equivalent to the horizontal component of the primary electric field generated between the common and pixel electrodes. Thus, a secondary electric field between the adjacent pixel electrodes can be generated to enhance the stability of the domains.

[0066] The tilt directions of all the domains form an angle of about 45 degrees with the gate lines **121**, and the gate lines **121** are parallel to or perpendicular to the edges of the panels **100** and **200**. Since a 45-degree intersection of the tilt directions and transmissive axes of the polarizers results in maximum transmittance, the polarizers can be attached such that the transmissive axes of the polarizers are parallel or perpendicular to the edges of the panels **100** and **200**, thereby reducing the production cost.

[0067] Referring to **FIGS. 1 and 2**, the symmetrical alignment of the pair of TFTs and the pair of pixel electrodes **191***a* and **191***b* about the gate electrode **123** and the data line **171**, respectively, creates constant parasitic capacitances between the data line **171** and the pixel electrodes **191***a*, **191***b* and between the gate electrode **123** and the drain electrodes **175***a*, **175***b*. As a result, brightness differences between shots are reduced.

[0068] It should be noted that increased resistance of the data lines **171** due to their curved structure can be compensated for by widening the data lines **171**. Further, distortion of the electric field and increase of the parasitic capacitance due to increases in width of the data lines **171** can, in turn, be compensated for by increasing the size of the pixel electrodes **191***a* and **191***b* and by adapting a thick organic passivation layer.

[0069] In a method of manufacturing the TFT array panel shown in **FIGS. 1 and 2**, a plurality of gate lines **121** including a plurality of gate electrodes **123** and a plurality of storage electrode lines **131** including a plurality of storage electrodes **133***a* and **133***b* are formed on an insulating substrate **110** such as transparent glass.

[0070] If the gate lines **121** and the storage electrode lines **131** have a double-layered structure including a lower conductive film and an upper conductive film, the lower conductive film is preferably made of material such as a Cr or Mo alloy having good physical and chemical characteristics and the upper conductive film is preferably made of Al or an Al containing metal.

[0071] After sequential deposition of a gate insulating layer **140** having a thickness of about 1,500 to about 5,000

Å, an intrinsic a-Si layer with a thickness of about 500 to about 2,000 Å, and an extrinsic a-Si layer with a thickness of about 300 to about 600 Å, are photo-etched to form a plurality of extrinsic semiconductor islands and a plurality of intrinsic semiconductor islands **150** on the gate insulating layer **140**.

[0072] Subsequently, a plurality of data lines **171** including a plurality of source electrodes **173** and a plurality of drain electrodes **175***a* and **175***b* are formed.

[0073] Thereafter, portions of the extrinsic semiconductor islands, which are not covered with the data lines **171** and the drain electrodes **175***a* and **175***b*, are removed to complete a plurality of ohmic contact islands **163** and **165** and to expose portions of the intrinsic semiconductor islands **150**. Oxygen plasma treatment preferably follows thereafter in order to stabilize the exposed surfaces of the semiconductor islands **150**.

[0074] A passivation layer **180** is formed of a photosensitive organic insulating material such as acryl-based material and is deposited on the existing structure. After depositing the passivation layer **180**, the passivation layer **180** and the gate insulating layer **140** are patterned to form a plurality of contact holes **182**, **185***a*, **185***b* and **189** exposing end portions **125** of the gate lines **121**, the drain electrodes **175***a* and **17***bb*, and end portions **179** of the data lines **171**, respectively.

[0075] Finally, a plurality of pixel electrodes **191***a* and **191***b* and a plurality of contact assistants **192** and **199** are formed on the passivation layer **180** by sputtering and photo-etching an IZO or ITO layer with a thickness of about 400 to about 500 Å.

[0076] **FIG. 3** is a layout view of an LCD according to another embodiment of the present invention, and **FIG. 4** is a sectional view of the LCD shown in **FIG. 3** taken along the line IV-VI'.

[0077] As shown in **FIGS. 3 and 4**, a layered structure of a TFT array panel of an LCD according to this embodiment includes some of the same elements as shown in **FIGS. 1 and 2**. In the configuration shown in **FIGS. 3 and 4**, a plurality of gate lines **121** including a plurality of gate electrodes **123** and a plurality of storage electrodes lines **131** including a plurality of storage electrodes **133***a* and **133***b* are formed on a substrate **110**. A gate insulating layer **140**, a plurality of semiconductor stripes **152**, and a plurality of ohmic contact stripes and islands **163** and **165** are sequentially formed on the substrate **110** including the gate lines **121**, gate electrodes **123**, storage electrode lines **131** and storage electrodes **133***a*, **133***b*. A plurality of data lines **171** including a plurality of source electrodes **173** and a plurality of drain electrodes **175***a* and **175***b* are formed on the ohmic contacts **163** and **165**, and a passivation layer **180** and an alignment layer **11** are sequentially formed thereon. A plurality of contact holes **182**, **185***a*, **185***b* and **189** are provided in the passivation layer **180** and/or the gate insulating layer **140**, and a plurality of pixel electrodes **191***a* and **191***b* and a plurality of contact assistants **192** and **199** are formed on the passivation layer **180**.

[0078] A layered structure of a common electrode panel of the LCD according to the embodiment shown in **FIG. 4** includes some of the same elements as shown in **FIGS. 1 and 2**. For example, a black matrix **220**, an overcoat **250**, and a common electrode **270** as well as an alignment layer **21** are sequentially formed on an insulating substrate **210**.

[0079] As distinguished from the TFT array panel shown in **FIGS. 1 and 2**, the TFT array panel according to the embodiment shown in **FIGS. 3 and 4** extends the semiconductor stripes **152** and the ohmic contacts **163** along the data lines **171**. Also, the semiconductor stripes **152** have almost the same planar shapes as the data lines **171** and the drain electrodes **175***a* and **175***b* as well as the underlying ohmic contacts **163** and **165**, except for channel portions of the TFTs.

[0080] Also unlike the LCD of **FIGS. 1 and 2**, a plurality of red, green and blue color filters R, G and B are formed under the passivation layer **180** opposite the pixel electrodes **191***a* and **191***b*, and there is no color filter on the upper panel **200**. Further, the contact holes **185***a* and **185***b* penetrate the color filters R, G and B. Two adjacent color filters of the color filters R, G and B may overlap each other to enhance the prevention of light leakage.

[0081] A manufacturing method of the TFT array panel according to an embodiment of the present invention simultaneously forms the data lines **171**, the drain electrodes **175***a* and **175***b*, the semiconductor stripes **152**, and the ohmic contacts **163** and **165** using one photolithography process. A photoresist pattern for the photolithography process has position-dependent thickness, and in particular, it has portions with smaller thickness located on the channels of TFTs. Therefore, additional photolithography processes can be omitted to simplify the manufacturing process.

[0082] Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to those precise embodiments, and that various other changes and modifications may be affected therein by one of ordinary skill in the related art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended claims.

What is claimed is:

1. A liquid crystal display, comprising:

a first substrate including a first electrode and a second electrode formed thereon;

a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap;

at least one gate electrode formed on the first substrate; and

at least two transistors formed on the first substrate and symmetrically disposed about the at least one gate electrode.

2. The liquid crystal display as recited in claim 1, wherein the first electrode is a first pixel electrode, the second electrode is a second pixel electrode and the third electrode is a common electrode.

3. The liquid crystal display as recited in claim 1, wherein a pair of the symmetrically disposed transistors includes the at least one gate electrode, at least one source electrode, at least two drain electrodes and at least one semiconductor island.

4. The liquid crystal display as recited in claim 1, further comprising a plurality of data lines for transmitting data voltages formed on the first substrate, wherein the first and second electrodes are symmetrically disposed about at least one data line of the plurality of data lines.

5. The liquid crystal display as recited in claim 1, further comprising at least one cutout formed in the third electrode, wherein the at least one cutout includes a first edge aligned parallel to an edge of the first electrode and a second edge aligned parallel to an edge of the second electrode.

6. The liquid crystal display as recited in claim 5, wherein the at least one cutout is aligned with a space between the first and second electrodes.

7. The liquid crystal display as recited in claim 5, wherein a component of an electric field generated between the third and the first and second electrodes for causing a change in tilt direction of liquid crystal molecules aligns at least one of perpendicular to the first edge of the cutout, perpendicular to the second edge of the cutout, perpendicular to the edge of the first electrode and perpendicular to the edge of the second electrode.

8. The liquid crystal display as recited in claim 5, wherein the at least one cutout has width within the range of about 9 to about 12 microns.

9. The liquid crystal display as recited in claim 5, wherein an electric field is generated between the first and second electrodes, and a direction of the electric field is at least one of perpendicular to the first edge of the at least one cutout and perpendicular to the second edge of the at least one cutout.

10. The liquid crystal display as recited in claim 1, further comprising:

a plurality of data lines for transmitting data voltages formed on the first substrate; and

at least one cutout formed in the third electrode, wherein the at least one cutout is aligned with the at least one data line.

11. The liquid crystal display as recited in claim 1, wherein a voltage having an opposite polarity with respect to a voltage applied to the third electrode is applied to one of the first electrode and the second electrode, and an electric field is generated between the first electrode and the second electrode.

12. The liquid crystal display of claim 11, wherein the electric field is due to a voltage difference between the first electrode and the second electrode.

13. A liquid crystal display, comprising:

a first substrate including a first pixel electrode and a second pixel electrode formed thereon; and

a second substrate including a common electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap, and a voltage having an opposite polarity with respect to a voltage applied to the common electrode is applied to one of the first pixel electrode and the second pixel electrode to generate an electric field between the first pixel electrode and the second pixel electrode having a direction which coincides with a component of an electric field generated between the common electrode and the first and second pixel electrodes.

14. A liquid crystal display, comprising:

a first substrate including a first electrode and a second electrode formed thereon;

a second substrate including a third electrode formed thereon, wherein the second substrate is spaced apart from the first substrate by a gap; and

a plurality of data lines for transmitting data voltages formed on the first substrate, wherein the first and second electrodes are symmetrically disposed about at least one data line of the plurality of data lines.

* * * * *

专利名称(译)	液晶显示器及其薄膜晶体管阵列面板		
公开(公告)号	[US20060203173A1](US20060203173A1)	公开(公告)日	2006-09-14
申请号	US11/433319	申请日	2006-05-12
[标]申请(专利权)人(译)	金东GYU 金相SOO		
申请(专利权)人(译)	金东GYU 金相洙		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	KIM DONG GYU KIM SANG SOO		
发明人	KIM, DONG-GYU KIM, SANG-SOO		
IPC分类号	G02F1/1343 G02F1/1333 G02F1/136 G02F1/1362 G02F1/1368 G02F1/139 H01L29/786		
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其他公开文献	US7872700		
外部链接	Espacenet USPTO		

摘要(译)

一种液晶显示器，包括：第一基板，包括形成在其上的第一电极和第二电极;第二基板，包括形成在其上的第三电极;其中，第二基板通过间隙与第一基板间隔开，并且形成至少一个切口在第三电极中，其中至少一个切口与第一和第二电极之间的空间对齐。