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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND FABRICATING METHOD THEREOF**

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(57) **ABSTRACT**

A thin film transistor substrate for applying a horizontal electric field and a fabricating method thereof for simplifying a process are disclosed. In a liquid crystal display device according to the present invention, a gate line on a substrate; a data line crossing the gate line having a gate insulating film there between to define a pixel area; a thin film transistor including a gate electrode, a source electrode, a drain electrode and a semiconductor layer to define a channel between the source electrode and the drain electrode; a common line on the substrate; a common electrode in the pixel area; and a pixel electrode in the pixel area to form a horizontal electrode field with the common electrode, wherein the data line, the source electrode and the drain electrode have an opaque conductive pattern and a transparent conductive pattern, the pixel electrode is formed by an extension of the transparent conductive pattern of the drain electrode, and a protective film borders with the transparent conductive pattern and in the remaining area thereof.

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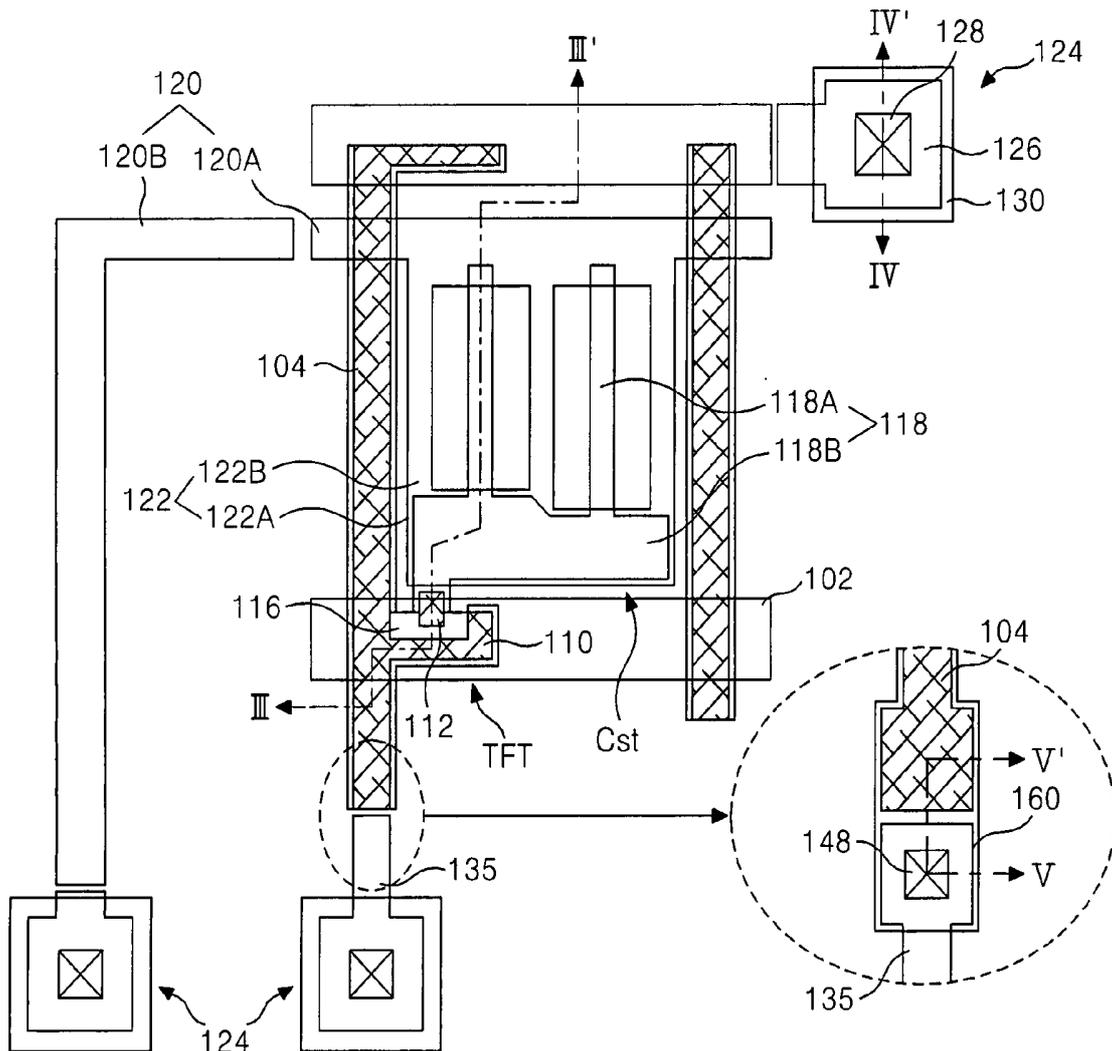


FIG. 1
RELATED ART

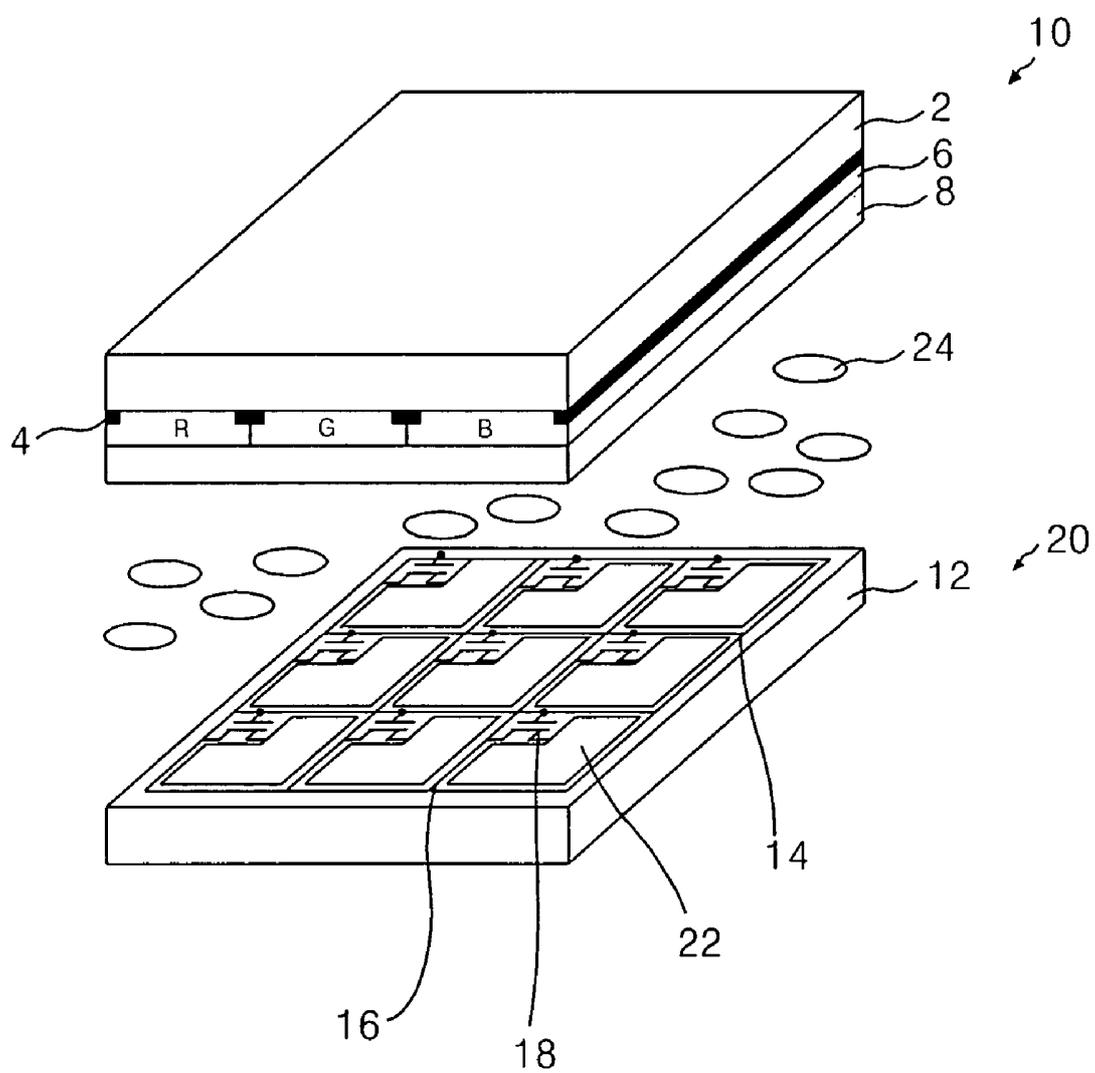
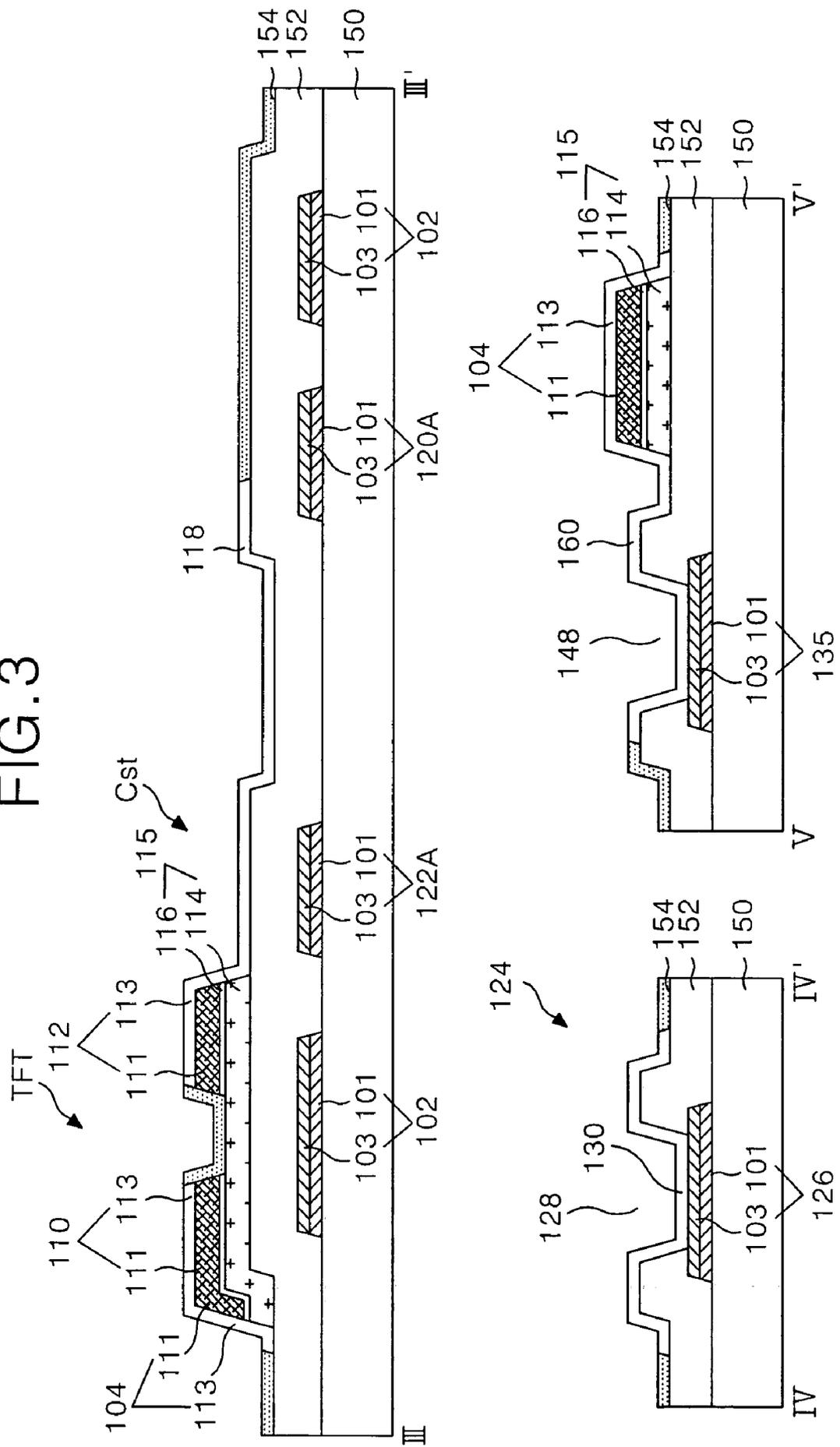


FIG. 3



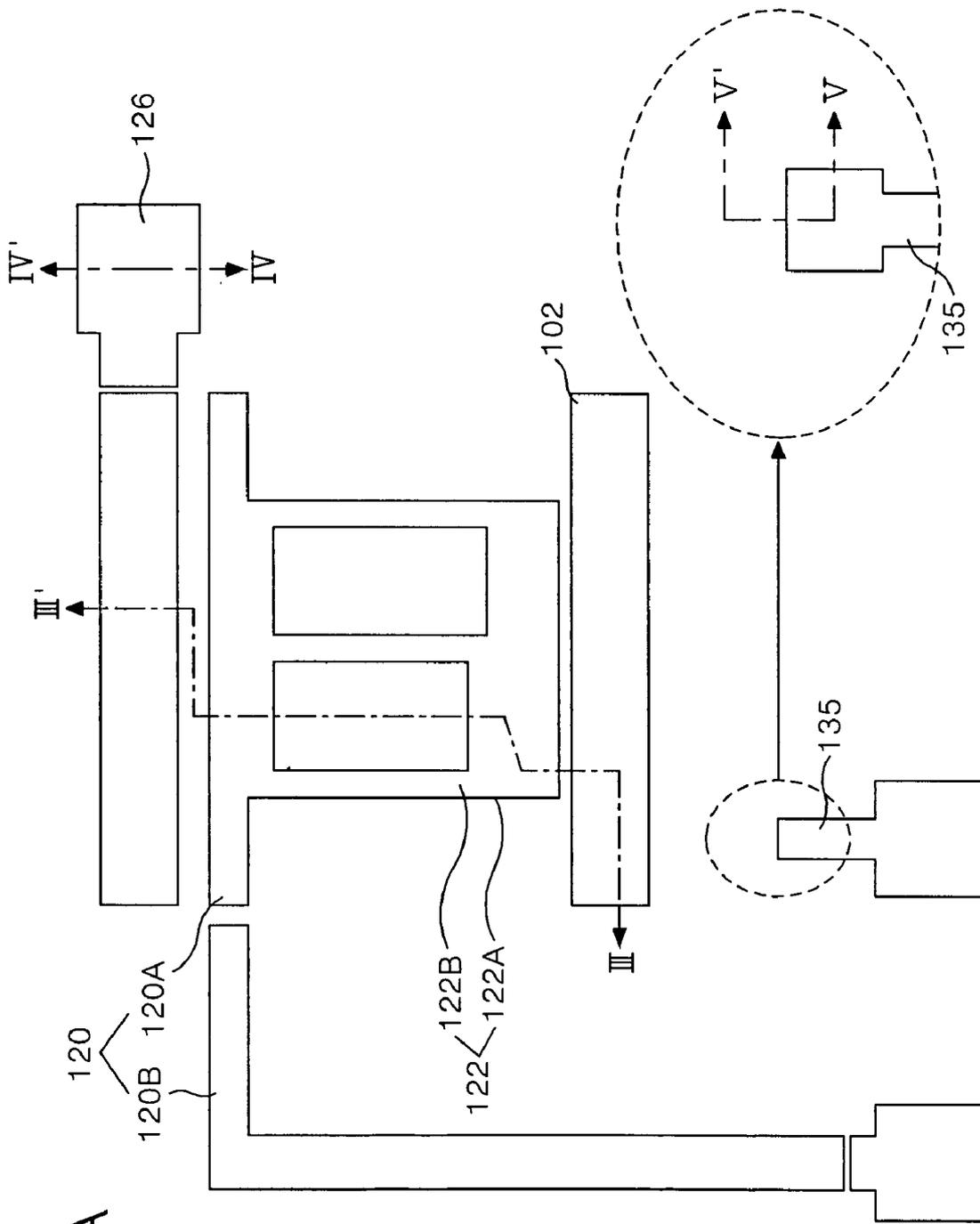
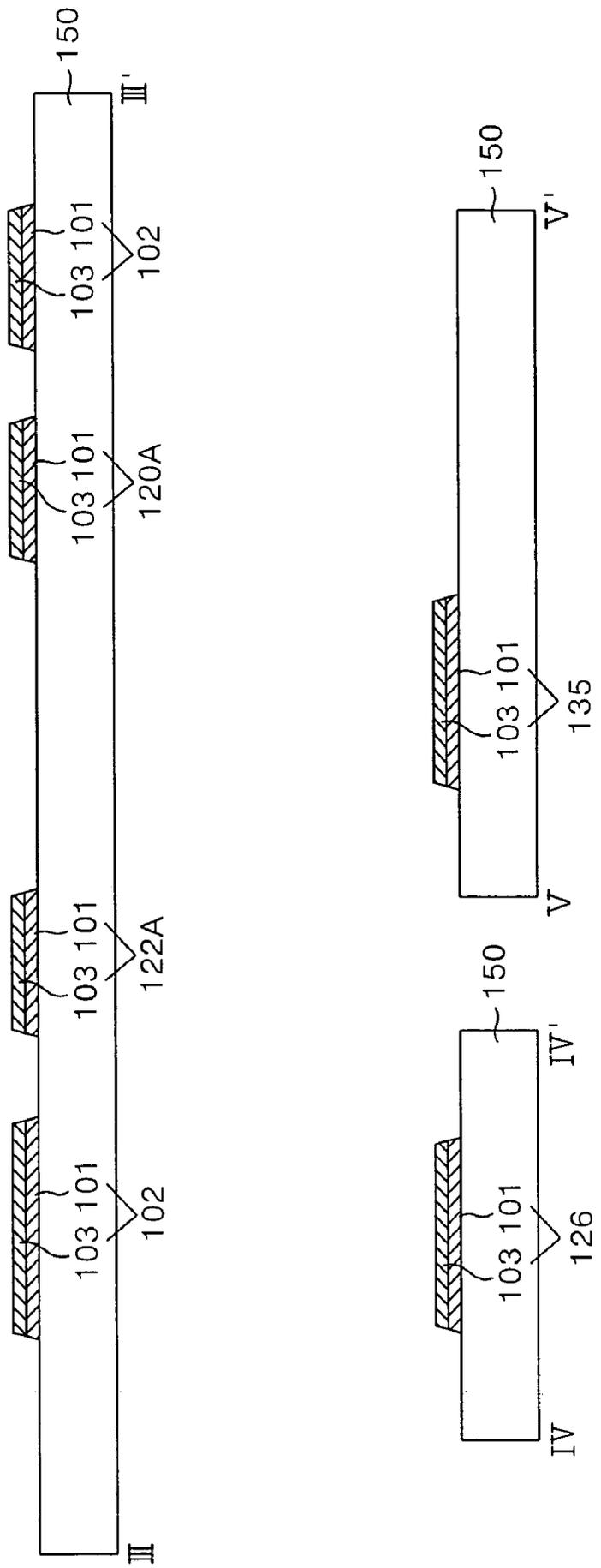


FIG. 5A

FIG. 5B



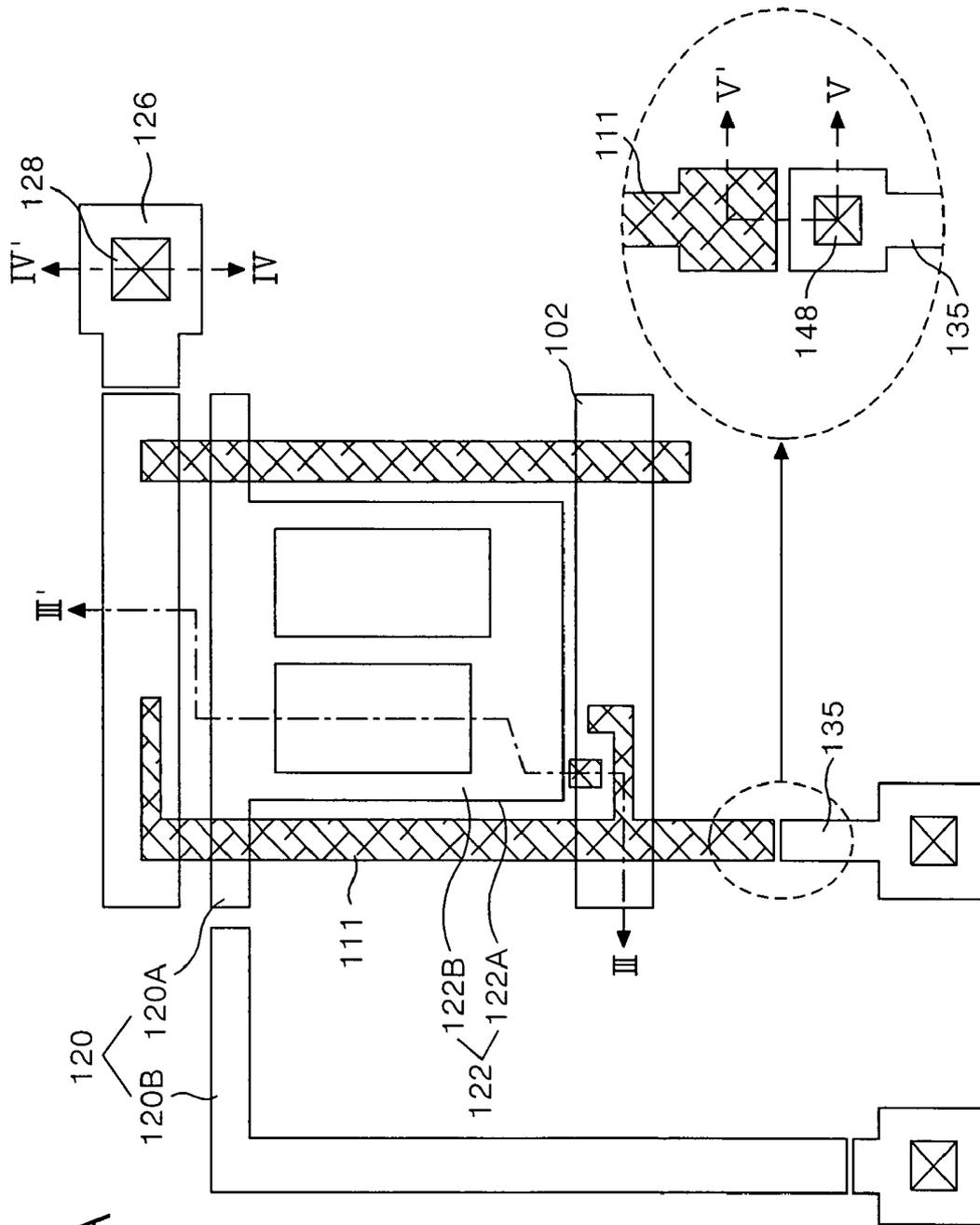


FIG. 6A

FIG. 6B

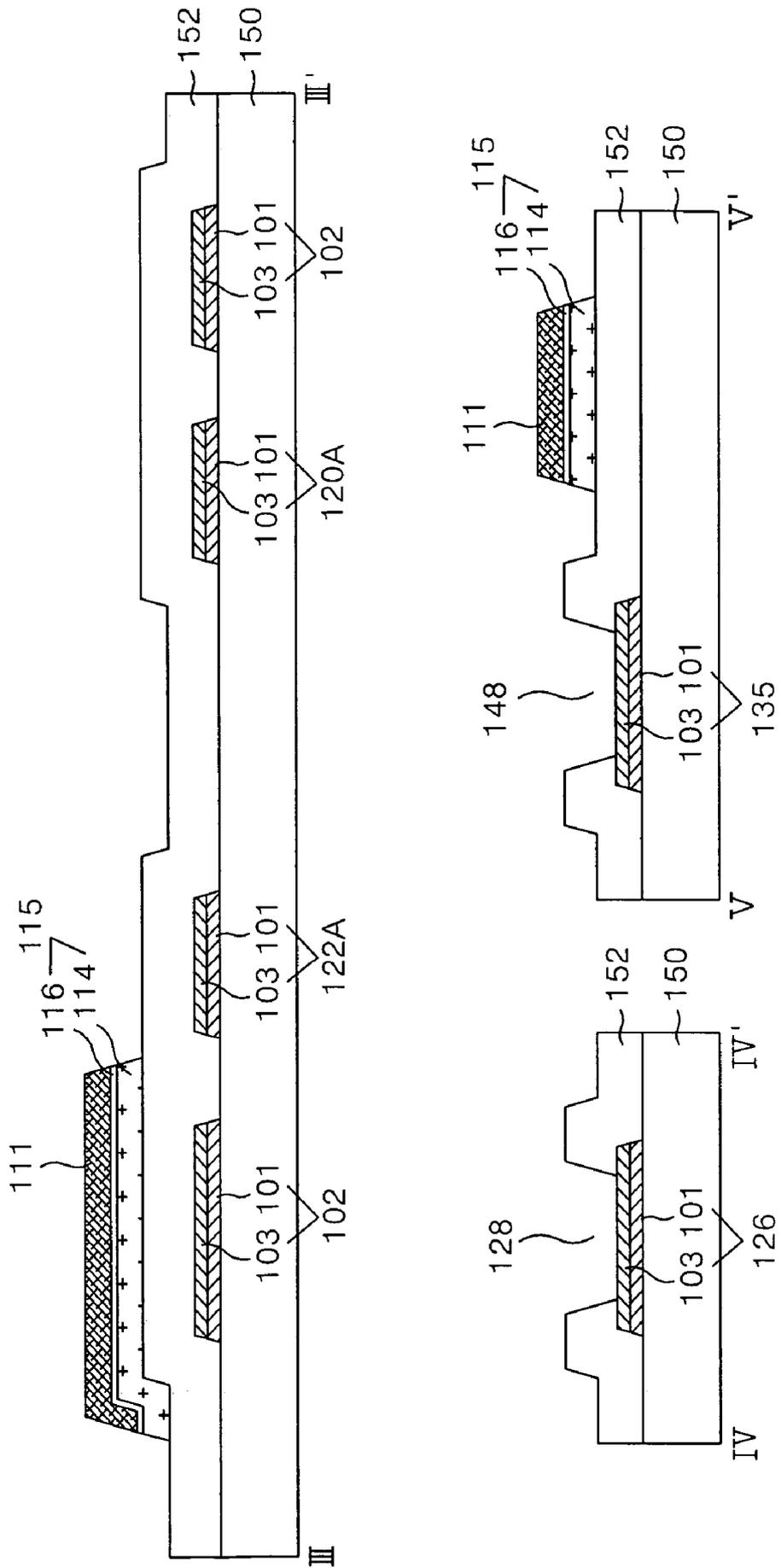


FIG. 7A

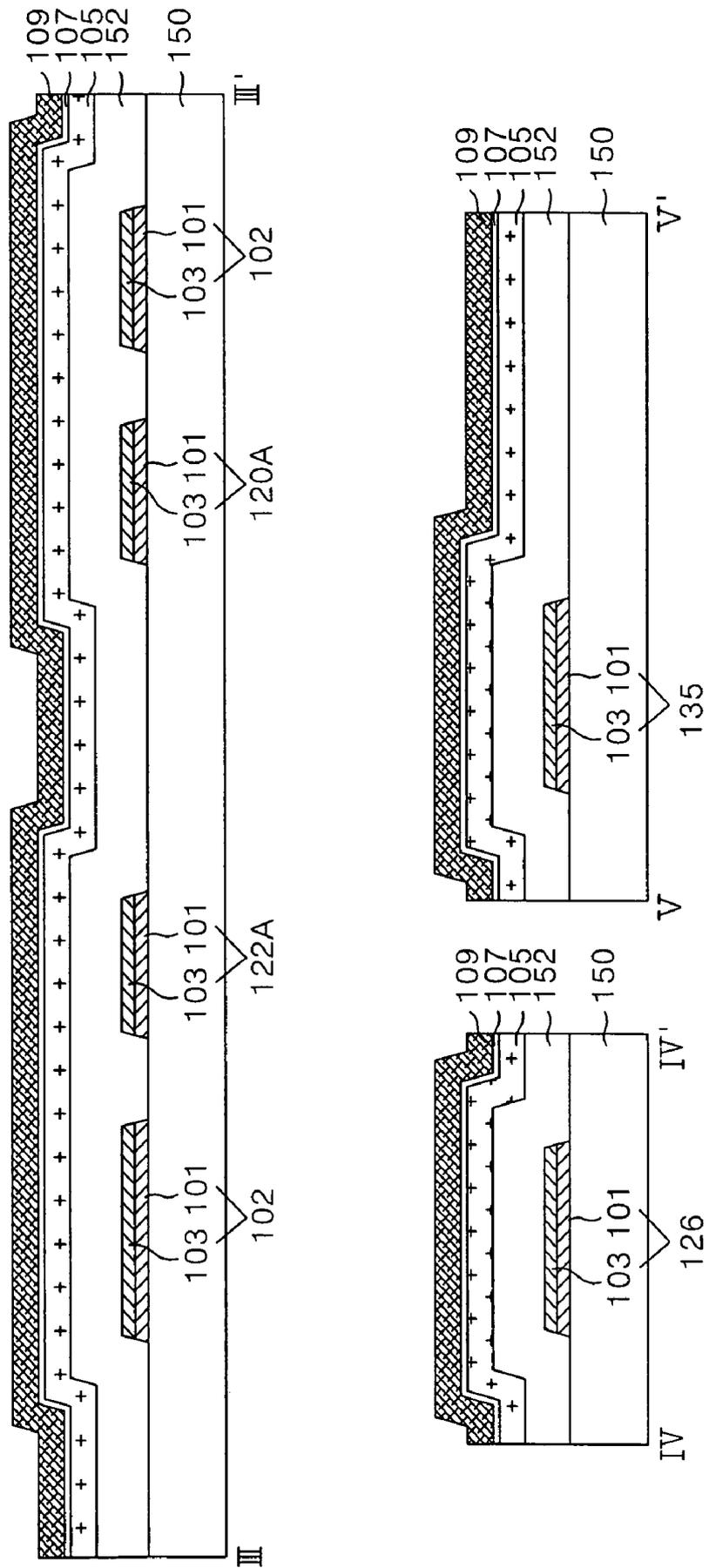


FIG. 7B

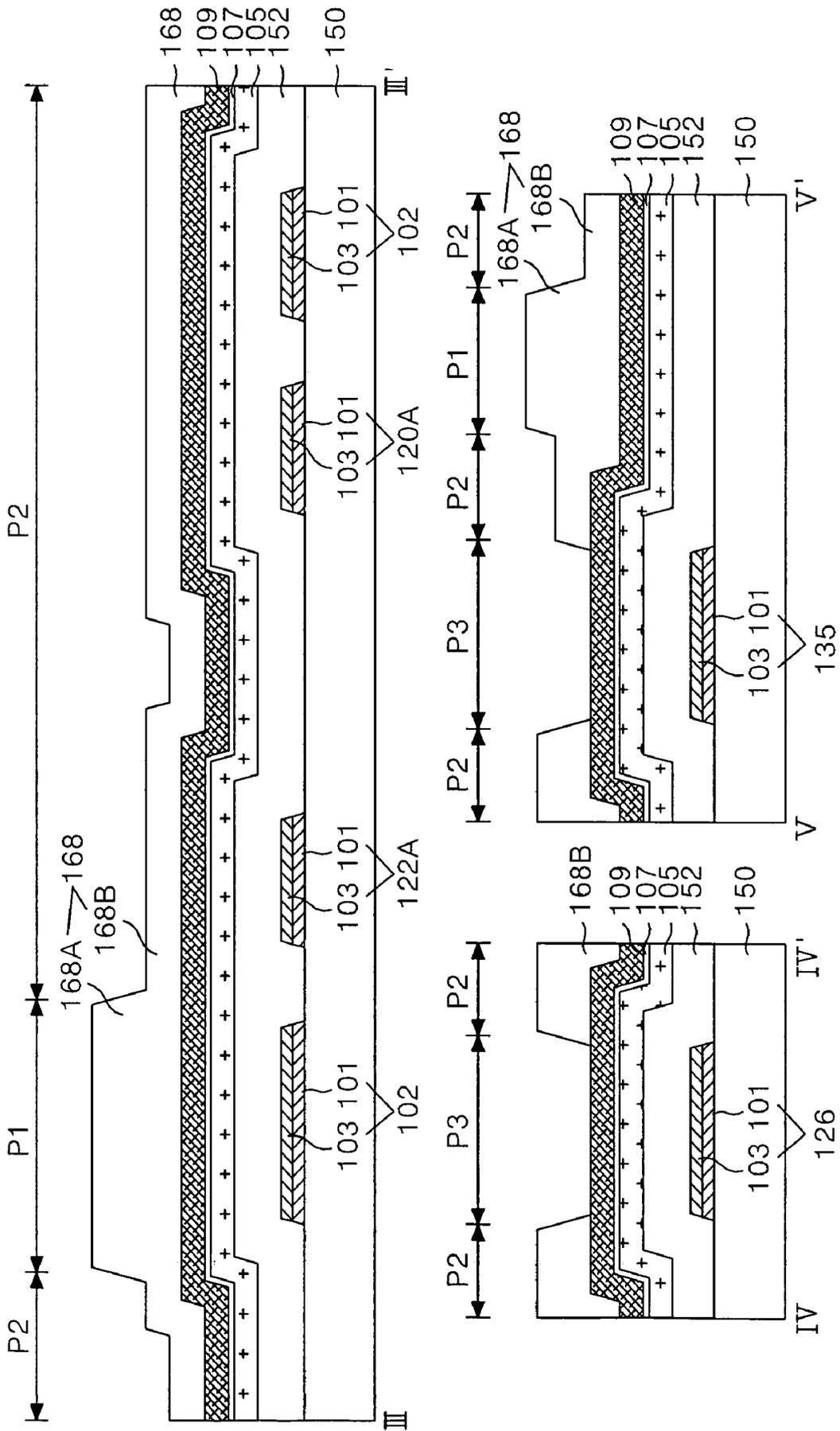


FIG. 7D

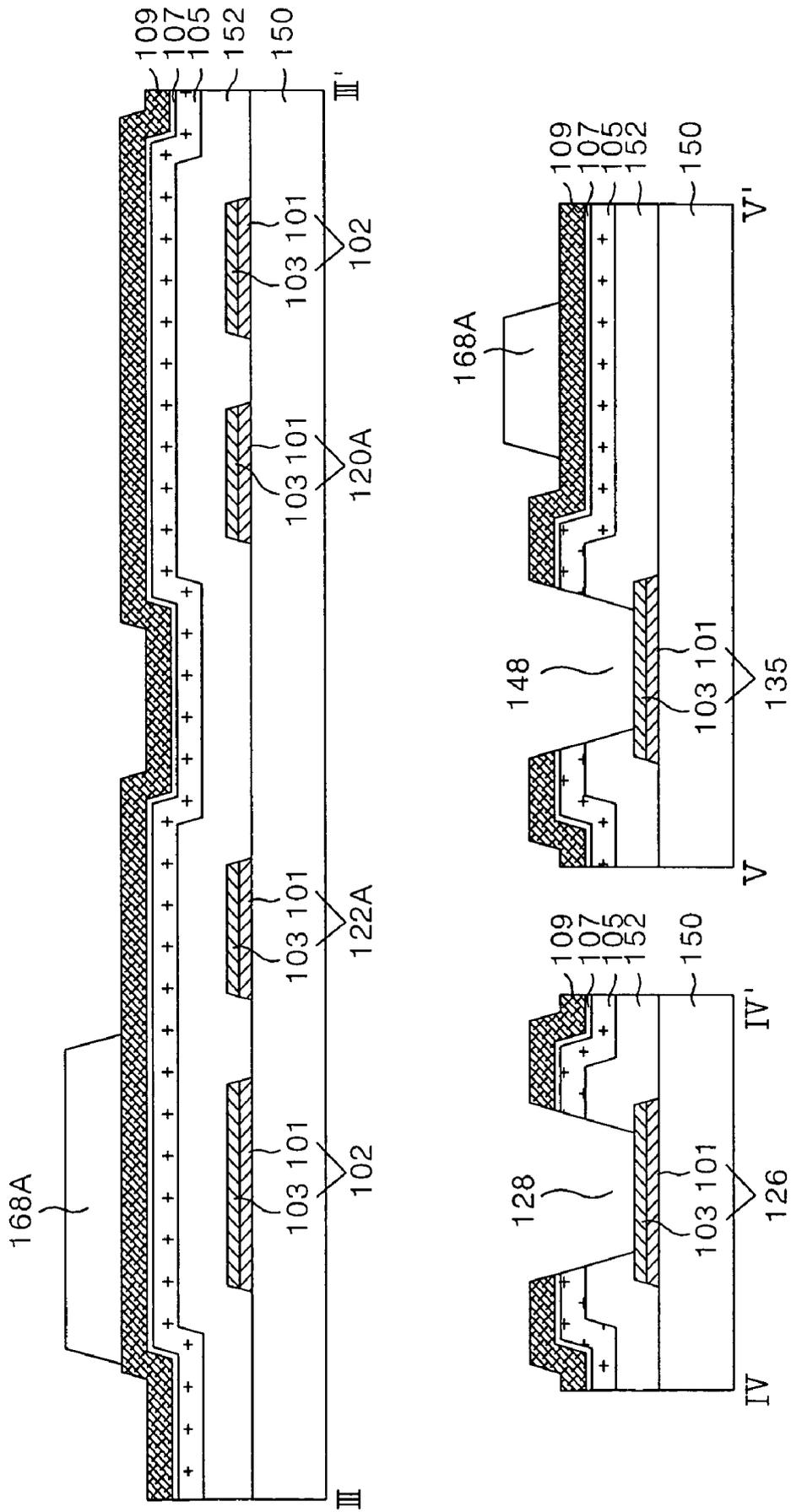


FIG. 7E

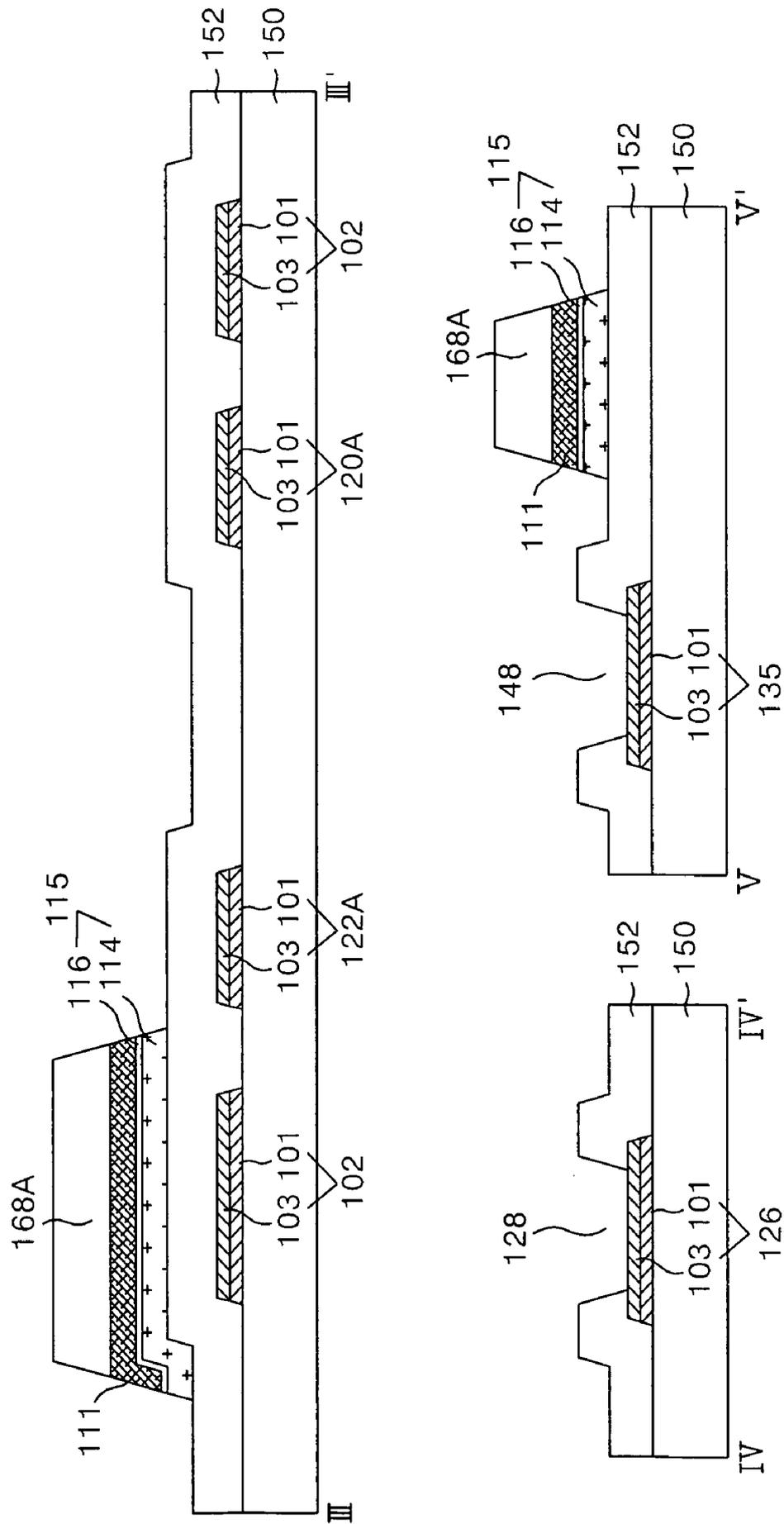


FIG. 7F

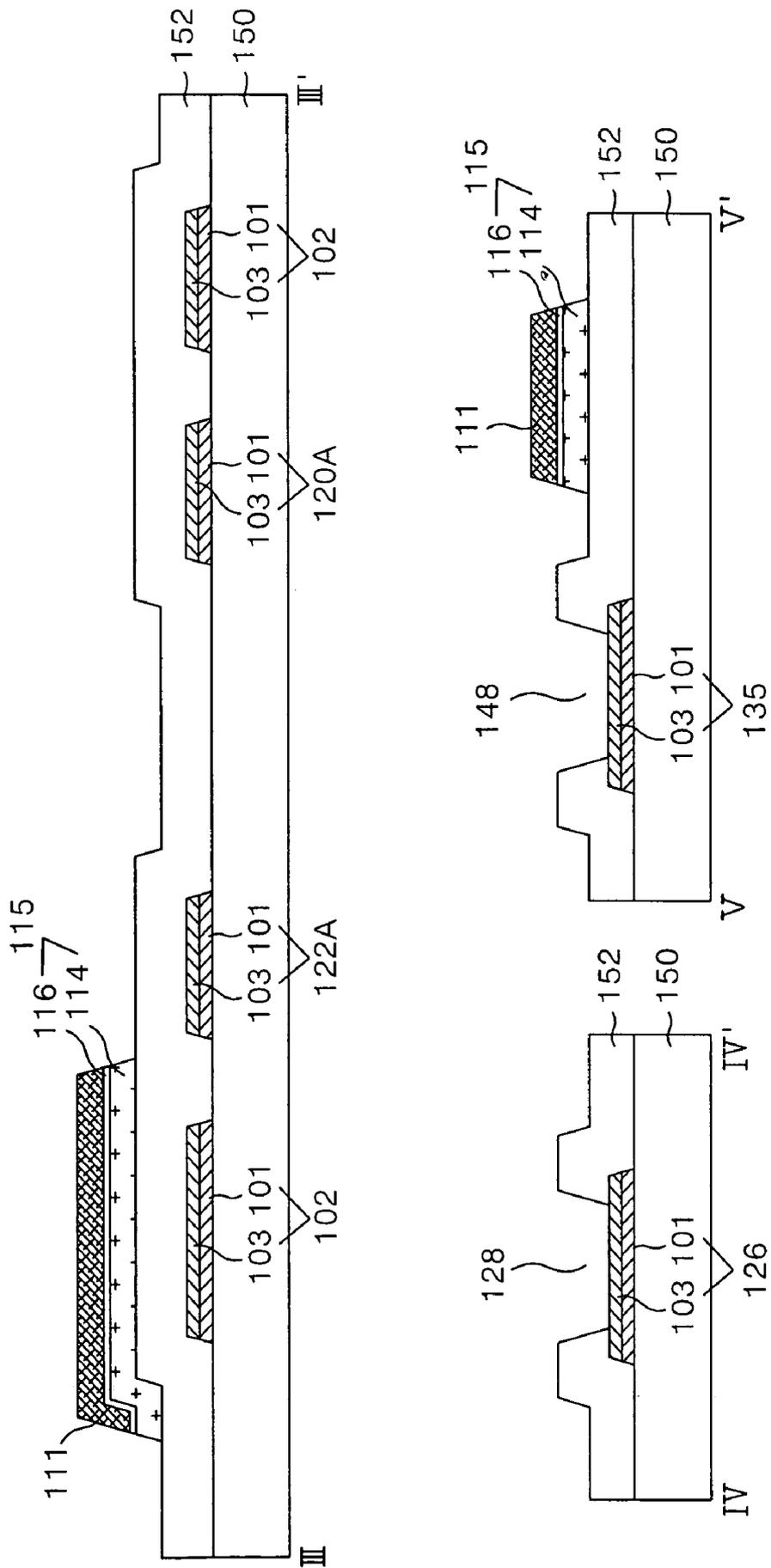


FIG. 9A

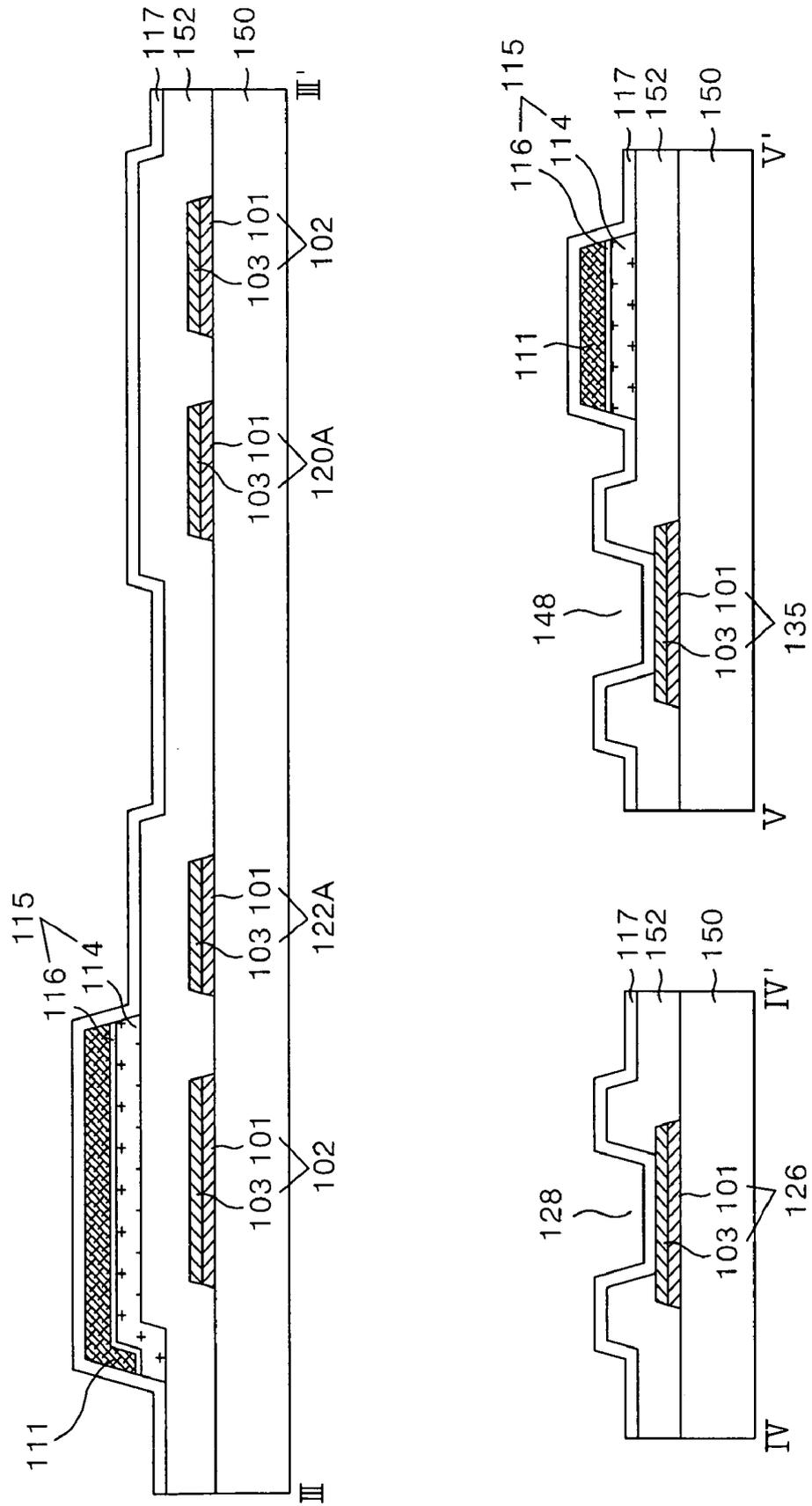


FIG. 9C

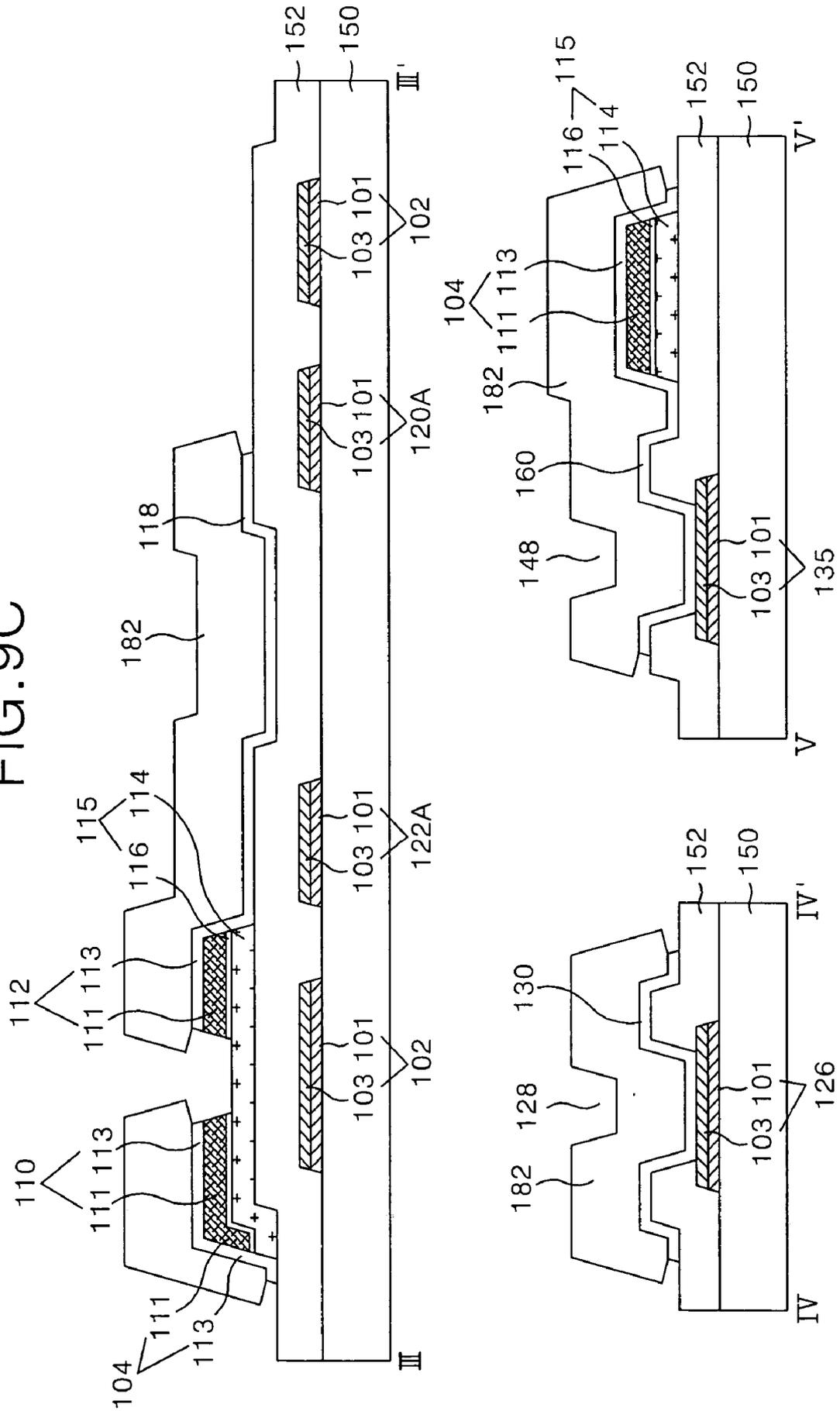


FIG. 9D

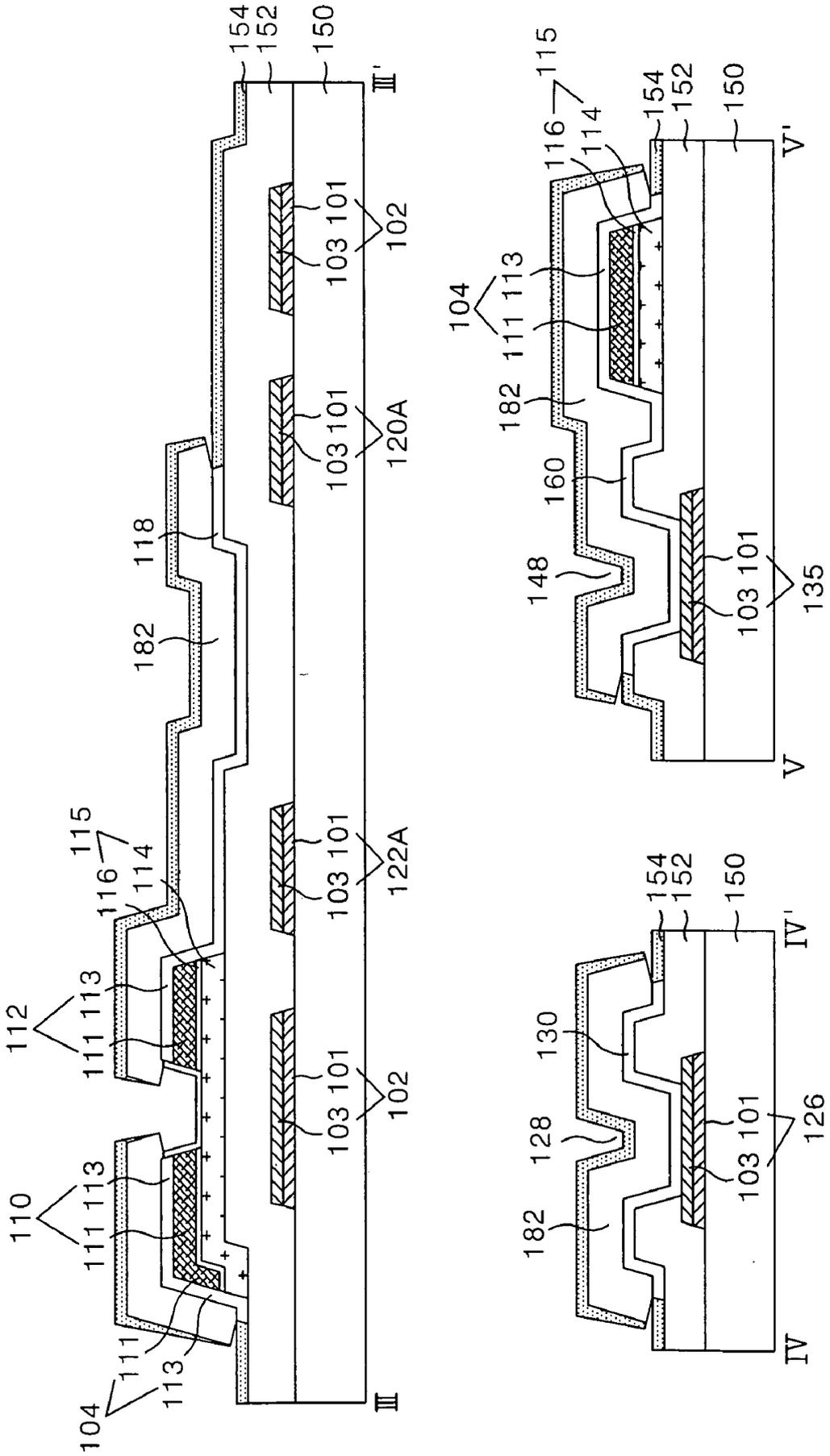
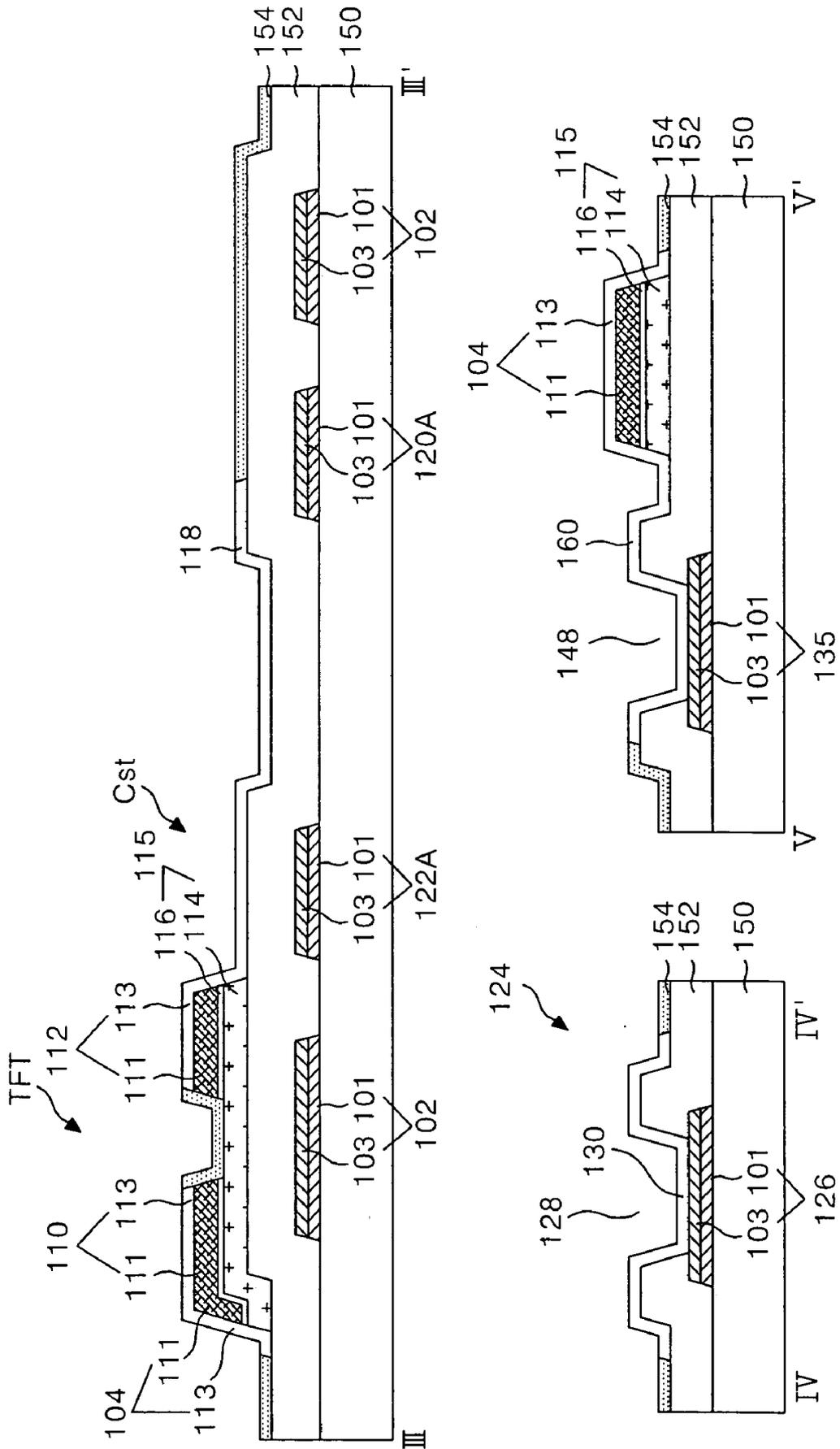


FIG. 9E



LIQUID CRYSTAL DISPLAY DEVICE AND FABRICATING METHOD THEREOF

[0001] This application claims the benefit of Korean Patent Application No. P2004-112584 filed in Korea on Dec. 24, 2004, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a liquid crystal display using a horizontal electric field, and more particularly to a thin film transistor substrate and a fabricating method thereof that are adaptive for simplifying a process.

[0004] 2. Description of the Related Art

[0005] Generally, a liquid crystal display (LCD) controls light transmittance of a liquid crystal having a dielectric anisotropy using an electric field to thereby display a picture. To this end, the LCD includes a liquid crystal display panel for displaying a picture by a liquid crystal cell matrix, and a driving circuit for driving the liquid crystal display panel.

[0006] Referring to **FIG. 1**, a related art liquid crystal display panel is comprised of a color filter substrate **10** and a thin film transistor substrate **20** that are joined to each other with having a liquid crystal **24** there between.

[0007] The color filter substrate **10** includes a black matrix **4**, a color filter **6** and a common electrode **8** that are sequentially provided on an upper glass substrate **2**. The black matrix **4** is provided in a matrix type on the upper glass substrate **2**. The black matrix **4** divides an area of the upper glass substrate **2** into a plurality of cell areas to be provided with the color filter **6**, and prevents a light interference between adjacent cells and an external light reflection. The color filter **6** is provided at the cell area divided by the black matrix **4** in such a manner to be divided into red(R), green(G) and blue(B) ones, thereby transmitting red, green and blue lights. The common electrode **8** is formed from a transparent conductive layer entirely coated onto the color filter **6**, and supplies a common voltage V_{com} that serves as a reference voltage upon driving of the liquid crystal **24**. Further, an over-coated layer (not illustrated) for smoothing the color filter **6** may be provided between the color filter **6** and the common electrode **8**.

[0008] The thin film transistor substrate **20** includes a thin film transistor **18** and a pixel electrode **22** provided for each cell area defined by an crossing between a gate line **14** and a data line **16** at a lower glass substrate **12**. The thin film transistor **18** applies a data signal from the data line **16** to the pixel electrode **22** in response to a gate signal from the gate line **14**. The pixel electrode **22** formed from a transparent conductive layer supplies a data signal from the thin film transistor **18** to drive the liquid crystal **24**.

[0009] The liquid crystal **24** having a dielectric anisotropy is rotated in accordance with an electric field formed by a data signal from the pixel electrode **22** and a common voltage V_{com} from the common electrode **8** to control light transmittance, thereby implementing a gray scale level.

[0010] Further, the liquid crystal display panel includes a spacer (not illustrated) for constantly keeping a cell gap between the color filter substrate **10** and the thin film transistor substrate **20**.

[0011] In such a liquid crystal display panel, the color filter substrate **10** and the thin film transistor substrate **20** are formed by a plurality of mask processes. Herein, one mask process includes a lot of processes such as thin film deposition (coating), cleaning, photolithography, etching, photoresist stripping and inspection processes, etc.

[0012] Particularly, because the thin film transistor substrate includes the semiconductor process and requires the plurality of mask processes, it has a complicate fabricating process to act as a major factor in the manufacturing cost rise of the liquid crystal display panel. Therefore, the thin film transistor substrate has been developed toward a reduction in the number of mask process.

[0013] Meanwhile, the liquid crystal displays are largely classified into a vertical electric field applying type and a horizontal electric field applying type depending upon with a direction of the electric field driving the liquid crystal.

[0014] The liquid crystal display of vertical electric field applying type drives a liquid crystal in a twisted nematic (TN) mode with a vertical electric field formed between a pixel electrode and a common electrode arranged in opposition to each other on the upper and lower substrate. The liquid crystal display of vertical electric field applying type has an advantage of a large aperture ratio while having a drawback of a narrow viewing angle about 90° .

[0015] The liquid crystal display of horizontal electric field applying type drives a liquid crystal in an in plane switching (IPS) mode with a horizontal electric field between the pixel electrode and the common electrode arranged in parallel to each other on the lower substrate. The liquid crystal display of horizontal electric field applying type has an advantage of a wide viewing angle about 160° .

[0016] The thin film transistor substrate in the liquid crystal display of horizontal electric field applying type also requires a plurality of mask process thereby complicating the fabricating process. Therefore, in order to reduce the manufacturing cost, it is necessary to reduce the number of mask processes.

SUMMARY OF THE INVENTION

[0017] Accordingly, it is an advantage of the present invention to provide a thin film transistor substrate of horizontal electric field applying type and a fabricating method thereof that are adaptive for simplifying a process.

[0018] In order to achieve these and other advantages of the invention, a liquid crystal display device according to one aspect of the present invention comprises a gate line on a substrate; a data line crossing the gate line having a gate insulating film there between to define a pixel area; a thin film transistor including a gate electrode, a source electrode, a drain electrode and a semiconductor layer for defining a channel between the source electrode and the drain electrode; a common line on the substrate; a common electrode in the pixel area; and a pixel electrode in the pixel area to form a horizontal electrode field with the common electrode, wherein the data line, the source electrode and the drain electrode have an opaque conductive pattern and a transparent conductive pattern, the pixel electrode is formed by an extension of the transparent conductive pattern of the drain electrode, and a protective film borders with the transparent conductive pattern and in the remaining area thereof.

[0019] A method of fabricating a liquid crystal display device according to another aspect of the present invention comprises a first mask process of forming a first mask pattern group including a gate line, a gate electrode, a common line and a common electrode on a substrate; a second mask process of forming a gate insulating film on the first mask pattern group and a semiconductor pattern and an opaque conductive pattern on the gate insulating film; and a third mask process of forming a transparent conductive pattern on the opaque conductive pattern and forming a protective film having a border with the transparent conductive pattern, wherein a data line crossing the gate line, a source electrode and a drain electrode are formed of a double-layer structure having the opaque conductive pattern and the transparent conductive pattern, and a pixel electrode is extended from the transparent conductive pattern of the drain electrode to form a horizontal electric field with the common electrode.

[0020] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0022] In the drawings:

[0023] **FIG. 1** is a schematic perspective view illustrating a structure of a related art liquid crystal display panel;

[0024] **FIG. 2** is a plan view illustrating a structure of a thin film transistor substrate of horizontal electric field applying type according to an embodiment of the present invention;

[0025] **FIG. 3** is a section view of the thin film transistor substrate taken along the III-III', IV-IV' and V-V' lines in **FIG. 2**;

[0026] **FIG. 4** is a plan view illustrating a structure of a thin film transistor substrate of horizontal electric field applying type according to another embodiment of the present invention;

[0027] **FIG. 5A** and **FIG. 5B** are a plan view and a section view illustrating a first mask process in a method of fabricating the thin film transistor substrate of horizontal electric field applying type according to the embodiment of the present invention, respectively;

[0028] **FIG. 6A** and **FIG. 6B** are a plan view and a section view illustrating a second mask process in a method of fabricating the thin film transistor substrate horizontal electric field applying type according to the embodiment of the present invention, respectively;

[0029] **FIG. 7A** to **FIG. 7F** are section views for specifically explaining the second mask process;

[0030] **FIG. 8A** and **FIG. 8B** are a plan view and a section view illustrating a third mask process in a method of fabricating the thin film transistor substrate horizontal elec-

tric field applying type according to the embodiment of the present invention, respectively; and

[0031] **FIG. 9A** to **FIG. 9E** are section views for specifically explaining the third mask process.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0032] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0033] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to **FIGS. 2** to **9E**.

[0034] **FIG. 2** is a plan view illustrating a structure of a thin film transistor substrate of horizontal electric field applying type according to an embodiment of the present invention, and **FIG. 3** is a section view of the thin film transistor substrate taken along the III-III', IV-IV' and V-V' lines in **FIG. 2**.

[0035] Referring to **FIG. 2** and **FIG. 3**, the thin film transistor substrate includes a gate line **102** and a data line **104** provided on a lower substrate **150** in such a manner to cross each other with having a gate insulating film **144** there between and define a pixel area, a thin film transistor TFT connected to the gate line **102** and the data line **104**, a pixel electrode **118** and a common electrode **122** provided to form a horizontal electric field at said pixel area, a common line **120** connected to the common electrode **122**, and a storage capacitor **Cst** provided at an overlapping portion between the pixel electrode **118** and a drain electrode **122**. Further, the thin film transistor substrate includes pads **124** connected to the gate line **102**, the data line **104** and the common line **120**.

[0036] The gate line **102** supplies a scanning signal from a gate driver (not illustrated) while the data line **104** supplies a video signal from a data driver (not illustrated). The gate line **102** and the data line **104** cross each other with having a gate insulating film **152** there between to define the pixel area.

[0037] The gate line **102** is formed on the substrate **150** in a multiple-layer structure having at least double gate metal layers built. For instance, as illustrated in **FIG. 3**, the gate line **102** has a double-layer structure in which first and second gate metal layers **101** and **103** are built. The data line **104** is formed on the gate insulating film **152** in a multiple-layer structure having at least double layers including a transparent conductive layer. For instance, as illustrated in **FIG. 3**, the data line **104** has a double-layer structure in which a source/drain metal pattern **111** and a transparent conductive pattern **113** are built. Herein, the transparent conductive pattern **113** is provided in such a manner to capture the source/drain metal pattern **111**, thereby preventing an illumination problem caused by an exposure of the source/drain metal pattern **111**.

[0038] The thin film transistor TFT allows a pixel signal on the data line **104** to be charged into the pixel electrode **118** and stored in response to a scanning signal from the gate line **102**. To this end, the thin film transistor TFT includes a gate electrode included in the gate line **102**, a source electrode **110** connected to the data line **104**, a drain elec-

trode 112 positioned in opposition to the source electrode 110 to be connected to the pixel electrode 118, and a semiconductor pattern 115 overlapping with the gate line 102 with having the gate insulating film 152 there between to define a channel between the source electrode 110 and the drain electrode 112. Herein, the source electrode 110 and the drain electrode 112 have a double-layer structure in which the source/drain metal pattern 111 and the transparent conductive pattern 113 are built. The semiconductor pattern 115 includes an active layer 114 forming a channel between the source electrode 110 and the drain electrode 112, and an ohmic contact layer 116 formed on the active layer 114 other than the channel portion to make an ohmic contact with the source electrode 110 and the drain electrode 112.

[0039] The common line 120 and the common electrode 122 supply a reference voltage for driving the liquid crystal, that is, a common voltage to each pixel. The common line 120 and the common electrode 122 have a double-layer structure in which the first and second gate metal layers 101 and 103 are built.

[0040] The common line 120 includes an internal common line 120A provided in parallel to the gate line 102 at a display area, and an external common line 120B commonly connected to the internal common line 120A at a non-display area.

[0041] The common electrode 122 is provided within the pixel area to be connected to the internal common line 120A. More specifically, the common electrode 122 includes a horizontal part 122A overlapping with the drain electrode 112 adjacently with the gate line 102, and a finger part 122B extended from the horizontal part 122A into the pixel area to be connected to the internal common line 120A.

[0042] The pixel electrode 118 is provided such that the transparent conductive pattern 113 of the drain electrode 112 is extended to form a horizontal electric field along with the common electrode 122. More specifically, the pixel electrode 118 includes a horizontal part 118a overlapping with the horizontal part 122A of the common electrode 122 with having the gate insulating film 152 there between, and a finger part 118B extended from the horizontal part 118a in such a manner to have a finger shape parallel to the finger part 122B of the common electrode 122. Herein, the finger part 118A of the pixel electrode 118 overlaps with a portion of the internal common line 120A. The pixel electrode 118 is formed of the transparent conductive pattern 113, so that it may contribute to an aperture ratio. If a video signal is applied, via the thin film transistor TFT, to the pixel electrode 118, then a horizontal electric field is formed between the pixel electrode 118 and the finger part 122B of the common electrode 122 supplied with the common voltage. Liquid crystal molecules arranged in the horizontal direction between the thin film transistor array substrate and the color filter array substrate by such a horizontal electric field is rotated due to a dielectric anisotropy. Transmittance of a light transmitting the pixel area is differentiated depending upon a rotation extent of the liquid crystal molecules, thereby implementing a gray level scale.

[0043] Further, the finger part 122B of the common electrode 122 and the pixel electrode 118 can be formed in a zigzag shape as illustrated in FIG. 4. In this case, the edge being adjacent to the data line 104 at the finger part 122B of the common electrode 122 can be formed in parallel to the

data line 104, or may be formed in a zigzag shape. Alternatively, the data line 104 may be formed in a zigzag shape along the finger part 122B of the adjacent common electrode 122.

[0044] The storage capacitor Cst is provided such that the first horizontal part 122A of the common electrode 122 overlaps with the horizontal part 118A of the pixel electrode 118 with having the gate insulating film 152 there between. Herein, the first horizontal part 118A of the pixel electrode 118 is provided in such a manner to be extended from the transparent conductive pattern 113 of the drain electrode 112 and overlap with the first horizontal part 122A of the common electrode 122 as widely as possible. Thus, a capacitance value of the storage capacitor Cst is increased by the wide overlapping area between the common electrode 122 and the pixel electrode 118, so that the storage capacitor Cst allows a video signal charged in the pixel electrode 118 to be stably maintained until the next signal is charged.

[0045] The gate line 102, the data line 104 and the common line 120 receive the corresponding driving signal, via the pad 124 connected to each of them, from the driving circuit. The pads 124 have the same structure. More specifically, the pad 124 includes a lower pad electrode 126, and an upper pad electrode 130 connected, via a first contact hole 128 passing through the gate insulating film 152, to the lower pad electrode 126. Herein, the lower pad electrode 126 has a double-layer structure in which the first and second gate metal layers 101 and 103 are built like the gate line 102 and the common line 120, whereas the upper pad electrode 130 has the transparent conductive pattern 113.

[0046] Thus, each of the gate line 102 and the common line 120 is connected, via the lower pad electrode 126 provided on the substrate 150 in the same structure, to the corresponding pad 124. On the other hand, the data line 104 provided on the gate insulating film 152 is connected, via a contact electrode 160, to a data link 135 extended from the corresponding lower pad electrode 126. Herein, the contact electrode 160 is extended such that the transparent conductive pattern 113 of the data line 104 overlaps with the data link 135. The contact electrode 160 is connected, via a second contact hole 148 passing through the gate insulating film 152, to the data link 135. The contact electrode 160 is extended along the data link 135 to be integral to the corresponding upper pad electrode 130.

[0047] The protective film 154 includes the pixel electrode 118, the upper pad electrode 130 and the contact electrode 160. The protective film 154 borders with the transparent conductive patterns 113 included in the data line 104, the source electrode 110 and the drain electrode 122. This is because the protective film 154 is formed in a state in which the photo-resist pattern used upon formation of the transparent conductive pattern 113 is left and then is patterned by lifting-off the photo-resist pattern.

[0048] Accordingly, the thin film transistor substrate of horizontal electric field applying type according to the embodiment of the present invention having the above-mentioned structure is formed by the following three-round mask process.

[0049] FIG. 5A and FIG. 5B are a plan view and a section view illustrating a first mask process, respectively, in a method of fabricating the thin film transistor substrate of

horizontal electric field applying type according to the embodiment of the present invention.

[0050] A first mask pattern group including the gate line 102, the lower pad electrode 126, the data link 135, the common line 120 and the common electrode 122 is formed on the lower substrate 150 by the first mask process. Such a first mask pattern group has a multiple-layer structure in which at least two conductive layers are built. But, the sake of explanation, there will be described only a double-layer structure having the first and second gate metal layers 101 and 103 built.

[0051] More specifically, the first and second gate metal layers 101 and 103 are formed on the lower substrate 150 by a deposition technique such as the sputtering, etc. Each of the first and second gate metal layers 101 and 103 is made from a metal material such as Mo, Ti, Cu, Al, Cr, a Mo alloy, a Cu alloy or an Al alloy, etc. For example, a layer built structure of the first and second gate metal layers 101 and 103 employs Al/Cr, Al/Mo, Al(Nd)/Al, Al(Nd)/Cr, Cu/Mo, Mo/Al, Cu-alloy/Mo, Cu-alloy/Al, Cu-alloy/Mo-alloy, Cu-alloy/Al-alloy, Al/Mo alloy, Mo-alloy/Al, Al-alloy/Mo-alloy, Mo-alloy/Al-alloy or Mo/Al alloy, etc. Alternatively, it may employ a triple-layer built structure such as Ti/Al(Nd)/Ti or Mo/Ti/Al(Nd), etc.

[0052] Then, the first and second gate metal layers 101 and 103 are patterned by the photolithography and the etching process using a first mask to thereby provide the first mask pattern group including the gate line 102, the lower pad electrode 126, the data link 135, the common line 120 and the common electrode 122 each of which takes a double-layer structure.

[0053] FIG. 6A and FIG. 6B are a plan view and a section view illustrating a second mask process in a method of fabricating the thin film transistor substrate of horizontal electric field applying type according to the embodiment of the present invention, respectively, and FIG. 7A to FIG. 7F are section views for specifically explaining the second mask process.

[0054] The gate insulating film 152 having the first and second contact holes 124 and 128, the semiconductor pattern 115 and the source/drain pattern 111 are formed on the lower substrate 150 provided with the first mask pattern group by the second mask process. These are formed by a single mask process employing a diffractive exposure mask or a half tone mask. Hereinafter, a case where the half tone mask is used as a second mask will be described.

[0055] Referring to FIG. 7A, the gate insulating film 152, an amorphous silicon layer 105, an amorphous silicon layer 107 doped with an n^+ or p^+ impurity and a source/drain metal layer 109 are sequentially formed on the lower substrate 155 provided with the first mask pattern group by a deposition technique such as the PECVD, etc. Herein, the gate insulating film 152 is formed of an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x). The source/drain metal layer 109 employs a single layer formed of a metal material such as Mo, Ti, Cu, AlNd, Al, Cr, a Mo alloy, a Cu alloy or an Al alloy, etc., or employs a layer built structure of at least double layers such as Al/Cr, Al/Mo, Al(Nd)/Al, Al(Nd)/Cr, Mo/Al(Nd)/Mo, Cu/Mo, Ti/Al(Nd)/Ti, Mo/Al, Mo/Ti/Al(Nd), Cu-alloy/Mo, Cu-alloy/Al, Cu-alloy/Mo-alloy, Cu-alloy/Al-alloy, Al/Mo alloy,

Mo-alloy/Al, Al-alloy/Mo-alloy, Mo-alloy/Al-alloy, Mo/Al alloy, Cu/Mo alloy or Cu/Mo(Ti), etc.

[0056] Referring to FIG. 7B, a first photo-resist pattern 168 having step coverage is formed by the photolithography using the half tone mask. The half tone mask is comprised of a shielding part for shielding an ultraviolet ray, a half-tone transmitting part for partially transmitting the ultraviolet ray using a phase-shifting material, and a full transmitting part for fully transmitting the ultraviolet ray. The first photo-resist pattern 168 having a different thickness of photo-resist patterns 168A and 168B provided by the photolithography using the half tone mask; and the aperture part is provided. The relatively thick photo-resist pattern 168A is provided at a shielding area P1 of the first photo-resist overlapping with the shielding part of the half tone mask; the photo-resist pattern 168B thinner than the photo-resist pattern 168A is provided at a half-tone exposure part P2 overlapping with the half-tone transmitting part; and the aperture part is provided at a full exposure area P3 overlapping with the full transmitting part.

[0057] Referring to FIG. 7C, the first and second contact holes 124 and 148 passing through an area extended from the source/drain metal layer 109 until the gate insulating film 144 are formed by the etching process using a second photo-resist pattern 168 as a mask. The first contact hole 128 exposes the lower pad electrode 126, whereas the second contact hole 148 exposes the data link 135.

[0058] Referring to FIG. 7D, a thickness of the photo-resist pattern 168A is thinned and the photo-resist pattern 168B is removed by the ashing process using oxygen (O_2) plasma.

[0059] Referring to FIG. 7E, the source/drain metal layer 109, the amorphous silicon layer 107 doped with an impurity and the amorphous silicon layer 105 are patterned by the etching process using the ashed photo-resist pattern 168A as a mask, thereby providing the semiconductor pattern 115 having the active layer 114 and the ohmic contact layer 116 and the source/drain metal pattern 111 overlapped thereon.

[0060] Referring to FIG. 7F, the photo-resist pattern 168A left on the source/drain metal pattern 111 in FIG. 7E is removed by the stripping process.

[0061] Otherwise, a process of forming the first and second contact holes 128 and 148 and the semiconductor pattern 115 including the active layer 114 and the ohmic contact layer 116 using the first photo-resist pattern 168 as a mask may be replaced by a single of process.

[0062] FIG. 8A and FIG. 8B are a plan view and a section view illustrating a third mask process in a method of fabricating the thin film transistor substrate of horizontal electric field applying type according to the embodiment of the present invention, respectively, and FIG. 9A to FIG. 9E are section views for specifically explaining the third mask process.

[0063] A transparent conductive pattern 113 covering the source/drain metal pattern 111 and the protective film 154 making a border with the transparent conductive pattern 113 are formed by the third mask process. Thus, the data line 104, the source electrode 110 and drain electrode 112 having a double-layer structure in which the source/drain metal pattern 111 and the transparent conductive pattern 113 are

built are provided and, at the same time, the pixel electrode **118**, the upper pad electrode **130** and the contact electrode **160** having a single-layer structure of the transparent conductive pattern **113** are provided.

[0064] More specifically, as illustrated in **FIG. 9A**, a transparent conductive layer **117** is formed on the gate insulating film **152** provided with the source/drain metal pattern **111**. The transparent conductive layer **117** is formed from ITO, TO, IZO or ITZO, etc.

[0065] Referring to **FIG. 9B**, a photo-resist pattern **182** is formed on the transparent conductive layer **117** by the photolithography using a third mask.

[0066] Referring to **FIG. 9C**, the transparent conductive layer **117** is patterned by an etching process using the photo-resist pattern **182** as a mask, that is, a wet etching process to thereby provide the transparent conductive pattern **113** capturing the source/drain metal pattern **111**. At this time, the transparent conductive pattern **113** is opened at a portion to be provided with the channel of the thin film transistor TFT. Thus, the exposed source/drain metal pattern **111** and the ohmic contact layer **116** under it are removed by an etching process using the transparent conductive pattern **113** as a mask, that is, a dry etching process, thereby allowing the active layer **114** to have an exposed structure. As a result, the data line **104**, the source electrode **110** and the drain electrode **112** having a double-layer structure are provided. Further, the pixel electrode **118** extended from the transparent conductive pattern **113** of the drain electrode **112** and the contact electrode **160** extended from the transparent conductive pattern **113** of the data line **104** are provided and, at the same time, the upper pad electrode **130** connected to the lower pad electrode **126** is provided. The transparent conductive pattern **113** is over-etched in comparison with the photo-resist pattern **182**.

[0067] Referring to **FIG. 9D**, the protective film **154** covering the photo-resist pattern **182** is entirely formed. In this case, the protective film **154** provided at the substrate in which the photo-resist pattern **182** does not exist has a structure opened with respect to the protective film **154** provided at the photo-resist pattern **182** by a spaced distance between the edge of the photo-resist pattern **182** and the edge of the transparent conductive pattern **113**. Thus, an infiltration of a stripper into a portion between the photo-resist pattern **182** and the transparent conductive pattern **113** is facilitated at the next lift-off process, thereby improving lift-off efficiency. The protective film **154** is formed from an inorganic insulating material like the gate insulating film **144**. Such a protective film **154** is formed by a deposition technique such as the PECVD or the sputtering, etc. But, it is desirable that the protective film **154** is formed by the sputtering in order to prevent a hardness of the photo-resist pattern **182** at a high temperature. Alternatively, the protective film **154** may be formed from an organic insulating material such as an acrylic organic compound, BCB or PFCB, etc.

[0068] Referring to **FIG. 9E**, the photo-resist pattern **182** illustrated in **FIG. 9D** and the protective film **154** provided thereon are removed by the lift-off process to thereby pattern the protective film **154**. The patterned protective film **154** makes a border with the transparent conductive pattern **113**. In other words, the protective film **154** making a border with

the transparent conductive pattern **113** is left at the remaining area other than an area provided with the transparent conductive pattern **113**.

[0069] Accordingly, a channel length L of the thin film transistor TFT is determined by the transparent conductive pattern **113**. Furthermore, a smoothing is possible in accordance with a thickness of the transparent conductive pattern **113**, so that it becomes possible to prevent a rubbing badness upon an alignment treatment process such as the rubbing, etc. after forming the alignment film.

[0070] As described above, according to the present invention, the semiconductor pattern and the source/drain metal pattern, along with the contact hole, are formed by utilizing a half tone (or diffractive exposure) mask in the second mask process.

[0071] Also, according to the present invention, the transparent conductive pattern is formed and the protective film is patterned by lifting off the photo-resist pattern used upon formation of the transparent conductive pattern in the third mask process. Such transparent conductive pattern and protective film protects the metal layer at the lower portion thereof, thereby preventing an illumination problem.

[0072] As a result, according to the present invention, a process can be simplified by the three-round mask process, so that it becomes possible to reduce the material cost and the equipment investment cost, etc. as well as to improve the productivity.

[0073] Furthermore, according to the present invention, the pixel electrode is formed from the transparent conductive pattern, so that it becomes possible to improve an aperture ratio.

[0074] Although the present invention has been explained by the embodiments illustrated in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display device, comprising:

- a gate line on a substrate;
- a data line crossing the gate line having a gate insulating film there between to define a pixel area;
- a thin film transistor including a gate electrode, a source electrode, a drain electrode and a semiconductor layer to define a channel between the source electrode and the drain electrode;
- a common line on the substrate;
- a common electrode in the pixel area; and
- a pixel electrode in the pixel area to form a horizontal electrode field with the common electrode,

wherein the data line, the source electrode and the drain electrode have an opaque conductive pattern and a transparent conductive pattern, the pixel electrode is formed by an extension of the transparent conductive

pattern of the drain electrode, and a protective film borders with the transparent conductive pattern and in the remaining area thereof.

2. The liquid crystal display device as claimed in claim 1, further comprising:

a storage capacitor provided such that the pixel electrode overlaps with a portion of the common electrode having the gate insulating film there between.

3. The liquid crystal display device as claimed in claim 1, wherein the gate line, the gate electrode, the common line and the common electrode includes one of a single-layer structure formed of one of Mo, Ti, Cu, AlNd, Al, Cr, a Mo alloy, a Cu alloy and an Al alloy, and a multiple-layer structure having at least two layers thereof.

4. The liquid crystal display device as claimed in claim 1, further comprising:

a pad connected to the gate line, the common line and the data line,

wherein the pad includes:

a lower pad electrode on the substrate with the gate line and the common line;

a contact hole passing through the gate insulating film to expose the lower pad electrode; and

an upper pad electrode connected to the lower data pad electrode via said contact hole and formed of the transparent conductive pattern.

5. The liquid crystal display device as claimed in claim 4, further comprising:

a data link extended from the lower pad electrode of the data pad;

a second contact hole passing through the gate insulating film to expose the data link; and

a contact electrode extended from the transparent conductive pattern of the data line to be connected to the data link via the second contact hole.

6. The liquid crystal display device as claimed in claim 5, wherein the contact electrode is integral to the upper pad electrode.

7. The liquid crystal display device as claimed in claim 5, wherein the transparent conductive pattern encloses the opaque conductive pattern.

8. The liquid crystal display device as claimed in claim 1, wherein the opaque conductive pattern includes one of a single-layer structure formed of one of Mo, Ti, Cu, AlNd, Al, Cr, a Mo alloy, a Cu alloy and an Al alloy, and a multiple-layer structure having at least two layers thereof.

9. The liquid crystal display device as claimed in claim 5, wherein the upper pad electrode and the contact electrode borders with the protective film.

10. The liquid crystal display device as claimed in claim 1, wherein the common line is parallel to the gate line.

11. The liquid crystal display device as claimed in claim 1, wherein the pixel electrode extends from the drain electrode.

12. A method of fabricating a liquid crystal display device, comprising:

a first mask process of forming a first mask pattern group including a gate line, a gate electrode, a common line and a common electrode on a substrate;

a second mask process of forming a gate insulating film on the first mask pattern group and a semiconductor pattern and an opaque conductive pattern on the gate insulating film; and

a third mask process of forming a transparent conductive pattern on the opaque conductive pattern and forming a protective film having a border with the transparent conductive pattern,

wherein a data line crossing the gate line, a source electrode and a drain electrode are formed of a double-layer structure having the opaque conductive pattern and the transparent conductive pattern, and a pixel electrode is extended from the transparent conductive pattern of the drain electrode to form a horizontal electric field with the common electrode.

13. The method as claimed in claim 12, wherein:

the first mask process further includes forming a lower pad electrode to be connected to at least one of the gate line, the data line and the common line,

the second mask process further includes forming a contact hole passing through the gate insulating film to expose the lower pad electrode, and

the third mask process further includes forming an upper pad electrode to be connected to the lower pad electrode via the contact hole, from the upper pad electrode being formed of the transparent conductive pattern.

14. The method as claimed in claim 12, wherein:

the first mask process includes forming a data link extended from the lower pad electrode to be connected to the data line,

the second mask process includes forming a second contact hole to expose the data link, and

the third mask process includes forming a contact electrode extended from the transparent conductive pattern of the data line to be connected to the data link via the second contact hole.

15. The method as claimed in claim 14, wherein the contact electrode is integral to the upper pad electrode.

16. The method as claimed in claim 14, wherein the upper pad electrode and the contact electrode borders with the protective film.

17. The method as claimed in claim 14, wherein the gate line, the gate electrode, the common line, the common electrode, the lower pad electrode and the data link include one of a single-layer structure formed of one of Mo, Ti, Cu, AlNd, Al, Cr, a Mo alloy, a Cu alloy and an Al alloy, and a multiple-layer structure having at least two layers thereof.

18. The method as claimed in claim 12, wherein the transparent conductive pattern encloses the opaque conductive pattern.

19. The method as claimed in claim 14, wherein the second mask process includes:

substantially sequentially forming a gate insulating film covering the first mask pattern group, an amorphous silicon layer, an amorphous silicon layer doped with an impurity and an opaque conductive layer;

forming photo-resist patterns having a different thickness by a photolithography using at least one of a half tone mask and a diffractive exposure mask; and

forming first and second contact holes passing through the opaque conductive layer and the gate insulating film, the opaque conductive pattern, and the semiconductor pattern having an active layer and an ohmic contact layer by an etching process using the photo-resist pattern.

20. The method as claimed in claim 12, wherein the third mask process includes:

forming a transparent conductive layer on the gate insulating film;

forming a photo-resist pattern by the photolithography;

forming the transparent conductive pattern by an etching process using the photo-resist pattern as a mask;

removing the opaque conductive pattern and an ohmic contact layer exposed through the transparent conductive pattern;

substantially entirely forming a protective film covering the photo-resist pattern; and

removing the photo-resist pattern with the protective film.

21. The method as claimed in claim 20, wherein the protective film is formed using a sputtering.

22. The method as claimed in claim 20, wherein the transparent conductive pattern is over-etched than the photo-resist pattern.

23. The method as claimed in claim 12, further comprising:

forming a storage capacitor such that the pixel electrode overlaps with a portion of the common electrode having the gate insulating film there between.

* * * * *

专利名称(译)	液晶显示装置及其制造方法		
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当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	AHN BYUNG CHUL LIM JOO SOO PARK BYUNG HO		
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摘要(译)

公开了一种用于施加水平电场的薄膜晶体管基板及其制造方法，以简化工艺。在根据本发明的液晶显示装置中，基板上的栅极线;与栅极线交叉的数据线，其间具有栅极绝缘膜以限定像素区域;薄膜晶体管，包括栅电极，源电极，漏电极和半导体层，以限定源电极和漏电极之间的沟道;基板上的公共线;像素区域中的公共电极;像素区域中的像素电极与公共电极形成水平电极场，其中数据线，源电极和漏电极具有不透明导电图案和透明导电图案，像素电极由延伸形成漏电极的透明导电图案和保护膜与透明导电图案相邻并在其余区域中。

