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(54) METHOD AND APPARATUS FOR PREVENTING RESIDUAL IMAGE IN LIQUID CRYSTAL DISPLAY

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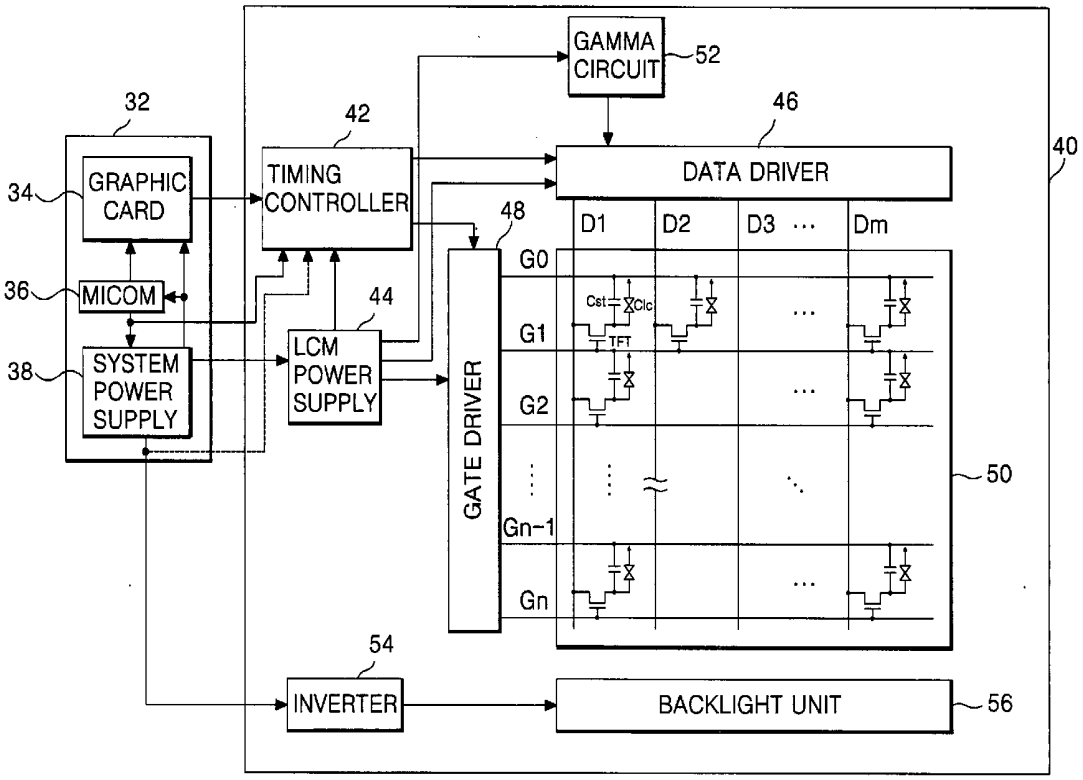
(57) **ABSTRACT**

An adaptive method and apparatus prevents the formation of residual images in a liquid crystal display caused by a discharge of liquid crystal cells upon power-off. When an off-time of a ramp voltage is sensed, a white data signal may be generated. The white data signal is then displayed on a liquid crystal display panel until a power supply for the liquid crystal module is turned off.



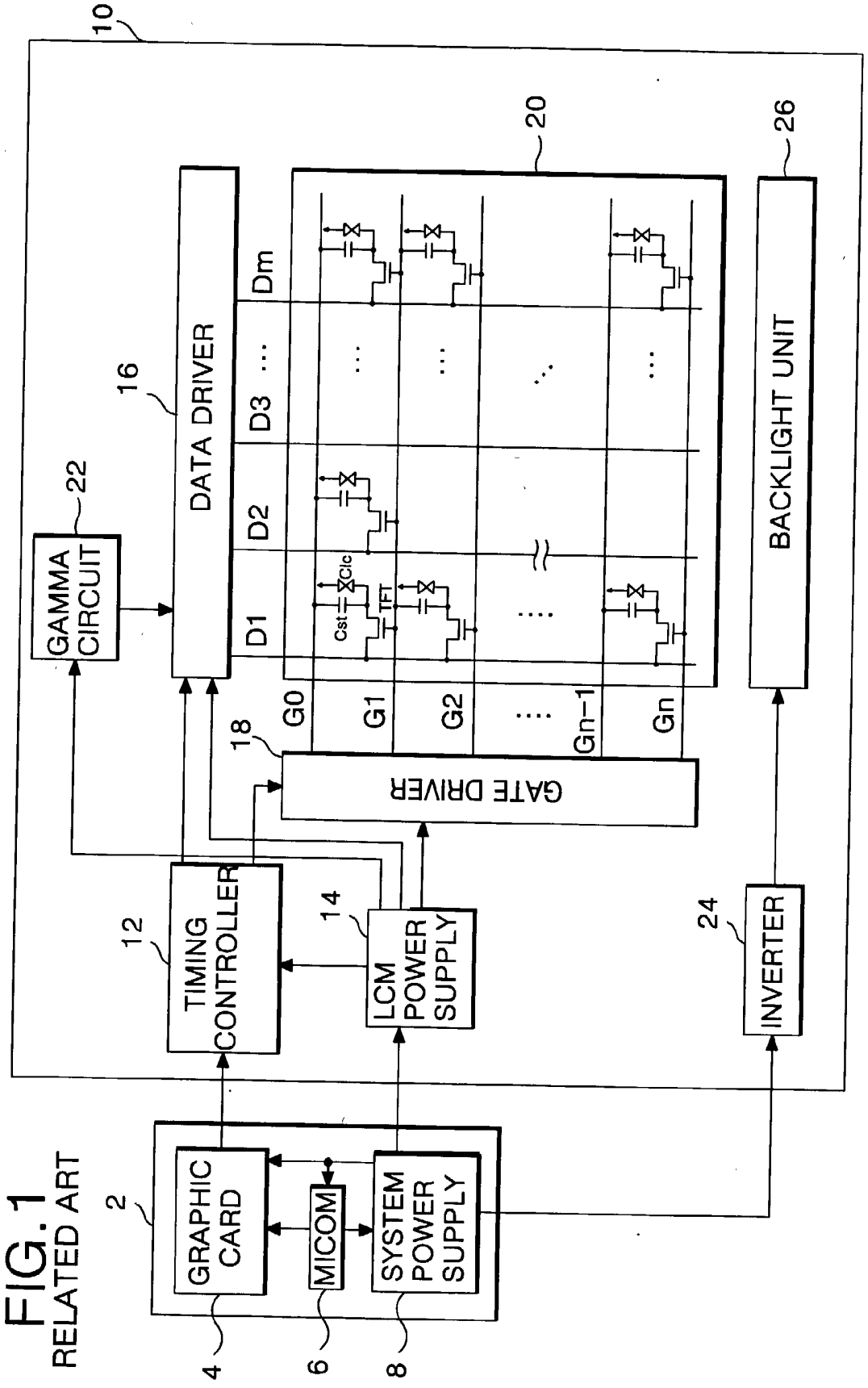
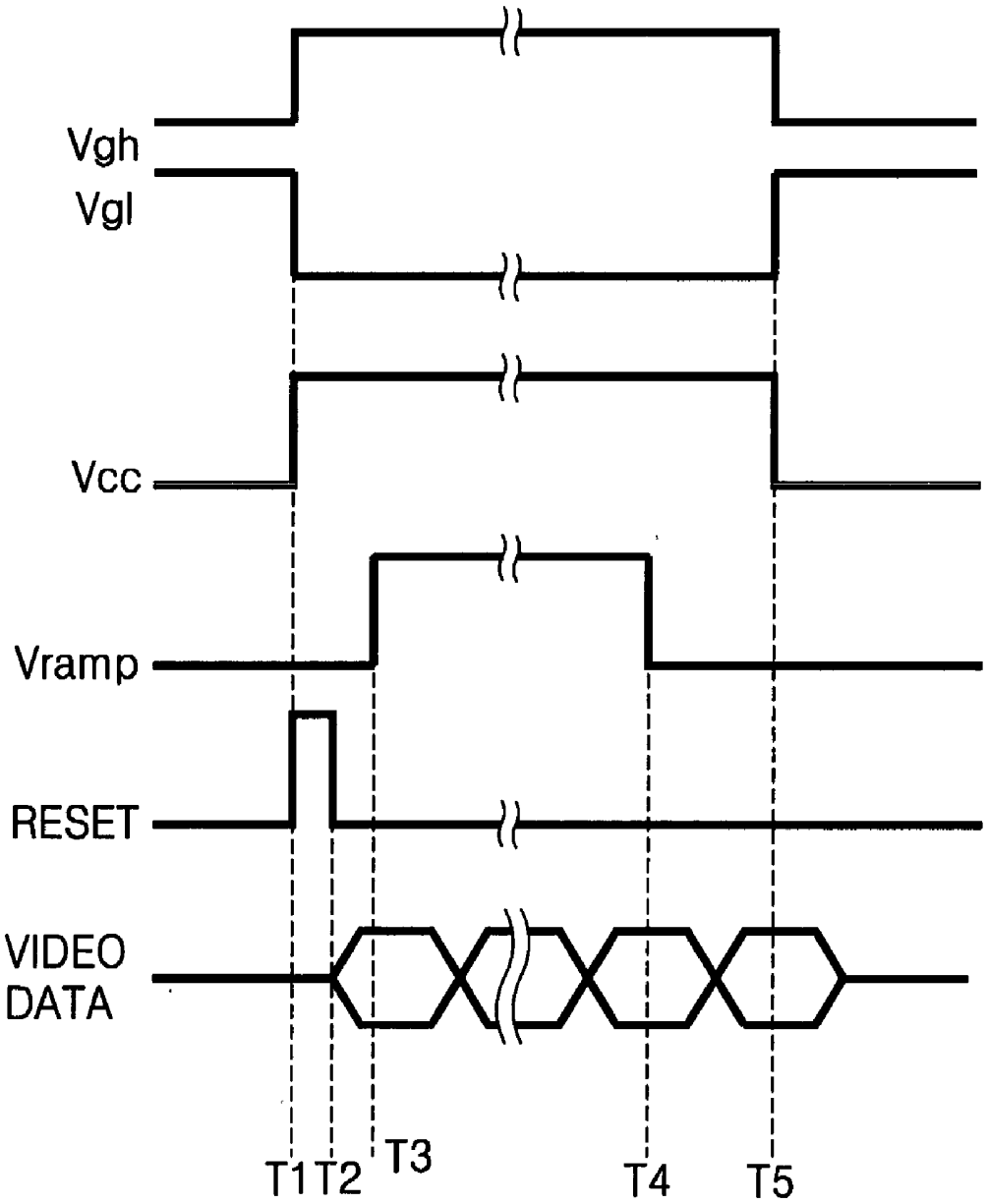


FIG. 1
RELATED ART

FIG. 2
RELATED ART



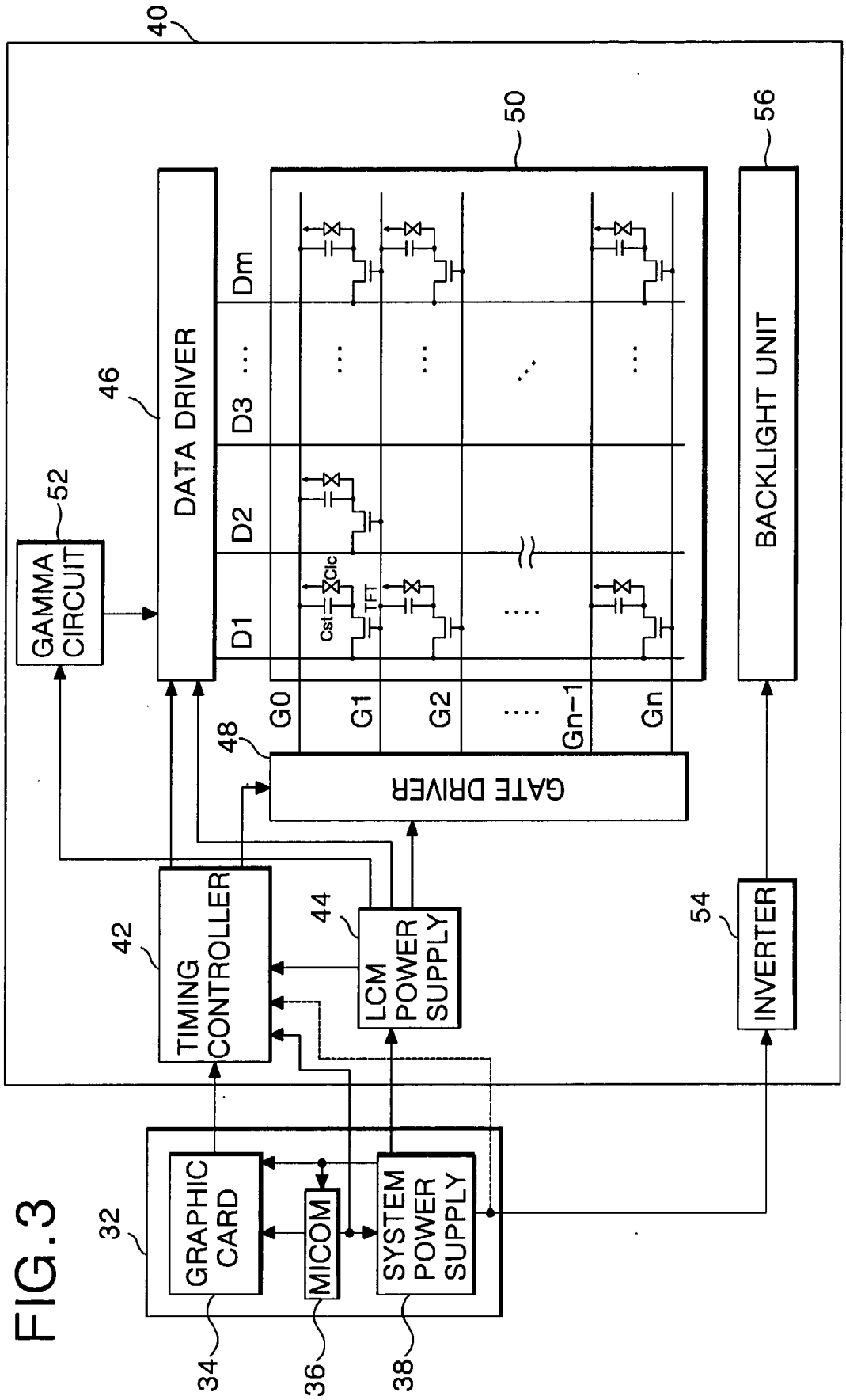

40
50
56
46
52
DATA DRIVER
GAMMA CIRCUIT
BACKLIGHT UNIT
Dm
D3
D2
D1
Clc
Cst
TFT
G0
G1
G2
Gn-1
Gn
48
GATE DRIVER
42
TIMING CONTROLLER
44
LCM POWER SUPPLY
54
INVERTER
32
GRAPHIC CARD
MICOM
SYSTEM POWER SUPPLY
34
36
38

FIG.3

FIG.4

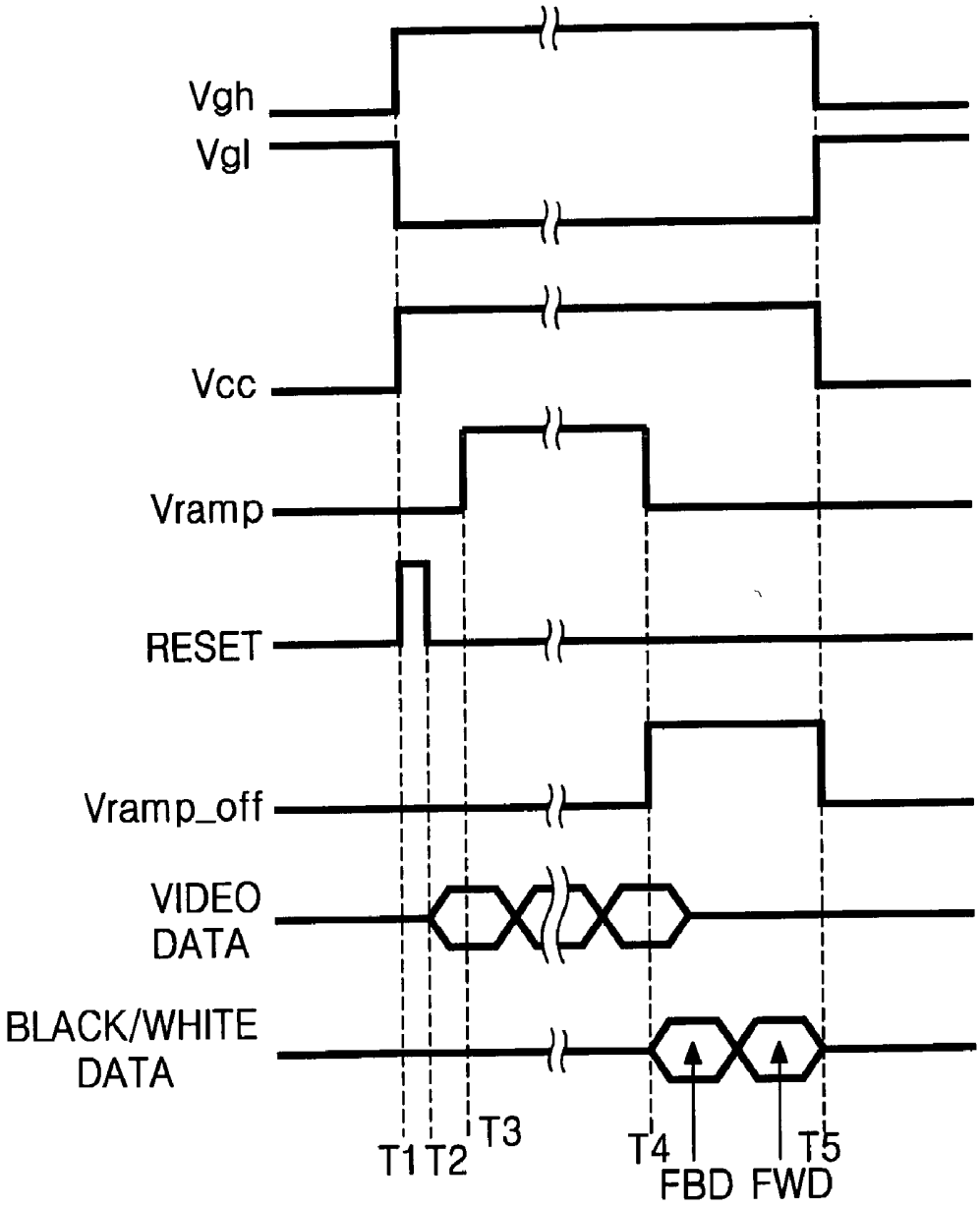

Vgh
Vgl
Vcc
Vramp
RESET
Vramp_off
VIDEO DATA
BLACK/WHITE DATA
T1
T2
T3
T4
T5
FBD
FWD

FIG.5

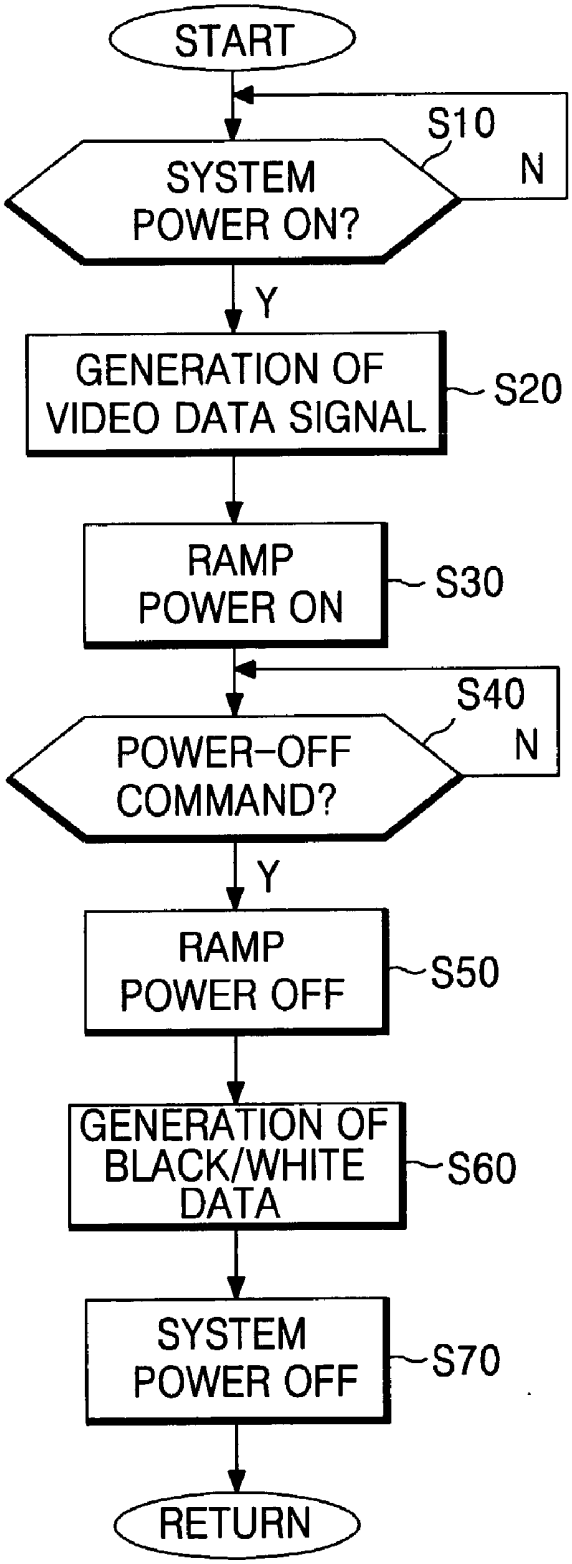
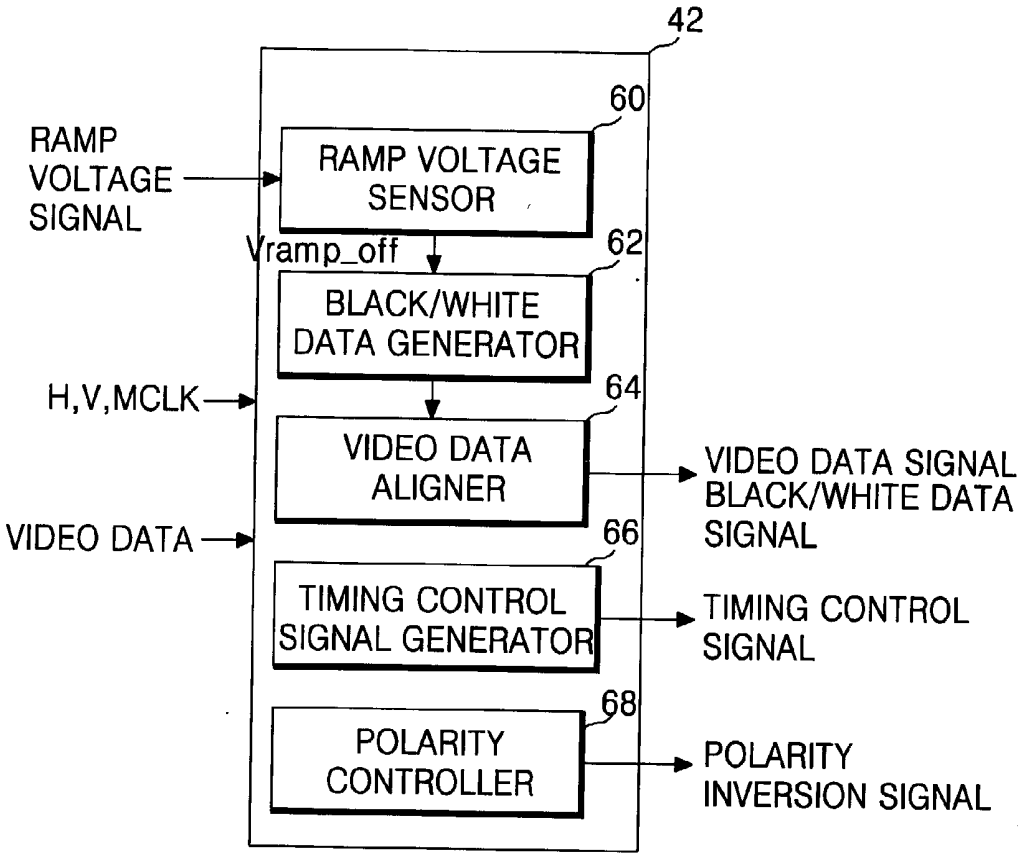

START
S10
SYSTEM POWER ON?
N
Y
GENERATION OF VIDEO DATA SIGNAL
S20
RAMP POWER ON
S30
S40
POWER-OFF COMMAND?
N
Y
RAMP POWER OFF
S50
GENERATION OF BLACK/WHITE DATA
S60
SYSTEM POWER OFF
S70
RETURN

FIG.6


42
60
RAMP VOLTAGE SENSOR
RAMP VOLTAGE SIGNAL
Vramp_off
62
BLACK/WHITE DATA GENERATOR
H,V,MCLK
64
VIDEO DATA ALIGNER
VIDEO DATA SIGNAL BLACK/WHITE DATA SIGNAL
VIDEO DATA
66
TIMING CONTROL SIGNAL GENERATOR
TIMING CONTROL SIGNAL
68
POLARITY CONTROLLER
POLARITY INVERSION SIGNAL

METHOD AND APPARATUS FOR PREVENTING RESIDUAL IMAGE IN LIQUID CRYSTAL DISPLAY

[0001] This application claims the benefit of Korean Patent Application No. 2002-18893, filed on Apr. 8, 2002, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to liquid crystal displays, and more particularly to an adaptive method and apparatus for preventing the formation of residual images in liquid crystal displays upon powering off.

[0004] 2. Discussion of the Related Art

[0005] Generally, liquid crystal displays (LCDs) display pictures using electric fields to control the light transmittance of a liquid crystal. To this end, LCDs include a liquid crystal display panel for supporting a pixel matrix and a driving circuit for driving the liquid crystal display panel.

[0006] Referring to **FIG. 1**, LCDs generally include a liquid crystal module **10** for displaying a picture in response to video data signals inputted from a system part **2**.

[0007] System part **2** includes a graphic card **4** for supplying signals (e.g., video data, etc.) suitable for driving the liquid crystal module **10**, a system power supply **8** for supplying power, and a microcomputer **6** for controlling the system power supply **8**.

[0008] The graphic card **4** converts inputted video data signals according to a resolution specific for a liquid crystal display panel **20**, applies the converted video data signals to the liquid crystal module **10**, and generates control signals (e.g., a main clock signal, a vertical synchronizing signal a horizontal synchronizing signal, etc.) specific to the resolution of the liquid crystal display panel **20**.

[0009] The system power supply **8** supplies a driving voltage required to operate the graphic card **4** and the microcomputer **6**. The supplied driving voltage is subsequently applied to a liquid crystal module (LCM) power supply **14** and inverter **24** included within the liquid crystal module **10**.

[0010] The microcomputer **6** controls the system power supply **8** in accordance with a user command inputted through a power switch (not shown). The microcomputer **6** controls the amount of power applied to the LCM power supply **14** and a ramp power applied to the inverter **24** via the system power supply **8**. For example, through the system power supply **8**, the microcomputer **6** controls the time during which power is applied to the LCM power supply **14** and the time during which ramp power is applied to the inverter **24**. Typically, the system power supply **8** is activated over the same time period during which the LCM power supply **14** is activated while the system power supply **8** is activated over a different time period during which the inverter **24** is activated. For example, inverter **24** is activated after the system power supply **8** is activated and is deactivated before the system power supply **8** is deactivated. Accordingly, an off-time of the inverter **24** occurs at an earlier point in time compared to the off-time of the system power supply **8**.

[0011] The liquid crystal module **10** includes the liquid crystal display panel **20** for supporting liquid crystal cells, a data driver **16** for driving data lines D1 to Dm included in the liquid crystal display panel **20**, a gate driver **18** for driving gate lines G0 to Gn included in the liquid crystal display panel **20**, a timing controller **12** for controlling a driving time of the data and gate drivers **16** and **18**, respectively, the LCM power supply **14** for generating driving voltages required for driving the liquid crystal display **10**, a gamma circuit **22** for supplying gamma voltages to the data driver **16**, a backlight unit **26** for providing light required to display pictures on the liquid crystal display panel **20**, and an inverter **24** for supplying a driving voltage to the backlight unit **26**.

[0012] Using a voltage received from the system power supply **8**, the LCM power supply **14** generates driving voltages (e.g., a base driving voltage Vcc, a gate high voltage Vgh, a gate low voltage Vgl, a gamma reference voltage, a common voltage, etc.) required to drive the liquid crystal module **10**. Accordingly, the generated driving voltages are applied to the timing controller **12**, the data driver **16**, the gate driver **18**, and the gamma circuit **22**.

[0013] The timing controller **12** accepts video data signals (e.g., R, G, and B) outputted from the graphic card **4** and applies the accepted video data signals to the data driver **16**. Further, the timing controller **12** accepts a control signal outputted from the graphic card **4** and generates timing signals to control the timing of the data and gate drivers **16** and **18**, respectively. Additionally, the timing controller **12** generates other control signals (e.g., polarity inversion signal, etc.).

[0014] The liquid crystal display panel **20** includes liquid crystal cells, arranged in a matrix pattern, connected to thin film transistors (TFTs). Each of the TFTs are provided at intersections of gate lines G1 to Gn and data lines D1 to Dm. The TFTs respond to gate signals applied from gate lines GI to Gn and receive video signals applied from the data lines D1 to Dm. Each liquid crystal cell consists of a pixel electrode connected to an opposing common electrode via a liquid crystal and TFT. Accordingly, each liquid crystal cell may be equivalently expressed as a liquid crystal capacitor Clc. Such liquid crystal cells include a storage capacitor Cst connected to a pre-stage gate line in order to sustain data voltages charged within the liquid crystal capacitor Clc until subsequent data voltages are charged.

[0015] In response to a control signal outputted from the timing controller **12**, the gate driver **18** sequentially applies a gate high voltage signal to gate lines G1 to Gn. The data driver **16** converts the video data signals outputted from the timing controller **12** into analog video voltage signals and applies analog video voltage signals, specific to one horizontal line, to data lines D1 to Dn for each horizontal period during which a gate high voltage signal is applied to the gate lines G1 to Gn. The gamma circuit **22** applies a predetermined gamma voltage to the data driver **16** in accordance with voltage levels associated with the analog video voltage signals. Thus, the data driver **16** uses gamma voltages supplied from the gamma circuit **22** to convert the video data signals outputted from the timing controller **12** into analog video voltage signals.

[0016] The inverter **24** converts a driving voltage inputted from the system power supply **8** into a high alternating

current voltage corresponding to a lamp luminance of the backlight unit **26**. The backlight unit **26** is provided at a rear side of the liquid crystal display panel **20** and supplies light suitable for displaying a picture. Accordingly, the backlight unit **26** includes lamp arranged within a lamp housing, a light guide for guiding light emitted from the lamp toward a surface of the liquid crystal panel, optical sheets attached to the light guide to enhance desirable lighting properties, and a reflector attached to a rear side of the light guide.

[**0017**] Referring to **FIG. 2, a** method for driving the liquid crystal display illustrated in **FIG. 1** will now be described.

[**0018**] At time T1, if a 'power-on' command is inputted by a user, the microcomputer **6** turns the system power supply **8** on such that a driving voltage is applied to the LCM power supply **14**. In turn, the LCM power supply **14** generates driving voltages (e.g., a base driving voltage Vcc, a gate high voltage Vgh, a gate low voltage Vgl, etc.) required to drive the liquid crystal module **10**.

[**0019**] Simultaneously, at T1, if a reset signal (RESET) is generated from the microcomputer **6**, the graphic card **4** generates video data signals at time T2 and applies the generated video data signals to the liquid crystal module **10**. Using the driving voltages generated by the LCM power supply **14**, the liquid crystal module **10** applies video data signals generated by the graphic card **4** to the liquid crystal display panel **20**.

[**0020**] Subsequently, at time T3, the microcomputer **6** allows a ramp voltage (Vramp) to be applied to the inverter **24** via the system power supply **6**. As the lamp is activated by the ramp voltage (Vramp) outputted by the inverter **24**, the backlight unit **26** emits light into the liquid crystal display panel **20**. Thus, the liquid crystal display panel **20** controls a transmittance of the light emitted from the backlight unit **26** in accordance with inputted video data signals, to display a picture.

[**0021**] A driving operation of the liquid crystal display panel **20** will now be described.

[**0022**] As the TFT is turned on by a gate high voltage Vgh applied to a gate line G, a video voltage signal, applied to the data lines D1 to Dm, is charged within the liquid crystal capacitor Clc. As the TFT is turned off by a gate low voltage Vgl applied to the gate line G, the video voltage signal remains charged within the liquid crystal capacitor Clc until the next data voltage signal is applied. Accordingly, the storage capacitor Cst connected to the liquid crystal capacitor Clc, in parallel, is charged with a data voltage signal when a gate high voltage Vgh is applied to a pre-stage gate line Gi-1. When a gate low voltage Vgl is applied, a higher voltage than the data voltage signal charged in the liquid crystal capacitor Clc is maintained during a turn-off interval of the thin film transistor. Thus, since the storage capacitor Cst applies electric charges to the liquid crystal capacitor Clc during a turn-off interval of the TFT, the variation in the voltage charged within the liquid crystal capacitor Clc is minimized.

[**0023**] At time T4, a power-off command is inputted from a user and the microcomputer **6** shuts off the ramp voltage applied to the inverter **24**, via the system power supply **8**. At time T5, the microcomputer **6** turns the system power supply **8** and the LCM power supply **14** off.

[**0024**] If the system power supply **8** is turned off, a problem occurs in that a video voltage charged within each liquid crystal cell of the liquid crystal display panel **20** slowly discharges through a leakage current of the TFT. This slow discharge causes residual images to be displayed by the liquid crystal display panel **20**.

[**0025**] In order to eliminate residual images generated upon power-off, a separate discharge circuit may be provided to discharge voltages charged within each of the liquid crystal cells. For instance, a discharge circuit so provided may monitor a power-off event and apply a ground voltage to the gate lines to turn the TFTs on. Thus, the discharge circuit rapidly discharges voltages charged in each liquid crystal cell to eliminate residual images. However, as such discharge circuits must be provided at each gate line, the structure of the liquid crystal display panel becomes complex. Furthermore, when discharge circuits are applied to dot or line inversion liquid crystal modules, TFTs are turned on in liquid crystal cells having a negative voltage lower than the ground voltage applied to the gate electrode and thereby perform the compulsory discharge. On the other hand, TFTs are turned off in liquid crystal cells having positive voltage higher than the ground voltage and thereby do not perform the compulsory discharge. Accordingly, residual images still exist in dot or line inversion liquid crystal modules. Moreover, voltages charged in the liquid crystal cells employing the above discharge circuit are compulsorily discharged because are not sufficient to eliminate residual images because a certain discharge time exists.

SUMMARY OF THE INVENTION

[**0026**] Accordingly, the present invention is directed to a method and apparatus for preventing residual images in liquid crystal displays that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[**0027**] Accordingly, an advantage of the present invention provides an adaptive method and apparatus for preventing residual images from forming in liquid crystal displays caused by the discharge of a liquid crystal cell upon power-off.

[**0028**] In order to achieve these and other advantages of the invention, a method of preventing the formation of residual images in liquid crystal displays, according to one aspect of the present invention, includes the steps of sensing an off-time of a ramp voltage to generate a white data signal and displaying the white data signal on a liquid crystal display panel until a power supply included within a liquid crystal module is turned off.

[**0029**] In one aspect of the present invention, the white data signal may be displayed on the liquid crystal display panel during at least one frame.

[**0030**] In another aspect of the present invention, a black data signal may be generated one frame prior to generation of the white data signal.

[**0031**] In yet another aspect of the present invention, an off-time of the ramp voltage may be sensed using a ramp voltage control signal applied from a microcomputer of a system driving the liquid crystal module to a system power supply when a power-off command is inputted from a user.

[0032] In still another aspect of the present invention, an off-time of the ramp voltage may be sensed using a ramp voltage outputted from the system power supply of the system driving the liquid crystal module when the power-off command is inputted from the user.

[0033] In accordance with the principles of the present invention, a residual image prevention apparatus for a liquid crystal display includes a liquid crystal module having a liquid crystal display panel for displaying a picture; a signal line driving circuit for driving signal lines of the liquid crystal display panel; a timing controller for controlling a driving time of the signal line driving circuit and for applying a data signal; a liquid crystal module power supply for supplying driving voltages required for driving the liquid crystal display panel; the signal line driving circuit, and the timing controller; a backlight unit for providing the liquid crystal display panel with light required to display the picture; a ramp driver for applying a ramp driving voltage to the backlight unit; and a system part for driving and controlling the liquid crystal module, wherein the timing controller may generate a white data signal when an off-time of the ramp voltage is applied to the ramp driver from the system part such that white data signal is displayed on the liquid crystal display panel.

[0034] In one aspect of the present invention, the residual image prevention apparatus, said system part may further include a system power supply for supplying a liquid crystal module voltage to a power supply of the liquid crystal module and supplying said ramp voltage to the ramp driver; a microcomputer for controlling the system power supply such that the power supply of the liquid crystal module and the ramp driver are activated during a different times; and a graphic card for applying the data signal and other control signals to the timing controller.

[0035] In another aspect of the present invention, the timing controller senses an off-time of the ramp voltage using a ramp voltage control signal applied from the microcomputer to the system power supply.

[0036] In yet another aspect of the present invention, the system part may further include a ramp voltage sensor for sensing an off-time of the ramp voltage to thereby generate a ramp voltage off signal; a white data signal generator for generating the white data signal in response to the ramp voltage off signal; a timing control signal generator for generating control signals controlling a driving time of a signal line driving integrated circuit using input control signals; and a data aligner for aligning and outputting an input data signal and the white data signal.

[0037] In still another aspect of the present invention, the timing controller may generate a black data signal for at least one frame prior to generating the white data signal when said off-time of the ramp voltage is sensed, thereby displaying the black data signal on the liquid crystal display panel.

[0038] The timing controller may allow the white data signal to be displayed on the liquid crystal display panel during at least one frame.

[0039] In another aspect of the present invention, the timing controller may generate the white data signal from the off-time of the ramp voltage until the power supply of the liquid crystal module is turned off, thereby displaying said white data signal on the liquid crystal display panel.

[0040] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0041] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0042] In the drawings:

[0043] **FIG. 1** illustrates a block diagram showing a configuration of a related liquid crystal display;

[0044] **FIG. 2** illustrates a waveform diagram of an input voltage applied to each liquid crystal element of the liquid crystal display shown in **FIG. 1**;

[0045] **FIG. 3** illustrates a block diagram showing a configuration of a residual image prevention apparatus for a liquid crystal display according to an embodiment of the present invention;

[0046] **FIG. 4** illustrates a waveform diagram of an input voltage applied to each liquid crystal element of the liquid crystal display shown in **FIG. 3**;

[0047] **FIG. 5** illustrates a flow chart of a method for preventing a residual image in a liquid crystal display according to an embodiment of the present invention; and

[0048] **FIG. 6** illustrates a block diagram showing a detailed configuration of the timing controller shown in **FIG. 3**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0049] Reference will now be made in detail to an embodiment of the present invention, example of which is illustrated in the accompanying drawings.

[0050] **FIG. 3** illustrates a block diagram showing a configuration of a residual image prevention apparatus for a liquid crystal display according to an embodiment of the present invention.

[0051] Referring to **FIG. 3**, the LCD according to the principles of the present invention may, for example, include a liquid crystal module **40** for displaying a picture in response to video data signals inputted from a system part **32**.

[0052] System part **32** may, for example, include a graphic card **34** for supplying signals (e.g., video data, etc.) suitable for driving the liquid crystal module **40**, a system power supply **38** for supplying power, and a microcomputer **36** for controlling the system power supply **38**.

[0053] The graphic card **34** converts inputted video data signals according to a resolution specific for a liquid crystal display panel **50**, applies the converted video data signals to the liquid crystal module **40**, and generates control signals (e.g., a main clock signal, a vertical synchronizing signal, a horizontal synchronizing signal, etc.) specific to the resolution of the liquid crystal display panel **50**.

[0054] The system power supply **38** supplies a driving voltage required to operate the graphic card **34** and the microcomputer **36**. The supplied driving voltage is subsequently applied to a liquid crystal module (LCM) power supply **44** and inverter **54** included within the liquid crystal module **40**.

[0055] The microcomputer **36** controls the system power supply **38** in accordance with a user command inputted through a power switch (not shown). The microcomputer **36** controls the amount of power applied to the LCM power supply **44** and a ramp voltage applied to the inverter **54** via the system power supply **38**. For example, through the system power supply **38**, microcomputer **36** controls the time during which power is applied to the LCM power supply **44** and the time during which ramp power is applied to the inverter **54**. In one aspect of the present invention, the system power supply **38** is activated over the same time period during which the LCM power supply **44** is activated while the system power supply **38** is activated over a different time period during which the inverter **54** is activated. For example, inverter **54** may be activated after the system power supply **38** may be activated after the system power supply **8** is activated and may be deactivated before the system power supply **38** is deactivated. Accordingly, an off-time of the inverter **54** occurs at an earlier point in time compared to the off-time of the system power supply **38**.

[0056] The liquid crystal module **40** may, for example, include the liquid crystal display panel **50** for supporting liquid crystal cells, a data driver **46** for driving data lines D1 to Dm included in the liquid crystal display panel **50**, a gate driver **48** for driving gate lines G0 to Gn included in the liquid crystal display panel **50**, a timing controller **42** for controlling a driving time of the data and gate drivers **46** and **48**, respectively, the LCM power supply **44** for generating driving voltages required for driving the liquid crystal module **40**, a gamma circuit **52** for supplying gamma voltages to the data driver **46**, a backlight unit **56** for providing light required to display pictures on the liquid crystal display panel **50**, and an inverter **54** for supplying a driving voltage to the backlight unit **56**.

[0057] Using a voltage received from the system power supply **38**, the LCM power supply **44** generates driving voltages (e.g., a base driving voltage Vcc, a gate high voltage Vgh, a gate low voltage Vgl, a gamma reference voltage, a common voltage, etc.) required to drive the liquid crystal module **40**. Accordingly, the generated driving voltages may be applied to the timing controller **42**, the data driver **46**, the gate driver **48**, and the gamma circuit **52**.

[0058] The timing controller **42** accepts video data signals (e.g., R, G, and B) outputted from the graphic card **34** and applies the accepted video data signals to the data driver **46**. Further, the timing controller **42** accepts a control signal outputted from the graphic card **34** and generates timing signals to control the timing of the data and gate drivers **46** and **48**, respectively. Additionally, the timing controller generates other control signals (e.g., polarity inversion signal, etc.), as will be discussed in greater detail below.

[0059] Upon sensing an off-time of a ramp voltage, the timing controller **42** further generates a black data signal and/or a white data signal until the system power supply **38** is turned off such that the black and/or white data signal may be displayed on the liquid crystal display panel **50**. Accordingly, residual images may be prevented from forming when the liquid crystal module **40** is powered-off. For example, the timing controller **42** may sense an off-time of the ramp voltage using either a ramp voltage control signal applied from the microcomputer **36** to the system power supply **38** or a ramp voltage applied from the system power supply **38** to the inverter **54**.

[0060] The liquid crystal display panel **50** may, for example, include a plurality of liquid crystal cells arranged in a matrix pattern and connected to thin film transistors (TFTs). Each of the TFTs may be provided at intersections of gate lines G1 to Gn and data lines D1 to Dm. The TFTs respond to gate signals applied from the gate lines G1 to Gn and receive video signals applied from the data lines D1 to Dm. Each liquid crystal cell may include a pixel electrode connected to an opposing common electrode via a liquid crystal and TFT. Accordingly, each liquid crystal cell may be equivalently expressed as a liquid crystal capacitor Clc. Such liquid crystal cells may include a storage capacitor Cst connected to the pre-stage gate line in order to sustain data voltages charged within the liquid crystal capacitor Clc until subsequent data voltages are charged.

[0061] In response to a control signal outputted from the timing controller **42**, the gate driver **48** sequentially applies a gate high voltage signal to gate lines G1 to Gn. The data driver **46** converts the video data signals outputted from the timing controller **42** into analog video voltage signals and applies analog video voltage signals, specific to one horizontal line, to data lines D1 to Dn for each horizontal period during which a gate high voltage signal is applied to the gate lines G1 to Gn. The gamma circuit **52** applies a predetermined gamma voltage to the data driver **46** in accordance with voltage levels associated with the analog video voltage signals. Thus, the data driver **46** uses gamma voltages supplied from the gamma circuit **52** to convert the video data signals outputted from the timing controller **12** into analog video voltage signals.

[0062] In one aspect of the present invention, the data driver **46** may convert the black and white data signals generated by the timing controller **42** into analog video voltage signals and apply them to the liquid crystal display panel **50**.

[0063] The inverter **54** converts a driving voltage inputted from the system power supply **38** into a high alternating current voltage corresponding to a lamp luminance of the backlight unit **56**. The backlight unit **56** may, for example, be provided at a rear side of the liquid crystal display panel **50** and supply light suitable for displaying a picture. Accordingly, the backlight unit **56** may include a lamp arranged within a lamp housing, a light guide for guiding light emitted from the lamp toward a surface of the liquid crystal panel, optical sheets arranged on the light guide to enhance light display properties, and a reflector arranged on a rear side of the light guide.

[0064] Referring to **FIGS. 4 and 5**, a method and driving procedure for driving the liquid crystal display illustrated in **FIG. 3** will now be described.

[0065] At step S10 and time T1, if a 'power-on' command is inputted by a user, the microcomputer **36** turns the system power supply **38** on such that a driving voltage may be applied to the LCM power supply **44**. In turn, the LCM

power supply **44** generates driving voltages (e.g., a base driving voltage Vcc, a gate high voltage Vgh, a gate low voltage Vgl, etc.) required to drive the liquid crystal module **40**.

[**0066**] At step S**20**, if a reset signal (RESET) is generated from the microcomputer **36**, the graphic card **34** generates video data signals at time T2 and applies the generated video data signals to the liquid crystal module **40**. Using the driving voltages generated by the LCM power supply **44**, the liquid crystal module **40** applies video data signals generated by the graphic card **34** to the liquid crystal display panel **50**.

[**0067**] At step S**30** and time T3, the microcomputer **36** allows a ramp voltage (Vramp) to be applied to the inverter **54** via the system power supply **36**. As the lamp is activated by the ramp voltage (Vramp) outputted by the inverter **54**, the backlight unit **56** emits light into the liquid crystal display panel **50**. Thus, the liquid crystal display panel **50** may control a transmittance of the light emitted from the backlight unit **56** in accordance with inputted video data signals, to display a picture.

[**0068**] A driving operation of the liquid crystal display panel **50** will now be described.

[**0069**] As the TFT is turned on by a gate high voltage Vgh applied to a gate line G, a video voltage signal, applied to the data lines D1 to Dm, may be charged within the liquid crystal capacitor Clc. As the TFT is turned off by a gate low voltage Vgl applied to the gate line G, the video voltage signal remains charged within the liquid crystal capacitor Clc until the next data voltage signal is applied. Accordingly, the storage capacitor Cst connected to the liquid crystal capacitor Clc, in parallel, is charged with a data voltage signal when a gate high voltage Vgh is applied to a pre-stage gate line Gi-1. When a gate low voltage Vgl is applied, a higher voltage than the data voltage signal charged in the liquid crystal capacitor Clc is maintained during a turn-off interval of the thin film transistor. Thus, since the storage capacitor Cst applies electric charges to the liquid crystal capacitor Clc during a turn-off interval of the TFT, the variation in the voltage charged within the liquid crystal capacitor Clc is minimized.

[**0070**] Next, at step S**40** and time T4, a power-off command is inputted from a user and the microcomputer **36** shuts off the ramp voltage applied to the inverter **54**, via the system power supply **38**.

[**0071**] At step S**50**, the timing controller **42** may sense an off-time of the ramp voltage (Vramp) and sequentially generate a full black data signal (FBD) and a full white data signal (FWD) such that the full black and white data signals may be displayed on the liquid crystal display panel **50**. In another aspect of the present invention, the timing controller **42** senses an off-time of the ramp voltage (Vramp) and may generate only a full white data signal (FWD) to be displayed on the liquid crystal display panel **50**.

[**0072**] At step S**60** and time T5, the microcomputer **36** turns the system power supply **38** and the LCM power supply **44** off.

[**0073**] As described above, a residual image prevention apparatus for the liquid crystal display, according to the present invention, senses an off-time of the ramp voltage (Vramp). In one aspect of the present invention, after a user inputs a power-off command, the off-time of the ramp voltage (Vramp) occurs earlier point in time compared to the off-time of the LCM power supply **44**. Subsequently, either a black data signal and a white data signal, or only a white data signal may be displayed on the liquid crystal display panel **50** until the LCM power supply **44** is turned off. Accordingly, the formation of residual images may be prevented when the LCM power supply **44** is turned off.

[**0074**] **FIG. 6** illustrates a block diagram showing a detailed configuration of the timing controller **42** shown in **FIG. 3**.

[**0075**] Referring to **FIG. 6**, the timing controller **42** may, for example, include a timing control signal generator **66** for generating a timing control signal, a polarity controller **68** for generating a polarity inversion signal, a video data aligner **64** for aligning and outputting video data, a ramp voltage sensor **60** for sensing an off-time of the ramp voltage (Vramp), and a black/white data signal generator **62** for generating and applying black and white data signals to the video data aligner **64** when a ramp voltage off signal (Vramp_off) is outputted from the ramp voltage sensor **60**.

[**0076**] Using the control signals (e.g., a main clock signal, a vertical synchronizing signal, a horizontal synchronizing signal, etc.) generated by the graphic card **34**, the timing control signal generator **66** generates timing control signals for the data driver **46** and the gate driver **48**.

[**0077**] In response to the control signals outputted from the graphic card **34**, the polarity controller **68** generates polarity inversion signals suitable for driving the liquid crystal display panel according to a predetermined inversion scheme (e.g., dot inversion, line inversion, frame inversion driving, etc.).

[**0078**] Using a ramp voltage control signal outputted from the microcomputer **36** and a ramp voltage signal (Vramp) from the system power supply **38**, the ramp voltage sensor **60** senses an off-time of the ramp voltage and generates a ramp voltage off signal (Vramp_off).

[**0079**] When a ramp voltage off signal (Vramp_off) is outputted from the ramp voltage sensor **60**, the black/white data signal generator **62** sequentially generates a full black data signal (FBD) and a full white data signal (FWD) for one frame and applies the data signals to the video data aligner **64**. In another aspect of the present invention, the black/white data signal generator **62** may be replaced by a white data signal generator, wherein the white data signal generator generates only a white data signal.

[**0080**] The video data aligner **64** receives video data outputted from the graphic card **34**, re-aligns, and outputs the video data to drive the data driver **46**. Further, when the ramp voltage is turned off, the video data aligner **64** re-aligns the full black data signal (FBD) and the full white data signal (FWD), outputted from the black/white data signal generator **62**, and applies them to the data driver **46**.

[**0081**] When an off-time of the ramp voltage is sensed, the timing controller **42** generates either a full black data signal (FBD) and a full white data signal (FWD) or only a full white data signal (FWD), applies the data signals to the data driver **46**, and drives the data driver **46** and the gate driver **48**. Accordingly, when a power-off command is inputted from a user, either a full black and full white signals, or only

a full white signal, are displayed on the liquid crystal display panel, thereby preventing the formation of residual images when the liquid crystal module **40** is powered-off.

[**0082**] According to the principles of the present invention, when a power-off command is inputted from a user, an off-time of the ramp voltage is sensed. In one aspect of the invention, the off-time of the ramp voltage occurs earlier than an off-time of the LCM power supply **44**. Accordingly, either a full black data signal (FBD) and a full white data signal (FED) or only a full white data signal (FWD) is displayed on the liquid crystal display panel until the LCM power supply **44** is turned off, thereby preventing the formation of residual images caused when the liquid crystal module **40** is powered-off.

[**0083**] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of preventing the formation of residual images in a liquid crystal display, comprising:

providing a liquid crystal module, the liquid crystal module including a liquid crystal module power supply;

generating a white data signal when an off-time of a ramp voltage is sensed; and

displaying the generated white data signal on a liquid crystal display panel until the power supply is turned off.

2. The method according to claim 1, further comprising generating a black data signal one frame prior to generating the white data signal.

3. The method according to claim 1, wherein sensing the off-time of the ramp voltage comprises:

providing a microcomputer;

connecting a system power supply to the microcomputer;

inputting a power-off command; and

outputting a ramp voltage control signal from the microcomputer to the system power supply in response to the inputted power-off command.

4. The method according to claim 1, wherein sensing the off-time of the ramp voltage comprises:

providing a system power supply;

inputting a power-off command; and

outputting a ramp voltage from the system power supply in response to the inputted power-off command.

5. The method according to claim 1, wherein the white data signal is displayed on the liquid crystal display panel during at least one frame.

6. A residual image prevention apparatus for a liquid crystal display, comprising:

a liquid crystal module including a liquid crystal display panel for displaying a picture, the liquid crystal display panel including a plurality of signal lines;

a signal line driving circuit for driving the plurality of signal lines;

a timing controller for controlling a driving time of the signal line driving circuit and for applying a data signal;

a liquid crystal module power supply for supplying driving voltages suitable for the liquid crystal display panel, the signal line driving circuit, and the timing controller;

a backlight unit for providing light to the liquid crystal display panel;

a ramp driver for applying a ramp driving voltage to the backlight unit; and

a system part for driving and controlling the liquid crystal module,

wherein the timing controller generates a white data signal when an off-time of the ramp voltage, applied to the ramp driver from the system part, is sensed and displays the white data signal on the liquid crystal display panel.

7. The residual image prevention apparatus according to claim 6, wherein the system part comprises:

a system power supply for supplying a liquid crystal module voltage to a power supply of the liquid crystal module and for supplying the ramp voltage to the ramp driver;

a microcomputer for controlling the system power supply such that the power supply of the liquid crystal module and the ramp driver are activated during different times; and

a graphic card for applying the data signal and a plurality of control signals to the timing controller.

8. The residual image prevention apparatus according to claim 7, wherein the timing controller senses an off-time of the ramp voltage using a ramp voltage control signal applied from the microcomputer to the system power supply.

9. The residual image prevention apparatus according to claim 6, wherein the timing controller comprises:

a ramp voltage sensor for sensing an off-time of the ramp voltage and for generating a ramp voltage off signal;

a white data signal generator for generating the white data signal in response to the generated ramp voltage off signal;

a timing control signal generator for generating control signals for controlling a driving time of a signal line driving integrated circuit using input control signals; and

a data aligner for aligning and outputting an input data signal and the white data signal.

10. The residual image prevention apparatus according to claim 6, wherein the timing controller generates a black data signal during at least one frame prior to generating the white data signal when said off-time of the ramp voltage is sensed, thereby displaying the black data signal on the liquid crystal display panel.

11. The residual image prevention apparatus according to claim 6, wherein the timing controller displays the white data signal on the liquid crystal display panel during at least one frame.

12. The residual image prevention apparatus according to claim 6, wherein the timing controller generates the white data signal based on the off-time of the ramp voltage until the power supply of the liquid crystal module is turned off, thereby displaying white data signal on the liquid crystal display panel.

13. A liquid crystal display, comprising:

a liquid crystal display panel;

a backlight unit;

an inverter for applying a ramp driving voltage to the backlight unit;

a timing controller for applying a data signal to the liquid crystal display panel,

wherein when the ramp driving voltage is not applied, the timing controller generates a white data signal displayable on the liquid crystal display panel.

14. The liquid crystal display according to claim 13, wherein the timing controller comprises:

a ramp voltage sensor for sensing when the ramp driving voltage is not applied;

a white data signal generator for generating the white data signal; and

a data aligner for aligning and outputting an input data signal and the white data signal.

15. The liquid crystal display according to claim 13, wherein the white data signal is displayable for at least one frame.

16. The liquid crystal display according to claim 13, wherein when the ramp driving voltage is not applied, the timing controller generates a black data signal displayable on the liquid crystal display panel.

17. The liquid crystal display according to claim 16, wherein the black data signal is displayable for at least one frame prior to the white data signal being displayable.

18. The liquid crystal display according to claim 13, further comprising:

a liquid crystal module power supply for generating driving voltages required for driving the liquid crystal display, wherein the white data signal is displayable until the liquid crystal module power supply is turned off.

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专利名称(译)	用于防止液晶显示器中残留图像的方法和装置		
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摘要(译)

自适应方法和装置防止在断电时由液晶单元放电引起的液晶显示器中残留图像的形成。当感测到斜坡电压的关闭时间时，可以生成白色数据信号。然后将白色数据信号显示在液晶显示板上，直到液晶模块的电源关闭。