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(54) **LIQUID CRYSTAL DISPLAY DEVICE, SYSTEM AND METHODS OF COMPENSATING FOR DELAYS OF GATE DRIVING SIGNALS THEREOF**

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(57) **ABSTRACT**

A liquid crystal display device includes a gate driving shift register having symmetrically split circuit portions by which each of plural gate lines is dually driven from both ends of the gate line during ripple-through scanning of rows of the LCD device. The LCD device includes a timing controller generating an output enable signal and a gate clock, where the timing controller adjusts a timing of a load signal for deciding a data output timing point when data will be loaded into a currently activated display row. The data output timing point is a function of a delay measuring feedback signal that is used to measure the cumulative delays of the sequentially connected stages of the shift register.

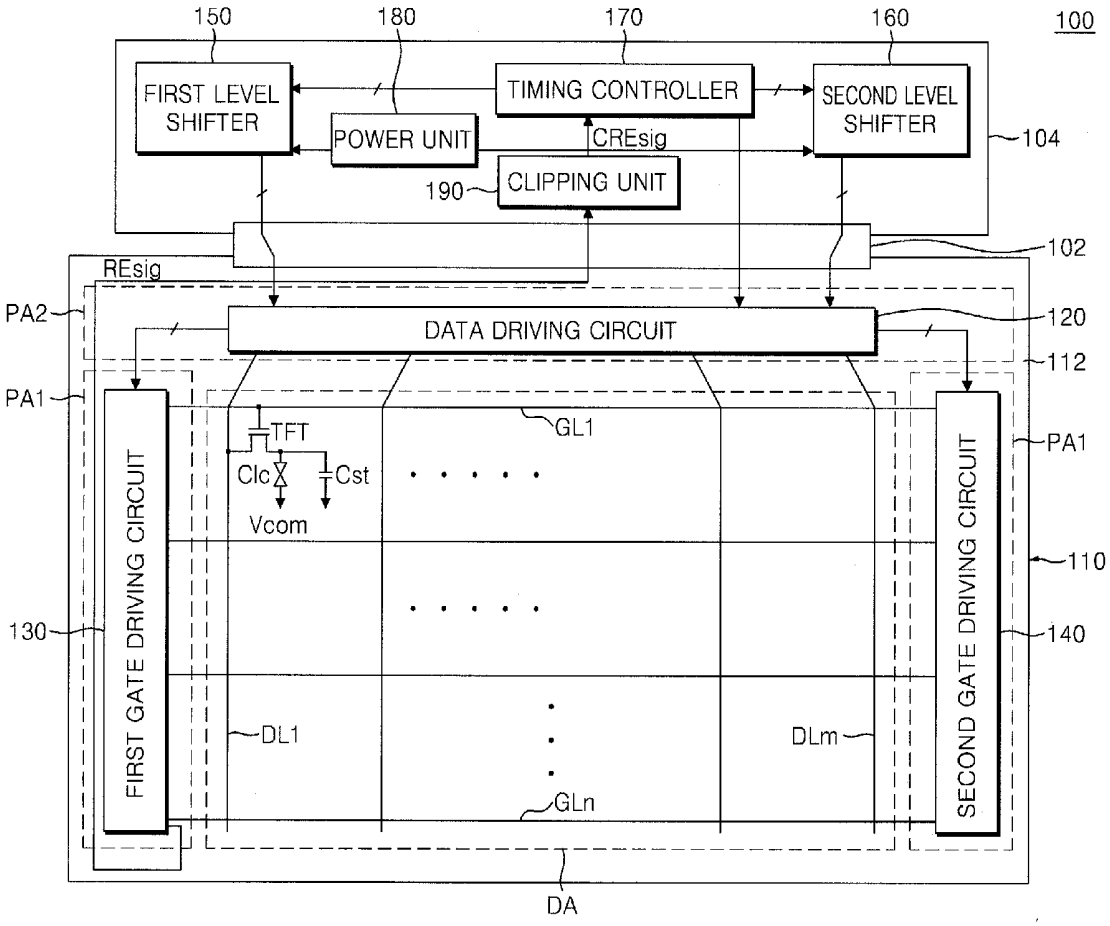


FIG. 1

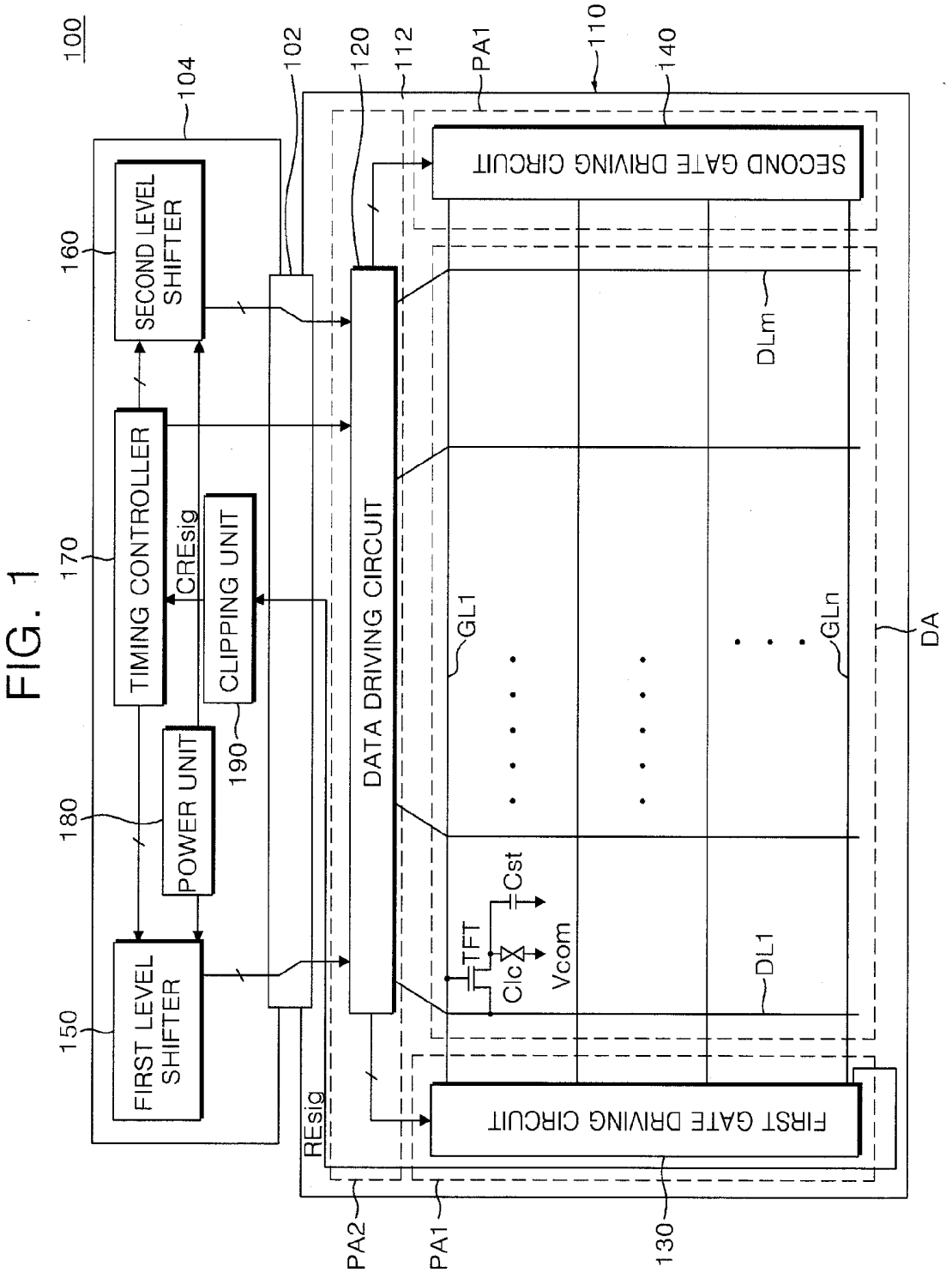

100
104
102
120
112
PA1
110
140
SECOND GATE DRIVING CIRCUIT
160
SECOND LEVEL SHIFTER
DLm
170
TIMING CONTROLLER
CREsig
CLIPPING UNIT
DATA DRIVING CIRCUIT
GL1
GLn
DA
180
POWER UNIT
190
Cst
TFT
Clc
Vcom
DL1
150
FIRST LEVEL SHIFTER
RESig
FIRST GATE DRIVING CIRCUIT
PA2
PA1
130

FIG. 2

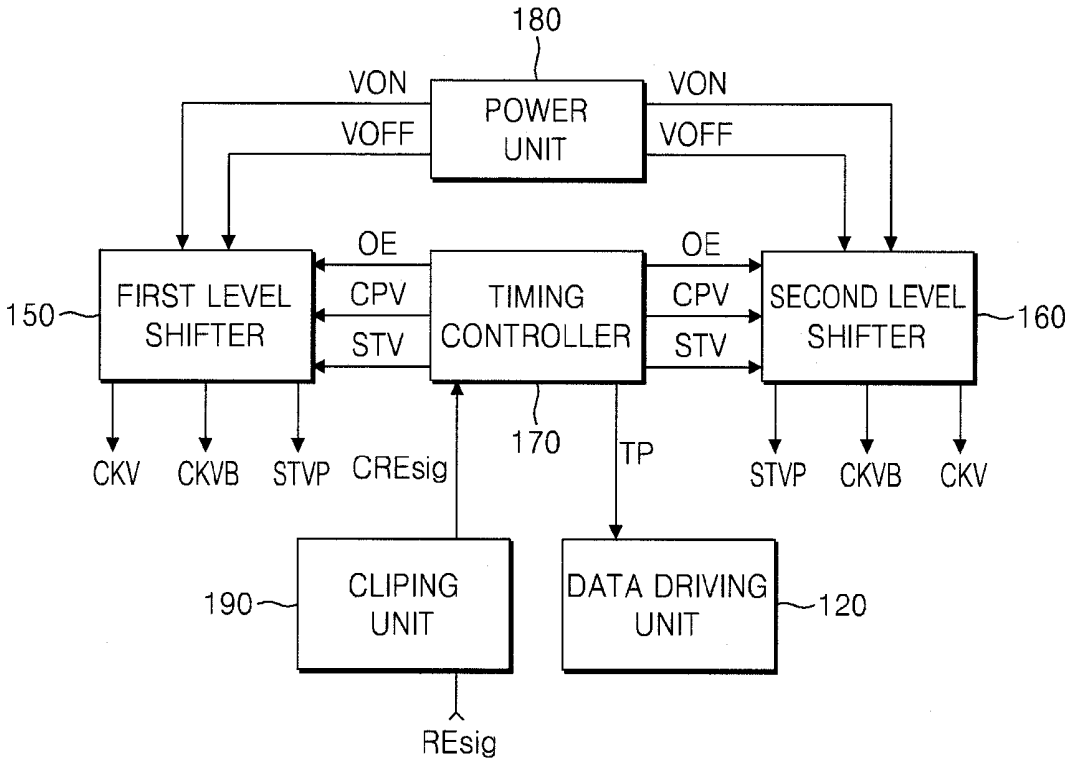

180
VON
VOFF
POWER UNIT
VON
VOFF
OE
CPV
STV
FIRST LEVEL SHIFTER
150
TIMING CONTROLLER
OE
CPV
STV
SECOND LEVEL SHIFTER
160
CKV
CKVB
STVP
CREsig
170
TP
STVP
CKVB
CKV
190
CLIPING UNIT
DATA DRIVING UNIT
120
REsig

FIG. 3

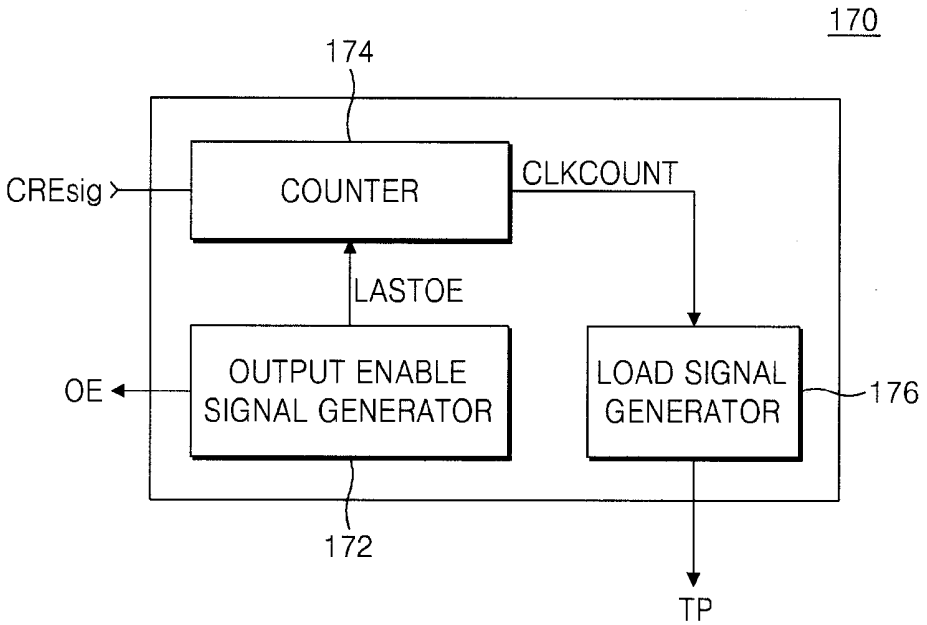

170
174
CREsig
COUNTER
CLKCOUNT
LASTOE
OE
OUTPUT ENABLE SIGNAL GENERATOR
LOAD SIGNAL GENERATOR
176
172
TP

FIG. 4

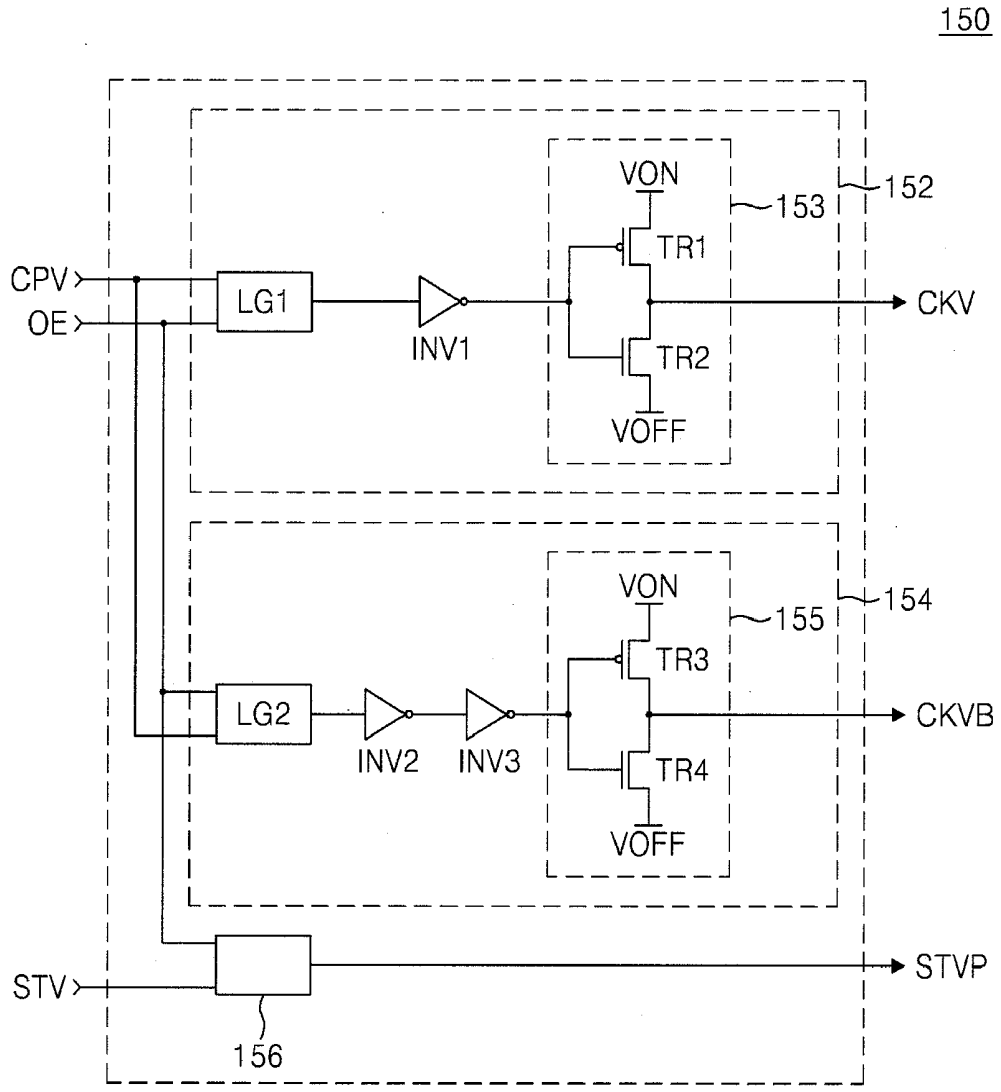

150
VON
153
152
TR1
CPV
OE
LG1
INV1
CKV
TR2
VOFF
VON
155
154
TR3
LG2
INV2
INV3
CKVB
TR4
VOFF
STV
156
STVP

FIG. 5

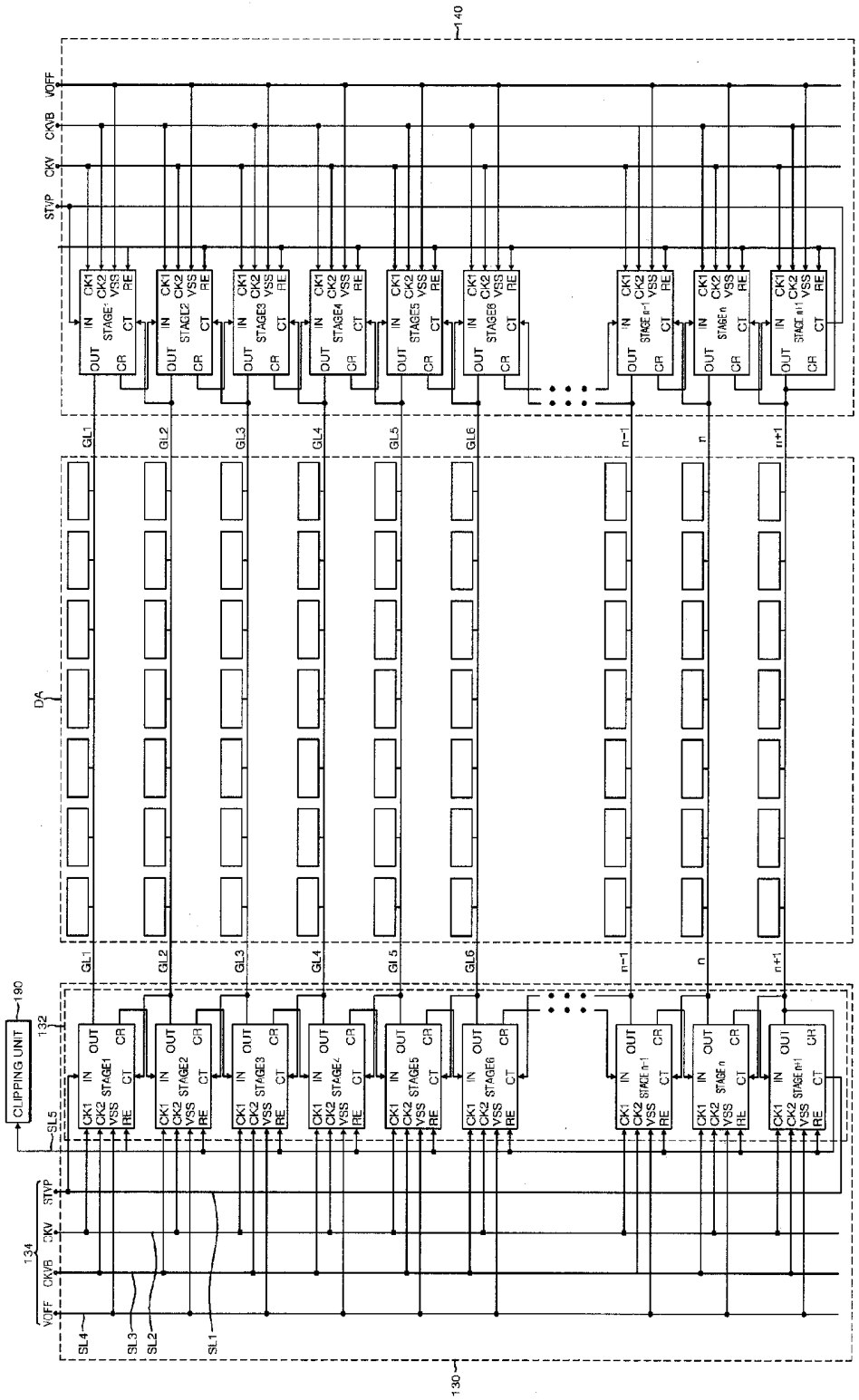

140
VOFF
CKVB
CKV
STVP
GL1
GL2
GL3
GL4
GL5
GL6
n-1
n
n+1
DA
CLIPPING UNIT
190
132
SL5
134
SL4
SL3
SL2
SL1
130

FIG. 6

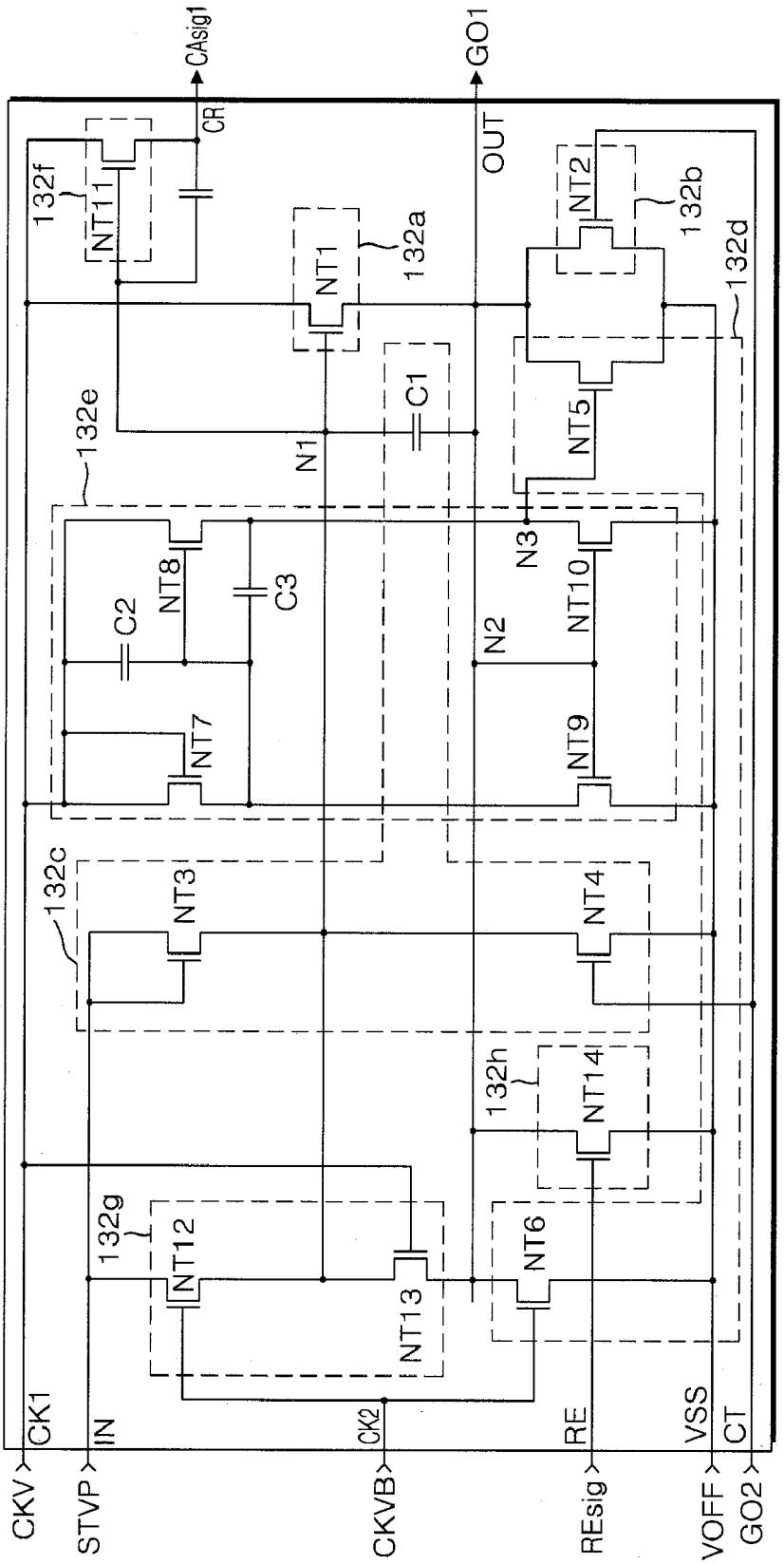

STAGE1
CAsig1
GO1
CR
OUT
132f
NT11
NT1
132a
NT2
132b
132d
C1
132e
N1
NT5
N3
C2
NT8
C3
N2
NT10
NT7
NT9
132c
NT3
NT4
132h
NT14
132g
NT12
NT13
NT6
CK1
IN
CK2
RE
VSS
CT
CKV
STVP
CKVB
REsig
VOFF
GO2

FIG. 7

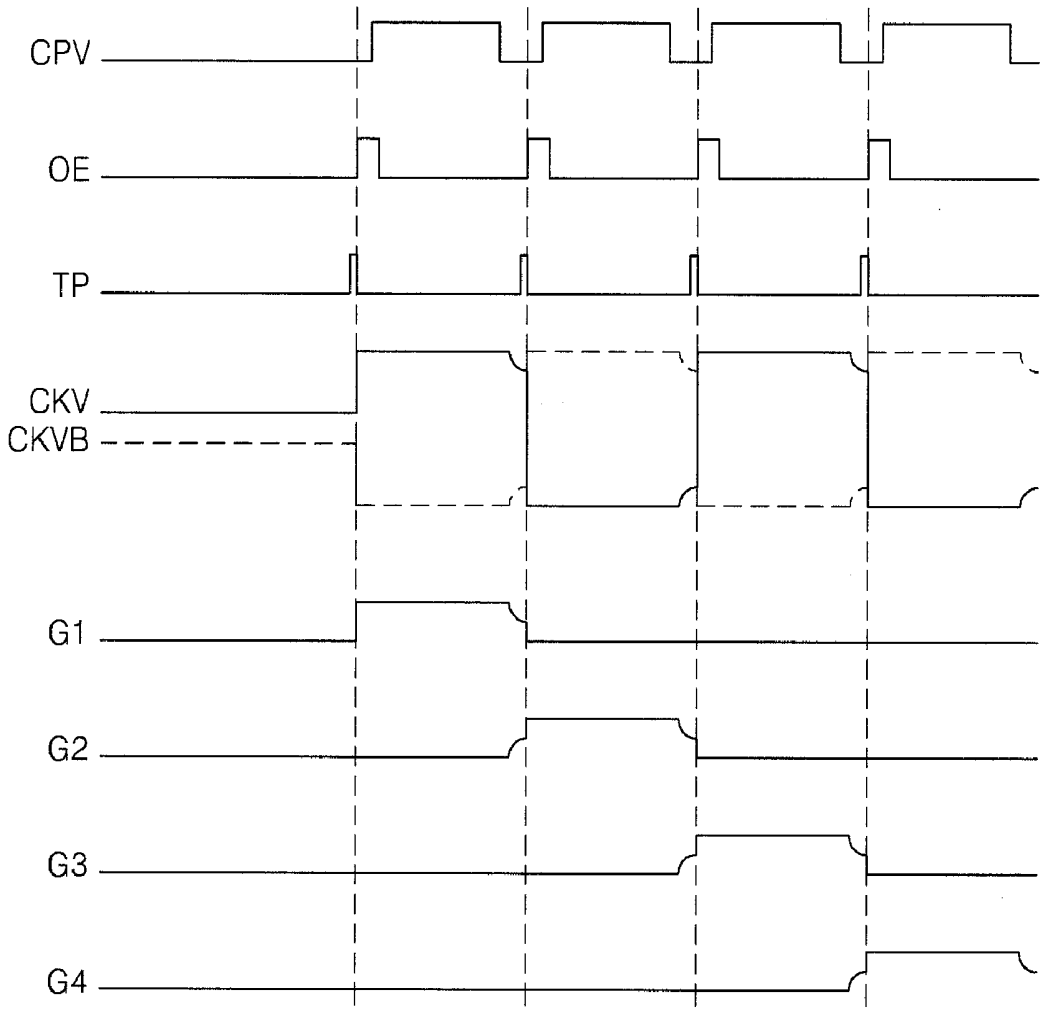


FIG. 8

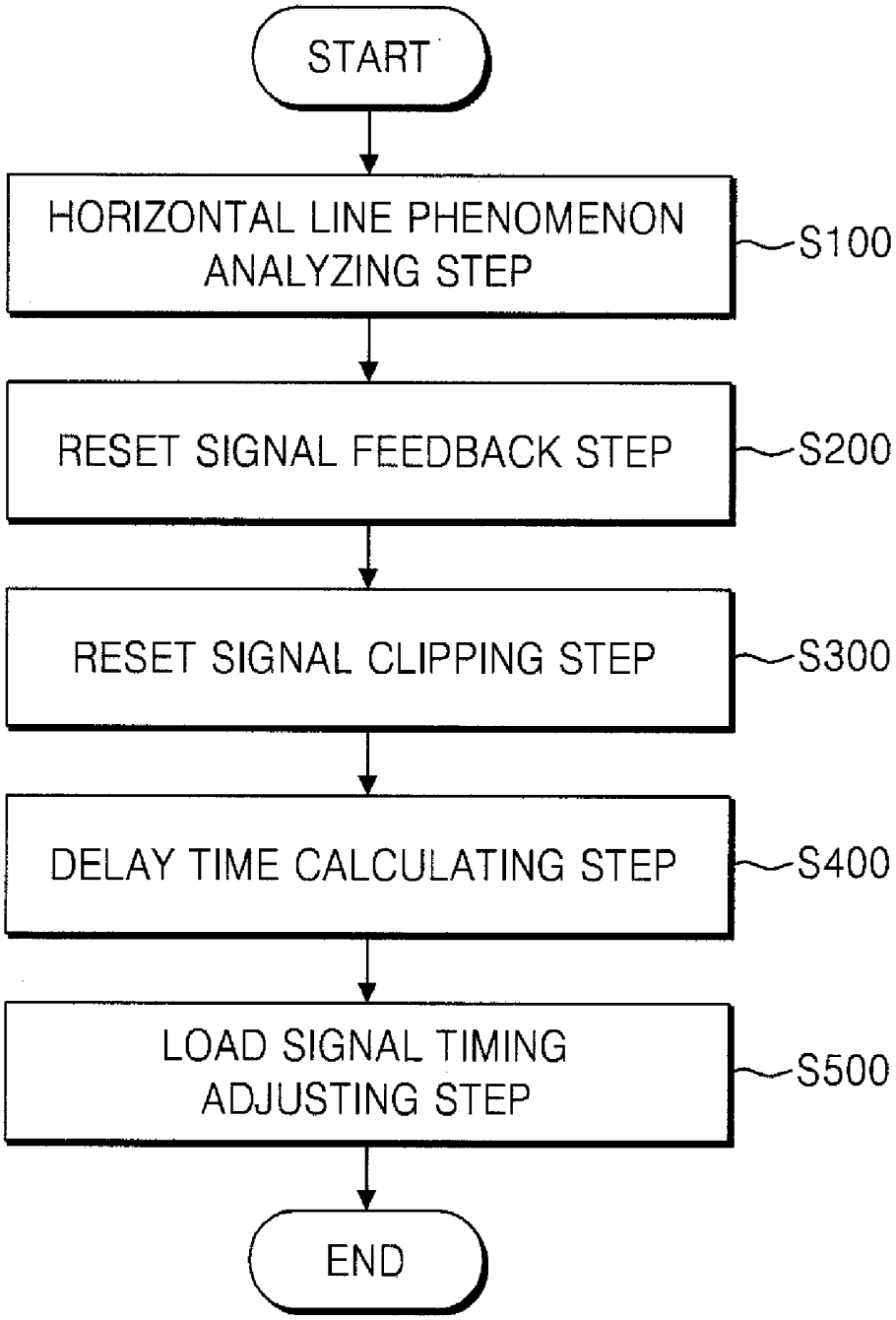

START
HORIZONTAL LINE PHENOMENON ANALYZING STEP
S100
RESET SIGNAL FEEDBACK STEP
S200
RESET SIGNAL CLIPPING STEP
S300
DELAY TIME CALCULATING STEP
S400
LOAD SIGNAL TIMING ADJUSTING STEP
S500
END

FIG. 9A

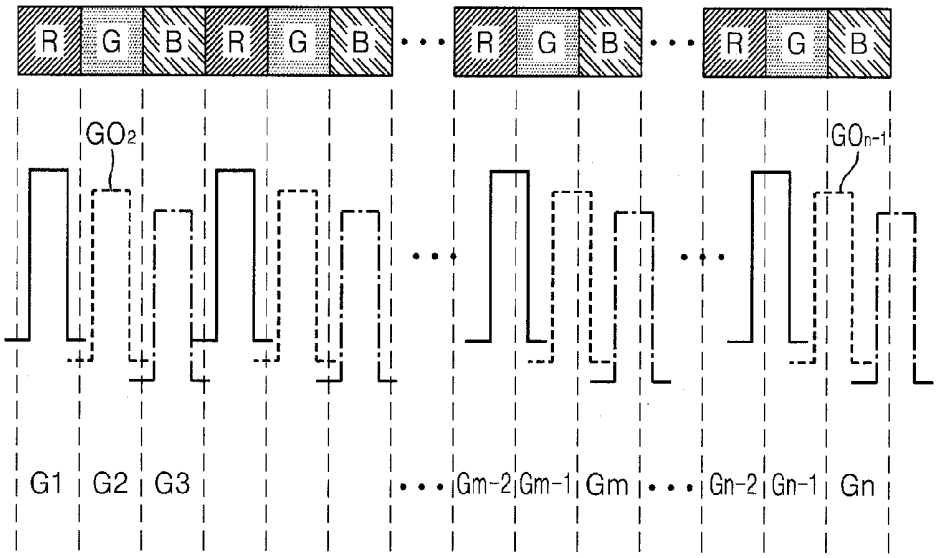

R
G
B
GO2
GOn-1
G1
G2
G3
Gm-2
Gm-1
Gm
Gn-2
Gn-1
Gn

FIG. 9B

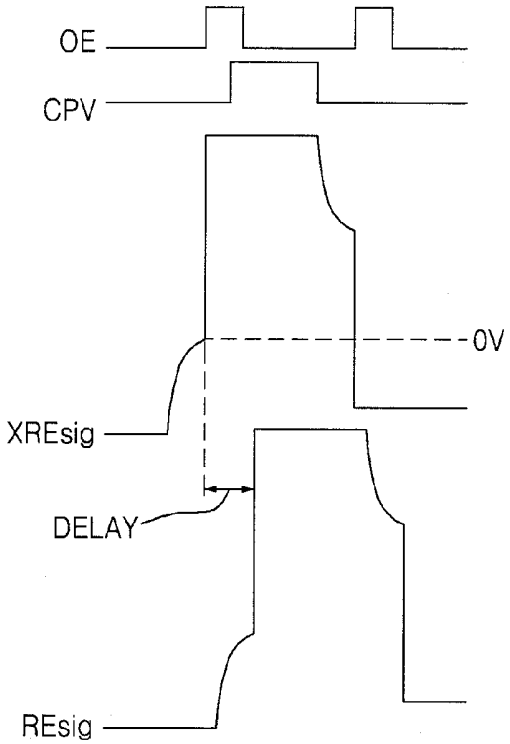

OE
CPV
0V
XREsig
DELAY
REsig

FIG. 9C

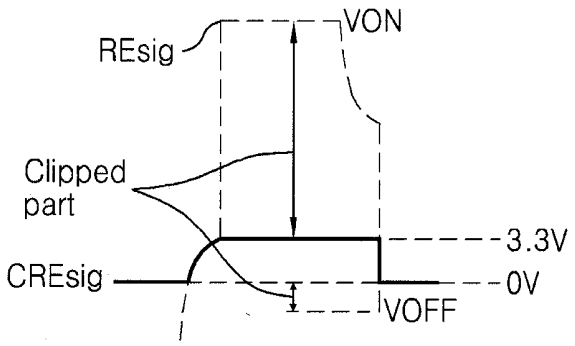
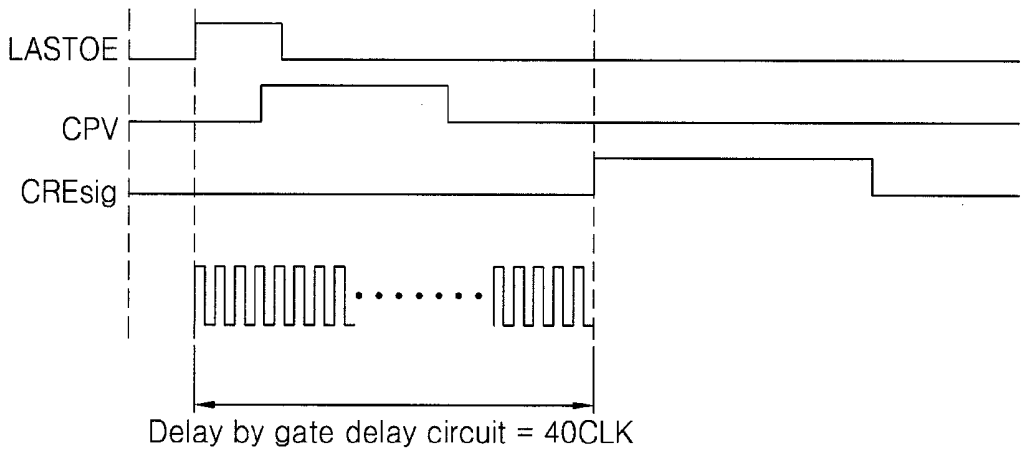

REsig
VON
Clipped part
3.3V
CREsig
0V
VOFF

FIG. 9D


LASTOE
CPV
CREsig
Delay by gate delay circuit = 40CLK

LIQUID CRYSTAL DISPLAY DEVICE, SYSTEM AND METHODS OF COMPENSATING FOR DELAYS OF GATE DRIVING SIGNALS THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and benefit of Korean Patent Application No. 10-2006-0125334 filed in the Korean Intellectual Property Office on Dec. 11, 2006, the entire disclosure of which is incorporated herein by reference.

FIELD OF INVENTION

[0002] The present disclosure of invention relates to a liquid crystal display device, and more particularly, to a liquid crystal display (LCD) device that includes means for decreasing delays of pulsed gate driving signals thereof.

DISCUSSION OF RELATED ART

[0003] Generally, a liquid crystal display ("LCD") device has an LCD panel for displaying a video image, a data driving unit for generating data-line signals of the LCD panel, and a gate driving unit for generating gate-line signals of the LCD panel. The LCD panel includes a plurality of gate lines, a plurality of intersecting data lines, and a plurality of pixels. Each of the pixels typically includes a thin film transistor ("TFT") and a pair of opposed electrode areas that define a liquid crystal capacitor. The data driving unit outputs its data signals (usually analog signals) to respective data lines of the panel and the gate driving unit outputs its gate driving signals (usually pulsed digital signals) to respective gate lines of the panel.

[0004] The gate driving unit is typically formed on the LCD panel by a same fabrication process as is used for the TFTs. The data driving unit typically has a chip type configuration whose chip or packaging is connected to a peripheral area of the LCD panel. The gate driving unit typically includes a shift register having a plurality of stages. Each of the stages is connected to a corresponding one of the gate lines and outputs a corresponding gate driving pulse or signal.

[0005] The gate driving unit is structured to sequentially output a gate line activating pulse that appears to cascade down the rows of the display panel and to thereby scan through the rows, one row at a time. The stages of the shift register are serially interconnected so that an input terminal of a current (Nth) stage is connected to an output terminal of a previous stage (N−1th) and so that an output terminal of a next stage (N+1th) is connected to a control terminal of the current (Nth)stage. Moreover, a start signal is inputted to a first one (N=1) of the plurality of stages to initiate the sequential scanning of the rows by a down-moving gate pulse.

[0006] In one embodiment, the above-configured gate driving unit is provided as left and right circuit portions respectively disposed on the left and right sides of the LCD panel. In one particular design, the left gate driving circuit portion drives only the odd-numbered gate lines, while a right gate driving circuit portion drives only the even-numbered gate lines. Thus, the gate driving unit of the one particular design is operated as a single driving system even though it has portions disposed at the left and right sides of the display panel.

[0007] Such a single driving system with split left and right portions sometimes has a problem in that artifacts in the form of left and right side horizontal lines or stripes become visible due to gate line propagation delays imposed on gate line activating pulses input form opposing sides of the display by the left and right drive portions. Additional delays may be imposed on gate line activating pulses by so-called ASG (amorphous silicon gate) delays.

[0008] By gate line delay, what is meant here is that the gate driving signals alternately applied from the left and right gate driving circuit portions are differently delayed as they propagate into a front portion and then toward the end of the corresponding gate line. The gate line delay may cause a pixel connected to a far end of a gate line to have insufficient time for charging to a desired pixel electrode voltage (corresponding to the data line voltage), thereby reducing luminance of the corresponding pixel. In such a case, a luminance difference between two gate lines adjacent to each other is generated at the left or right sides of the neighboring gate lines, which causes the horizontal lines or stripes visibility phenomenon to undesirably appear at the left and right margins of the display.

[0009] By the ASG delay, what is meant here is that a gate driving pulse signal is sometimes applied to the gate of a given TFT later in time than a corresponding data output time slot that is to be associated with the gate driving pulse, this being due to delay variations in gate driving circuit itself where the gate driving circuit is designed to sequentially apply the gate driving pulse signal to a plurality of gate lines one after the next in open loop manner. So, there occurs a problem that a pixel connected to an Nth gate line located at a lower part of an LCD panel has a luminance lower than a luminance corresponding to the value of the data signal that is to be originally displayed because the open loop gate driving circuit is not perfectly synchronized with the timings of the data driving circuit and vise versa. For instance, in case that a data signal of a green level (G) and a data signal of a blue level (B) are respectively provided by a data line driving unit in respective time slots associated with the data driving unit, if a gate driving signal is sequentially applied to a plurality of gate lines, there occurs a problem that the displayed luminance of the blue level (B) gets lower than what level of blue (B) was supposed to be originally displayed by a data signal representing the blue level (B) as one moves toward a lower part of an LCD panel.

SUMMARY

[0010] In accordance with the disclosure, a liquid crystal display and a method of decreasing delay problems of a gate driving unit thereof are provided where each gate line is dually driven from both ends by providing gate driving circuit portions at both ends of each of the gate lines and where the synchronization delay problem between the gate driving and data line driving circuits is compensated for by feeding back a reset signal of the gate driving circuit.

[0011] In one exemplary embodiment, a liquid crystal display device includes a timing controller generating an output enable signal and a gate clock signal, the timing controller adjusts the timing of a load signal for deciding a data output timing point. The device includes a level shifter that generates a gate clock pulse in response to the output enable signal and the gate clock. The device includes a gate driving circuit that sequentially drives a plurality of gate lines by generating a first gate driving signal in response to the gate clock pulse, and the device includes a clipping unit that provides the timing controller with a second gate driving signal generated

by clipping the first gate driving signal, wherein the timing controller measures an actual delay of the gate driving circuit; such as from start of scan of a display frame to the end of the frame and then it calculates a per row delay time associated with stages of the gate driving circuit. The calculated per-row delay time is used to adjust the timing of the load signal according to the number of rows cumulatively scanned during a given frame.

[0012] The level shifter generates the gate clock pulse of a gate-on voltage level and a gate-off voltage level.

[0013] The gate clock pulse includes a gate clock bar pulse having an inverted phase with respect to a phase of the gate clock pulse.

[0014] The first gate driving signal includes a reset signal for resetting the gate driving circuit.

[0015] The gate driving circuit is integrated on a liquid crystal display panel having the gate lines formed thereon and is dually formed at both ends of the gate lines to dually drive the data lines.

[0016] The gate driving circuit includes a shift register having a plurality of stages serially connected one to the next in a ripple forward manner.

[0017] The plurality of stages are connected to the plurality of gate lines, respectively.

[0018] The plurality of stages include a dummy stage generating a reset signal that is coupled back to all the stages for resetting them at the end of vertical scan of a display frame.

[0019] The timing controller includes an output enable signal generator providing a last output enable signal corresponding to the end of one frame, a counter generating a clock count signal by comparing the clipped reset signal and the last output enable signal of the one frame to thereby determine how far apart from ideal the actual delay is, and a load signal generator for adjusting the timing of the load signal on a per-rows scanned basis and on the basis of the measured ripple-through delay for the whole frame.

[0020] In another exemplary embodiment, a liquid crystal display includes a gate driving circuit generating a gate driving signal including a reset signal and a timing controller calculating a delay time of the gate driving signal circuit by comparing the reset signal and an output enable signal corresponding to the reset signal, the timing controller adjusting a timing of a load signal for deciding a data output timing point in response to the delay time.

[0021] The liquid crystal display further includes a clipping unit providing the timing controller with a clipped reset signal generated by clipping the reset signal.

[0022] The timing controller includes an output enable signal generator providing the output enable signal, a counter generating a clock count signal by comparing the clipped reset signal and a last output enable signal of one frame, and a load signal generator adjusting the timing of the load signal in response to the clock count signal.

[0023] The gate driving circuit includes a shift register having a plurality of stages dependently connected to each other and each of the plurality of the stages includes a dummy stage generating the reset signal.

[0024] The counter generates as the clock count signal the number of clocks corresponding to an interval from a rising timing point of the output enable signal to a rising timing point of the clipped reset signal.

[0025] The load signal generator calculates a delay time of the gate driving signal by dividing the number of gate lines provided on the display by a value of the clock count signal and responsively delays a falling timing point of the load signal corresponding to the calculated delay time of the gate driving signal and corresponding to the number rows scanned thus far when proceeding down one frame.

[0026] In another exemplary embodiment, a method of decreasing a delay of a gate driving signal includes a reset signal feedback step of feeding back a reset signal that is an output signal of a dummy stage of a gate driving circuit to a timing controller, a delay time calculating step of calculating a delay time of a gate driving signal generated from the gate driving circuit by comparing the reset signal to an output enables signal corresponding to the reset signal, and a load signal timing adjusting step of adjusting a timing of a load signal for deciding an output timing point of data in response to the delay time.

[0027] The reset signal feedback step includes clipping the reset signal to a predetermined voltage level and then feeding back the clipped reset signal to the timing controller.

[0028] The delay time calculating step includes generating a clock count signal by counting the number of clocks corresponding to an interval from a rising timing point of the output enable signal to a rising timing point of the clipped reset signal.

[0029] The load signal timing adjusting step includes calculating a delay time of the gate driving signal by dividing the number of gate lines provided with the gate driving signal by a value of the clock count signal and delaying a falling timing point of the load signal corresponding to the calculated delay time of the gate driving signal.

[0030] It is to be understood that both the foregoing initial description and the following detailed description of the present disclosure of invention are exemplary and explanatory and are intended to provide further explanation rather than limiting constraints.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] The accompanying drawings, which are included to provide a further understanding of the disclosure, illustrate various embodiments. In the drawings:

[0032] FIG. **1** is a block diagram of an LCD device according to one embodiment of the present disclosure;

[0033] FIG. **2** is a block diagram to explain an input/output signal relation of a timing controller shown in FIG. **1**;

[0034] FIG. **3** is a block diagram of a timing controller shown in FIG. **2**;

[0035] FIG. **4** is a circuit diagram of a first level shifter shown in FIG. **1**;

[0036] FIG. **5** is a block diagram of first and second gate driving circuits shown in FIG. **1**;

[0037] FIG. **6** is an exemplary circuit diagram of a stage of the first gate driving circuit shown in FIG. **5**;

[0038] FIG. **7** is an operational timing diagram of the LCD device shown in FIG. **1**;

[0039] FIG. **8** is a flow chart of a method of decreasing ASG delay according to one embodiment of the present disclosure; and

[0040] FIGS. **9**A to **9**D are timing diagrams of signals to explain the ASG delay decreasing method shown in FIG. **8**.

DETAILED DESCRIPTION

[0041] Reference will now be made in detail to the embodiments illustrated in the accompanying drawings. Where prac-

tical, the same reference numbers will be used throughout the drawings to refer to same or like parts.

[0042] FIG. **1** is a block diagram of an LCD device **100** according to one embodiment. The LCD device **100** includes an LCD panel **110**, a data driving circuit **120**, a first gate driving circuit **130** on the left, a second gate driving circuit **140** on the right, a first level shifter **150** on the left, a second level shifter **160** on the right, a timing controller **170**, a power supply unit **180**, and a clipping unit **190**.

[0043] The LCD panel **110** includes a TFT's-containing substrate **112**, a color filters containing substrate (not shown), and a liquid crystal material (not shown) inserted between the TFTs substrate **112** and the color filters substrate.

[0044] The TFTs substrate **112** includes a display area DA, a first set of peripheral areas PA**1**, PA**1**' (on the left and right sides), and a second peripheral area PA**2** (on the top). The display area DA is provided with gate lines GL**1** to GLn extending therethrough in a first direction, data lines DL**1** to DLm extending therethrough in a different second direction, and a plurality of pixels each connected to adjacent ones of the gate lines GL**1** to GLn and the data lines DL**1** to DLm. The first set of peripheral areas PA**1**, PA**1**' are respectively provided with first and second gate driving circuit portions **130** and **140** (on the left and right sides) for driving respective ends of the gate lines GL**1** to GLn. And, the data driving circuit **120** for driving the data lines DL**1** to DLm is located on the second peripheral area PA**2**. As mentioned, the first set of peripheral areas PA**1**, PA**1**' are positioned adjacent to both ends of the gate lines GL**1** to GLn and the second peripheral area PA**2** is the area adjacent to one set of ends (i.e., top ends) of the data lines DL**1** to DLm.

[0045] Each of the pixels, e.g., one pixel includes a corresponding TFT (one shown) connected to the adjacent gate line (e.g., GL**1**) and to the adjacent data line (e.g., DL**1**). The equivalent circuit of each pixel may be viewed as including an LCD capacitor CLC connected to a drain terminal of the TFT, and a storage capacitor CST also connected to the same drain terminal. The gate and source of the TFT are respectively connected to the gate line GL**1** and the data line DL**1**. The LCD capacitor CLC includes a pixel electrode (not explicitly shown but understood to be one covering a substantial portion of the pixel area), an opposed portion of a common electrode, and liquid crystal molecules interposed and functioning as a dielectric material between the two electrodes.

[0046] The colors filter substrate is typically provided with a black matrix for preventing light leakage between pixel area, a plurality of differently colored color filters (e.g., R, G, B), and a common electrode. As understood by those skilled in the art, liquid crystals are substances having dielectric anisotropy and which may be used to adjust transmissivity of polarized light by being rotated by a difference between a voltage applied to the common electrode and a voltage applied to the pixel electrode.

[0047] The first and second gate driving circuits **130** and **140** are integrated on the first set of peripheral areas PA**1**, PA**1**' and more particularly, on both opposing sides of the LCD panel **110** as shown to thereby leave the gate lines GL**1** to GLn in-between. Respective gate line driving outputs of the first and second driving circuits **130** and **140** are connected to respective ends of each of the gate lines GL**1** to GLn. The first and second gate driving circuits **130** and **140** dually drive each of the gates lines GL**1** to GLn by supplying gate driving pulses from both ends of each of the gate lines GL**1** to GLn where the pulses are sequentially applied to one gate line at a time to thereby effect a vertical scanning operation. At least one of the first and second gate driving circuits, e.g., the left gate driving circuit **130** provides a reset signal, REsig that is used for resetting the gate driving circuit **130** at the end of a vertical frame scan. As shown, this end-of-frame reset signal, REsig is operatively coupled to the clipping unit **190**. The clipping unit **190** responsively produces a CREsig signal that is coupled to the timing controller **170** for indicating to the latter controller **170** that gate driving circuit **130** has now output its end-of-frame reset signal, REsig.

[0048] The data driving circuit **120** receives a data timing control signal from the timing controller **170**, and in response provides a set of analog driving voltages corresponding to the data to be displayed along the currently activated row of pixels, where the provided analog driving voltages are respectively applied to the top ends of the DATA lines DL**1** to DLm as predefined gray scale display voltages. In one embodiment, the data driving circuit **120** is implemented with a monolithic integrated chip whose substrate or packaging is loaded on (e.g., bonded to) the second peripheral area PA**2** of the TFT substrate **112**. Although not all connections are shown, the data driving circuit **120** is connected to the timing controller **170** and to the power supply unit **180** via a flexible printed circuit board **102** connected to the second peripheral area PA**2**.

[0049] Although the data driving circuit **120** of the illustrated embodiment is exemplarily loaded on the TFT substrate **112** by a COG (chip on glass) technique, it can be loaded in various other ways. For instance, it can be loaded by a TCP (tape carrier package) technique. For another instance, it can be directly integrated on the TFT substrate **112** like the first or second gate driving circuit **130** or **140**.

[0050] The first and second level shifters **150** and **160** receive a gate control signal from the timing controller **170** and a driving voltage from the power supply unit **180**, and they generate respective left and right gate driving signals for driving the left and right gate driving circuits **130** and **140**.

[0051] In addition to the CREsig signal, the timing controller **170** receives a set of digital data signals (e.g., RGB pixel data) and an input control signal from an external unit (not shown), and the timing controller **170** responsively generates a gate control signal and a data control signal, and then supplies the generated control signals to the first and second level shifters **150** and **160** and to the data driving circuit **120**. In one embodiment, the data is an RGB video signal. The data control signal includes a load signal, and the input control signal includes a vertical synchronizing signal, a horizontal synchronizing signal, a main clock, and a data enable signal. As already mentioned, the timing controller **170** receives a clipped reset signal (CREsig) from the clipping unit **190**. In response to the received clipped reset signal (CREsig), the timing controller **170** adjusts a timing of the load signal provided to the data driving circuit **120**.

[0052] The power supply unit **180** generates an analog driving voltage, a common voltage VCOM, and a gate driving voltage using a power voltage supplied from an external unit. The power supply unit **180** supplies the analog driving voltage to the data driving circuit **120**. The power supply unit **180** supplies the common voltage VCOM to the common electrode of the LCD panel **110**. And, the power supply unit **180** supplies the gate driving voltage to the first and second level shifters **150** and **160**.

[0053] The clipping unit **190** receives a reset signal REsig from the first gate driving circuit **130**, clips the received signal, and then provides the clipped reset signal CREsig to the timing controller **170**.

[0054] The clipped reset signal CREsig is the signal resulting from restricting the reset signal REsig to a voltage level that can be handled by the timing controller **170**. The reset signal REsig is the signal of a gate-on voltage VON or gate-off voltage VOFF outputted from a dummy stage of the gate driving circuit **130** to reset the first gate driving circuit **130** at the end of each vertical scan of the display. Thus the reset signal REsig can be combined with the start of scan signal (vertical synch signal) to indicate the cumulative delay of the first gate driving circuit **130** in its operation of sequentially activating all of the display rows, one after the next. Then the per-line delay can be calculated by dividing the measured delay by the total number of scanned lines. It is to be understood that although one is not shown an appropriate arithmetic logic unit or microcontroller or microprocessor may be used for generating the calculated per-row correction amount and that such a calculating means is provided with a number indicating the predetermined number of rows in the given display. Note that the output of the dummy STAGE(n+1) is loaded by the Reset inputs of all the stages as well as by the input of clipping circuit **190**. It is desirable but not necessary to load the output of the dummy STAGE(n+1) to have an approximately same load as that of the other stages. To this end, the gate line (GL(n+1)) of the dummy STAGE(n+1) may have a same or lesser number of dummy gate pads attached to it as may be appropriate for approximately simulating the output loadings on the other stages.

[0055] In one embodiment (see FIG. **9***c*), the clipping unit **190** includes a clipping circuit for outputting a clipped reset signal CREsig by restricting respective high and low amplitudes of a reset signal REsig having the gate-on voltage VON and the gate-off voltage VOFF to 3.3V level and to ground. Those skilled in the art have numerous acceptable designs to choose from for implementing the clipping circuit that performs this function (see FIG. **9***c*). So, details of a specific clipping circuit are omitted here.

[0056] In one embodiment, the timing controller **170**, the first and second level shifters **150** and **160**, the power supply unit **180** and the clipping unit **190** are mounted on a control printed circuit board **104**. The control printed circuit board **104** is connected to the second peripheral area PA**2** of the TFT substrate **112** via the flexible printed circuit board **102**. The first and second gate driving circuits **130** and **140** provided to the LCD panel **110** are connected to the timing controller **170** and the power supply unit **180** via the data driving circuit **120** or can be directly connected to the timing controller **170** and the power supply unit **170** via the flexible printed circuit board **102**.

[0057] FIG. **2** is a block diagram to explain in more detail an input/output signal relation of a timing controller **170** in one embodiment according to FIG. **1**.

[0058] Referring to FIG. **2**, the timing controller **170** provides an output enable signal OE, a gate clock signal CVP, and a gate start signal STV to each of the first and second level shifters **150** and **160**. And, the timing controller **170** adjusts a timing of a load signal (TP) and then provides it to the data driving circuit **120** in response to the timing of the clipped reset signal CREsig as received from the clipping unit **190**.

[0059] Meanwhile, the first and second level shifters **150** and **160** are provided with the gate-on voltage VON and gate-off voltage OFF as the gate line driving voltages by the power supply unit **180** and they are also provided with the output enable signal OE, the gate clock signal CPV, and the gates scan start signal STV as gate control signals by the timing controller **170**. The first and second level shifters **150** and **160** generate a corresponding start pulse STVP that transitions between the levels of the gate-on voltage VON and gate-off voltage VOFF, a gate clock pulse CKV, and a gate clock bar pulse CKVB (inverted gate clock). The first and second level shifters **150** and **160** then supply the generated pulses to the first and second gate driving circuits **130** and **140** via the data driving circuit **120**.

[0060] The gate start signal STV is the signal indicating a start of one frame. The start pulse STVP is the signal for enabling the gate driving circuit **130** or **140** to generate a first gate driving signal in one frame. The gate clock pulse CKV and the inverted gate clock bar pulse CKVB are the clocks having 180 degree phases with respect to each other and are used to synchronize the driving of respective gate lines between the VON and VOFF states.

[0061] FIG. **3** is a block diagram of an embodiment of the timing controller **170** which may be used in FIG. **2**.

[0062] Referring to FIG. **3**, the illustrated timing controller **170** includes an output enable signal generator **172**, a counter **174**, and a load signal generator **176**.

[0063] The output enable signal generator **172** provides a last output enable signal LASTOE of one frame to the counter **174**. What is meant here by the last output enable signal LASTOE of one frame is that it corresponds in timing the output enable signal OE used to generate a gate clock pulse CKV provided to an end dummy stage at the end of the serial sequence of live stages used to form the gate lines activating shift register. The dummy stage is fabricated with the same fabrication process used for the other stages of the shift register and thus its response delay is representative of that of the other stages.

[0064] The counter **174** generates a clock counter signal CLOCKCOUNT representing the timing difference between a rising timing point of a clipped reset signal CREsig with a corresponding rising timing point of the last output enable signal LASTOE (see FIG. **9**D). The counter **174** then provides the clock counter signal to the load signal generator **176**. The clock counter signal CLKCOUNT is the signal resulting from counting the delay time of a gate driving signal in terms of a reference system clock.

[0065] The load signal generator **176** adjusts a falling timing point of the load signal TP in response to the clock counter signal CLKCOUNT. This is because the data driving circuit **120** outputs new data for the data lines at the falling timing point of the load signal TP (see FIG. **7**).

[0066] Since the LCD device according to one embodiment of the present disclosure is able to adjust the load time (e.g., falling edge of the TP pulse) so as to compensate for an output delay of a gate driving signal by the gate driving circuit in a manner of having a representative reset signal (REsig) of the gate driving circuit fed back to it, the exemplary design is able to solve the problem that luminance becomes lower than that of data originally displayed by a pixel connected to a gate line provided to a lower part of an LCD panel due to a gate driving signal applied later than a data output according to a delay of the gate driving circuit itself.

[0067] FIG. **4** is a circuit diagram of an embodiment for the first level shifter shown in FIG. **1**. The first level shifter **150**

includes a first level shifting unit **152**, a second level shifting unit **154**, and a third level shifting unit **156**.

[0068] The first level shifting unit **152** generates a gate clock pulse CKV that transitions between VON and VOFF and is supplied to the first gate driving circuit. The level-shifted clock pulse CKV is generated by performing a first logical operation, LG**1** (i.e., OR, AND, etc.) on an output enable signal, OE and a supplied gate clock signal, CPV and amplifying the high and low voltage levels. For this, the first level shifting unit **152** includes a logical operation unit LG**1**, a driving inverter INV**1**, and a full swing CMOS inverter **153** as shown.

[0069] In one embodiment, the first logical operation unit LG**1** performs an OR operation on the output enable signal OE and the gate clock signal CPV. The driving inverter INV**1** inverts the output of the logical operation unit LG**1** and then amplifies it into a driving level of the full swing inverter **153**. The full swing inverter **153** inverts the clock signal a second time and generates a gate clock pulse CKV at a level of a gate-on/off voltages VON/VOFF in response to an output of the driving inverter INV**1**.

[0070] The second level shifting unit **154** supplies a gate clock bar pulse CKVB to the first gate driving circuit by performing a second logical operation LG**2** on an output enable signal OE and a gate clock signal CPV and amplifying a voltage level. For this, the second level shifting unit **154** includes a logical operation unit LG**2**, a logical inverter INV**2**, a driving inverter INV**3**, and a full swing inverter **155**. The gate clock bar signal CKVB is a clock resulting from inverting a phase of the gate clock pulse CKV.

[0071] The logical operation unit LG**2** performs an OR operation on the output enable signal OE and the gate clock signal CPV. The logic inverter INV**2** inverts to output an output of the logical operation unit LG**1**. The driving inverter INV**3** inverts a phase of an output of the inversion inverter INV**2** and then amplifies it to a driving level of the full swing inverter **155**. The full swing inverter **155** generates a gate clock bar pulse CKVB at a level of a gate-on/off voltage VON/VOFF in response to an output of the driving inverter INV**3**.

[0072] The third level shifting unit **156** receives an output enable signal OE and a gate start signal STV and then generates a start pulse STVP at a level of a gate-on/off voltage VON/VOFF. The start pulse STVP has the same cycle and pulse width as a gate start pulse STV and has a level of a gate-on/off voltage VON/VOFF. This may be accomplished with a circuit similar to **152** except that LG**1** is replaced with an AND function.

[0073] The configuration of the second level shifter **160** is substantially the same as the configuration of the first level shifter **150** and further detailed description thereof is therefore omitted for brevity.

[0074] FIG. **5** is a block diagram of a detailed implementation for the first and second gate driving circuits shown in FIG. **1**.

[0075] Referring to FIG. **5**, the first and second gate driving circuits **130** and **140** are arranged adjacent to both sides of a display area DA to dually drive the operational gate lines GL**1** to GLn, respectively. However, as seen, there is one additional gate line, GL_{n+1} and one extra drive stage (n+1) on each side. The first and second gate driving circuits **130** and **140** have a symmetric structure based on the gate lines GL**1** to GLn.

[0076] The first gate driving circuit **130** includes an interconnect lines unit **134** and a circuit unit **132**. The lines unit **134** receives various signals from a data driving unit and then supplies the received signals to the circuit unit **132**. The circuit unit **132** sequentially outputs gate driving signals for activating the gate lines GL**1** through GLn and then GLn+1 one after the other in response to the various signals delivered via the lines unit **134**.

[0077] The circuit unit **132** includes a shift register having a plurality of stages STAGE**1** to STAGEn+1 that are serially connected one to the next as shown. The first to n^{th} stages of STAGE**1** to STAGEn+1 are electrically connected to the first to n^{th} gate lines GL**1** to GLn to sequentially output the gate driving signals, respectively. In this case, the $(n+1)^{th}$ stage STAGEn+1 is a dummy stage. In one embodiment, n is an even number.

[0078] Each of the n+1 stages, STAGE**1** to STAGEn+1 includes a first clock terminal CK**1**, a second clock terminal CK**2**, an input terminal IN, a control terminal CT, an output terminal OUT, a reset terminal RE, a carry terminal CR, and a ground voltage terminal VSS.

[0079] For the odd-numbered stages, STAGE**1**, STAGE**3**, . . . , and STAGEn+1 (assuming n is even), the noninverted gate clock pulse CKV is provided to the first clock terminal CK**1** and the inverted gate clock bar pulse CKVB is provided to the second clock terminal CK**2**. For the even-numbered stages STAGE**2**, STAGE**4**, . . . , and STAGEn (assuming n is even), the inverted gate clock bar pulse CKVB is provided to the first clock terminal CK**1** and the noninverted gate clock pulse CKV is provided to the second clock terminal CK**2**.

[0080] In the stages STAGE**2** to STAGEn+1, the input terminal IN of a Jth stage is connected to the carry terminal CR of a previous (J−1) stage so as to be provided with a carry signal of the previous stage. The IN terminal of stage**1** receives the STVP signal. The control terminal CT of each Jth stage is connected to the output terminal OUT of a next (J+1) stage so as to be provided with an output signal of the next stage, the exception being Stage(n+1) whose CT terminal connects to the STVP line (SL**1**). Since the first stage STAGE**1** is not provided with the previous stage, the start pulse STVP is provided to the input terminal IN of the first stage STAGE**1**. The carry signal outputted from the carry terminal CR of each stage drives the IN terminal of the next stage, the exception being Stage(n+1). Also as seen, the output (OUT terminal) of the dummy Stage(n+1) connects to the SL**5** line where the latter couples to the Reset terminals of all the stages in unit **130** and also to the input of the clipper **190**.

[0081] Since the start pulse STVP is provided to the control terminal CT of the dummy stage STAGEn+1, the latter STAGEn+1 is blocked from outputting a VON level at start-up as shall be understood shortly (see FIG. **6**). The OUT terminal of stage STAGEn+1 provides a carry signal to the control terminal CT of the n^{th} stage STAGEn. A gate-off voltage VOFF is provided to the local ground voltage terminal VSS of each of the stages STAGE**1** to STAGEn+1. As mentioned, output signal of the $(n+1)^{th}$ dummy stage STAGEn+1 is provided to the reset terminals RE by way of line SL**5**.

[0082] The output terminal OUT of each of the odd-numbered stages STAGE**1**, STAGE**3**, . . . , and STAGEn+1 can output a VON level synchronized to the noninverted gate clock pulse CKV as its gate line driving signal and the carry terminal CR can similarly output a VON level synchronized to the noninverted gate clock pulse CKV as its carry signal. The output terminal OUT of the even-numbered stages

STAGE2, STAGE4, . . . , and STAGEn can output a VON level synchronized to the inverted gate clock bar pulse CKVB as its gate driving signal and the carry terminal CR can similarly output a VON level synchronized to the inverted gate clock bar pulse CKVB as its carry signal.

[0083] In the illustrated structure of the first gate driving circuit **130**, each of the odd-numbered stages STAGE1, STAGE3, . . . , and STAGEn+1 is thus synchronized with the noninverted gate clock pulse CKV to output a respective gate driving signal and each of the even-numbered stages STAGE2, STAGE4, . . . , and STAGEn is synchronized with the inverted gate clock bar pulse CKVB to output a respective gate driving signal.

[0084] The output terminals OUT of the stages STAGE1 to STAGEn+1 of the first gate driving circuit **130** are connected to the gate lines GL1 to GLn provided to the display area DA, respectively and then sequentially drive the gate lines GL1 to GLn by sequentially supplying the gate driving signals to the gate lines GL1 to GLn.

[0085] The lines unit **134** is provided in the vicinity of the circuit unit **132**. The lines unit **134** includes a start pulse line SL1, a gate clock pulse line SL2, a gate clock bar pulse line SL3, a ground voltage line SL4, and a reset line SL5, which extend in parallel with each other.

[0086] The start pulse line SL1 receives a start pulse STVP from the first level shifter and then inputs the received pulse to the input terminal of the first stage STAGE1 and the control terminal CT of the $(n+1)^{th}$ stage STAGEn+1.

[0087] The gate clock line SL2 receives a gate clock pulse CKV from the first level shifter and then provides the received pulse to the first clock terminals CK1 of the odd-numbered stages STAGE1, STAGE3, . . . , and STAGEn+1 and the second clock terminals CK2 of the even-numbered stages STAGE2, STAGE4, . . . , and STAGEn.

[0088] The gate clock bar line SL3 receives the inverted gate clock bar pulse CKVB from the first level shifter **150** and provides the received pulse to the second clock terminals CK2 of the odd-numbered stages STAGE1, STAGE3, . . . , and STAGEn+1 and the first clock terminals CK1 of the even-numbered stages STAGE2, STAGE4, . . . , and STAGEn.

[0089] The ground voltage line SL4 receives the gate-off voltage VOFF from the power supply unit **180** and then supplies the received voltage to the local ground voltage terminals VSS of the stages STAGE1 to STAGEn+1.

[0090] The reset line SL5 provides the output signal of the output terminal OUT of the $(n+1)^{th}$ stage STAGEn+1 as a reset signal REsig to the reset terminals RE of the stages STAGE1 to STAGEn+1. Moreover, the reset line SL5 provides the clipping unit **190** with the output signal of the output terminal OUT of the $(n+1)^{th}$ stage STAGEn+1.

[0091] The first and second gate driving circuits **130** and **140** have symmetric structures as shown relative to the gate lines GL1 to GLn. It will be apparent from FIG. **5** to those skilled in the art that the second gate driving circuit **140** can be implemented according to the above description of the first gate driving circuit **130**. So, details of the second driving circuit **140** will be omitted in the following description for sake of brevity. The one exception is that the Reset line of the right side circuit portion **140** does not need to connect to clipping unit **190**. Of course in an alternate embodiment, clipping unit **190** can receive the Reset pulse of the right side circuit portion **140** instead of that from the left.

[0092] The LCD device according to the illustrated embodiment is thus configured to dually drive the gate lines by providing a pair of the equivalent gate driving circuits to both sides of the gate lines, respectively. Hence, the illustrated embodiment is able to overcome the problem of luminance differences between two adjacent gate lines at both ends of the left and right sides of the gate lines due to the gradually delayed outputs of the gate driving signal toward the end of the corresponding gate line in the case where gate lines are driven only from one end and adjacent gate lines are driven from opposite ends.

[0093] FIG. **6** is an exemplary circuit diagram of the stage of the first gate driving circuit shown in FIG. **5**.

[0094] Referring to FIG. **6**, the first stage STAGE1 includes an output pull-up unit **132***a* (transistor NT1), an output pull-down unit **132***b* (transistor NT2), a driving unit **132***c*, a holding unit **132***d*, a switching unit **132***e*, and a carry unit **132***f*.

[0095] The pull-up unit **132***a* receives its power from the noninverted gate clock pulse CKV as provided via the first clock terminal CK1 and the pull-up unit **132***a* outputs a gate driving signal GO1 via the output terminal OUT where GO1 can go high when CKV goes high. The pull-up unit **132***a* includes a first NMOS transistor NT1 having a gate connected to a first node N1, a drain connected to the first clock terminal CK1, and a source connected to the output terminal OUT. (First capacitor C1 straddles between the gate and source of NT1.)

[0096] The pull-down unit **132***b* (NT2) is structured to pull down the gate driving signal GO1 to the VOFF level in response to a going high state of a gate driving signal GO2 provided from the second stage (STAGe2). In the illustrated embodiment, the pull-down unit **132***b* includes a second NMOS transistor NT2 having a gate connected to the control terminal CT, a drain connected to the output terminal OUT, and a source connected to the local ground voltage terminal VSS.

[0097] The driving unit **132***c* turns on the pull-up unit **132***a* in response to a start pulse STVP provided via the input terminal IN or turns off the pull-up unit **132***a* in response to the gate driving signal GO2 of the second stage. For this, the driving unit **132***c* includes a buffer unit, a charge unit, and a discharge unit.

[0098] The buffer unit includes a third NMOS transistor NT3 in a diode configuration where its gate and drain are commonly connected to the input terminal IN and a source connected for charging up the first node N1. The charge retaining unit includes a first capacitor C1 having a first electrode connected to the first node N1 (gate of NT1) and a second electrode connected to a second node N2 (source of NT1). The discharge unit includes a fourth NMOS transistor NT4 having a gate connected to the control terminal CT (G02), a drain connected to the first node N1, and a source connected to the ground voltage terminal VSS so as to be able to selectively drive N1 low when GO2 goes high.

[0099] If a start pulse STVP is inputted to the input terminal IN, the third transistor NT3 is turned on in response to the pulse input and the first capacitor C1 is thereby charged with the start pulse STVP. If the first capacitor C1 is charged over a threshold voltage of the first transistor NT1, the first transistor NT1 is turned on and then outputs a high level corresponding to the noninverted gate clock pulse CKV, which high level (VON) is to be provided to the output terminal OUT at the appropriate time.

[0100] In this case, a potential of the first node N1 becomes boot-strapped to track potential variations of the second node N2 due to coupling by the charged first capacitor C1 from N2

to N1. Accordingly if there is an abrupt downward potential change on the second node N2 due for example to NT2 turning on, the potential on N1 will head downward as well. On the other hand, if there is an abrupt upward potential change on the second node N2 due for example to GO1 going high, the potential on N1 will head upward as well. So, the first transistor NT1 is facilitated to output the first gate clock pulse CKV applied to the drain to the output terminal OUT when GO1 starts going high in response to NT3 charging up the first capacitor C1. The gate clock pulse CKV outputted to the output terminal OUT becomes the gate driving signal GO1 provided to a gate line. The start pulse STVP is used as a signal for preliminarily charging the first capacitor C1 and thus turning on the first transistor NT1 to generate a first going high gate driving signal GO1.

[0101] Subsequently, if the fourth transistor NT4 is turned on in response to the gate driving signal G02 as the output signal of the second stage which is inputted via the control terminal CT, charges in the first capacitor C1 are discharged to a level of a gate-off voltage VOFF provided via the ground voltage terminal VSS.

[0102] The holding unit **132***d* includes fifth and sixth transistors NT5 and NT6 for holding the gate driving signal GO1 in a status of the gate-off voltage (VOFF) level. The fifth transistor NT5 has a gate connected to a third node N3, a drain connected to the second node N2, and a source connected to the ground voltage terminal VSS. The sixth transistor NT6 has a gate connected to the second clock terminal CK2, a drain connected to the second node N2, and a source connected to the ground voltage terminal VSS.

[0103] The switching unit **132***e* includes seventh to tenth transistors NT7 to NT10 and second and third capacitors C2 and C3 to control the holding unit **132***d* to be driven. The seventh transistor NT7 has gate and drain connected to the first clock terminal CK1 and a source commonly connected to a drain of the ninth transistor NT9 and a gate of the eighth transistor NT8. The eighth transistor NT8 has a drain connected to the first clock terminal CK1, a gate connected to the drain of the seventh transistor NT7 via the second capacitor C2, and a source connected to the third node N3. In particular, the gate and the source of the eighth transistor NT8 are connected to each other via the third capacitor C3. The ninth transistor NT9 has a drain connected to the source of the seventh transistor NT7, a gate connected to the second node N2, and a source connected to the ground voltage terminal VSS. The tenth transistor NT10 has a drain connected to the third node N3, a gate connected to the second node N2, and a source connected to the ground voltage terminal VSS.

[0104] If a gate clock pulse CKV in a high state is outputted to the output terminal OUT as the gate driving signal G0, a potential of the second node N2 is raised to a high state. If the potential of the second node N2 is raised to the high state, each of the ninth and tenth transistors NT9 and NT10 is switched to a turned-on mode. In this case, although both of the seventh and eighth transistors NT7 and NT8 are switched to the turned-on state by the gate clock pulse CKV provided to the first clock terminal CK1, signals outputted from the seventh and eighth transistors NT7 and NT8 are discharged to a ground voltage (VOFF) state via the ninth and tenth transistors NT9 and NT10, respectively. Since the potential of the third node N3 is maintained at the low state while the gate driving signal GO1 of the high state is outputted, the fifth transistor NT5 can maintain the turned-on state.

[0105] Subsequently, when the high state of the gate driving signal GO1 is discharged via the ground voltage terminal VSS in response to the gate driving signal GO2 going high, the potential of the second node N2 gradually falls to a low state. So, each of the ninth and tenth transistors NT9 and NT10 is switched to a turned-off state and a potential of the third node N3 is raised to a high state by signals outputted from the seventh and eighth transistors NT7 and NT8. As the potential of the third node N3 is raised, the fifth transistor NT5 becomes turned on. And, the potential of the second node N2 is discharged to a gate-off voltage (VOFF) state via the fifth transistor NT5.

[0106] While this status is maintained, if the sixth transistor NT6 is turned on by the inverted gate clock bar pulse CKVB provided to the second clock terminal CK2, the potential of the second node N2 can be discharged via the ground voltage terminal VSS more surely.

[0107] Consequently, the fifth and sixth transistors NT5 and NT6 of the holding unit **132***d* hold the potential of the second node N2 at the gate-off voltage (VOFF) state. And, the switching unit **132***e* decides a timing point at which the fifth transistor NT5 is turned on.

[0108] The carry unit **132***f* includes an eleventh transistor NT11 having a drain connected to the first clock terminal CK1, a gate connected to the first node N1, and a source connected to the carry terminal CR. The eleventh transistor NT11 is turned on as the potential of the first node N1 rises. The eleventh transistor NT11 then outputs a gate clock pulse CKV inputted to the drain as a carry signal CAsig1. The carry signal is provided to an input terminal of a next stage to be used as a start pulse for driving the next stage.

[0109] The first stage STAGE1 further includes a ripple preventing unit **132***g* and a reset unit **132***h*. The ripple preventing unit **132***g* prevents the gate driving signal GO1 already maintained at the gate-of voltage (VOFF) state from being rippled by noise inputted via the input terminal IN. For this, the ripple preventing unit **132***g* includes a twelfth and thirteenth transistors NT12 and NT13. The twelfth transistor NT12 has a drain connected to the input terminal IN, a gate connected to the second clock terminal CK2, and a source connected to the first node N1. The thirteenth transistor NT13 has a drain connected to the first node N1, a gate connected to the first clock terminal CK1, and a source connected to the second node N2.

[0110] The reset unit **132***h* includes a fourteenth NMOS transistor NT14 having a drain connected to the first node N1, a gate connected to the reset terminal RE, and a source connected to the ground voltage terminal VSS. The fourteenth transistor NT14 causes the second node N2 to become discharged to the gate-off voltage (VOFF) state in response to the reset signal REsig going high, where the latter is an output signal of the $(n+1)^{th}$ stage STAGEn+1. Since the reset signal REsig corresponding to the output signal of the $(n+1)^{th}$ stage STAGEn+1 means an end of one frame, activation of the reset unit **132***h* corresponds to all the first nodes N1 of all the stages STAGE1 to STAGEn being driven low simultaneously at the timing point at which one frame ends.

[0111] In particular, the reset unit **132***h* resets the first nodes N1 of the stages STAGE1 to STAGEn in a manner of turning on the fourteenth transistors NT14 of the stages STAGE1 to STAGEn by the output signal of the $(n+1)^{th}$ stage STAGEn+1 after completion of outputting the gate driving signals from the stages STAGE1 to STAGEn sequentially.

Hence, the stages STAGE1 to STAGEn of the circuit unit **132** can restart their operations in a reset state.

[0112] In the illustrated embodiment, the reset signal REsig is used as a feed back signal to the timing controller **170** for allowing the controller **170** to measure the delay time between activation of the first stage of the shift register (by way of an OE signal) and the subsequent, ripple-induced activation of the dummy gate driving signal due to inherent delays within the gate driving circuit and to then calculate the approximate per-display-row accumulating delay associated with the stages of the shift register. Of course, it is to be understood that all of the second to $(n+1)^{th}$ stages shown in FIG. **5** are implemented with the same internal configuration of the above-explained first stage of FIG. **6**. So, details of the second to $(n+1)^{th}$ stages are omitted in the following description.

[0113] FIG. **7** is an operational timing diagram (voltage levels versus a common time line) of the LCD device shown in FIG. **1**.

[0114] Referring to FIG. **7**, the first and second level shifters **150** and **160** generate the noninverted gate clock pulse CKV and the inverted gate cock bar pulse CKVB with the gate-on voltage level VON and the gate-off voltage level VOFF by performing the above-described OR operation on the output enable signal OE and the gate clock signal CPV provided by the timing controller **170**. Each of the odd-numbered stages STAGE**1**, STAGE**3**, . . . , and STAGEn+1 of the first and second gate driving circuits **130** and **140** outputs a gate clock pulse CKV as a gate driving signal. Each of the even-numbered stages STAGE**2**, STAGE**4**, . . . , STAGEn outputs a gate clock bar pulse CKVB as a gate driving signal.

[0115] The timing controller **170** enables the data driving circuit **120** to provide a gray scale display voltage to the data line in a manner of synchronizing a falling timing point of a load signal TP at a timing point at which a gate driving signal sequentially provided to each of the gate lines GL**1** to GLn rises to a high level. If the gate driving signal is delayed by inherent delays within the gate driving circuits **130** and **140**, the falling timing point of the load signal TP is correspondingly delayed by an amount of time compensating for the propagation delay of the gate driving circuits **130**/**140**. Hence, the feedback system is able to solve the problem caused by the gate driving signals being differently delayed by the gate driving circuits **130** and **140** depending on factors such as variation in fabrication process, variation in temperature, variation in power supply levels and so on.

[0116] A method of compensating for a delay caused by a gate driving circuit in a manner of feeding back a reset signal of a gate driving circuit using an LCD device according to one embodiment is explained in detail with reference to FIGS. **8** and **9**A to **9**D as follows. FIG. **8** is a flowchart of a method of decreasing ASG delay according to one embodiment while FIGS. **9**A to **9**D are timing diagrams of signals to explain the ASG delay decreasing method shown in FIG. **8**.

[0117] Referring to FIG. **8**, a method of decreasing ASG delay according to one embodiment includes a horizontal line phenomenon analyzing step S**100**, a rest signal feedbacking step S**200**, a reset signal clipping step S**300**, a delay time measuring and calculating step S**400**, and a load signal timing adjusting step S**500**.

[0118] In the horizontal line phenomenon analyzing step S**100**, when the gate driving circuits **130** sequentially apply gate driving signals to the gate lines GL**1** to GLn, a horizontal line phenomenon, which occurs if a gate driving signal is applied later than a data output due to delays of the gate driving circuits **130** and **140**, is analyzed.

[0119] Referring to FIG. **9**A, outputs of the gate driving signals provided to the gate lines GL**1** to GLn are gradually (cumulatively) delayed due to rippling of sequential GO signals toward the lower part of the LCD panel **110** where the cumulative delays are due to individual delays of the gate driving circuits **130** and **140** themselves. For instance, while gate lines are sequentially driven, if a gray scale display voltage corresponding to red (R), green (G) or blue (B) is supplied to a pixel connected to the corresponding gate line, a gate driving signal tends to be more delayed toward the lower part of the LCD panel **110** than near its top as is indicated in FIG. **9**A. So, the pixel connected to the corresponding lower gate line might be incorrectly displayed as a color different from an original color supposed to be displayed if the cumulative delay is large enough.

[0120] In case that gate lines G**2** and Gn−1, to which a gray scale display voltage for green (G) is applied, are compared to each other, pixels connected to the gate line G**2** are normally provided with a gray scale display voltage corresponding to green for a section having a gate driving signal GO**2** in a high level. Yet, a gray scale display voltage corresponding to blue as well as a gray scale display voltage corresponding to green is simultaneously provided to pixels connected to the gate line Gn−1. So, it is unable to display a color supposed to be originally displayed. This is because a gate driving signal is applied later than a data output due to the self-delays of the gate driving circuits **130** and **140**. Hence, the above-mentioned problem can be solved in a manner of compensatingly delaying the timing of the data load signal to approximately match the accumulative delay times of the gate driving signal attributed to the self-delays of the gate driving circuits **130** and **140**.

[0121] The reset signal feedbacking step S**200** is the step of providing the clipping unit **190** with a reset signal REsig as an output signal of the dummy stage STAGEn+1 of the gate driving circuits **130** and **140**. In particular, referring to FIG. **9**B, compared to the hypothetical output signal XREsig of the dummy stage STAGEn+1 in case that no delay is generated by the gate driving circuits **130** and **140**, a reset signal REsig is delayed by a predetermined delay duration, DELAY in case that a delay of a gate driving signal is generated by the gate driving circuit **130**/**140**. In this case, 'OE' and 'CVP' respectively indicate an output enable signal and a gate clock signal used to generate the hypothetical output signal XREsig.

[0122] The reset signal clipping step S**300** is the step of clipping a reset signal REsig to a predetermined voltage level via the clipping unit **190** and then providing the clipped signal to the timing controller **170**. Referring to FIG. **9**C, since the reset signal REsig has a gate-on voltage VON and a gate-off voltage VOFF, a clipped reset signal CREsig is generated by converting the reset signal REsig to a signal at voltage levels controllable in the timing controller **170**, e.g., a signal at 0V and 3.3V.

[0123] The delay time calculating step S**400** is the step of measuring and calculating a delay time of a gate driving signal using the clipped reset signal CREsig and a last output enable signal LASTOE. If there is no delay of the gate driving signal, a reset signal REsig outputted from the dummy stage STAGEn+1 is outputted at a rising timing point of the last output enable signal LASTOE and data should be outputted at a falling timing point of a load signal TP. So, it is able to calculate the delay time of the gate driving signal using the

clipped reset signal CREsig and the last output enable signal LASTOE. In this case, the measured delay time obtained from the gate driving signal of the dummy stage is used to calculate the per-row delay and the latter is repeatedly used to cumulatively over time adjust the timing of the falling edge of the load signal TP so as to approximately match the cumulative delays produced over time by the VON level rippling through the STAGe**1** through STAGen of the shift register.

[0124] The delay time of the gate driving signal can be calculated via Formulas 1 to 3 as follows.

$$1H_{ideal}=1\text{Frame}_{ideal}\div Gn \quad \text{[Formula 1]}$$

[0125] In Formula 1, $1H_{ideal}$ is a one-horizontal cycle in case that it is assumed there is no delay caused by the gate driving circuit **130** or **140**, 1Frame_{ideal} is a one-frame cycle in case that there is no delay caused by the gate driving circuit **130** or **140**, and Gn is the number of total gate lines driven by the shift register.

$$1H_{real}=1\text{Frame}_{real}\div Gn \quad \text{[Formula 2]}$$

[0126] In Formula 2, $1H_{real}$ is a one-horizontal cycle in case that there is a delay caused by the gate driving circuit **130** or **140**, 1Frame_{real} is a one-frame cycle in case that there is a delay caused by the gate driving circuit **130** or **140**, and Gn is the number of total gate lines.

$$T_{TP}=1H_{ideal}\times Gm+(1H_{real}-1H_{ideal})\times Gm\div Gn \quad \{\text{Formula 3}\}$$

[0127] In Formula 3, $1T_{TP}$ is a timing point at which data should be applied to a pixel connected to an m^{th} gate line, i.e., a falling timing point of a load signal and Gm is the m^{th} gate line.

[0128] Referring to FIG. **9**D, a delay time of a gate driving signal is calculated by measuring the delay between a clipped reset signal CREsig and the last output enable signal LASTOE.

[0129] If there is no delay caused by the gate driving circuit **130** or **140**, a rising timing point of the clipped reset signal CREsig should be equal to that of the last output enable signal LASTOE. However, since the reset signal REsig is outputted in a manner of being inherently delayed by rippling through of signals through the physical gate driving circuit **130** or **140**, the rising point of the clipped reset signal CREsig is typically not matched (when measured) with that of the last output enable signal LASTOE.

[0130] So, the delay time of the gate driving signal can be calculated in a manner of comparing the rising timing point of the clipped reset signal CREsig to that of the last output enable signal LASTOE, counting a system clock count corresponding to an interval from the rising point of the output enable signal LATOE to the rising timing point of the clipped reset signal CREsig, and then generating a corresponding clock count signal CLOCKCOUNT.

[0131] The load signal timing adjusting step **S500** is the step of adjusting a falling timing point of a load signal TP in response to the clock count signal CLOCKCOUNT that represents the measured ripple-through delay of the shift register. For instance, if the number of gate lines is 768 and if the clock count signal CLOCKCOUNT is 40, it is calculated into 768/40 (total lines)/(total clock pulses)=19.2 lines per one clock pulse. Hence, it can be observed that a ripple-through delay is generated by the shift register corresponding to 1 clock per every 19.2 lines that are scanned by the shift register. If this is rounded up, a cumulative TP adjusting delay of 1 clock per every 20 consecutive lines can be generated as the approximate adjustment amount per every 20 display lines that are scanned by the shift register.

[0132] Accordingly, data is outputted to pixels connected to the first to 20^{th} gate lines GL**1** to GL**20** in a manner of synchronizing a falling timing point of a load signal TP with a rising timing point of an output enable signal OE corresponding to each gate line. And, data is outputted to pixels connected to the 21^{st} to 40^{th} gate lines GL**21** to GL**40** in a manner of synchronizing a falling timing point of a load signal TP with a timing point delayed by 1 clock period in this exemplary case behind a rising timing point of an output enable signal OE corresponding to each gate line.

[0133] Moreover, data is outputted to pixels connected to the 41^{st} to 60^{th} gate lines GL**21** to GL**40** in a manner of synchronizing a falling timing point of a load signal TP with a timing point delayed by two (2) clocks behind a rising timing point of an output enable signal OE corresponding to each gate line. Besides, a falling timing point of a load signal TP is adjusted in the above manner for the pixels connected to the rest of the gate lines GL**61** to **768**, whereby a delay of a gate driving signal caused by the gate driving circuit **130** or **140** can be compensated for.

[0134] In other words, by adjusting a falling timing point of a load signal TP outputted by one-horizontal cycle using a set 1-frame time and an actual timing point at which a reset signal REsig is outputted from a dummy stage STAGEn+1, a delay of a gate driving signal caused by a self-delay of the gate driving circuit **130** or **140** can be compensated for.

[0135] As described above, gate lines are dually driven by a pair of gate driving circuits which are identical and provided to both sides of the gate lines. And, a reset signal of the gate driving circuit is fed back. Accordingly, the disclosed design compensates for a ripple-through delay which is caused by the serially-connected stages of the gate driving circuit.

[0136] It will be apparent to those skilled in the art in view of the present disclosure that various modifications and variations can be made in the disclosed embodiments without departing from the spirit or scope of the present teachings. Thus, it is intended that the present teachings cover such modifications and variations.

What is claimed is:

1. A liquid crystal display device having a plurality of display rows and comprising:

a timing controller generating an output enable signal and a gate clock signal, the timing controller adjusting a timing of a load signal for deciding a timing point when display data signals will be output for a correspondingly activated row;

a level shifter generating a gate clock pulse in response to the output enable signal and the gate clock;

a gate driving circuit sequentially activating the display rows one after the next by driving a plurality of gate lines by generating a rippling-down first gate driving signal in response to the gate clock pulse; and

a clipping unit providing the timing controller with a second gate driving signal generated by clipping the first gate driving signal when the first gate driving signal is output from a last stage of the gate driving circuit,

wherein the timing controller measures and calculates a delay time of the first gate driving signal by comparing the second gate driving signal with the output enable signal to adjust the timing of the load signal using the delay time.

2. The liquid crystal display device of claim 1, wherein the level shifter generates the gate clock pulse of a gate-on voltage level and a gate-off voltage level.

3. The liquid crystal display device of claim 2, wherein the gate clock pulse comprises a gate clock bar pulse having an inverted phase with respect to a phase of the gate clock pulse.

4. The liquid crystal display device of claim 3, wherein the first gate driving signal comprises a reset signal for resetting the gate driving circuit.

5. The liquid crystal display device of claim 4, wherein the gate driving circuit is integrated on a liquid crystal display panel having the gate lines formed thereon and is dually formed at both ends of the gate lines to dually drive the data lines.

6. The liquid crystal display device of claim 5, wherein the gate driving circuit includes a shift register having a plurality of stages dependently connected to each other.

7. The liquid crystal display device of claim 6, wherein the plurality of stages are connected to the plurality of gate lines, respectively.

8. The liquid crystal display device of claim 7, wherein the plurality of stages include a dummy stage generating the reset signal.

9. The liquid crystal display device of claim 8, wherein the timing controller comprises:

an output enable signal generator providing a last output enable signal of one frame;

a counter generating a clock count signal by comparing the clipped reset signal and the last output enable signal of the one frame; and

a load signal generator adjusting the timing of the load signal in response to the clock count signal.

10. A liquid crystal display device comprising:

a gate driving circuit generating a gate driving signal including a reset signal; and

a timing controller calculating a delay time of the gate driving signal by comparing the reset signal and an output enable signal corresponding to the reset signal, the timing controller adjusting a timing of a load signal for deciding a data output timing point in response to the delay time.

11. The liquid crystal display device of claim 10, further comprising a clipping unit providing the timing controller with a clipped reset signal generated by clipping the reset signal.

12. The liquid crystal display device of claim 11, the timing controller comprising:

an output enable signal generator providing the output enable signal;

a counter generating a clock count signal by comparing the clipped reset signal and a last output enable signal of one frame; and

a load signal generator adjusting the timing of the load signal in response to the clock count signal.

13. The liquid crystal display device of claim 12, wherein the gate driving circuit comprises a shift register having a plurality of stages dependently connected to each other and wherein each of the plurality of stages includes a dummy stage generating the reset signal.

14. The liquid crystal display device of claim 13, wherein the counter generates as the clock count signal the number of clocks corresponding to an interval from a rising timing point of the output enable signal to a rising timing point of the clipped reset signal.

15. The liquid crystal display device of claim 14, wherein the load signal generator calculates a delay time of the gate driving signal by dividing the number of gate lines provided with the gate driving signal by a value of the clock count signal and delays a falling timing point of the load signal corresponding to the calculated delay time of the gate driving signal.

16. A method of decreasing a delay of a gate driving signal, comprising:

a reset signal feedback step of feeding back a reset signal that is an output signal of a dummy stage of a gate driving circuit to a timing controller;

a delay time calculating step of calculating a delay time of a gate driving signal generated from the gate driving circuit by comparing the reset signal to an output enables signal corresponding to the reset signal; and

a load signal timing adjusting step of adjusting a timing of a load signal for deciding an output timing point of data in response to the delay time.

17. The method of claim 16, wherein the reset signal feedback step comprises clipping the reset signal to a predetermined voltage level and then feeding back the clipped reset signal to the timing controller.

18. The method of claim 17, wherein the delay time calculating step comprises generating a clock count signal by counting the number of clocks corresponding to an interval from a rising timing point of the output enable signal to a rising timing point of the clipped reset signal.

19. The method of claim 18, wherein the load signal timing adjusting step comprises calculating a delay time of the gate driving signal by dividing the number of gate lines provided with the gate driving signal by a value of the clock count signal, and delaying a falling timing point of the load signal corresponding to the calculated delay time of the gate driving signal.

20. The method of claim 19, wherein the reset signal feedback step further comprises analyzing a horizontal line visible phenomenon appearing by the gate driving signal applied later than an output timing point of data due to the delay caused by the gate driving circuit when the gate driving circuit sequentially applies the gate driving signal to a plurality of gate lines.

21. A method for compensating for variable ripple-through delay of plural stages of a shift register used to scan through and sequentially activated rows of a display frame, the method comprising:

(a) following initiation at a first time point of a vertical scan through the display frame, identifying a second time point when an end stage or a dummy end stage of the shift register outputs a corresponding end row or dummy end row activating pulse;

(b) from the difference between the first and second time points and the number of display rows scanned, determining a per-display-row delay associated with the ripple-through delay of the plural stages of the shift register; and

(c) adjusting a third time point at which display data is to be loaded into a display row that is being correspondingly activated by the shift register based on said determined per-display-row delay and on the number of display rows already activated during a current scanning through and activation of rows of a current display frame.

22. A system for compensating for variable ripple-through delay of plural stages of a shift register used to scan through and sequentially activated rows of a display frame, the system comprising:

(a) identifying means responsive to initiation at a first time point of a vertical scan through the display frame, the identifying means being for identifying a second time point when an end stage or a dummy end stage of the shift register outputs a corresponding end row or dummy end row activating pulse;

(b) difference determining means, operatively coupled to the identifying means, for determining from the difference between the first and second time points and the number of display rows scanned, a per-display-row delay or its equivalent that is associated with the ripple-through delay of the plural stages of the shift register; and

(c) adjusting means, responsive to the difference determining means, for adjusting a third time point at which display data is to be loaded into a display row that is being correspondingly activated by the shift register based on said determined per-display-row delay and on the number of display rows already activated during a current scanning through and activation of rows of a current display frame.

* * * * *

专利名称(译)	液晶显示装置，补偿其栅极驱动信号延迟的系统和方法		
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申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	YEO JANG HYUN KIM WOO CHUL PARK JAE HYOUNG		
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摘要(译)

一种液晶显示装置，包括栅极驱动移位寄存器，该栅极驱动移位寄存器具有对称分离的电路部分，通过该电路部分，在LCD装置的行的纹波扫描期间，从栅极线的两端双重驱动多条栅极线中的每一条。 LCD装置包括产生输出使能信号和栅极时钟的定时控制器，其中定时控制器调整负载信号的定时，以在数据将被加载到当前激活的显示行时确定数据输出定时点。数据输出定时点是延迟测量反馈信号的函数，该反馈信号用于测量移位寄存器的顺序连接级的累积延迟。