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(54) LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

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(57) **ABSTRACT**

An LCD and a method of manufacturing the same are provided. The LCD includes first and second substrates defined by a display region and a non-display region, and spaced a predetermined interval apart from each other. The LCD further comprises a liquid crystal layer interposed between the first and second substrates, a conductive part formed on at least one side of the first substrate corresponding to the non-display region. The conductive part has a first dummy pattern formed of metal identical to that of a gate line in the display region. The LCD then comprises a common electrode formed on the second substrate, and a conductive thread pattern that electrically connects the common electrode and the conductive part, and attaches the first and second substrates.

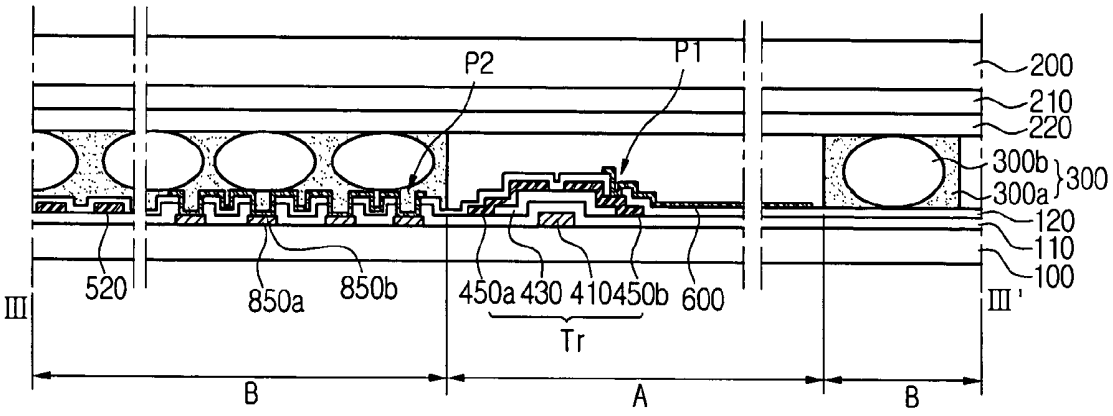


Fig. 1A (Related Art)

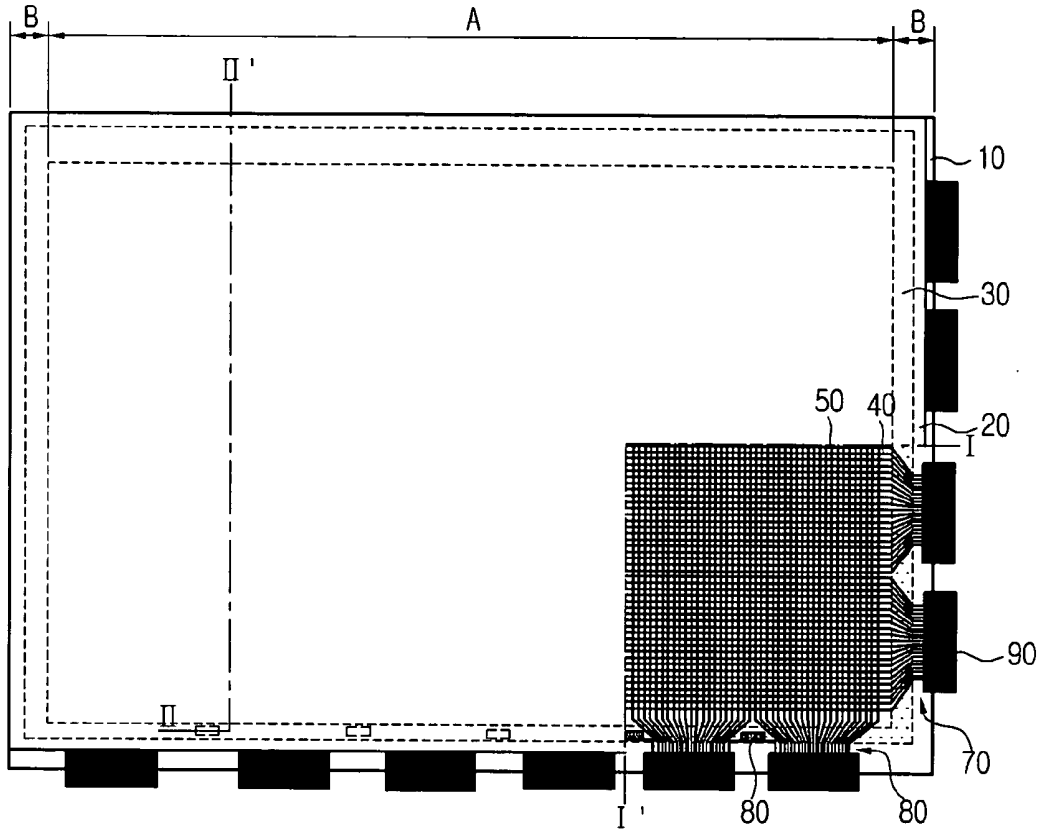


Fig. 1B (Related Art)

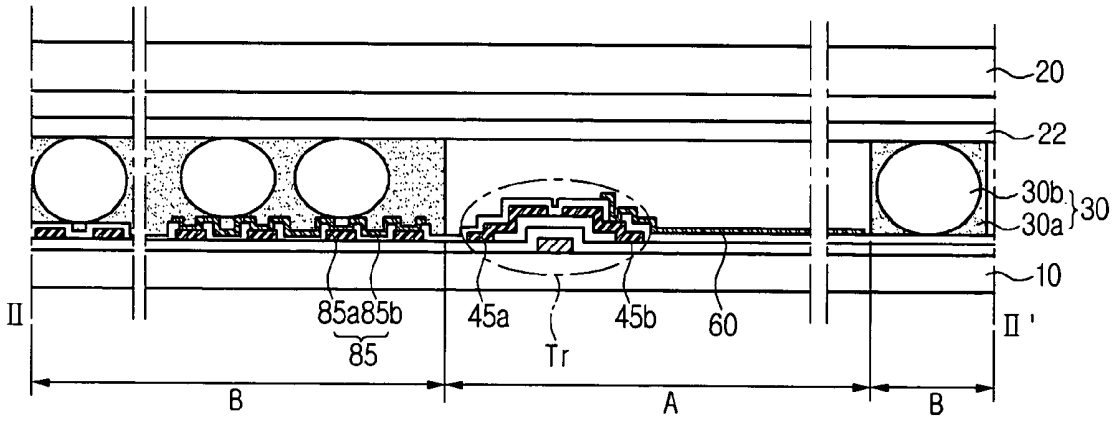


Fig. 2A

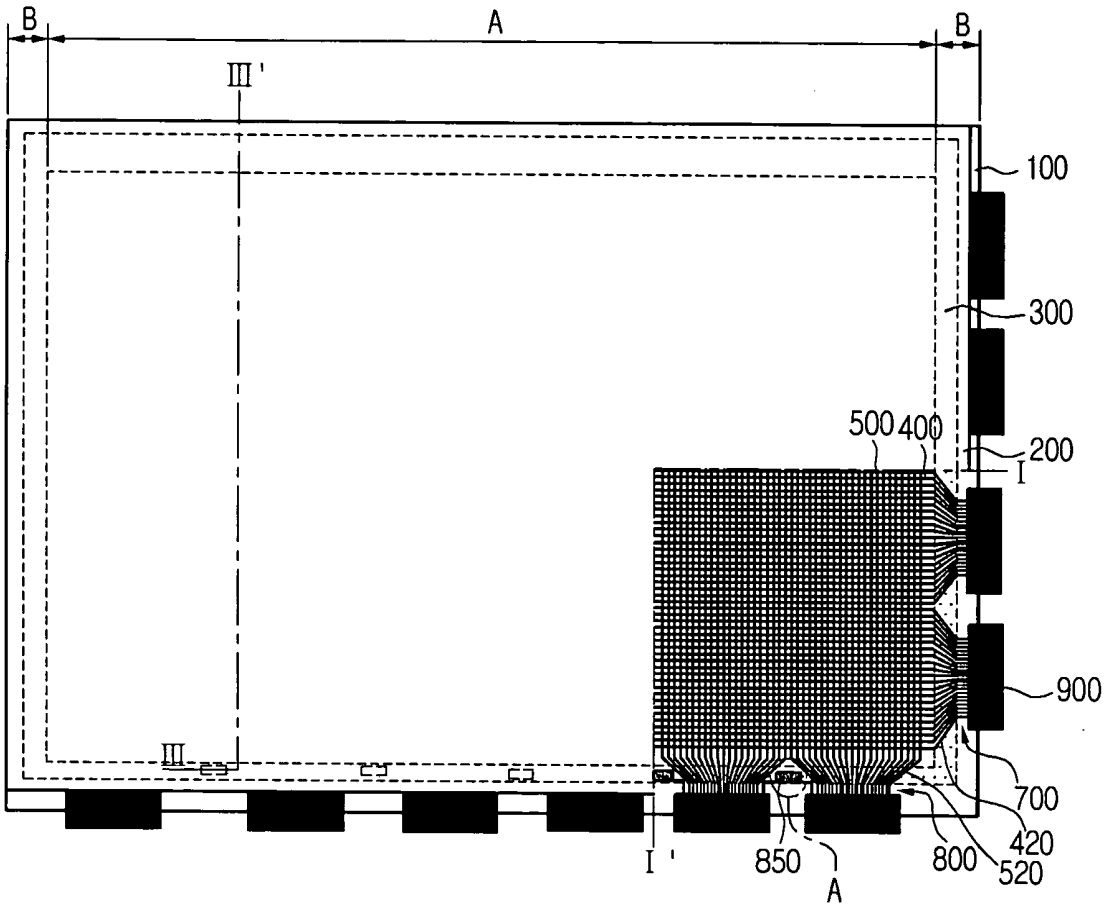

B
A
B
III'
100
300
500
400
200
I
900
III
700
420
520
I'
850
A
800

Fig. 2B

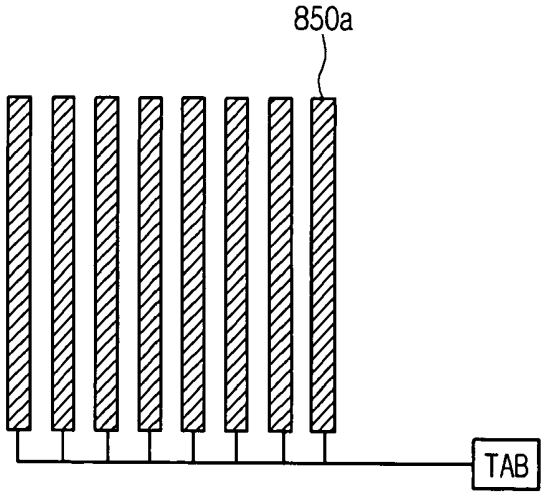

850a
TAB

Fig. 2C

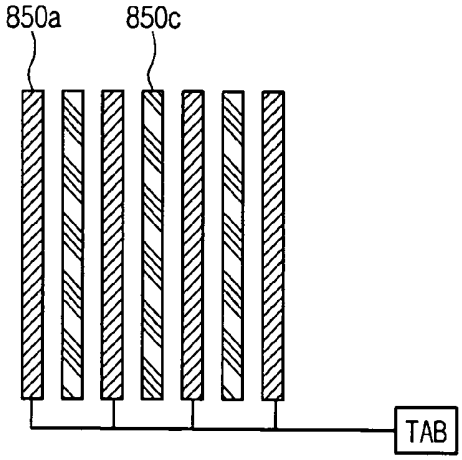


Fig. 3

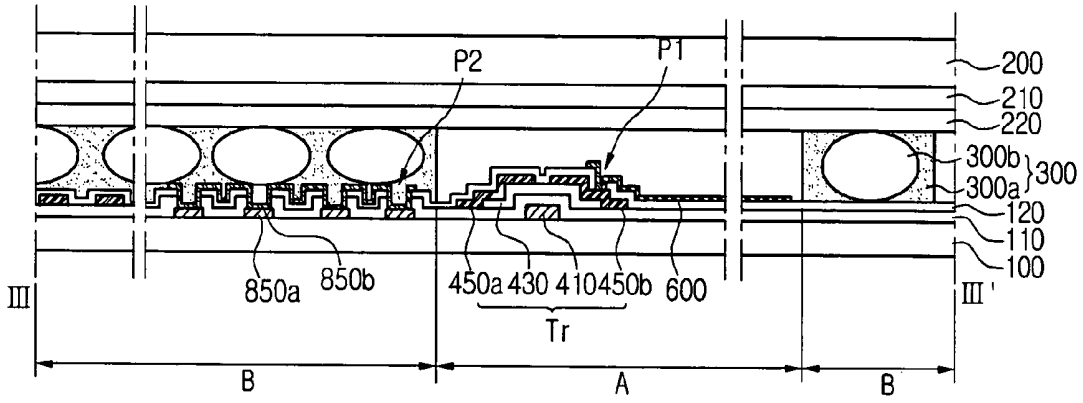


Fig. 4A

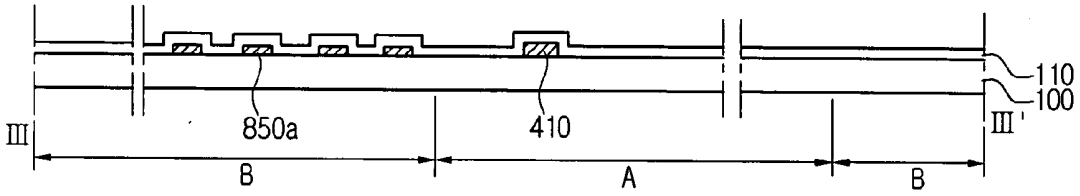


Fig. 4B

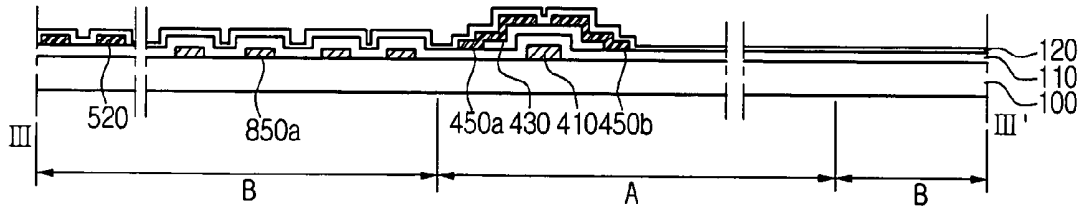


Fig. 4C

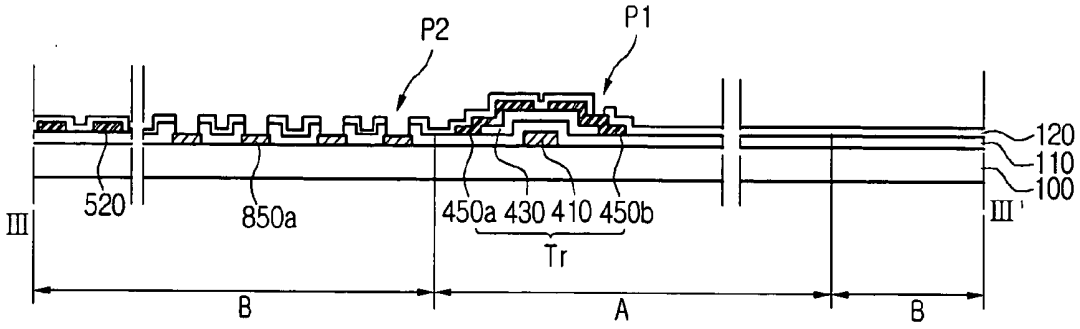


Fig. 4D

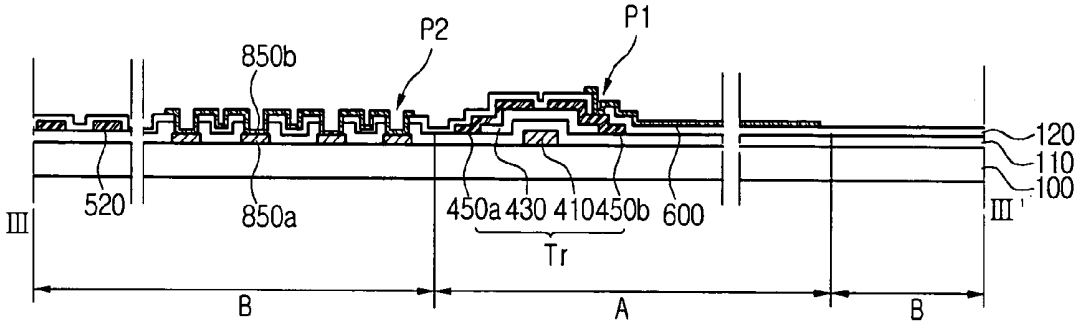


Fig. 4E

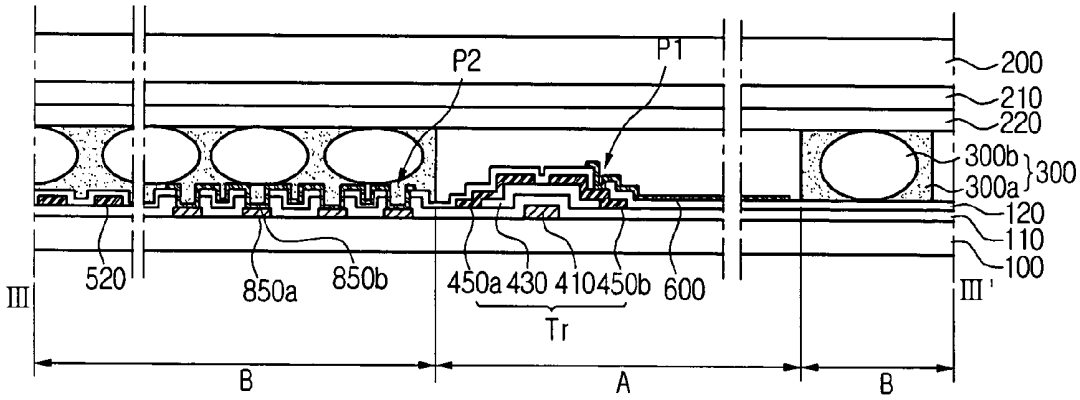


Fig. 5

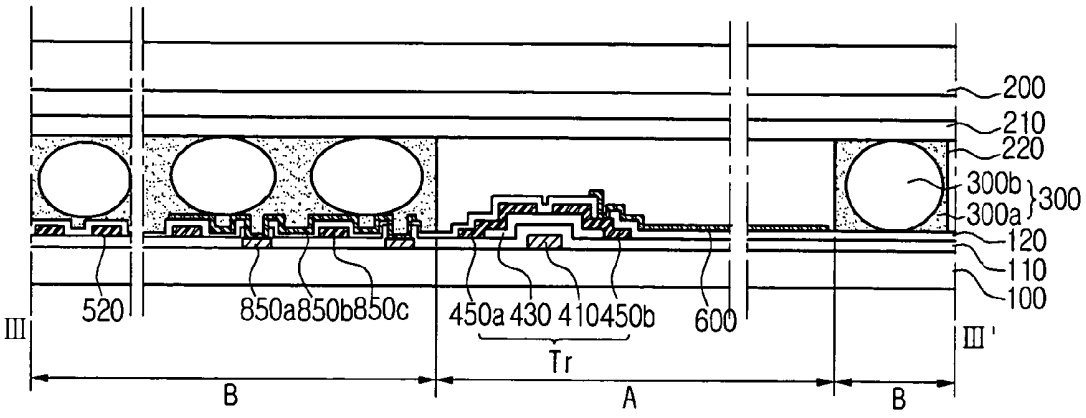


Fig. 6A

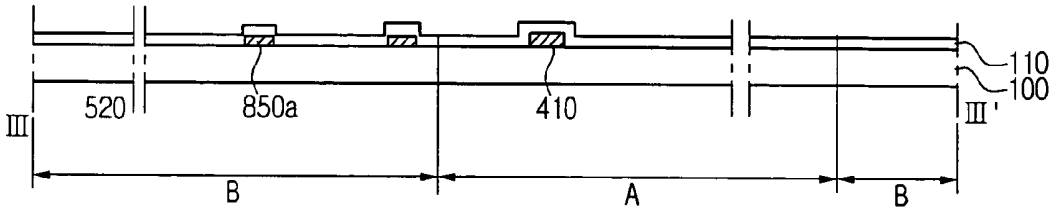


Fig. 6B

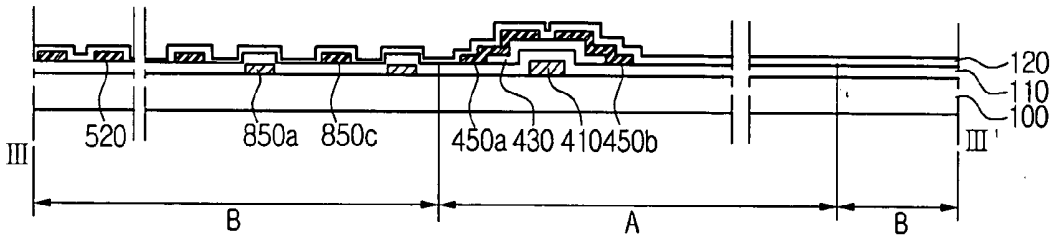


Fig. 6C

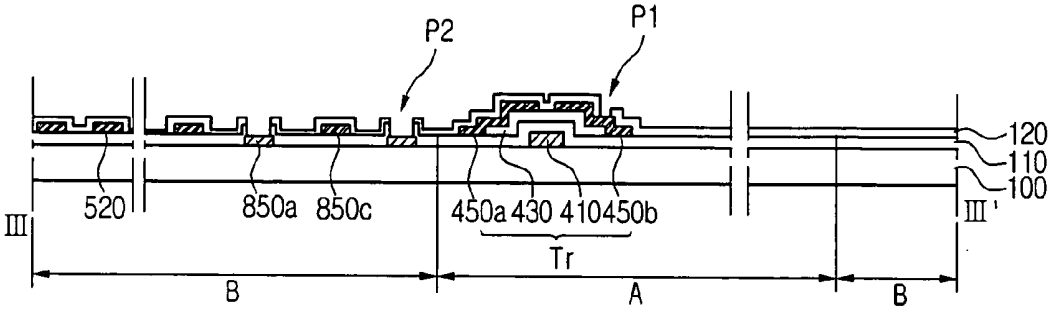


Fig. 6D

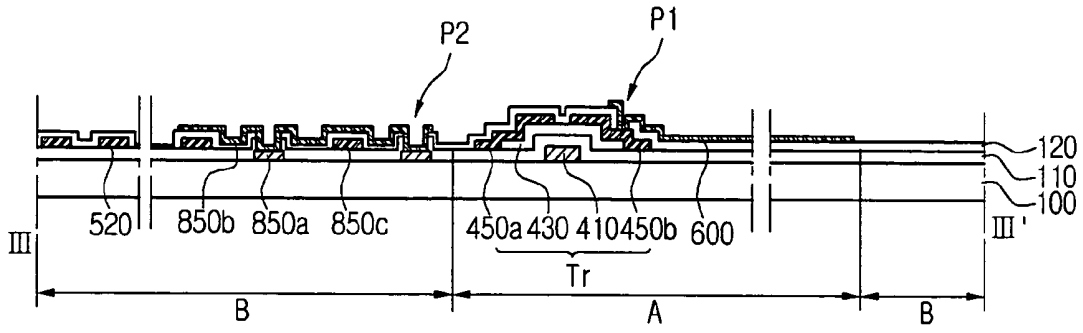
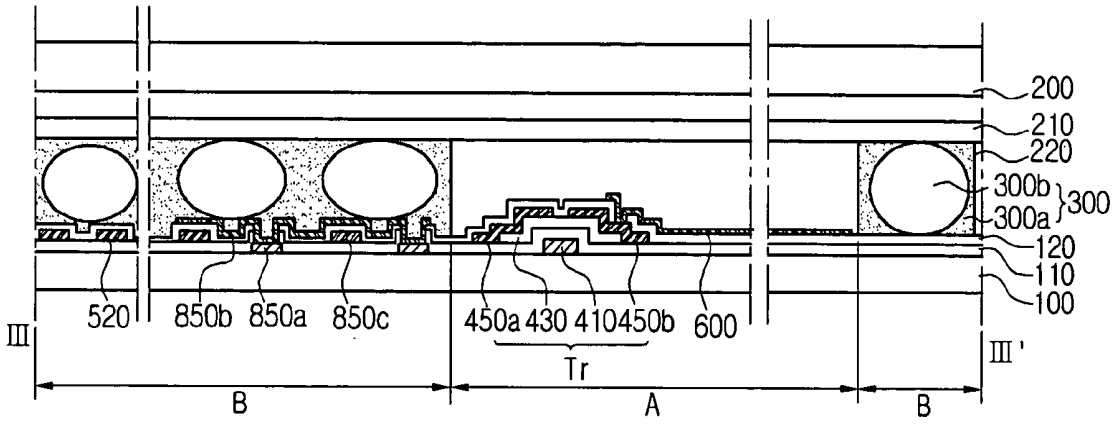

P2
P1
120
110
100
520
850b
850a
850c
450a
430
410
450b
600
III
III'
Tr
B
A
B

Fig. 6E


200
210
220
300b
300a
300
120
110
100
520
850b
850a
850c
450a
430
410
450b
600
III
III'
Tr
B
A
B

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

[0001] This application claims the benefit of Korean Patent Application No. 102071/2005 filed in Korea on Oct. 28, 2005, which is hereby incorporated by reference.

FIELD

[0002] The present invention relates to a liquid crystal display device, and more particularly, to a liquid crystal display device conducting two substrates using a conductive thread pattern, and a method of manufacturing the same.

BACKGROUND

[0003] A liquid crystal display device (LCD) is one example of flat display devices. The LCD displays data through physical optics characteristics. Since the LCD has a lower power consumption compared to other display devices, takes advantages of lightweight and thin properties, and can be manufactured in various sizes, it has been widely used in diverse fields.

[0004] The LCD includes a thin film transistor (TFT) array substrate, a color filter array substrate, and a liquid crystal. The color filter array substrate is disposed opposite to the TFT array substrate. The liquid crystal is interposed between the TFT array substrate and the color filter array substrate. The TFT array substrate includes a plurality of signal lines, and a pixel electrode connected to the TFT transistor. Additionally, the color filter array substrate includes a color filter layer for color displaying, and common electrodes.

[0005] The common electrode disposed on the color filter array substrate is electrically connected to a conductive part, which is disposed on the outside of the TFT array substrate. A common voltage supplied from an external circuit through the conductive part is supplied to the common electrode.

[0006] The common electrode is electrically connected to the conductive part through a silver dot medium. The silver dot is manufactured by coating silver in a paste state through a dispenser, drying the resulted silver dot during a predetermined time, and attaching the two substrates by pressure. At this point, in case the two substrates are attached when a silver paste coated on the TFT is not dried completely, the silver of a low density is formed. Therefore, the area contacting the common electrode is reduced and also an appropriate voltage can not be supplied.

[0007] To overcome this problem, there is provided an LCD having the conductive part formed through a conductive ball of a high density without the silver paste.

[0008] FIGS. **1**A and **1**B are views of an LCD using a related art conductive thread pattern. FIG. **1**A is a plan view when a second substrate of I-I' portion is removed from the LCD. FIG. **1**B is a sectional view taken along line II-II' of FIG. **1**A.

[0009] Referring to FIGS. **1**A and **1**B, the related art LCD includes a first substrate **10** and a second substrate **20**, which are defined by a display region A and a non-display region B. The first substrate **10** and the second substrate **20** are attached by a conductive thread pattern. A plurality of gate lines **40** and data lines **50** are crossing each other on the first substrate **10** corresponding to the display region A. Each crossing of the gate lines **40** and the data lines **50** includes at least one TFT, and a pixel electrode **60** electrically connected to the TFT.

[0010] A pad part is formed on the first substrate **100** corresponding to the non-display region B to connect to an external circuit. That is, at least two gate pad parts **70** are formed on one side of the first substrate **10**. The gate pad part **70** includes a predetermined region to which the end of each gate line **40** is gathered. Moreover, at least two data pad parts **80** are formed on another side of the first substrate **10**. The data pad part **60** includes a predetermined region to which the end of each data line is gathered. At this point, each of the pad parts is electrically connected to a printed circuit board (PCB) (not shown) through a tape automated bonding (TAB) **90**.

[0011] On the other hand, a conductive part **85** is disposed between the data pad parts **80**, and the conductive thread pattern **30** is disposed on the outside of the first substrate having the conductive part **85**. The conductive pattern **30** includes sealant **30***a* and a conductive ball **30***b*. The conductive thread pattern **30** attaches the first substrate **10** to the second substrate **20**. Additionally, the conductive thread pattern **30** connects the common electrode **22** in the second substrate **20**, and the conductive part **85**.

[0012] Thus, a common voltage is supplied from an external circuit to the conductive part **85**. The common voltage applied to the conductive part **85** is supplied to the common electrode **22** through the conductive thread pattern **30**.

[0013] The conductive part **85** includes a dummy pattern **85***a* and a dummy pattern contact part **85***b*. The dummy pattern **85***a* is simultaneously formed when source/drain electrodes **45***a* and **45***b* of the TFT, and the data line **50** are formed. The dummy pattern contact part **58***b* is simultaneously formed on the dummy pattern **85***a* when the pixel electrode is formed.

[0014] Since the dummy pattern **85***a* is simultaneously formed with the data line **50** and the source/drain electrodes **45***a* and **45***b*, there is no choice for selecting a conductive material of the dummy pattern **85***a*. That is, the dummy pattern **85***a* may be formed of a low resistance metal to minimize the loss of a common voltage supplied to the common electrode **22**. However, when considering simplicity of processes, the dummy pattern **85***a* is formed of a conductive metal of the data line **50** and the source/drain electrodes **45***a* and **45***b*.

[0015] Additionally, when the dummy pattern **85***a*, the data line **50**, and data pad **80** are formed on an identical layer, there is limitation in designing the dummy pattern **85***a*.

SUMMARY

[0016] An liquid crystal display (LCD) device includes first and second substrates defined by a display region and a non-display region, and spaced a predetermined interval apart from each other. The LCD further comprises a liquid crystal layer interposed between the first and second substrates, and a conductive part formed on at least one side of the first substrate corresponding to the non-display region. The conductive part has a first dummy pattern formed of metal identical to that of a gate line in the display region. The LCD then compsries a common electrode formed on the

second substrate, and a conductive thread pattern that electrically connects the common electrode and the conductive part, and attaches the first and second substrates.

[0017] In another aspect of the present invention, an LCD includes a first substrate defined by a display region and a non-display region, a gate electrode disposed on the first substrate corresponding to the display region, and a dummy pattern disposed on the first substrate corresponding to the non-display region and formed on a layer identical to that of the gate electrode. The LCD further comprises a gate insulating layer formed on a surface of the first substrate that has the gate electrode and the first dummy pattern, source and drain electrodes formed spaced apart from each other on both sides of an active layer on the gate insulating layer corresponding to the gate electrode, and a pixel electrode electrically connected to the drain electrode.

[0018] In a further aspect of the present invention, an LCD includes a first substrate defined by a display region and a non-display region, a gate electrode disposed on the first substrate corresponding to the display region, and a dummy pattern disposed on the first substrate corresponding to the non-display region. The LCD further comprises a gate insulating layer formed on a surface of the first substrate that has the gate electrode and the first dummy pattern, source and drain electrodes formed spaced apart from each other on both sides of an active layer on the gate insulating layer corresponding to the gate electrode, a second dummy pattern disposed on the gate insulating layer corresponding to the non-display region, and a pixel electrode electrically connected to the drain electrode.

[0019] In still another aspect of the present invention, a method of manufacturing an LCD includes depositing a first conductive material on a first substrate, forming a gate electrode and a first dummy pattern through a patterning process on the first substrate, forming a gate insulating layer on a surface of the first substrate that includes the gate electrode and the first dummy pattern, and forming an active layer, and source and drain electrodes on the gate insulating layer. The method of manufacturing an LCD further comprises forming a protective layer on the surface of the first substrate that includes the active layer and the source and drain electrodes, forming first and second contact holes in the protective layer to expose the drain electrode and the first dummy pattern, and forming a pixel electrode connected to the drain electrode through the first contact hole.

[0020] In yet another aspect of the present invention, a method of manufacturing an LCD includes depositing a first conductive material on a first substrate, forming a gate electrode and a first dummy pattern through a patterning process on the first substrate, forming a gate insulating layer in a surface of the first substrate that includes the gate electrode and the first dummy pattern, and forming an active layer, source and drain electrodes, and a second dummy pattern on the gate insulating layer. The method of manufacturing an LCD further comprises forming a protective layer on the surface of the first substrate that includes the active layer, the source and drain electrodes, and the second dummy pattern, forming first and second contact holes in the protective layer to expose the drain electrode and the first dummy pattern, and forming a pixel electrode connected to the drain electrode through the first contact hole.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0022] FIGS. **1**A and **1**B are views of an LCD using a related art conductive thread pattern;

[0023] FIGS. **2**A-**2**C are views of an LCD according to an embodiment of the present invention;

[0024] FIG. **3** is a sectional view taken along line III-III' of FIG. **2**A;

[0025] FIGS. **4**A to **4**E are views taken along line III-III' of FIG. **2**A to illustrate a method of manufacturing an LCD according to an embodiment of the present invention;

[0026] FIG. **5** is another sectional view taken along line III-III of FIG. **2**A; and

[0027] FIGS. **6**A to **6**E are views taken along line III-III' of FIG. **2**A to illustrate another method of manufacturing an LCD according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0028] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0029] FIGS. **2**A to **2**C are views of an LCD according to an embodiment of the present invention. FIG. **2**A is a plan view when I-I' portion of a second substrate is removed from the LCD. FIGS. **2**B and **2**C are views of a conductive part **850** of FIG. **2**A.

[0030] Referring to FIG. **2**A, the LCD is defined by a display region A and a non-display region B. The LCD includes first and second substrates **100** and **200** with a predetermined cell gap therebetween, and a liquid crystal layer (not shown) interposed between the first and second substrates **100** and **200**.

[0031] A plurality of gate lines **400** and data lines **500** are crossed to define a plurality of unit pixels in the first substrate **100** corresponding to the display region A. Each of the unit pixels includes at least one thin film transistor (TFT), and a pixel electrode driven by the TFT. In one side of the first substrate **100** corresponding to the non-display region B, a gate pad part **700** is disposed on the ends of the gate lines **400** for connecting an external circuit part. In another side of the first substrate **100**, a data pad part **800** is disposed on the ends of the data lines **500** for connecting the external circuit part. Here, each pad part is connected to the external circuit part through a tape automated bonding (TAB) **900** using a tape carrier package (TCP) with a driving IC. Additionally, the second substrate **200** includes a color filter layer for displaying colors in a region corresponding to each unit pixel, and a common electrode on the color filter layer.

[0032] The first and second substrates **100** and **200** are attached to each other through a conductive thread pattern

300 in the outside of the first and second substrates **100** and **200**. The conductive thread pattern **300** attaches the first substrate **100** to the second substrates **200**, and also electrically connects the first substrate **100** and a predetermined portion of the second substrate **200**. The first substrate **100** includes a conductive part **850** disposed on a predetermined portion corresponding to the non-display region B. The conductive thread pattern **300** is formed on the conductive part **850**. Thus, the conductive part **850** receives a common voltage applied from the outside, and supplies the common voltage to the common electrode of the second substrate **200** through the conductive thread pattern **300**.

[**0033**] Referring to FIG. **2**B, the conductive part **850** includes the data pad part **800** and a first dummy pattern **850***a* on and between the data pad parts **800**. The first dummy pattern **850***a* may be formed of metal identical to that of the gate line **400** of FIG. **2**A. Here, since the gate line **400** and gate electrode are generally formed of metal of a low resistance, the first dummy pattern **850***a* can be formed of metal of a low resistance. For example, the first dummy pattern **850***a* can be formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

[**0034**] Furthermore, referring to FIG. **2**C, the conductive part **850** further includes the second dummy pattern **850***c*, which is alternately disposed with the first dummy pattern **850***a*. The second dummy pattern **850***c* is not directly connected to the conductive thread pattern **300** and serves to compensate an irregular cell gap generated from a step height between the dummy pattern **850***a* and the data pad part. Additionally, the second dummy pattern **850***c* may be formed of metal identical to that of the data line. Thus, a picture quality deterioration, which is generated by an irregular cell gap, can be reduced.

[**0035**] Referring to FIG. **2**A, the conductive thread pattern **300** includes sealant and a conductive ball. The conductive ball can be formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn. The conductive ball in the conductive thread pattern **300** serves to electrically connect the conductive part and the common electrode.

[**0036**] Therefore, when the conductive part **850** is formed of a low resistance metal identical to that of the gate line **400** and the gate electrode, a common voltage from the outside can be effectively supplied to the common electrode without loss.

[**0037**] The LCD of the present invention and a method of manufacturing the same will be described in more detail with reference to sectional views taken along line III-III' of FIG. **2**A.

[**0038**] FIG. **3** is a sectional view taken along line III-III' of FIG. **2**A.

[**0039**] Referring to FIG. **3**, a first substrate **100** is defined by a display region A and a non-display region B.

[**0040**] A plurality of gate lines **400** of FIG. **2**A and gate electrodes **410** are disposed on the first substrate **100** corresponding to the display region A. An extension line **520** of the gate line is disposed on the first substrate **100** corresponding to the non-display region B. A dummy pattern **850***a* is disposed on a gate pad electrode (not shown) at the end of the gate line, and on another side having the gate pad electrode.

[**0041**] The first dummy pattern **850***a* may be formed of metal of a low resistance. For example, the first dummy pattern **850***a* can be formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

[**0042**] Since the gate electrode **410** is generally formed of a low resistance metal, the first dummy pattern **850***a* can be formed of a conductive material identical to that of the gate electrode **410**. Thus, an additional process is unnecessary to form the first dummy pattern **850***a*.

[**0043**] A gate insulating layer **110** is disposed on the first substrate **100** having the gate electrode **410** and the first dummy pattern **850***a*.

[**0044**] An active layer **430** is formed on the gate insulating layer **110** corresponding to the gate electrode **410**, and source/drain electrodes **450***a* and **450***b* are spaced apart from each other on both sides of the active layer **430**. Additionally, an extension line **520** of the data line is disposed on the gate insulating layer **110** corresponding to the non-display region B. A data pad electrode (not shown) is disposed at the end of the extension line **520** of the data line.

[**0045**] A protective layer **120** is disposed on the gate insulating layer **110** having the source/drain electrodes **450***a* and **450***b*. The protective layer **120** includes a first contact hole P**1** exposing a portion of the drain electrode **450***b*, and a second contact hole P**2** exposing a portion of the first dummy pattern **850***a*.

[**0046**] A pixel electrode **600** is electrically connected to the drain electrode **450***b* through the fist contact hole P**1**, and a first dummy pattern contact part **850***b* is electrically connected to the first dummy pattern **850***a* through the second contact hole P**2**.

[**0047**] The pixel electrode **600** can be formed of a conductive material identical to that of the fist dummy pattern contact part **850***b*. Furthermore, the first dummy pattern contact part **850***b* can be formed of indium-tin oxide (ITO) or indium-zinc oxide (IZO). Here, the first dummy pattern contact part **850***b* can serve to prevent a corrosion of the first dummy pattern **850***a*.

[**0048**] A first alignment layer (not shown) for an initial alignment of liquid crystal is disposed on the protective layer **120** of the display region A having the pixel electrode **600**.

[**0049**] On the other hand, a second substrate **200** is spaced a predetermined interval apart from the first substrate **100**. The second substrate **200** includes a color filter layer **210** in a region corresponding to each unit pixel of the first substrate **100**, and a common electrode **220** on the first substrate **100** having the color filter layer **210**. The common electrode **220** may be formed of a transparent conductive material such as ITO and IZO.

[**0050**] Additionally, a conductive thread pattern **300** is disposed on the outside of the first substrate **100** and the second substrate **200**. The conductive thread pattern **300** is disposed on the first dummy pattern **850***a* of the first substrate **100**. The first dummy pattern **850***a* is electrically connected to the common electrode **220** through the conductive thread pattern **300**. The conductive thread pattern **300** can include sealant **300***a* and a conductive ball **300***b*. The conductive ball **300***b* can be formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and

Pb—Sn. Thus, the first dummy pattern **850***a* is electrically connected to the common electrode **220** through the conductive ball **300***b* in the conductive thread pattern **300**.

[**0051**] Furthermore, the first dummy pattern **850***a* is formed on the data pad part and between the data pad parts. Since the first dummy pattern **850***a* is formed on the data pad part or a protective layer **120** on the extension line **520** of the data line, it does not contact the data pad part or the protective layer **120**. The first dummy pattern **850***a* can be formed to be overlapped with the extension line **520** of the data line or the data pad part. Thus, when the first dummy pattern **850***a* is formed, it can be designed without considering the data pad part or the extension line **520** of the data line.

[**0052**] The protective layer **120** may be formed of an insulation layer of a low dielectric constant. This can prevent a parasite capacity generated from overlapping the first dummy pattern **850***a* with the data pad part or the extension line **520** of the data line.

[**0053**] When the first and second substrates **100** and **200** are conducted through the conductive ball **300***b*, the first dummy pattern **850***a* can be formed with a more enlarged size compared to a related art by forming the first dummy pattern **850***a* on a layer identical to that of the gate electrode **410** and the gate line. The first dummy pattern **850***a* supplies a common voltage to the second substrate **200**. Additionally, the first dummy pattern **850***a* can be formed of a low resistance metal, and thus more efficiently supplies the common voltage to the common electrode **220**.

[**0054**] FIGS. **4**A to **4**E are views taken along line III-III' of FIG. **2**A to illustrate a method of manufacturing an LCD according to an embodiment of the present invention.

[**0055**] Referring to FIG. **4**A, a first substrate **100** is defined by a display region A and a non-display region B. Here, the first substrate **100** can be formed of glass or plastic.

[**0056**] A first conductive material is deposited on the first substrate **100**. The first conductive material can be a low resistance metal. The first conductive material can be formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

[**0057**] Next, a plurality of gate lines and a gate electrode **410** protruded toward a direction different from that of the gate line are formed by patterning the first conductive material. Additionally, an extension line of the gate line, and a gate pad electrode and a first dummy pattern **850***a* disposed at the end of the extension line of the gate line are formed on a region corresponding to the non-display region B.

[**0058**] Next, a gate insulating layer **110** is formed on an entire surface of the first substrate **100** having the gate electrode **410** and the first dummy pattern **850***a*. The gate insulating layer **110** can be formed by depositing silicon nitride or silicon oxide through a chemical vapor deposition (CVD) process.

[**0059**] Referring to FIG. **4**B, an amorphous silicon and an amorphous silicon doped with impurity are sequentially deposited on the gate insulating layer **110**. Then, an active layer **430** is formed on a region corresponding to the gate electrode **410** by patterning the amorphous silicon layer and the amorphous silicon layer doped with impurity.

[**0060**] Next, a second conductive material is deposited on the gate insulating layer **110** having the active layer **430**, and then patterned. Then, source/drain electrodes **450***a* and **450***b* are formed spaced apart from each other on the both sides of the active layer **430**. Each data line is formed to be crossed with the gate line. At this point, a unit pixel is defined in the display region A through the gate line and the data line. On the other hand, an extension line **520** of the data line, and a data pad electrode at the end of the extension line **520** of the data line are formed on the gate insulating layer **110** corresponding to the non-display region B.

[**0061**] The active layer **430** and the source/drain electrodes **450***a* and **450***b* are formed using another mask process, but the present invention is not limited to this. Thus, the active layer **430** and the source/drain electrodes **450***a* and **450***b* can be formed using an identical mask process. An amorphous silicon layer and an amorphous silicon layer doped with impurity can be disposed on the bottom of the data line and the data pad electrode.

[**0062**] Next, a protective layer **120** is formed on the gate insulating layer **110** having the source/drain electrodes **450***a* and **450***b*. The protective layer **120** can be formed of silicon oxide or silicon nitride using a CVD process. The protective layer **120** may be formed of benzo-cyclo-butene (BCB) of a low dielectric constant. This allows the protective layer **120** to be interposed between the first dummy pattern **850***a* and the extension line **520** of the data line or the data pad part. When the first dummy pattern **850***a* is designed with a more enlarged size, the first dummy pattern **850***a* can be formed to be overlapped with the extension line **520** of the data line or the data pad part. However, since a parasite capacity can be generated in a region where the first dummy pattern **850***a* is overlapped with the extension line **520** of the data line or the data pad part, the protective layer **120** may be formed of an insulation layer of a low dielectric constant.

[**0063**] Referring to FIG. **4**C, a first contact hole P**1** is formed on the protective layer **120** to expose a portion of the drain electrode **450***b*. At this point, a second contact hole P**2** may be simultaneously formed to expose a portion of the first dummy pattern **850***a*. The second contact hole P**2** can be formed by etching the protective layer **120** and the gate insulating layer **100** collectively.

[**0064**] Referring to FIG. **4**D, a transparent conductive material is deposited on the protective layer **120**, and then patterned. Thus, a pixel electrode **600** connected electrically to the drain electrode **450***b* is formed through the first contact hole P**1**. The transparent conductive material can be ITO or IZO. On the other hand, the first dummy pattern contact part **850***b* is simultaneously formed, which is electrically connected to the first dummy pattern **850***a* exposed through the second contact hole P**2**. Since the outside of the first dummy pattern **850***a* can be prevented from corroding, reliability of the LCD can be achieved. A first alignment layer (not shown) can be further formed on the pixel electrode **600**.

[**0065**] Referring to FIG. **4**E, a conductive thread pattern **300** having sealant **300***a* and a conductive ball **300***b* is formed on the first substrate **100** having the first dummy pattern **850***a*. The conductive ball can be formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn. Additionally, the conductive thread pattern **300** can be formed on a second substrate.

[0066] Next, the second substrate **200** is disposed on the first substrate **100**. The first and second substrates **100** and **200** are coupled by pressure. Here, the second substrate **200** includes a color filter layer **210** and a common electrode **220** on a region corresponding to a unit pixel of the first substrate **100**. Additionally, an alignment layer (not shown) can be further formed on the common electrode **220**.

[0067] The first and second substrates **100** and **200** are coupled together through the conductive thread pattern **300**. The first dummy pattern **850***a* of the first substrate **100** is electrically connected to the common electrode **220** of the second substrate **200**.

[0068] Therefore, a common voltage supplied to the first dummy pattern **300** is supplied to the common electrode **220** through the conductive ball **300***b* of the conductive thread pattern **300**.

[0069] FIG. **5** is another sectional view taken along line III-III' of FIG. **2**A.

[0070] Here, except for adding a second dummy pattern **850***c*, like reference numerals in the drawings denote like elements.

[0071] Referring to FIG. **5**, a first substrate **100** is defined by a display region A and a non-display region B. A plurality of gate lines and gate electrodes **410** are disposed on the first substrate **100** corresponding to the display region A. An extension line **520** of the gate line is disposed on the first substrate **100** corresponding to the non-display region B. A dummy pattern **850***a* is disposed on a gate pad electrode (not shown) at the end of the gate line, and on another side having the gate pad electrode. The first dummy pattern **850***a* may be formed of metal of a low resistance. For example, the first dummy pattern **850***a* can be formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

[0072] Since the gate electrode **410** is formed of a low resistance metal, the first dummy pattern **850***a* can be formed of a conductive material identical to that of the gate electrode **410**. Thus, an additional process is unnecessary to form the first dummy pattern **850***a*.

[0073] A gate insulating layer **110** is disposed on the first substrate **100** having the gate electrode **410** and the first dummy pattern **850***a*.

[0074] An active layer **430** is formed on the gate insulating layer **110** corresponding to the gate electrode **410**, and source/drain electrodes **450***a* and **450***b* are spaced apart from each other on both sides of the active layer **430**. Additionally, a second dummy pattern **850***c* is disposed on the gate insulating layer **110** corresponding to the non-display region B.

[0075] The second dummy pattern **850***c* and the first dummy pattern **850***a* are disposed alternately. Since a step height between the first dummy pattern **850***a* and the extension line of the data line or the data pad part can be overcome, a picture quality deterioration, which is generated by an irregular cell gap, can be reduced.

[0076] A protective layer **120** is disposed on the gate insulating layer **110** having the source/drain electrodes **450***a* and **450***b*. The protective layer **120** includes a first contact hole P**1** exposing a portion of the drain electrode **450***b*, and a second contact hole P**2** exposing a portion of the first dummy pattern **850***a*.

[0077] A pixel electrode **600** is disposed and electrically connected to the drain electrode **450***b* through the fist contact hole P**1**. A first dummy pattern contact part **850***b* is disposed and electrically connected to the first dummy pattern **850***a* through the second contact hole P**2**. Here, the area where the first dummy pattern contact part **850***b* contacts a conductive thread pattern **300** increases through the second dummy pattern **850***c*. Thus, a common voltage can be easily supplied to a common electrode in the second substrate **200**. Additionally, since the area contacting the conductive thresh pattern increases, an adhesive strength between the first substrate **100** and the second substrate **200** can be improved.

[0078] The pixel electrode **600** can be formed of a conductive material identical to that of the fist dummy pattern contact part **850***b*. Furthermore, the first dummy pattern contact part **850***b* can be formed of ITO or IZO. Here, the first dummy pattern contact part **850***b* can serve to reduce a corrosion of the first dummy pattern **850***a*.

[0079] A first alignment layer (not shown) for an initial alignment of liquid crystal is disposed on the protective layer **120** of the display region A having the pixel electrode **600**.

[0080] On the other hand, a second substrate **200** is spaced a predetermined interval apart from the first substrate **100**. The second substrate **200** includes a color filter layer **210** in a region corresponding to each unit pixel of the first substrate **100**, and a common electrode **220** on the first substrate **100** having the color filter layer **210**. The common electrode **200** may be formed of a transparent conductive material such as ITO and IZO.

[0081] Additionally, a conductive thread pattern **300** is disposed on the outside of the first substrate **100** and the second substrate **200**. The conductive thread pattern **300** is disposed on the first dummy pattern **850***a* and the second dummy pattern **850***b* of the first substrate **100**. The first dummy pattern **850***a* is electrically connected to the common electrode **220** through the conductive thread pattern **300**. The conductive thread pattern **300** can include sealant **300***a* and a conductive ball **300***b*. The conductive ball **300***b* can be formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn. Thus, the first dummy pattern **850***a* is electrically connected to the common electrode **220** through the conductive ball **300***b* in the conductive thread pattern **300**. Additionally, the second dummy pattern **850***c* serves to overcome a step height between the extension line **520** of the data line or the data pad part, and also increase the area contacting the conductive thread pattern **300**. Thus, an adhesive strength and a voltage mobility can be improved.

[0082] As described above, since the first dummy pattern **850***a* is formed on the data pad part, and between the data pad parts, it is formed on the protective layer **120** on the data pad part or the extension line **520** of the data line. Thus, when the first dummy pattern **850***a* is formed, it can be designed without considering the data pad part or the extension line **520** of the data line. Additionally, when the first and second substrates **100** and **200** are conducted through the conductive ball **300***b*, the first dummy pattern **850***a* is formed on a layer identical to that of the gate electrode **410**. The first dummy pattern **850***a* is a conductive part for supplying a common voltage to the second substrate

200. Thus, the first dummy pattern **850***a* can be formed with a more enlarged size compared to a related art. Additionally, since the first dummy pattern **850***a* can be formed of a low resistance metal, a common voltage can be more efficiently supplied to the common electrode **220**.

[**0083**] FIGS. **6**A to **6**E are views taken along line III-III' of FIG. **2**A to illustrate another method of manufacturing an LCD according to an embodiment of the present invention. Except for the additional second dummy pattern **850***c*, like reference numerals in the drawings denote like elements.

[**0084**] Referring to FIG. **6**A, a first substrate **100** is defined by a display region A and a non-display region B. Here, the first substrate **100** can be formed of glass or plastic.

[**0085**] A first conductive material is deposited on the first substrate **100**. The first conductive material can be a low resistance metal. The first conductive material can be formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

[**0086**] Next, a plurality of gate lines, and a gate electrode **410** protruded toward a direction different from that of the gate line are formed by patterning the first conductive material. Additionally, an extension line of the gate line, and a gate pad electrode and a first dummy pattern **850***a* disposed on the end of the extension line of the gate line are formed on a region corresponding to the display region B.

[**0087**] Next, a gate insulating layer **110** is formed on an entire surface of the first substrate having the gate electrode **410** and the first dummy pattern **850***a*. The gate insulating layer **110** can be formed by depositing silicon nitride or silicon oxide through the CVD process.

[**0088**] Referring to FIG. **6**B, an amorphous silicon and an amorphous silicon doped with impurity are sequentially deposited on the gate insulating layer **110**. Then, an active layer **430** is formed on a region corresponding to the gate electrode **410** by patterning the amorphous silicon layer and the amorphous silicon layer doped with impurity.

[**0089**] Next, a second conductive material is deposited on the gate insulating layer **110** having the active layer **430**, and then patterned. Then, source/drain electrodes **450***a* and **450***b* are formed spaced apart from each other on the both sides of the active layer **430**. Each data line is formed to be crossed with the gate line. At this point, a plurality of unit pixels is defined in the display region A by the gate lines and the data lines. On the other hand, an extension line **520** of the data line, and a data pad electrode and the second dummy pattern **850***c* at the end of the extension line **520** of the data line are formed on the gate insulating layer **110** corresponding to the non-display region B. At this point, the second dummy pattern **850***c* and the first dummy pattern **850***a* are formed to be disposed alternately.

[**0090**] Here, the active layer **430** and the source/drain electrodes **450***a* and **450***b* are formed using another mask process, but the present invention is not limited thereto. Thus, the active layer **430** and the source/drain electrodes **450***a* and **450***b* can be formed using an identical mask process. An amorphous silicon layer and an amorphous silicon layer doped with impurity can be disposed on the bottom of the data line and the data pad electrode.

[**0091**] Next, a protective layer **120** is formed on the gate insulating layer **110** having the source/drain electrodes **450***a* and **450***b*. The protective layer **120** can be formed of silicon oxide or silicon nitride using a CVD process. The protective layer **120** may be formed of benzo-cyclo-butene (BCB) of a low dielectric constant. A parasite capacity can be generated in a region where the first dummy pattern **850***a* is overlapped with the extension line **520** of the data line or the data pad part.

[**0092**] Referring to FIG. **6**C, a first contact hole P**1** is formed on the protective layer **120** to expose a portion of the drain electrode **450***b*. At this point, a second contact hole P**2** may be simultaneously formed to expose a portion of the first dummy pattern **850***a*. The second contact hole P**2** can be formed by etching the protective layer **120** and the gate insulating layer **110** collectively.

[**0093**] Referring to FIG. **6**D, a transparent conductive material is deposited on the protective layer **120**, and then patterned. Thus, a pixel electrode **600** connected electrically to the drain electrode **450***b* is formed through the first contact hole P**1**. The transparent conductive material can be ITO or IZO. On the other hand, the first dummy pattern contact part **850***b* is simultaneously formed, which is electrically connected to the first dummy pattern **850***a* exposed through the second contact hole P**2**. Since the outside of the first dummy pattern **850***a* can be prevented from corroding, reliability of the LCD can be achieved. A first alignment layer (not shown) can be further formed on the pixel electrode **600**.

[**0094**] Referring to FIG. **6**E, a conductive thread pattern **300** having sealant **300***a* and a conductive ball **300***b* is formed on the first substrate **100** having the first dummy pattern **850***a*. The conductive ball can be formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn.

[**0095**] Next, the second substrate **200** is disposed on the first substrate **100**. The first and second substrates **100** and **200** are coupled by pressure. Here, the second substrate includes a color filter layer **210** and a common electrode **220** on a region corresponding to a unit pixel of the first substrate **100**. Additionally, a second alignment layer (not shown) can be further formed on the common electrode **220**.

[**0096**] The first and second substrates **100** and **200** are coupled together by the conductive thread pattern **300**. The first dummy pattern **850***a* of the first substrate **100** is electrically connected to the common electrode **220** of the second substrate **200**.

[**0097**] Therefore, a common voltage supplied to the first dummy pattern **300** is supplied to the common electrode **220** through the conductive ball **300***b* of the conductive thread pattern **300**.

[**0098**] According to the present invention, since the first substrate is conducted to the second substrate through the conductive thread pattern having a high-density conductive ball, the LCD with an improved conductivity can be manufactured.

[**0099**] Additionally, since the first dummy pattern, which is the conductive part of the first substrate, can be formed using a low resistance gate metal, a common voltage supplied from the external circuit part can be efficiently supplied to the common electrode of the second substrate.

[0100] Additionally, since the first dummy pattern, which is a conductive part of the first substrate, can be designed to be overlapped with the extension line of the data line or the data pad electrode, the design margin area of the first dummy pattern can be enlarged.

[0101] Moreover, since the first dummy pattern and the second dummy pattern are disposed alternately to overcome a step height between the first dummy pattern and the data pad, an irregular cell gap between the first and second substrates can be prevented.

[0102] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An LCD (liquid crystal display device), comprising:

first and second substrates defined by a display region and a non-display region, and spaced a predetermined interval apart from each other;

a liquid crystal layer interposed between the first and second substrates;

a conductive part formed on at least one side of the first substrate corresponding to the non-display region, and that has a first dummy pattern formed of a metal identical to that of a gate line in the display region;

a common electrode formed on the second substrate; and

a conductive thread pattern that electrically connects the common electrode and the conductive part, and attaches the first and second substrates.

2. The LCD according to claim 1, wherein the conductive part further comprises a second dummy pattern.

3. The LCD according to claim 2, wherein the second dummy pattern and the first dummy pattern are disposed alternately.

4. The LCD according to claim 2, wherein the second dummy pattern is formed of a metal identical to that of a data line crossed with the gate line.

5. The LCD according to claim 1, wherein the conductive part is disposed between pad parts for connecting to an external circuit part.

6. The LCD according to claim 5, wherein the pad parts are data pad parts.

7. The LCD according to claim 1, wherein the conductive thread pattern includes a sealant and a conductive ball.

8. The LCD according to claim 7, wherein the conductive ball is formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn.

9. An LCD comprising:

a first substrate defined by a display region and a non-display region;

a gate electrode disposed on the first substrate corresponding to the display region;

a first dummy pattern disposed on the first substrate corresponding to the non-display region and formed on a layer identical to that of the gate electrode;

a gate insulating layer formed on a surface of the first substrate that includs the gate electrode and the first dummy pattern;

source and drain electrodes formed spaced apart from each other on both sides of an active layer on the gate insulating layer corresponding to the gate electrode; and

a pixel electrode electrically connected to the drain electrode.

10. The LCD according to claim 9, further comprising a conductive thread pattern formed on an outside region of the first substrate with the first dummy pattern.

11. The LCD according to claim 10, further comprising a second substrate that has a common electrode electrically connected to the first dummy pattern through the conductive thread pattern.

12. The LCD according to claim 10, wherein the conductive thresh pattern comprises a sealant and a conductive ball.

13. The LCD according to claim 12, wherein the conductive ball is formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn.

14. The LCD according to claim 9, further comprising:

a protective layer formed on the gate insulating layer that includes the source and drain electrodes;

first and second contact holes formed in the protective layer to expose the drain electrode and the first dummy pattern; and

a first dummy pattern contact part electrically connected to the first dummy pattern through the second contact hole.

15. The LCD according to claim 14, wherein the first dummy pattern contact part is formed of a conductive material identical to that of the pixel electrode.

16. The LCD according to claim 14, wherein the first dummy pattern contact part is formed of one of ITO (indium-tin oxide) or IZO (indium-zinc oxide).

17. The LCD according to claim 9, wherein the first dummy pattern is formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

18. The LCD according to claim 9, wherein the first dummy pattern is formed of metal identical to that of the gate electrode.

19. An LCD comprising:

a first substrate defined by a display region and a non-display region;

a gate electrode disposed on the first substrate corresponding to the display region;

a first dummy pattern disposed on the first substrate corresponding to the non-display region;

a gate insulating layer formed on a surface of the first substrate that includes the gate electrode and the first dummy pattern;

source and drain electrodes formed spaced apart from each other on both sides of an active layer on the gate insulating layer corresponding to the gate electrode;

a second dummy pattern disposed on the gate insulating layer corresponding to the non-display region; and

a pixel electrode electrically connected to the drain electrode.

20. The LCD according to claim 19, further comprising a conductive thread pattern formed on an outside region of the first substrate with the first dummy pattern.

21. The LCD according to claim 20, further comprising a second substrate that has a common electrode connected to the first dummy pattern through the conductive thread pattern.

22. The LCD according to claim 20, wherein the conductive pattern comprises a sealant and a conductive ball.

23. The LCD according to claim 22, wherein the conductive ball is formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn.

24. The LCD according to claim 19, further comprising:

a protective layer formed on the gate insulating layer that has the source and drain electrodes;

first and second contact holes formed in the protective layer to expose the drain electrode and the first dummy pattern; and

a first dummy pattern contact part electrically connected to the first dummy pattern through the second contact hole.

25. The LCD according to claim 24, wherein the first dummy pattern contact part is formed of a conductive material identical to that of the pixel electrode.

26. The LCD according to claim 24, wherein the first dummy pattern contact part is formed of ITO or IZO.

27. The LCD according to claim 19, wherein the first dummy pattern is formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

28. The LCD according to claim 19, wherein the first dummy pattern is formed of a metal identical to that of the gate electrode.

29. The LCD according to claim 19, wherein the second dummy pattern and the first dummy pattern are disposed alternately.

30. The LCD according to claim 19, wherein the second dummy pattern is formed of a metal identical to that of the source and drain electrodes.

31. A method of manufacturing an LCD, comprising:

depositing a first conductive material on a first substrate;

forming a gate electrode and a first dummy pattern through a patterning process on the first substrate;

forming a gate insulating layer on a surface of the first substrate that includes the gate electrode and the first dummy pattern;

forming an active layer, and source and drain electrodes on the gate insulating layer;

forming a protective layer on the surface of the first substrate that includes the active layer and the source and drain electrodes;

forming first and second contact holes in the protective layer to expose the drain electrode and the first dummy pattern; and

forming a pixel electrode connected to the drain electrode through the first contact hole.

32. The method according to claim 31, further comprising forming a first dummy pattern contact part electrically connected to the first dummy pattern through the second contact hole during the forming of the pixel electrode.

33. The method according to claim 31, further comprising:

forming a conductive thread pattern on an outside of the first substrate that has the first dummy pattern; and

attaching the first substrate and a second substrate, wherein the second substrate is spaced a predetermined interval apart from the first substrate, and have a common electrode.

34. The method according to claim 33, wherein the conductive thread pattern comprises a sealant and a conductive ball.

35. The method according to claim 34, wherein the conductive ball is formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn.

36. The method according to claim 32, wherein the first dummy pattern contact part is formed of a conductive material identical to that of the pixel electrode.

37. The method according to claim 32, wherein the first dummy pattern contact part is formed of one of ITO (indium-tin oxide) or IZO (indium-zinc oxide).

38. The method according to claim 31, wherein the first dummy pattern is formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

39. The method according to claim 31, wherein the first dummy pattern is formed of metal identical to that of the gate electrode.

40. A method of manufacturing an LCD, comprising:

depositing a first conductive material on a first substrate;

forming a gate electrode and a first dummy pattern through a patterning process on the first substrate;

forming a gate insulating layer in a surface of the first substrate that includes the gate electrode and the first dummy pattern;

forming an active layer, source and drain electrodes, and a second dummy pattern on the gate insulating layer;

forming a protective layer on the surface of the first substrate that includes the active layer, the source and drain electrodes, and the second dummy pattern;

forming first and second contact holes in the protective layer to expose the drain electrode and the first dummy pattern; and

forming a pixel electrode connected to the drain electrode through the first contact hole.

41. The method according to claim 40, further comprising forming a first dummy pattern contact part electrically connected to the first pattern through the second contact hole during the forming of the pixel electrode.

42. The method according to claim 40, further comprising:

forming a conductive thread pattern on an outside of the first substrate having the first dummy pattern; and

attaching the first substrate and a second substrate, wherein the second substrate is spaced a predetermined interval apart from the first substrate, and has a common electrode.

43. The method according to claim 42, wherein the conductive thread pattern comprises a sealant and a conductive ball.

44. The method according to claim 43, wherein the conductive ball is formed of at least one selected from the group comprising of Ag, Au, Pb—Ag, and Pb—Sn.

45. The method according to claim 41, wherein the first dummy pattern contact part is formed of a conductive material identical to that of the pixel electrode.

46. The method according to claim 41, wherein the first dummy pattern contact part is formed of ITO or IZO.

47. The method according to claim 40, wherein the first dummy pattern is formed of at least one selected from the group comprising of Ta, Al, Ti, Ni, and AlNd.

48. The method according to claim 40, wherein the first dummy pattern is formed of a metal identical to that of the gate electrode.

49. The method according to claim 40, wherein the first dummy pattern and the second dummy pattern are disposed alternately.

50. The method according to claim 40, further comprising connecting a second substrate that has a common electrode to the first dummy pattern through the conductive thread pattern.

51. The method according to claim 40, wherein the second dummy pattern is formed of a metal identical to that of the source and drain electrodes.

* * * * *

专利名称(译)	液晶显示装置及其制造方法		
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申请(专利权)人(译)	LG飞利浦LCD CO.，LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO.，LTD.		
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摘要(译)

提供一种LCD及其制造方法。 LCD包括由显示区域和非显示区域限定的第一和第二基板，并且彼此隔开预定间隔。 LCD还包括插入在第一和第二基板之间的液晶层，形成在第一基板的与非显示区域对应的至少一侧上的导电部分。导电部分具有由与显示区域中的栅极线相同的金属形成的第一虚设图案。然后，LCD包括形成在第二基板上的公共电极，以及电连接公共电极和导电部分，并附着第一和第二基板的导电线图案。