US 20030058396A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2003/0058396 A1

(43) Pub. Date: Mar. 27, 2003

Shih

(54) MANUFACTURING METHOD FOR IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY (LCD) UNIT

(75) Inventor: **Po-Sheng Shih**, Taoyuan Shien (TW)

Correspondence Address:
Haverstock & Owens L.L.P.
Suite 420
260 Sheridan Avenue
Polo Alto, CA 94306 (US)

(73) Assignee: **Hannstar Display Corp.**

(21) Appl. No.: **10/157,453**

(22) Filed: **May 28, 2002**

(30) **Foreign Application Priority Data**

Sep. 25, 2001 (TW) 090123652

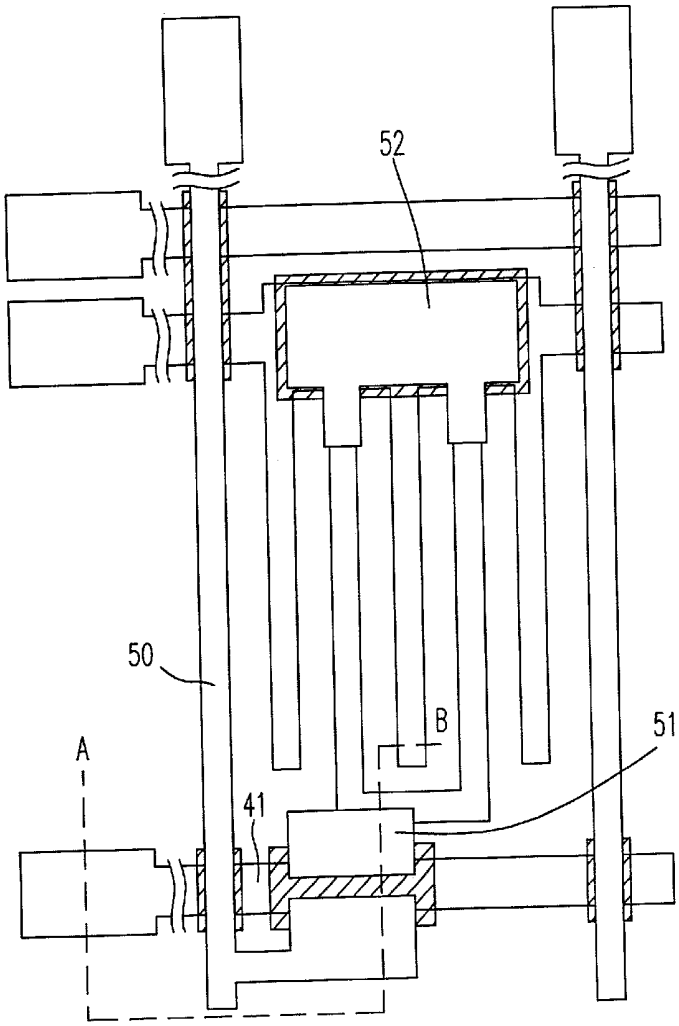
Publication Classification

(51) **Int. Cl.**[7] **G02F 1/1343**

(52) **U.S. Cl.** **349/141**; 349/43

(57) **ABSTRACT**

A manufacturing method for an in-plane switching mode liquid crystal display (LCD) unit is provided. The method includes steps of: providing a substrate, forming a first conductive layer on the substrate, patterning the first conductive layer to form a gate line, a comb-shaped first electrode, a wiring pad, and a comb-shaped second electrode by a first photo etching process, forming a first insulation layer and a first semi-conductive layer, patterning the first insulation layer and the first semi-conductive layer to form a channel, an insulation structure, a dielectric layer, and plural crossed-conductive line insulation structures by a second photo etching process, forming a second semi-conductive layer and a second conductive layer on the substrate, patterning the second semi-conductive layer and the second conductive layer to form a source/drain electrode, a data line, a connecting electrode, and a first electrode by a third photo etching process, and forming a passivation layer.



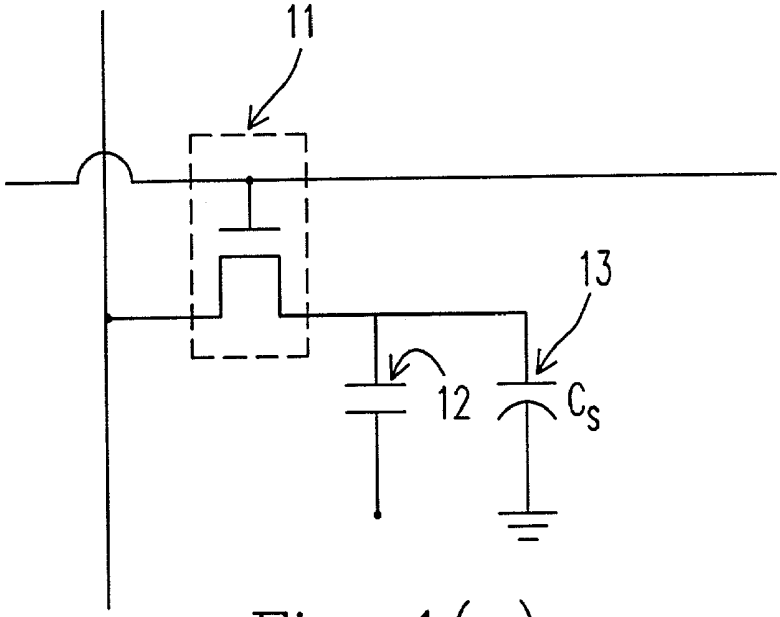


Fig. 1(a)
PRIOR ART

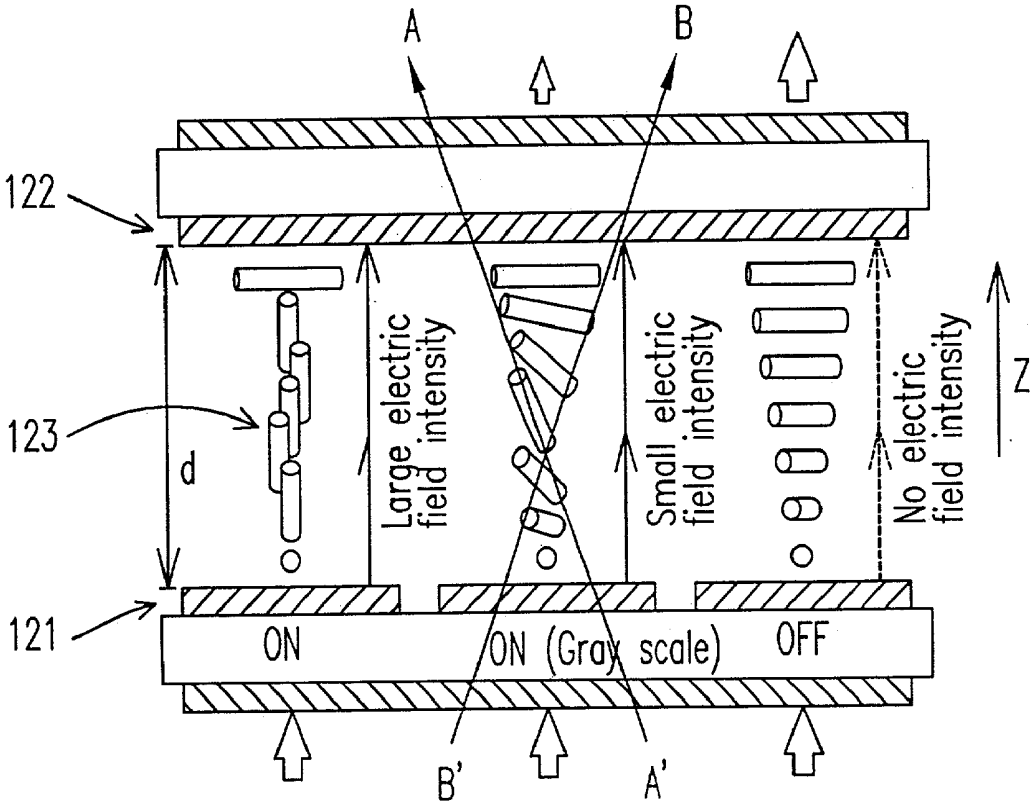


Fig. 1(b)
PRIOR ART

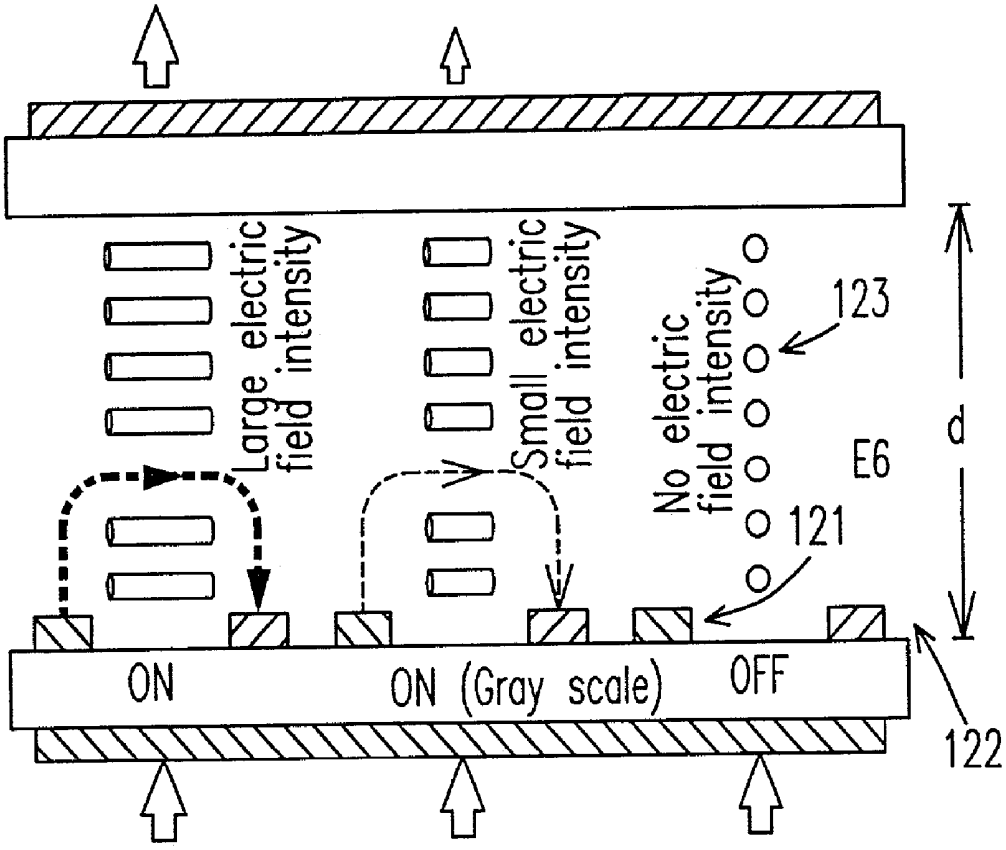


Fig. 1(c)
PRIOR ART

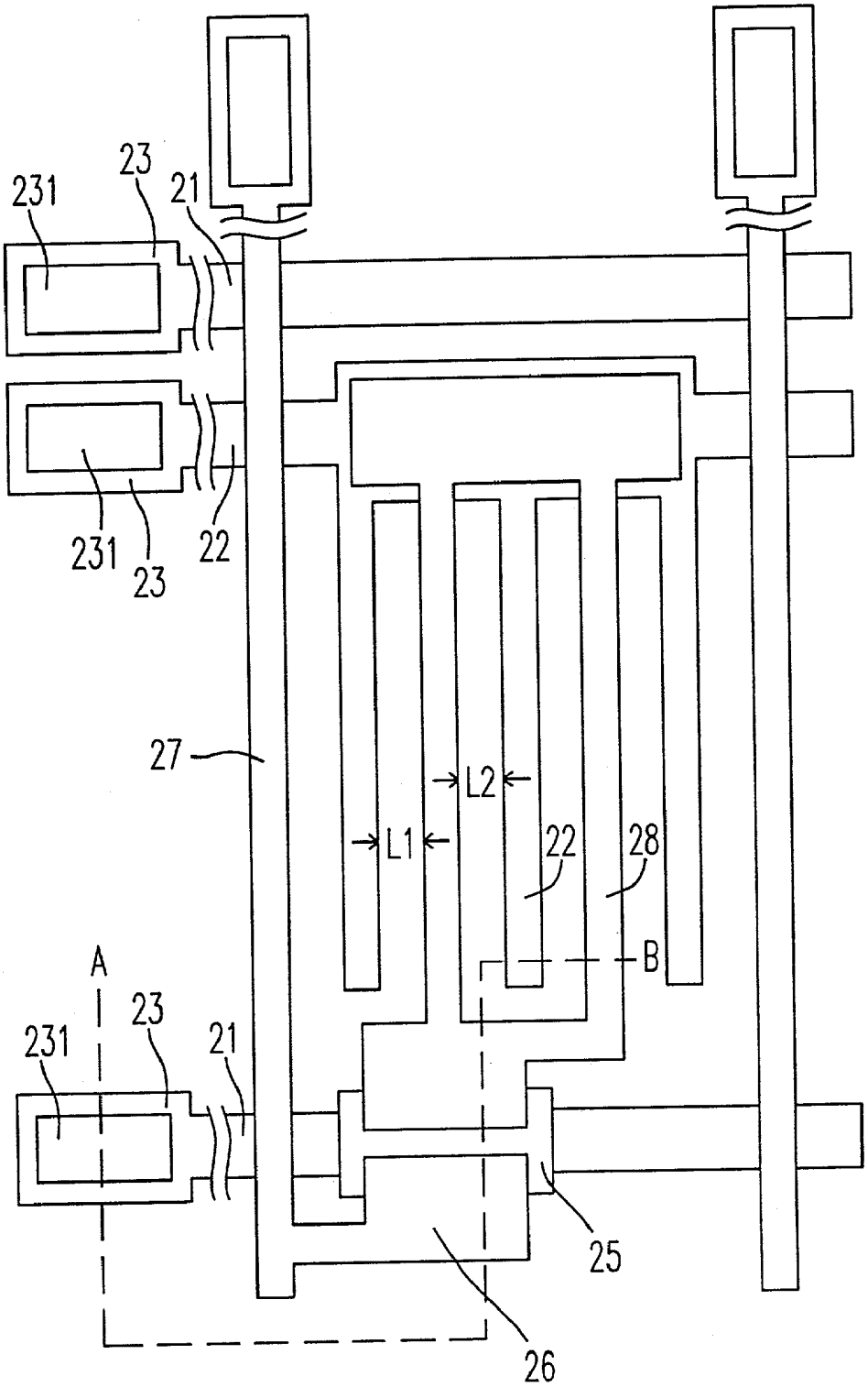


Fig. 2(a)
PRIOR ART

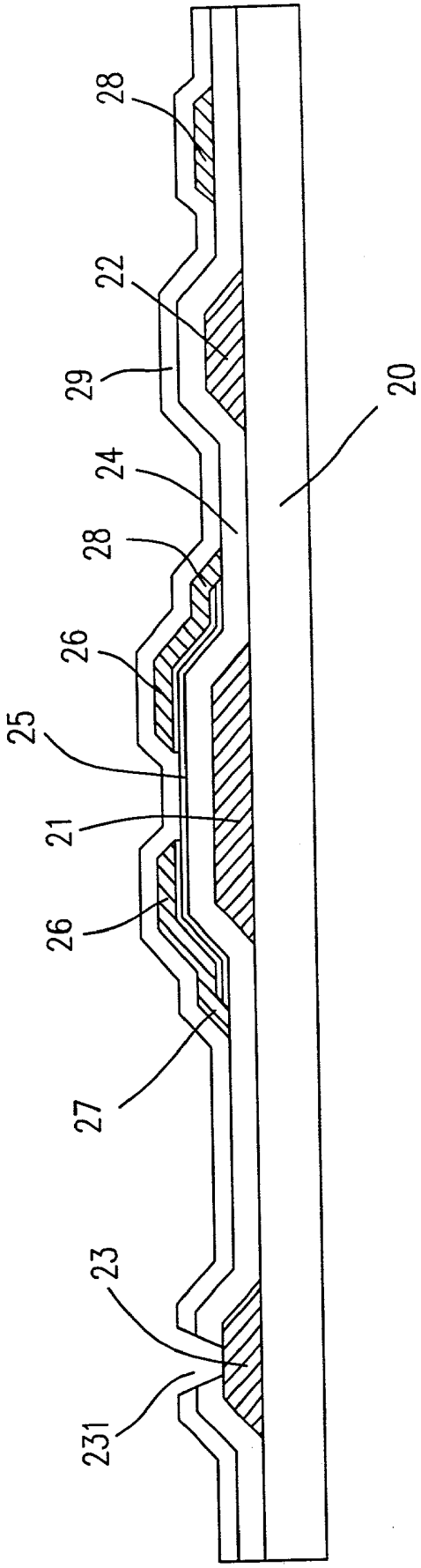


Fig. 2(b)
PRIOR ART

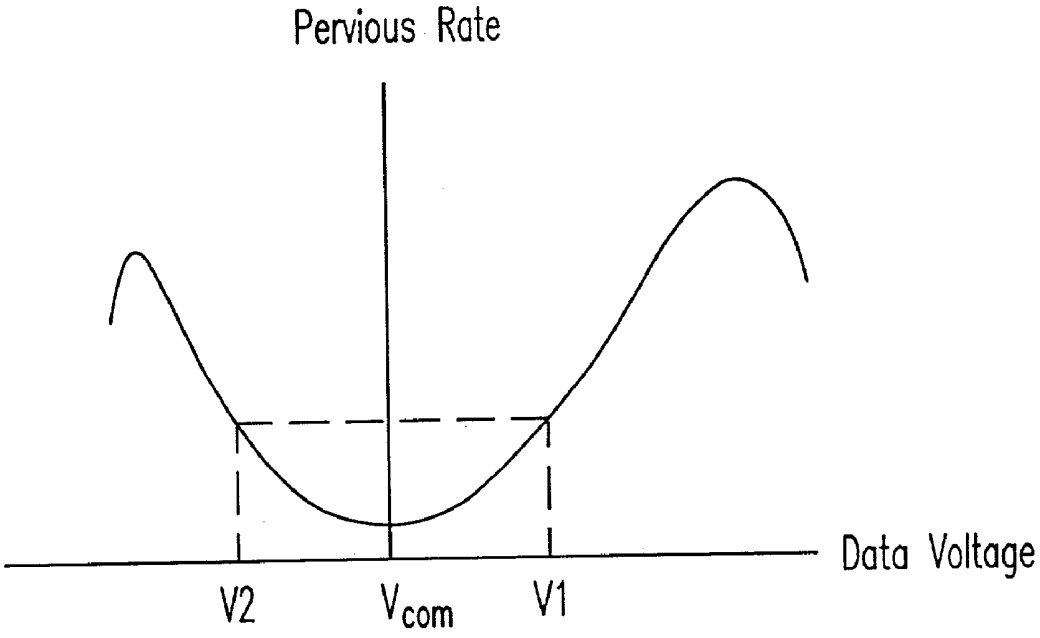


Fig. 2(c)
PRIOR ART

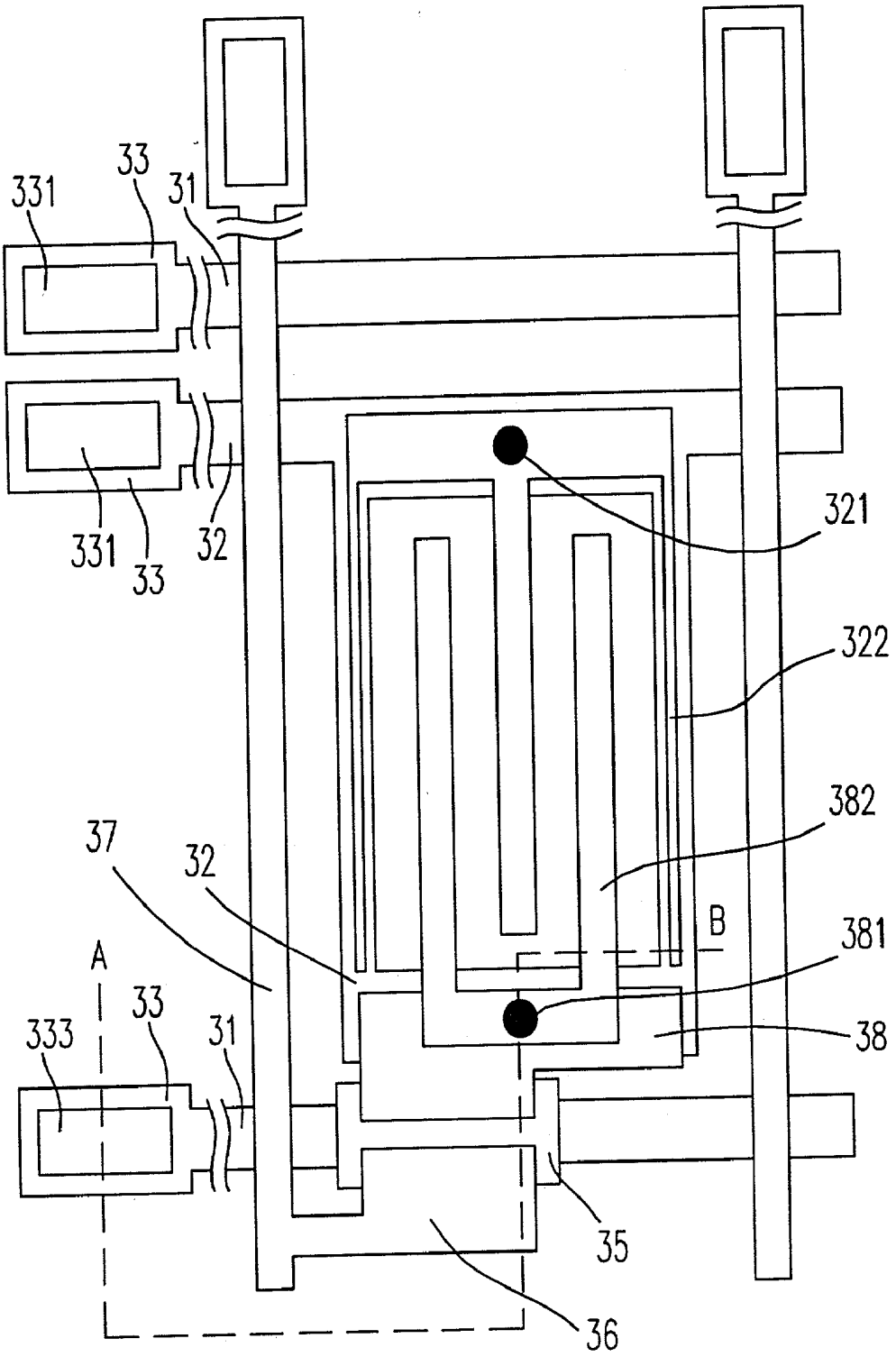


Fig. 3(a)
PRIOR ART

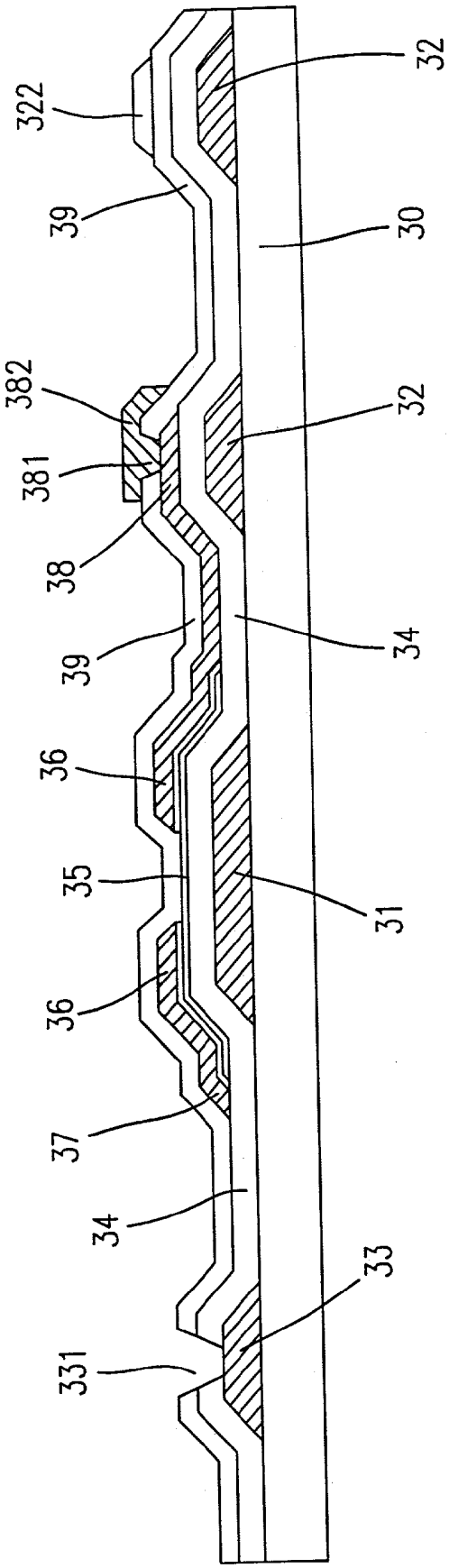


Fig. 3(b)
PRIOR ART

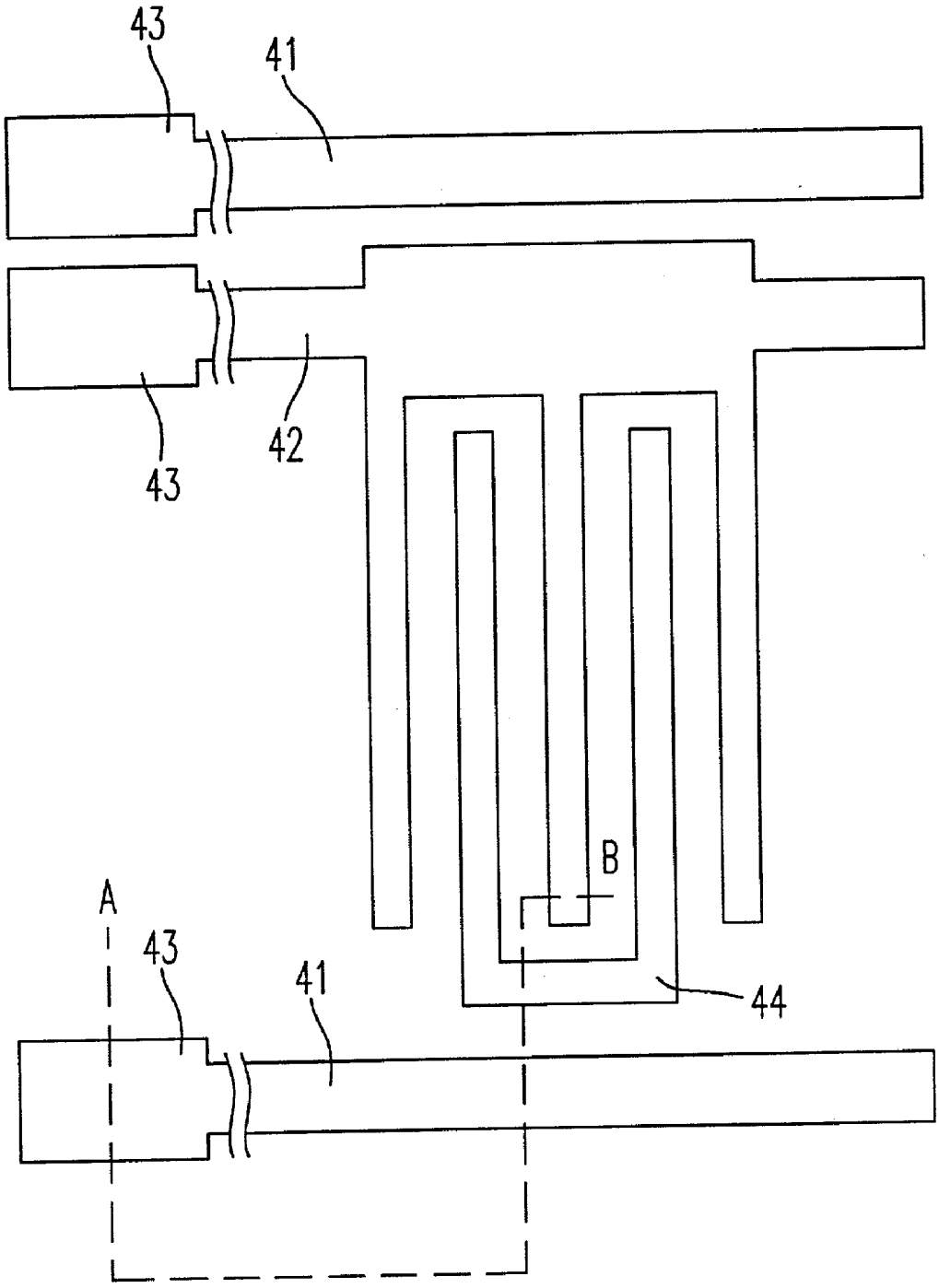


Fig. 4(a)

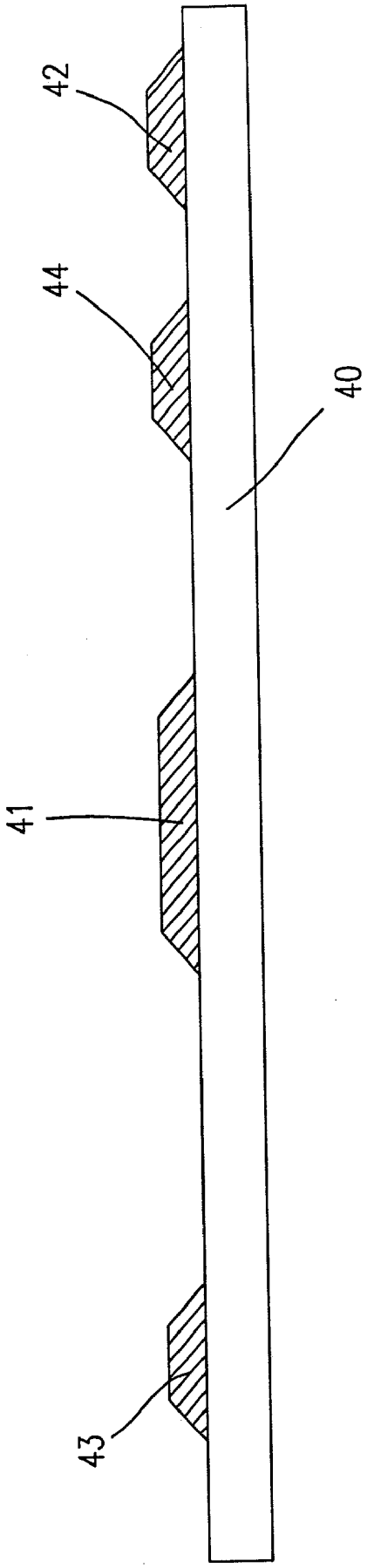


Fig. 4(b)

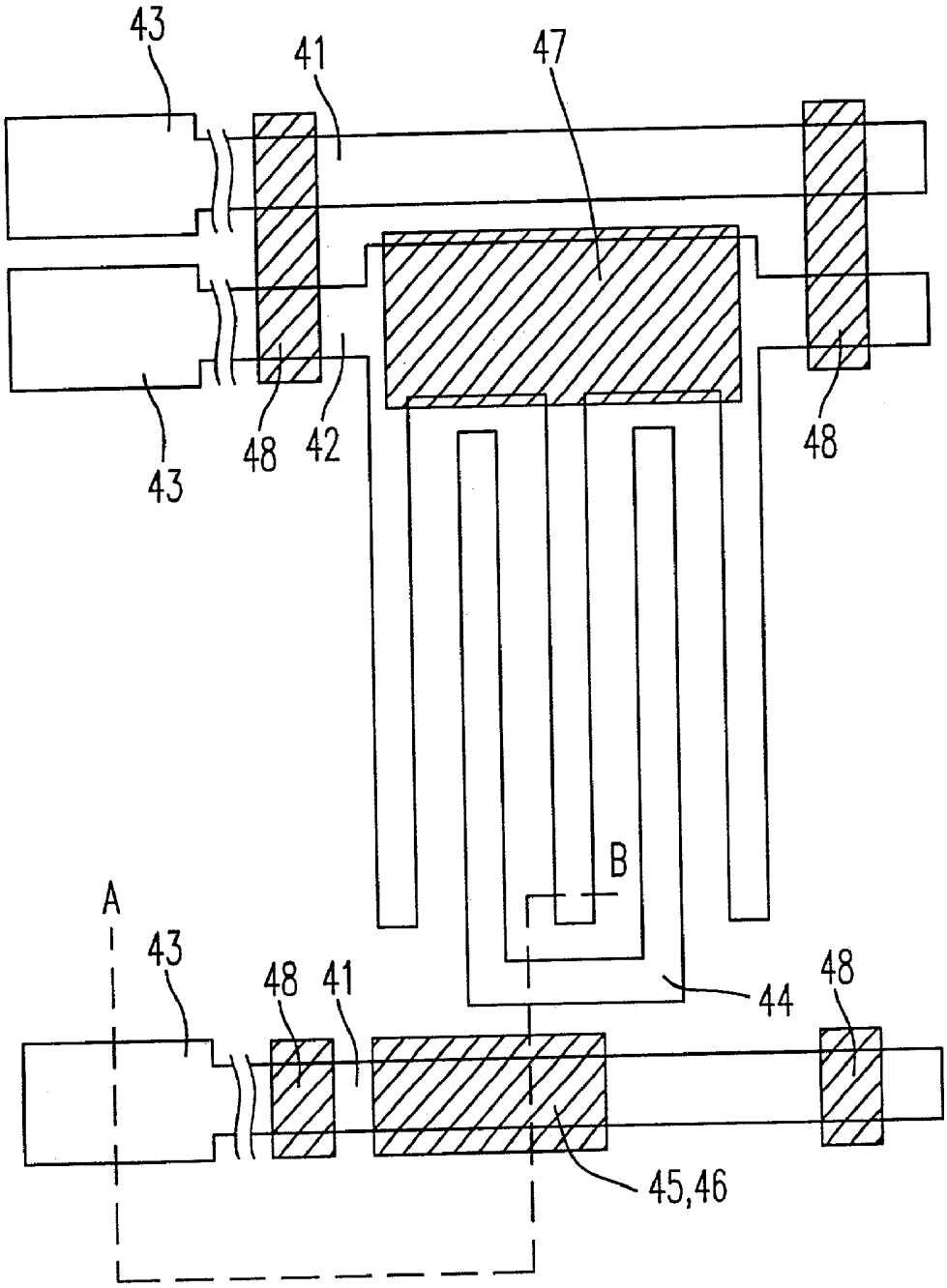


Fig. 4(c)

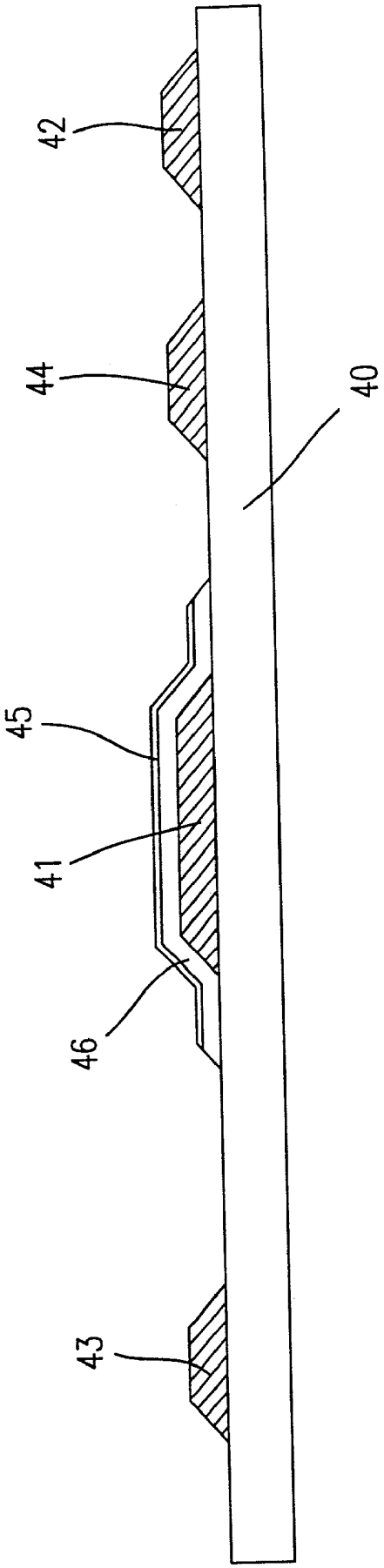


Fig. 4(d)

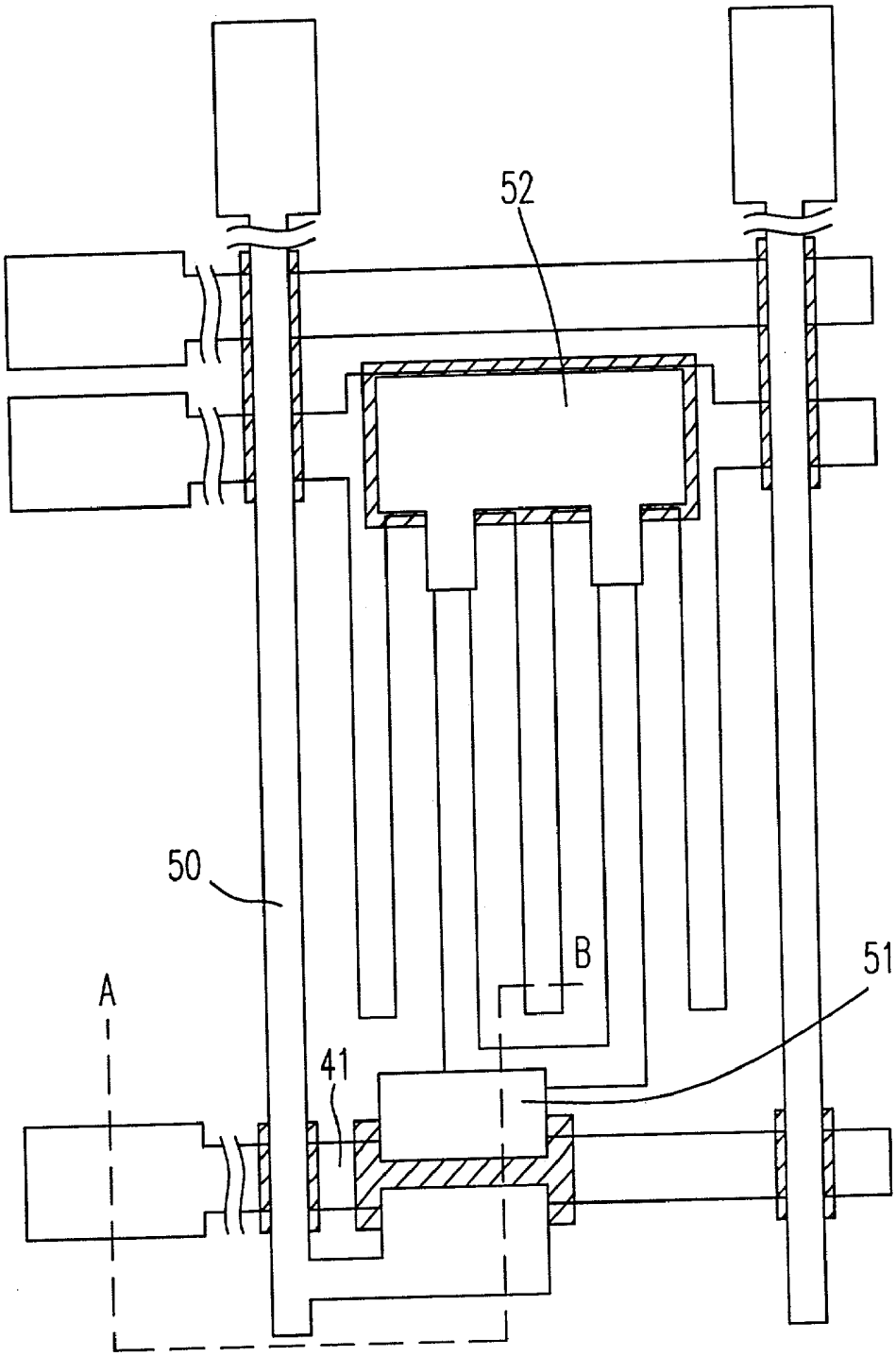


Fig. 4(e)

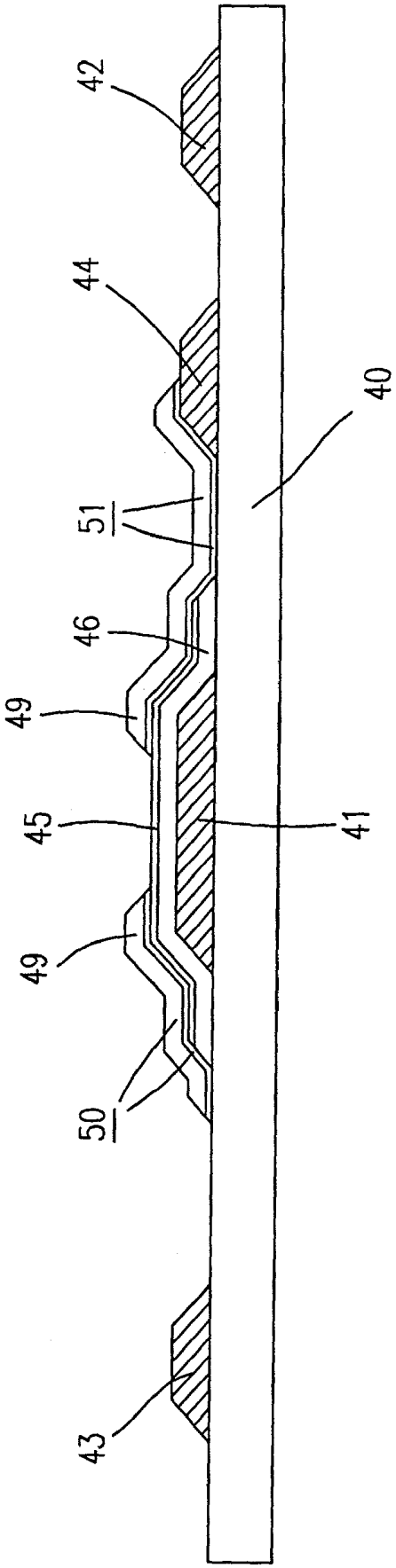


Fig. 4(f)

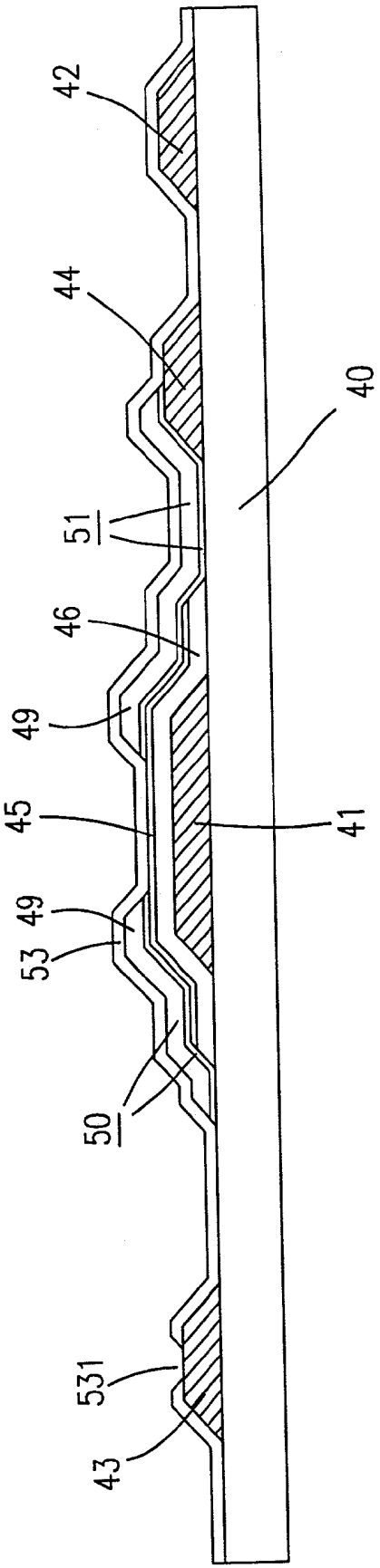


Fig. 4(g)

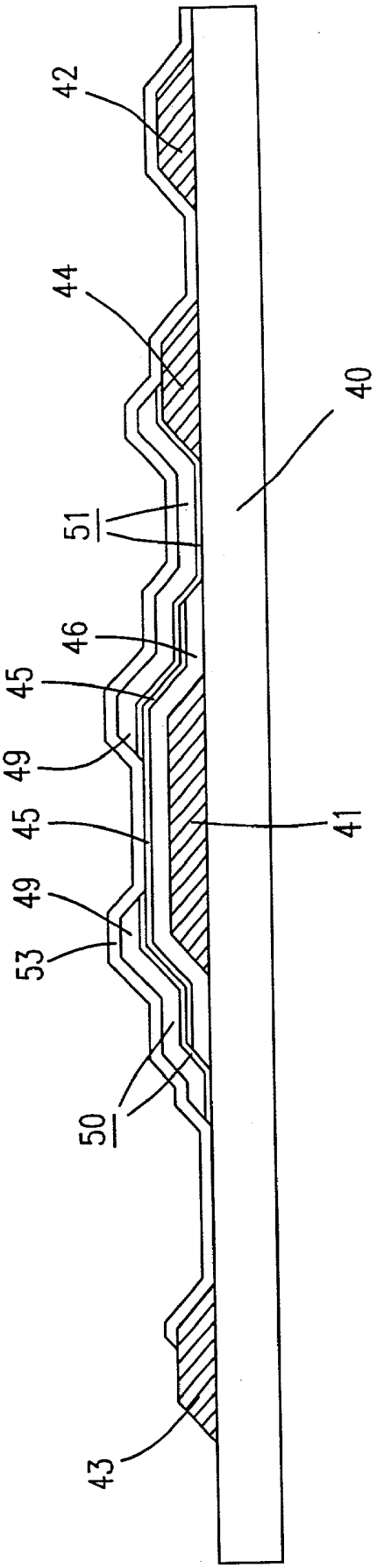


Fig. 4(h)

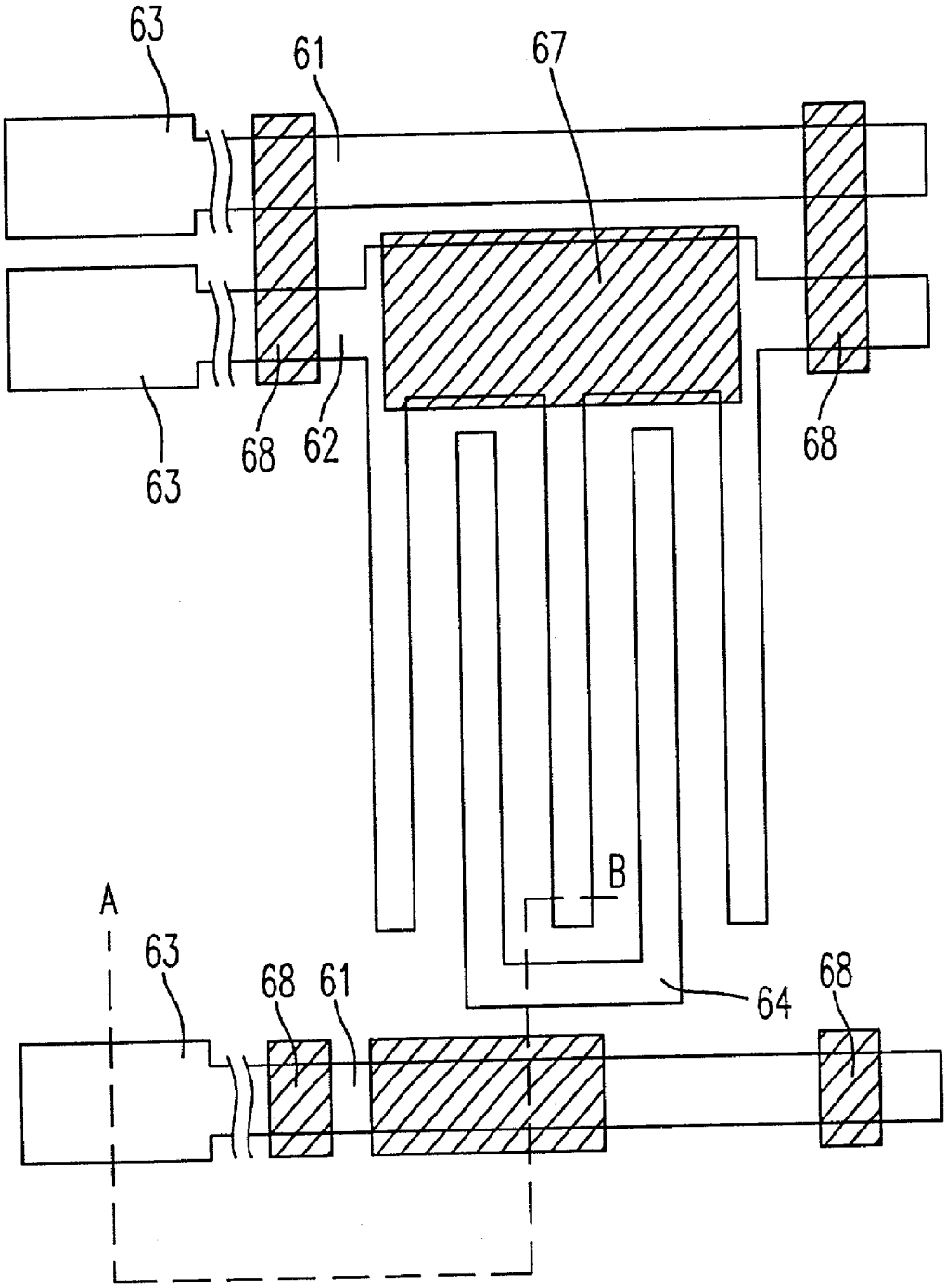


Fig. 5(a)

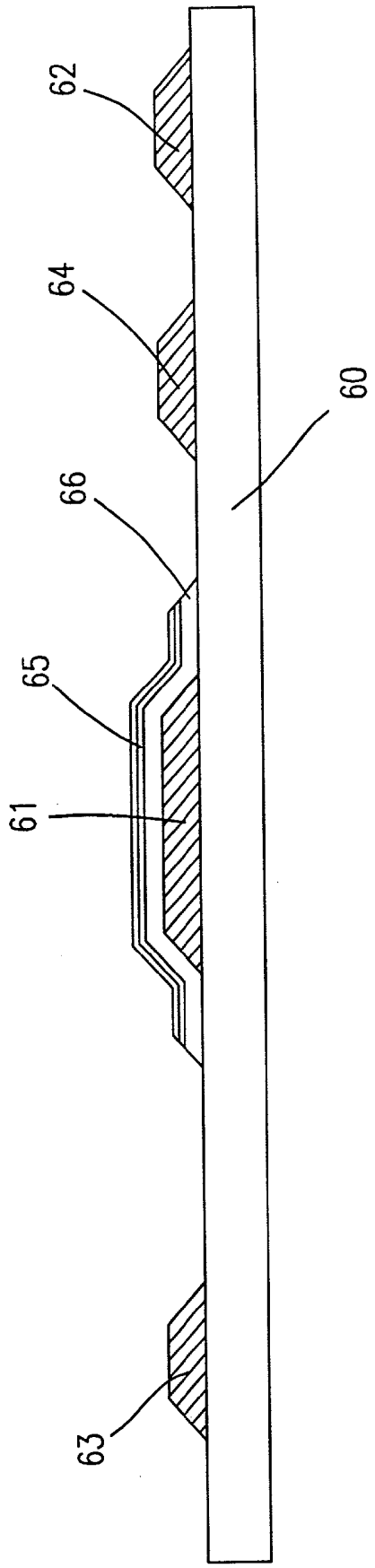


Fig. 5(b)

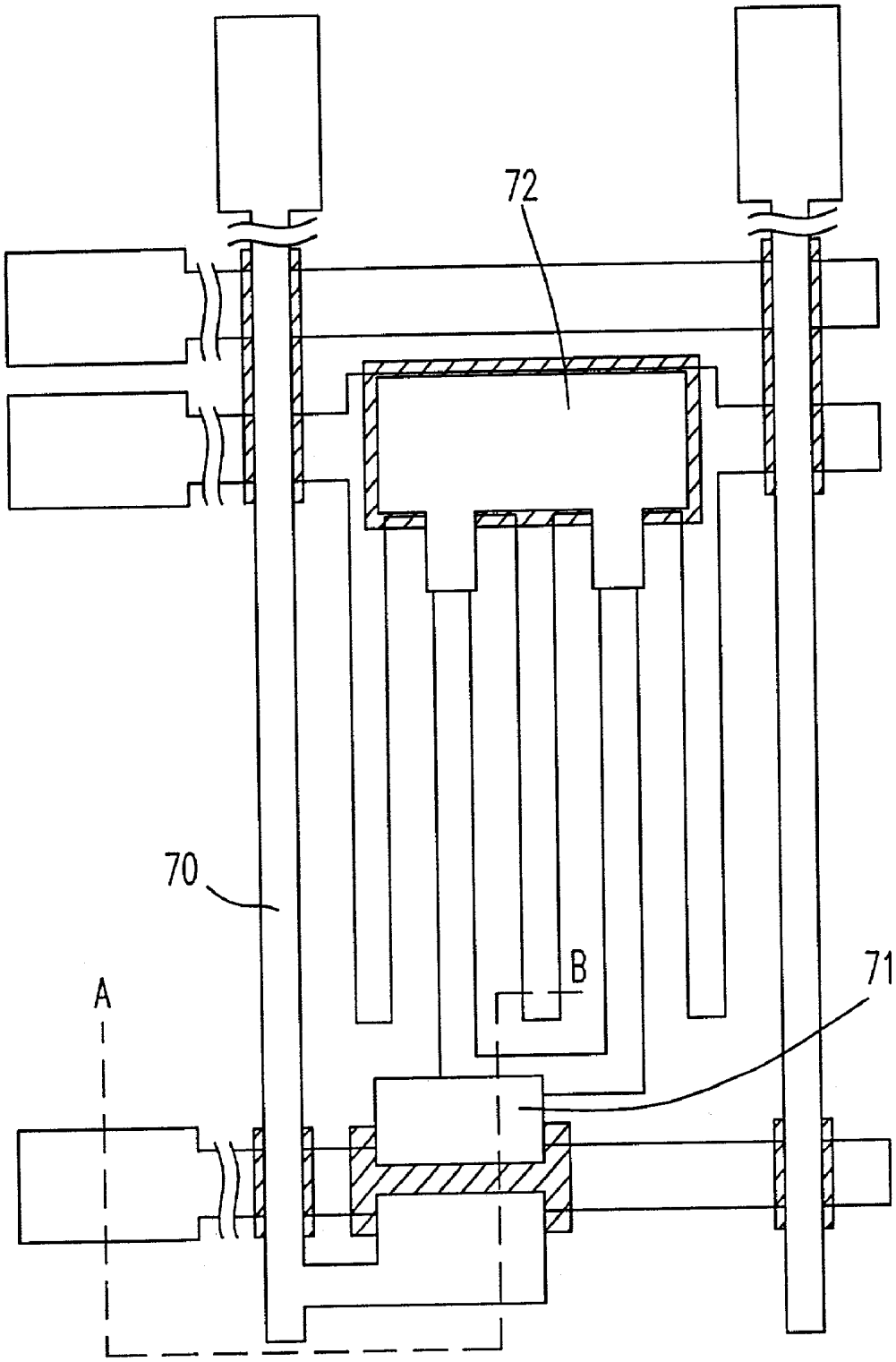


Fig. 5(c)

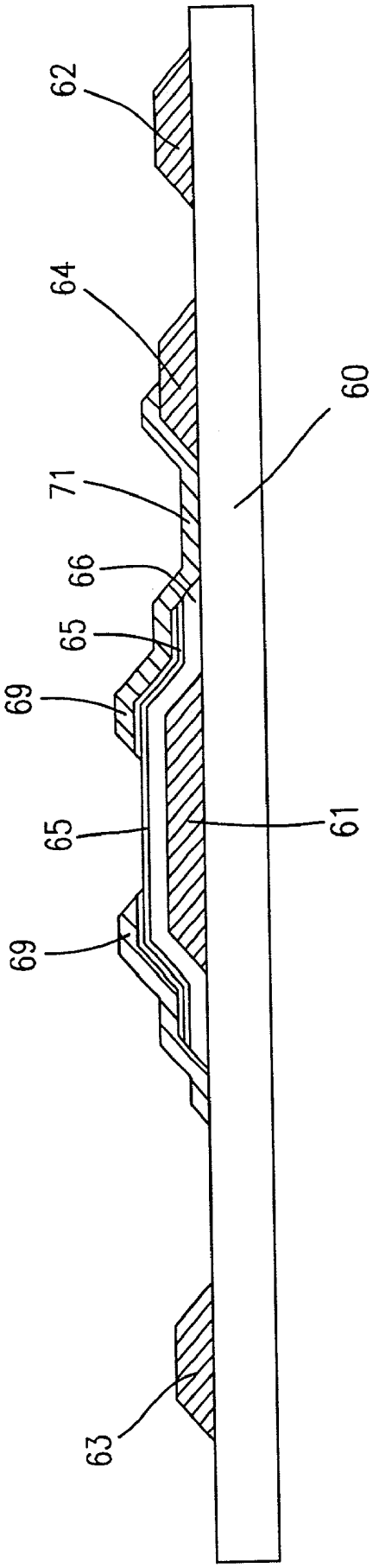


Fig. 5(d)

MANUFACTURING METHOD FOR IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY (LCD) UNIT

FIELD OF THE INVENTION

[0001] The present invention is related to a manufacturing method for a liquid crystal display (LCD) unit, and more particularly to a manufacturing method for an in-plane switching mode liquid crystal display (LCD) unit.

BACKGROUND OF THE INVENTION

[0002] As the technique is developing, it is the trend that the liquid crystal display (LCD) takes the place of the conventional picture tube display and becomes the main stream in the market. Please refer to **FIG. 1**(*a*). **FIG. 1**(*a*) is a diagram illustrating the circuit of a pixel unit in a liquid crystal display according to the prior art. It is composed of a display unit **12**, a storage capacitor **13**, and a switching unit accomplished by a thin film transistor **11**. Regarding the structure of the display unit **12**, it is mainly divided into two types at present. The common structure is a twisted nematic liquid crystal display (TN-LCD), as shown in **FIG. 1**(*b*). In **FIG. 1**(*b*), the data electrode **121** and the common electrode **122** are mounted at both sides of the liquid crystal molecule **123**. The cell gap between the upper and lower glasses is "d." Through controlling the potential difference between the data electrode **121** and the common electrode **122** (the direction of the electric field is shown in a dotted line in the diagram), the liquid crystal molecule **123** can stand erect to form the included angle between the liquid crystal molecule **123** and the Z-axis. Therefore, the light-pervious rate will follow to be changed according to the included angle and the pixel brightness can be controlled. However, due to the rotation way of the liquid crystal molecule in the above display unit structure, the distribution of plural refractions is very different while the watcher has different visual angles, for example, in the inclined directions of A-A' and B-B' (as shown in **FIG. 1**(*b*)). Besides, the pervious rate will be very different and the disadvantage that the bigger visual angle cannot be provided will be existed. Therefore, the above display unit structure has its limitation indeed, especially that the superficial size of the display panel is getting increased at the present time.

[0003] Compared with the second type structure (TN-LCD), the first type structure (TN-LCD) has the disadvantage that the rotation way of the liquid crystal molecule has a smaller visual angle. On the contrary, the display unit structure **12** in the second type has a better range of visual angle. Please refer to **FIG. 1**(*c*). **FIG. 1**(*c*) is a diagram illustrating the display unit structure **12** of an in-plane switching mode (IPS mode) according to the prior art. It is clear in the diagram that the data electrode **121** and the common electrode **122** are mounted at the same side of the liquid crystal molecule **123**. Therefore, while the potential difference between the data electrode **121** and the common electrode **122** is changed (the direction of the electric field is shown in a dotted line in the diagram), the liquid crystal molecule **123** will take Z-axis as the axle center and rotate around it. The light-pervious rate will follow to be changed and the pixel brightness control will be accomplished. The rotation way of the liquid crystal molecule in this kind of display unit structure will not have a light-pervious rate change while the watcher has different visual angles. Therefore, it has the advantage that a bigger visual angle can be provided, and it will help a lot for manufacturing the display panel with bigger size.

[0004] Please refer to FIGS. **2**(*a*) and **2**(*b*). **FIG. 2**(*a*) is a top view showing the pixel unit structure of the in-plane switching mode (IPS mode) in the first conventional thin film transistor LCD according to the prior art. **FIG. 2**(*b*) is a sectional view along the A-B line segment showing the pixel unit structure of the in-plane switching mode (IPS mode) in the first conventional thin film transistor LCD according to the prior art. The pixel unit structure is accomplished by the following process:

[0005] (a) forming a first mental layer on the substrate **20** and defining thereon a gate line **21**, a common electrode **22** of the display unit, and a wiring pad **23** needed for the periphery (the first photo etching process (PEP)).

[0006] (b) depositing a gate insulation layer **24**, a semi-conductive layer, and a relatively high doped semi-conductive layer, and additionally, defining a channel structure **25**(the second photo etching process (PEP)).

[0007] (c) forming a second mental layer and defining a source/drain electrode region **26** of thin film transistor, a data line **27**, and pixel electrode **28** of the display unit (the third photo etching process (PEP)).

[0008] (d) depositing a passivation layer **29** and defining a contact window **231** on the wiring pad **23** (the fourth photo etching process (PEP)).

[0009] It is clear in **FIG. 2**(*a*) and **2**(*b*) that the common electrode **22** and pixel electrode **28** of the display unit are respectively accomplished from the first mental layer and the second mental layer, which forms two flats with different altitudes. Therefore, the curve of the data voltage and the pervious rate is asymmetric, as shown in **FIG. 2**(*c*). Besides, the display image will have the drawbacks of image-sticking and flicker. Since the common electrode **22** and pixel electrode **28** of the display unit are respectively accomplished from the first mental layer and the second mental layer in two different photo etching processes, the two electrodes will unavoidably have the problem of misalignment, which will cause uneven light-pervious rate and mura.

[0010] In order to improve the above drawbacks, another conventional pixel unit structure is developed, as shown in **FIG. 3**. **FIG. 3**(*a*) is a top view showing the pixel unit structure of the in-plane switching mode (IPS mode) in the second conventional thin film transistor LCD according to the prior art. **FIG. 3**(*b*) is a sectional view along the A-B line segment showing the pixel unit structure of the in-plane switching mode (IPS mode) in the second conventional thin film transistor LCD according to the prior art. The pixel unit structure is accomplished by the following process:

[0011] (a) forming a first mental layer on the substrate **30** and defining thereon a gate line **31**, a common electrode **32** of the display unit, a lower electrode **320** for storing capacitance, and a wiring pad **33** needed for the periphery (the first photo etching process (PEP)).

[0012] (b) depositing a gate insulation layer **34**, a semi-conductive layer, and a relatively high doped

semi-conductive layer, and additionally, defining a channel structure **35**(the second photo etching process (PEP)).

[**0013**] (c) forming a second mental layer and defining a source/drain electrode region **36** of thin film transistor, a data line **37**, and an upper electrode **38** for storing capacitance (the third photo etching process (PEP)).

[**0014**] (d) depositing a passivation layer **39** and respectively defining contact windows **331**, **381**, and **321** on the wiring pad **33**, the upper electrode **38** for storing capacitance, and the common electrode **32** (the fourth photo etching process (PEP)).

[**0015**] (e) forming a third mental layer and defining two comb-shaped electrodes **382** and **322** to have electric contact with the upper electrode **38** and the common electrode **32** through the contact windows **381** and **321** respectively (the fifth photo etching process (PEP)).

[**0016**] It is known from the above description that the two comb-shaped electrodes **382** and **322** are accomplished at the flats with same altitudes in the same photo etching process. Since there is no altitude difference between the two comb-shaped electrodes **382** and **322**, it will not result in the problem of misalignment. Although the drawback of the former technique is solved, however, the steps of the photo etching process (PEP) are too many, which will lower the yield efficiency and increase the cost. Hence, how to rectify the foresaid conventional drawback has become the main purpose of the present invention.

SUMMARY OF THE INVENTION

[**0017**] It is an object of the present invention to provide a manufacturing method for an in-plane switching mode liquid crystal display (LCD) unit with reduced steps of the photo etching process (PEP).

[**0018**] It is another object of the present invention to provide a manufacturing method for an in-plane switching mode liquid crystal display (LCD) unit to reduce the manufacturing cost and increase the yield efficiency.

[**0019**] According to the present invention, a manufacturing method for in-plane switching mode liquid crystal display (LCD) unit includes steps of: providing a substrate, forming a first conductive layer on said substrate; patterning said first conductive layer to form a gate line, a comb-shaped first electrode, a wiring pad, and a comb-shaped second electrode by a first photo etching process (PEP), forming a first insulation layer and a first semi-conductive layer on said substrate in sequence; patterning said first insulation layer and said first semi-conductive layer to form a channel, an insulation structure, a dielectric layer for storing capacitance, and plural crossed-conductive line insulation structures by a second photo etching process (PEP), forming a second semi-conductive layer and a second conductive layer on said substrate; patterning said second semi-conductive layer and said second conductive layer to form a source/drain electrode, a data line, a connecting electrode, and a first electrode for storing capacitance by a third photo etching process (PEP), wherein said data line covers said crossed-conductive line insulation structure thereon and connects said drain electrode, said connecting electrode is connected between said source electrode and said comb-shaped second electrode, and said first electrode for storing capacitance covers said dielectric layer for storing capacitance thereon and connects said comb-shaped second electrode; and forming a passivation layer on said substrate except partial region of said wiring pad.

[**0020**] In accordance with the present invention, the step of forming a passivation layer further comprises the step of: patterning said passivation layer by a fourth photo etching process (PEP), wherein said passivation layer having a wiring hole on said wring pad.

[**0021**] Preferably, the step of forming a passivation layer further comprises the step of: forming said passivation structure on said substrate except partial region of said wiring pad by a mask deposition method to generate a wiring hole on said wring pad.

[**0022**] Preferably, the substrate is a glass substrate pervious to light.

[**0023**] Preferably, the first conductive and said second conductive layer are made of a material selected from a group consisted of chromium, molybdenum, tantalum molybdate, tungsten molybdate, tantalum, aluminum, aluminum silicide, copper and the combination thereof.

[**0024**] Preferably, the gate insulation layer is made of a material selected from of a group consisted of silicon nitride (SiN_X), silicon oxide (SiO_X), silicon oxynitride (SiO_XN_Y), tantalum oxide (TaO_X), aluminum oxide (AlO_X) and the combination thereof.

[**0025**] Preferably, the first semi-conductive layer is made of a material selected from of a group consisted of intrinsic amorphous silicon, intrinsic micro-crystalline silicon, and intrinsic polycrystalline silicon.

[**0026**] Preferably, the second semi-conductive layer is made of a material selected from of a group consisted of N-typed highly doped amorphous silicon, N-typed highly doped micro-crystalline silicon, P-typed highly doped micro-crystalline silicon, N-typed highly doped polycrystalline silicon, and P-typed highly doped polycrystalline silicon.

[**0027**] Preferably, the passivation structure is made of a material selected from of a group consisted of silicon nitride (SiN_X), silicon oxide (SiO_X), and silicon oxynitride (SiO_XN_Y).

[**0028**] Preferably, the comb-shaped first electrode structure has a comb-shaped structure crossly and parallelly mounted between a comb-shaped structure of said comb-shaped second electrode.

[**0029**] Preferably, the dielectric layer for storing capacitance covers thereon a lower electrode under an storage capacitor of said comb-shaped common electrode structure.

[**0030**] Preferably, the second semi-conductive layer has relatively high doped than first semi-conductive layer.

[**0031**] Preferably, the comb-shaped first electrode is a comb-shaped common electrode.

[**0032**] Preferably, the comb-shaped second electrode is a comb-shaped pixel electrode.

[0033] The foregoing and other features and advantages of the present invention will be more clearly understood through the following descriptions with reference to the drawings, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] **FIG. 1**(*a*) is a diagram illustrating the circuit of a pixel unit in a liquid crystal display according to the prior art;

[0035] FIGS. **1**(*b*) and (*c*) are diagrams illustrating the display unit structures belonged to two types according to the prior art;

[0036] **FIG. 2**(*a*) is a top view showing the pixel unit structure of the in-plane switching mode (IPS mode) in the first conventional thin film transistor LCD according to the prior art;

[0037] **FIG. 2**(*b*) is a sectional view along the A-B line segment showing the pixel unit structure of the in-plane switching mode (IPS mode) in the first conventional thin film transistor LCD according to the prior art;

[0038] **FIG. 2**(*c*) is a diagram illustrating the asymmetric curve of the data voltage and the penetrating rate in the first conventional thin film transistor LCD according to the prior art;

[0039] **FIG. 3**(*a*) is a top view showing the pixel unit structure of the in-plane switching mode (IPS mode) in the second conventional thin film transistor LCD according to the prior art;

[0040] **FIG. 3**(*b*) is a sectional view along the A-B line segment showing the pixel unit structure of the in-plane switching mode (IPS mode) in the second conventional thin film transistor LCD according to the prior art;

[0041] FIGS. **4**(*a*)-(*h*) are diagrams illustrating the structures and manufacturing processes of the in-plane switching mode liquid crystal display (LCD) unit according to a preferred embodiment of the present invention; and

[0042] FIGS. **5**(*a*)-(*d*) are diagrams illustrating the structures and manufacturing processes of the in-plane switching mode liquid crystal display (LCD) unit according to another preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0043] In order to improve the conventional technique, a manufacturing method for the in-plane switching mode liquid crystal display (LCD) unit with reduced steps is developed in the present invention. Please refer to FIGS. **4**(*a*)-(*h*). FIGS. **4**(*a*)-(*h*) are diagrams illustrating the structures and manufacturing processes of the in-plane switching mode liquid crystal display (LCD) unit according to a preferred embodiment of the present invention. In **FIG. 4**(*a*), an insulation substrate **40** is provided, and a first conductive layer is formed on the insulation substrate **40**. Afterward, a gate line structure **41**, a comb-shaped common electrode structure **42**, a wiring pad **43**, and a comb-shaped pixel electrode **44** are defined by the first photo etching process (PEP). The sectional view along the A-B line segment is shown in **FIG. 4**(*b*). In **FIG. 4**(*c*), a gate insulation layer and a semi-conductive layer are formed on the insulation substrate **40** in sequence. Then, the channel structure **45**, the insulation structure **46**, the dielectric layer **47** for storing capacitance, and plural crossed-conductive line insulation structures **48** are defined by the second photo etching process (PEP). Nevertheless, the dielectric layer **47** for storing capacitance covers the lower electrode which is disposed in the comb-shaped common electrode structure **42** for storing capacitance. The sectional view along the A-B line segment is shown in **FIG. 4**(*d*). In **FIG. 4**(*e*), a relatively high doped semi-conductive layer and a second conductive layer are formed on the insulation substrate, and a source/drain electrode structure **49**, a data line **50**, a connecting electrode **51**, and an upper electrode **52** for storing capacitance are defined thereon by the third photo etching process (PEP). Nevertheless, the data line **50** covers the crossed-conductive line insulation structure **48** and connects the drain electrode structure. The connecting electrode **51** is connected between the source electrode structure and the comb-shaped pixel electrode **44**. The upper electrode **52** covers the dielectric layer **47** and connects the comb-shaped pixel electrode **44**. The sectional view along the A-B line segment is shown in **FIG. 4**(*f*). Additionally, a passivation structure **53** is formed on the insulation substrate **40**, except partial region of the wiring pad **43**. The forming way of the passivation structure **53** can be chosen form one of the following two ways. The first way is shown in **FIG. 4**(*g*). After forming a passivation layer on the insulation substrate **40**, the passivation layer is defined by the fourth photo etching process (PEP). Then the passivation structure **53** with the wiring hole **531** on the wring pad **43** is formed. The second way is shown in **FIG. 4**(*h*). The passivation structure is directly formed by a mask deposition method. Since the mask above the wring pad **43** is hollow, the region around substrate can be covered. Without the need of the fourth photo etching process (PEP), the passivation structure **53** can be directly formed on the insulation substrate **40**, except partial region of the wiring pad **43**, where is the region for connecting lines.

[0044] In another preferred embodiment of the present invention, the only differences compared to the previous embodiment are in the steps of the second and the third photo etching process, as shown in FIGS. **5**(*a*)-(*d*). In **FIG. 5**(*a*), on the insulation substrate **60**, a gate line structure **61**, a comb-shaped common electrode structure **62**, a wiring pad **63**, and a comb-shaped pixel electrode **64** are defined by the first photo etching process (PEP). Afterwards, a gate insulation layer, a semi-conductive layer and a relatively high doped semi-conductive layer is formed on the insulation substrate **60** in sequence. Nevertheless, a channel structure **65**, an insulation structure **66**, a dielectric layer **67** for storing capacitance, and plural crossed-conductive line insulation structures **68** are defined by a second photo etching process (PEP). The dielectric layer **67** for storing capacitance covers the lower electrode which is disposed in the comb-shaped common electrode structure **62** for storing capacitance, as shown in FIGS. **5**(*a*)-(*b*). In **FIG. 5**(*c*), after the second conductive layer is formed on the insulation substrate **60**, a source/drain electrode structure **69** are defined on the relatively high doped semi-conductive layer. A data line **70**, a connecting electrode **71**, and an upper electrode **72** for storing capacitance are then defined by the third photo etching process (PEP). The data line **70** covers the crossed-conductive line insulation structure **68** and connects the drain electrode structure. The connecting electrode **71** is

connected between the source electrode structure and the comb-shaped pixel electrode **64**. The upper electrode **72** covers the dielectric layer **67** and connects the comb-shaped pixel electrode **64**, as shown in FIGS. **5**(*c*)-(*d*). The forming way of the passivation structure **53** is similar to that of the above-described embodiment of the present invention, and it is therefore not to be described repeatedly.

[0045] In the above preferred embodiments, the insulation substrate is a glass substrate pervious to light. As for the first conductive and the second conductive layer, which are made of the material selected from a group consisted of chromium, molybdenum, tantalum molybdate, tungsten molybdate, tantalum, aluminum, aluminum silicide, copper and the combination thereof. The gate insulation layer is made of the material selected from of a group consisted of silicon nitride (SiN_X), silicon oxide (SiO_X), silicon oxynitride (SiO_XN_Y), tantalum oxide (TaO_X), aluminum oxide (AlO_X) and the combination thereof. The semi-conductive layer is made of the material selected from of a group consisted of intrinsic amorphous silicon, intrinsic micro-crystalline silicon, and intrinsic polycrystalline silicon. The relatively high doped semi-conductive layer is made of the material selected from of a group consisted of N-typed highly doped amorphous silicon, N-typed highly doped micro-crystalline silicon, P-typed highly doped micro-crystalline silicon, N-typed highly doped polycrystalline silicon, and P-typed highly doped polycrystalline silicon.

[0046] From the above description of the processing steps and the accomplished structures of the preferred embodiments, the two comb-shaped structures are mounted crossly and parallelly to each other at the plats with same altitudes, and additionally, in the same photo etching process. Therefore, since there is no altitude difference between the two comb-shaped electrodes, it will not result in the problem of misalignment. Besides, the needed steps of photo etching process (PEP) are reduced to four or even three steps. Indeed, the yield efficiency can be increased and the cost can be lower. Hence, the drawback of the conventional technique is improved and the main purpose of the present invention is achieved.

[0047] While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

ATTACHMENT

ATTORNEYS OF Haverstock & Owens LLP

[0048]

Thomas B. Haverstock	Reg. No. 32,571
Jonathan O. Owens	Reg. No. 37,902
Ronald R. Shea	Reg. No. 45,098
Michael O'Connell (Agent)	Reg. No. 42,950
James A. Gavney (Agent)	Reg. No. 45,687
Suvashis Bhattacharya (Agent)	Reg. No. 46,554

What is claimed is:

1. A manufacturing method for in-plane switching mode liquid crystal display (LCD) unit, comprising the steps of:

providing a substrate;

forming a first conductive layer on said substrate;

patterning said first conductive layer to form a gate line, a comb-shaped first electrode, a wiring pad, and a comb-shaped second electrode by a first photo etching process (PEP);

forming a first insulation layer and a first semi-conductive layer on said substrate in sequence;

patterning said first insulation layer and said first semi-conductive layer to form a channel, an insulation structure, a dielectric layer for storing capacitance, and plural crossed-conductive line insulation structures by a second photo etching process (PEP);

forming a second semi-conductive layer and a second conductive layer on said substrate;

patterning said second semi-conductive layer and said second conductive layer to form a source/drain electrode, a data line, a connecting electrode, and a first electrode for storing capacitance by a third photo etching process (PEP), wherein said data line covers said crossed-conductive line insulation structure thereon and connects said drain electrode, said connecting electrode is connected between said source electrode and said comb-shaped second electrode, and said first electrode for storing capacitance covers said dielectric layer for storing capacitance thereon and connects said comb-shaped second electrode; and

forming a passivation layer on said substrate except partial region of said wiring pad.

2. The manufacturing method according to claim 1, wherein said step of forming a passivation layer further comprises the step of:

patterning said passivation layer by a fourth photo etching process (PEP), wherein said passivation layer having a wiring hole on said wring pad.

3. The manufacturing method according to claim 1, wherein said step of forming a passivation layer further comprises the step of:

forming said passivation structure on said substrate except partial region of said wiring pad by a mask deposition method to generate a wiring hole on said wring pad.

4. The manufacturing method according to claim 1, wherein said substrate is a glass substrate pervious to light.

5. The manufacturing method according to claim 1, wherein said first conductive and said second conductive layer are made of a material selected from a group consisted of chromium, molybdenum, tantalum molybdate, tungsten molybdate, tantalum, aluminum, aluminum silicide, copper and the combination thereof.

6. The manufacturing method according to claim 1, wherein said insulation layer is made of a material selected from of a group consisted of silicon nitride (SiN_X), silicon oxide (SiO_X), silicon oxynitride (SiO_XN_Y), tantalum oxide (TaO_X), aluminum oxide (AlO_X) and the combination thereof.

7. The manufacturing method according to claim 1, wherein said first semi-conductive layer is made of a material selected from of a group consisted of intrinsic amorphous silicon, intrinsic micro-crystalline silicon, and intrinsic polycrystalline silicon.

8. The manufacturing method according to claim 1, wherein said second semi-conductive layer is made of a material selected from of a group consisted of N-typed highly doped amorphous silicon, N-typed highly doped micro-crystalline silicon, P-typed highly doped micro-crystalline silicon, N-typed highly doped polycrystalline silicon, and P-typed highly doped polycrystalline silicon.

9. The manufacturing method according to claim 1, wherein said passivation layer is made of a material selected from of a group consisted of silicon nitride (SiN_X), silicon oxide (SiO_X), and silicon oxynitride (SiO_XN_Y).

10. The manufacturing method according to claim 1, wherein said comb-shaped first electrode structure has a comb-shaped structure crossly and parallelly mounted between a comb-shaped structure of said comb-shaped second electrode.

11. The manufacturing method according to claim 1, wherein said dielectric layer for storing capacitance covers thereon a lower electrode under an storage capacitor of said comb-shaped common electrode structure.

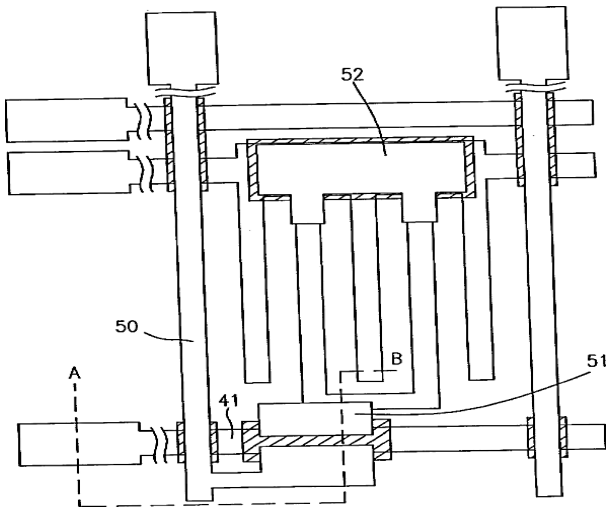
12. The manufacturing method according to claim 1, wherein said second semi-conductive layer has relatively high doped than first semi-conductive layer.

13. The manufacturing method according to claim 1, wherein said comb-shaped first electrode is a comb-shaped common electrode.

14. The manufacturing method according to claim 1, wherein said comb-shaped second electrode is a comb-shaped pixel electrode.

* * * * *

专利名称(译)	面内切换模式液晶显示（LCD）单元的制造方法		
公开(公告)号	US20030058396A1	公开(公告)日	2003-03-27
申请号	US10/157453	申请日	2002-05-28
[标]申请(专利权)人(译)	瀚宇彩晶股份有限公司		
申请(专利权)人(译)	瀚宇彩晶股份有限公司.		
当前申请(专利权)人(译)	瀚宇彩晶股份有限公司.		
[标]发明人	SHIH PO SHENG		
发明人	SHIH, PO-SHENG		
IPC分类号	G02F1/1343 G02F1/1362		
CPC分类号	G02F1/134363 G02F1/13458		
优先权	090123652 2001-09-25 TW		
其他公开文献	US6757041		
外部链接	Espacenet USPTO		

摘要(译)

提供一种用于面内切换模式液晶显示（LCD）单元的制造方法。该方法包括以下步骤：提供衬底，在衬底上形成第一导电层，图案化第一导电层以形成栅极线，梳状第一电极，布线焊盘和梳状第二电极第一光刻工艺，形成第一绝缘层和第一半导体层，图案化第一绝缘层和第一半导体层以形成沟道，绝缘结构，介电层和多个交叉导线绝缘通过第二光刻工艺形成结构，在基板上形成第二半导体层和第二导电层，图案化第二半导体层和第二导电层以形成源/漏电极，数据线，连接电极和第一电极通过第三光刻工艺，并形成钝化层。