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(54) LIQUID CRYSTAL DISPLAY USING SWING COMMON ELECTRODE AND A METHOD FOR DRIVING THE SAME

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(57) **ABSTRACT**

A liquid crystal display includes swing common electrodes for storage capacitors to sequentially apply signal voltages based on display data to target pixels to display picture images at respective frames. The voltage applied to the common electrodes is terminated with minus (−) during the period of gate on in case the pixel voltage is inverted from minus (−) to plus (+) while being terminated with plus (+) in case the pixel voltage is inverted from plus (+) to minus (−). The common voltage is repeatedly swung from minus (−) to plus (+) after the gate turns off. In these conditions, the respective common electrode lines for the storage capacitors are periodically swung synchronized with gate pulses to thereby generate overshoot. The response speed of the liquid crystal is enhanced due to the overshoot when the gray scale is altered due to the memory effect of the liquid crystal capacitor.

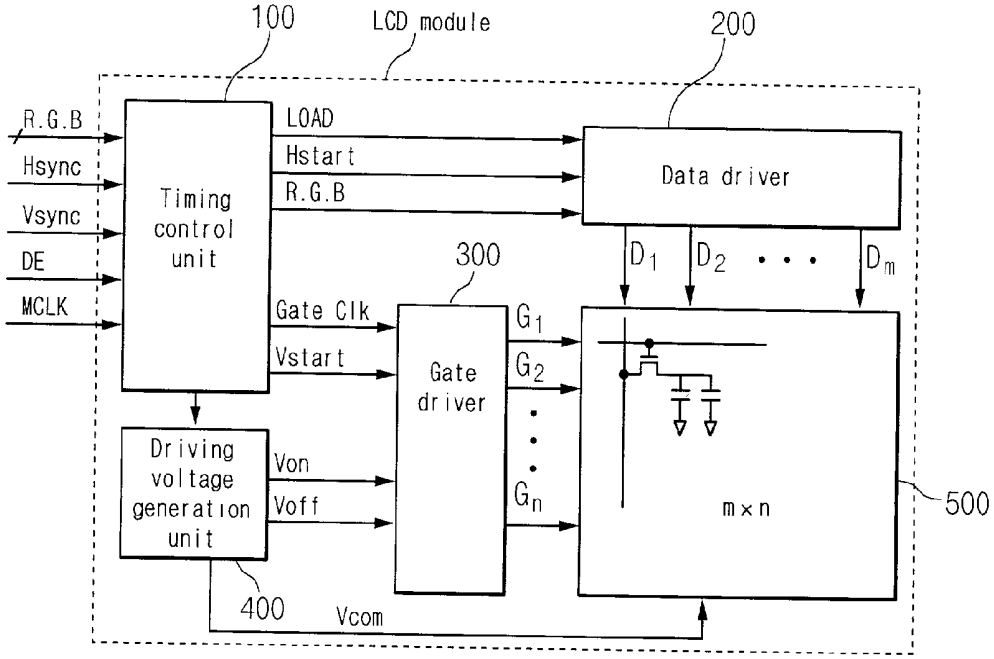


Fig. 1
Prior art

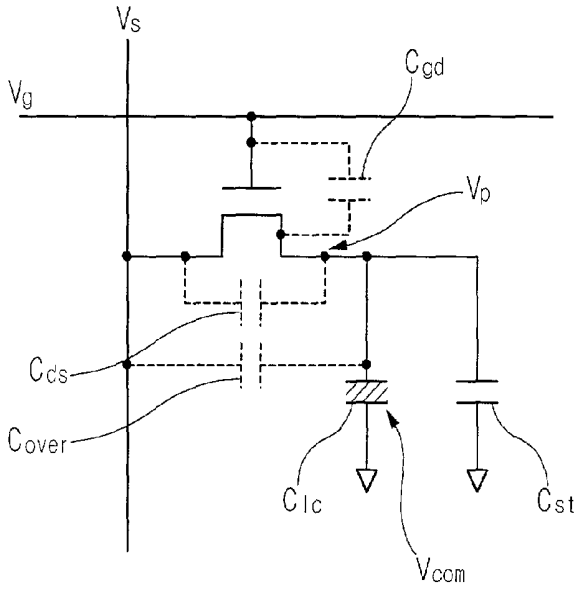


Fig. 2
Prior art

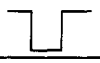
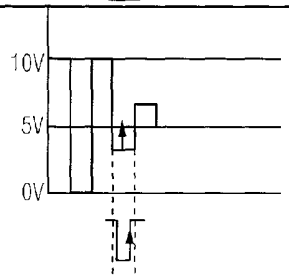
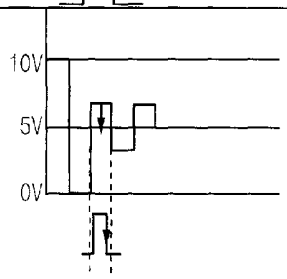
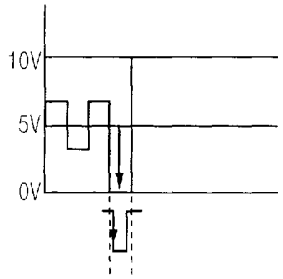
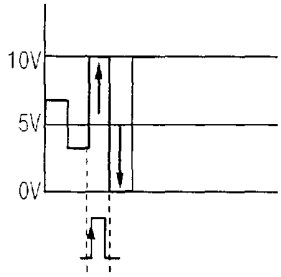
	(+)→(-) Inversion	(-)→(+) Inversion
Form of Pulse signal application to storage COM		
□Dielectric constnat - High → Low □Voltage - High → Low □Gray - High → Low	 Effect of approximating data signal to COM signal	 Effect of approximating data signal to COM signal
□Dielectric constnat - Low → High □Dielectric constnat - Low → High □Dielectric constnat - High → Low	 Overshoot of data voltage	 Overshoot of data voltage

Fig. 3

Prior art

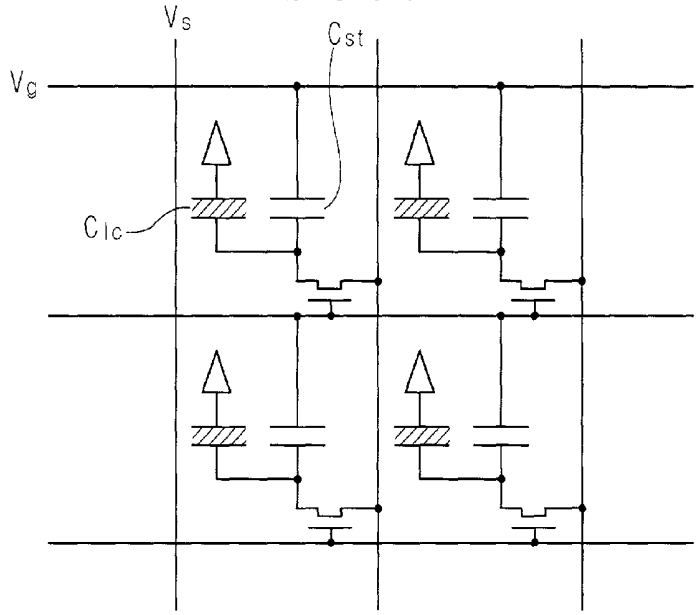


Fig. 4

Prior art

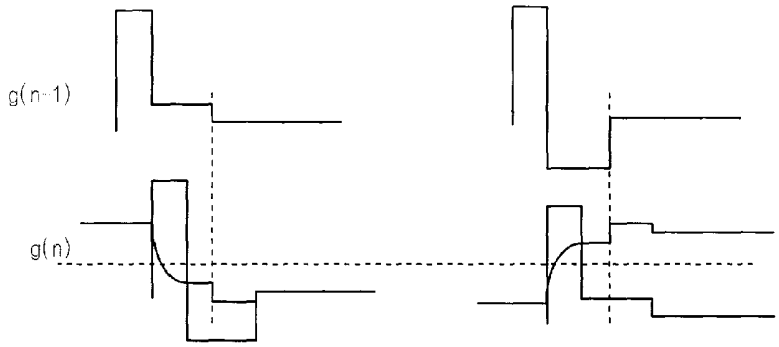


Fig. 5

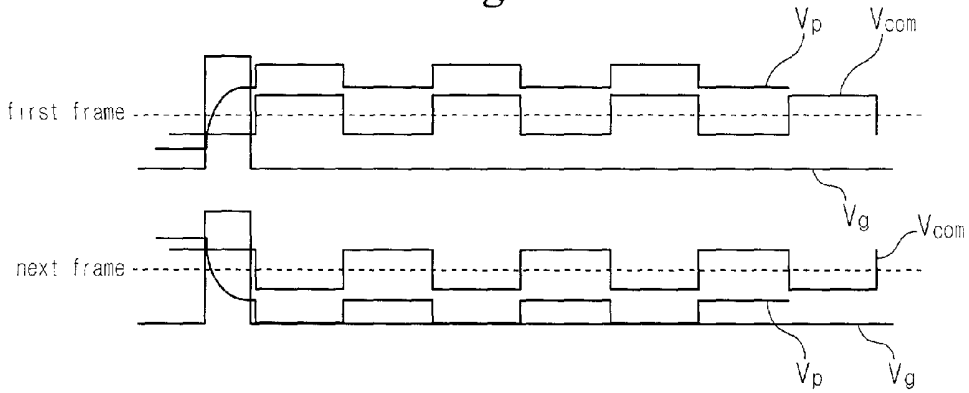


Fig. 6

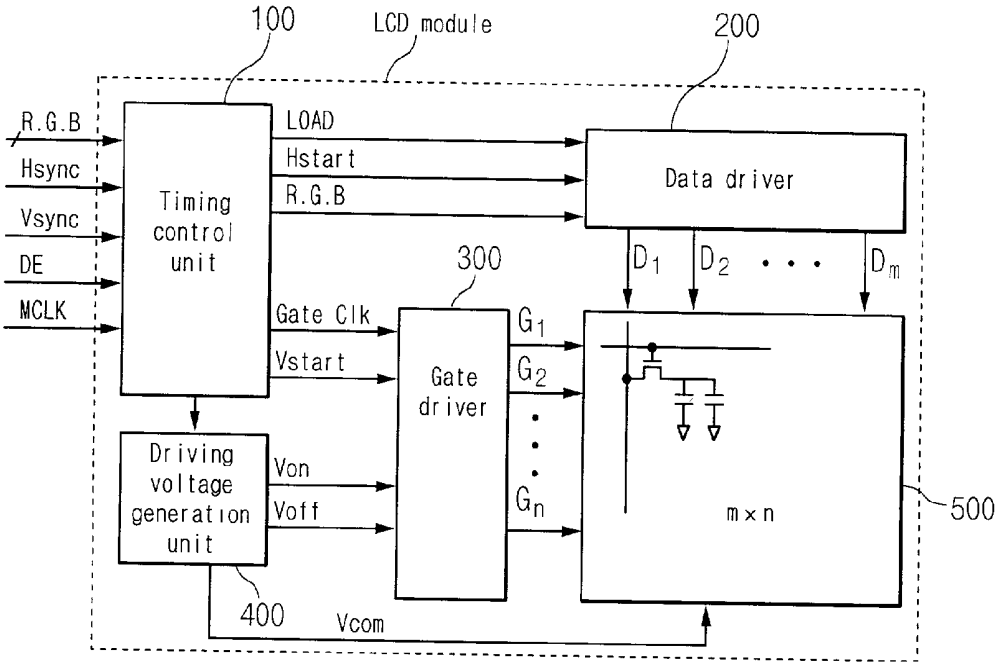

100
LCD module
200
R.G.B
Hsync
Vsync
DE
MCLK
Timing control unit
LOAD
Hstart
R.G.B
Data driver
D1
D2
Dm
300
Gate Clk
Vstart
Gate driver
G1
G2
Gn
Driving voltage generation unit
Von
Voff
m×n
500
400
Vcom

Fig. 7

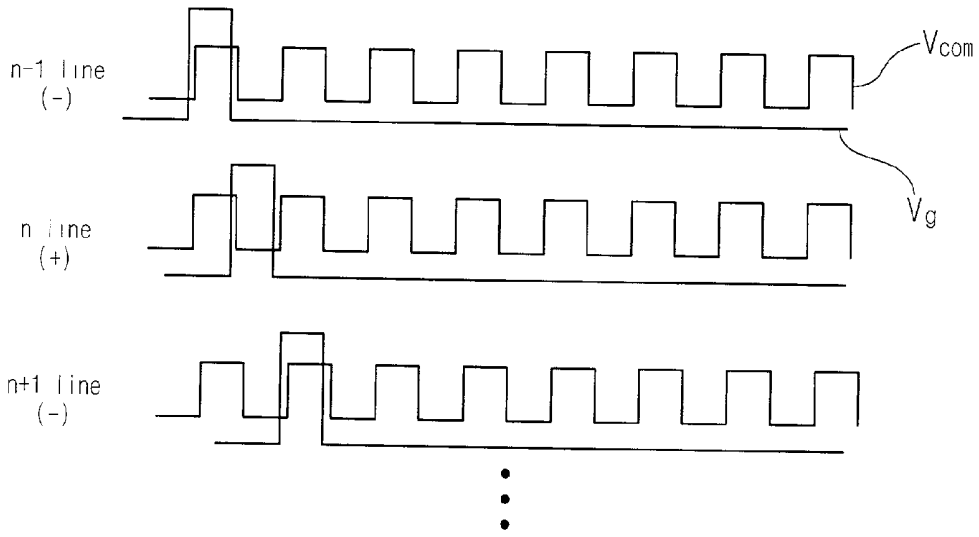

n-1 line
(-)
Vcom
Vg
n line
(+)
n+1 line
(-)

Fig. 8

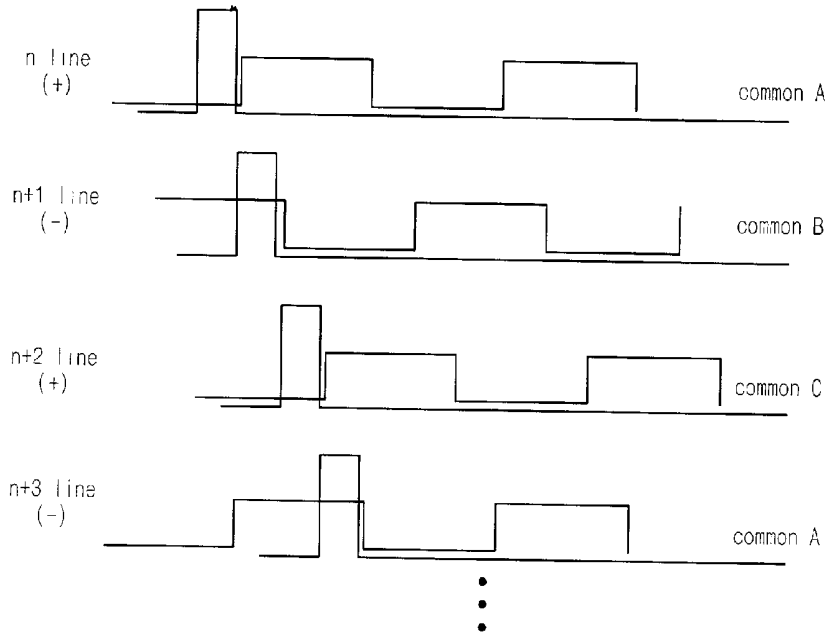


Fig. 9

Prior art

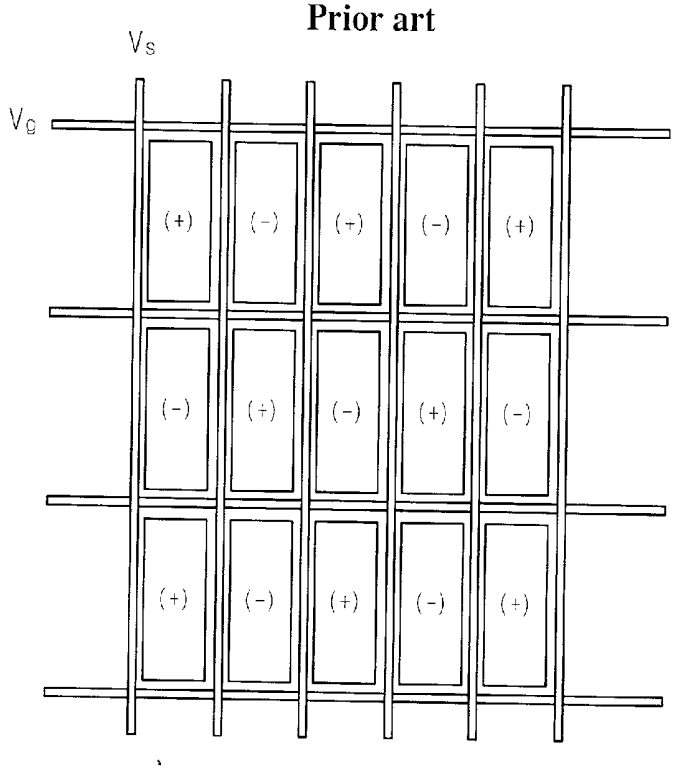


Fig. 10

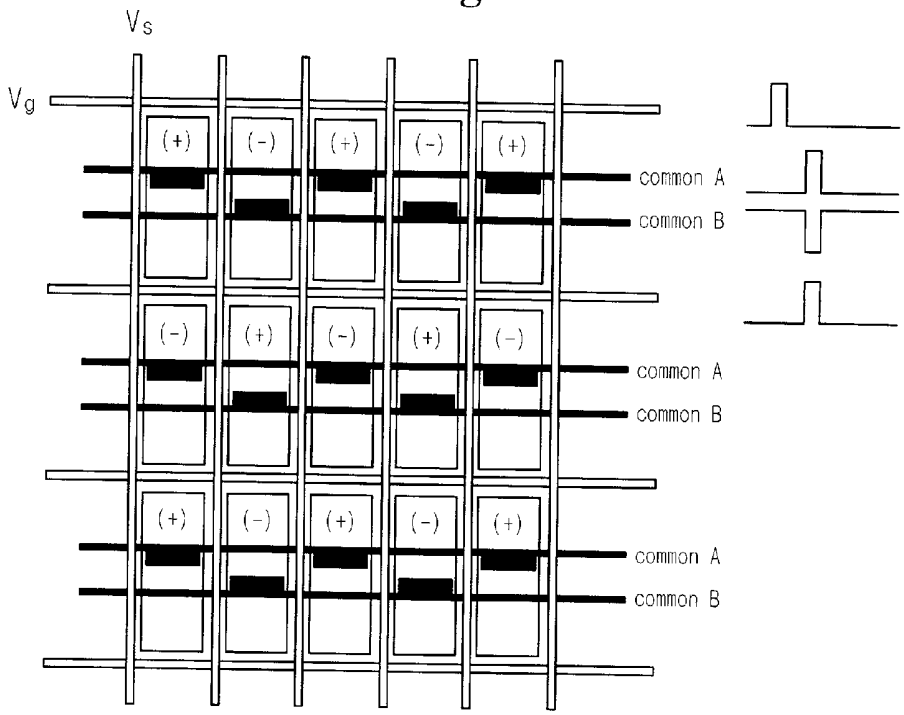

Vs
Vg
(+)
(-)
common A
common B

Fig. 11

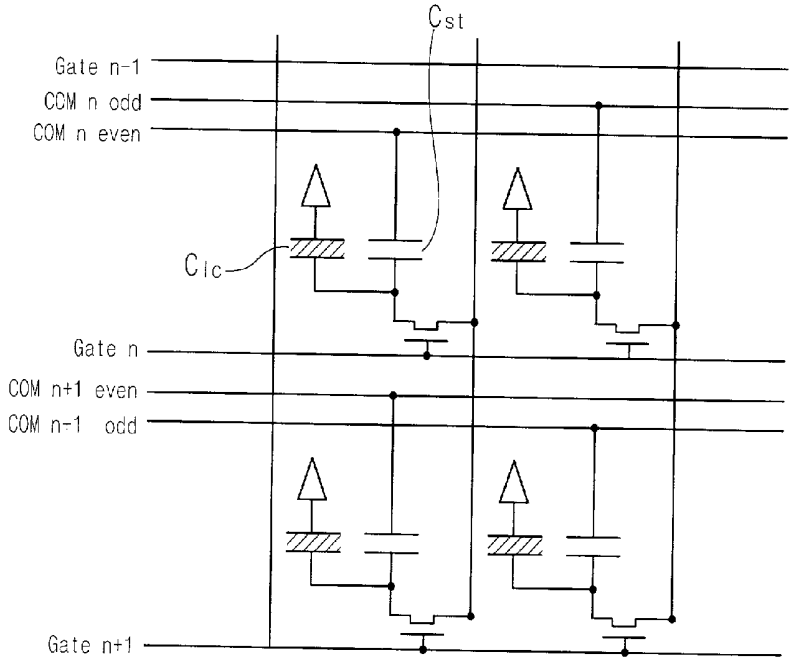

Cst
Gate n-1
COM n odd
COM n even
Clc
Gate n
COM n+1 even
COM n-1 odd
Gate n+1

Fig. 12

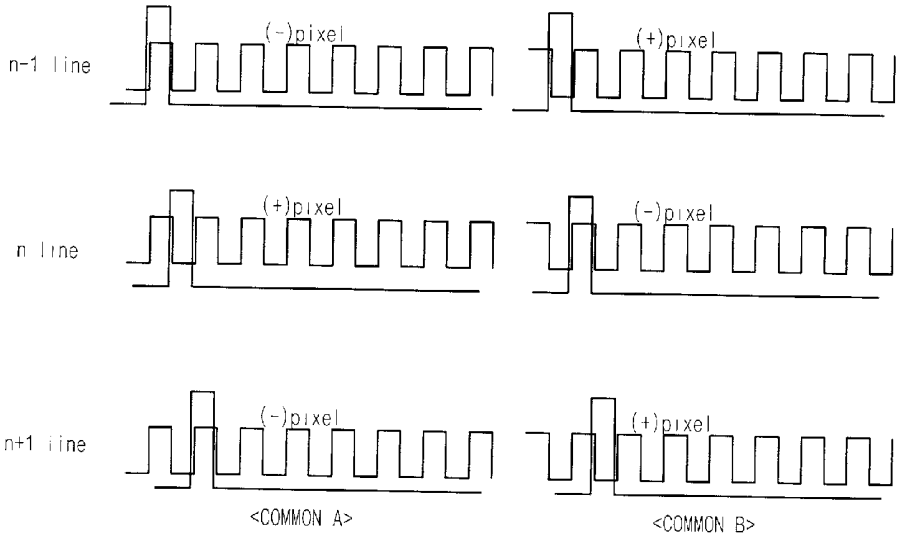

n-1 line
(-)pixel
(+)pixel
n line
(+)pixel
(-)pixel
n+1 line
(-)pixel
(+)pixel
<COMMON A>
<COMMON B>

Fig. 13

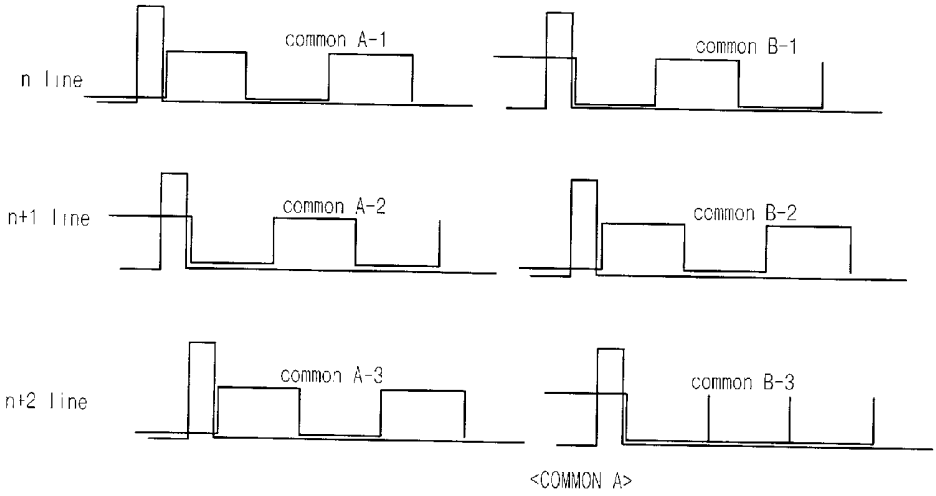

n line
common A-1
common B-1
n+1 line
common A-2
common B-2
n+2 line
common A-3
common B-3
<COMMON A>

Fig. 14

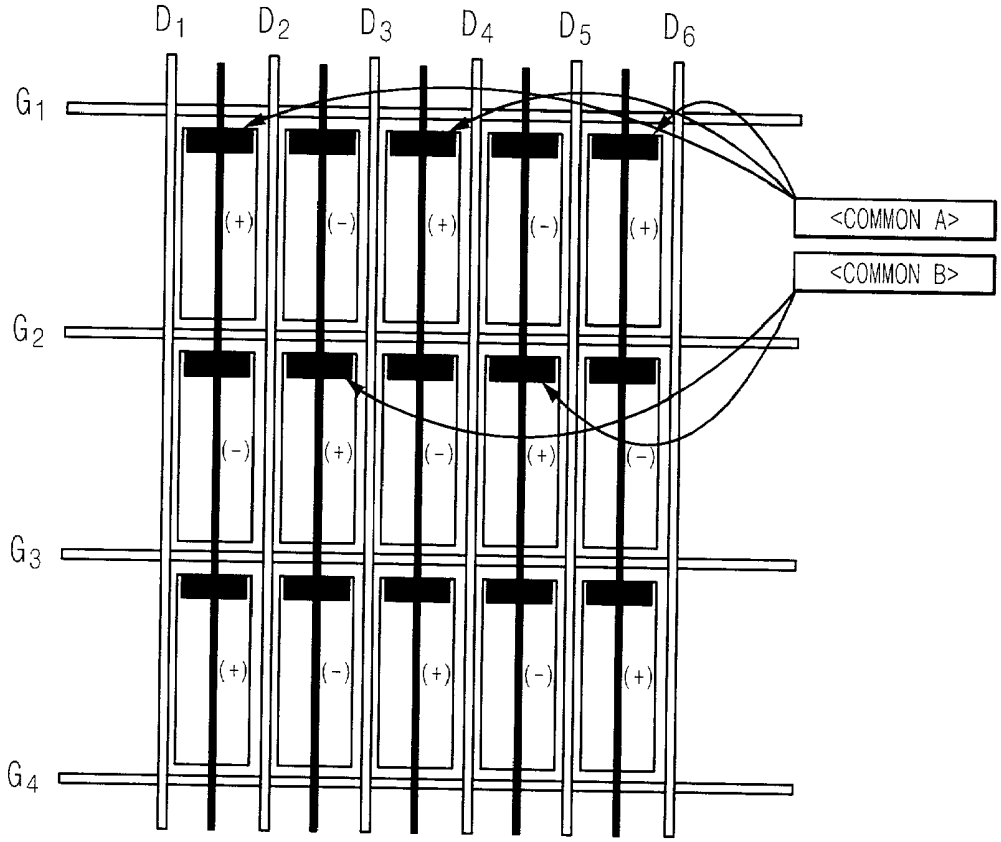


Fig. 15

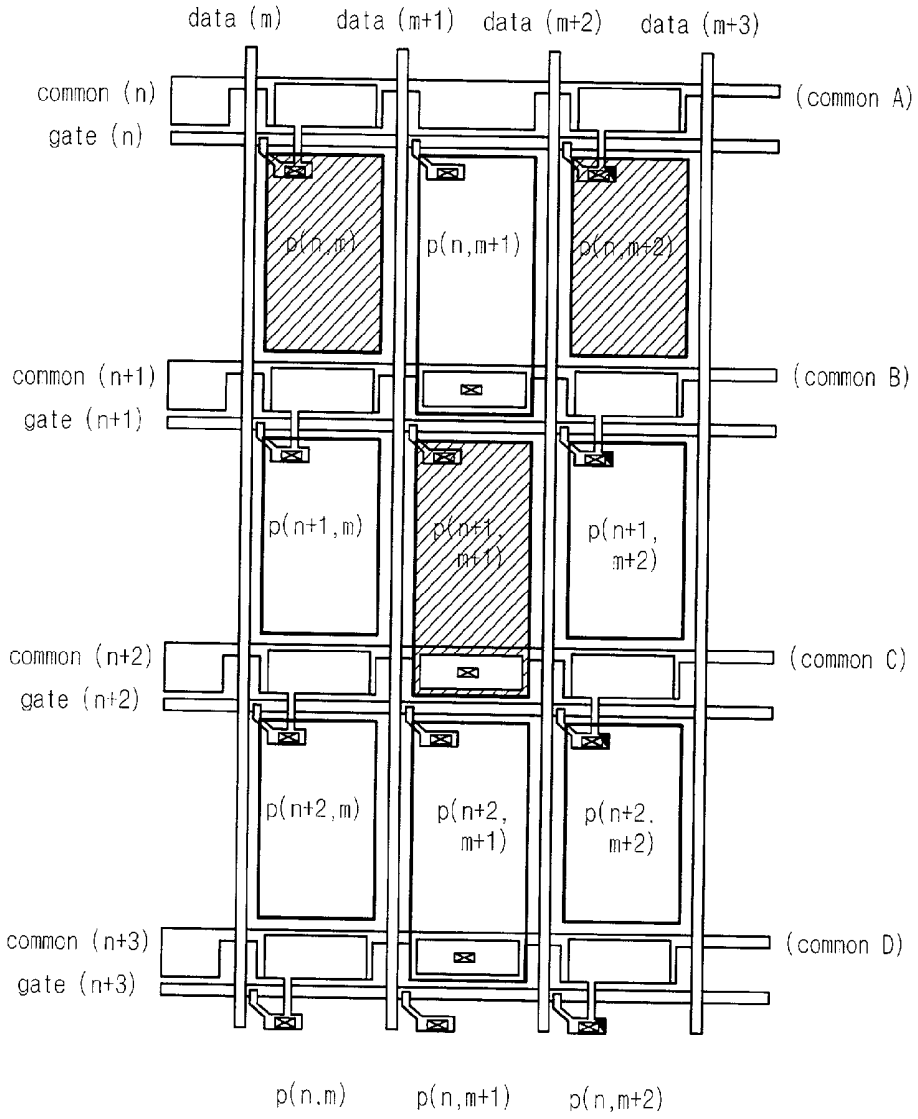

data (m)
data (m+1)
data (m+2)
data (m+3)
common (n)
gate (n)
(common A)
p(n,m)
p(n,m+1)
p(n,m+2)
common (n+1)
gate (n+1)
(common B)
p(n+1,m)
p(n+1, m+1)
p(n+1, m+2)
common (n+2)
gate (n+2)
(common C)
p(n+2,m)
p(n+2, m+1)
p(n+2, m+2)
common (n+3)
gate (n+3)
(common D)
p(n,m)
p(n,m+1)
p(n,m+2)

Fig. 16

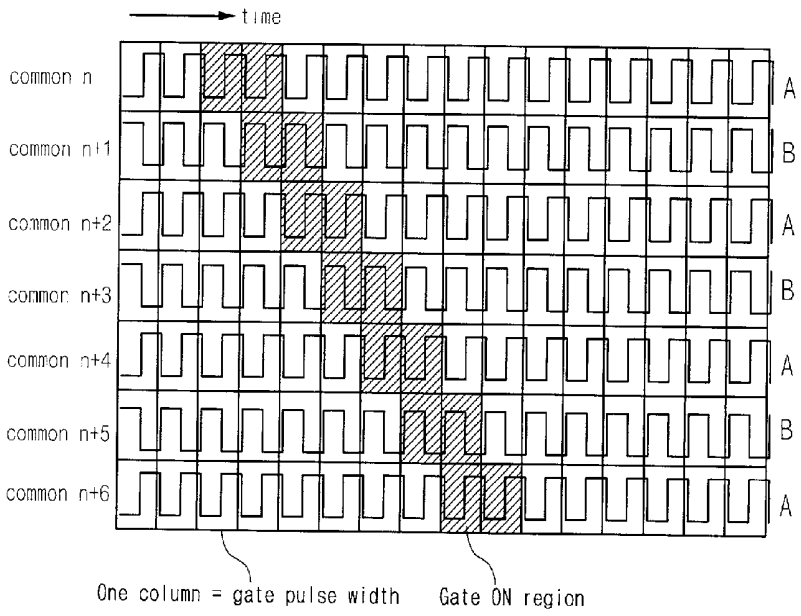

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
common n+6
A
B
A
B
A
B
A
One column = gate pulse width
Gate ON region

Fig. 17

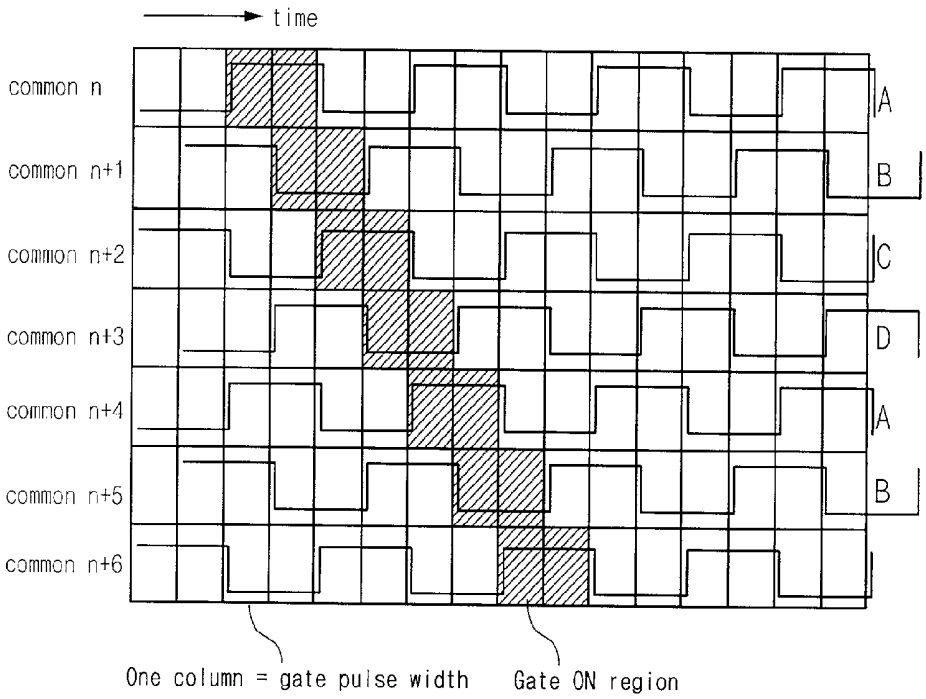

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
common n+6
A
B
C
D
A
B
One column = gate pulse width
Gate ON region

Fig. 18

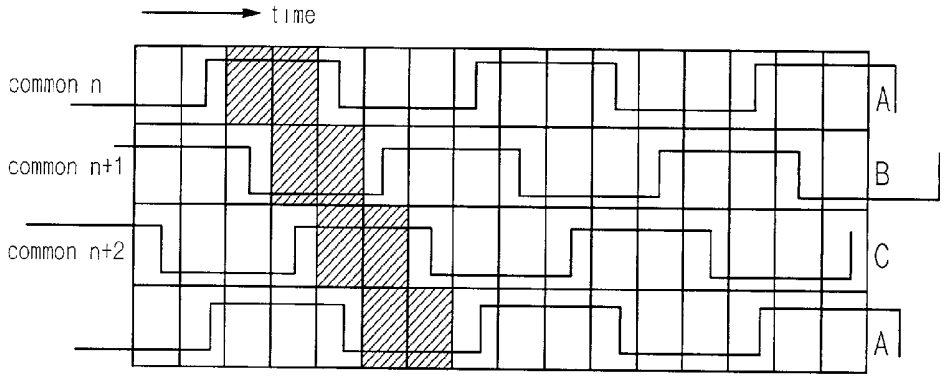

time
common n
common n+1
common n+2
A
B
C
A

Fig. 19

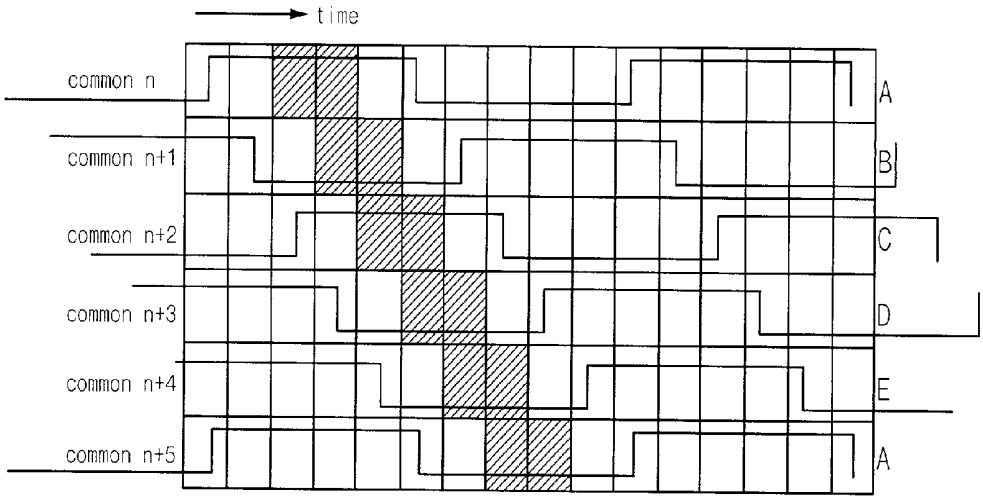

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
A
B
C
D
E
A

Fig. 20

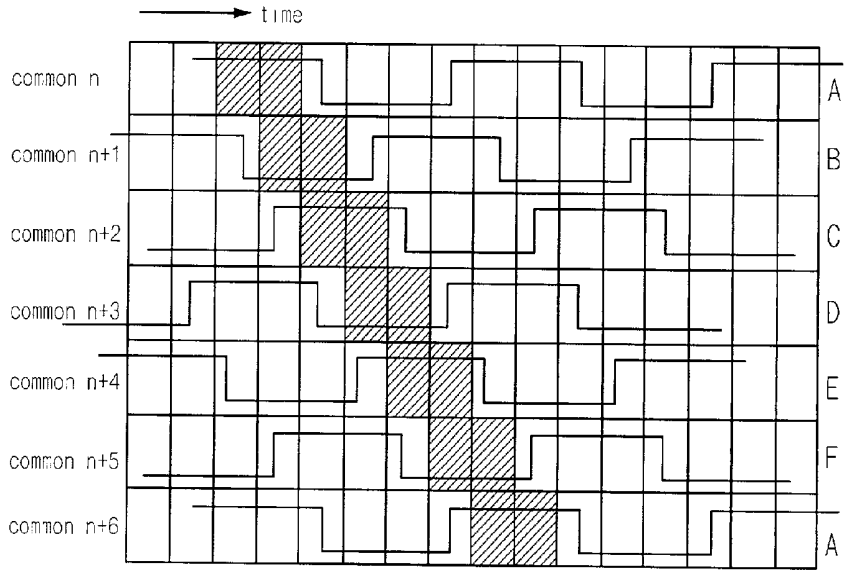
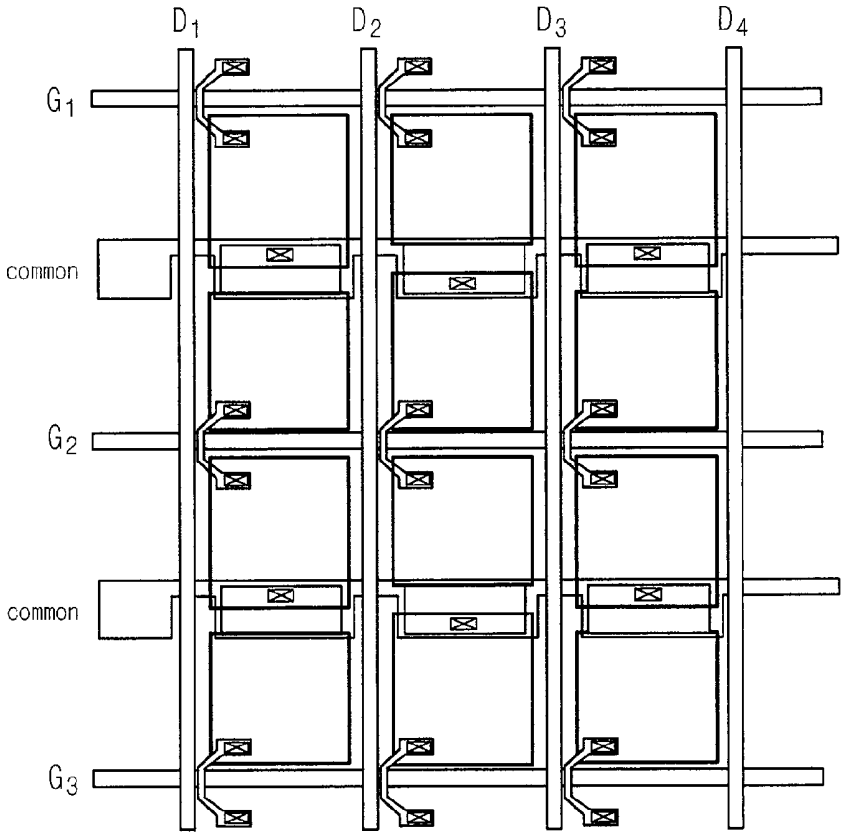

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
common n+6
A
B
C
D
E
F
A

Fig. 21



LIQUID CRYSTAL DISPLAY USING SWING COMMON ELECTRODE AND A METHOD FOR DRIVING THE SAME

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to a liquid crystal display and a method for driving the same and, more particularly, to a liquid crystal display achieving a quick response speed based on the overshoot generated through swinging common electrode voltages in tune with gate pulses.

[0003] (b) Description of the Related Art

[0004] Pursuant to the requirements by the consumers for thin and lightweight display devices, a liquid crystal display as a flat panel display has been currently used in a most extensive manner in lieu of cathode ray tubes (CRTs). Such a liquid crystal display basically has two glass substrates with electrodes for generating electric fields, and a liquid crystal layer sandwiched between the substrates. When voltages are applied to the electrodes, the liquid crystal molecules are rearranged to control light transmission.

[0005] One of the substrates is provided with an array of thin film transistors (TFTs) for switching voltages applied to the electrodes, and the other is provided with a common electrode and color filters. The former is usually called the "TFT array substrate", and the latter called the "color filter substrate."

[0006] **FIG. 1** illustrates a pixel equivalent circuit of a typical TFT LCD. In the TFT LCD, each pixel includes a TFT switching circuit where a source terminal and a gate terminal are connected to a data line and a gate line, a liquid crystal capacitor C_{lc} and a storage capacitor C_{st} each connected to a drain terminal of the TFT switching circuit, a first parasitic capacitor C_{gd} formed between the gate terminal and the drain terminal, a second parasitic capacitor C_{ds} formed between the drain terminal and the source terminal, and an overlap capacitor C_{over} formed between the data line and a pixel electrode.

[0007] The way of driving the liquid crystal disposed between the pixel electrodes V_p of the TFT array substrate and the common electrode V_{com} of the color filter substrate will be briefly explained.

[0008] When the TFT switching circuit receives a positive pulse through the gate line, it becomes to be in a state of turn on. At this time, a signal voltage is applied to the source electrode of the TFT switching circuit through the signal line, and transmitted to the liquid crystal capacitor C_{lc} and the storage capacitor C_{st} through the drain. The signal voltage is applied to the liquid crystal capacitor C_{lc} even after the gate voltage turns off. However, a pixel voltage shifts its voltage level shift to a certain degree because of the first parasitic capacitance C_{gd} formed between the gate and the drain.

[0009] When it is intended to use the above-structured LCD in a large display, the response speed. In order to enhance the response speed, Matsushita company of Japan proposes to improve the currently used capacitive coupled driving (CCD) technique.

[0010] **FIG. 2** illustrates the effects of a usual CCD technique. As shown in **FIG. 2**, the direction of making overshoot and undershoot with repect to the pixel is determined depending upon the property of the liquid crystal. When a pulse is applied to the common electrode COM, the amount of capacitive coupling is turned out to be greater in the direction of the pulse at the liquid crystal with a lower dielectric constant. The pulse of voltage down and votage up is applied to the common electrode COM in the case of being inverted from plus (+) to minus (−), and the pulse of voltage up and voltage down is applied thereto in the case of being inverted from minus (−) to plus (+). In the normally white mode, when a high gray level becomes to be a low gray level, or a low gray level becomes to be a high gray level, undershoot or overshoot that is lower or higher than the desired normal state of voltage occurs at the liquid crystal so that the liquid crystal molecules are rotated more rapidly.

[0011] **FIG. 3** illustrates a pixel equivalent circuit of the TFT LCD using previous gates proposed by Matsushita company, and **FIG. 4** illustrates the response speed characteristic of the TFT LCD shown in **FIG. 3**.

[0012] In the pixel equivalent circuit, one end of the storage capacitor C_{st} is connected to the drain, and the other end is connected to a previous gate.

[0013] In operation, the average voltage Vp applied to the pixel under the application of is a gate pulse is calculated using the following equation 1:

$$V_p = \pm V_s + (C_{st}/(C_{st}+C_{gd}+C_{lc})) \cdot \Delta V_g \quad (1)$$

[0014] where V_s indicates the voltage applied to the source terminal, C_{st} indicates the capacitance of the storage capacitor, C_{gd} is the parasitic capacitance between the gate terminal and the drain terminal, C_{lc} is the capacitance of the liquid crystal capacitor, and Δ_g is the difference between the previous gate voltage and the present gate voltage.

[0015] However, the technique of using previous gates increases the gate load. Furthermore, the technique can be employed only for the line inversion driving method and the cross talk or flickermakes it difficult to be used for high resolution wide screen LCDs.

[0016] Furthermore, the currently available gate tap IC cannot be used with such a technique. When the gate voltage is over-heightened at the off state, the off current (I_{off}) increases, making it difficult to change the gate value.

[0017] As described above, the use of previous gate signals as well as the two stepped gate signal application serves to enhance the response speed, but may not be applied to high resolution wide screen LCDs.

SUMMARY OF THE INVENTION

[0018] It is an object of the present invention to provide an LCD that uses swing common electrodes to enhance the response speed.

[0019] It is another object of the present invention to provide an LCD that uses swing common electrodes in the line inversion driving method to enhance the response speed.

[0020] It is still another object of the present invention to provide an LCD that uses swing common electrodes in the dot inversion driving method to enhance the response speed.

[0021] It is still another object of the present invention to provide a method for driving an LCD that uses swing common electrodes to enhance the response speed.

[0022] These and other objects may be achieved by a liquid crystal display bearing the following features.

[0023] According to one aspect of the present invention, the liquid crystal display sequentially applies signal voltages based on display data to target pixels to display picture images at respective frames. When pixels using swing common electrodes for storage capacitors are driven, voltages applied to the common electrodes are terminated with minus (−) during the period of gate on in case the pixel voltages are inverted from minus (−) to plus (+). In contrast, in case the pixel voltage is inverted from plus (+) to minus (−), the voltages applied to the common electrodes are terminated with plus (+). After the gates turn off, the voltages applied to the common electrodes are repeatedly swung from minus (−) to plus (+).

[0024] According to another aspect of the present invention, the liquid crystal display includes a timing signal control unit outputting data driver driving signals and gate driver driving signals. The timing signal control unit also outputs first signals for defining the cycle and amplitude of common voltages depending upon vertical synchronization signals, horizontal synchronization signals, and main clock signals applied from the outside.

[0025] A data driver outputs data driving voltages for driving polarities of a liquid crystal capacitor on the basis of the data driver driving signals.

[0026] A gate driver ouputs gate driving voltages on the basis of the gate driver driving signals.

[0027] A driving voltage generation unit makes the voltage level of the first signals to go up or down upon receipt of the first signals, and outputs swing common voltages in tune with the gate driving voltages at a predetermined cycle.

[0028] A liquid crystal display panel has one or more gate lines carrying scanning signals, one or more data lines crossing over the gate lines to carry picture signals, switching elements surrounded by the gate and data lines while being connected thereto, a liquid crystal capacitor transmitting light in proportion to the data driving voltages depending upon the turn on operations of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element and applying the stored data driving voltage to the liquid crystal capacitor at the turn off of the switching element.

[0029] The liquid crystal display panel is driven through line inversion such that the line at the present frame has a polarity inverted from the polarity of the line at the previous frame.

[0030] Alternatively, the liquid crystal display panel may be driven through dot inversion such that the dot at the present frame has a polarity inverted from the polarity of the dot at the previous frame.

[0031] In a method for driving the liquid crystal display, variations in pixel voltages depending upon gate on and off operations of the switching circuits are first checked. When it is checked at the (a) step that the pixel voltage is inverted from minus (−) to plus (+), a common voltage is output such that it is terminated with minus (−) during the period of gate on, and repeatedly swung from minus (−) to plus (+) during the period of gate off. In contrast, when it is checked at the (a) step that the pixel voltage is inverted from minus (−) to plus (+), a common voltage is output such that it is terminated with plus (+) during the period of gate on, and repeatedly swung from plus (+) to minus (−) during the period of gate off.

[0032] Consequently, the respective common electrode lines for the storage capacitors are periodically swung in tune with gate pulses to thereby generate overshoot. The response speed is enhanced due to the overshoot when the gray scale is altered due to the memory effect of the liquid crystal capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

[0034] **FIG. 1** is a circuit diagram of a typical TFT LCD;

[0035] **FIG. 2** illustrates the performance characteristics of the TFT LCD shown in **FIG. 1** under the application of a conventional CCD technique;

[0036] **FIG. 3** is a circuit diagram of a TFT LCD with the use of previous gate signals as proposed by Matsushita company;

[0037] **FIG. 4** is a waveform chart illustrating the response speed characteristic of the TFT LCD shown in **FIG. 3**;

[0038] **FIG. 5** is a waveform chart illustrating variations in pixel voltages due to periodical swing common voltages according to the present invention;

[0039] **FIG. 6** is a block diagram of an LCD using swing common electrodes according to a preferred embodiment of the present invention;

[0040] **FIG. 7** is a waveform chart illustrating the application of a single type of common electrodes for the line inversion driving in the LCD shown in **FIG. 6**;

[0041] **FIG. 8** is a waveform diagram illustrating the application of multiple types of common electrodes for the line inversion driving in the LCD shown in **FIG. 6**;

[0042] **FIG. 9** illustrates a pixel arrangement for the dot inversion driving in an LCD according to a prior art;

[0043] **FIG. 10** illustrates a double-lined common electrode structure for the dot inversion driving in the LCD shown in **FIG. 6**;

[0044] **FIG. 11** is a circuit diagram illustrating a pixel equivalent circuit of the LCD shown in **FIG. 10**;

[0045] **FIG. 12** is a waveform chart illustrating waveforms of common voltages applied to the double-structured common electrode lines shown in **FIG. 10**;

[0046] **FIG. 13** is a waveform chart further illustrating waveforms of common voltages applied to the double-structured common electrode lines shown in **FIG. 10**;

[0047] **FIG. 14** illustrates an arrangement of common electrodes at the source/drain regions of the LCD shown in **FIG. 6**;

[0048] **FIG. 15** illustrates an arrangement of a signal type of common electrodes for the dot inversion driving in the LCD shown in **FIG. 6**;

[0049] **FIG. 16** is a waveform chart illustrating two types of common voltage signals applied to the common electrode lines shown in **FIG. 15**;

[0050] **FIG. 17** is a waveform chart illustrating four types of common voltage signals applied to the common electrode lines shown in **FIG. 15**;

[0051] **FIG. 18** is a waveform chart illustrating three types of common voltage signals applied to the common electrode lines shown in **FIG. 15**;

[0052] **FIG. 19** is a waveform chart illustrating five types of common voltage signals applied to the common electrode lines shown in **FIG. 15**;

[0053] **FIG. 20** is a waveform chart illustrating six types of common voltage signals applied to the common electrode lines shown in **FIG. 14**; and

[0054] **FIG. 21** illustrates a separation type pixel structure for the dot inversion driving in the LCD shown in **FIG. 6**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0055] Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

[0056] **FIG. 5** is a waveform chart illustrating variations in pixel voltages due to periodical swing common voltages according to the present invention.

[0057] As shown in **FIG. 5**, the voltages applied to a pixel are swung through swinging the common voltages. The average pixel voltage Vp can be given by the following equation 2:

$$V_p=\pm V_s+(C_{st}/2(C_{st}+C_{gd}+Cc))\cdot\Delta V_{com} \quad (2)$$

[0058] where V_s indicates the voltage applied to the source terminal, C_{st} indicates the capacitance of the storage capacitor, C_{gd} is the parasitic capacitance between the gate terminal and the drain terminal, C_{lc} is the capacitance of the liquid crystal capacitor, and ΔV_{com} is the difference between the previous common voltage V_{com} and the present common voltage V_{com}.

[0059] The voltage additionally applied to the common electrode is proportional to the value of $C_{st}/(C_{st}+C_{lc})$. Therefore, when the gray scale is altered due to the memory effect of the liquid crystal capacitor C_{lc}, it generates overshoot to enhance the response speed of the liquid crystal.

[0060] For such a purpose, the following conditions should be all satisfied: (a) when the pixel voltage is inverted from minus (−) to plus (+), the common voltage is terminated with minus (−) during the period of gate on; (b) when the pixel voltage is inverted from plus (+) to minus (−), the common voltage is terminated with plus (+) during the period of gate on; and (c) when the gate is in an off state, minus (−) and plus (+) are repeatedly swung.

[0061] Various techniques of driving an LCD satisfying all of the above conditions will be now described in detail.

[0062] **FIG. 6** is a block diagram of an LCD using swing common electrodes according to a preferred embodiment of the present invention.

[0063] As shown in **FIG. 6**, the LCD includes a timing control unit **100**, a data driver **200**, a gate driver **300**, a driving voltage generation unit **400**, and an LCD panel **500**.

[0064] The timing control unit **100** outputs data driver driving signals (LOAD, Hstart, R, G, and B), and gate driver driving signals (Gate Clk, and Vstart). The timing control unit **100** also outputs first signals to the driving voltage generation unit **400** to define the cycle and amplitude of the common voltage V_{com} depending upon vertical synchronization signals Vsync, horizontal synchronization signals Hsync, and main clock signals MCLK applied from the outside.

[0065] The data driver **200** outputs data driving voltages (D1, D2, . . . , Dm) to data lines of the LCD panel **500** to drive polarities of the liquid crystal capacitor Clc on the basis of the data driver driving signals (LOAD, Hstart, R, G, and B).

[0066] The gate driver **300** ouputs gate driving voltages (G1, G2, . . . , Gn) to gate lines of the LCD panel **500** on the basis of the gate driver driving signals (Gate Clk, and Vstart) received from the timing control unit **100**, and the signals of Von and Voff received from the driving voltage generation unit **400**.

[0067] The driving voltage generation unit **400** makes the voltage level of the first signals to go up or down upon receipt of the first signals defining the cycle and amplitude of the common voltage, and outputs swing common voltages V_{com} in synchronization with the gate driving voltages at a predetermined cycle.

[0068] The LCD panel **500** includes one or more gate lines carrying scanning signals, one or more data lines carrying picture signals, switching elements TFTs surrounded by the gate lines and the data lines and connected thereto, a liquid crystal capacitor C_{lc} transmitting the light received from a backlight in proportion to the data driving voltages depending upon the state of the switching elements, and storage capacitors Cst storing the data driving voltage the switching element is turned on, and applying the stored data driving voltage to the liquid crystal capacitor Clc when the switching element is turned off.

[0069] In short, the common voltages output from the driving voltage generation unit **400** are applied to common electrode lines horizonally or vertically arranged at the LCD panel **500** while generating overshoot, which enhances the response speed of the liquid crystal.

[0070] **FIG. 7** is a waveform chart illustrating variations in common voltages V_{com} when a single type of common electrodes is used for the line inversion driving.

[0071] As shown in **FIG. 7**, when the odd-numbered (n−1)th or (n+1)th line is driven under the application of a gate pulse, first common voltages are output with the same width as that of the gate pulse. In contrast, when the

even-numbered nth line is driven under the application of a gate pulse, second common voltages are output with the same width as that of the gate pulse.

[0072] That is, the common voltage is terminated with minus (−) at the nth line where minus (−) is inverted into plus (+), and this satisfies the condition (a). In contrast, the common voltage is terminated with plus (+) at the (n−1)th or (n+1)th line where plus (+) is inverted into minus (−), and this satisfies the condition (b). The common voltages are periodically swung at the state of gate off, and this satisfies the condition (c).

[0073] Since the voltages at the respective lines are outlined in the same shape, the voltages required for generating overshoot can be applied only with one kind of common electrodes.

[0074] In short, when the line inversion driving is initiated under the application of a gate pulse, a single type of common voltages that have the same width as that of the gate pulse with a inverted polarity can be used for the driving. In this way, the response speed of the liquid crystal can be enhanced while satisfying all of the three conditions (a), (b) and (c) in a simultaneous manner.

[0075] **FIG. 8** is a waveform chart illustrating variations in common voltages V_{com} with the use of three types of common electrodes for the line inversion driving.

[0076] As shown in **FIG. 8**, when the (n)th line is driven by a gate pulse, common voltages of a first type having a pulse width three times than that of the gate pulse are output. When the (n+1)th line is driven by a gate pulse, common voltages of a second polarity having a pulse width three times longer than that of the gate pulse are output. When the (n+2)th line is driven by a gate pulse, common voltages of a third type having a pulse width three times longer than that of the gate pulse are output.

[0077] The common voltage is terminated with minus (−) at the (n)th or (n+2)th line where the pixel voltage is inverted from minus (−) into plus (+), and this satisfies the condition (a). In contrast, during the gate on period, the common voltage is terminated with plus (+) at the (n+1)th or (n+3)th line where plus (+) the pixel voltage is inverted from minus (−), and this satisfies the condition (b). The common voltages are periodically swung at the gate off state, and this satisfies the condition (c).

[0078] In short, three types of common electrodes A, B and C are used to enhance the response speed of the liquid crystal in the line inversion driving. In the common electrodes A, the same common voltage is applied to the group of (n)th, (n+3)th, (n+6)th, and (n+9)th lines. Likewise in the common electrodes B, the same common voltage is applied to the group of (n+1)th, (n+4)th, and (n+7)th lines. In the common electrodes C, the same common voltage is applied to the group of (n+2)th, (n+5)th, and (n+8)th lines.

[0079] In this way, various types (four, five, six, etc.) of common electrodes can be used to drive the LCD panel based on the line inversion driving. The advantage of such a technique is that the frequency for swinging the common electrode can be lowered. For instance, it solves the problem of the increased power consumption occuring when the voltages are applied to the common electrode more frequently.

[0080] A technique of enhancing the response speed of the liquid crystal in a dot inversion driving method will be now described in detail.

[0081] In order to apply the swinging common electrodes for the storage capacitors to the dot inversion driving, several aspects has to be considered.

[0082] **FIG. 9** illustrates a pixel arrangement for the dot inversion driving in a conventional LCD.

[0083] In the dot inversion driving with the conventional LCDs, plus (+) and minus (−) polarities are co-existent at one line simultaneously. Therefore, when the gate opens, at least two types of common electrodes should be present at one line. However, as shown in **FIG. 9**, in the pixel arrangement for the conventional dot inversion driving, a single type of common electrodes cannot generate the desired overshoot.

[0084] **FIG. 10** illustrates a double-structured common electrode lines for the dot inversion driving in the LCD shown in **FIG. 6**. **FIG. 11** illustrates a pixel equivalent circuit of the LCD shown in **FIG. 10**.

[0085] As shown in **FIG. 10**, first and second common electrode lines A and B are arranged between the neighboring gate lines in the horizontal direction. The first common electrode line A is connected to odd-numbered (or even-numbered) pixel electrodes, and the second common electrode line B is connected to even-numbered (or odd-numbered) pixel electrodes.

[0086] In the above structure, the pixels connected to the same data line Vs are connected to the same common electrode line while being arranged in the vertical direction.

[0087] **FIG. 12** is a waveform chart illustrating variations in the common voltages V_{com} applied to the double-structured common electrode lines shown in **FIG. 10**.

[0088] As shown in **FIG. 12**, when the odd-numbered line (or the even-numbered line) is driven by a gate pulse, a first common voltage is output to the first common electrode line. In contrast, when the even-numbered line (or the odd-numbered line) is driven by a gate pulse, a second common voltage inverted in polarity with respect to the first common voltage is output to the first common electrode line with the same width as that of the gate pulse.

[0089] Furthermore, when the odd-numbered line (or the even-numbered line) is driven by a gate pulse, the second common voltage inverted in polarity with respect to the first common voltage is output to the second common electrode line with the same width as that of the gate pulse. In contrast, when the even-numbered line (or the odd-numbered line) is driven under the application of a gate pulse, the first common voltage is output to the second common electrode line with the same width as that of the gate pulse.

[0090] That is, the technique of driving each of the common voltages A or B is the same as that of driving the single type of common voltages for the line inversion driving described with reference to **FIG. 6**.

[0091] **FIG. 13** is a waveform chart illustrating the waveforms of common voltages applied to the double-structured common electrode lines shown in **FIG. 10**.

[0092] As shown in **FIG. 13**, the first common voltages A are divided into three types of common voltages A-**1**, A-**2** and A-**3**, and the second common voltages B are also divided into three types of common voltages B-**1**, B-**2** and B-**3**. Whenever the frames are changed, the first and second common voltages A and B are alternated.

[0093] It is also possible that the common voltages are further divided into a plurality of numbers (eight, ten, etc.) of common voltages to lower the frequency of voltage waveforms applied to the common electrodes.

[0094] **FIG. 14** illustrates common electrodes formed at source/drain (S/D) regions of the LCD shown in **FIG. 6**.

[0095] As shown in **FIG. 14**, first and second common electrode lines are provided between the data lines proceeding in the vertical direction. The first common electrode lines are arranged at the odd-numbered vertical columns, and the second common electrode lines are arranged at the even-numbered horizontal columns.

[0096] First and second storage capacitors A and B are formed on the first and second common electrode lines at the crossed area of the gate and data lines with a predetermined volume. The volume of the first and second storage capacitors A and B is so large as to compensate for the leakage of current due to the liquid crystal capacitor when the gate pulse is in an off state.

[0097] The technique of driving the common voltage signals is the same as that described with reference to FIGS. **12** or **13**.

[0098] **FIG. 15** illustrates the structure of a single type of common electrode lines for the dot inversion driving in the LCD shown in **FIG. 6**.

[0099] As shown in **FIG. 15**, odd-numbered and even-numbered common electrode lines are arranged in the horizontal direction. Odd-numbered gate lines are arranged in the horizontal direction such that they are positioned close to the odd-numbered common electrode lines.

[0100] Furthermore, even-numbered gate lines are arranged in the horizontal direction such that they are positioned close to the even-numbered common electrode lines. Odd-numbered and even-numbered data lines are arranged in the vertical direction.

[0101] First storage capacitors are formed at the regions partitioned by the odd-numbered data lines and the even-numbered data lines while interconnecting the odd-numbered common electrode lines and the odd numbered gate lines close thereto.

[0102] Furthermore, the first storage capacitors are also formed at the regions partitioned by the odd-numbered data lines and the even-numbered data lines while interconnecting the even-numbered common electrode lines and the even-numbered gate lines close thereto.

[0103] Second storage capacitors are formed at the regions partitioned by the even-numbered data lines and the odd-numbered data lines while interconnecting the even-numbered common electrode lines and the odd numbered gate lines.

[0104] Furthermore, the second storage capacitors are also formed at the regions partitioned by the even-numbered data lines and the odd-numbered data lines while interconnecting the odd-numbered common electrode lines and the even-numbered gate lines.

[0105] **FIG. 16** is a waveform chart illustrating two types of common voltage signals applied to the common electrode lines shown in **FIG. 15**.

[0106] As shown in **FIG. 16**, the vertical axis indicates the common electrode lines, and time passes by in the horizontal direction. One column in the horizontal direction has the same width as that of the gate pulse. The gate opens at the deviant lined region covering two columns at each row. The deviant lined two columns at each row are present because each pixel connected to the common electrode ranges over the two upper and lower lines centering the common electrode. That is, one common electrode ranges over a half of the upper line and a half of the lower line.

[0107] The (n)th, (n+2)th, (n+4)th, and (n+6)th common electrode lines are terminated with plus (+) while covering the pixels where plus (+) is inverted into minus (−). In contrast, the (n+1)th, (n+3)th, (n+5)th common electrode lines cover the pixels where minus (−) is inverted into plus (+).

[0108] The (n)th, (n+2)th, (n+4)th, and (n+6)th common electrode lines bear the same signals, and the (n+1)th, (n+3)th, (n+5)th common electrode lines bear the same signals.

[0109] Therefore, in the above driving technique, signals are applied to the odd-numbered lines and the even-numbered lines while being inverted from each other.

[0110] **FIG. 17** illustrates four types of common voltage signals applied to the common electrode lines shown in **FIG. 15**.

[0111] As shown in **FIG. 17**, the frequency of the common electrode line is a half of that of the data line. When one frame passes by, the signals of A and C are inverted from each other, and those of B and D are inverted from each other.

[0112] In the above driving technique, the driving can be made with a number of signals.

[0113] **FIG. 18** is a waveform chart illustrating three types of common voltage signals applied to the common electrode lines shown in **FIG. 15**. **FIG. 19** is a waveform chart illustrating five types of common voltage signals applied to the common electrode lines shown in **FIG. 15**, and **FIG. 20** is a waveform chart illustrating six types of common voltage signals applied to the common electrode lines shown in **FIG. 15**.

[0114] As shown in the drawings, the odd-numbered signals have a wavelength longer than those of others.

[0115] **FIG. 21** illustrates a separation type pixel structure for the dot inversion driving in the LCD shown in **FIG. 6**.

[0116] As shown in **FIG. 21**, common electrode lines are arranged in the horizontal direction interposed between neighboring gate lines.

[0117] First pixels are formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as odd-numbered data lines and even-numbered data lines. One end of each pixel is connected to the

corresponding odd-numbered gate line, and the opposite end thereof connected to the corresponding common electrode line.

[0118] Second pixels are formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the odd-numbered data lines and the even-numbered data lines. One end of each pixel is connected to the corresponding even-numbered gate line.

[0119] Third pixels are formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the even-numbered data lines and the odd-numbered data lines. One end of each pixel is connected to the corresponding odd-numbered gate line.

[0120] Finally, fourth pixels are formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the even-numbered data lines and the odd-numbered data lines. One end of each pixel is connected to the corresponding common electrode line, and the opposite end connected to the corresponding even-numbered gate line.

[0121] In short, in order to drive the LCD based on the dot inversion driving, pixels are partitioned centering around the gate lines. Since the gate lines are spaced apart from the common electrode lines with a predetermined distance, device failure due to line shorts can be prevented. The various techniques described with reference to FIGS. **16** to **20** can be also applied for the driving.

[0122] As described above, separate common electrode lines for storage capacitors are periodically swung in synchronization with gate pulses to thereby generate overshoot. Consequently, when the gray scales are altered due to the memory effect of the liquid crystal capacitor, the response speed of the liquid crystal can be enhaced with the overshoot.

[0123] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A liquid crystal display sequentially applying signal voltages based on display data to target pixels to display picture images at respective frames, comprising:

swing common electrodes for forming storage capacitors;

wherein voltages applied to said swing common electrodes are terminated with minus (−) during the period of gate on when the pixel voltages are inverted from minus (−) to plus (+), while being terminated with plus (+) when the pixel voltages are inverted from plus (+) to minus (−), and repeatedly swung from minus (−) to plus (+) after the gates turn off.

2. The liquid crystal display of claim 1, wherein an average pixel voltage V_p is given by following equation:

$$V_p=\pm V_s+(C_{st}/2(C_{st}+C_{gd}+C_{lc}))\cdot\Delta V_{com}$$

where V_s indicates voltage applied to a source terminal, C_{st} indicates capacitance of a storage capacitor, C_{gd} is parasitic capacitance between a gate terminal and a drain terminal, C_{lc} is capacitance of a liquid crystal capacitor, and ΔV_{com} is a difference between previous common voltage V_{com} and present common voltage V_{com}.

3. A liquid crystal display using swing common electrodes, comprising:

a timing signal control unit outputting a data driver driving signal and a gate driver driving signal, and also outputting first signals for defining cycle and amplitude of common voltages depending upon vertical synchronization signals, horizontal synchronization signals, and main clock signals applied from the outside;

a data driver outputting data driving voltages for driving polarities of a liquid crystal capacitor based on the data driver driving signal;

a gate driver ouputting gate driving voltages based on the gate driver driving signal;

a driving voltage generation unit making the voltage level of the first signals to go up or down upon receipt of the first signals, and outputting swing common voltages synchronized with the gate driving voltages at a predetermined cycle; and

a liquid crystal display panel having one or more gate lines carrying scanning signals, one or more data lines crossing over the gate lines to carry picture signals, switching elements surrounded by the gate and data lines while being connected thereto, a liquid crystal capacitor transmitting light in proportion to the data driving voltages depending upon the turn on operations of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element, and applying the stored data driving voltage to the liquid crystal capacitor at the turn off of the switching element;

wherein the liquid crystal display panel is driven through a line inversion method such that the line at the present frame has a polarity inverted from the polarity of the line at the previous frame.

4. The liquid crystal display of claim 3, wherein the driving voltage generation unit outputs common voltages, the common voltage being terminated with minus (−) during the period of gate on in case the pixel voltage is inverted from minus (−) to plus (+) while being terminated with plus (+) when the pixel voltage is inverted from plus (+) to minus (−), and repeatedly swung from minus (−) to plus (+) after the gate turns off.

5. The liquid crystal display of claim 1, wherein an average pixel voltage V_p is given by following equation:

$$V_p=\pm V_s+(C_{st}/2(C_{st}+C_{gd}+C_{lc}))\cdot\Delta V_{com}$$

where V_s indicates voltage applied to a source terminal, C_{st} indicates capacitance of a storage capacitor, C_{gd} is parasitic capacitance between a gate terminal and a drain terminal, C_{lc} is capacitance of the liquid crystal capacitor, and ΔV_{com} is a difference between previous common voltage V_{com} and present common voltage V_{com}.

6. The liquid crystal display of claim 3, wherein the driving voltage generation unit outputs a first common voltage with the same width as a gate pulse when an odd numbered line is driven under the application of the gate pulse, and outputs a second common voltage with the same

width as the gate pulse when an even-numbered line is driven under the application of the gate pulse.

7. The liquid crystal display of claim 3, wherein the driving voltage generation unit outputs a first common voltage with a pulse width k times longer than a gate pulse when the (n)th line is driven under the application of the gate pulse, outputs a second common voltage with a pulse width k times longer than the gate pulse when the (n+1)th line is driven under the application of the gate pulse, and outputs a third common voltage with a pulse width k times longer than the gate pulse when the (n+2)th line is driven under the application of the gate pulse.

8. A liquid crystal display using swing common electrodes, comprising:

a timing signal control unit outputting a data driver driving signal and a gate driver driving signal, and also outputting first signals for defining cycle and amplitude of common voltages depending upon vertical synchronization signals, horizontal synchronization signals, and main clock signals applied from the outside;

a data driver outputting data driving voltages for driving polarities of a liquid crystal capacitor based on the data driver driving signals;

a gate driver ouputting gate driving voltages based on the gate driver driving signals;

a driving voltage generation unit making the voltage level of the first signals to go up or down upon receipt of the first signals, and outputting swing common voltages synchronized with the gate driving voltages at a predetermined cycle; and

a liquid crystal display panel comprising one or more gate lines carrying scanning signals, one or more data lines crossing over the gate lines to carry picture signals, switching elements surrounded by the gate and data lines while being connected thereto, a liquid crystal capacitor transmitting light in proportion to the data driving voltages depending upon the turn on operations of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element, and applying the stored data driving voltage to the liquid crystal capacitor at the turn off of the switching element;

wherein the liquid crystal display panel is driven through a dot inversion method such that the dot at the present frame has a polarity inverted from the polarity of the dot at the previous frame.

9. The liquid crystal display of claim 8, wherein the driving voltage generation unit outputs common voltages, the common voltage being terminated with minus (−) during the period of gate on when pixel voltage is inverted from minus (−) to plus (+) while being terminated with plus (+) when pixel voltage is inverted from plus (+) to minus (−), and repeatedly swung from minus (−) to plus (+) after the gate turns off.

10. The liquid crystal display of claim 1, wherein an average pixel voltage V_p is given by following equation:

$$V_p=\pm V_s+(C_{st}/2(C_{st}+C_{gd}+C_{lc}))\cdot\Delta V_{com}$$

where V_s indicates voltage applied to a source terminal, C_{st} indicates capacitance of a storage capacitor, C_{gd} is parasitic capacitance between a gate terminal and a drain terminal, C_{lc} is capacitance of the liquid crystal capacitor, and ΔV_{com} is a difference between previous common voltage V_{com} and present common voltage V_{com}.

11. The liquid crystal display of claim 9, wherein the liquid crystal display panel further comprises a first common electrode line and a second common electrode line arranged between the neighboring gate lines in a horizontal direction, the first common electrode line connected to odd-numbered pixel electrodes, and the second common electrode line connected to even-numbered pixel electrodes.

12. The liquid crystal display of claim 11, wherein the driving voltage generation unit outputs a first common voltage with the same width as a gate pulse to the first common electrode line when the odd-numbered line is driven under the application of the gate pulse while outputting a second common voltage inverted in polarity against the first common voltage with the same width as the gate pulse to the first common electrode line when the even-numbered line is driven under the application of the gate pulse, and outputs the second common voltage inverted in polarity against the first common voltage to the second common electrode line with the same width as the gate pulse when the odd-numbered line is driven under the application of the gate pulse while outputting the first common voltage with the same width as the gate pulse when the even-numbered line is driven under the application of the gate pulse.

13. The liquid crystal display of claim 11, wherein the driving voltage generation unit outputs a first common voltage with a pulse width k times longer than the gate pulse to the first common electrode line and the second common electrode line when the (n)th line is driven under the application of the gate pulse, outputs a second common voltage with a pulse width k times longer than the gate pulse to the first common electrode line and the second common electrode line when the (n+1)th line is driven under the application of the gate pulse, and outputs a third common voltage with a pulse width k times longr than the gate pulse to the first common electrode line and the second common electrode line when the (n+2)th line is driven under the application of the gate pulse.

14. The liquid crystal display of claim 11, wherein the liquid crystal display panel further comprises first and second common electrode lines provided between the data lines, the first common electrode lines being arranged at the odd-numbered vertical columns, the second common electrode lines being arranged at the even-numbered horizontal columns, the first and the second common electrode lines each having a storage capacitor formed at the crossed area of the gate and data lines with a predetermined volume so large as to co-act with the the liquid crystal capacitor.

15. The liquid crystal display of claim 11, wherein the first common electrode line is odd-numbered and the second common electrode line is even-numbered, arranged in a horizontal direction,

odd-numbered gate lines arranged in the horizontal direction are positioned close to the odd-numbered common electrode lines,

even-numbered gate lines arranged in the horizontal direction are positioned close to the even-numbered common electrode lines;

odd-numbered data lines and even-numbered data lines are arranged in a vertical direction,

first storage capacitors are formed at the regions partitioned by the odd-numbered data lines and the even-numbered data lines while interconnecting the odd-numbered common electrode lines and the odd numbered gate lines close thereto, and

second storage capacitors are formed at the regions partitioned by the even-numbered data lines and the odd-numbered data lines while interconnecting the even-numbered common electrode lines and the odd numberedgate lines.

16. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with the same width as the width of a gate pulse to the odd-numbered common electrode lines under the application of the gate pulse, and outputs a common voltage of a second type with the same width as the width of a gate pulse to the even-numbered common electrode lines under the application of the gate pulse.

17. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width twice longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second type with a pulse width twice longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, outputs a common voltage of a third type with a pulse width twice longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a fourth type with a pulse width twice longer than the width of a gate pulse to the (n+3)th common electrode lines under the application of the gate pulse.

18. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width three times longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second polarity with a pulse width three times longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a third polarity with a pulse width three times longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse.

19. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width five times longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second type with a pulse width five times longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, outputs a common voltage of a third type with a pulse width five times longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse, outputs a common voltage of a fourth type with a pulse width five times longer than the gate pulse to the (n+3)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a fifth type with a pulse width five times longer than the gate pulse to the (n+4)th common electrode lines under the application of the gate pulse.

20. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width three times longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second type with a pulse width three times longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, outputs a common voltage of a third type with a pulse width three times longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse, outputs a common voltage of a fourth type with a pulse width three times longer than the gate pulse to the (n+3)th common electrode lines under the application of the gate pulse, outputs a common voltage of a fifth type with a pulse width three times longer than the gate pulse to the (n+4)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a sixth type with a pulse width three times longer than the gate pulse to the (n+5)th common electrode lines under the application of the gate pulse.

21. The liquid crystal display of claim 11, further comprising:

a first pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as odd-numbered data lines and even-numbered data lines, said first pixel electrode having one end connected to the corresponding odd-numbered gate line and the other end connected to the corresponding common electrode line;

a second pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the odd-numbered data lines and the even-numbered data lines, said second pixel electrode having one end connected to the corresponding even-numbered gate line and the other end connected to the corresponding common electrode line;

a third pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the even-numbered data lines and the odd-numbered data lines, said third pixel electrode having one end connected to the corresponding odd-numbered gate line and the other end connected to the corresponding common electrode line; and

a fourth pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the even-numbered data lines and the odd-numbered data lines, said fourth pixel electrode having one end connected to the corresponding common electrode line and the other end connected to the corresponding even-numbered gate line.

22. A method of driving a liquid crystal display, the liquid crystal display comprising a liquid crystal display panel having a gate line carrying scanning signals, a data line crossing over the gate lines to carry picture signals, a switching element **20** surrounded by the gate line and the data line while being connected thereto, a liquid crystal capacitor transmitting light in proportion to data driving voltages depending upon states of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element and applying the stored data driving voltage to the liquid crystal capacitor at the turn off of the switching element, the liquid crystal display being inversion-driven at each frame, the method comprising the steps of:

(a) checking variations in pixel voltages depending upon gate on and off operations of the switching circuits;

(b) outputting a common voltage terminated with minus (−) during a period of gate on while outputting a common voltage repeatedly swung from minus (−) to plus (+) during the period of gate off when the pixel voltage is inverted from minus (−) to plus (+) and

(c) outputting a common voltage terminated with plus (+) during a period of gate on while outputting a common voltage repeatedly swung from plus (+) to minus (−) during the period of gate off when the pixel voltage is inverted from plus (+) to minus (−)

* * * * *

专利名称(译)	使用摆动公共电极的液晶显示器及其驱动方法		
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[标]申请(专利权)人(译)	SONG JANG KUN CHOI JOON HOO		
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当前申请(专利权)人(译)	SONG JANG-KUN 崔俊HOO		
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摘要(译)

液晶显示器包括用于存储电容器的摆动公共电极，以基于显示数据顺序地将信号电压施加到目标像素，以在各个帧处显示图像。施加到公共电极的电压在栅极导通期间以负（-）终止，以防像素电压从负（-）反转为正（+），而在像素电压的情况下以正（+）结束。从加号（+）反转为减号（-）。在栅极关闭后，公共电压从负（-）到正（+）重复摆动。在这些条件下，用于存储电容器的各个公共电极线周期性地与栅极脉冲同步，从而产生过冲。当由于液晶电容器的记忆效应而改变灰度级时，由于过冲，液晶的响应速度增强。