



US 20010040665A1

(19) **United States**(12) **Patent Application Publication**  
**Ahn**(10) **Pub. No.: US 2001/0040665 A1**(43) **Pub. Date: Nov. 15, 2001**(54) **LIQUID CRYSTAL DISPLAY PANEL**(52) **U.S. Cl. .... 349/156**(76) **Inventor: Byung Chul Ahn, Kumi-shi (KR)**

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**MORGAN, LEWIS & BOCKIUS LLP****1800 M Street, N.W.****Washington, DC 20036 (US)**(21) **Appl. No.: 09/792,050**(22) **Filed: Feb. 26, 2001**(30) **Foreign Application Priority Data**

Feb. 25, 2000 (KR) ..... 2000-9502

**Publication Classification**(51) **Int. Cl.<sup>7</sup> ..... G02F 1/1339**(57) **ABSTRACT**

A liquid crystal display panel provided with a lower substrate and an upper substrate spaced from and facing to each other to have a gap therebetween. In the liquid crystal panel, a liquid crystal layer is positioned between the first and second substrate. The lower substrate has a thin film transistor formed thereon and a patterned spacer formed on the thin film transistor and supporting the second substrate. The thin film transistor has a semiconductor pattern, a source electrode and drain electrode. A portion of the semiconductor pattern is exposed between the source electrode and the drain electrode. The patterned spacer has an insulating layer on the bottom which is in contact with the exposed portion of the semiconductor pattern.

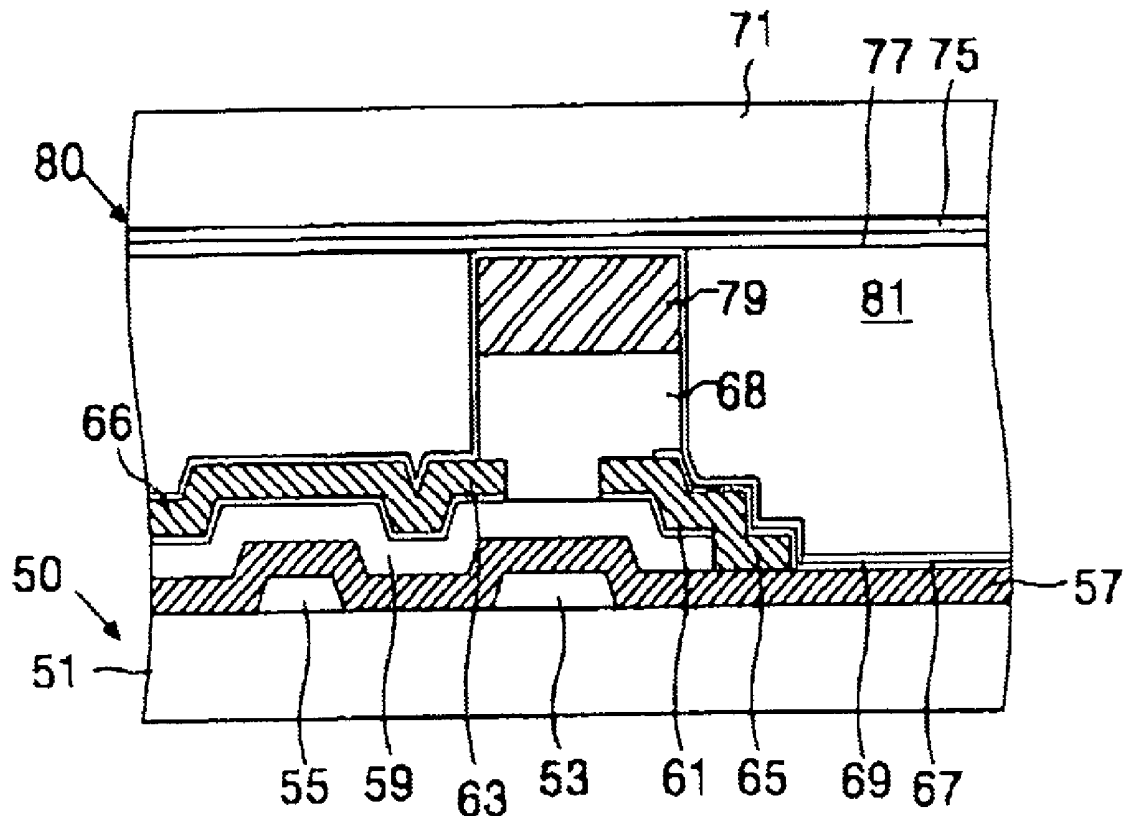


FIG. 1

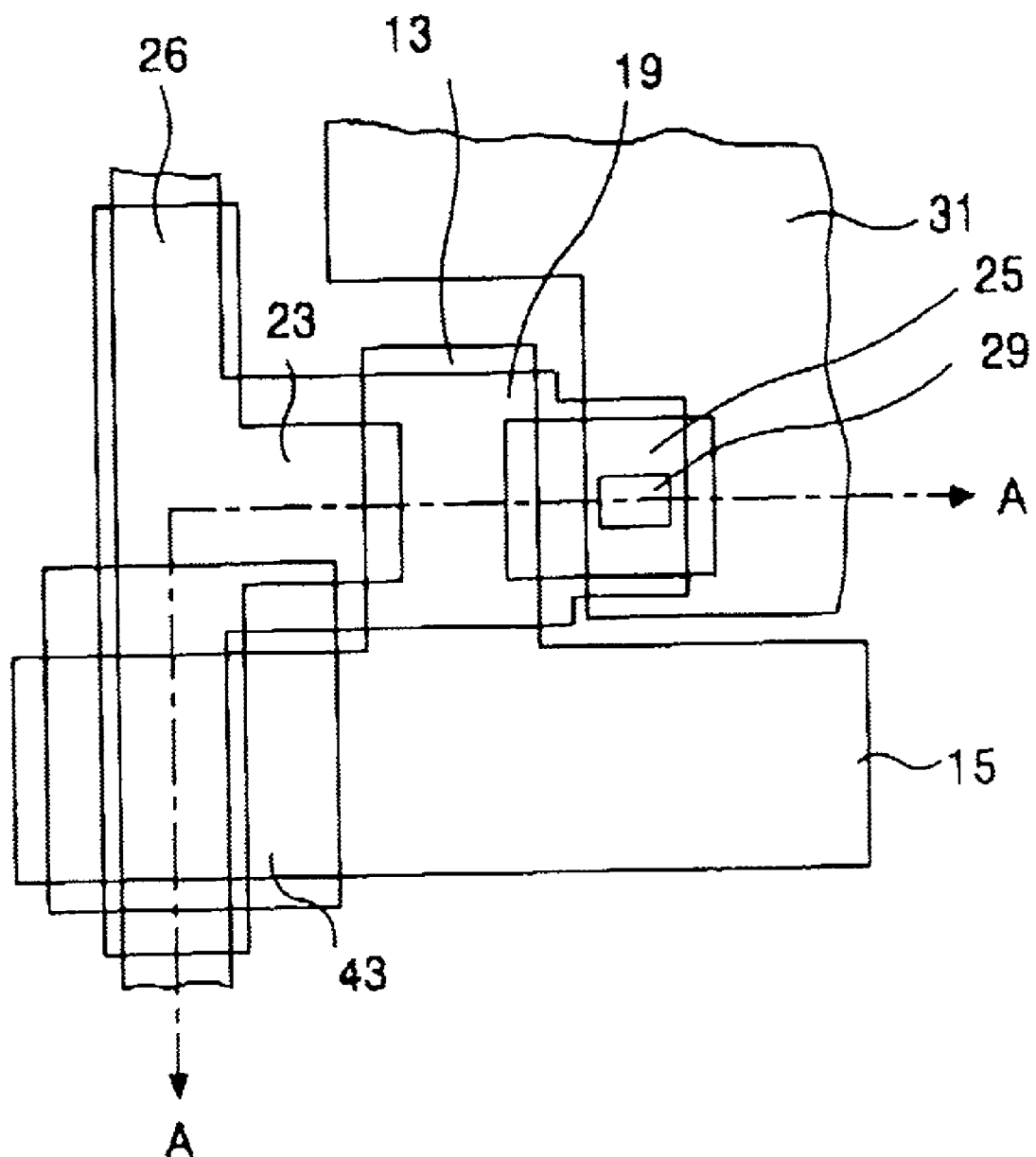


FIG. 2

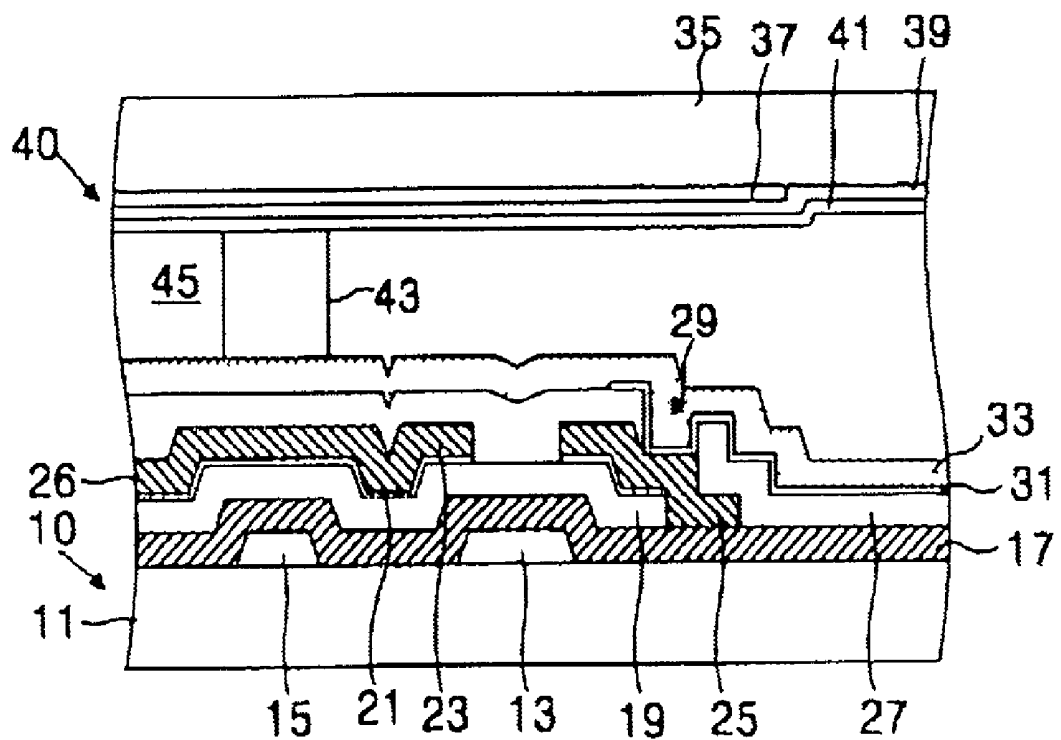


FIG. 3

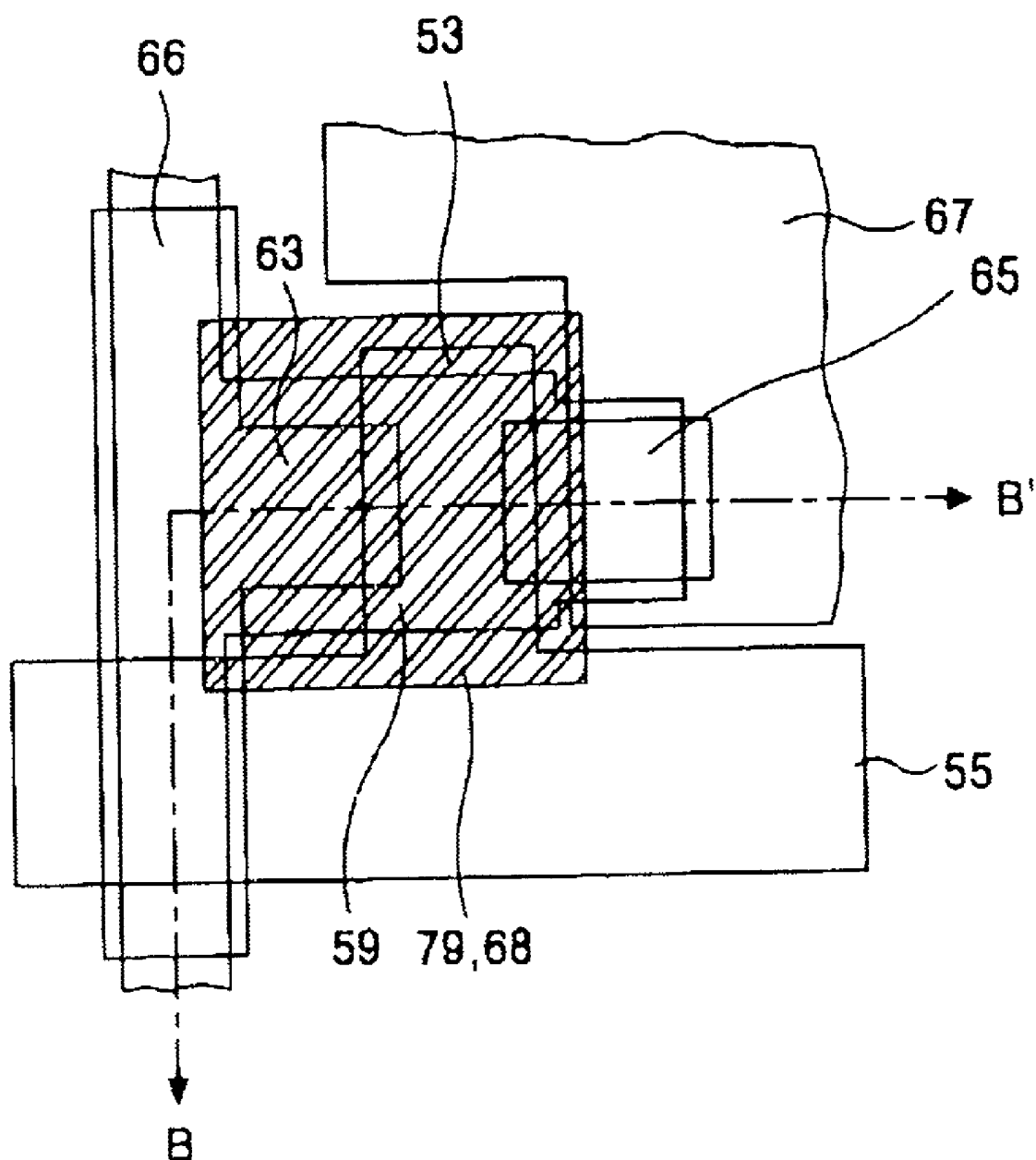


FIG. 4

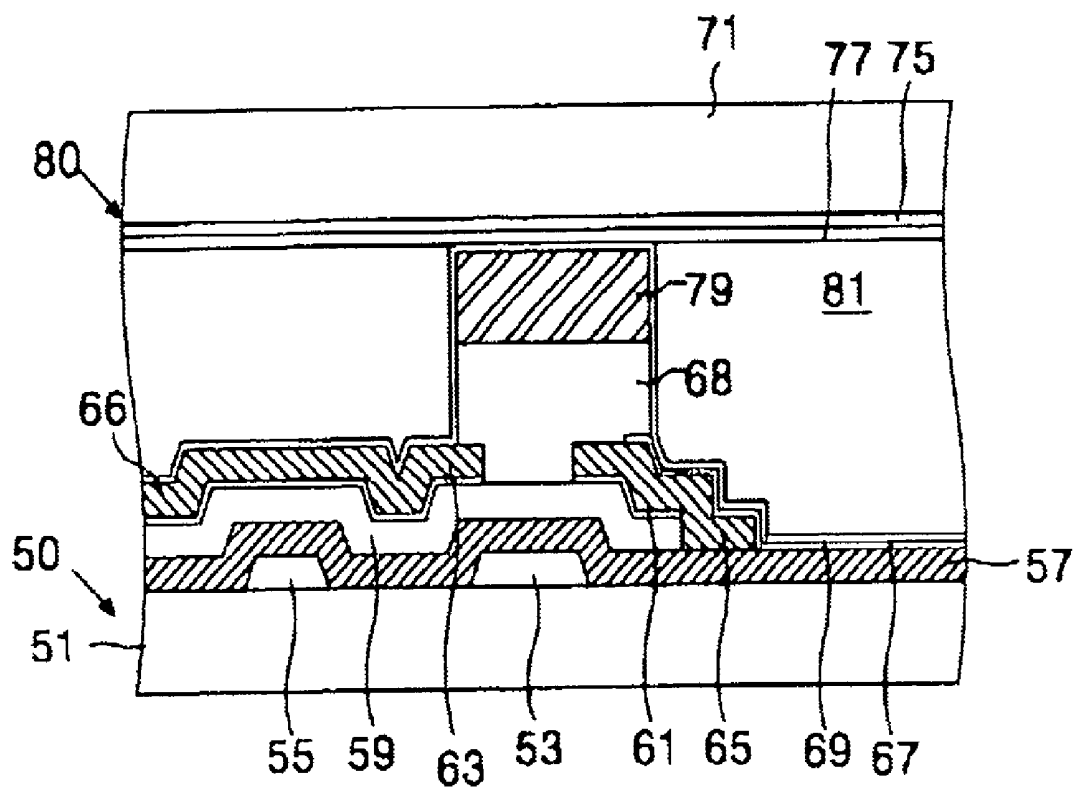


FIG. 5

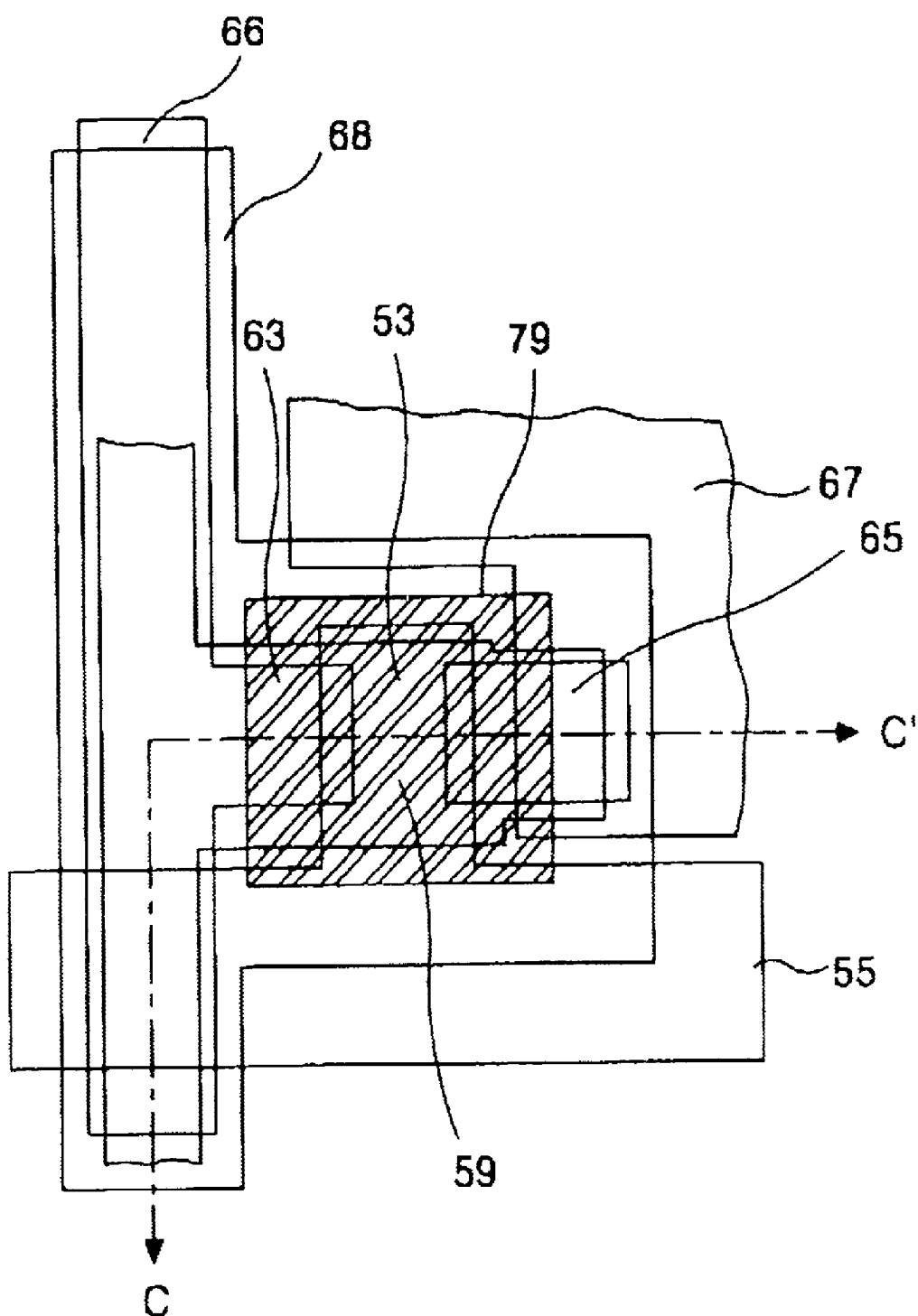


FIG. 6

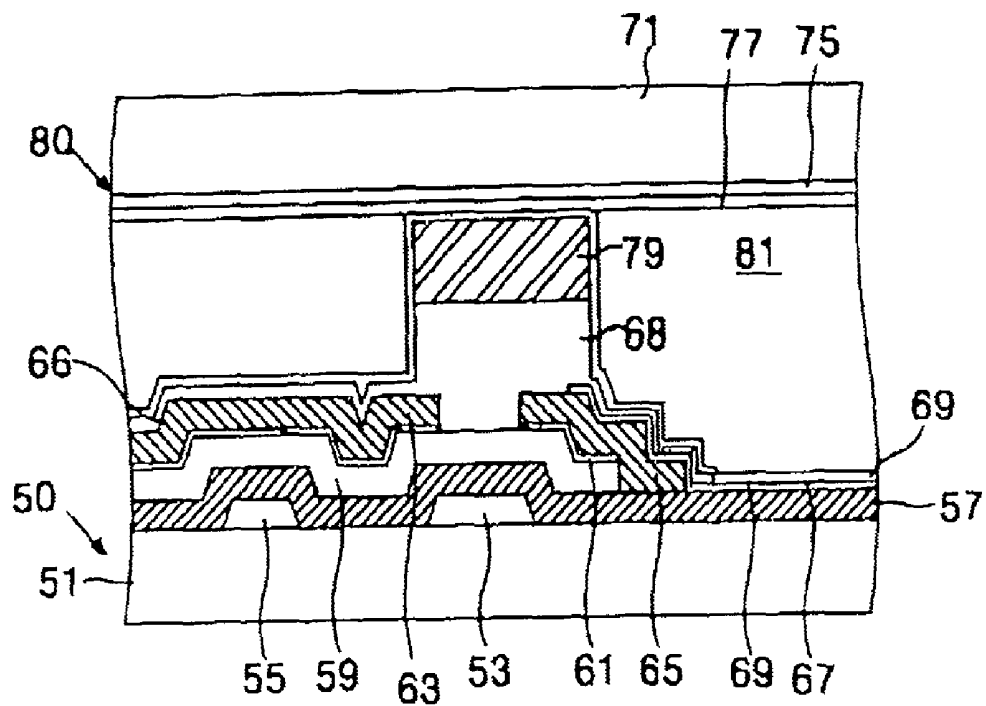


FIG. 7

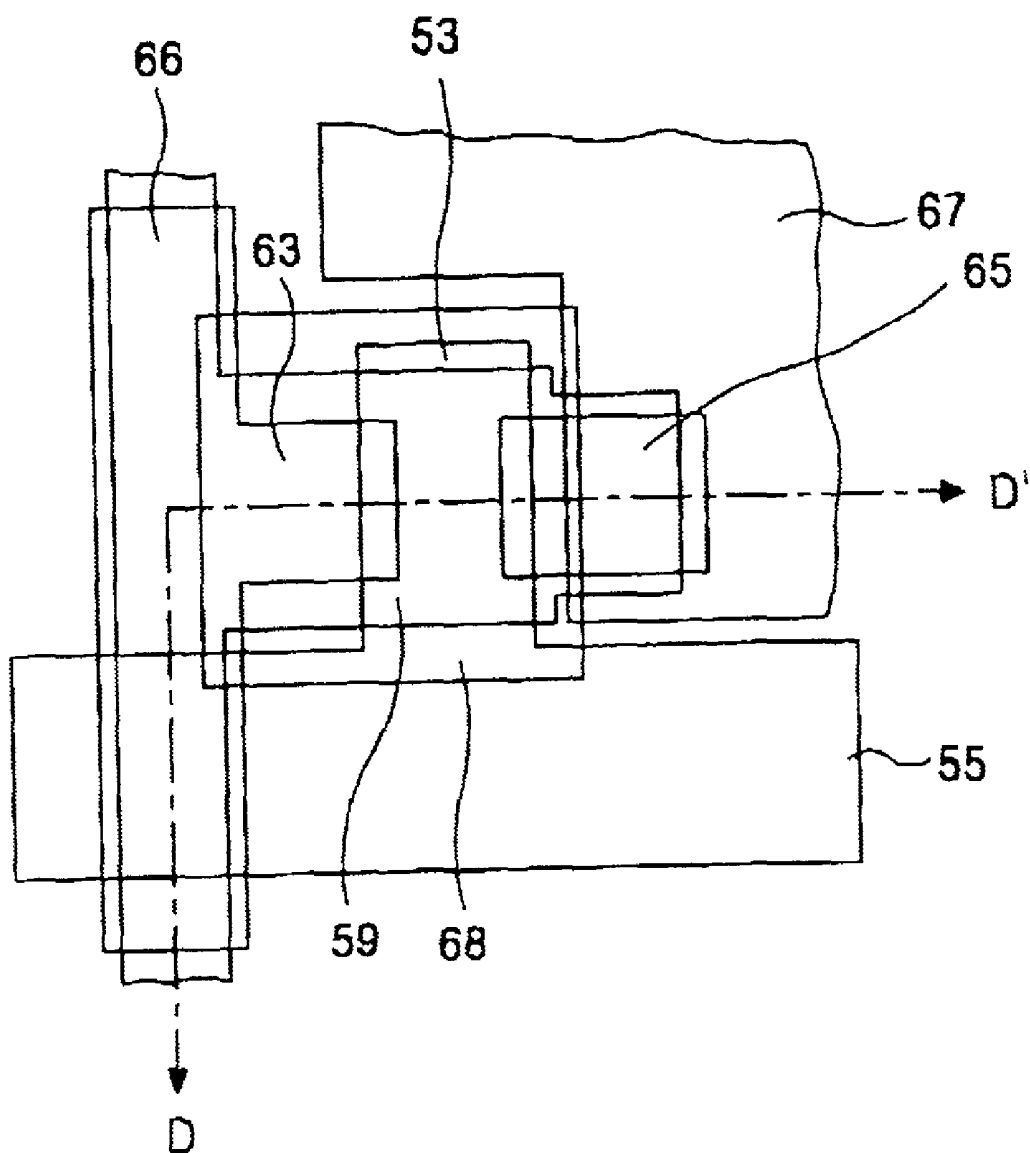




FIG. 8

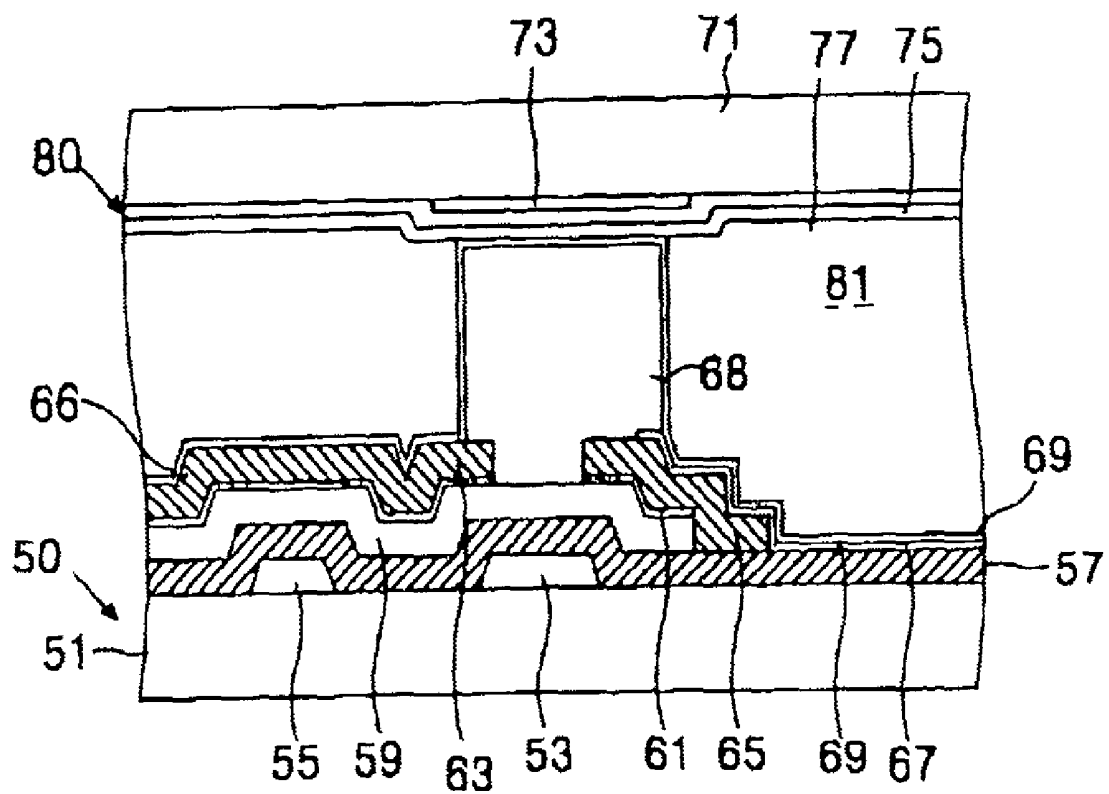


FIG. 9A

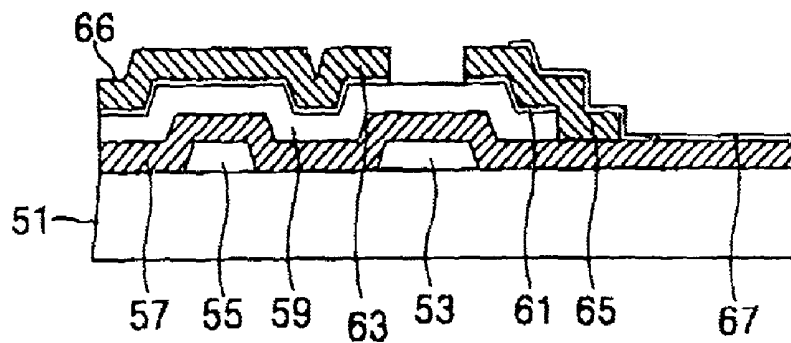


FIG. 9B

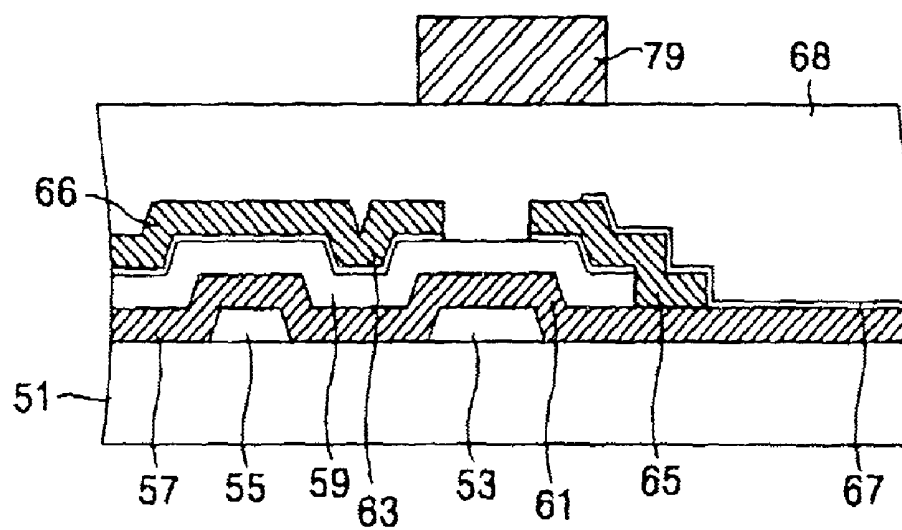


FIG. 9C

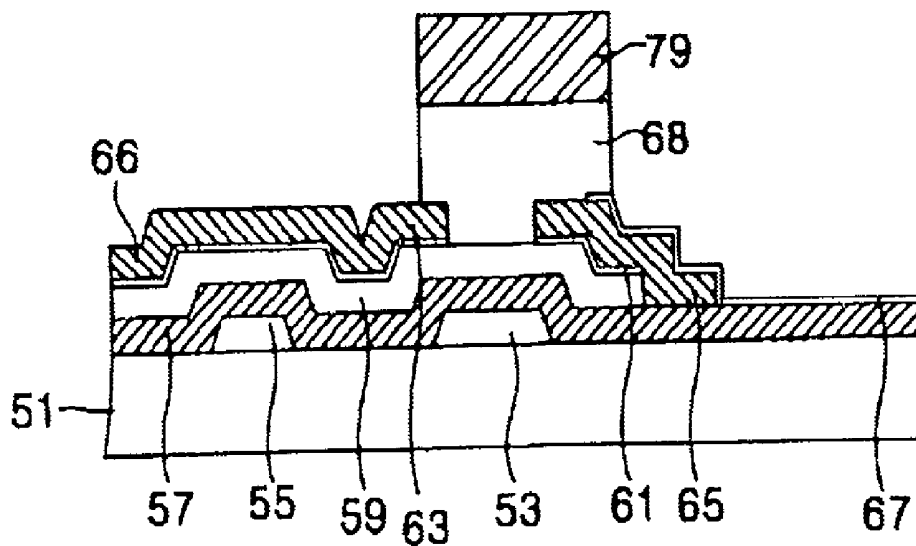
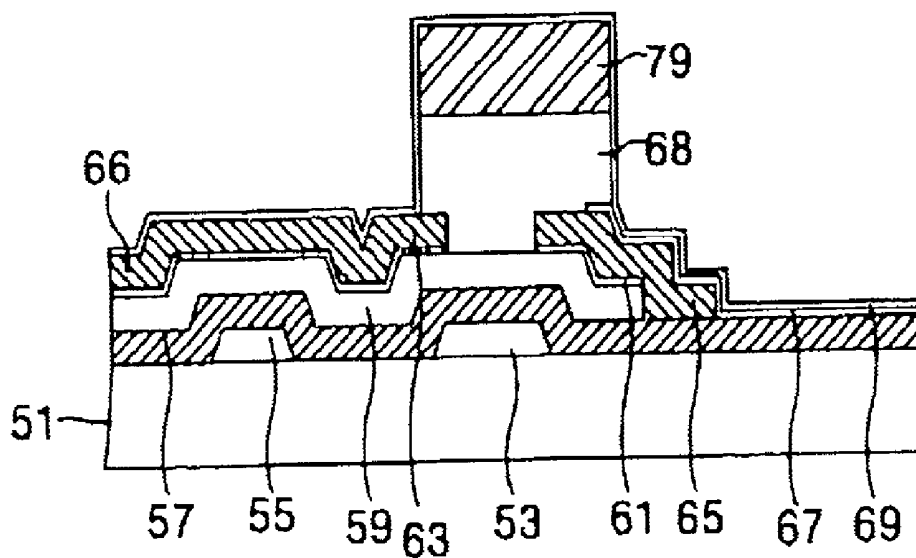
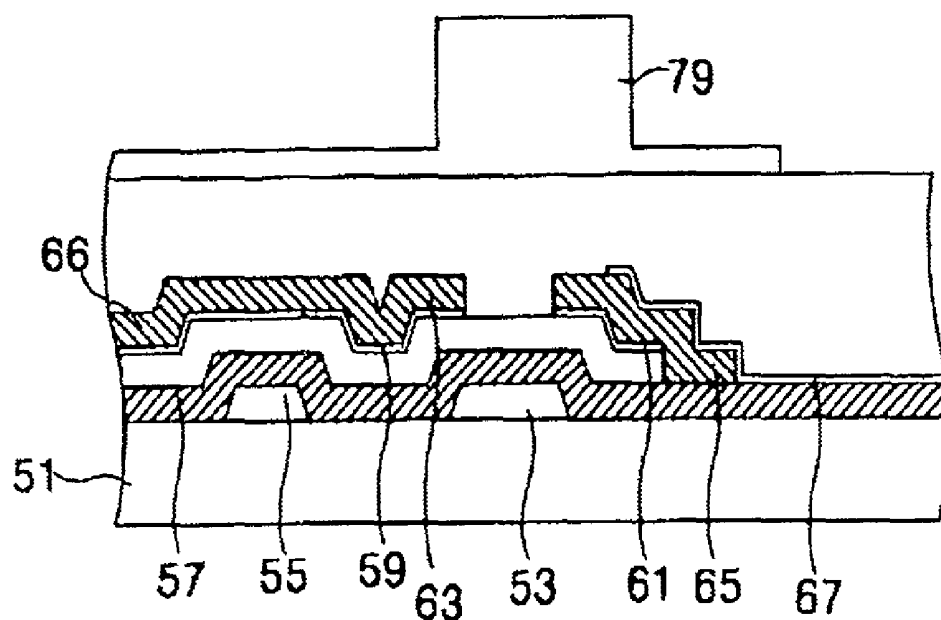


FIG. 9D



# FIG.10A



# FIG.10B

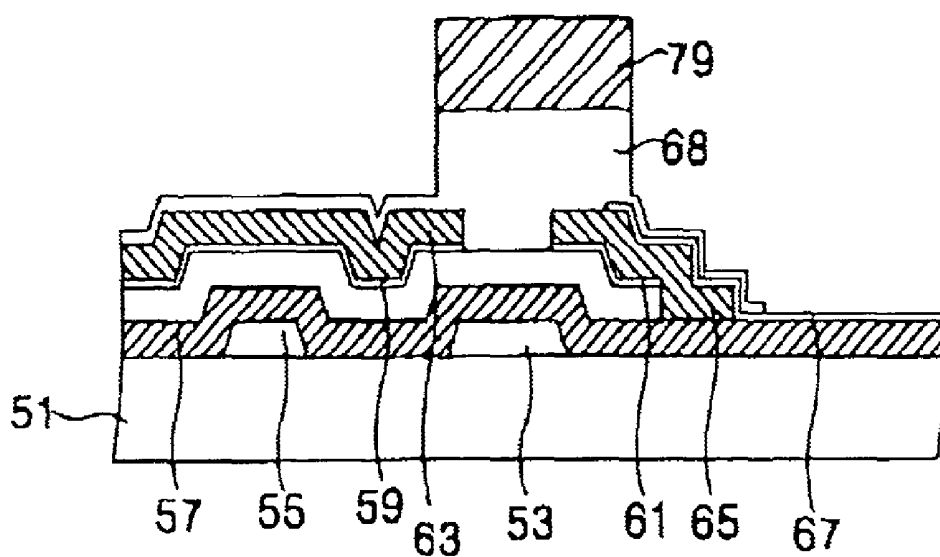


FIG. 10C

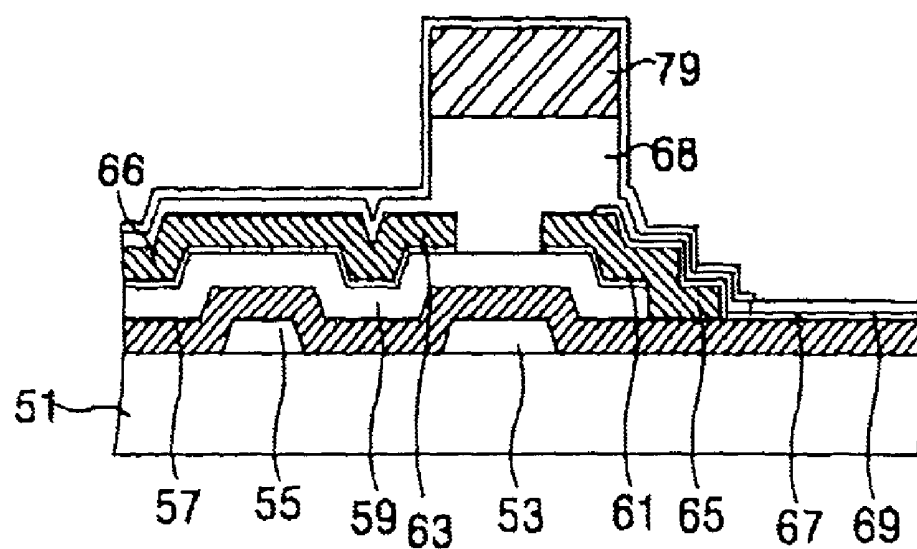


FIG. 11A

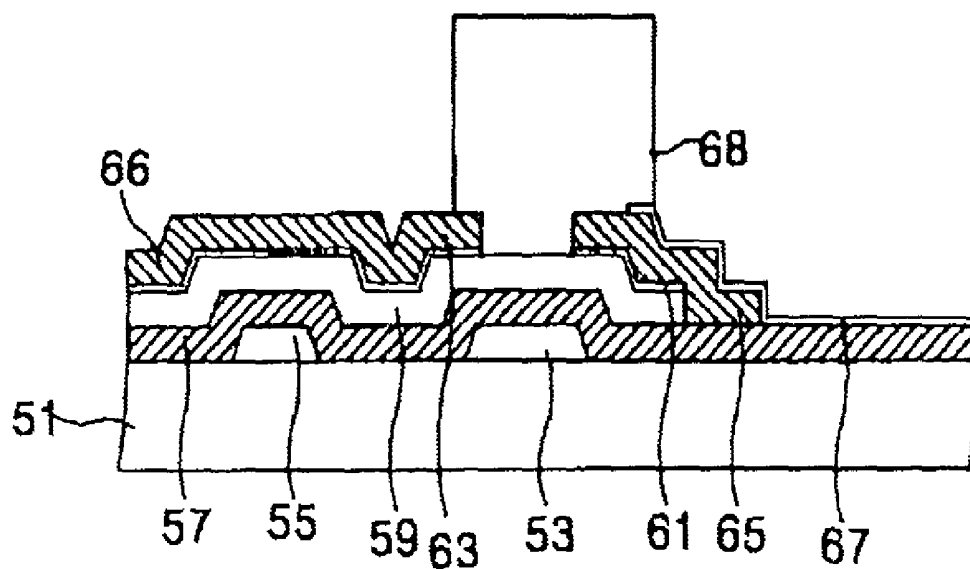
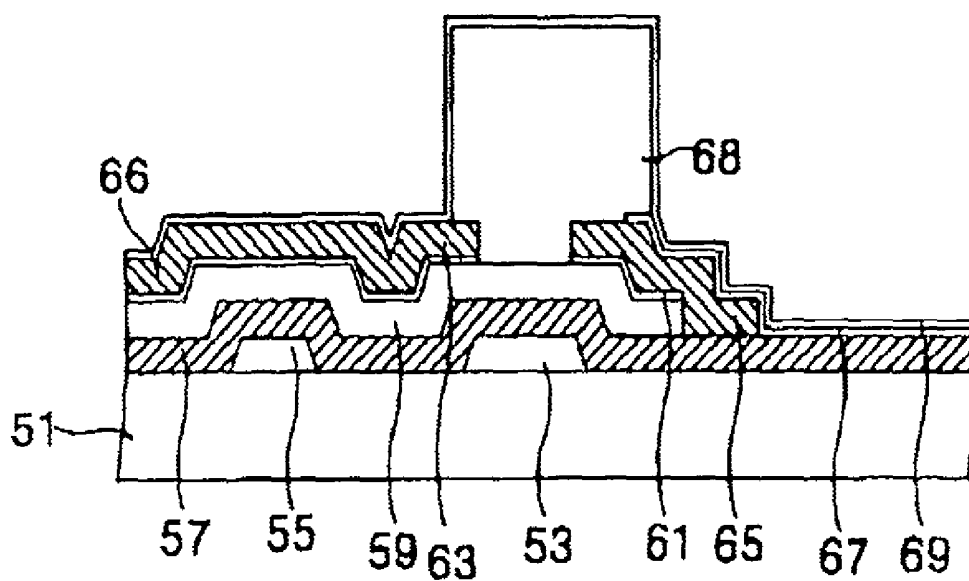


FIG. 11B



## LIQUID CRYSTAL DISPLAY PANEL

### BACKGROUND OF THE INVENTION

#### [0001] 1. Field of the Invention

[0002] This invention relates to a liquid crystal display panel, and more particularly to a liquid crystal display panel wherein a lower substrate provided with a thin film transistor array has a constant distance from an upper substrate provided with color filters.

#### [0003] 2. Description of the Related Art

[0004] Generally, a liquid crystal display (LCD) panel consists of a lower transparent substrate, an upper transparent substrate and a liquid crystal injected into a space defined by an adhesion of the upper transparent substrate to the lower transparent substrate.

[0005] In the lower transparent substrate, a pixel array in which a plurality of thin film transistors each consists of a gate electrode, a gate insulating film, an active layer, an ohmic contact layer, source and drain electrodes is electrically connected to a pixel electrode to make each pixel. Also, a driving circuit is formed or installed on the lower transparent substrate. In the upper transparent substrate, color filters and black matrices used as light-shielding layers are formed.

[0006] In a fabricating process of the LCD panel, the lower substrate and the upper substrate are manufactured by a separate process. Then, the lower substrate and the upper substrate are adhered to each other by a sealant such that the pixel electrodes of the lower substrate are opposed to the color filters of the upper substrate at a desired distance to define a space. A liquid crystal is injected into this space.

[0007] FIG. 1 is a planar view showing a lower substrate of a conventional liquid crystal panel, and FIG. 2 is a sectional view showing a structure of a conventional LCD panel, which includes the lower substrate of FIG. 1, across line A-A' of FIG. 1.

[0008] Referring to FIGS. 1 and 2, the conventional LCD panel consists of a lower substrate 10, an upper substrate 40 and a liquid crystal 45 filled in a space between the lower substrate 10 and the upper substrate 40.

[0009] The lower substrate 10 includes: a gate line 15; a data line 26; a thin film transistor positioned at an intersection of the gate line 15 with the data line 26; a pixel electrode 31 formed in a pixel area defined by crossing the gate and data lines 15 and 26; a spacer 43 on the intersection of the gate line 15 with the data line 26 for maintaining a constant distance between the upper and lower substrates. The thin film transistor consisting of a gate electrode 13, a gate insulating film 17, an active layer 19, an ohmic contact layer 21 and source and drain electrodes 23 and 25 formed on a first transparent substrate 11. The gate electrode 13 is connected to a gate line 15, and the source electrode 23 is connected to a data line 26.

[0010] A protective layer 27 covering the thin film transistors having the above-mentioned structure are formed on the gate insulating film 17, and a contact hole 29 exposing the drain electrode 25 is defined at this protective layer 27. On the protective layer 27 are provided a transparent pixel electrode 31 being in contact with and electrically connected

to the drain electrode via the contact hole 29. Also, a first alignment film 33 covering a pixel electrode 31 is formed on the protective layer 27.

[0011] The upper substrate 40 has a black matrix 37 and color filters (not shown) formed on a second transparent substrate 35. The black matrix 37 is formed at a portion corresponding to the thin film transistor of the lower substrate, or a portion corresponding to the gate line 15 and the data line 26 including said portion corresponding to the thin film transistor. The color filters are formed in correspondence with the pixel electrode to filter and pass red(R), green(G) and blue(B) lights. A transparent common electrode 39 are formed at the front side of the second transparent substrate 35, and a second alignment film 41 is formed on this common electrode 39.

[0012] The lower substrate 10 and the upper substrate 40 are adhered to each other such that the thin film transistor is opposed to the black matrix 37. In this case, a spacer 43 for allowing the lower substrate 10 to have a constant distance from the upper substrate is provided. The spacer 43 is made from an organic insulating material. The spacer 43 is formed at an intersection between the gate line 15 and the data line 26 of the data line 26 of the lower substrate 10 to constantly keep a distance between the lower substrate 10 and the upper substrate 40. The spacer 43 may be formed at the lower substrate 10 or the upper substrate 40. A liquid crystal 45 is injected a space made by an adhesion of the lower substrate 10 to the upper substrate 40.

[0013] As described above, the conventional LCD panel has constantly keep a space between the lower substrate and the upper substrate adhered to each other by means of the spacer formed at an intersection between the gate line and the data line of the lower substrate or the upper substrate.

[0014] However, the conventional LCD panel has a problem in that, since the lower substrate requires a spacer for constantly keeping a space between the lower substrate adhered to the protective layer protecting the thin film transistor and the upper substrate and the upper substrate requires a black matrix for shutting off a light, its structure and its fabricating process become complex. Also, the conventional LCD panel has a problem in that, since it is necessary to define a contact hole for connecting the pixel electrode to the drain electrode, its fabricating process becomes complex.

### SUMMARY OF THE INVENTION

[0015] Accordingly, it is an object of the present invention to provide a liquid crystal display panel wherein a space between a lower substrate and an upper substrate can be constantly kept by means of a protective film pattern.

[0016] Another object of the present invention is to provide a liquid crystal display panel wherein an upper substrate thereof does not require a black matrix for shielding a light.

[0017] In order to achieve these and other objects of the invention, a liquid crystal display panel according to one aspect of the present invention includes: a first substrate and a second substrate spaced from and facing to each other to have a gap therebetween; a liquid crystal layer between the first and second substrate; a thin film transistor formed on the first substrate, the thin film transistor having a semicon-

ductor pattern, a source electrode and drain electrode, a portion of the semiconductor pattern being exposed between the source electrode and the drain electrode; and a patterned spacer formed on the thin film transistor and supporting the second substrate, the patterned spacer having an insulating layer on the bottom which is in contact with the exposed portion or the semiconductor pattern.

[0018] The first substrate and the second substrate include a first alignment layer and a second alignment layer respectively. A part of the first alignment layer contacts the second alignment layer on a top surface of the patterned spacer. The patterned spacer includes a nontransparent layer on the organic layer. The nontransparent layer is wider than the exposed portion of the semiconductor pattern.

[0019] The liquid crystal display panel further including a data line formed on the first substrate and electrically coupled to one of the source and drain electrodes. The organic layer of the patterned spacer extends over the data line.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0020] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[0021] **FIG. 1** is a planar view showing a lower substrate of a conventional liquid crystal display panel;

[0022] **FIG. 2** is a sectional view showing a structure of a conventional liquid crystal display panel across line A-A' of **FIG. 1**;

[0023] **FIG. 3** is a planar view showing a structure of a liquid crystal display panel according to a first embodiment of the present invention;

[0024] **FIG. 4** is a sectional view showing a structure of a liquid crystal display panel according to a first embodiment of the present invention across line B-B' of **FIG. 3**;

[0025] **FIG. 5** is a planar view showing a structure of a liquid crystal display panel according to a second embodiment of the present invention;

[0026] **FIG. 6** is a sectional view showing a structure of a liquid crystal display panel according to a second embodiment of the present invention across line C-C' of **FIG. 5**;

[0027] **FIG. 7** is a planar view showing a structure of a liquid crystal display panel according to a third embodiment of the present invention;

[0028] **FIG. 8** is a sectional view showing a structure of a liquid crystal display panel according to a third embodiment of the present invention across line D-D' of **FIG. 7**;

[0029] **FIG. 9A** to **FIG. 9D** are section views showing a process of fabricating the lower substrate of the liquid crystal display panel in **FIG. 4**;

[0030] **FIG. 10A** to **FIG. 10C** are section views showing a process of fabricating the lower substrate of the liquid crystal display panel in **FIG. 6**; and

[0031] **FIG. 11A** and **FIG. 11B** are section views showing a process of fabricating the lower substrate of the liquid crystal display panel in **FIG. 6**.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0032] **FIG. 3** is a planar view showing a structure of a liquid crystal display panel according to a first embodiment of the present invention. **FIG. 4** is a sectional view showing a structure of a liquid crystal display panel according to a first embodiment of the present invention across line B-B' of **FIG. 3**.

[0033] Referring to **FIGS. 3 and 4**, there is shown a liquid crystal display (LCD) panel according to a first embodiment of the present invention. The LCD panel consists of a lower substrate **50**, an upper substrate **80** and a liquid crystal **81** filled in a space between the lower substrate **50** and the upper substrate **80**. The lower substrate **50** has a patterned spacer formed thereon. The pattern spacer supports the upper substrate **80** and includes an insulating layer.

[0034] As shown in **FIG. 3**, the lower substrate **50** includes: a gate line **55**; a data line **66**; a thin film transistor positioned at an intersection of the gate line **55** with the data line **66**; a pixel electrode **67** formed in a pixel area defined by crossing the gate and data lines **55** and **66**; and a protective layer **68** and a light-shielding layer **79**, formed on the thin film transistor, for a protection and a light-shielding of the thin film transistor. The thin film transistor consists of a gate electrode **53**, a gate insulating film **57**, an active layer **59**, an ohmic contact layer **61** and source and drain electrodes **63** and **65** formed on a first transparent substrate **51**. The gate electrode **53** is connected to a gate line **55**, and the source electrode **63** is connected to a data line **66**. The gate line **55** and the data line **66** cross each other, thereby defining a pixel area. The source electrode **63** and the drain electrode **65** on the ohmic contact layer **61** allow a portion of the active layer **59** to be exposed therebetween.

[0035] A transparent pixel electrode **67** being in contact with and electrically connected to the drain electrode **65** is formed at the pixel area on the gate insulating film **57**. A protective film **68** and a light-shielding layer **79** patterned to cover the thin film transistor are formed on the active layer **59** in such a manner to overlap with portions of the source and drain electrodes **63** and **65**. The protective film **68** is formed from a high-resistance organic insulating material such as acrylic organic compound, polyimide, cytop, BCB (benzocyclobutene) or PFCB (perfluorocyclobutane), etc., or an inorganic insulating material such as silicon nitride or silicon oxide, etc. to have a thickness of about 2 to 3  $\mu\text{m}$ . The light-shielding layer **79** is formed from a high polymer material such as black carbon absorbing a light or polyacryl including a photosensitive component to have a thickness of about 2 to 3  $\mu\text{m}$ .

[0036] The protective layer **68** and the light-shielding layer **79** are not only responsible for a protection and a light-shielding of the thin film transistor, respectively, but also serves a spacer for (constantly keeping an adhesion space between the lower substrate **50** and the upper substrate **80**). The protective layer **68** also prevents an off current of the thin film transistor from being increased due to a conductive carbon component contained in the light-shielding layer **79**. In other words, the protective layer **68** and the light-shielding layer **79** on the thin film transistor form a patterned spacer for supporting the second substrate. the patterned spacer uses the protective layer **68** on the bottom which is in contact with the exposed portion or the semiconductor pattern, as an insulating layer.



[0037] The entire surface of the lower substrate **50** having the above-mentioned structure is provided with a first alignment film **69** covering the Pixel electrode **67**, the protective layer **68** and the light-shielding layer **79**. The first alignment film **69** is formed from polyimide to have a thickness of about 500 to 800 Å.

[0038] The upper substrate **80** has color filters (not shown) filtering and passing red(R), green(G) and blue(B) lights formed at a portion corresponding to a pixel area on a second transparent substrate **71**. In this case, since the light-shielding layer **79** is formed on the thin film transistor of the lower substrate **50**, the upper substrate **80** does not require a black matrix.

[0039] A transparent common electrode **15** is formed at the front side of the second transparent substrate **71**, and a second alignment film **77** is formed on this common electrode **75**. The second alignment film **77** is formed from polyimide like the first alignment film **69** to have a thickness of about 500 to 800 Å.

[0040] The lower substrate **50** and the upper substrate **80** having the above-mentioned structure are adhered to each other such that the thin film transistor is opposed to the color filters (not shown). The lower substrate **50** has a constant distance from the upper substrate **80** by means of the protective layer **68** and the light-shielding layer **79** used as a spacer. A liquid crystal **81** is injected into a space defined by an adhesion of the lower substrate **50** to the upper substrate **80**.

[0041] FIG. 5 is a planar view showing a structure of a liquid crystal display panel according to a second embodiment of the present invention. FIG. 6 is a sectional view showing a structure of a liquid crystal display panel according to a second embodiment of the present invention across line C-C' of FIG. 5.

[0042] The LCD panel shown in FIGS. 5 and 6 has a structure identical to the LCD panel according to the first embodiment shown in FIGS. 3 and 4 except for a pattern of the protective layer **68**. Therefore, the same reference numerals are given to the parts of FIGS. 5 and 6 identical to those of FIGS. 3 and 4.

[0043] The protective layer **68** is formed such that a portion thereof corresponding to the active layer **59** of the thin film transistor has a thickness of about 2 to 3 μm and also is left on the source and drain electrodes **63** and **65** and the data line **66** at a thickness of about 0.2 to 1 μm. Thus, the protective layer **68** not only prevents the active layer **59** of the thin film transistor from being in contact with the light-shielding layer **79** to thereby prevent an increase of off current, but also prevents a corrosion and a current leakage of the source and drain electrodes **63** and **65** and the data line **66**.

[0044] The above-mentioned LCD panels according to the first and second embodiments do not require a spacer because the protective layer **68** and the light-shielding layer are formed on the thin film transistor to constantly keep a distance between the lower substrate **50** and the upper substrate **80**. Also, the upper substrates **80** of the LCD panels does not require a black matrix owing to such a light-shielding layer **70**.

[0045] FIG. 7 is a planar view showing a structure of a liquid crystal display panel according to a second embodi-

ment of the present invention. FIG. 8 is a sectional view showing a structure of a liquid crystal display panel according to a second embodiment of the present invention across line D-D' of FIG. 7.

[0046] The LED panel shown in FIGS. 7 and 8 has a structure identical to the LCD panel according to the first embodiment shown in FIGS. 3 and 4 except that only a protective layer **66** constantly keeps a distance between the lower substrate **50** and the upper substrate **80** and a black matrix is formed at the upper substrate **80**. Therefore, the same reference numerals are given to the parts of FIGS. 7 and 8 identical to those of FIGS. 3 and 4.

[0047] The protective layer **68** is formed on the thin film transistor to have a thickness of about 4 to 6 μm. Thus, the first alignment film **69** is formed at the entire surface of the lower substrate **50** in such a manner to cover the pixel electrode **67** and the protective layer **68**.

[0048] The black matrix **73** is formed on the second transparent substrate **35** of the upper substrate **80** at a portion corresponding to the thin film transistor of the upper substrate **50**, or a portion corresponding to the gate line **55** and the data line **66** including the thin film transistor.

[0049] FIG. 9A to FIG. 9D shows a process of fabricating the lower substrate of the LCD panel in FIG. 4.

[0050] Referring first to FIG. 9A, a plurality of thin film transistors each consisting of the gate electrode **53**, the gate insulating film **57**, the active layer **59**, the ohmic contact layer **61** and the source and drain electrodes **63** and **65** provided on the first transparent **51** are formed in such a manner to be electrically connected to the adjacent ones via the gate line **55** and the data line **66**.

[0051] Subsequently, a transparent conductive material such as indium tin oxide (ITO), tin oxide (TO) or indium zinc oxide (IZO), etc. is deposited onto the entire surface of the above-mentioned structure. At this time, the transparent conductive material is in direct contact with the source and drain electrodes **63** and **65** and the data line **66**. In this case, since the transparent conductive material is directly contacted with the drain electrode **65** without a contact hole, the subject process is simplified.

[0052] Furthermore, the transparent conductive material is patterned by the photolithography including a wet etching in such a manner to be in contact with the drain electrode **65** and be left only at the pixel area, thereby forming the pixel electrode **67**. At this time, the pixel electrode **67** is formed such that it is not in contact with the adjacent data line **66**.

[0053] Referring to FIG. 9B, a high-resistance organic insulating material such as acrylic organic compound, polyimide, cytop, BCB or PFCB, etc. is coated on the pixel electrode **67** into a thickness of about 2 to 3 μm to cover the thin film transistor, thereby, forming the protective film **68**. Alternatively, the protective layer **68** may be formed by depositing an inorganic material such as silicon nitride or silicon oxide, etc.

[0054] A high polymer material such as black carbon absorbing a light or polyacryl including a photosensitive component, etc. is coated on the protective layer **68** into a thickness of about 2 to 3 μm, thereby forming the light-shielding layer **79**. A sum of the thickness of the protective

layer 68 and the light-shielding layer 79 should be larger than a distance between the lower substrate and the upper substrate.

[0055] The light-shielding layer 79 is patterned by the conventional photographing method to expose the protective layer 68 and thus is left only at a portion corresponding to the thin film transistor.

[0056] Referring to FIG. 9C, the patterned light-shielding layer 79 is used as a mask to etch the exposed portion of the protective layer 68. The protective layer 68 is selectively etched by a mixture gas of a  $\text{SF}_6$  or  $\text{SF}_4$  gas and an  $\text{O}_2$  gas. At this time, the protective layer 68 as well as a desired thickness of the light-shielding layer 79 is removed.

[0057] In this case, the left protective film 68 and light-shielding layer 79 serves as a spacer for constantly keeping a distance between the upper substrate 80 and the lower substrate 50. Also, the light-shielding layer 79 eliminates the necessity of forming the black matrix on the upper substrate 80.

[0058] Referring to FIG. 9D, the entire surface on the above-mentioned structure is provided with the first alignment film 69 covering the pixel electrode 67, the protective layer 68 and the light-shielding layer 79. At this time, the first alignment film 69 is formed by printing polyimide into a thickness of about 500 to 800 Å by means of a screen printer.

[0059] FIGS. 10A to FIG. 10C show a process of fabricating the lower substrate 50 of the LCD panel in FIG. 6.

[0060] Referring first to FIG. 10A, a plurality of thin film transistors each consisting of the gate electrode 53, the gate insulating film 57, the active layer 59, the ohmic contact layer 61 and the source and drain electrodes 63 and 65 provided on the first transparent 51 are formed in such a manner to be electrically connected to the adjacent ones via the gate line 55 and the data line 66. The pixel electrode 67 is formed in such a manner to be in contact with the drain electrode 65 and be left only at the pixel area.

[0061] A high-resistance organic insulating material such as acrylic organic compound, polyimide, cytop, BCB or PFCB, etc. is coated on the pixel electrode 67 into a thickness of about 2 to 3  $\mu\text{m}$  to cover the thin film transistor, thereby forming the protective film 68. Alternatively, the protective layer 68 may be formed by depositing an inorganic material such as silicon nitride or silicon oxide, etc.

[0062] A high polymer material such as black carbon absorbing a light or polyacryl including a photosensitive component, etc. is coated on the protective layer 68 into a thickness of about 2 to 3  $\mu\text{m}$ , thereby forming the light-shielding layer 79. A sum of the thickness of the protective layer 68 and the light-shielding layer 79 should be larger than a distance between the lower substrate and the upper substrate.

[0063] The light-shielding layer 79 is patterned by the conventional photographing method using a half-tone mask. At this time, a portion responding to the thin film transistor of the light-shielding layer 79 is not patterned and a portion corresponding to the source and drain electrodes 63 and 65 and the data line 66 of the light-shielding layer 79 is left only into a thickness of 0.2 to 1  $\mu\text{m}$ . The remaining pixel area of the light-shielding layer 79 allows the protective layer to be exposed.

[0064] Referring to FIG. 10B, the patterned light-shielding layer 79 is used as a mask to selectively etch the exposed portion of the protective layer 68 by a mixture gas of a  $\text{SF}_6$  or  $\text{SF}_4$  gas and an  $\text{O}_2$  gas by exposing the pixel electrode 67 at the pixel area. At this time, the protective layer 68 as well as a desired thickness of the light-shielding layer 79 is removed. When the protective layer 68 on the pixel area is etched, a portion left at a thin thickness on said portion of the light-shielding layer 79 corresponding to the source and drain electrodes 64 and 65 and the data line 66 also is removed.

[0065] Accordingly, a portion of the protective layer 68 corresponding to the source and drain electrodes 63 and 65 and the data line 66 also is exposed and etched. Thus, the pixel electrode 67 at the pixel area is exposed, and said portion of the protective layer 68 corresponding to the source and drain electrodes 63 and 65 and the data line 66 is left into a desired thickness, for example, a thickness of about 0.2 to 1  $\mu\text{m}$ .

[0066] In this case, the protective layer 68 left at said portion corresponding to the source and drain electrodes 63 and 65 and the data line 66 prevents a corrosion and a current leakage of the source and drain electrodes 63 and 65 and the data line 66.

[0067] Referring to FIG. 10C, the entire surface on the above-mentioned structure is provided with the first alignment film 69 covering the pixel electrode 67, the protective layer 68 and the light-shielding layer 79. At this time, the first alignment film 69 is formed by printing polyimide into a thickness of about 500 to 800 Å by means of a screen printer.

[0068] FIG. 11A and FIG. 11C show a process of fabricating the lower substrate 50 of the LCD panel in FIG. 8.

[0069] Referring to FIG. 11A, plurality of thin film transistors each consisting of the gate electrode 53, the gate insulating film 57, the active layer 59, the ohmic contact layer 61 and the source and drain electrodes 63 and 65 provided on the first transparent 51 are formed in such a manner to be electrically connected to the adjacent ones via the gate line at 55 and the data line 66. The pixel electrode 61 is formed in such a manner to be in contact with the drain electrode 65 and be left only at the pixel area.

[0070] A high-resistance organic insulating material such as acrylic organic compound, polyimide, cytop, BCB or PFCB, etc. is coated on the pixel electrode 67 into a thickness of about 4 to 6  $\mu\text{m}$  to cover the thin film transistor, thereby forming the protective film 68. Alternatively, the protective layer 68 may be formed by depositing an inorganic material such as silicon nitride or silicon oxide, etc.

[0071] The protective layer 68 is patterned by the photolithography including a wet etching using a mixture gas of a  $\text{SF}_6$  or  $\text{SF}_4$  gas and an  $\text{O}_2$  gas in such a manner to be left only at a portion corresponding to the thin film transistor.

[0072] Referring to FIG. 11B, the entire surface on the above-mentioned structure is provided with the first alignment film 69 covering the pixel electrode 67 and the protective layer 68. At this time, the first alignment film 69 is formed by printing polyimide into a thickness of about 500 to 800 Å by means of a screen printer.

[0073] Since the lower substrate **50** formed by the above-mentioned process shown in **FIG. 11A** and **FIG. 11B** does not have a light-shielding layer, the black matrix **73** should be provided at the upper substrate **80** as shown in **FIG. 8**.

[0074] As described above, in the, LCD panel according to the present invention, the protective layer or two layers of the protective layer and the light-shielding layer formed at a portion corresponding to at least the thin film transistor are formed on the lower substrate at a higher position corresponding to a spaced distance from the upper substrate. Also, since the pixel electrode is formed prior to formation of the protective layer, it is in direct contact with the drain electrode without using a contact hole.

[0075] Accordingly, a spaced distance between the lower substrate and the upper substrate can be constantly kept by the protective layer or two layers of the protective layer and the light-shielding layer without an additional spacer, and the upper substrate does not require a black matrix for shutting off a light owing to the light-shielding layer provided on the lower substrate. Also, the pixel electrode is in direct contacted with the drain electrode without a contact hole. As a result, the LCD panel fabricating process can be reduced.

[0076] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display comprising:

a first substrate and a second substrate spaced from and facing to each other to have a gap therebetween;

a liquid crystal layer between the first and second substrate;

a thin film transistor formed on the first substrate, the thin film transistor having a semiconductor pattern, a source electrode and drain electrode, a portion of the semiconductor pattern being exposed between the source electrode and the drain electrode; and

a patterned spacer formed on the thin film transistor and supporting the second substrate, the patterned spacer having an insulating layer on the bottom which is in contact with the exposed portion of the semiconductor pattern.

2. The liquid crystal display as claimed in claim 1, the first substrate and the second substrate including a first alignment layer and a second alignment layer respectively, a part of the first alignment layer being in contact with the second alignment layer on a top surface of the patterned spacer.

3. The liquid crystal display as claimed in claim 1, the patterned spacer having a nontransparent layer on the organic layer, the nontransparent layer being wider than the exposed portion of the semiconductor pattern.

4. The liquid crystal display as claimed in claim 1, the liquid crystal display further including a data line formed on the first substrate and electrically coupled to one of the source and drain electrodes, the organic layer of the patterned spacer extending over the data line.

\* \* \* \* \*

专利名称(译)	液晶显示面板		
公开(公告)号	<a href="#">US20010040665A1</a>	公开(公告)日	2001-11-15
申请号	US09/792050	申请日	2001-02-26
[标]申请(专利权)人(译)	AHN BYUNG CHUL		
申请(专利权)人(译)	AHN BYUNG CHUL		
当前申请(专利权)人(译)	AHN BYUNG CHUL		
[标]发明人	AHN BYUNG CHUL		
发明人	AHN, BYUNG CHUL		
IPC分类号	G02F1/136 G02F1/1335 G02F1/1339 G02F1/1368		
CPC分类号	G02F1/133512 G02F1/13394 G02F1/1368		
优先权	1020000009502 2000-02-25 KR		
其他公开文献	US6774975		
外部链接	<a href="#">Espacenet</a> <a href="#">USPTO</a>		

#### 摘要(译)

一种液晶显示面板，设置有下列基板和上基板，上基板彼此间隔开并且彼此面对，以在它们之间具有间隙。在液晶面板中，液晶层位于第一和第二基板之间。下基板具有形成在其上的薄膜晶体管和形成在薄膜晶体管上并支撑第二基板的图案化间隔物。薄膜晶体管具有半导体图案，源电极和漏电极。半导体图案的一部分暴露在源电极和漏电极之间。图案化间隔物在底部具有绝缘层，该绝缘层与半导体图案的暴露部分接触。

