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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING METHOD THEREOF**

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(57) **ABSTRACT**

A liquid crystal display device includes a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel; a data converter for converting a first video data having a first frame frequency into a second video data having a second frame frequency, which is higher than the first frame frequency; a backlight unit having a first lamp group with at least two lamps for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and a driver for driving the gate lines, the first data lines and the second data lines in accordance with the second video data and for driving the first and second lamp groups at the second frame frequency so that the lamps of the first lamp group are sequentially turned on and off in synchronization with the lamps of the second lamp group.

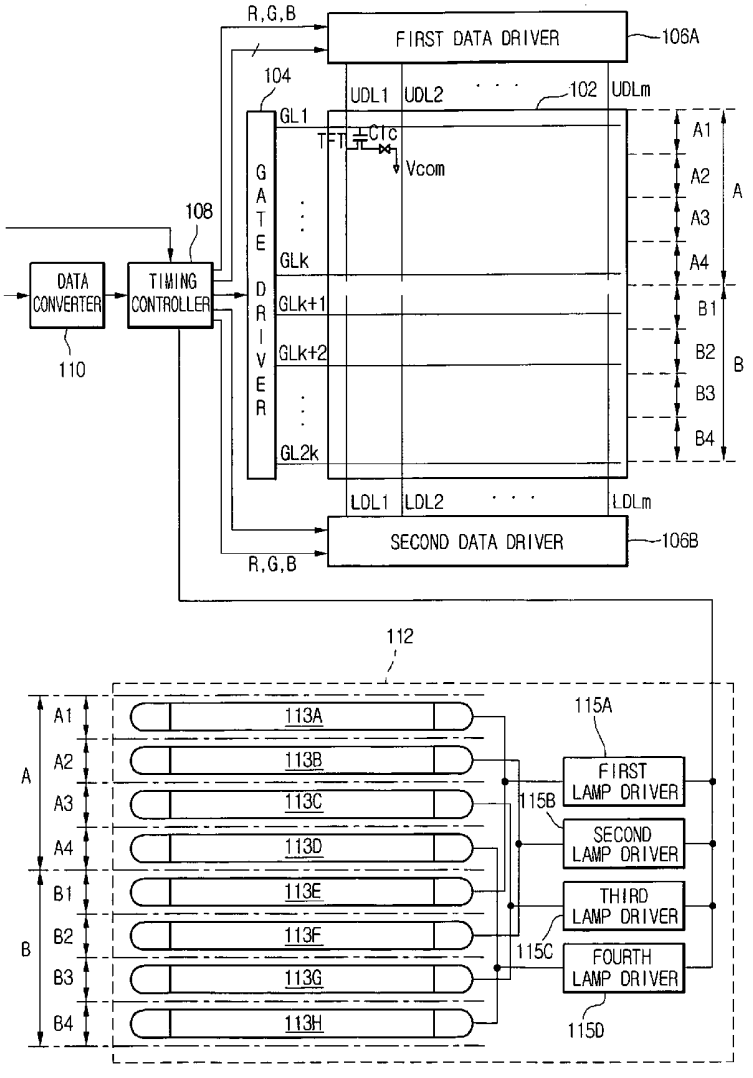


Fig. 1 (Related Art)

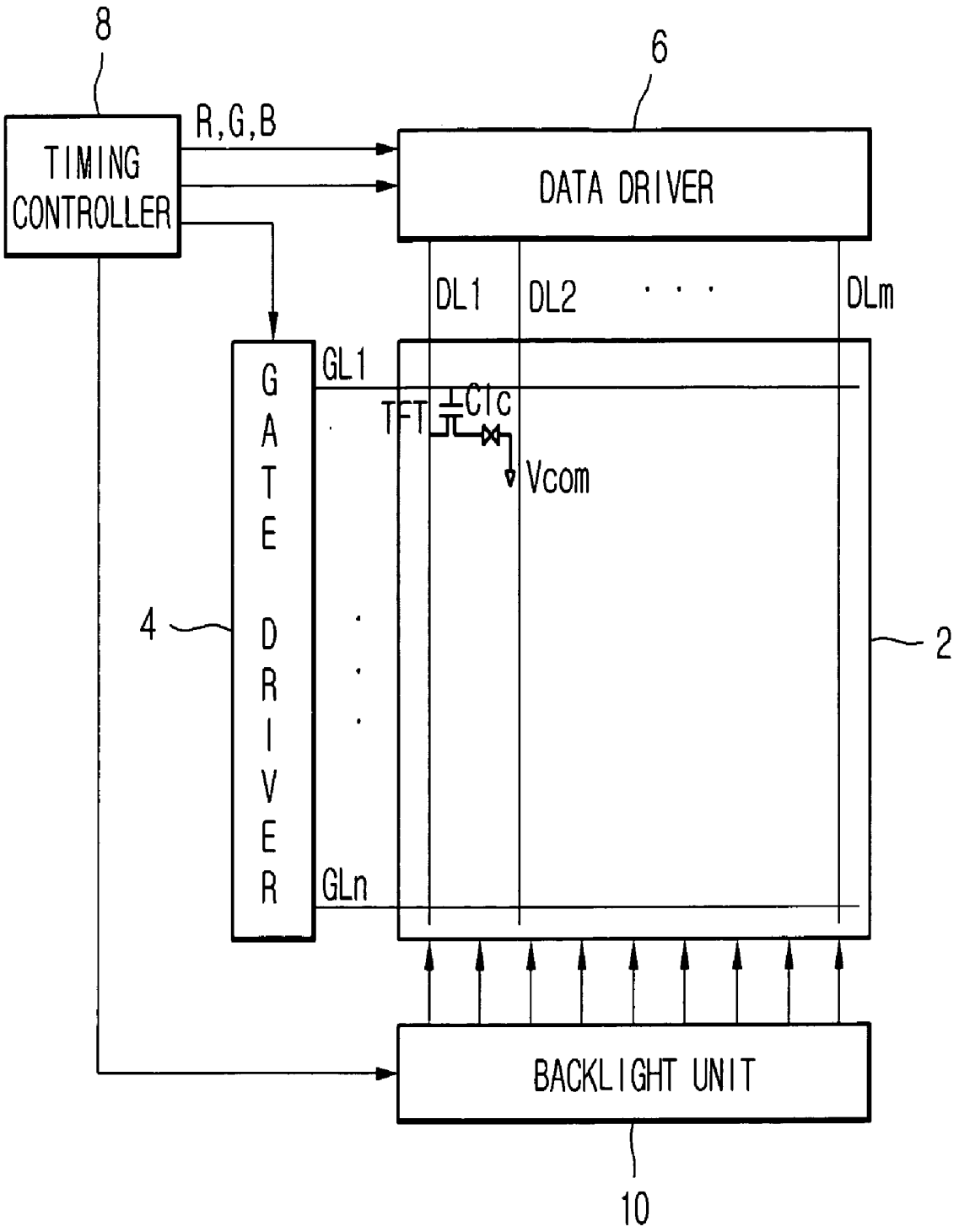


Fig. 2

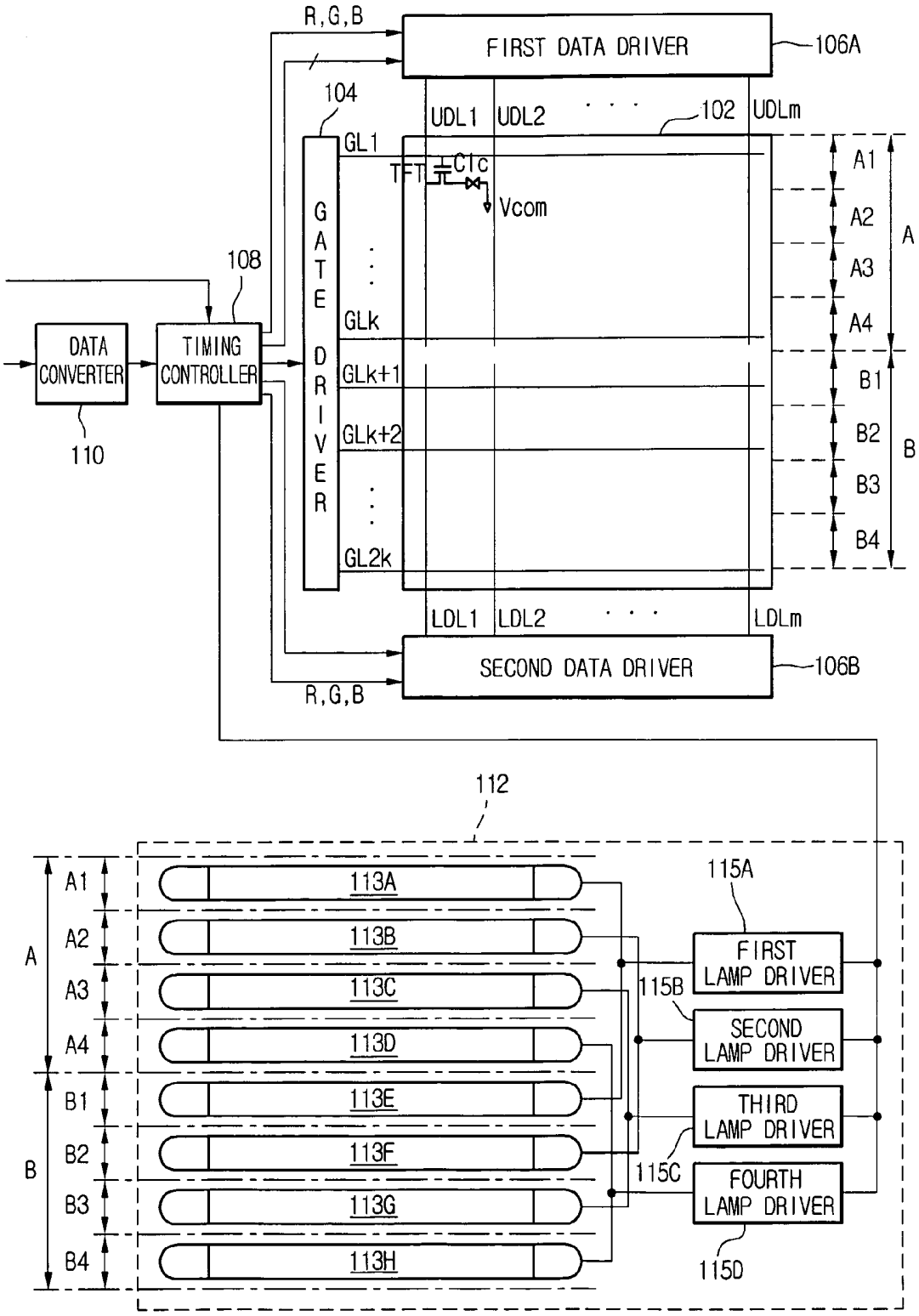
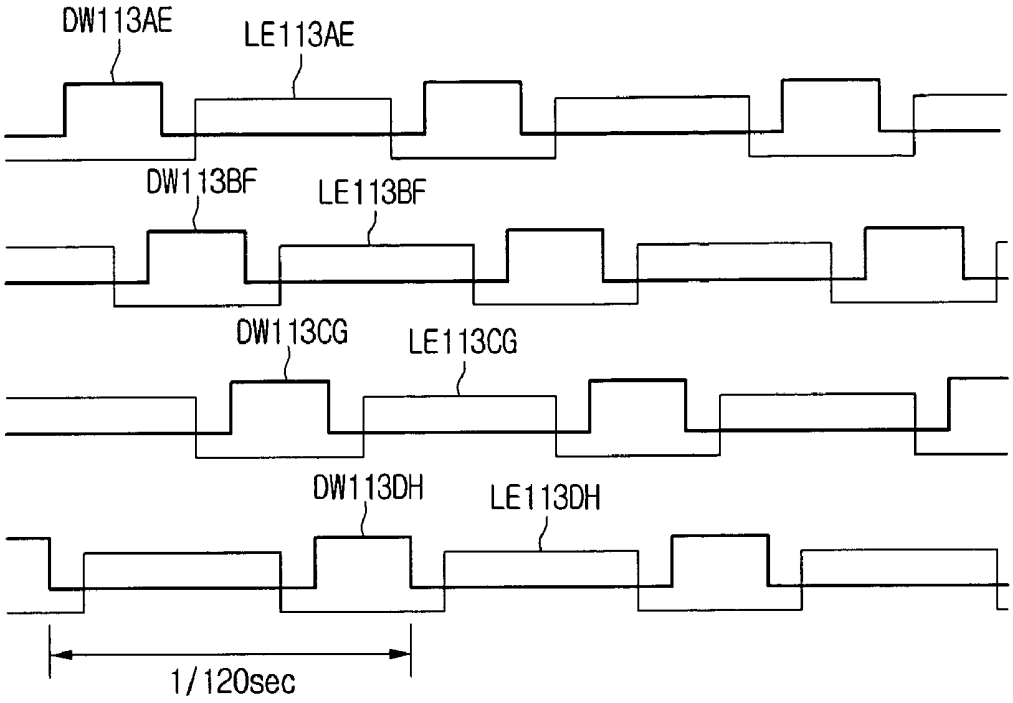

R,G,B
FIRST DATA DRIVER
106A
104
UDL1
UDL2
102
UDLm
GL1
TFT
Clc
Vcom
GATE DRIVER
108
DATA CONVERTER
TIMING CONTROLLER
110
GLk
GLk+1
GLk+2
GL2k
A1
A2
A3
A4
A
B1
B2
B3
B4
B
LDL1
LDL2
LDLm
SECOND DATA DRIVER
106B
R,G,B
112
113A
113B
113C
113D
113E
113F
113G
113H
115A
FIRST LAMP DRIVER
115B
SECOND LAMP DRIVER
THIRD LAMP DRIVER
115C
FOURTH LAMP DRIVER
115D

Fig. 3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LE113AE
DW113BF
LE113BF
DW113CG
LE113CG
DW113DH
LE113DH
1/120sec

Fig. 4

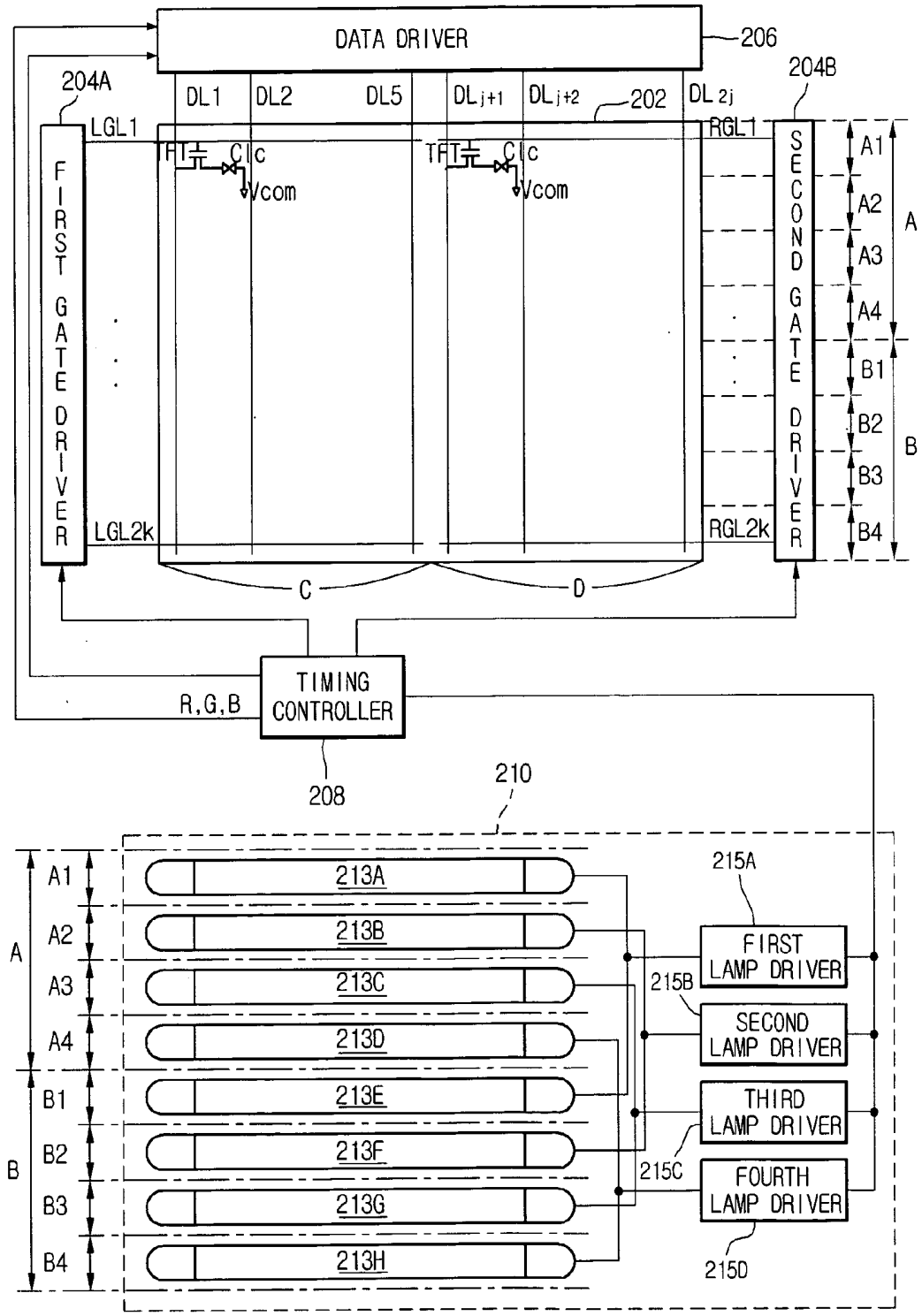

DATA DRIVER
206
204A
204B
DL1
DL2
DL5
DLj+1
DLj+2
202
DL 2j
LGL1
RGL1
TFT
Clc
Vcom
FIRST GATE DRIVER
SECOND GATE DRIVER
A1
A2
A3
A4
A
B1
B2
B3
B4
B
LGL2k
RGL2k
C
D
TIMING CONTROLLER
R,G,B
208
210
213A
213B
213C
213D
213E
213F
213G
213H
215A
FIRST LAMP DRIVER
215B
SECOND LAMP DRIVER
THIRD LAMP DRIVER
215C
FOURTH LAMP DRIVER
215D

Fig. 5

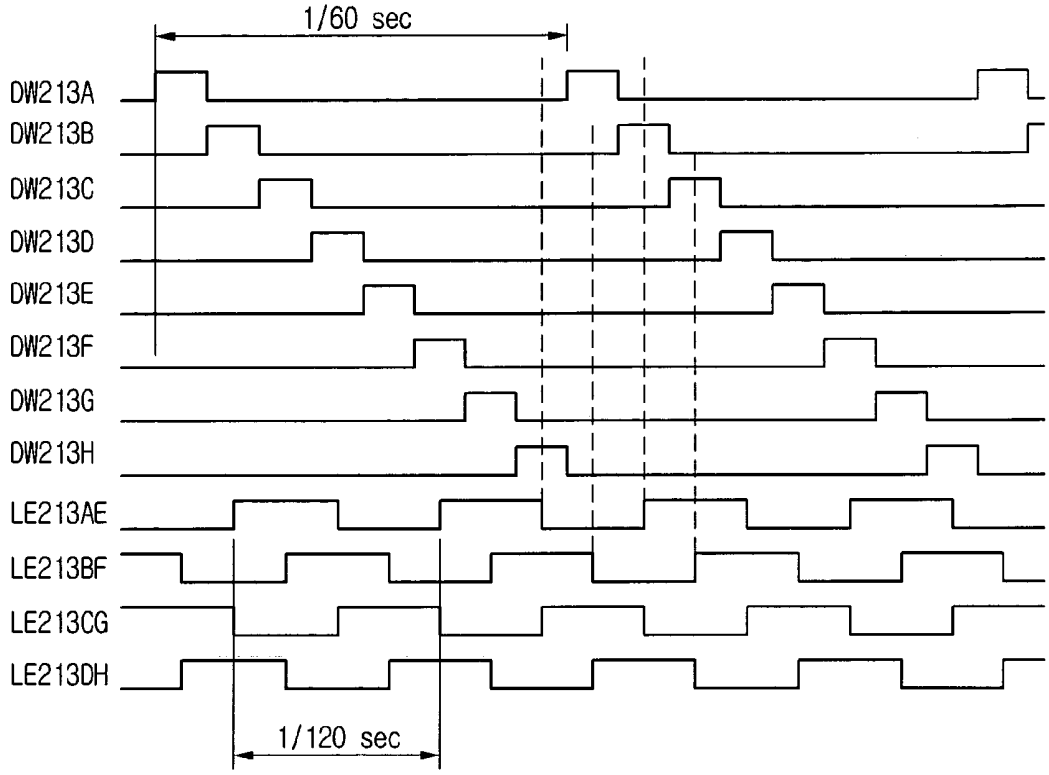

1/60 sec
DW213A
DW213B
DW213C
DW213D
DW213E
DW213F
DW213G
DW213H
LE213AE
LE213BF
LE213CG
LE213DH
1/120 sec

Fig. 6

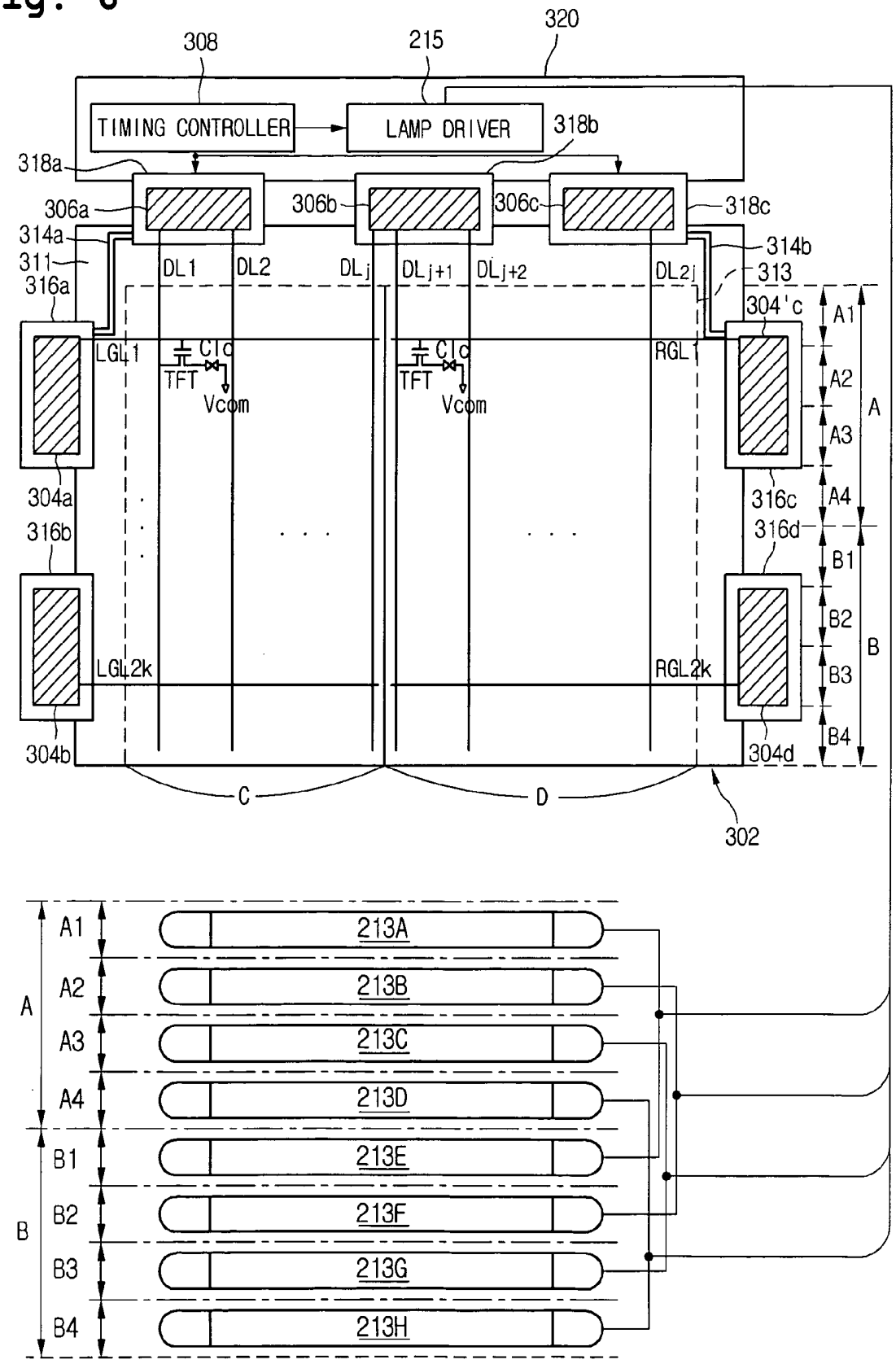

308
215
320
TIMING CONTROLLER
LAMP DRIVER
318a
318b
306a
306b
306c
318c
314a
314b
311
313
316a
DL1
DL2
DLj
DLj+1
DLj+2
DL2j
304'c
LGL1
RGL1
Clc
TFT
Vcom
A1
A2
A3
A4
A
304a
316c
316b
316d
B1
B2
B3
B4
B
LGL2k
RGL2k
304b
304d
C
D
302
213A
213B
213C
213D
213E
213F
213G
213H

Fig. 7

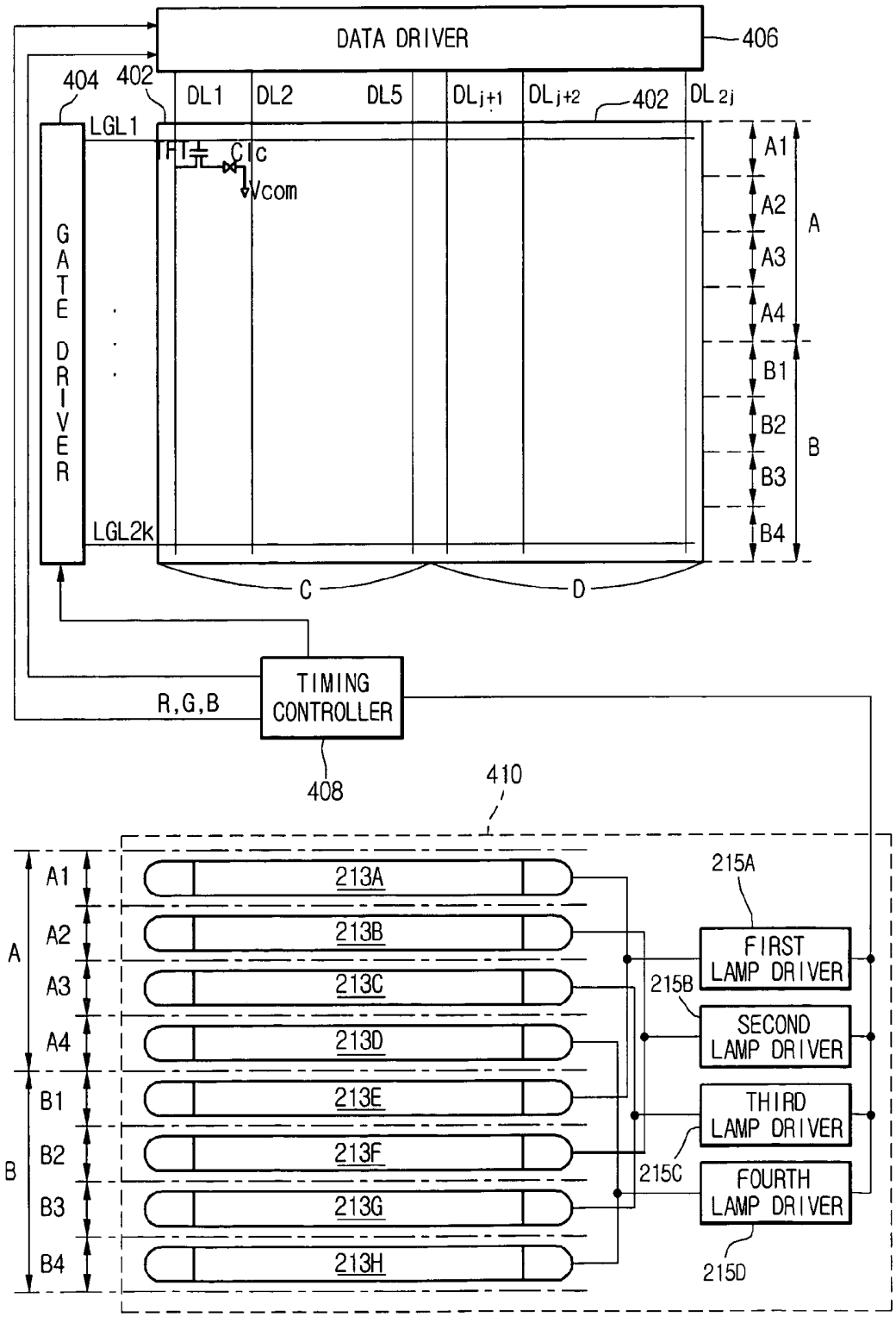

DATA DRIVER
406
404
402
DL1
DL2
DL5
DLj+1
DLj+2
402
DL2j
LGL1
TFT
Clc
Vcom
GATE DRIVER
A1
A2
A3
A4
A
B1
B2
B3
B4
B
LGL2k
C
D
TIMING CONTROLLER
R,G,B
408
410
213A
213B
213C
213D
213E
213F
213G
213H
215A
FIRST LAMP DRIVER
215B
SECOND LAMP DRIVER
THIRD LAMP DRIVER
215C
FOURTH LAMP DRIVER
215D

Fig. 8

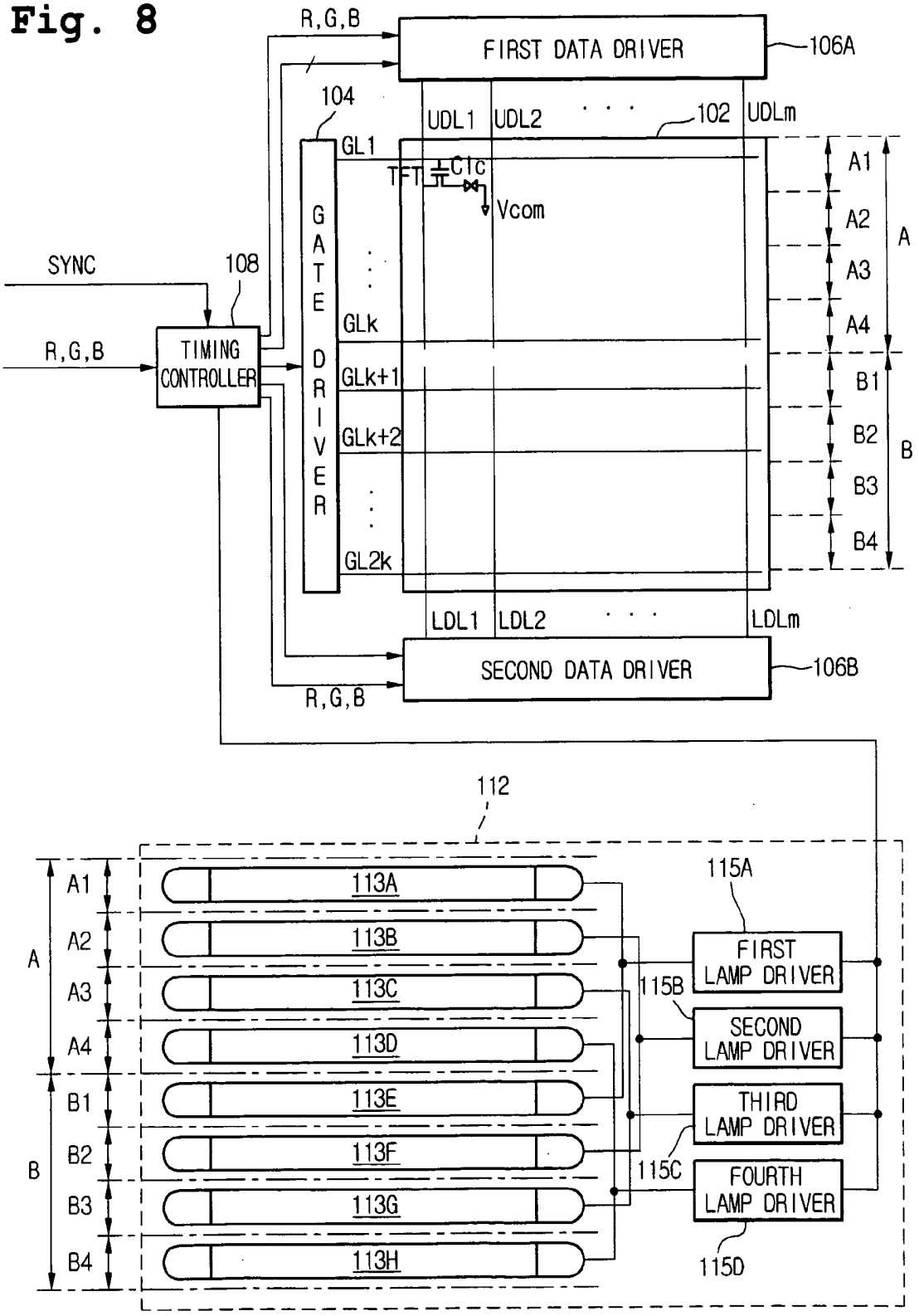

R,G,B
FIRST DATA DRIVER
106A
104
UDL1
UDL2
102
UDLm
GL1
TFT
C1c
Vcom
A1
A2
A3
A4
A
SYNC
108
GATE DRIVER
GLk
R,G,B
TIMING CONTROLLER
GLk+1
GLk+2
B1
B2
B3
B4
B
GL2k
LDL1
LDL2
LDLm
SECOND DATA DRIVER
106B
R,G,B
112
A1
A2
A3
A4
A
B1
B2
B3
B4
B
113A
113B
113C
113D
113E
113F
113G
113H
115A
FIRST LAMP DRIVER
115B
SECOND LAMP DRIVER
THIRD LAMP DRIVER
115C
FOURTH LAMP DRIVER
115D

Fig. 9A

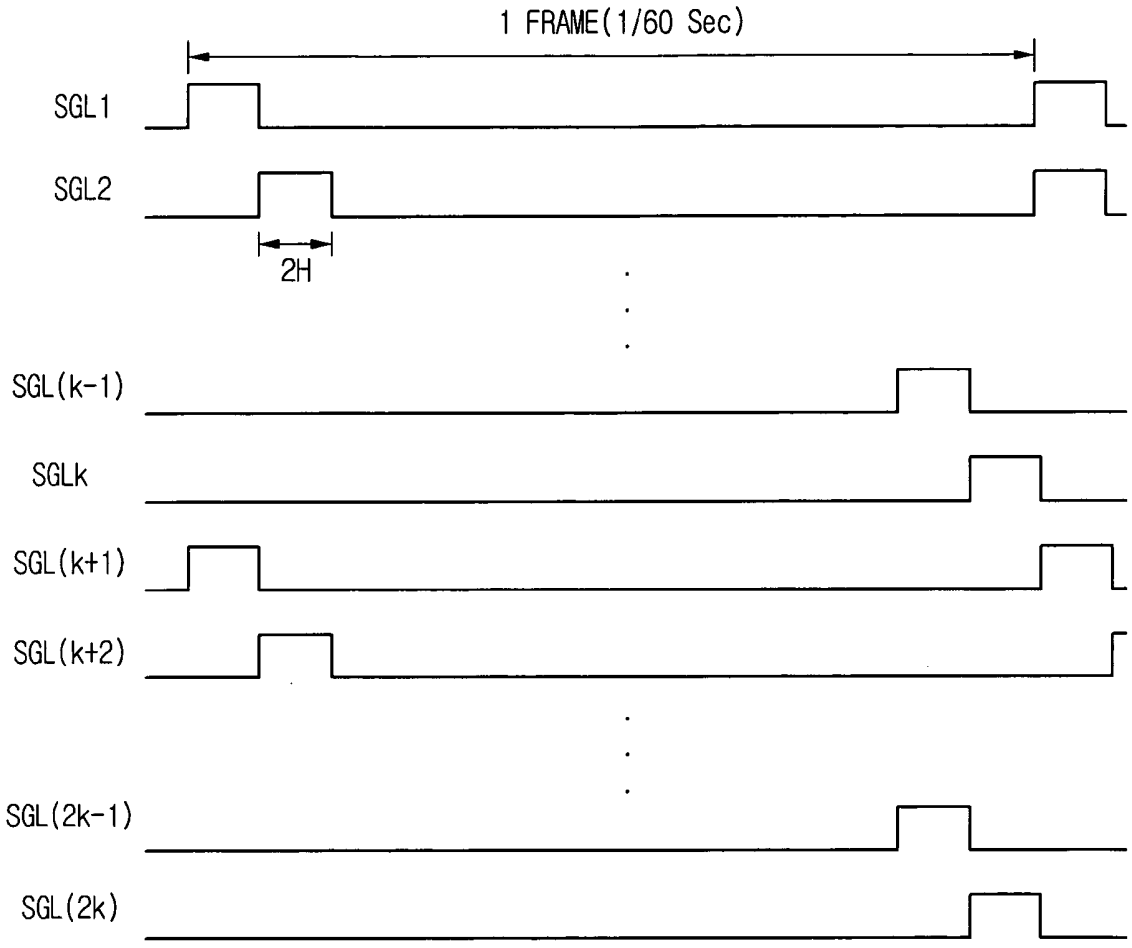

1 FRAME(1/60 Sec)
SGL1
SGL2
2H
SGL(k-1)
SGLk
SGL(k+1)
SGL(k+2)
SGL(2k-1)
SGL(2k)

Fig. 9B

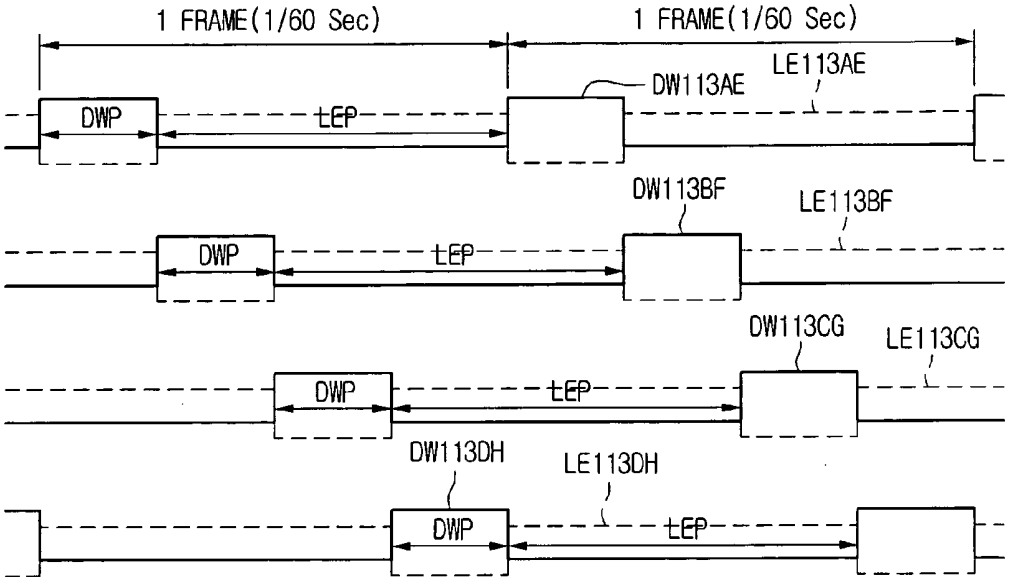

1 FRAME(1/60 Sec)
1 FRAME(1/60 Sec)
DW113AE
LE113AE
DWP
tEP
DW113BF
LE113BF
DWP
tEP
DW113CG
LE113CG
DWP
tEP
DW113DH
LE113DH
DWP
tEP

Fig. 10A

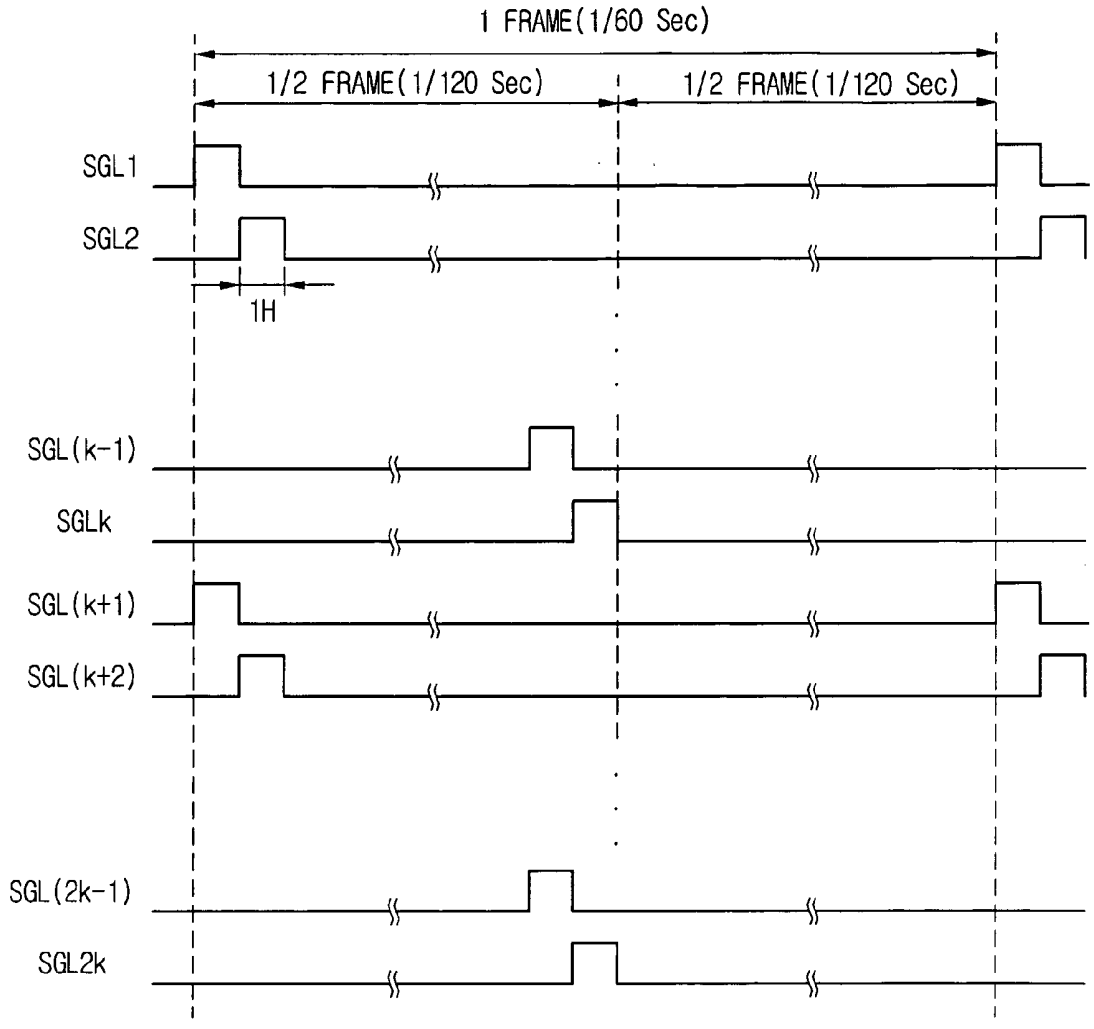
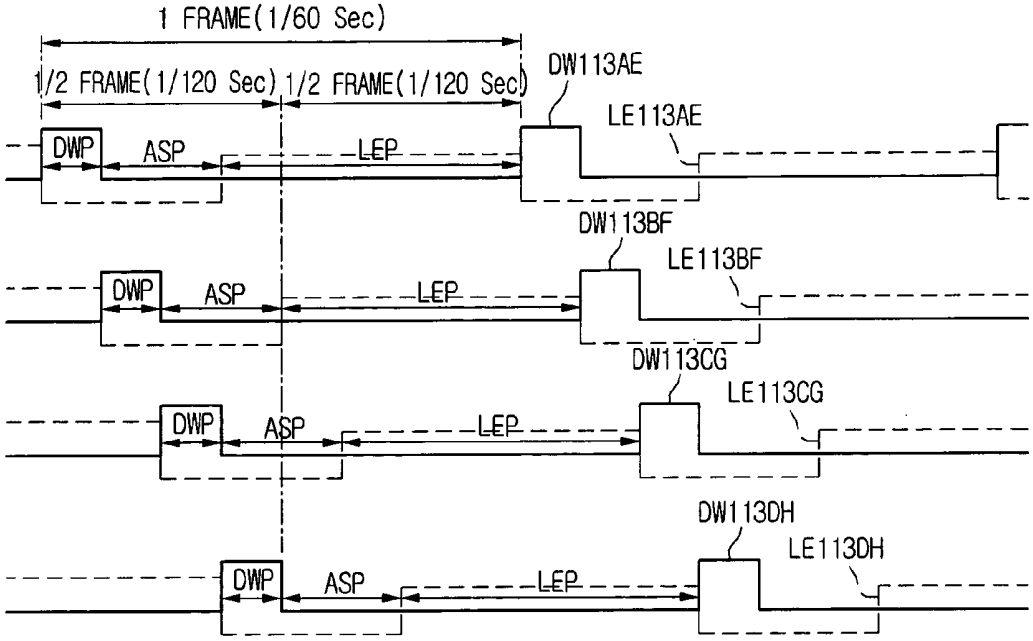

1 FRAME(1/60 Sec)
1/2 FRAME(1/120 Sec)
1/2 FRAME(1/120 Sec)
SGL1
SGL2
1H
SGL(k-1)
SGLk
SGL(k+1)
SGL(k+2)
SGL(2k-1)
SGL2k

Fig. 10B


1 FRAME(1/60 Sec)
1/2 FRAME(1/120 Sec)
1/2 FRAME(1/120 Sec)
DW113AE
LE113AE
DWP
ASP
LEP
DW113BF
LE113BF
DWP
ASP
LEP
DW113CG
LE113CG
DWP
ASP
LEP
DW113DH
LE113DH
DWP
ASP
LEP

LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING METHOD THEREOF

[0001] This application claims the benefit of the Korean Patent Application Nos. 10-2005-0132789, filed on Dec. 29, 2005, and 10-2006-080887, filed on Aug. 25, 2006, both of which are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Embodiments of the present invention relates to a display device, and more particularly, to a liquid crystal display device and a driving method thereof. Embodiments of the present invention are suitable for a wide scope of applications. In particular, some embodiments are suitable for preventing image-sticking and/or image blur.

[0004] 2. Description of the Related Art

[0005] As the information society develops, demand for various flat panel display devices is increasing. To meet such a demand, flat panel display devices, such as liquid crystal display device (LCD), plasma display panel (PDP), and electroluminescent display (ELD), have been developed. In particular, LCDs are lightweight, slim and have low power consumption. Also, LCDs can provide high image quality. Because LCDs have these advantages, LCDs have been replacing CRTs. For example, LCDs are widely used as monitors for TVs, computer displays and other types of display devices.

[0006] LCDs display images using optical anisotropy and polarization characteristics of liquid crystal molecules to display an image. Since the liquid crystal molecule is thin and long, liquid crystal molecules can be aligned in a predetermined direction. The direction of the molecular alignment of the liquid crystal molecules can be controlled by applying an electric field across the liquid crystal molecule. When the direction of the molecular alignment of the liquid crystal is controlled, the liquid crystal can be arranged such that the polarization state of light is changed along a chain of the liquid crystal molecules. Thus, by controlling the direction of the molecular alignment of the liquid crystal molecules, image information can be displayed.

[0007] FIG. **1** is a schematic diagram of a related art LCD. As shown in FIG. **1**, the related art LCD includes a liquid crystal panel **2** for displaying an image, a gate driver **4** and a data driver **6** for driving the liquid crystal panel **2**, a timing controller **8** for controlling the gate driver **4** and the data driver **6**, and a backlight unit **10** for generating light with a predetermined brightness that is irradiated onto the liquid crystal panel **2**.

[0008] In the liquid crystal panel **2**, a plurality of gate lines GL**1** to GLn and a plurality of data lines DL**1** to DLm are arranged to cross each other. Thin film transistors (TFTs) serve as switching elements at the crossings of the gate lines GL**1** to GLn and the data lines DL**1** to DLm. The TFTs are responsive to scan signals applied on corresponding gate lines GL to switch data voltages supplied from corresponding data lines DL to liquid crystal cells Clc, which are connected to a common voltage line Vcom.

[0009] The gate driver **4** supplies the scan signals to the gate lines GL**1** to GLn in response to gate control signals generated from the timing controller **8**. The scan signals are supplied to the gate lines GL**1** to GLn and each of the scan signals has a pulse of gate high voltage VGH, which is sequentially shifted. The pulse of the high voltage VGH has a width equal to a period of a horizontal sync signal. In response to the scan signals, the gate lines GL**1** to GLn are sequentially enabled once in each frame period, that is, in each period of a vertical sync signal.

[0010] The data driver **6** is responsive to data control signals to convert red (R), green (G) and blue (B) pixel data for one line into analog data voltages. The data driver **6** periodically supplies the one-line data voltages to the data lines DL**1** to DLm in accordance with a period of a horizontal sync signal.

[0011] The timing controller **8** generates the gate control signals, the data control signals, and the backlight control signals using vertical/horizontal sync signals (Vsync/Hsync), data enable signal (DE), and clock signal, which are generated from an external system (not shown), such as graphic card of computer system or TV signal decoder module of television receiver. In addition, the timing controller **8** receives video data containing R, G and B pixel data for each pixel, that is, in each frame, from a system (not shown), and supplies the inputted pixel data to the data driver **6** in line by line fashion.

[0012] The backlight unit **10** includes lamps (not shown), optical sheets, and a lamp driver for driving the lamps. The lamps generate light with a predetermined brightness in response to a lamp driving signal supplied from the lamp driver and provide the generated light to the liquid crystal panel **2**. The lamp driver generates the lamp driving voltage for driving the lamps by using a power voltage (Vdd) supplied from a power supply (not shown). The lamp driving voltage is supplied to the lamps according to the lamp control signal generated by the timing controller **8**.

[0013] The timing controller **8** generates the gate control signal, the data control signal, and the backlight control signal. When the gate control signal is supplied to the gate driver **4**, the gate driver **4** supplies the scan signals having the sequentially shifted pulses of gate high voltage VGH to the gate lines GL**1** to GLn. The gate lines GL**1** to GLn are sequentially enabled by the gate high voltage VGH of the scan signals. A TFT connected to the enabled gate line GL is turned on, so that the data voltage on the data line DL corresponding to the TFT is transferred to the corresponding liquid crystal cell Clc. Thereafter, when the scan signal changes from the gate high voltage VGH to a gate low voltage VGL, the TFT is turned off, so that the data line DL is electrically disconnected from the corresponding liquid crystal cell Clc. The liquid crystal cell Clc maintains the data voltage charged during the period of the pulse until another pulse of gate high voltage VGH is supplied in a next frame. The liquid crystal panel **2** is driven through this procedure such that an image is displayed on the liquid crystal panel **2**.

[0014] While the data voltage supplied to the liquid crystal cell is maintained during one frame, the lamps of the backlight unit **10** are on, regardless of timing in a frame. When displaying a moving picture, such a hold-type LCD cannot cope with the rapid image changes and a motion blurring phenomenon occurs. Consequently, an unclear image or image-sticking occurs in the LCD, which degrades image quality.

[0015] In addition, in the related art LCD, a predetermined time (hereinafter, referred to as an alignment saturation period) is required for alignment of the liquid crystal molecules of the liquid crystal cells in a direction corresponding to an applied data voltage after the data voltage has been

applied to the liquid crystal cells. During the alignment saturation period, the liquid crystal cells cannot correctly display the pixel data, thereby causing a motion blurring phenomenon and a more serious degradation of the image quality.

SUMMARY OF THE INVENTION

[0016] Accordingly, embodiments of the present invention are directed to an LCD and a driving method thereof that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[0017] An object of embodiments of the present invention is to provide an LCD that can improve the image quality by preventing motion blur.

[0018] Another object of embodiments of the present invention is to provide a method of driving an LCD that can improve the image quality by preventing motion blur.

[0019] Another object of embodiments of the present invention is to provide an LCD that can improve the image quality by preventing image-sticking.

[0020] Another object of embodiments of the present invention is to provide a method of driving an LCD that can improve the image quality by preventing image-sticking.

[0021] Additional advantages, objects, and features of embodiments of the present invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of embodiments of the present invention. The objectives and other advantages of embodiments of the present invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0022] To achieve these objects and other advantages and in accordance with the purpose of embodiments of the present invention, as embodied and broadly described herein, a liquid crystal display device includes a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel; a data converter for converting a first video data having a first frame frequency into a second video data having a second frame frequency, which is higher than the first frame frequency; a backlight unit having a first lamp group with at least two lamps for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and a driver for driving the gate lines, the first data lines and the second data lines in accordance with the second video data and for driving the first and second lamp groups at the second frame frequency so that the lamps of the first lamp group are sequentially turned on and off in synchronization with the lamps of the second lamp group.

[0023] In another aspect, a liquid crystal display device includes a liquid crystal panel having gate lines and data lines crossing each other; a backlight unit having a first lamp group with at least two lamps for divisionally irradiating light on a first region of the liquid crystal panel and a second lamp group with at least two lamps divisionally irradiating light on a second region of the liquid crystal panel; and a driver for driving the gate lines and data lines in accordance with a video data having first frame frequency and for controlling the first and second lamp groups to be simultaneously driven at a second frame frequency higher than the first frame frequency so that the lamps of the first lamp group are sequentially turned on and off in synchronization with the lamps of the second lamp group.

[0024] In another aspect, a liquid crystal display device includes a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel; a backlight unit having a first lamp group with at least two lamp for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and a driver for driving the gate lines and the data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in each frame in line by line fashion, and for driving the first and second lamp groups so that the at least two lamps of the first lamp group are sequentially turned on and off once in synchronization with the at least two lamps of the second lamp group.

[0025] In another aspect, a liquid crystal display device includes a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel; a backlight unit having a first lamp group with at least two lamps for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and a driver for operating the gate lines and the data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in each frame in a line by line manner, and for driving the first and second lamp groups so that the lamps of the first and second lamp groups are turned on and off at time when an alignment saturation period elapses after the data voltages are written to liquid crystal cells of the corresponding sub-regions.

[0026] In another aspect, a liquid crystal display device includes a liquid crystal panel having gate lines and data lines crossing each other; a backlight unit having a first lamp group with at least two lamps for divisionally irradiating light on a first region of the liquid crystal panel and a second lamp group with at least two lamps for divisionally irradiating light on a second region of the liquid crystal panel; and a driver for driving the gate lines and data lines to sequentially write data voltages of a video data to liquid crystal cells of the liquid crystal panel in each frame in line by line manner, and for controlling the first and second lamp groups to be sequentially turned on and off once in synchronization with each other.

[0027] In another aspect, a method is provided for driving a liquid crystal display device with a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel, and second data lines crossing the gate lines on a second region of the liquid crystal panel, the method including converting a first video data having a first frame frequency into a second video data having a second frame frequency higher than the first frame frequency; driving the gate lines, the first and second data lines in accordance with the second video data; and controlling the first and second lamp groups to turn-on and turn-off simultaneously at the second frame frequency, the first lamp

groups having at least two lamps for a first region and the second lamp group having at least two lamps for the second region.

[0028] In another aspect, a method is provided for driving a liquid crystal display device with a liquid crystal panel having gate lines and data lines crossing each other, the method including driving the gate lines and data lines in accordance with a video data having a first frame frequency; and controlling the first and second lamp groups to turn-on and turn-off simultaneously at a second frame frequency higher than the first frame frequency, the first lamp group having at least two lamps for a first region of the liquid crystal panel and the second lamp group having at least two lamps for a second region of the liquid crystal panel.

[0029] In another aspect, a method is provided for controlling a liquid crystal display device having a liquid crystal panel with first data lines crossing gate lines on a first region and second data lines crossing the gate lines on a second region, at least two first lamps partially corresponding to the first region of the liquid crystal panel, and at least two second lamps partially corresponding to the second region of the liquid crystal panel, the method including driving the gate lines and data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in line by line fashion; and turning on and off once the first lamps together with the second lamps by one pair at a time.

[0030] In another aspect, a method is provided for controlling a liquid crystal display device having a liquid crystal panel with first data lines crossing gate lines on a first region and second data lines crossing the gate lines on a second region, at least two first lamps partially corresponding to the first region of the liquid crystal panel, and at least two second lamps partially corresponding to the second region of the liquid crystal panel, the method including driving the gate lines and data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in a line by line manner; and driving the first and second lamps so that the lamps of the first and second lamps are turned on and off at time when an alignment saturation period elapses after the data voltages are written to liquid crystal cells on the liquid crystal panel.

[0031] It is to be understood that both the foregoing general description and the following detailed description of embodiments of the present invention are exemplary and explanatory and are intended to provide further explanation of embodiments of the present invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings, which are included to provide a further understanding of embodiments of the present invention and are incorporated in and constitute a part of this application, illustrate embodiments of the present invention and together with the description serve to explain the principle of embodiments of the present invention. In the drawings:

[0033] FIG. **1** is a schematic diagram of a related art LCD;

[0034] FIG. **2** is a schematic diagram of an LCD according to a first embodiment of the present invention;

[0035] FIG. **3** is a timing diagram of the respective parts of FIG. **2**;

[0036] FIG. **4** is a schematic diagram of an LCD according to a second embodiment of the present invention;

[0037] FIG. **5** is a timing diagram of the respective parts of FIG. **4**;

[0038] FIG. **6** is a schematic diagram of an LOG type LCD according to a third embodiment of the present invention;

[0039] FIG. **7** is a schematic diagram of an LCD according to a fourth embodiment of the present invention;

[0040] FIG. **8** is a schematic diagram of an LCD according to a fifth embodiment of the present invention;

[0041] FIGS. **9**A and **9**B are timing diagrams of respective parts of FIG. **8** according to a first driving mode; and

[0042] FIGS. **10** and **10**B are timing diagrams of respective parts of FIG. **8** according to a second driving mode.

DETAILED DESCRIPTION OF EMBODIMENTS

[0043] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0044] FIG. **2** is a schematic diagram of an LCD according to a first embodiment of the present invention. As shown in FIG. **2**, the LCD includes a liquid crystal panel **102** for displaying an image, a gate driver **104** for driving a plurality of gate lines GL**1**-GL**2***k* on the liquid crystal panel **102**, a first data driver **106**A for driving a plurality of upper data lines UDL**1**-UDLm formed on the liquid crystal panel **102**, and a second data driver **106**B for driving a plurality of lower data lines LDL**1**-LDLm on the liquid crystal panel **102**.

[0045] The upper data lines UDL**1**-UDLm are arranged on an upper portion A of the liquid crystal panel **102** and cross a first k number of gate lines GL**1**-GLk arranged in a vertical direction. The lower data lines LDL**1**-LDLm are arranged on a lower portion B of the liquid crystal panel **102** and cross a second k number of gate lines GL(k+1)-GL**2***k* arranged in a vertical direction. TFTs, acting as switching elements, are formed at crossings of the gate lines GL**1**-GL**2***k* and the upper and lower data lines UDL**1**-UDLm and LDL**1**-LDLm. In response to scan signals applied on the corresponding gate lines GL, the TFTs switch data voltages supplied from the corresponding data lines UDL and LDL to liquid crystal cells Clc connected to common voltage lines Vcom. The liquid crystal cells Clc of the liquid crystal panel **102** transmit light proportionally or inversely proportional to an electric potential difference between the data voltages of the data lines UDL and LDL and the reference voltage, that is, the common voltage Vcom.

[0046] The gate driver **104** generates the scan signals for the gate lines GL**1**-GL**2***k* in response to the gate control signals. The scan signals from the gate driver **104** enable the first k number of gate lines GL**1** to GLk to be sequentially driven once for a half period of one vertical sync signal, and enable the second k number of the gate lines GL(k+1)-GL**2***k* sequentially once for a half period of one vertical sync signal. For example, while the first gate line GL**1** on the upper portion A of the liquid crystal panel **102** is enabled (that is, for a period of one horizontal sync signal), the first gate line GL(k+1) on the lower portion B of the liquid crystal panel **102** also is enabled. In another example, for the period of one horizontal sync signal that the last gate line GLk at the upper portion A of the liquid crystal panel **102** is enabled, the last gate line GK**2***k* on the lower portion B of the liquid crystal panel **102** also is enabled. Thus, each of the k number of scan signals supplied to the first k number of

gate lines GL**1**-GLk arranged on the upper portion A of the liquid crystal panel **102** has shifted pulses of gate high voltage VGH. Likewise, each of the second k number of scan signals supplied to the second k number of gate lines GL(k+1)-GL**2***k* arranged on the lower portion B of the liquid crystal panel **102** has a shifted pulse of gate high voltage VGH. The scan signals supplied to the first k number of gate lines GL**1**-GLk arranged on the upper portion A of the liquid crystal panel **102** have the same waveforms as the scan signals supplied to the second k number of gate lines GL(k+1)-GL**2***k* arranged on the lower portion B of the liquid crystal panel **102**. The pulse of the gate high voltage VGH contained in the scan signal has a width equal to the period of one horizontal sync signal.

[0047] The first data driver **106**A converts R, G and B pixel data corresponding to one line into analog data voltages in response to the data control signals at each period of the horizontal sync signal, and supplies the one-line data voltages to the upper data lines UDL**1**-UDLm arranged on the upper portion A of the liquid crystal panel **102**. In other words, the first data driver **106**A outputs the one-line data voltages whenever any one of the gate lines GL**1**-GLk arranged on the upper portion A of the liquid crystal panel **102** is enabled, that is, in every period of one horizontal sync signal. When the pulse of the gate high voltage VGH enables one of the gate lines GL**1**-GLk, the TFT connected to the enabled gate line is turned on, so that the data voltage from the corresponding upper data line UDL is transferred to the corresponding liquid crystal cell Clc. When the scan signal changes from the gate high voltage VGH to the gate low voltage VGL, the turned-on TFT is turned off, so that the corresponding liquid crystal cell Clc is electrically disconnected from the corresponding upper data line UDL. The liquid crystal cell Clc is charged with the data voltage supplied from the corresponding data line UDL during the turn-on period of the TFT, and the charged data voltage is maintained until the corresponding TFT is turned on again.

[0048] Likewise, the second data driver **106**B converts R, G and B pixel data corresponding to one line into analog data voltages in response to the data control signals at each period of the horizontal sync signal, and supplies the one-line data voltages to the lower data lines LDL**1**-LDLm arranged on the lower portion B of the liquid crystal panel **102**. The second data driver **106**B outputs the one-line data voltages whenever any one of the gate lines GL(k+1)-GL**2***k* arranged on the lower portion B of the liquid crystal panel **102** is enabled, that is, in every period of one horizontal sync signal. When the pulse of the gate high voltage VGH enables one of the gate lines GL(k+1)-GL**2***k*, the TFT connected to the enabled gate line is turned on, so that the data voltage from the corresponding lower data line LDL is transferred to the corresponding liquid crystal cell Clc. When the scan signal changes from the gate high voltage VGH to the gate low voltage VGL, the turned-on TFT is turned off, so that the corresponding liquid crystal cell Clc is electrically disconnected from the corresponding lower data line LDL. The liquid crystal cell Clc is charged with the data voltage supplied from the corresponding data line LDL during the turn-on period of the TFT, and the charged data voltage is maintained until the corresponding TFT is turned on again.

[0049] The gate driver **104** and the first and second data drivers **106**A and **106**B write the data voltage to the liquid crystal cells of the liquid crystal panel **102** once for a half period of the frame period, that is, a half period of the vertical sync signal.

[0050] Referring to FIG. **2**, the LCD includes a timing controller **108** for controlling the gate driver **104** and the first and second data drivers **106**A and **106**B, a data converter **110** for converting the frame frequency of the video data to be supplied to the timing controller **108**, and a backlight unit **112** for irradiating light onto the liquid crystal panel **102**. The timing controller **108** generates the gate control signals and the data control signals using vertical/horizontal sync signals (Vsync/Hsync), data enable signal (DE), and clock signal, which are generated from an external system (not shown), such as graphic card of computer system or TV signal decoder module of television receiver. In response to the gate control signals, the gate driver **104** enables the first k number of gate lines GL**1**-GLk arranged on the upper portion A of the liquid crystal panel **102** to be sequentially driven once for a half period of one vertical sync signal and forces the second k number of the gate lines GL(k+1)-GL**2***k* arranged on the lower portion B of the liquid crystal panel **102** to be sequentially driven in synchronization with the first k number of the gate lines GL(k+1)-GL**2***k*. In response to the data control signals, the first data driver **106**A supplies the one-line data voltages to the upper data lines UDL**1**-UDLm whenever any one of the first k number of the gate lines GL**1**-GLk is enabled, the second data driver **106**B also supplies the one-line data voltages to the lower data lines LDL**1**-LDLm whenever any one of the second k number of the gate lines GL(k+1)-GL**2***k* is enabled.

[0051] In addition, the timing controller **108** arranges the R, G and B pixel data supplied from the external system into a line by line R, G and B pixel data, and supplies the one-line R, G and B pixel data to the first and second data drivers **106**A and **106**B. Therefore, the first and second data drivers **106**A and **106**B convert the l-line R, G and B pixel data into analog data voltages. The 1-line data voltages converted by the first data driver **106**A and the 1-line data voltages converted by the second data driver **106**B are simultaneously supplied to the upper and lower data lines UDL**1**-UDLm and LDL**1**-LDLm.

[0052] The data converter **110** converts the frame frequency of the frame-based pixel data supplied from the external system to the timing controller **108**. The frame-based pixel data supplied from the external system to the data converter **110** has a frame frequency of a first integer (e.g., 60 Hz), the frame-based pixel data outputted from the data converter **110** has a frame frequency of a second integer (e.g., 120 Hz) corresponding to multiple of the first integer. In other words, the data converter **110** multiplies the frame frequency of the pixel data from the external system by at least two. The data converter **110** generates frame-based interpolation pixel data from the frame-based pixel data outputted from the external system, arranges the frame-based interpolation pixel data between the frame-based original pixel data to create new pixel data, and supplies the new pixel data to the timing controller **108**. The timing controller **108** controls the gate driver **104** and the first and second data drivers **106**A and **106**B to drive the liquid crystal panel **102** at a frame frequency (e.g., 120 Hz) that is at least twice the original frame frequency (e.g., 60 Hz).

[0053] The backlight unit **112** includes first to eighth lamps **113**A to **113**H arranged in parallel under the liquid crystal panel **102**. The first to fourth lamps **113**A to **113**D are

arranged to correspond to the upper portion A of the liquid crystal panel **102**, while the fifth to eighth lamps **113**E to **113**H are arranged to correspond to the lower portion B of the liquid crystal panel **102**. The first to fourth lamps **113**A to **113**D irradiate light onto first to fourth sub-sections A**1** to A**4** defined by dividing the upper portion A of the liquid crystal panel **102** by four. For example, the first lamp **113**A irradiates light to the uppermost sub-section A**1** on the upper portion A of the liquid crystal panel **102**, and the fourth lamp **113**D irradiates light onto the lowermost sub-section A**4** on the lower portion A of the liquid crystal panel **102**. Likewise, the fifth to eighth lamps **113**E to **113**H irradiate light onto four sub-sections B**1** to B**4** defined by dividing the lower portion B of the liquid crystal panel **102** by four. For example, the fifth lamp **113**E irradiates light onto the uppermost sub-section B**1** on the lower portion B of the liquid crystal panel **102**, and the eighth lamp **113**H irradiates light onto the lowermost sub-section B**4** on the lower portion B of the liquid crystal panel **102**.

[0054] The backlight unit **112** includes first to fourth lamp drivers **115**A to **115**D commonly connected to the timing controller **108**. Each of the first to fourth lamp drivers **115**A to **115**D simultaneously turns on and off (or turns off and on) one of the lamps for the upper portion A of the liquid crystal panel **102** and one of the lamps for the lower portion B of the liquid crystal panel **102**. In response to the lamp control signals outputted from the timing controller **108**, the first to fourth lamp drivers **115**A to **115**D sequentially turn on and off once the first to fourth lamps **113**A to **113**D for the upper portion A of the liquid crystal panel **102** for a half period of one vertical sync signal in such a way that the turn-on periods are shifted by a predetermined interval. The shift period between the tune-on periods of the first to fourth lamps **113**A to **113**D may be at least period in which the liquid crystal cells Clc on the sub-sections A**1** to A**4** of the liquid crystal panel **102** corresponding to the lamps **113**A to **113**D charge data voltages. Simultaneously, the first to fourth lamp drivers **115**A to **115**D turn on and off (in detail, after or before) once the fifth to eighth lamps **113**E to **113**H for the lower portion B of the liquid crystal panel **102** together with the first to fourth lamps **113**A to **113**D for the upper portion A of the liquid crystal panel **102**. Therefore, the fifth to eighth lamps **113**E to **113**H are also sequentially turned on such that the turn-on periods are shifted at predetermined interval. In other words, the turn-on periods of the lamps **113**A-**113**D or **113**E-**113**G for the sub-sections A**1**-A**4** or B**1**-B**4** of the liquid crystal panel **102** can be different. Thus, at least one of lamp driving voltages generated by the first to fourth lamp drivers **115**A to **115**D have a different duty cycle from the others.

[0055] In response to the lamp control signal outputted from the timing controller **108**, the first lamp driver **115**A turns off and on the first lamp **113**A for the uppermost sub-section A**1** of the upper portion A of the liquid crystal panel **102** and the fifth lamp **113**E for the uppermost sub-section B**1** of the lower portion B of the liquid crystal panel **102** simultaneously once for a half frame period, or a half period of the vertical sync signal. The first lamp driver **115**A turns off the first and fifth lamps **113**A and **113**E during the periods (high-voltage periods in DW**113**AE of FIG. **3**) in which the data voltages are charging the liquid crystal cells Clc on the uppermost sub-sections A**1** and B**1** of the upper and lower portions A and B of the liquid crystal panel **102**, or during the periods (low-voltage periods in LE**113**AE of FIG. **3**) including predetermined intervals before and after the high-voltage periods. On the other hand, during the periods (low-voltage periods in DW**113**AE of FIG. **3**) when the liquid crystal cell Clc on the uppermost sub-sections A**1** and B**1** of the liquid crystal panel **102** are maintaining the charged data voltages, the first lamp driver **115**A turns on the first and fifth lamps **113**A and **113**E for a predetermined time (high-voltage period in LE**113**AE of FIG. **3**).

[0056] In response to the lamp control signal outputted from the timing controller **108**, the second lamp driver **115**B turns off and on the second lamp **113**B for the second uppermost sub-section A**2** of the upper portion A of the liquid crystal panel **102** and the sixth lamp **113**F for the second uppermost sub-section B**2** of the lower portion B of the liquid crystal panel **102** simultaneously once for a half frame period, or a half period of the vertical sync signal. The second lamp driver **115**B turns off the second and sixth lamps **113**B and **113**F during the periods (high-voltage periods in DW**113**BF of FIG. **3**) when the data voltages are charging liquid crystal cells Clc in the second uppermost sub-sections A**2** and B**2** of the upper and lower portions A and B of the liquid crystal panel **102**, or during the periods (low-voltage periods in LE**113**BF of FIG. **3**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods in which the liquid crystal cell Clc on the second uppermost sub-sections A**2** and B**2** of the upper and lower portions A and B of the liquid crystal panel **102** are maintaining the charged data voltages, the second lamp driver **115**B turns on the second and sixth lamps **113**B and **113**F during the period (high-voltage period in LE**113**BF of FIG. **3**).

[0057] In response to the lamp control signal outputted from the timing controller **108**, the third lamp driver **115**C turns off and on the third lamp **113**C for the second lowermost sub-section A**3** of the upper portion A of the liquid crystal panel **102** and the seventh lamp **113**G for the second lowermost sub-section B**3** of the lower portion B of the liquid crystal panel **102** simultaneously once for a half frame period, or a half period of the vertical sync signal. The third lamp driver **115**C turns off the third and seventh lamps **113**C and **113**G during the periods (high-voltage periods in DW**113**CG of FIG. **3**) in which the data voltages are charging the liquid crystal cells Clc in the second lowermost sub-sections A**3** and B**3** on the upper and lower portions A and B of the liquid crystal panel **102**, or during the periods (low-voltage periods in LE**113**CG of FIG. **3**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods in which the liquid crystal cell Clc on the second lowermost sub-sections A**3** and B**3** of the liquid crystal panel **102** are maintaining the charged data voltages, the third lamp driver **115**C turns on the third and seventh lamps **113**C and **113**G for a predetermined time (high-voltage period in LE**113**CG of FIG. **3**).

[0058] In response to the lamp control signal outputted from the timing controller **108**, the fourth lamp driver **115**D turns off and on the fourth lamp **113**D for the lowermost sub-section A**4** of the upper portion A of the liquid crystal panel **102** and the eighth lamp **113**H for the lowermost sub-section B**4** of the lower portion B of the liquid crystal panel **102** simultaneously once for a half frame period, or a half period of the vertical sync signal. The fourth lamp driver **115**D turns off the fourth and eighth lamps **113**D and **113**H during the periods (high-voltage periods in DW**113**DH of

FIG. **3**) in which the data voltages are charging the liquid crystal cells Clc in the lowermost sub-sections A**4** and B**4** of the upper and lower portions A and B of the liquid crystal panel **102**, or during the periods (low-voltage periods in LE**113**DH of FIG. **3**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods (low-voltage periods in DW**113**DH of FIG. **3**) in which the liquid crystal cells Clc of the lowermost sub-sections A**4** and B**4** of the liquid crystal panel **102** are maintaining the charged data voltages, the fourth lamp driver **115**D turns on the fourth and eighth lamps **113**D and **113**H for a predetermined time (high-voltage period in LE**113**DH of FIG. **3**).

[0059] As can be seen from the timing diagram of FIG. **3**, the first to fourth lamp drivers **115**A to **115**D are controlled by the timing controller **108** to sequentially turn on and off the first to fourth lamps **113**A to **113**D for the upper portion A of the liquid crystal panel **102** together with the fifth to eighth lamps **113**E to **113**H for the lower portion B of the liquid crystal panel **102** to be synchronized at every converted frame period while the data voltages are simultaneously written to the liquid crystal cells Clc in both the upper portion A of the liquid crystal panel **102** and the lower portion B of the liquid crystal panel **102**. In other words, video data and black level data are alternately displayed once on the liquid crystal panel **102** at each frame having frame frequency (the second frame frequency of e.g., 120 Hz) that is twice the frame frequency (e.g., the first frame frequency of 60 Hz) of the video data generated from the external system. Therefore, the LCD according to embodiments of the present invention can display video data quickly on the liquid crystal panel. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed. Further, providing charging data voltages simultaneously to two portions of the liquid crystal panel also prevents an unclear image or image-sticking so that the image is presented quickly. Thus, according to embodiments of the present invention, the LCD can display higher quality images.

[0060] Further, since the lamps for the sub-sections of the upper portion of the liquid crystal panel and the lamps for the sub-sections of the lower portion of the liquid crystal panel can be turned on and off by a single lamp driver, the circuit for driving the lamps can be simplified.

[0061] FIG. **4** is a schematic diagram of an LCD according to a second embodiment of the present invention. Referring to FIG. **4**, the LCD includes a first gate driver **204**A for driving a plurality of left gate lines LGL**1**-LGL**2***k* disposed on the left of the liquid crystal panel **202**, a second gate driver **204**B for driving a plurality of right gate lines RGL**1**-RGL**2***k* disposed on the right of the liquid crystal panel **202**, and a data driver **206** for driving a plurality of data lines DL**1**-DL**2***j* disposed on the liquid crystal panel **202**.

[0062] The left gate lines LGL**1**-LGL**2***k* are arranged on a left portion C of the liquid crystal panel **202** and cross a first j number of data lines DL**1** to DLj arranged in a horizontal direction. The right gate lines RGL**1**-RGL**2***k* are arranged on a right portion D of the liquid crystal panel **202** and cross a second j number of data lines DL(j+1)-DL**2***j* arranged in a horizontal direction. TFTs acting as switching elements are formed at crossings between the data lines DL**1**-DL**2***j* and the left and right gate lines LGL**1**-LGL**2***k* and RGL**2***k*-RGL**2***k*. The TFTs are responsive to scan signals applied on corresponding gate lines GL to switch data voltages supplied from the corresponding data lines DL to liquid crystal cells Clc, which are connected to a common voltage line Vcom. The liquid crystal cells Clc of the liquid crystal panel **202** transmit light proportionally or inversely proportional to an electric potential difference between the data voltages of the data lines DL and the reference voltage, that is, the common voltage Vcom.

[0063] The first gate driver **204**A generates the scan signals for the left gate lines LGL**1**-LGL**2***k* in response to the gate control signals in each period of one vertical sync signal, that is, in each frame period. The scan signals from the first gate driver **204**A enable the first 2k number of left gate lines LGL**1** to LGL**2***k* sequentially once for period of one vertical sync signal. The first 2k number of scan signals is supplied exclusively to the first 2k number of left gate lines LGL**1**-LGL**2***k* arranged on the left portion C of the liquid crystal panel **202** as shifted pulses of gate high voltages VGH. The pulse of the gate high voltage VGH contained in the scan signal has a width equal to the period of one horizontal sync signal.

[0064] The second gate driver **204**B generates the scan signals for the right gate lines RGL**1**-RGL**2***k* in response to the gate control signals in each period of one vertical sync signal, that is, in each frame period. The scan signals from the second gate driver **204**B enable the second 2k number of right gate lines RGL**1** to RGL**2***k* sequentially once for period of one vertical sync signal. The 2k number of scan signals generated from the second gate driver **204**B has the same waveform as the 2k number of scan signals generated from the first gate driver **204**A. Therefore, the right gate lines RGL**1**-RGL**2***k* disposed on the right portion D of the liquid crystal panel **202** are simultaneously enabled or disabled together with the left gate lines LGL disposed at the left portion of the liquid crystal panel **202**.

[0065] The data driver **206** converts R, G and B pixel data corresponding to one line into analog data voltages in response to the data control signals in each period of the horizontal sync signal, and supplies the one-line data voltages to the data lines DL**1**-DL**2***j* arranged on the liquid crystal panel **202**. The data driver **206** outputs the one-line data voltages when the 2k pairs of left and right gate lines LGL**1**-LGL**2***k* and RGL**1**-RGL**2***k* are sequentially enabled as pairs, that is, in each period of one horizontal sync signal. If one pair of the 2k pairs of the left and right gate lines LGL**1**-LGL**2***k* and RGL**1**-RGL**2***k* is enabled by the pulses of the gate high voltage VGH, the TFTs connected to the enabled left and right gate lines LGL and RGL are turned on, so that the data voltages from the corresponding data lines DL are transferred to the corresponding liquid crystal cells Clc. When one pair of the scan signals change from the gate high voltage VGH to the gate low voltage VGL, the turned-on TFTs are turned off, so that the corresponding liquid crystal cells Clc are electrically disconnected from the corresponding data lines DL. The liquid crystal cells Clc are charged with the data voltage supplied from the corresponding data lines DL during the turn-on period of the TFTs, and the charged data voltages are maintained until the corresponding TFTs are turned on again.

[0066] The gate driver **104** and the first and second data drivers **106**A and **106**B write the data voltage to the liquid crystal cells of the liquid crystal panel **102** once for the frame period, that is, for period of the vertical sync signal.

[0067] Referring to FIG. **4**, the LCD includes a timing controller **208** for controlling the first and second gate drivers **204**A and **204**B and the data driver **206**, and a backlight unit **210** for irradiating light onto the liquid crystal panel **202**. The timing controller **208** generates the gate control signals for controlling the first and second gate drivers **204**A and **204**B and the data control signals for controlling the data driver **206** by using vertical/horizontal sync signals (Vsync/Hsync), data enable signal (DE), and clock signal, which are generated from an external system (not shown), such as graphic card of computer system or TV signal decoder module of television receiver. In response to the gate control signals generated from the timing controller **208**, the first and second gate drivers **204**A and **204**B enable the 2k pairs of left and right gate lines LGL**1**-LGL**2***k* and RGL**1**-RGL**2***k* arranged on the left and right portions C and D of the liquid crystal panel **202** to be sequentially driven once for period of one vertical sync signal, that is, for frame period. In response to the data control signals, the data driver **206** supplies the one-line data voltages to the data lines DL**1**-DL**2***j* in a line by line fashion whenever any one pair of the 2k pairs of the left and right gate lines LGL**1**-LGL**2***k* and RGL**1**-RGL**2***k* is enabled.

[0068] In addition, the timing controller **208** arranges the R, G and B pixel data supplied from the external system line by line, and supplies the one-line R, G and B pixel data to the data driver **206** in each period of the horizontal sync signal. The data driver **206** converts the one-line R, G and B pixel data into analog data voltages. The one-line data voltages converted by the data driver **206** are simultaneously supplied to the data lines DL**1**-DL**2***j*.

[0069] The backlight unit **210** includes first to eighth lamps **213**A to **213**H arranged in parallel under the liquid crystal panel **202**. The first to fourth lamps **213**A to **213**D are arranged to correspond to the upper portion A of the liquid crystal panel **202**, while the fifth to eighth lamps **213**E to **213**H are arranged to correspond to the lower portion B of the liquid crystal panel **202**. The first to fourth lamps **213**A to **213**D irradiate light respectively onto sub-sections defined by dividing the upper portion A of the liquid crystal panel **202** by four. For example, the first lamp **213**A irradiates light onto the uppermost sub-section A**1** of the upper portion A of the liquid crystal panel **202** and the fourth lamp **213**D irradiates light onto the lowermost sub-section A**4** of the lower portion A of the liquid crystal panel **202**. Likewise, the fifth to eighth lamps **213**E to **213**H respectively irradiate light onto the sub-sections defined by dividing the lower portion B of the liquid crystal panel **202** by four. For example, the fifth lamp **213**E irradiates light onto the uppermost sub-section B**1** of the lower portion B of the liquid crystal panel **202** and the eighth lamp **213**H irradiates light onto the lowermost sub-section B**4** of the lower portion B of the liquid crystal panel **202**.

[0070] The backlight unit **210** includes first to fourth lamp drivers **215**A to **215**D commonly connected to the timing controller **208**. Each of the first to fourth lamp drivers **215**A to **215**D turns on and off (in detail, after or before) one of the lamps for the upper portion A of the liquid crystal panel **202** and one of the lamps for the lower portion B of the liquid crystal panel **202** simultaneously twice. In response to the lamp control signals outputted from the timing controller **208**, the first to fourth lamp drivers **215**A to **215**D sequentially turn on and off the first to fourth lamps **213**A to **213**D for the upper portion A of the liquid crystal panel **202** for a half period of one vertical sync signal in such a way that the turn-on periods are shifted at a predetermined interval. The shift period between the turn-on periods of the lamps may be a period in which the liquid crystal cells Clc on the one sub-section A**1** to A**4** corresponding to the first to fourth lamp drivers **215**A to **215**D charge the data voltages. Simultaneously, the first to fourth lamp drivers **215**A to **215**D turn on the fifth to eighth lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **202** together with the first to fourth lamps **213**A to **213**D. Therefore, the fifth to eighth lamps **213**E to **213**H are sequentially turned on such that the turn-on periods are shifted at predetermined period for a half period of the vertical sync signal, that is, for a half frame period. In other words, there may be differences between the turn-on periods of the lamps **213**A-**213**D or **213**E-**213**H for the sub-sections A**1**-A**4** or B**1**-B**4**. Thus, at least one of the lamp driving voltages generated by the first to fourth lamp drivers **215**A to **215**D have a different duty cycle from the others.

[0071] In response to the lamp control signal outputted from the timing controller **208**, the first lamp driver **215**A turns on and off the first lamp **213**A for the uppermost sub-section A**1** of the upper portion A of the liquid crystal panel **202** and the fifth lamp **213**E for the uppermost sub-section B**1** of the lower portion B of the liquid crystal panel **202** simultaneously once for a half period of the vertical sync signal, that is, for a half frame period. The first lamp driver **215**A turns off the first and fifth lamps **213**A and **213**E during the data voltage charging periods (high-voltage periods in DW**213**A and DW**213**E of FIG. **5**) in which data voltages are charging the liquid crystal cells Clc on the uppermost sub-sections A**1** and B **1** of the upper and lower portions A and B of the liquid crystal panel **202**, or during the periods (low-voltage periods in LE**213**AE of FIG. **5**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods (low-voltage periods in DW**213**A and DW**213**E of FIG. **5**) in which the liquid crystal cells Clc on the uppermost sub-sections A**1** and B**1** of the liquid crystal panel **202** maintain the charged data voltages, the first lamp driver **215**A turns on the first and fifth lamps **213**A and **213**E for a predetermined time (high-voltage period in LE**213**AE of FIG. **5**).

[0072] In response to the lamp control signal outputted from the timing controller **208**, the second lamp driver **215**B turns on and off the second lamp **213**B for the second uppermost sub-section A**2** of the upper portion A of the liquid crystal panel **202** and the sixth lamp **213**F for the second uppermost sub-section B**2** of the lower portion B of the liquid crystal panel **202** simultaneously once for a half period of the vertical sync signal, that is, for a half frame period. The second lamp driver **215**B turns off the second and sixth lamps **213**B and **213**F during the periods (high-voltage periods in DW**213**B and DW**213**F of FIG. **5**) in which the data voltages are charging the liquid crystal cells Clc in the second uppermost sub-sections A**2** and B**2** of the upper and lower portions A and B of the liquid crystal panel **202**, or during the periods (low-voltage periods in LE**213**BF of FIG. **5**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods in which the liquid crystal cells Clc of the second uppermost sub-sections A**2** and B**2** of the liquid crystal panel **202** maintain the charged data voltages, the second lamp

driver **215**B turns on the second and sixth lamps **213**B and **213**F for a predetermined time (high-voltage period in LE**213**BF of FIG. **5**).

[0073] In response to the lamp control signal outputted from the timing controller **208**, the third lamp driver **215**C turns off and on the third lamp **213**C for the second lowermost sub-section A**3** of the upper portion A of the liquid crystal panel **202** and the seventh lamp **213**G for the second lowermost sub-section B**3** of the lower portion B of the liquid crystal panel **202** simultaneously once for a half period of the vertical sync signal, that is, for a half frame period. The third lamp driver **215**C turns off the third and seventh lamps **213**C and **213**G during the periods (high-voltage periods in DW**213**C and DW**213**G of FIG. **5**) in which the data voltages are charging the liquid crystal cells Clc in the second lowermost sub-sections A**3** and B**3** of the upper and lower portions A and B of the liquid crystal panel **202**, or during the periods (low-voltage periods in LE**213**CG of FIG. **5**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods in which the liquid crystal cells Clc of the second lowermost sub-sections A**3** and B**3** of the liquid crystal panel **202** maintain the charged data voltages, the third lamp driver **215**C turns on the third and seventh lamps **213**C and **213**G for a predetermined time (high-voltage period in LE**213**CG of FIG. **5**).

[0074] In response to the lamp control signal outputted from the timing controller **108**, the fourth lamp driver **215**D turns off and on the fourth lamp **213**D for the lowermost sub-section A**4** of the upper portion A of the liquid crystal panel **202** and the eighth lamp **213**H for the lowermost sub-section B**4** of the lower portion B of the liquid crystal panel **202** simultaneously once for a half period of the vertical sync signal, that is, for a half frame period. The fourth lamp driver **215**D turns off the fourth and eighth lamps **213**D and **213**H during the periods (high-voltage periods in DW**213**D and DW**213**H of FIG. **5**) in which the data voltages are charging the liquid crystal cells Clc in the lowermost sub-sections A**4** and B**4** of the upper and lower portions A and B of the liquid crystal panel **202**, or during the periods (low-voltage periods in LE**213**DH of FIG. **5**) including predetermined intervals before and after the data voltage charging periods. On the other hand, during the periods (low-voltage periods in DW**213**D and DW**213**H of FIG. **5**) in which the liquid crystal cells Clc of the lowermost sub-sections A**4** and B**4** of the liquid crystal panel **202** maintain the charged data voltages, the fourth lamp driver **215**D turns on the fourth and eighth lamps **213**D and **213**H for a predetermined time (high-voltage period in LE**213**DH of FIG. **5**).

[0075] As can be seen from the timing diagram of FIG. **5**, the first to fourth lamp drivers **215**A to **215**D sequentially turn on and off twice the first to fourth lamps **213**A to **213**D corresponding to the upper portion A of the liquid crystal panel **202** and the fifth to eighth lamps **213**E to **213**H corresponding to the lower portion B of the liquid crystal panel **102** in such a way that the first to fourth lamps **213**A to **213**D are synchronized with the fifth to eighth lamps **213**E to **213**H in each frame period while lines of liquid crystal cells Clc are sequentially written one at a time. Thus, video data and black level data are alternately displayed twice on the liquid crystal panel **202** at a frame frequency (the second frame frequency of e.g., 120 Hz) that is twice the frame frequency (e.g., the first frame frequency of 60 Hz) of the video data generated from the external system. Therefore, according to embodiments of the present invention, the LCD can respond to the video data quickly. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed.

[0076] In addition, the lamps for the sub-sections of the upper portion of the liquid crystal panel and the lamps for the sub-sections of the lower portion of the liquid crystal panel are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0077] In the LCD according to embodiments of the present invention, the gate line for enabling the TFTs for one line is divided into the left gate line and the right gate line, so that the left gate line and the right gate line are individually driven. Therefore, the propagation delay time of the scan signal in the gate line is reduced. Consequently, the LCD according to embodiments of the present invention can respond to the image change rapidly, thereby improving the image quality.

[0078] FIG. **6** is a schematic diagram of a Line On Glass (LOG) type LCD according to a third embodiment of the present invention. Referring to FIG. **6**, the LCD includes a liquid crystal panel **302** for displaying an image, a plurality of data tape carrier packages (TCPs) **318***a* to **318***c* connected between the liquid crystal panel **302** and a data printed circuit board (PCB) **320**, a plurality of gate TCPs **316***a* to **316***d* provided at one side and another side of the liquid crystal panel **302**, a plurality of data driver ICs **306***a* to **306***c* mounted on the data TCPs **318***a* to **318***c*, and a plurality of gate driver ICs **304***a* to **304***d* mounted on the gate TCPs **316***a* to **316***d*. The liquid crystal panel **302** includes a lower substrate **311**, an upper substrate **313**, and a liquid crystal (not shown) injected between the lower substrate **311** and the upper substrate **313**. The lower substrate **311** and the upper substrate **313** are transparent insulation substrates. Among the plurality of gate TCPs **316***a* to **316***d*, the first and second gate TCPs **316***a* and **316***b* are provided at one side of the liquid crystal panel **302**. A first LOG type signal line group **314***a* is disposed on the lower substrate **311** to serially connect the first and second gate driver ICs **304***a* and **304***b* mounted on the first and second gate TCPs **316***a* and **316***b*. In addition, the third and fourth gate TCPs **316***c* and **316***d* are provided at another side of the liquid crystal panel **302**. A second LOG type signal line group **314***b* is disposed on the lower substrate **311** to serially connect the third and fourth gate driver ICs **304***c* and **304***d* mounted on the third and fourth TCPs **316***c* and **316***d*.

[0079] The liquid crystal panel **302** includes a plurality of left gate lines LGL**1**-LGL**2***k* arranged at a left portion C of the liquid crystal panel **302** in a vertical direction, and a plurality of right gate lines RGL**1**-RGL**2***k* arranged at a right portion D of the liquid crystal panel **302** in a vertical direction. The left gate lines LGL**1**-LGL**2***k* are crossed with a first j number of data lines DL**1**-DLj disposed at the left portion C of the liquid crystal panel **202**, and the right gate lines RGL**1**-RGL**2***k* are crossed with a second j number of data lines DL(k+1)-DL**2***j* arranged at the right portion of the liquid crystal panel **202** in a horizontal direction. The left gate lines LGL**1**-LGL**2***k* are sequentially driven by the first and second gate driver ICs **304***a* and **304***b*, and the right gate lines RGL**1**-RGL**2***k* are sequentially driven by the third and fourth gate driver ICs **304***c* and **304***d* in such a way that they are synchronized with the left gate lines LGL**1**-LGL**2***k*. The data lines DL**1**-DL**2***j* are all charged with data voltages when

one pair of the left gate line LGL and the right gate line RGL are enabled. The gate lines LGL**1**-LGL**2***k* and RGL**1**-RGL**2***k* and the data lines DL **1**-DL**2***j* arranged on the liquid crystal panel **302** are driven in the same manner as those of FIG. **4**. In other words, the liquid crystal panel **302**, the first to fourth gate driver ICs **304***a* to **304***d*, and the first to third data driver ICs **306***a* to **306***c* connected to thereto are driven in the same manner as those of FIG. **4**. Therefore, detailed description about the liquid crystal panel **302**, the first to fourth gate driver ICs **304***a* to **304***d*, and the first to third data driver ICs **306***a* to **306***c* will be omitted.

[0080] The LOG type LCD of FIG. **6** includes first to eighth lamps **213**A to **213**H arranged in parallel under the liquid crystal panel **302**, a timing controller **308** mounted on the data PCB **320**, and a lamp driver **215**. The first to fourth lamps **213**A to **213**D are arranged to correspond to the upper portion A of the liquid crystal panel **302**, while the fifth to eighth lamps **213**E to **213**H are arranged to correspond to the lower portion B of the liquid crystal panel **302**. The first to fourth lamps **213**A to **213**D respectively irradiate light onto sub-sections defined by dividing the upper portion A of the liquid crystal panel **302** by four. For example, the first lamp **213**A irradiates light onto the uppermost sub-section A**1** in the upper portion A of the liquid crystal panel **302**, and the fourth lamp **213**D irradiates light onto the lowermost sub-section A**4** in the lower portion A of the liquid crystal panel **302**. Likewise, the fifth to eighth lamps **213**E to **213**H respectively irradiate light onto sub-sections defined by dividing the lower portion B of the liquid crystal panel **302**. For example, the fifth lamp **213**E irradiates light onto the uppermost sub-section B**1** of the lower portion B of the liquid crystal panel **302**, and the eighth lamp **213**H irradiates light onto the lowermost sub-section B**4** of the lower portion B of the liquid crystal panel **302**.

[0081] In response to the lamp control signals outputted from the timing controller **308**, the lamp driver **215** turns on and off the lamps **213**A to **213**D for the upper portion A of the liquid crystal panel **302** and the lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **302** simultaneously and sequentially once for a half period of the vertical sync signal, that is, a half frame period. The first to fourth lamps **213**A to **213**D are sequentially turned off and on in such a way that their turn-on periods are shifted at predetermined interval. The shift period between the turn-on periods of the first to fourth lamps **213**A to **213**D corresponds to the periods in which the liquid crystal cells Clc on one sub-section charge data voltages. The fifth to eighth lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **302** are simultaneously turned on and off together with the first to fourth lamps **213**A to **213**D, respectively. Therefore, the fifth to eighth lamps **213**E to **213**H are sequentially turned on once, such that the turn-on periods are shifted at predetermined interval for a half period of the vertical sync signal, that is, for a half frame period. To drive the first to eighth lamps **213**A to **213**H in the above-described manner, the lamp driver **215** includes the first to fourth lamp drivers **215**A to **215**D of FIG. **4**. Since the lamp driver **215** and the first to eighth lamps **213**A to **213**H are similar to those described in the detailed description of FIG. **4**, a detailed description about the lamp driver will be omitted.

[0082] As can be seen from the timing diagram of FIG. **5**, the timing controller **308** controls the gate driver ICs **304***a* to **304***d* and the data drivers **306***a* to **306***c* for sequentially writing data voltages, based on a line, to all liquid crystal cells Clc of the liquid crystal panel **302** once in every frame, and controls the lamp driver **215** for turning on and off the first to eighth lamps **213**A to **213**H twice. Since the timing controller **308** is similar to the one described in the detailed description of FIG. **4**, detailed description about the timing controller **308** will be omitted.

[0083] As can be seen from the timing diagram of FIG. **5**, the LOG type LCD of FIG. **6** sequentially turns on and off twice the first to fourth lamps **213**A to **213**D for the upper portion A of the liquid crystal panel **302** and the fifth to eighth lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **302** in such a way that the first to fourth lamps **213**A to **213**D are synchronized with the fifth to eighth lamps **213**E to **213**H, during one frame period in which the data are written once to all the liquid crystal cells Clc of the liquid crystal panel **302**. In other words, video data and black level data are alternately displayed on the liquid crystal panel **302** at the frame frequency (the second frame frequency of e.g., 120 Hz) that is twice the frame frequency (e.g., the first frame frequency of 60 Hz) of the video data generated from the external system. Therefore, the LOG type LCD according to embodiments of the present invention can respond to the video data quickly. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed.

[0084] In addition, the lamps for the sub-sections of the upper portion and the lamps for the sub-sections of the lower portion are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0085] In the LOG type LCD according to the third embodiment, the gate line for enabling the TFTs for one line is divided into the left gate line and the right gate line, so that the left gate line and the right gate line are individually driven. Therefore, the propagation delay time of the scan signal in the gate line is reduced. Consequently, the LOG type LCD according to embodiments of the present invention can respond to the image change rapidly, thereby improving the image quality.

[0086] FIG. **7** is a schematic diagram of an LCD according to a fourth embodiment of the present invention. Referring to FIG. **7**, the LCD according to the fourth embodiment of the present invention includes a gate driver **404** for driving a plurality of gate lines GL**1**-GL**2***k* disposed on the liquid crystal panel **402**, and a data driver **406** for driving a plurality of data lines DL**1**-DL**2***j* disposed on the liquid crystal panel **402**.

[0087] The gate lines GL**1**-GL**2***k* are arranged on the liquid crystal panel **402** and cross the data lines DL**1** to DL**2***j* arranged in a horizontal direction. TFTs acting as switching elements are formed at crossings between the data lines DL**1**-DL**2***j* and the gate lines GL**1**-GL**2***k*. In response to scan signals applied on the corresponding gate lines GL, the TFTs switch data voltages supplied from the corresponding data lines DL to liquid crystal cells Clc connected to common voltage lines Vcom. The liquid crystal cells Clc of the liquid crystal panel **402** transmit light proportionally to a potential difference between the data voltages of the data lines DL and the reference voltage, that is, the common voltage Vcom.

[0088] The gate driver **404** generates the scan signals supplied to the gate lines GL**1**-GL**2***k* in response to the gate control signals in each period of one vertical sync signal, that is, in each frame period. The scan signals from the gate

driver **404** enable a 2k number of gate lines GL**1** to GL**2***k* to be sequentially driven once for period of one vertical sync signal. To this end, the 2k number of scan signals supplied to the 2k number of the gate lines GL**1**-GL**2***k* arranged on the liquid crystal panel **402** exclusively has shifted pulses of gate high voltage VGH. The pulse of the gate high voltage VGH contained in the scan signal has a width equal to the period of one horizontal sync signal.

[0089] The data driver **406** converts R, G and B pixel data corresponding to one line into analog data voltages in response to the data control signals in each period of the horizontal sync signal, and supplies the one-line data voltages to the data lines DL**1**-DL**2***j* arranged on the liquid crystal panel **402**. Specifically, the data driver **406** outputs the one-line data voltages whenever any one of the 2k number of the gate lines GL**1**-GL**2***k* is enabled, that is, in each period of one horizontal sync signal. When one of the gate lines GL**1**-GL**2***k* is enabled by the pulse of the gate high voltage VGH, the TFTs connected to the enabled gate lines GL are turned on, so that the data voltages from the corresponding data lines DL are transferred to the corresponding liquid crystal cells Clc. When the scan signal changes from the gate high voltage VGH to the gate low voltage VGL, the turned-on TFT is turned off, so that the corresponding liquid crystal cell Clc is electrically disconnected from the corresponding data line DL. The liquid crystal cell Clc charges the data voltage supplied from the corresponding data line DL during the turn-on period of the TFT, and the charged data voltage is maintained until the corresponding TFT is turned on again.

[0090] The gate driver **404** and the data driver **406** write once the data voltage to the liquid crystal cells of the liquid crystal panel **402** in each frame period, that is, in each period of the vertical sync signal.

[0091] Referring to FIG. **7**, the LCD includes a timing controller **408** for controlling the gate driver **404** and the data driver **406**, and a backlight unit **410** for irradiating light onto the liquid crystal panel **402**. The timing controller **408** generates the gate control signals for controlling the gate driver **404** and the data control signals for controlling the data driver **406** by using vertical/horizontal sync signals (Vsync/Hsync), data enable signal (DE), and clock signal, which are generated from an external system (not shown), such as graphic card of computer system or TV signal decoder module of television receiver. In response to the gate control signals generated from the timing controller **408**, the gate driver **404** sequentially drives the 2k number of the gate lines GL**1**-GL**2***k* arranged on the liquid crystal panel **402**. In response to the data control signals generated from the timing controller **408**, the data driver **406** supplies the one-line data voltages to the data lines DL**1**-DL**2***j* line by line.

[0092] The timing controller **408** also arranges the R, G and B pixel data supplied from the external system in line by line fashion, and supplies the one-line R, G and B pixel data to the data driver **406** in each period of the horizontal sync signal. Therefore, the data driver **406** converts the one-line R, G and B pixel data into analog data voltages. The one-line data voltages converted by the data driver **406** are simultaneously supplied to the data lines DL**1**-DL**2***j*.

[0093] Like the backlight unit **210** of FIG. **4**, the backlight unit **410** includes first to eighth lamps **213**A to **213**H and first to fourth lamp drivers **215**A to **215**D. The first to fourth lamps **213**A to **213**D are arranged to correspond to the upper portion A of the liquid crystal panel **402** while the fifth to eighth lamps **213**E to **213**H are arranged to correspond to the lower portion B of the liquid crystal panel **402**. The first to fourth lamps **213**A to **213**D respectively irradiate light onto the sub-sections defined by dividing the upper portion A of the liquid crystal panel **402** by four. For example, the first lamp **213**A irradiates light onto the uppermost sub-section A**1** of the upper portion A of the liquid crystal panel **402**, and the fourth lamp **213**D irradiates light onto the lowermost sub-section A**4** of the lower portion A of the liquid crystal panel **402**. Likewise, the fifth to eighth lamps **213**E to **213**H respectively irradiate light onto sub-sections defined by dividing the lower portion B of the liquid crystal panel **402** by four. In other words, the fifth lamp **213**E irradiates light onto the uppermost sub-section B**1** of the lower portion B of the liquid crystal panel **402**, and the eighth lamp **213**H irradiates light onto the lowermost sub-section B**4** of the lower portion B of the liquid crystal panel **402**.

[0094] In response to the lamp control signals outputted from the timing controller **408**, the first to fourth lamp drivers **215**A to **215**D simultaneously and sequentially turn off and on twice the lamps **213**A to **213**D for the upper portion A of the liquid crystal panel **402** together with the lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **402**, for period of one vertical sync signal. In response to the lamp control signals outputted from the timing controller **208**, the first to fourth lamp drivers **215**A to **215**D sequentially turn off and on once the first to fourth lamps **213**A to **213**D in each half period of the vertical sync signal, that is, in each half frame period, in such a way that the turn-on periods are shifted at predetermined interval. The shift period between the turn-on periods of the first to fourth lamps **213**A to **213**D may be period in which the liquid crystal cell Clc on sub-sections A**1** to A**4** of the liquid crystal panel **402** charge the data voltages. Simultaneously, the fifth to eighth lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **402** are turned on together with the first to fourth lamps **213**A to **213**D, respectively. Therefore, the fifth to eighth lamps **213**E to **213**H are sequentially turned on once for a half period of the vertical sync signal, that is, for a half frame period, in such a way that the turn-on periods are sequentially shifted at predetermined interval. In other words, there may be differences between the turn-on periods of the lamps **213**A-**213**D or **213**E-**213**H for the sub-sections A**1**-A**4** or B**1**-B**4** of the liquid crystal panel **402**. Thus, at least one of the lamp driving voltages generated by the first to fourth lamp drivers **215**A to **215**D has a different duty cycle from the others. Since the first to fourth lamp drivers **215**A to **215**D and the first to eighth lamps **213**A to **213**H are similar to those described with reference to FIG. **4**, their detailed description will be omitted.

[0095] As can be seen from the timing diagram of FIG. **5**, the LOG type LCD of FIG. **7** sequentially turns on and off twice the first to fourth lamps **213**A to **213**D for the upper portion A of the liquid crystal panel **402** and the fifth to eighth lamps **213**E to **213**H for the lower portion B of the liquid crystal panel **402** in such a way that the first to fourth lamps **213**A to **213**D are synchronized with the fifth to eighth lamps **213**E to **213**H, during one frame period in which the video data is written one at a time to all the liquid crystal cells Clc of the liquid crystal panel **402**. In other words, video data and black level data are alternately displayed on the liquid crystal panel **402** at a frame frequency (the second frame frequency of e.g., 120 Hz) that is

twice the frame frequency (e.g., the first frame frequency of 60 Hz) of the video data generated from the external system. Therefore, the LOG type LCD according to embodiments of the present invention can respond to the video data quickly. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed. Further, alternating the display of video data and black level data twice on the liquid crystal panel also prevents an unclear image or image-sticking so that the image is presented quickly. Consequently, the LCD according to embodiments of the present invention improves image quality with minimizing a reduction of brightness.

[0096] In addition, the lamps for the sub-sections of the upper portion of the liquid crystal panel and the lamps for the sub-sections of the lower portion of the liquid crystal panel are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0097] FIG. **8** is a schematic diagram of an LCD according to a fifth embodiment of the present invention. The LCD according to the fifth embodiment of the present invention is similar to the LCD according to the LCD of FIG. **2**, except that the data converter **110** is removed and the timing controller **108** directly receives the video data from a system (not shown) such as graphic card of computer system or TV signal decoder module of television receiver. Unlike the LCD of FIG. **2**, the liquid crystal panel **102** and the lamps **113**A to **113**H included in the LCD of FIG. **8** operate at a frame frequency (e.g., 60 Hz) of an original video data. In addition, the liquid crystal panel **102** and the lamps **113**A to **113**H can be selectively driven in a first driving mode or a second driving mode. In the first driving mode, the LCD of FIG. **8** is driven according to the timing of FIGS. **9**A and **9**B. In the second driving mode, the LCD of FIG. **8** is driven according to the timing of FIGS. **10**A and **10**B. For convenience, the operation of the LCD in the second driving mode will be referred to as a sixth embodiment of the present invention. The LCD of FIG. **8** will be described below in detail according to the driving modes.

[0098] Referring to FIG. **9**A, the gate driver **104** sequentially enables once the gate lines GL**1**-GLk on the upper portion A of the liquid crystal panel **102** in each frame period of the video data, that is, in each period (1/60 sec) of the vertical sync signal. The gate driver **104** sequentially enables once the gate lines GL(k+1)-GL**2***k* on the lower portion B of the liquid crystal panel **102** to be driven in synchronization with the gate lines GL**1**-GLk. For example, the gate driver **104** enables the first gate line GL**1** and the $(k+1)^{th}$ gate line GL(k+1) simultaneously for two periods of the horizontal sync signal, enables the second gate line GL**2** and the $(k+2)^{th}$ gate line GL(k+2) simultaneously for two periods of the horizontal sync signal, and enables the third gate line GL**3** and the $(k+3)^{th}$ gate line GL(k+3) simultaneously for two periods of the horizontal sync signal. In this way, the k^{th} gate line GLk and the $2k^{th}$ gate line GL**2***k* are simultaneously enabled for the last two periods of the horizontal sync signal. In other words, the gate driver **104** drives k pairs of a first k number of gate lines GL**1**-GLk for the upper portion A of the liquid crystal panel **102** and a second k number of gate lines GL(k+1)-GL**2***k* for the lower portion B of the liquid crystal panel **102** by one pair for two periods of the horizontal sync signal. In this end, as illustrated in FIG. **9**A, the gate driver **104** supplies the 2k number of the scan signals SGL**1**-SGL**2***k* to the 2k number of the gate lines GL**1**-GL**2***k* on the liquid crystal panel **102** in each period of the vertical sync signal, that is, in each frame period, respectively. The 2k number of the scan signals SGL**1**-SGL**2***k* is divided into a first scan signal group SGL**1**-SGLk supplied to the first k number of the gate lines GL**1**-GLk for the upper portion A of the liquid crystal panel **102**, and a second scan signal group SGL(k+1)-SGL**2***k* supplied to the second k number of the gate lines GL(k+1)-GL**2***k* for the lower portion B of the liquid crystal panel **102**. The first scan signal group SGL**1**-SGLk has a pulse of gate high voltage VGH with a phase and a width equal to those of the second scan signal group SGL(k+1)-SGL**2***k*. The pulse width of the gate high voltage VGH corresponds to two periods of the horizontal sync signal. The pulse of the gate high voltage VGJ contained in the first scan signal group SGL is sequentially shifted by its own width (e.g., two periods of the horizontal sync signal) as the gate lines GL on the upper portion A of the liquid crystal panel **102** move downward. Likewise, the pulse of the gate high voltage VGH contained in the second scan signal group SGL(k+1)-SGL**2***k* is sequentially shifted by its own width (e.g., two periods of the horizontal sync signal) as the gate lines on the lower portion B of the liquid crystal panel **102** move downwards.

[0099] The first data driver **106**A converts R, G and B pixel data corresponding to one line into analog data voltages in response to the data control signals, and supplies the one-line data voltages to the upper data lines UDL**1**-UDLm arranged on the upper portion A of the liquid crystal panel **102**. The first data driver **106**A outputs the one-line data voltages whenever any one of the k number of the gate lines GL**1**-GLk on the upper portion A of the liquid crystal panel **102** is enabled. The period in which the first data driver **106**A supplies the one-line data voltages to the upper data lines UDL**1**-UDLm corresponds to two periods of the horizontal sync signal having the width equal to that of the gate high pulse enabling the gate lines GL**1**-GLk arranged on the upper portion A of the liquid crystal panel **102**.

[0100] Likewise, the second data driver **106**B converts R, G and B pixel data corresponding to one line into analog data voltages in response to the data control signals, and supplies the one-line data voltages to the lower data lines LDL**1**-LDLm arranged on the lower portion B of the liquid crystal panel **102**. The second data driver **106**B outputs the one-line data voltages to the lower data lines LDL**1**-LDLm whenever any one of the gate lines GL(k+1)-GL**2***k* is enabled. The period in which the second data driver **106**B supplies the one-line data voltages to the lower data lines LDL**1**-LDLm corresponds to two periods of the horizontal sync signal having the width equal to that of the gate high pulse enabling the gate lines GL(k+1)-GL**2***k* arranged on the lower portion B of the liquid crystal panel **102**.

[0101] Since the gate lines GL(k+1)-GL**2***k* are simultaneously enabled together with the gate lines GL **1**-GLk, the one-line data voltages from the first data driver **106**A and the one-line data voltages from the second data driver **106**B are simultaneously supplied to the upper data lines UDL**1**-UDLm and the lower data lines LDL**1**-LDLm, respectively. Accordingly, when the one-line liquid crystal cells for the upper portion A of the liquid crystal panel **102** charge the data voltages, the one-line liquid crystal cells for the lower portion B of the liquid crystal panel **102** charge the data voltages. In other words, the liquid crystal cells on the liquid crystal panel **102** are charged with the data voltages two lines by two lines for two periods of the horizontal sync signal by the first and second data drivers **106**A and **106**B

and the gate driver **104**. Therefore, the liquid crystal cells Clc on the first and second sub-sections A**1** and B**1** of the upper and lower portions A and B of the liquid crystal panel **102** are simultaneously charged with the data voltages. Then, the data voltages are written to the liquid crystal cells Clc on the second sub-sections A**2** and B**2** of the upper and lower portions A and B of the liquid crystal panel **102**. Next, the data voltages are simultaneously written to the third sub-sections A**3** and B**3** of the upper and lower portions A and B of the liquid crystal panel **102**. Finally, the data voltages are simultaneously written to the liquid crystal cells on the fourth sub-sections A**4** and B**4** of the upper and lower portions A and B of the liquid crystal panel **102**.

[0102] When any one of the first k number of the gate lines GL**1**-GLk on the upper portion A of the liquid crystal panel **102** is enabled for two periods of the horizontal sync signal by the pulse of the gate high voltage VGH, TFTs connected to the enabled gate lines are turned on so that the data voltages from the upper data lines UDL are transferred to the corresponding liquid crystal cells Clc. When the scan signal changes from the gate high voltage VGH to the gate low voltage VGL, the turned-on TFTs on the upper portion A of the liquid crystal panel **102** are turned off so that the liquid crystal cells Clc are electrically disconnected from the upper data lines UDL. The liquid crystal cells Clc charge the data voltages supplied from the upper data lines UDL during two periods of the horizontal sync signal, that is, during the period in which the TFTs are turned on. Then, the charged data voltages are maintained until the TFTs are turned on again in a next frame period.

[0103] Likewise, when any one of the second k number of the gate lines GL(k+1)-GL**2***k* on the lower portion B of the liquid crystal panel **102** is enabled by the pulse of the gate high voltage VGH, TFTs connected to the enabled gate lines are turned on so that the data voltages from the lower data lines LDL are transferred to the corresponding liquid crystal cells Clc. When the scan signal changes from the gate high voltage VGH to the gate low voltage VGL, the turned-on TFTs on the lower portion B of the liquid crystal panel **102** are turned off so that the liquid crystal cells Clc are electrically disconnected from the lower data lines LDL. The liquid crystal cells Clc charge the data voltages supplied from the lower data lines LDL during two periods of the horizontal sync signal, that is, during the period in which the TFTs are turned on. Then, the charged data voltages are maintained until the TFTs are turned on again in a next frame period.

[0104] The first and fourth lamp drivers **115**A to **115**D of the backlight unit **112** commonly connected to the timing controller **108** sequentially turn on and off the lamps **113**A to **113**D of the sub-sections A**1** to A**4** of the upper portion A of the liquid crystal panel **102** to be synchronized with the lamps **113**E to **113**H of the sub-sections B**1** to B**4** of the lower portion B of the liquid crystal panel **102**. Each of the lamps **113**A to **113**D is turned on and off once in each frame period. The frame period corresponds, for example, to a period of the vertical sync signal. To this end, the first to fourth lamp drivers **115**A to **115**D control the lamp driving voltages to be supplied to the lamps **113**A to **113**H. The duty cycle of respective the lamp driving voltages (that is, the ratio of the on-time to the off-time) can be different. The operation and effect of the first to fourth lamp drivers **115** will be described in detail with reference to FIG. **9**B.

[0105] Referring to FIG. **9**B, the waveform "DW**113**AE" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the first sub-sections A**1** and B **1** of the upper and lower portions A and B of the liquid crystal panel **102**. During the period DW**113**AE, the liquid crystal cells Clc arranged on the first sub-sections A**1** and B**1** of the upper and lower portions A and B of the liquid crystal panel **102** charge the data voltages for the first ¼ period of the frame period, that is, for DWP period, and maintain the charged data voltages for the remaining ¾ period of the frame period. The waveform "DW**113**BF" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the second sub-sections A**2** and B**2** of the upper and lower portions A and B of the liquid crystal panel **102**. The liquid crystal cells Clc on the second sub-sections A**2** and B**2** of the liquid crystal panel **102** charge the data voltages for the second ¼ period of the frame period, that is, for DWP period, and maintain the charged data voltages for the ½ period of the frame period and a ¼ period of a next frame period. The waveform "DW**113**CG" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the third sub-sections A**3** and B**3** of the upper and lower portions A and B of the liquid crystal panel **102**. The liquid crystal cells Clc on the third sub-sections A**3** and B**3** of the liquid crystal panel **102** charge the data voltages for the third ¼ period of the frame period, that is, for a DWP period, and maintain the charged data voltages for the remaining ¼ period of the frame period and a first ½ period of the next frame period. The waveform "DW**113**DH" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the fourth sub-sections A**4** and B**4** of the upper and lower portions A and B of the liquid crystal panel **102**. The liquid crystal cells Clc on the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** charge the data voltages for the last ¼ period of the frame period, that is, for a DWP period, and maintain a ¾ period of the next frame period.

[0106] The first lamp driver **115**A simultaneously supplies the first lamp driving voltage LE**113**AE of FIG. **9**B to the first lamp **113**A and the fifth lamp **113**E for the first sub-sections A**1** and B**1** of the liquid crystal panel **102**. The first lamp driving voltage LE**113**AE generated from the first lamp driver **115**A has a low voltage level during the period DWP in which the data voltages are written to the liquid crystal cells Clc on the first sub-sections A**1** and B**1** of the liquid crystal panel **102**, and has a high voltage level during the period LEP in which the liquid crystal cells Clc on the first sub-sections A**1** and B**1** of the liquid crystal panel **102** maintain the data voltages. The high voltage level period LEP of the first lamp driving voltage LE**113**AE may be shortened according to an amount of brightness in the first sub-sections A**1** and B**1** of the liquid crystal panel **102**. The first and fifth lamps **113**A and **113**E commonly responding to the first lamp driving voltage LE**113**AE outputted from the first lamp driver **115**A are simultaneously turned off during the period in which the liquid crystal cells Clc of the first sub-sections A**1** and B**1** of the liquid crystal panel **102** charge the data voltages, and are turned on in the period in which the liquid crystal cells Clc on the first sub-sections A**1** and B**1** of the liquid crystal panel **102** maintain the charged data voltages, so that light is irradiated onto the first sub-sections A**1** and B**1** of the liquid crystal panel **102**.

[0107] The second lamp driver **115**B simultaneously supplies the second lamp driving voltage LE**113**BF of FIG. **9**B

to the second lamp **113**B and the sixth lamp **113**F for the second sub-sections A**2** and B**2** of the liquid crystal panel **102**. The second lamp driving voltage LE**113**BF generated from the second lamp driver **115**B has a low voltage level during the period DWP in which the data voltages are written to the liquid crystal cells Clc on the second sub-sections A**2** and B**2** of the liquid crystal panel **102**, and has a high voltage level during the period LEP in which the liquid crystal cells Clc on the second sub-sections A**2** and B**2** of the liquid crystal panel **102** maintain the data voltages. The high voltage level period LEP of the second lamp driving voltage LE**113**BF may be shortened according to an amount of brightness in the second sub-sections A**2** and B**2** of the liquid crystal panel **102**. The second and sixth lamps **113**B and **113**F commonly responding to the second lamp driving voltage LE**113**BF outputted from the second lamp driver **115**B are simultaneously turned off during the period in which the liquid crystal cells Clc on the second sub-sections A**2** and B**2** of the liquid crystal panel **102** charge the data voltages, and are turned on in the period in which the liquid crystal cells Clc on the second sub-sections A**2** and B**2** of the liquid crystal panel **102** maintain the charged data voltages, so that light is irradiated onto the second sub-sections A**2** and B**2** of the liquid crystal panel **102**.

[0108] The third lamp driver **115**C simultaneously supplies the third lamp driving voltage LE**113**CG of FIG. **9**B to the third lamp **113**C and the seventh lamp **113**G for the third sub-sections A**3** and B**3** of the liquid crystal panel **102**. The third lamp driving voltage LE**113**CG generated from the third lamp driver **115**C has a low voltage level during the period DWP in which the data voltages are written to the liquid crystal cells Clc on the third sub-sections A**3** and B**3** of the liquid crystal panel **102**, and has a high voltage level during the period LEP in which the liquid crystal cells Clc on the third sub-sections A**3** and B**3** of the liquid crystal panel **102** maintain the data voltages. The high voltage level period LEP of the third lamp driving voltage LE**113**CG may be shortened according to an amount of brightness in the third sub-sections A**3** and B**3** of the liquid crystal panel **102**. The third and seventh lamps **113**C and **113**G commonly responding to the third lamp driving voltage LE**113**CG outputted from the third lamp driver **115**C are simultaneously turned off during the period in which the liquid crystal cells Clc on the third sub-sections A**3** and B**3** of the liquid crystal panel **102** charge the data voltages, and are turned on in the period in which the liquid crystal cells Clc on the third sub-sections of the liquid crystal panel **102** maintain the charged data voltages, so that light is irradiated onto the third sub-sections A**3** and B**3** of the liquid crystal panel **102**.

[0109] The fourth lamp driver **115**D simultaneously supplies the fourth lamp driving voltage LE**113**DH of FIG. **9**B to the fourth lamp **113**D and the eighth lamp **113**H for the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**. The fourth lamp driving voltage LE**113**DH generated from the fourth lamp driver **115**D has a low voltage level during the period DWP in which the data voltages are written to the liquid crystal cells Clc on the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**, and has a high voltage level during the period LEP in which the liquid crystal cells Clc on the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** maintain the data voltages. The high voltage level period LEP of the four lamp driving voltage LE**113**DH may be shortened according to an amount of brightness in the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**. The fourth and eighth lamps **113**D and **113**H commonly responding to the fourth lamp driving voltage LE**113**DH outputted from the fourth lamp driver **115**D are simultaneously turned off during the period in which the liquid crystal cells Clc of the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** charge the data voltages, and are turned on in the period in which the liquid crystal cells Clc on the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** maintain the charged data voltages, so that light is irradiated onto the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**.

[0110] To drive the liquid crystal panel **102** and the lamps **113**A to **113**H as illustrated in FIGS. **9**A and **9**B, the timing controller **108** supplies the gate control signal to the gate driver **104**, the data control signal to the first and second data drivers **106**A and **106**B, and the lamp control signal to the first to fourth lamp drivers **115**A to **115**D. In addition, the timing controller **108** divides two-line pixel data to the first and second data drivers **106**A and **106**B for two periods of the horizontal sync signal. In other words, the timing controller **108** supplies one-line pixel data to the first data driver **106**A, and another one-line pixel data to the second data driver **106**B for two periods of the horizontal sync signal. To this end, the timing controller **108** responds to vertical/horizontal sync signals (Vsync/Hsync), data enable signal (DE), clock signal, and video data, which are generated from an external system (not shown), such as graphic card of computer system or TV signal decoder module of television receiver. The timing controller **108** generates the gate control signals for the gate driver **104**, the data control signals for the first and second data drivers **106**A and **106**B, and the lamp control signals for the first to fourth lamp drivers **113**A to **113**D, by using the vertical/horizontal sync signals (Vsync/Hsync), the data enable signal (DE), and the clock signal. In addition, the timing controller **108** arranges the R, G and B pixel data supplied from the external system into a line by line R, G and B pixel data, and supplies the one-line R, G and B pixel data to the first and second data drivers **106**A and **106**B in each two period of the horizontal sync signals. Therefore, the first data driver **106**A converts the one-line R, G and B pixel data into analog data voltages in each two period of the horizontal sync signal. The one-line data voltages converted by the first data driver **106**A are simultaneously supplied to the upper data lines UDL**1**-UDLm. In synchronization with the first data driver **106**A, the second data driver **106**B converts the one-line R, G and B pixel data into analog data voltages. The one-line data voltages converted by the second data driver **106**B are simultaneously supplied to the lower data lines LDL**1**-LDLm.

[0111] The first to fourth lamp drivers **115**A to **115**D sequentially turn on and off the first to fourth lamps **113**A to **113**D corresponding to the upper portion A of the liquid crystal panel **102** and the fifth to eighth lamps **113**E to **113**H corresponding to the lower portion B of the liquid crystal panel **102** in such a way that the first to fourth lamps **113**A to **113**D are synchronized with the fifth to eighth lamps **113**E to **113**H in each frame period while the liquid crystal cells Clc are simultaneously written once, as illustrated in FIG. **9**B. Thus, video data and black level data are alternately displayed once on the liquid crystal panel **102** in each frame period (e.g., 1/60 sec) of the video data generated from the external system.

[0112] Therefore, the LCD according to embodiments of the present invention can respond to the video data quickly. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed. Further, providing charging data voltages simultaneously to two portions of the liquid crystal panel also prevents an unclear image or image-sticking so that the image is presented quickly

[0113] In addition, the lamps for the sub-sections of the upper portion of the liquid crystal panel **102** and the lamps for the sub-sections of the lower portion of the liquid crystal panel **102** are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0114] Referring to FIG. **10**A, the gate driver **104** sequentially enables once each of the gate lines GL**1**-GLk for the upper portion A of the liquid crystal panel **102** during a half of each frame period (e.g., 1/60 sec) of the video data. The gate driver **104** sequentially enables once the gate lines GL(k+1)-GL**2***k* for the lower portion B of the liquid crystal panel **102** to be driven in synchronization with the gate lines GL**1**-GLk. For example, the gate driver **104** enables the first gate line GL**1** and the $(k+1)^{th}$ gate line GL(k+1) simultaneously for one period of the horizontal sync signal, enables the second gate line GL**2** and the $(k+2)^{th}$ gate line GL(k+2) simultaneously for another period of the horizontal sync signal, and enables the third gate line GL**3** and the $(k+3)^{th}$ gate line GL(k+3) simultaneously for yet another period of the horizontal sync signal. In this way, the k^{th} gate line GLk and the $2k^{th}$ gate line GL**2***k* are simultaneously enabled for the last period of the horizontal sync signal. In other words, the gate driver **104** drives k pairs of a first k number of gate lines GL**1**-GLk for the upper portion A of the liquid crystal panel **102** and a second k number of gate lines GL(k+1)-GL**2***k* for the lower portion B of the liquid crystal panel **102** pair-wise for each period of the horizontal sync signal. In addition, the gate driver **104** is in an idle mode so that no gate lines are enabled for the remaining half frame period in each frame period of the video data.

[0115] To this end, as illustrated in FIG. **10**A, the gate driver **104** supplies the 2k number of the scan signals SGL**1**-SGL**2***k* to the 2k number of the gate lines GL**1**-GL**2***k* on the liquid crystal panel **102** in each half period of the vertical sync signal, respectively. The 2k number of the scan signals SGL**1**-SGL**2***k* is divided into a first scan signal group SGL**1**-SGLk supplied to the first k number of the gate lines GL**1**-GLk on the upper portion A of the liquid crystal panel **102**, and a second scan signal group SGL(k+1)-SGL**2***k* supplied to the second k number of the gate lines GL(k+1)-GL**2***k* on the lower portion B of the liquid crystal panel **102**. The first scan signal group SGL**1**-SGLk has a pulse of gate high voltage with a phase and a width equal respectively to those of the second scan signal group SGL(k+1)-SGL**2***k*. The pulse width of the gate high voltage VGH corresponds to one period of the horizontal sync signal. The pulse of the gate high voltage VGH contained in the first scan signal group SGL is sequentially shifted by its own width (e.g., one period of the horizontal sync signal) as the gate lines GL on the upper portion A of the liquid crystal panel **102** move downward. Likewise, the pulse of the gate high voltage VGH contained in the second scan signal group SGL(k+1)-SGL**2***k* is sequentially shifted by its own width (e.g., one period of the horizontal sync signal) as the gate lines on the lower portion B of the liquid crystal panel **102** move downwards. In addition, the gate driver **104** maintains the 2k number of the scan signals at the gate low voltage VGL for the latter period of the vertical sync signal in each period of the vertical sync signal, so that the operation of writing the data voltage is not performed.

[0116] As the gate driver **104** sequentially enables the gate lines GL**1**-GLk on the upper portion A of the liquid crystal panel **102** in each period of the horizontal sync signal, the first data driver **106**A sequentially charges the liquid crystal cells Clc on the upper portion A of the liquid crystal panel **102** with the data voltages for a half period of the vertical sync signal in line by line fashion. Then, the first data driver **106**A is set to an idle mode for the latter period of one vertical sync signal. During the half period of one vertical sync signal, that is, during the data voltage write period, the one-line data voltages supplied from the first data driver **106**A to the data lines UDL**1**-UDLm are updated in each period of one horizontal sync signal.

[0117] Likewise, as the gate driver **104** sequentially enables the gate lines GL(k+1)-GL**2***k* on the lower portion B of the liquid crystal panel **102** in each period of the horizontal sync signal, the second data driver **106**B sequentially charges the liquid crystal cells Clc on the lower portion B of the liquid crystal panel **102** with the data voltages for a half period of the vertical sync signal in line by line fashion. Then, the second data driver **106**B is set to an idle mode for the latter period of one vertical sync signal. In synchronization with the one-line data voltages supplied from the first data driver **106**A, the one-line data voltages supplied from the second data driver **106**B to the data lines LDL**1**-LDLm are updated in each period of one horizontal sync signal.

[0118] The first and second data drivers **106**A and **106**B and the gate driver **104** sequentially charge the liquid crystal cells for the sub-sections of the upper portion A of the liquid crystal panel **102** and the liquid crystal cells for the sub-sections of the lower portion B of the liquid crystal panel **102** with the data voltages for a half period of the vertical sync signal such that they are synchronized with each other, respectively. For example, the liquid crystal cells on the first sub-section A**1** of the upper portion A of the liquid crystal panel **102** and the liquid crystal cells on the first sub-section B**1** of the lower portion B of the liquid crystal panel **102** charge the data voltages for a first 1/8 period DWP of one vertical sync signal, and maintains the charged data voltages for the remaining 7/8 period of one vertical sync signal. The liquid crystal cells on the second sub-section A**2** of the upper portion A of the liquid crystal panel **102** and the liquid crystal cells on the second sub-section B**2** of the lower portion B of the liquid crystal panel **102** charge the data voltages for a second 1/8 period DWP of one vertical sync signal, and maintains the charged data voltages for the remaining 6/8 period of one vertical sync signal and a first 1/8 period of a next vertical sync signal. The liquid crystal cells on the third sub-section A**3** of the upper portion A of the liquid crystal panel **102** and the liquid crystal cells on the third sub-section B**3** of the lower portion B of the liquid crystal panel **102** charge the data voltages for a third 1/8 period DWP of one vertical sync signal, and maintains the charged data voltages for the remaining 5/8 period of one vertical sync signal and a first 1/4 period of the next vertical sync signal. The liquid crystal cells on the fourth sub-section A**4** of the upper portion A of the liquid crystal panel **102** and the liquid crystal cells on the fourth sub-section B**4** of the lower portion B of the liquid crystal panel **102** charge the data voltages for a fourth 1/8 period DWP of one vertical sync

signal, and maintains the charged data voltages for the remaining ½ period of one vertical sync signal and a ⅜ period of a next vertical sync signal.

[0119] The first to fourth lamp drivers **115**A to **115**D of the backlight unit **112**, which are commonly controlled by the timing controller **108**, sequentially turn on and off the lamps **113**A to **113**H in each period of the vertical sync signal, that is, for each frame period. Each of the lamps **113**A to **113**H is turned on and off once in each frame period. The lamps **113**A to **113**D of the sub-sections A**1** to A**4** and the lamps **113**E to **113**H of the sub-sections B**1** to B**4** are turned on at a time when the alignment saturation period elapses after the liquid crystal cells charge the data voltages. Therefore, the lamp driving voltages supplied from the first to fourth lamp drivers **115**A to **115**D to the corresponding lamps **113**A to **113**H can be enabled at the time when the alignment saturation period elapses after the data voltage write period is finished, and can be disabled at the time when the data voltages are written to the sub-sections of the liquid crystal panel **102**. The enable period of the lamp driving voltages generated from the lamp drivers **115**A to **115**D are adjusted within the period except for the data voltage write period of the sub-sections and the alignment saturation period in the period of one vertical sync signal. The operation and effect of the first to fourth lamp drivers **115**A to **115**D generating the above-described lamp driving voltages will be described in detail with reference to FIG. **10**B.

[0120] Referring to FIG. **10**B, the waveform "DW**113**AE" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the first sub-sections A**1** and B**1** of the upper and lower portions A and B of the liquid crystal panel **102**. The waveform "LE**113**AE" represents the time period for enabling the first lamp driving signal outputted from the first lamp driver **115**A. According to the time periods of DW**113**AE and LE**113**AE, the first lamp driving voltage LE**113**AE from the first lamp driver **115**A has a low voltage level during half period of the vertical sync signal, including the first ⅛ period DWP of the vertical sync signal in which the data voltages are charged to the liquid crystal cells Clc of the first sub-sections A**1** and B**1** of the liquid crystal panel **102** and the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal. On the other hand, the first lamp driving voltage LE**113**AE has a high voltage level during the period (light irradiation period LEP) except for the alignment saturation period ASP in which the liquid crystal molecules are rearranged in an alignment direction corresponding to the data voltage, among the period (ASP+LEP) in which the liquid crystal cells Clc in the first sub-sections A**1** and B**1** of the liquid crystal panel **102** maintain the data voltages. The light irradiation period LEP corresponds to a half period of one vertical sync signal, and may be shortened according to an amount of brightness in the first sub-sections A**1** and B**1** of the liquid crystal panel **102**. When the light irradiation period LEP is shortened, the alignment saturation period ASP is lengthened as much as the reduced period of the light irradiation period LEP. The first and fifth lamps **113**A and **113**E commonly responding to the first lamp driving voltage LE**113**AE outputted from the first lamp driver **115**A are simultaneously turned on during half period of the vertical sync signal from the time when the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal elapses after the data voltages are written or charged to the liquid crystal cells Clc arranged on the first sub-sections A**1** and B**1** of the liquid crystal panel **102**. Thus, the light is irradiated onto the first sub-sections A**1** and B**1** of the liquid crystal panel **102**. Because the first and fifth lamps **113**A and **113**E irradiate light after the liquid crystal cells Clc of the first sub-sections A**1** and B**1** of the liquid crystal panel **102** are aligned in a direction corresponding to the data voltage, the pixel data can be correctly displayed. In addition, the black level data are displayed in the first sub-sections A**1** and B**1** of the liquid crystal panel **102** during the period in which the first and second lamps **113**A and **113**E are turned off. Therefore, a pseudo impulse display effect in the first sub-sections A**1** and B**1** of the liquid crystal panel **102** can be maximized.

[0121] In FIG. **10**B, the waveform "DW**113**BF" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the second sub-sections A**2** and B**2** of the upper and lower portions A and B of the liquid crystal panel **102**. The waveform "LE**113**BF" represents the time period for enabling the second lamp driving signal outputted from the second lamp driver **115**B. According to the time periods of DW**113**BF and LE**113**BF, the second lamp driving voltage LE**113**BF from the second lamp driver **115**B has a low voltage level during a half period of the vertical sync signal, including the second ⅛ period DWP of the vertical sync signal in which the data voltages are charged to the liquid crystal cells Clc of the second sub-sections A**2** and B**2** of the liquid crystal panel **102** and the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal. On the other hand, the second lamp driving voltage LE**113**BF has a high voltage level during the period (light irradiation period LEP) except for the alignment saturation period ASP in which the liquid crystal molecules are rearranged in an alignment direction corresponding to the data voltage, among the period (ASP+LEP) in which the liquid crystal cells Clc in the second sub-sections A**1** and B**1** of the liquid crystal panel **102** maintain the data voltages. The light irradiation period LEP corresponds to half period of one vertical sync signal, and may be shortened according to an amount of brightness in the second sub-sections A**2** and B**2** of the liquid crystal panel **102**. When the light irradiation period LEP is shortened, the alignment saturation period ASP is lengthened as much as the reduced period of the light irradiation period LEP. The second and sixth lamps **113**B and **113**F commonly responding to the second lamp driving voltage LE**113**BF outputted from the second lamp driver **115**B are simultaneously turned on during half period of the vertical sync signal from the time when the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal elapses after the data voltages are written or charged to the liquid crystal cells Clc arranged on the second sub-sections A**2** and B**2** of the liquid crystal panel **102**. Thus, the light is irradiated onto the second sub-sections A**2** and B**2** of the liquid crystal panel **102**. Because the second and sixth lamps **113**B and **113**F irradiate the light after the liquid crystal cells Clc of the second sub-sections A**2** and B**2** of the liquid crystal panel **102** are aligned in a direction corresponding to the data voltage, the pixel data can be correctly displayed. In addition, the black level data are displayed in the second sub-sections A**2** and B**2** of the liquid crystal panel **102** during the period in which the second and sixth lamps **113**B and **113**F are turned off. Therefore, the pseudo impulse display effect in the second sub-sections A**2** and B**2** of the liquid crystal panel **102** can be maximized.

[0122] In FIG. **10**B, the waveform "DW**113**CG" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the third sub-sections A**3** and B**3** of the upper and lower portions A and B of the liquid crystal panel **102**. The waveform "LE**113**CG" represents the time period for enabling the third lamp driving signal outputted from the third lamp driver **115**C. According to the time periods of DW**113**CG and LE**113**CG, the third lamp driving voltage LE**113**CG from the third lamp driver **115**C has a low voltage level during a half period of the vertical sync signal, including the third ⅛ period DWP of the vertical sync signal in which the data voltages are charged to the liquid crystal cells Clc of the third sub-sections A**3** and B**3** of the liquid crystal panel **102** and the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal. On the other hand, the third lamp driving voltage LE**113**CG has a high voltage level during the period (light irradiation period LEP) except for the alignment saturation period ASP in which the liquid crystal molecules are aligned corresponding to the data voltage, among the period (ASP+LEP) in which the liquid crystal cells Clc in the third sub-sections A**3** and B**3** of the liquid crystal panel **102** maintain the data voltages. The light irradiation period LEP corresponds to half period of one vertical sync signal, and may be shortened according to an amount of brightness in the third sub-sections A**3** and B**3** of the liquid crystal panel **102**. When the light irradiation period LEP is shortened, the alignment saturation period ASP is lengthened as much as the reduced period of the light irradiation period LEP. The third and seventh lamps **113**C and **113**G commonly responding to the third lamp driving voltage LE**113**CG outputted from the third lamp driver **115**C are simultaneously turned on during a half period of the vertical sync signal from the time when the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal elapses after the data voltages are written or charged to the liquid crystal cells Clc arranged on the third sub-sections A**3** and B**3** of the liquid crystal panel **102**. Thus, the light is irradiated onto the third sub-sections A**3** and B**3** of the liquid crystal panel **102**. Because the third and seventh lamps **113**C and **113**G irradiate light after the liquid crystal cells Clc of the third sub-sections A**3** and B**3** of the liquid crystal panel **102** are aligned in a direction corresponding to the data voltage, the pixel data can be correctly displayed. In addition, the black level data are displayed in the third sub-sections A**3** and B**3** of the liquid crystal panel **102** during the period in which the third and seventh lamps **113**C and **113**G are turned off. Therefore, the pseudo impulse display effect in the third sub-sections A**3** and B**3** of the liquid crystal panel **102** can be maximized.

[0123] In FIG. **10**B, the waveform "DW**113**DH" represents the time period for writing the data voltages to the liquid crystal cells Clc arranged on the fourth sub-sections A**4** and B**4** of the upper and lower portions A and B of the liquid crystal panel **102**. The waveform "LE**113**DH" represents the time period for enabling the fourth lamp driving signal outputted from the fourth lamp driver **115**D. According to the timing diagrams of DW**113**DH and LE**113**DH, the fourth lamp driving voltage LE**113**DH from the fourth lamp driver **115**D has a low voltage level during a half period of the vertical sync signal, including the fourth ⅛ period DWP of the vertical sync signal in which the data voltages are charged to the liquid crystal cells Clc of the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** and the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal. On the other hand, the fourth lamp driving voltage LE**113**DH has a high voltage level during the period (light irradiation period LEP) except for the alignment saturation period ASP in which the liquid crystal molecules are aligned corresponding to the data voltage, among the period (ASP+LEP) in which the liquid crystal cells Clc in the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** maintain the data voltages. The light irradiation period LEP corresponds to a half period of one vertical sync signal, and may be shortened according to an amount of brightness in the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**. When the light irradiation period LEP is shortened, the alignment saturation period ASP is lengthened as much as the reduced period of the light irradiation period LEP. The fourth and eighth lamps **113**D and **113**H commonly responding to the fourth lamp driving voltage LE**113**DH outputted from the fourth lamp driver **115**D are simultaneously turned on during half period of the vertical sync signal from the time when the alignment saturation period ASP corresponding to the ⅜ period of the vertical sync signal elapses after the data voltages are written or charged to the liquid crystal cells Clc arranged on the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**. Thus, the light is irradiated onto the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102**. Because the fourth and eighth lamps **113**D and **113**H irradiate the light after the liquid crystal cells Clc of the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** are aligned in a direction corresponding to the data voltage, the pixel data can be correctly displayed. In addition, the black level data are displayed in the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** during the period in which the fourth and eighth lamps **113**D and **113**H are turned off. Therefore, the pseudo impulse display effect in the fourth sub-sections A**4** and B**4** of the liquid crystal panel **102** can be maximized.

[0124] The timing controller **108** controls the gate driver **104** and the first and second data drivers **106**A and **106**B so that the data voltages are writen to the liquid crystal cells of the liquid crystal panel **102** during half frame period, as illustrated in FIGS. **10**A and **10**B. Meanwhile, upon a controlling of the timing controller **108**, the lamp drivers drive the lamps **113**A to **113**H to be sequentially turned on and off once in each frame period. To this end, the timing controller **108** supplies the gate control signal to the gate driver **104**, the data control signal to the first and second data drivers **106**A and **106**B, and the lamp control signal to the first to fourth lamp drivers **115**A to **115**D. In addition, the timing controller **108** supplies two-line pixel data to the first and second data drivers **106**A and **106**B for one period of the horizontal sync signal. In other words, the timing controller **108** supplies the one-line pixel data to the first data driver **106**A, and the one-line pixel data to the second data driver **106**B for one period of the horizontal sync signal. To this end, the timing controller **108** responds to vertical/horizontal sync signals (Vsync/Hsync), data enable signal (DE), clock signal, and video data, which are generated from an external system (not shown), such as a graphic card of computer system or a TV signal decoder module from a television receiver. The timing controller **108** generates the gate control signals for the gate driver **104**, the data control signals for the first and second data drivers **106**A and **106**B, and the lamp control signals for the first to fourth lamp drivers **113**A to **113**D, by using the vertical/horizontal sync signals

(Vsync/Hsync), the data enable signal (DE), and the clock signal. In addition, the timing controller **108** arranges the R, G and B pixel data supplied from the external system into line by line R, G and B pixel data, and supplies the one-line R, G and B pixel data to the first and second data drivers **106**A and **106**B in each period of the horizontal sync signals.

[0125] Therefore, the first data driver **106**A converts the one-line R, G and B pixel data into analog data voltages in each period of the horizontal sync signal. The one-line data voltages converted by the first data driver **106**A are simultaneously supplied to the upper data lines UDL**1**-UDLm. In synchronization with the first data driver **106**A, the second data driver **106**B converts the one-line R, G and B pixel data into analog data voltages. The one-line data voltages converted by the second data driver **106**B are simultaneously supplied to the lower data lines LDL**1**-LDLm. As illustrated in FIG. **10**B, the first to fourth lamp drivers **115**A to **115**D controlled by the timing controller **108** turn on the first to fourth lamps **113**A to **113**D from the time when the alignment saturation period ASP elapses after the data voltages are written to the sub-sections A**1** to A**4** of the liquid crystal panel **102** to the time when the data voltages start to be written to the sub-sections A**1** to A**4** of the liquid crystal panel **102**. In addition, the first to fourth lamp drivers **115**A to **115**D turn on and off the fifth to eighth lamps **113**E to **113**H to be synchronized (simultaneously) with the first to fourth lamps **113**A to **113**D. Therefore, the fifth to eighth lamps **113**E to **113**H are turned on from the time when the alignment saturation period ASP elapses after the data voltages are written to the sub-sections B**1** to B**4** of the liquid crystal panel **102** to the time when the data voltages start to be written to the sub-sections B**1** to B**4** of the liquid crystal panel **102**.

[0126] The timing controller **108** controls the first to fourth lamp drivers in that light irradiates onto the sub-sections of the liquid crystal panel **102** from the time after the liquid crystal molecules are aligned in a direction corresponding to the data voltage after the data voltages are written to the lamps **113**A to **113**H. Therefore, while the lamps **113**A to **113**H are turned on, the liquid crystal panel **102** correctly displays the image corresponding to the video data (data voltages) on the sub-sections. On the other hand, while the lamps **113**A to **113**H are turned off, the black level data are displayed on the sub-sections corresponding to the lamps **113** to **113**H.

[0127] In this way, the black level image and the image corresponding to the video data are correctly displayed once because the lamps **113**A to **113**H are turned on and off once in each frame, thereby maximizing the pseudo impulse driving effect. Therefore, the LCD according to embodiments of the present invention can respond to the video data quickly. In addition, the motion blurring phenomenon does not occur when a moving picture is displayed. Further, it is possible to prevents an unclear image or image-sticking. Thus, the LCD according to embodiments of the present invention can display the high quality image.

[0128] Moreover, the lamps for the sub-sections of the upper portion of the liquid crystal panel and the lamps for the sub-sections of the lower portion of the liquid crystal panel are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0129] Thus, video data and black level data are alternately displayed twice on the liquid crystal panel **202** at a frame frequency (the second frame frequency of e.g., 120 Hz) that is twice the frame frequency (e.g., the first frame frequency of 60 Hz) of the video data generated from the external system. Therefore, the LCD according to embodiments of the present invention can respond to the video data quickly. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed. Further, providing charging data voltages simultaneously to two portions of the liquid crystal panel also prevents an unclear image or image-sticking so that the image is presented quickly

[0130] In addition, the lamps for the sub-sections of the upper portion of the liquid crystal panel and the lamps for the sub-sections of the lower portion of the liquid crystal panel are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0131] As described above, in the LCD and the driving method thereof according to embodiments of the present invention, video data and black level data are alternately displayed at least once on the liquid crystal panel at a frame frequency (the second frame frequency of e.g., 120 Hz) that is at least twice the frame frequency (e.g., the first frame frequency of 60 Hz) of the video data generated from the external system. Therefore, the LCD according to embodiments of the present invention can respond to the video data quickly. Thus, the motion blurring phenomenon does not occur when a moving picture is displayed. Further, alternating the display of video data and black level data on the liquid crystal panel in each frame period also prevents an unclear image or image-sticking so that the image is presented quickly while minimizing a reduction of brightness.

[0132] In addition, the lamps for the sub-sections of the upper portion of the liquid crystal panel and the lamps for the sub-sections of the lower portion of the liquid crystal panel are turned on and off by a single lamp driver. Therefore, the circuit for driving the lamps can be simplified.

[0133] It will be apparent to those skilled in the art that various modifications and variations can be made in the liquid crystal display device and driving method thereof of embodiments of the present invention. Thus, it is intended that embodiments of the present invention cover the modifications and variations of the embodiments described herein provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display device, comprising:

a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel;

a data converter for converting a first video data having a first frame frequency into a second video data having a second frame frequency, which is higher than the first frame frequency;

a backlight unit having a first lamp group with at least two lamps for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and

a driver for driving the gate lines, the first data lines and the second data lines in accordance with the second video data and for driving the first and second lamp groups at the second frame frequency so that the lamps of the first lamp group are sequentially turned on and off in synchronization with the lamps of the second lamp group.

2. The liquid crystal display device according to claim 1, wherein the driver includes:

a gate driver for simultaneously driving the gate lines on the first and second regions so that the gate lines on the second region are sequentially enabled in synchronization with the gate lines on the first region;

a first data driver for driving the first data lines on the first region;

a second data driver for driving the second data lines on the second region; and

a timing controller responsive to the second video data for controlling the gate driver, the first data driver and the second data driver and enabling the lamps of the first and second lamp groups to be sequentially turned on and off in synchronization with each other.

3. The liquid crystal display device according to claim 2, wherein the backlight unit includes at least two lamp drivers being controlled by the timing controller and generating lamp driving voltages for enabling the lamps of the first and second lamp groups to be sequentially driven in synchronization with each other.

4. The liquid crystal display device according to claim 3, wherein the lamp driving voltages have different duty cycles.

5. The liquid crystal display device according to claim 4, wherein the second frame frequency is at least twice the first frame frequency.

6. A liquid crystal display device, comprising:

a liquid crystal panel having gate lines and data lines crossing each other;

a backlight unit having a first lamp group with at least two lamps for divisionally irradiating light on a first region of the liquid crystal panel and a second lamp group with at least two lamps divisionally irradiating light on a second region of the liquid crystal panel; and

a driver for driving the gate lines and data lines in accordance with a video data having a first frame frequency and for controlling the first and second lamp groups to be simultaneously driven at a second frame frequency higher than the first frame frequency so that the lamps of the first lamp group are sequentially turned on and off in synchronization with the lamps of the second lamp group.

7. The liquid crystal display device according to claim 6, wherein the driver includes:

a gate driver for driving the gate lines;

a data driver for driving the data lines; and

a timing controller responsive to the video data having the first frame frequency for controlling the gate driver and the date driver and enabling the lamps of the first and second lamp groups to be sequentially turned on and off in synchronization with each other.

8. The liquid crystal display device according to claim 7, wherein the backlight unit includes at least two lamp drivers being controlled by the timing controller and generating lamp driving voltages for enabling the lamps of the first and second lamp groups to be sequentially driven in synchronization with each other.

9. The liquid crystal display device according to claim 8, wherein the lamp driving voltages have different duty cycles.

10. The liquid crystal display device according to claim 6, wherein the second frame frequency is at least twice the first frame frequency.

11. The liquid crystal display device according to claim 6, wherein the gate lines include:

first gate lines crossing the data lines on a third region occupying parts of the first and second regions; and

second gate lines crossing the data lines on a fourth region occupying remaining parts of the first and second regions.

12. The liquid crystal display device according to claim 11, wherein the driver includes:

a first gate driver for driving the first gate lines;

a second gate driver for driving the second gate lines in synchronization with the first gate lines;

a data driver for driving the data lines; and

a timing controller responsive the video data having the first frame frequency for controlling the first and second gate drivers and the date driver and enabling the lamps of the first and second lamp groups to be sequentially turned on and off in synchronization with each other.

13. The liquid crystal display device according to claim 12, wherein the backlight unit includes at least two lamp drivers being controlled by the timing controller and generating lamp driving voltages for enabling the lamps of the first and second lamp groups to be sequentially driven in synchronization with each other.

14. The liquid crystal display device according to claim 13, wherein the lamp driving voltages have different duty cycles.

15. The liquid crystal display device according to claim 11, wherein the second frame frequency is at least twice the first frame frequency.

16. A liquid crystal display device, comprising:

a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel;

a backlight unit having a first lamp group with at least two lamp for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and

a driver for driving the gate lines and the data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in each frame in line by line fashion, and for driving the first and second lamp groups so that the at least two lamps of the first lamp group are sequentially turned on and off once in synchronization with the at least two lamps of the second lamp group.

17. The liquid crystal display device according to claim 16, wherein the gate lines on the first region and the gate lines on the second region are sequentially enabled in each two period of a horizontal sync signal in synchronization with each other.

18. The liquid crystal display device according to claim 17, wherein the driver includes:

a gate driver for simultaneously driving the gate lines on the first and second regions so that the gate lines on the second region are sequentially enabled in synchronization with the gate lines on the first region;

a first data driver for driving the first data lines on the first region;

a second data driver for driving the second data lines on the second region; and

a timing controller responsive to the video data for controlling the gate driver, the first data driver and the second data driver and enabling the lamps of the first and second lamp groups to be sequentially turned on and off in synchronization with each other.

19. The liquid crystal display device according to claim **18**, wherein the backlight unit includes at least two lamp drivers being controlled by the timing controller and generating lamp driving voltages for enabling the lamps of the first and second lamp groups to be sequentially driven in synchronization with each other.

20. The liquid crystal display device according to claim **18**, wherein the lamp driving voltages have different duty cycles.

21. A liquid crystal display device, comprising:

a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel and second data lines crossing the gate lines on a second region of the liquid crystal panel;

a backlight unit having a first lamp group with at least two lamps for respectively irradiating light onto sub-regions of the first region and a second lamp group with at least two lamps respectively irradiating light on sub-regions of the second region; and

a driver for operating the gate lines and the data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in each frame in a line by line manner, and for driving the first and second lamp groups so that the lamps of the first and second lamp groups are turned on and off at time when an alignment saturation period elapses after the data voltages are written to liquid crystal cells of the corresponding sub-regions.

22. The liquid crystal display device according to claim **21**, wherein the gate lines on the first region and the gate lines on the second region are sequentially enabled in each period of one horizontal sync signal in synchronization with each other.

23. The liquid crystal display device according to claim **22**, wherein the gate lines on the first region and the gate lines on the second region are sequentially enabled once in synchronization with each other during a half frame period in each frame.

24. The liquid crystal display device according to claim **23**, wherein the driver includes:

a gate driver for simultaneously driving the gate lines on the first and second regions so that the gate lines on the second region are sequentially enabled in synchronization with the gate lines on the first region;

a first data driver for driving the first data lines on the first region;

a second data driver for driving the second data lines on the second region; and

a timing controller responsive to the video data for controlling the gate driver, the first data driver and the second data driver and enabling the lamps of the first and second lamp groups to be sequentially turned on and off in synchronization with each other.

25. The liquid crystal display device according to claim **24**, wherein the backlight unit includes at least two lamp drivers being controlled by the timing controller and generating lamp driving voltages for enabling the lamps of the first and second lamp groups to be sequentially driven in synchronization with each other.

26. The liquid crystal display device according to claim **25**, wherein the lamp driving voltages have different duty cycles.

27. A liquid crystal display device, comprising:

a liquid crystal panel having gate lines and data lines crossing each other;

a backlight unit having a first lamp group with at least two lamps for divisionally irradiating light on a first region of the liquid crystal panel and a second lamp group with at least two lamps for divisionally irradiating light on a second region of the liquid crystal panel; and

a driver for driving the gate lines and data lines to sequentially write data voltages of a video data to liquid crystal cells of the liquid crystal panel in each frame in line by line manner, and for controlling the first and second lamp groups to be sequentially turned on and off once in synchronization with each other.

28. The liquid crystal display device according to claim **27**, wherein the driver includes:

a gate driver for sequentially driving the gate lines once in each frame;

a data driver for driving the data lines; and

a timing controller responsive to the video data for controlling the gate driver and the date driver and enabling the lamps of the first and second lamp groups to be sequentially turned on and off once in synchronization with each other.

29. The liquid crystal display device according to claim **28**, wherein the backlight unit includes at least two lamp drivers being controlled by the timing controller and generating lamp driving voltages for enabling the lamps of the first and second lamp groups to be sequentially driven in synchronization with each other.

30. The liquid crystal display device according to claim **29**, wherein the lamp driving voltages have different duty cycles.

31. A method of driving a liquid crystal display device with a liquid crystal panel having first data lines crossing gate lines on a first region of the liquid crystal panel, and second data lines crossing the gate lines on a second region of the liquid crystal panel, comprising:

converting a first video data having a first frame frequency into a second video data having a second frame frequency higher than the first frame frequency;

driving the gate lines, the first and second data lines in accordance with the second video data; and

controlling the first and second lamp groups to turn-on and turn-off simultaneously at the second frame frequency, the first lamp groups having at least two lamps for a first region and the second lamp group having at least two lamps for the second region.

32. The method according to claim **31**, wherein the second frame frequency is at least twice the first frame frequency.

33. A method of driving a liquid crystal display device with a liquid crystal panel having gate lines and data lines crossing each other, comprising:

driving the gate lines and data lines in accordance with a video data having a first frame frequency; and

controlling the first and second lamp groups to turn-on and turn-off simultaneously at a second frame frequency higher than the first frame frequency, the first

lamp group having at least two lamps for a first region of the liquid crystal panel and the second lamp group having at least two lamps for a second region of the liquid crystal panel.

34. The method according to claim **33**, wherein the second frame frequency is at least twice the first frame frequency.

35. The method according to claim **35**, wherein the gate lines include:

first gate lines crossing the data lines on a third region occupying parts of the first and second regions; and

second gate lines crossing the data lines on a fourth region occupying remaining parts of the first and second regions.

36. A method for controlling a liquid crystal display device having a liquid crystal panel with first data lines crossing gate lines on a first region and second data lines crossing the gate lines on a second region, at least two first lamps partially corresponding to the first region of the liquid crystal panel, and at least two second lamps partially corresponding to the second region of the liquid crystal panel, the method comprising:

driving the gate lines and data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in line by line fashion; and

turning on and off once the first lamps together with the second lamps by one pair at a time.

37. The method according to claim **36**, wherein the gate lines on the first region and the gate lines on the second region are sequentially enabled in synchronization with each other in each two period of a horizontal sync signal.

38. A method for controlling a liquid crystal display device having a liquid crystal panel with first data lines crossing gate lines on a first region and second data lines crossing the gate lines on a second region, at least two first lamps partially corresponding to the first region of the liquid crystal panel, and at least two second lamps partially corresponding to the second region of the liquid crystal panel, the method comprising:

driving the gate lines and data lines to simultaneously write data voltages of a video data to liquid crystal cells of the first region and liquid crystal cells of the second region in a line by line manner; and

driving the first and second lamps so that the lamps of the first and second lamps are turned on and off at time when an alignment saturation period elapses after the data voltages are written to liquid crystal cells on the liquid crystal panel.

39. The method according to claim **38**, wherein the driving of the gate lines and the data lines includes enabling sequentially the gate lines on the first region and the gate lines on the second region in synchronization with each other in each period of a horizontal sync signal, and the driving of the lamps includes turning on and off the first and second lamps once in each frame.

40. The method according to claim **39**, wherein the gate lines on the first region and the gate lines on the second region are sequentially enabled once in synchronization with each other during half frame period in each frame.

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摘要(译)

一种液晶显示装置，包括液晶面板，所述液晶面板具有与所述液晶面板的第一区域上的栅极线交叉的第一数据线和与所述液晶面板的第二区域上的栅极线交叉的第二数据线。数据转换器，用于将具有第一帧频的第一视频数据转换为具有第二帧频的第二视频数据，所述第二帧频高于第一帧频;背光单元，具有第一灯组，其具有至少两个灯，用于分别将光照射到第一区域的子区域上;以及第二灯组，其中至少两个灯分别在第二区域的子区域上照射光;驱动器，用于根据第二视频数据驱动栅极线，第一数据线和第二数据线，并用于以第二帧频率驱动第一和第二灯组，使得第一灯组的灯依次与第二个灯组的灯同步打开和关闭。