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(43) **Pub. Date: Mar. 29, 2007**(54) **LIQUID CRYSTAL DISPLAY AND
MANUFACTURING METHOD THEREOF****Publication Classification**(75) Inventors: **Yeong-Beom Lee**, Cheonan-si (KR);
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Yong-Eui Lee, Seongnam-si (KR)(51) **Int. Cl.**
G02F 1/1339 (2006.01)(52) **U.S. Cl.** **349/156**Correspondence Address:
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WOODBURY, NY 11797 (US)(57) **ABSTRACT**

A liquid crystal display includes a first substrate, a first electrode formed on the first substrate, a passivation layer formed between the first substrate and the first electrode, a second substrate facing the first substrate, a second electrode formed on the second substrate, a columnar spacer formed between the second substrate and the first substrate, and a liquid crystal layer having liquid crystal molecules vertically aligned with respect to the first and second substrates, and formed between the first and second substrates. The passivation layer and the columnar spacer are made of substantially the same material at the same layer.

(73) Assignee: **Samsung Electronics Co., LTD.**(21) Appl. No.: **11/492,424**(22) Filed: **Jul. 25, 2006**(30) **Foreign Application Priority Data**

Sep. 29, 2005 (KR) 10-2005-0091141

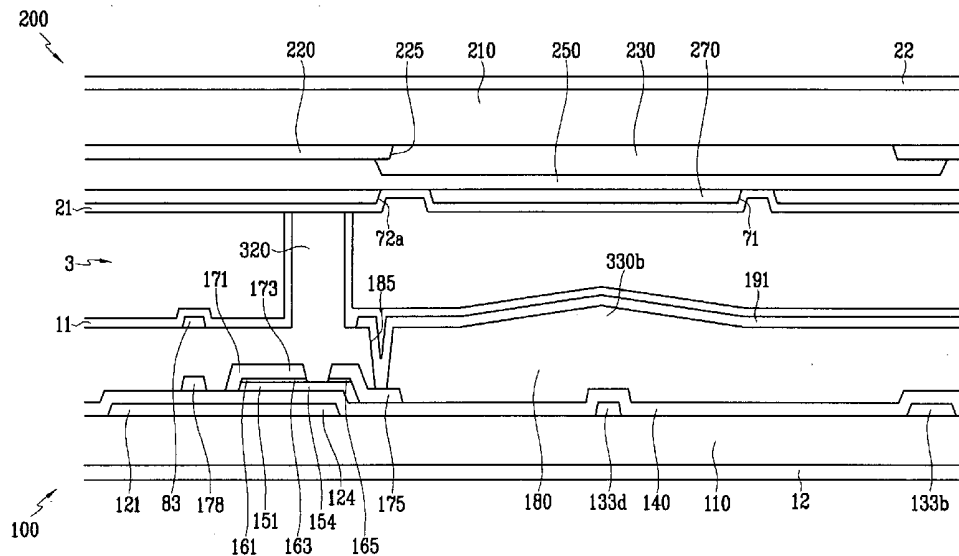


FIG.3

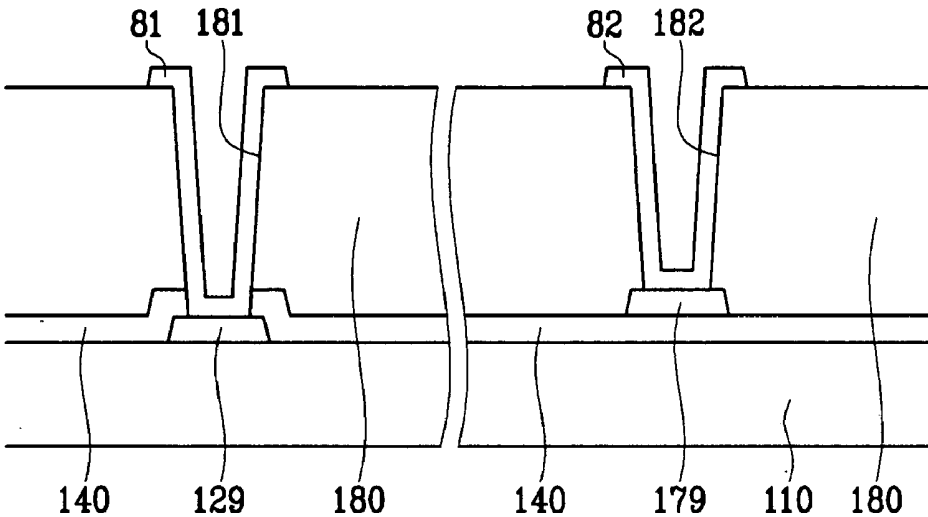


FIG. 4A

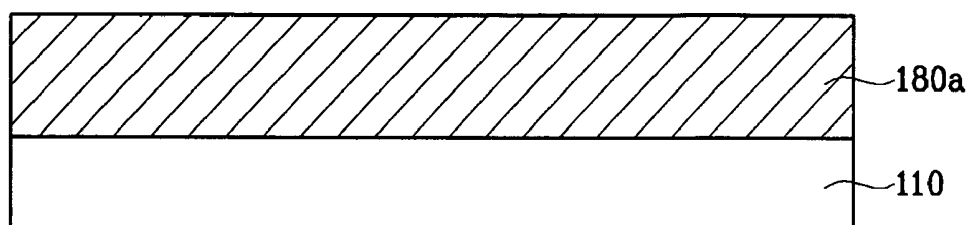


FIG. 4B

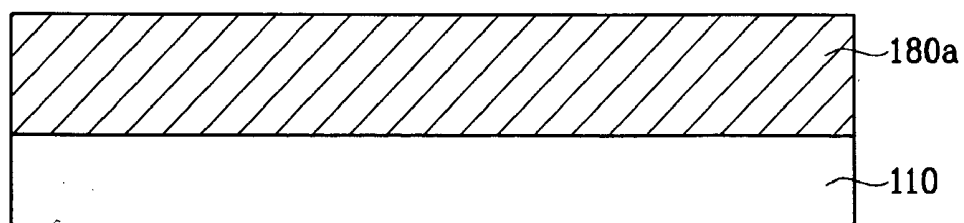
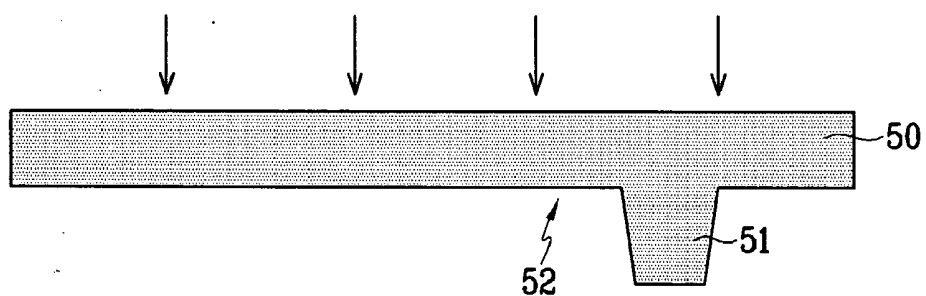


FIG. 4C

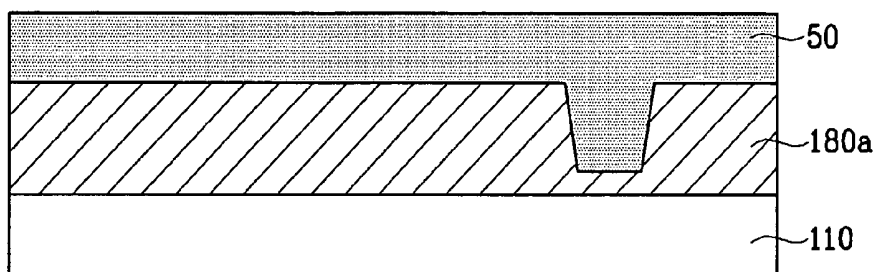


FIG. 4D

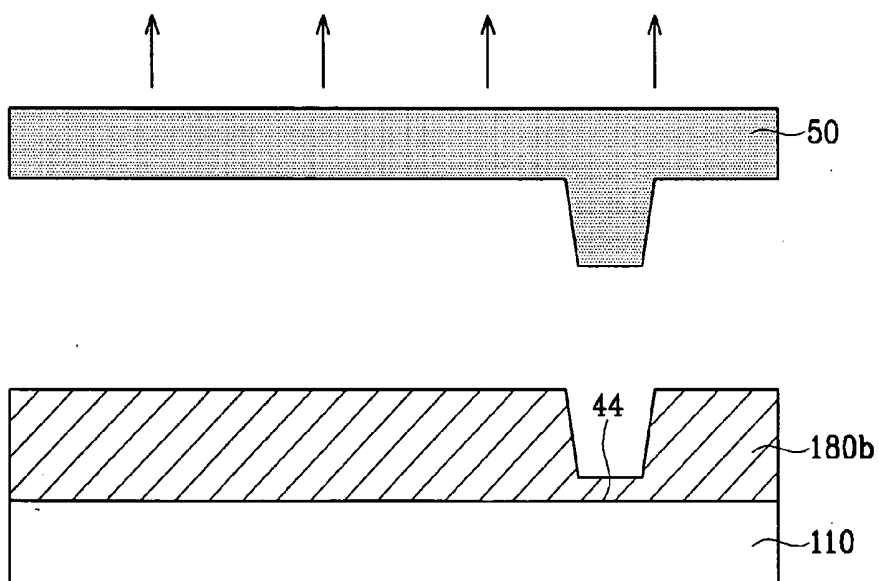


FIG. 4E

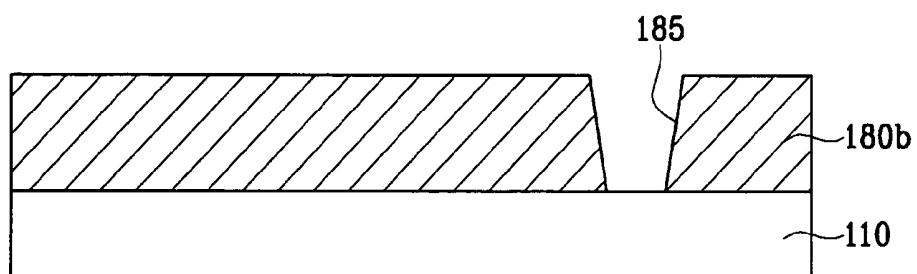


FIG. 5A

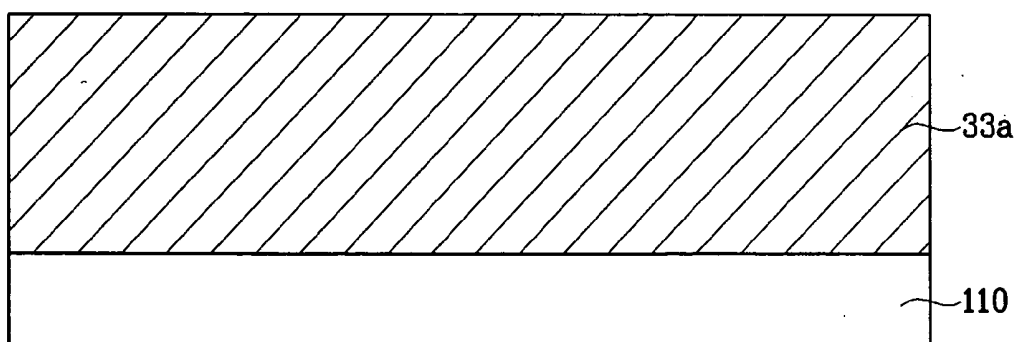


FIG.5B

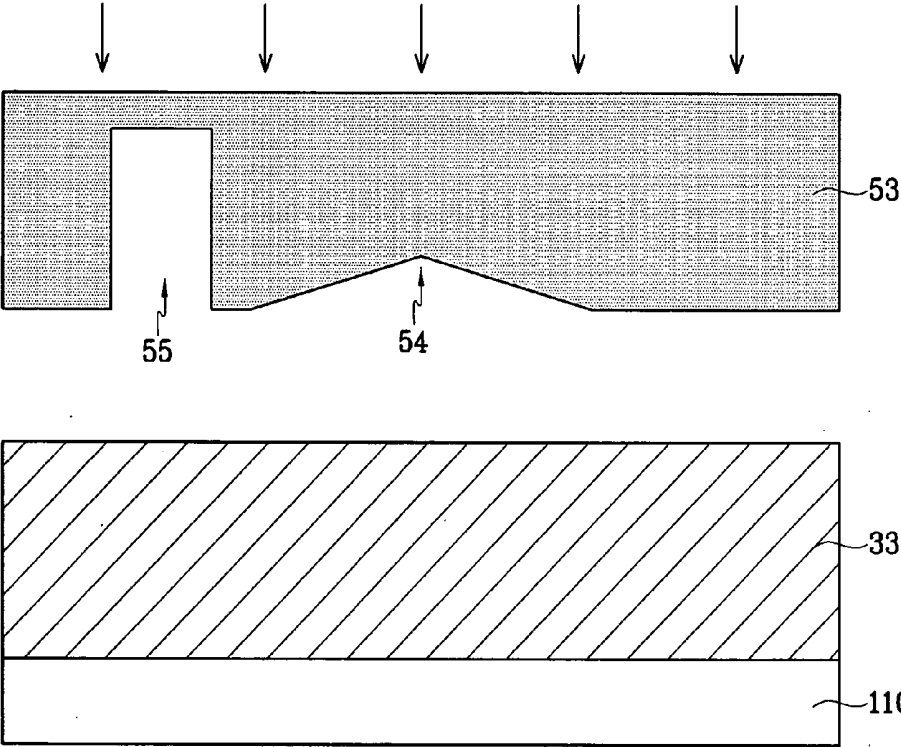


FIG.5C

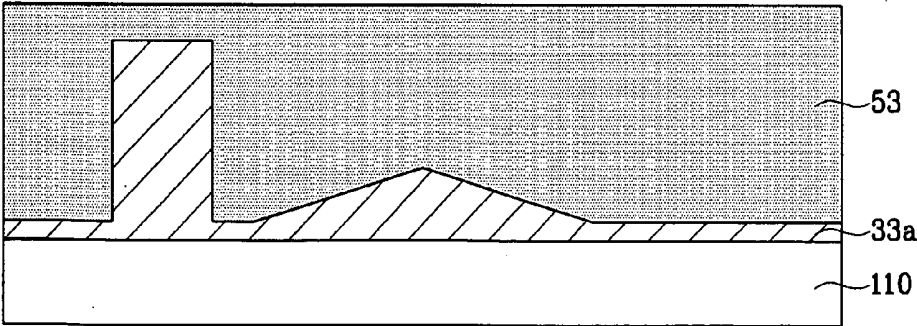


FIG. 5D

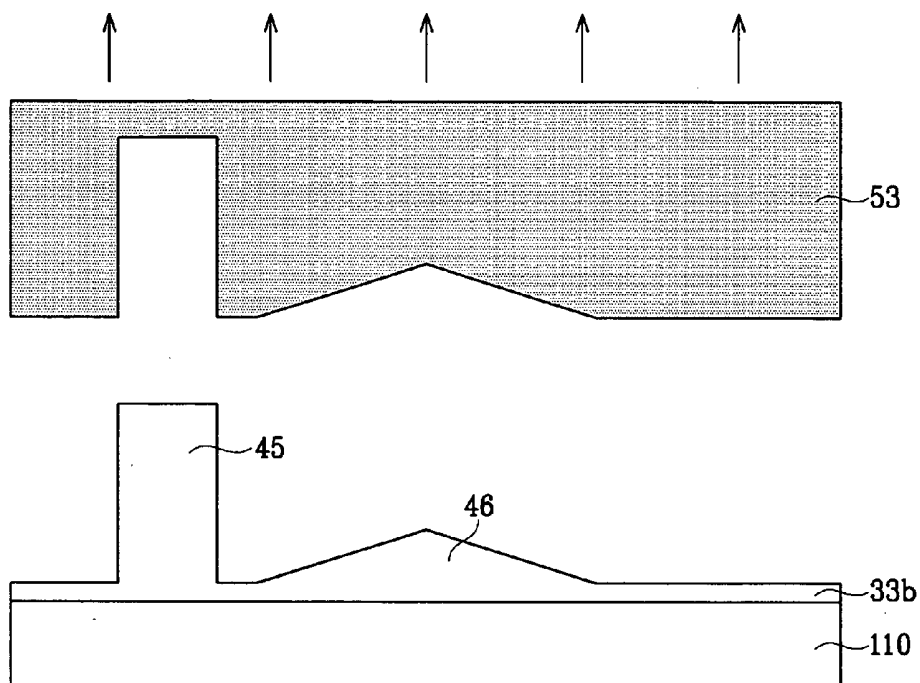


FIG. 5E

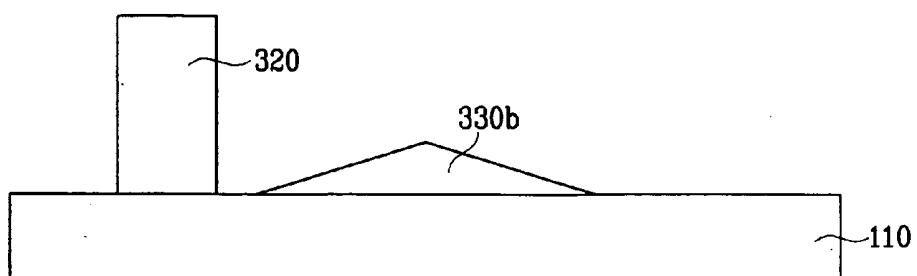


FIG. 6A

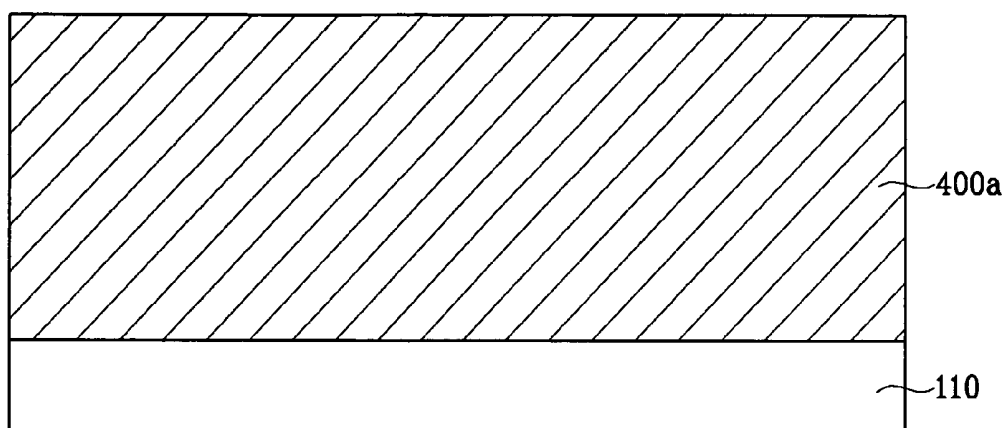


FIG. 6B

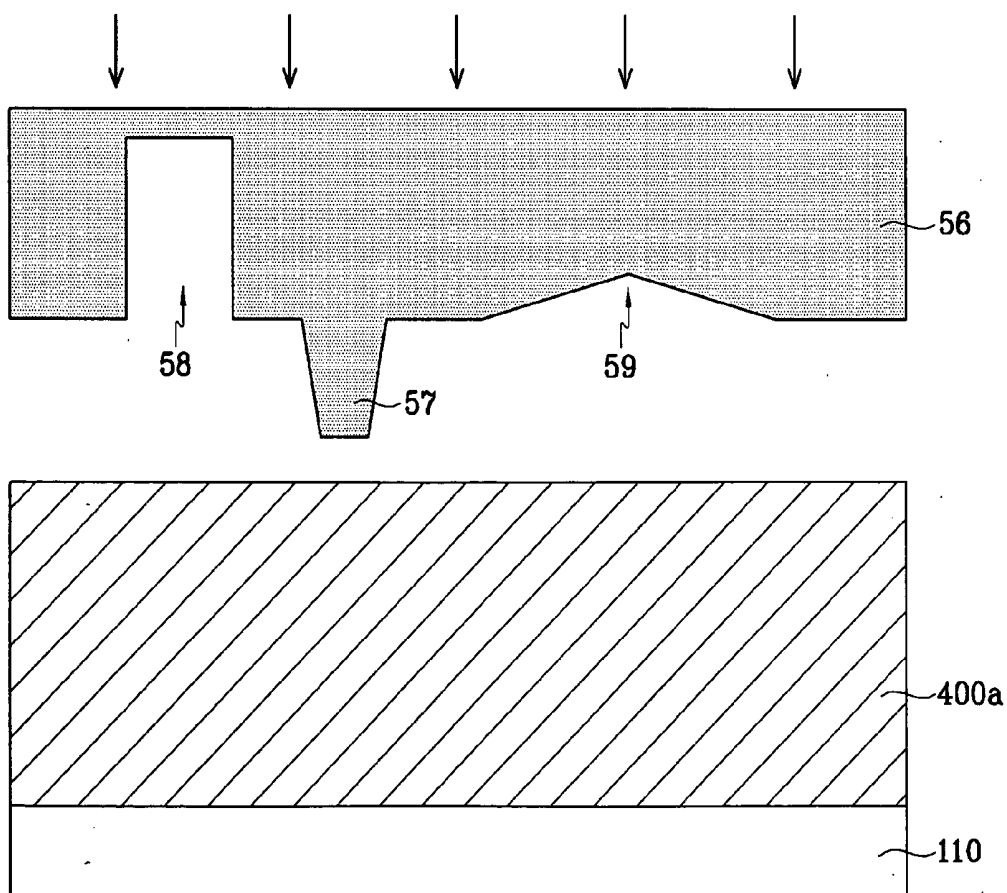


FIG. 6C

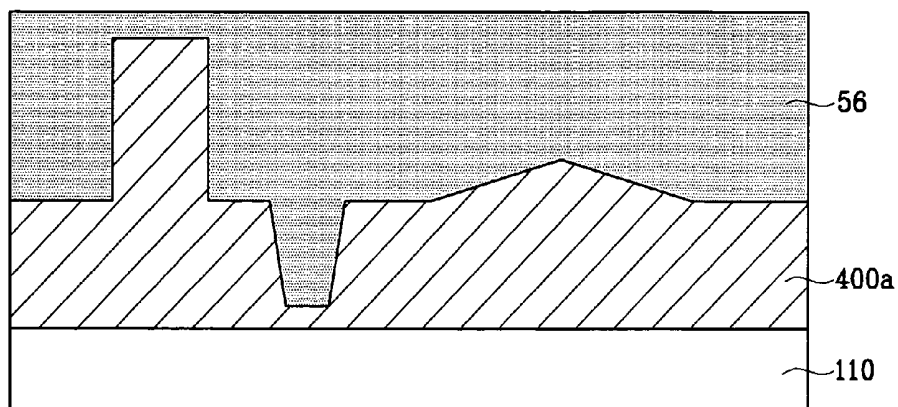


FIG. 6D

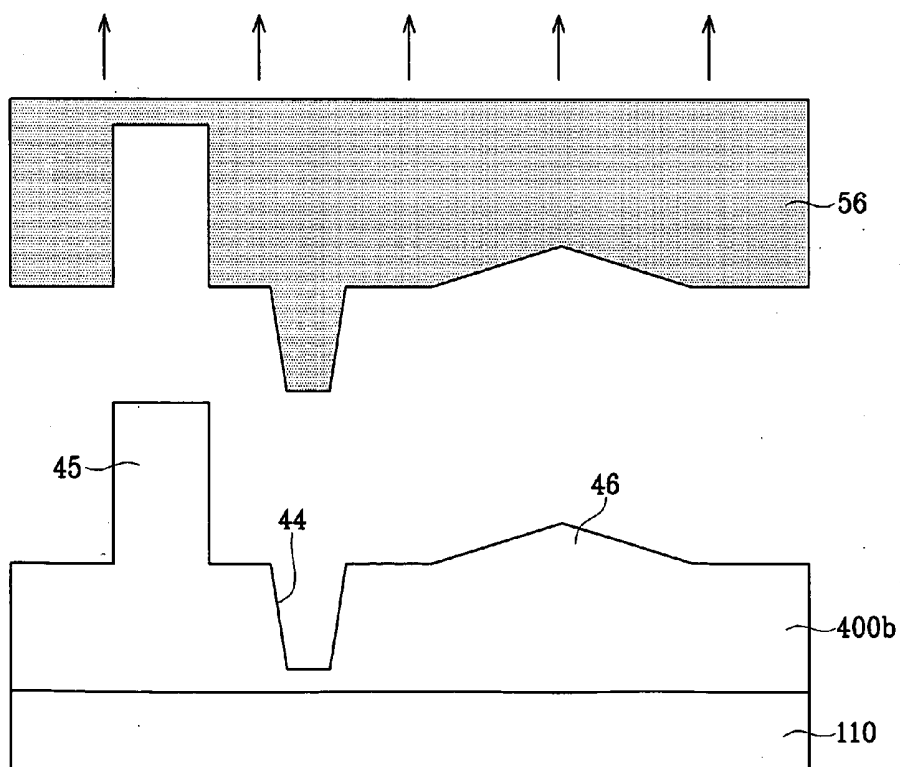


FIG. 6E

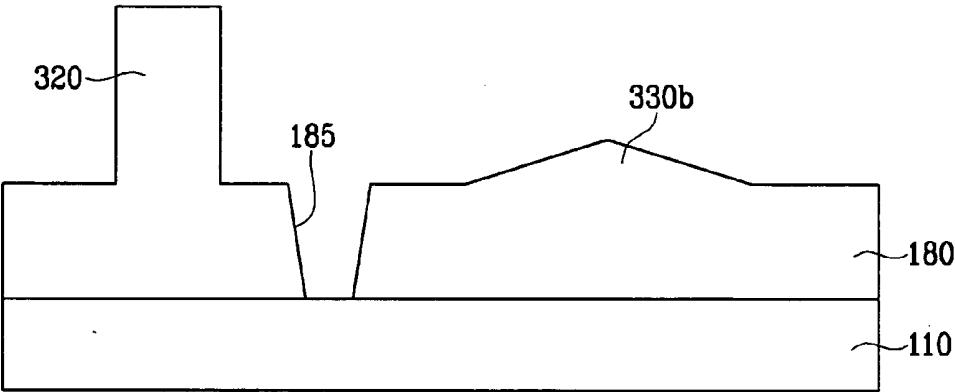


FIG. 7

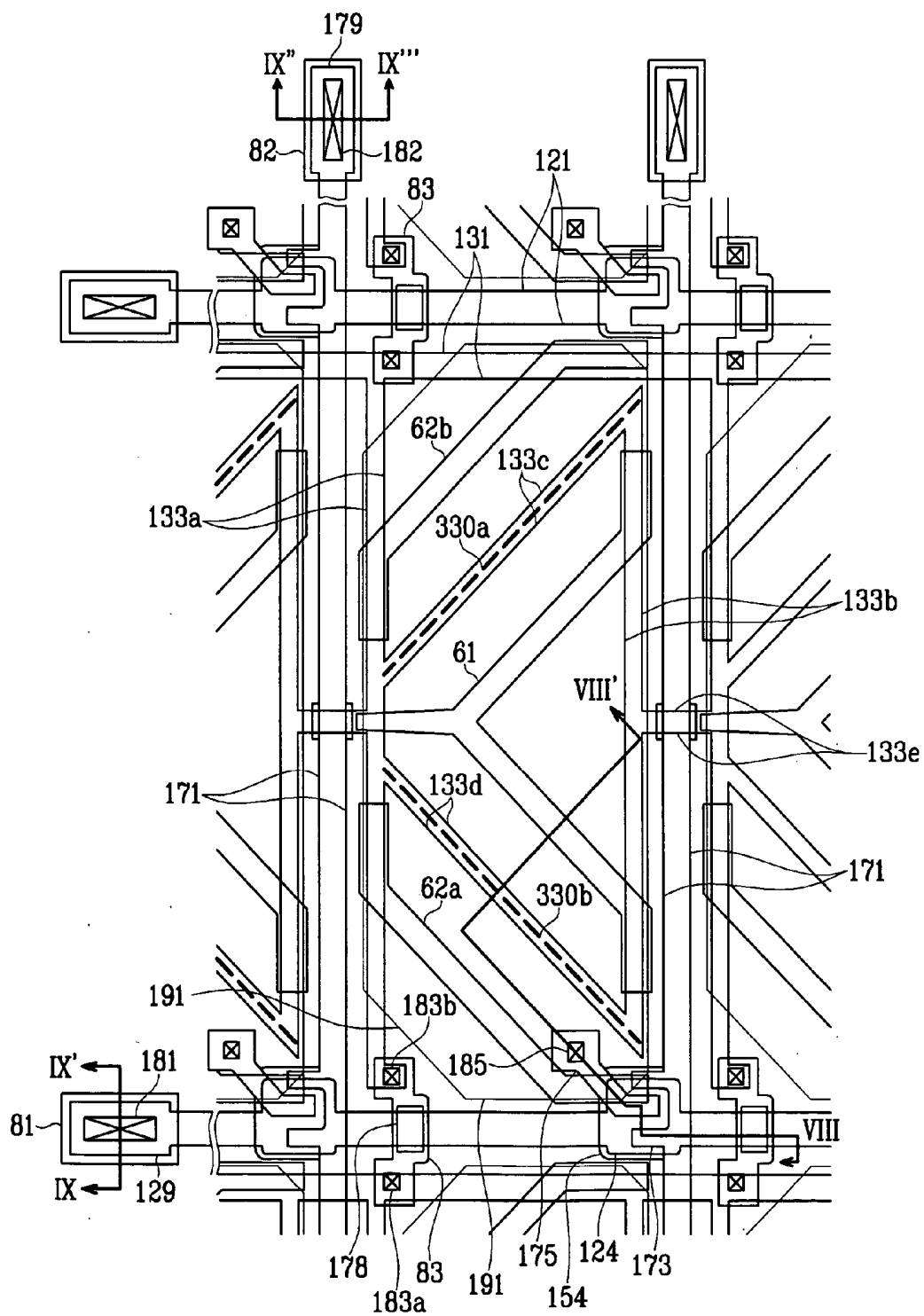


FIG. 8

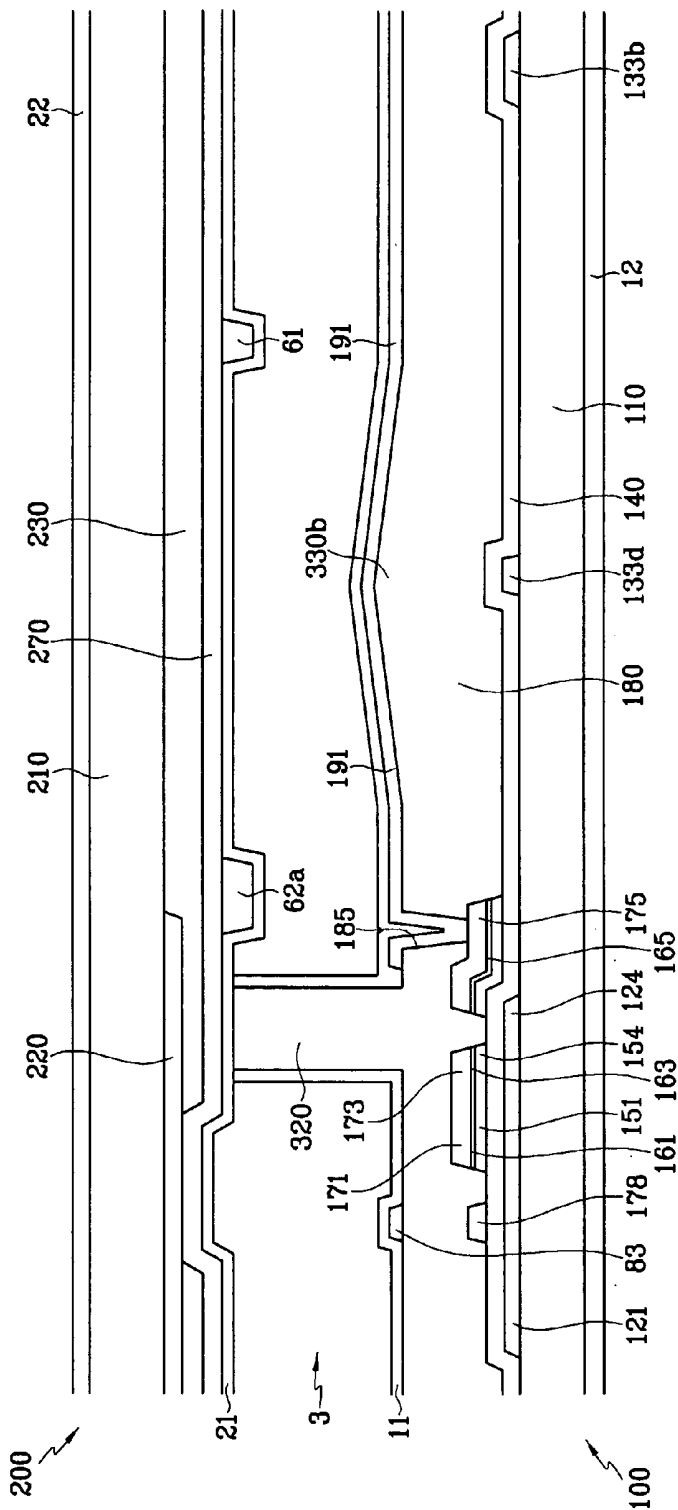
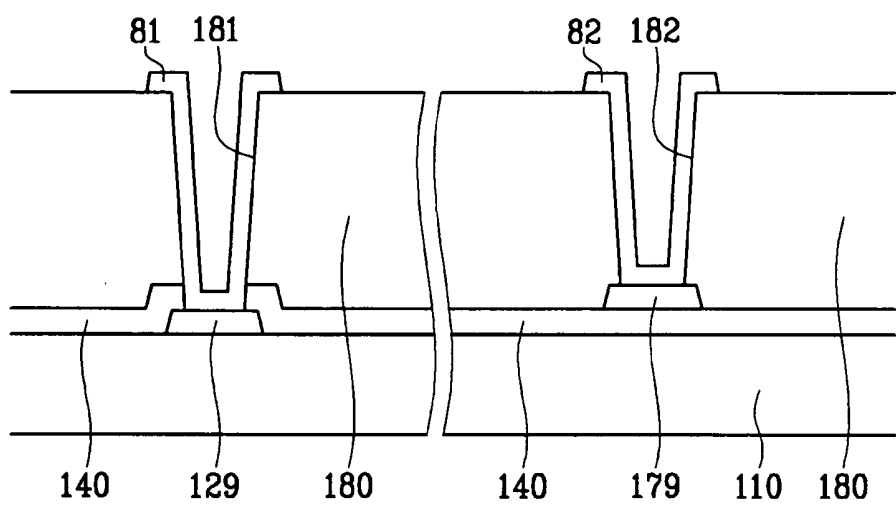


FIG. 9



LIQUID CRYSTAL DISPLAY AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This Application claims priority from Korean patent application number 10-2005-0091141 filed on Sep. 29, 2005, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Technical Field

[0003] The present invention relates to a liquid crystal display and a method for manufacturing the same and, more particularly, to a liquid crystal display and a method for manufacturing same in which the number of lithography processes is reduced.

[0004] 2. Discussion of the Related Art

[0005] A conventional liquid crystal display (LCD) includes two panels provided with field-generating electrodes such as pixel electrodes and a common electrode, and a liquid crystal (LC) layer interposed therebetween. The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer, which determines orientations of LC molecules in the LC layer to adjust polarization of incident light.

[0006] The LCD may have a layered structure including several thin films, and several photolithography processes may be employed in manufacturing the LCD panel.

[0007] However, because the photolithography processes include complicated steps, the LCD panels are costly to produce. The production costs and time increase as the number of photolithography processes increase. Therefore, it is desirable to reduce the number of photolithography steps.

SUMMARY OF THE INVENTION

[0008] A liquid crystal display includes a first substrate, a first electrode formed on the first substrate, a passivation layer formed between the first substrate and the first electrode, a second substrate facing the first substrate, a second electrode formed on the second substrate, a columnar spacer formed between the second substrate and the first substrate, and a liquid crystal layer having liquid crystal molecules vertically aligned with respect to the first and second substrates, and formed between the first and second substrates. The passivation layer and the columnar spacer are made of substantially the same material at the same layer.

[0009] The liquid crystal display may further include a gate line and a data line formed on the first substrate, and a thin film transistor connected to the gate line and the data line.

[0010] A color filter may be formed on the second substrate of the liquid crystal display, or a light-blocking member may be formed thereon.

[0011] The second electrode may include a plurality of cutouts.

[0012] The liquid crystal display may further include a slope member formed between the passivation layer and the first electrode. The slope member may include a ridge protruding upward and an inclined surface. The ridge and the cutouts of the second electrode may be alternatively arranged.

[0013] The slope member, the passivation layer, and the columnar spacers may be made of the same layer and of substantially the same material. The slope member, the passivation layer, and the columnar spacers may be formed by a mold.

[0014] A method for manufacturing a liquid crystal display includes coating an organic layer on a substrate, pressing the organic layer by using a mold, forming a thin film by absorbing solvent from the organic layer into the mold to harden the organic layer, and removing the mold from the substrate.

[0015] The method may further include removing a pressed portion of the organic layer after the removal of the mold, or soft-baking the mold while absorbing solvent from the organic layer and the organic layer to further harden the organic layer before removing the mold.

[0016] The thin film may include a passivation layer having a contact hole, it may include a slope member and a columnar spacer, or it may include a passivation layer having a contact hole, a slope member, and a columnar spacer.

[0017] The mold may include polydimethylsiloxane.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Exemplary embodiments of the present invention can be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings in which:

[0019] FIG. 1 shows a layout view of an LCD according to an embodiment of the present invention;

[0020] FIG. 2 shows a sectional view of the LCD of FIG. 1 taken along the line II-II';

[0021] FIG. 3 shows sectional views of the LCD of FIG. 1 taken along the lines III-III' and III"-III''';

[0022] FIGS. 4A to 4E show sectional views of a passivation layer of an LCD in an intermediate step of a manufacturing method according to an embodiment of the present invention;

[0023] FIGS. 5A to 5E show sectional views of a passivation layer, a slope member and a columnar spacer of an LCD in an intermediate step of a manufacturing method according to an embodiment of the present invention;

[0024] FIGS. 6A to 6E show sectional views of a passivation layer, a slope member, and a columnar spacer of an LCD in an intermediate step of a manufacturing method according to an embodiment of the present invention;

[0025] FIG. 7 shows a layout view of an LCD according to an embodiment of the present invention;

[0026] FIG. 8 shows a sectional view of the LCD of FIG. 7 taken along the line VIII-VIII'; and

[0027] FIG. 9 shows sectional views of the LCD of FIG. 7 taken along the lines IX-IX' and IX"-IX'''.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0028] Exemplary embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like numerals refer to like elements throughout.

[0029] An LCD according to an embodiment of the present invention will be described in detail with reference to FIGS. 1-3. FIG. 1 shows a layout view of an LCD according to an embodiment of the present invention, FIG. 2 shows a sectional view of the LCD of FIG. 1 taken along the line II-II', and FIG. 3 shows sectional views of the LCD of FIG. 1 taken along the lines III-III' and III"-III'''.

[0030] Referring to FIGS. 1-3, an LCD according to an embodiment of the present invention includes a thin film transistor (TFT) array panel 100, a common electrode panel 200, and an LC layer 3 interposed between the TFT array and common electrode panels 100 and 200.

[0031] A plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on an insulating substrate 110 made of a material such as transparent glass.

[0032] The gate lines 121 extend substantially in a transverse direction, are separated from each other and transmit gate signals. Each gate line 121 includes a plurality of projections forming a plurality of gate electrodes 124 and an end portion 129 having a large area for contact with another layer (not shown) or an external driving circuit (not shown). A gate driving circuit (not shown) for generating the gate signals may be mounted on a flexible printed circuit (FPC) film (not shown), which may be attached to the insulating substrate 110, directly mounted on the insulating substrate 110, or integrated with the insulating substrate 110. The gate lines 121 may extend to be connected to a driving circuit (not shown) that may be integrated with the insulating substrate 110.

[0033] Each storage electrode line 131 extends substantially in the transverse direction and is disposed between two adjacent gate lines 121 and close to an upper one of the two gate lines 121. Each storage electrode line 131 includes a plurality of branches forming first through fourth storage electrodes 133a-133d, wherein storage electrode connections 133e connect the first and second storage electrodes 133a and 133b.

[0034] The first and second storage electrodes 133a and 133b are disposed longitudinally and are spaced apart from each other, and the third and fourth storage electrodes 133c and 133d are disposed obliquely and are connected between the first and second storage electrodes 133a and 133b. In detail, the first storage electrode 133a has a free end portion and a fixed end portion that is connected to the storage electrode line 131, and has a projection. The third and fourth storage electrodes 133c and 133d extend approximately from a center of the first storage electrode 133a to upper and lower ends of the second storage electrode 133b, respectively.

[0035] The storage electrode lines 131 are supplied with a predetermined voltage such as a common voltage, which is applied to a common electrode 270 on the common electrode panel 200 of the LCD. Each storage electrode line 131 may include a pair of stems extending in the transverse direction, and may have various shapes and arrangements.

[0036] The gate lines 121 and the storage electrode lines 131 are preferably made of an Al-containing metal such as Al and an Al alloy, a Ag-containing metal such as Ag and a Ag alloy, a Cu-containing metal such as Cu and a Cu alloy, a Mo-containing metal such as Mo and a Mo alloy, Cr, Ta, or Ti. However, they may have a multi-layered structure including two conductive films (not shown) having different physical characteristics. One of the two conductive films is preferably made of a low resistivity metal including, for example, an Al-containing metal, a Ag-containing metal, and/or a Cu-containing metal for reducing signal delay or voltage drop. The other conductive film is preferably made of a material such as a Mo-containing metal, Cr, Ta, or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Good examples of the combination of the two conductive films are a lower Cr conductive film and an upper Al (alloy) conductive film and a lower Al (alloy) conductive film and an upper Mo (alloy) conductive film. However, the gate lines 121 and the storage electrode lines 131 may be made of various metals or conductors.

[0037] In addition, the lateral sides of the gate lines 121 and the storage electrode lines 131 are inclined relative to a surface of the substrate, and the inclination angle thereof ranges from about 30 degrees to about 80 degrees.

[0038] A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121 and the storage electrode lines 131.

[0039] A plurality of semiconductor stripes 151 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") or polysilicon are formed on the gate insulating layer 140. Each semiconductor stripe 151 extends substantially in the longitudinal direction and has a plurality of projections 154 branched out toward the gate electrodes 124. The semiconductor stripes 151 become wide near the gate lines 121 and the storage electrode lines 131 such that the semiconductor stripes 151 cover the gate lines 121 and the storage electrode lines 131.

[0040] A plurality of ohmic contact stripes and islands 161 and 165 are formed on the semiconductor stripes 151. The ohmic contact stripes and islands 161 and 165 are preferably made of n+ hydrogenated a-Si heavily doped with an n-type impurity such as phosphorous, or they may be made of silicide. Each ohmic contact stripe 161 includes a plurality of projections 163, and the projections 163 and the ohmic contact islands 165 are located in pairs on the projections 154 of the semiconductor stripes 151.

[0041] The lateral sides of the semiconductor stripes 151 and the ohmic contact stripes and islands 161 and 165 are tapered, and the inclination angles thereof range from about 30 degrees to about 80 degrees.

[0042] A plurality of data lines 171, a plurality of drain electrodes 175 that are separated from the data lines 171, and

a plurality of isolated metal pieces **178** are formed on the ohmic contact stripes and islands **161** and **165** and the gate insulating layer **140**.

[0043] The data lines **171** for transmitting data voltages extend substantially in the longitudinal direction and cross the gate lines **121** at right angles. The data lines **171** also intersect the storage electrode lines **131** and the storage electrode connections **133e** such that each data line **171** is disposed between adjacent first and second storage electrodes **133a** and **133b**. Each data line **171** includes an end portion **179** having a large area for contact with another layer or an external device. Each data line **171** includes a plurality of source electrodes projecting toward the drain electrodes **175**. A data driving circuit (not shown) for generating the data signals may be mounted on an FPC film (not shown), which may be attached to the insulating substrate **110**, directly mounted on the insulating substrate **110**, or integrated with the insulating substrate **110**. The data lines **171** may extend to be connected to a driving circuit that may be integrated with the insulating substrate **110**.

[0044] Each drain electrode **175** includes an end portion having a large area for contact with another layer, and another end portion disposed on a gate electrode **124** and partly enclosed by a source electrode **173**.

[0045] A gate electrode **124**, a source electrode **173**, and a drain electrode **175** along with a projection **154** of a semiconductor stripe **151** form a TFT having a channel formed in the projection **154** disposed between the source electrode **173** and the drain electrode **175**.

[0046] The metal pieces **178** are disposed on the gate lines **121** near the end portions of the first storage electrodes **133a**.

[0047] The data lines **171**, the drain electrodes **175**, and the metal pieces **178** are preferably made of a refractory metal such as Cr, Mo, Ti, Ta, or alloys thereof. However, they may also have a multilayered structure including a low-resistivity film (not shown) and a good-contact film (not shown). A good example of the combination is a lower Mo film, an intermediate Al film, and an upper Mo film as well as the above-described combinations of a lower Cr film and an upper Al alloy film and a lower Al film and an upper Mo film. However, the data lines **171** and the drain electrodes **175** may be made of various metals or conductors.

[0048] Like the gate lines **121** and the storage electrode lines **131**, the data lines **171** and the drain electrodes **175** have tapered lateral sides, and the inclination angles thereof range from about 30 degrees to about 80 degrees.

[0049] The ohmic contact stripes and islands **161** and **165** are interposed only between the underlying semiconductor stripes **151** and the overlying data lines **171** and the overlying drain electrodes **175** thereon, and reduce the contact resistance therebetween. The semiconductor stripes **151** include a plurality of exposed portions, which are not covered with the data lines **171** and the drain electrodes **175**, such as portions located between the source electrodes **173** and the drain electrodes **175**. Although the semiconductor stripes **151** are narrower than the data lines **171** at most places, the width of the semiconductor stripes **151** becomes large near the gate lines **121** and the storage electrode lines **131** as described above, to smooth the profile of the surface, thereby preventing the disconnection of the data lines **171**.

[0050] A passivation layer **180**, preferably made of an inorganic or organic insulator, may have a flat top surface. Examples of the inorganic insulator include silicon nitride and silicon oxide. The organic insulator may have photosensitivity and a dielectric constant less than about 4.0. The passivation layer **180** may include a lower film of an inorganic insulator and an upper film of an organic insulator such that it takes the excellent insulating characteristics of the organic insulator while protecting the exposed portions of the semiconductor stripes **151** from being damaged by the organic insulator.

[0051] The passivation layer **180** has a plurality of contact holes **182** and **185** exposing the end portions **179** of the data lines **171** and the end portions of the drain electrodes **175**, respectively. The passivation layer **180** and the gate insulating layer **140** have a plurality of contact holes **181** exposing the end portions **129** of the gate lines **171**, a plurality of contact holes **183a** exposing portions of the storage electrode lines **131** near the fixed end portions of the first storage electrodes **133a**, and a plurality of contact holes **183b** exposing the projections of the free end portions of the first storage electrodes **133a**.

[0052] A plurality of columnar spacers **320** and a plurality of slope members **330a** and **330b** are formed in the passivation layer **180**.

[0053] The columnar spacers **320** and the slope members **330a** and **330b** may be made of the same layer as the passivation layer **180**, and may be made of the same material as that of the passivation layer **180**.

[0054] The slope members **330a** and **330b** include a ridge indicated by a thick dotted line in FIG. 1, and an inclined surface of which the height is gradually reduced from the ridge to the edge of the slope members **330a** and **330b**. The ridge of the slope members **330a** and **330b** substantially has inversion symmetry with respect to an imaginary transverse line bisecting the pixel electrode **191**.

[0055] The ridges of the lower and upper slope members **330a** and **330b** obliquely extend from a right edge of the pixel electrode **191** near an upper right corner approximately to a center of a left edge of the pixel electrode **191**, and overlap the third and fourth storage electrodes **133c** and **133d**. The lower and upper slope members **330a** and **330b** are disposed at lower and upper halves of the pixel electrode **191**, respectively, which can be divided by the imaginary transverse line. The ridges of the lower and upper slope members **330a** and **330b** make an angle of about 45 degrees with the gate lines **121**, and they extend substantially perpendicular to each other.

[0056] The columnar spacers **320** support the interval between the TFT array panel **100** and the common electrode panel **200** along with the passivation layer **180**.

[0057] A plurality of pixel electrodes **191**, a plurality of contact assistants **81** and **82**, and a plurality of overpasses **83**, which are preferably made of a transparent conductor such as ITO or IZO or a reflective conductor such as Ag or Al, are formed on the passivation layer **180** and the slope members **330a** and **330b**.

[0058] The pixel electrodes **191** are physically and electrically connected to the drain electrodes **175** through the

contact holes **185** such that the pixel electrodes **191** receive the data voltages from the drain electrodes **175**.

[0059] The pixel electrodes **191** are supplied with the data voltages and generate electric fields in cooperation with the common electrode **270**, which determine orientations of liquid crystal molecules (not shown) in the liquid crystal layer **3**.

[0060] A pixel electrode **191** and the common electrode **270** form a liquid crystal capacitor, which stores applied voltages after deactivation of the TFT. An additional capacitor called a "storage capacitor," which is connected in parallel with the liquid crystal capacitor, is provided for enhancing the voltage storing capacity. The storage capacitors are implemented by overlapping the pixel electrodes **191** with the storage electrode lines **131** including the first through fourth storage electrodes **133a-133d**.

[0061] Each pixel electrode **191** is chamfered at its left corners, and the chamfered edges of the pixel electrode **191** make an angle of about 45 degrees with the gate lines **121**.

[0062] The contact assistants **81** and **82** are connected to the end portions **129** of the gate lines **121** and the end portions **179** of the data lines **171** through the contact holes **181** and **182**, respectively. The contact assistants **81** and **82** protect the end portions **129** and **179** and complement the adhesion of the end portions **129** and **179** and external devices.

[0063] The overpasses **83** cross over the gate lines **121** and are connected to the exposed projection of the fixed end portions of the first storage electrodes **133a** and the exposed portions of the storage electrode lines **131** through the contact holes **183b** and **183a**, respectively, which are disposed opposite each other with respect to the gate lines **121**. The overpasses **83** overlap the metal pieces **178**, and may be electrically connected to the metal pieces **178**. The storage electrode lines **131** including the first through fourth storage electrodes **133a-133d** along with the overpasses **83** and the metal pieces **178** are used for repairing defects in the gate lines **121**, the data lines **171**, or the TFTs. The electrical connection between the gate lines **121** and the storage electrode lines **131** for repairing the gate lines **121** is obtained by illuminating the crossing points of the gate lines **121** and the overpasses **83** with a laser beam to electrically connect the gate lines **121** to the overpasses **83**. In this case, the metal pieces **178** enhance the electrical connection between the gate lines **121** and the overpasses **83**.

[0064] A description of the common electrode panel **200** follows with reference to FIGS. **1** and **2**.

[0065] A light-blocking member **220** called a black matrix for preventing light leakage is formed on an insulating substrate **210** made of a material such as transparent glass. The light-blocking member **220** may include a plurality of openings **225** that face the pixel electrodes **191** and may have substantially the same planar shape as the pixel electrodes **191**. Otherwise, the light-blocking member **220** may include linear portions corresponding to the data lines **171** and other portions corresponding to the TFTs.

[0066] A plurality of color filters **230** are formed on the flexible substrate **210** and are disposed substantially in the areas enclosed by the light-blocking member **220**. The color filters **230** may extend substantially in the longitudinal

direction along the pixel column such that they may be stripe shaped. The color filters **230** may represent one of the primary colors such as red, green, or blue colors.

[0067] An overcoat **250** for preventing the color filters **230** from being exposed and for providing a flat surface is formed on the color filters **230** and the light-blocking member **220**. The overcoat **250** may be omitted.

[0068] A common electrode **270**, preferably made of a transparent conductive material such as ITO and IZO, is formed on the overcoat **250**. The common electrode **270** has a plurality of sets of cutouts including a center cutout **71**, a lower cutout **72a** and an upper cutout **72b** facing a pixel electrode **191**. Each of the cutouts **71-72b** is disposed between adjacent ridges of the slope members **330a** and **330b**, and/or between the slope members **330a** and **330b** and a chamfered edge of the pixel electrode **191**. In addition, each of the cutouts **71-72b** has at least an oblique portion extending parallel to the slope members **330a** and **330b**. The cutouts **71-72b** substantially have inversion symmetry with respect to the above-described transverse line bisecting the pixel electrode **191**.

[0069] Each of the lower and upper cutouts **72a** and **72b** includes an oblique portion extending approximately from a left edge of the pixel electrode **191** approximately to lower or upper edges of the pixel electrode **191**, and transverse and longitudinal portions extending from respective ends of the oblique portion along edges of the pixel electrode **191**, overlapping the edges of the pixel electrode **191**, and making obtuse angles with the oblique portion.

[0070] The center cutout **71** includes a central transverse portion extending approximately from the left edge of the pixel electrode **191** along the third storage electrode **133c**, a pair of oblique portions extending from an end of the central transverse portion approximately to a right edge of the pixel electrode and making obtuse angles with the central transverse portion, and a pair of terminal longitudinal portions extending from the ends of the respective oblique portions along the right edge of the pixel electrode **191**, overlapping the right edge of the pixel electrode **191**, and making obtuse angles with the respective oblique portions.

[0071] The number of cutouts **71-72b** may be varied depending on design factors, and the light-blocking member **220** may also overlap the cutouts **71-72b** to block the light leakage through the cutouts **71-72b**.

[0072] Alignment layers **11** and **21** that may be homeotropic are coated on inner surfaces of the TFT array and common electrode panels **100** and **200**, and polarizers **12** and **22** are provided on outer surfaces of the TFT array and common electrode panels **100** and **200** such that their polarization axes may be crossed and one of the transmissive axes may be parallel to the gate lines **121**. One of the polarizers may be omitted when the LCD is a reflective LCD.

[0073] The LCD may further include at least one retardation film (not shown) for compensating the retardation of the LC layer **3**. The retardation film has birefringence and gives a retardation opposite to that given by the LC layer **3**. The retardation film may include a uniaxial or biaxial optical compensation film, and in particular, a negative uniaxial compensation film.

[0074] The LCD may further include a backlight unit (not shown) for supplying light to the LC layer 3 through the polarizers 12 and 22, the retardation film, and the TFT array and common electrode panels 100 and 200.

[0075] It is preferable that the LC layer 3 has negative dielectric anisotropy and is subjected to a vertical alignment such that the LC molecules in the LC layer 3 are aligned such that their long axes are substantially vertical to the surfaces of the TFT array and common electrode panels 100 and 200 in the absence of an electric field.

[0076] As shown in FIG. 1, a set of the cutouts 71-72b and the slope members 330a and 330b divides a pixel electrode 191 into a plurality of sub-areas, and each sub-area has two major edges.

[0077] The cutouts 71-72b and the slope members 330a and 330b control the tilt directions of the LC molecules in the LC layer 3.

[0078] Upon application of the common voltage to the common electrode 270 and a data voltage to the pixel electrodes 191, an electric field substantially perpendicular to the surfaces of the TFT array and common electrode panels 100 and 200 is generated. The LC molecules tend to change their orientations in response to the electric field such that their long axes are perpendicular to the field direction.

[0079] The LC molecules are pre-tilted by the slope members 330a and 330b in the absence of the electric field, and the pre-tilt directions of the LC molecules determines the tilt directions of the LC molecules upon application of the electric field, which coincide with the tilt directions determined by the cutouts 71-72b and the chamfered edge of the pixel electrode 191.

[0080] In addition, the slope members 330a and 330b having varying thickness distort the equipotential lines of the electric field, and the distortion of the equipotential lines gives the tilting force which also coincides with the tilt directions determined by the cutouts 71-72b when the dielectric constant of the slope members 330a and 330b is lower than that of the LC layer 3.

[0081] Accordingly, the tilt directions of the LC molecules far from the cutouts 71-72b and the chamfered edges of the pixel electrodes 191 are also determined to reduce the response time of the LC molecules.

[0082] The cutouts 71-72b of the common electrode 270, the slope members 330a and 330b of the passivation layer 180 and the edges of the pixel electrodes 191 distort the electric field to have a horizontal component that is substantially perpendicular to the edges of the cutouts 71-72b and the edges of the pixel electrodes 191. Accordingly, the LC molecules on each sub-area are tilted in a direction by the horizontal component and the azimuthal distribution of the tilt directions are localized to four directions, thereby increasing the viewing angle of the LCD.

[0083] At least one of the cutouts 71-72b can be substituted with protrusions (not shown) or depressions (not shown). The protrusions are preferably made of an organic or inorganic material and disposed on or under the field-generating electrodes 191 or 270.

[0084] The shapes and the arrangements of the cutouts 71-72b and the slope members 330a and 330b may be modified.

[0085] Since the tilt directions of all domains make an angle of about 45 degrees with the gate lines 121, which are parallel or perpendicular to the edges of the TFT array and common electrode panels 100 and 200, and the 45-degree intersection of the tilt directions and the transmissive axes of the polarizers 12 and 22 gives maximum transmittance, the polarizers 12 and 22 can be attached such that the transmissive axes of the polarizers 12 and 22 are parallel or perpendicular to the edges of the TFT array and common electrode panels 100 and 200 and it reduces the production cost.

[0086] The passivation layer 180, the slope members 330a and 330b, and the columnar spacers 320 in the LCD according to an embodiment of the present invention may be made of the same layer, and may include substantially the same material.

[0087] Now, the manufacturing method for forming the passivation layer 180, the slope members 330a and 330b, and the columnar spacers 320 is described for the LCD according to an embodiment of the present invention, with reference to FIGS. 4A to 5E.

[0088] FIGS. 4A to 4E show sectional views of a passivation layer of an LCD in an intermediate step of a manufacturing method according to an embodiment of the present invention, and FIGS. 5A to 5E show sectional views of a passivation layer, a slope member, and a columnar spacer of an LCD in an intermediate step of a manufacturing method according to an embodiment of the present invention.

[0089] As shown in FIG. 4A, an organic insulating layer 180a is coated on an insulating substrate 110 and, as shown in FIG. 4B, a mold 50 having a depression 52 corresponding to the passivation layer 180 (FIGS. 2 and 3) and a projection 51 corresponding to the contact holes 181, 182, 183a, 183b, and 185 (FIGS. 2 and 3) is aligned with the organic insulating layer 180a and presses the organic insulating layer 180a. The mold 50 may be formed of polydimethylsiloxane, and the organic insulating layer may include a thermal hardening resin.

[0090] As shown in FIG. 4C, the mold 50 including polydimethylsiloxane absorbs solvent from the organic insulating layer 180a during the application of pressure, and the organic insulating layer 180a is hardened. Here, a soft-bake treatment may be added to further harden the organic insulating layer 180a.

[0091] As shown in FIG. 4D, the mold 50 is removed from the hardened organic insulating layer 180b, and a portion 44 that is pressed by the mold is dry-etched to complete the contact hole 185, as shown in FIG. 4E.

[0092] Because the passivation layer 180 has only the contact holes 181, 182, 183a, 183b, and 185, the process using the mold 50 is more effective than a photolithography process using a mask for forming the passivation layer 180, and more particularly, the process may reduce production time and costs for manufacturing the LCD by omitting an exposure step and a developing step.

[0093] Furthermore, because the exposure step is omitted in this method for forming the passivation layer 180, the organic insulating layer does not include a photo acid generator (PAG). Accordingly, the cost of materials for forming the passivation layer 180 is lower and the deposition of the materials is simplified.

[0094] As shown in FIG. 5A, an organic insulating layer 33a is coated on an insulating substrate 110 and, as shown in FIG. 5B, a mold 53 having depressions 54 and 55 corresponding to the columnar spacers 320 and the slope members 330a and 330b of FIGS. 1 and 2 is aligned with the organic insulating layer 33a and presses the organic insulating layer 33a. The mold 53 may be formed of polydimethylsiloxane, and the organic insulating layer may include a thermal hardening resin.

[0095] As shown in FIG. 5C, the mold 53 including polydimethylsiloxane absorbs solvent from the organic insulating layer 33a during the application of pressure and the organic insulating layer 33a is hardened. Here, a soft-bake treatment may be added to further harden the organic insulating layer 33a.

[0096] As shown in FIG. 5D, the mold 53 is removed from the hardened organic insulating layer 33b, and portions 45 and 46 pressed by the mold 53 are dry-etched to simultaneously complete the columnar spacer 320 and the slope member 330b, as shown in FIG. 5E.

[0097] This method for manufacturing the columnar spacers 320 and the slope members 330a and 330b may reduce production time and costs by omitting an exposure step and a developing step. Furthermore, because the exposure step is omitted, the organic insulating layer may omit a PAG. Accordingly, the cost of materials for forming the passivation layer 180 is reduced and the deposition of the materials is simplified.

[0098] The passivation layer 180, columnar spacer 320, and the slope members 330a and 330b are simultaneously formed using one mold according to an embodiment of the present invention, which will be described with reference to FIGS. 6A to 6E.

[0099] FIGS. 6A to 6E show sectional views of a passivation layer, a slope member, and a columnar spacer of an LCD in an intermediate step of a manufacturing method according to an embodiment of the present invention.

[0100] As shown in FIG. 6A, an organic insulating layer 400a is coated on an insulating substrate 110, and a mold 56 having depressions 58 and 59 corresponding to the columnar spacer 320 and the slope member 330b (FIG. 2) and a projection 57 corresponding to the contact hole 185 is aligned with the organic insulating layer 400a and presses the organic insulating layer 400a. The mold 56 may be formed of polydimethylsiloxane, and the organic insulating layer may include a thermal hardening resin.

[0101] As shown in FIG. 6C, the mold 56 including polydimethylsiloxane soaks up the solvent of the organic insulating layer 400a on the application of the pressure and the organic insulating layer 400a is hardened. Here, a soft-bake treatment may be added to further harden the organic insulating layer 400a.

[0102] As shown in FIG. 6D, the mold 56 is removed from the hardened organic insulating layer 400b, and portions 44, 45 and 46 pressed by the mold 56 are dry-etched to simultaneously complete the passivation layer 180 including the contact hole 185, the columnar spacer 320, and the slope members 330a and 330b, as shown in FIG. 6E.

[0103] This method of manufacturing the passivation layer 180, the columnar spacer 320, and the slope member 330b may reduce production time and costs by omitting an exposure step and a developing step, compared with the photolithography process.

[0104] Furthermore, the passivation layer 180, the columnar spacer 320, and the slope members 330a and 330b may be simultaneously formed by using one mold, and accordingly production time and costs may be further reduced.

[0105] Because the exposure step is omitted in this method for forming the passivation layer 180, the columnar spacer 320, and the slope members 330a and 330b, the organic insulating layer does not include a PAG. Accordingly, the cost of materials for forming the passivation layer 180 is reduced and the deposition of the materials is simplified.

[0106] An LCD according to another embodiment of the present invention will be described in detail with reference to FIGS. 6 and 7.

[0107] FIG. 7 shows a layout view of an LCD according to an embodiment of the present invention, FIG. 8 shows a sectional view of the LCD of FIG. 7 taken along the line VIII-VIII', and FIG. 9 shows sectional views of the LCD of FIG. 7 taken along the lines IX-IX' and IX"-IX'''.

[0108] Referring to FIGS. 7 to 9, an LCD also includes a TFT array panel 100, a common electrode panel 200, an LC layer 3, a plurality of columnar spacers 320 interposed between the TFT array and common electrode panels 100 and 200, and a pair of polarizers 12 and 22 attached on outer surfaces of the TFT array and common electrode panels 100 and 200.

[0109] Layered structures of the TFT array and common electrode panels 100 and 200 according to this embodiment are almost the same as those shown in FIGS. 1-3.

[0110] Regarding the TFT array panel 100, a plurality of gate lines 121 including gate electrodes 124 and end portions 129 and a plurality of storage electrode lines 131 connecting with a plurality of first through fourth storage electrodes 133a-133d and storage electrode connections 133e are formed on an insulating substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including projections 154, and a plurality of ohmic contact stripes 161 including projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including source electrodes 173 and end portions 179, a plurality of drain electrodes 175, and a plurality of isolated metal pieces 178 are formed on the ohmic contact stripes and islands 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 181, 182, 183a, 183b, and 185 are provided at the passivation layer 180 and the gate insulating layer 140. A plurality of columnar spacers 320 and a plurality of slope members 330a and 330b are formed on the passivation layer 180, and a plurality of pixel electrodes 191, a plurality of contact assistants 81 and 82, and a plurality of overpasses 83 are formed on the passivation layer 180 and the slope members 330a and 330b, and an alignment layer 11 is coated thereon.

[0111] Regarding the common electrode panel 200, a light-blocking member 220 having a plurality of openings 225, a plurality of color filters 230, a common electrode 270, and an alignment layer 21 are formed on an insulating substrate 210.

[0112] The semiconductor stripes 151 of the TFT array panel 100 according to this embodiment have similar planar shapes as the data lines 171 and the drain electrodes 175 of FIGS. 1-3 as well as the underlying ohmic contact stripes and islands 161 and 165. However, the projections 154 of the semiconductor stripes 151 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0113] Furthermore, the TFT array panel 100 further includes a plurality of semiconductor islands (not shown) and a plurality of ohmic contact islands (not shown) disposed thereon, which are disposed on the metal pieces 178.

[0114] A manufacturing method of the TFT array panel according to an embodiment of the present invention simultaneously forms the data lines 171, the drain electrodes 175, the metal pieces 178, the semiconductors 151, and the ohmic contact stripes and islands 161 and 165 using one photolithography process.

[0115] A photoresist pattern for the photolithography process has position-dependent thickness, and in particular, it has first and second portions with decreased thickness. The first portions are located on wire areas that will be occupied by the data lines 171, the drain electrodes 175, and the metal pieces 178, and the second portions are located on channel areas of TFTs.

[0116] The position-dependent thickness of the photoresist may be obtained by several techniques, for example, by providing translucent areas on the exposure mask as well as transparent areas and light-blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, or have thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is to use a reflowable photoresist. In detail, once a photoresist pattern made of a reflowable material is formed by using a normal exposure mask with only transparent areas and opaque areas, it is subject to reflow process to flow onto areas without the photoresist, thereby forming thin portions. As a result, the manufacturing process is simplified by omitting a photolithography step.

[0117] Furthermore, the common electrode panel 200 includes a plurality of sets of protrusions including a center protrusion 61, a lower protrusion 62a, and an upper protrusion 62b disposed on the common electrode 270. The protrusions 61-62b are preferably made of an inorganic insulator or an organic insulator.

[0118] In addition, the common electrode 270 has no cutouts and thus there is no overcoat, although the omission of the overcoat is optional.

[0119] Although there are no cutouts at the common electrode panel 200, the protrusions 61-62b can sufficiently play a role of determining tilt directions along with the slope members 330a and 330b of the thin film transistor panel 100.

[0120] The portion of the alignment layer 21 on the protrusions 61-62b is also protruded, and has inclined surfaces. Because the alignment layer 21 is homeotropic, the LC molecules are vertically aligned with respect to the surface of the alignment layer 21, and they are pre-tilted by the protrusions 61-62b in absence of an electric field.

[0121] In addition, because the dielectric constant of the protrusions 61-62b is lower than that of the LC layer 3, the protrusions 61-62b distort the equipotential lines of the electric field, and the distortion of the equipotential lines gives the tilting force which also coincides with the tilt directions determined by the slope members 330a and 330b.

[0122] Each set of the protrusions 61-62b faces a pixel electrode 191 and is located at the same positions as that of the cutouts 71-72b of FIGS. 1 to 3.

[0123] Like the description of the cutouts 71-72b of FIGS. 1-3, a set of the protrusions 61-62b and the slope members 330a and 330b divides a pixel electrode 191 into a plurality of sub-areas and each sub-area has two major edges.

[0124] The protrusions 61-62b, the slope members 330a and 330b of the passivation layer 180 and the edges of the pixel electrodes 191 distort the electric field to have a horizontal component that is substantially perpendicular to the edges of the protrusions 61-62b and the edges of the pixel electrodes 191. Accordingly, the LC molecules on each sub-area are tilted in a direction by the horizontal component and the azimuthal distribution of the tilt directions are localized to four directions, thereby increasing the viewing angle of the LCD.

[0125] The protrusions 61-62b may be formed under the common electrode 270.

[0126] The passivation layer 180, the columnar spacers 320, and the slope members 330a and 330b may be formed as in FIGS. 4A-6B, and accordingly production time and cost may be further reduced.

[0127] Because the exposure step is omitted in this method for forming the passivation layer 180, the columnar spacers 320, and the slope members 330a and 330b, the organic insulating layer does not include a PAG. Accordingly, the cost of the materials for forming the passivation layer 180 is lower and the deposition of the materials is simplified.

[0128] The omission of the cutouts removes a lithography step for forming cutouts at the common electrode 270.

[0129] Many of the above-described features of the LCD shown in FIGS. 1-3 may be appropriate for the TFT array panel shown in FIGS. 7-9.

[0130] As described above, the passivation layer, the columnar spacers, and the slope members may be formed using the mold, and accordingly the photolithography process may be omitted such that the production time and the cost may be further reduced.

[0131] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications

and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A liquid crystal display, comprising:

a first substrate;

a first electrode formed on the first substrate;

a passivation layer formed between the first substrate and the first electrode;

a second substrate facing the first substrate;

a second electrode formed on the second substrate;

a columnar spacer formed between the second substrate and the first substrate; and

a liquid crystal layer having liquid crystal molecules vertically aligned with respect to the first and second substrates, and formed between the first and second substrates,

wherein the passivation layer and the columnar spacer are made of substantially the same material at the same layer.

2. The liquid crystal display of claim 1, further comprising:

a gate line and a data line formed on the first substrate; and

a thin film transistor connected to the gate line and the data line,

wherein the thin film transistor is connected to the first electrode.

3. The liquid crystal display of claim 1, further comprising a color filter formed on the second substrate.

4. The liquid crystal display of claim 3, further comprising a light-blocking member formed on the second substrate.

5. The liquid crystal display of claim 1, wherein the second electrode includes a plurality of cutouts.

6. The liquid crystal display of claim 1, further comprising a slope member formed between the passivation layer and the first electrode.

7. The liquid crystal display panel of claim 6, wherein the slope member includes a ridge protruding upward and an inclined surface.

8. The liquid crystal display panel of claim 7, wherein the ridge and the cutouts of the second electrode are alternatively arranged.

9. The liquid crystal display of claim 6, wherein the slope member, the passivation layer, and the columnar spacers are made of the same layer and of substantially the same material.

10. The liquid crystal display panel of claim 6, wherein the slope member, the passivation layer, and the columnar spacers are formed by a mold.

11. A method for manufacturing a liquid crystal display, comprising:

coating an organic layer on a substrate;

pressing the organic layer by using a mold;

forming a thin film by absorbing solvent from the organic layer into the mold to harden the organic layer; and

removing the mold from the substrate.

12. The method of claim 11, further comprising:

removing a pressed portion of the organic layer after the removal of the mold.

13. The method of claim 11, further comprising soft-baking the mold while absorbing solvent from the organic layer and the organic layer to further harden the organic layer before removing the mold.

14. The method of claim 11, wherein the thin film comprises a passivation layer having a contact hole.

15. The method of claim 11, wherein the thin film comprises a slope member and a columnar spacer.

16. The method of claim 11, wherein the thin film comprises a passivation layer having a contact hole, a slope member, and a columnar spacer.

17. The method of claim 11, wherein the mold includes polydimethylsiloxane.

* * * * *

专利名称(译)	液晶显示器及其制造方法		
公开(公告)号	US20070070287A1	公开(公告)日	2007-03-29
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[标]申请(专利权)人(译)	三星电子株式会社		
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其他公开文献	US7595855		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示器包括第一基板，形成在第一基板上的第一电极，形成在第一基板和第一电极之间的钝化层，面向第一基板的第二基板，形成在第二基板上的第二电极，柱状在第二基板和第一基板之间形成间隔物，和具有相对于第一和第二基板垂直对准的液晶分子的液晶层，并形成在第一和第二基板之间。钝化层和柱状衬垫料在同一层由基本相同的材料制成。

