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(54) IN-PLANE SWITCHING LIQUID CRYSTAL DISPLAY DEVICE HAVING STORAGE CAPACITORS

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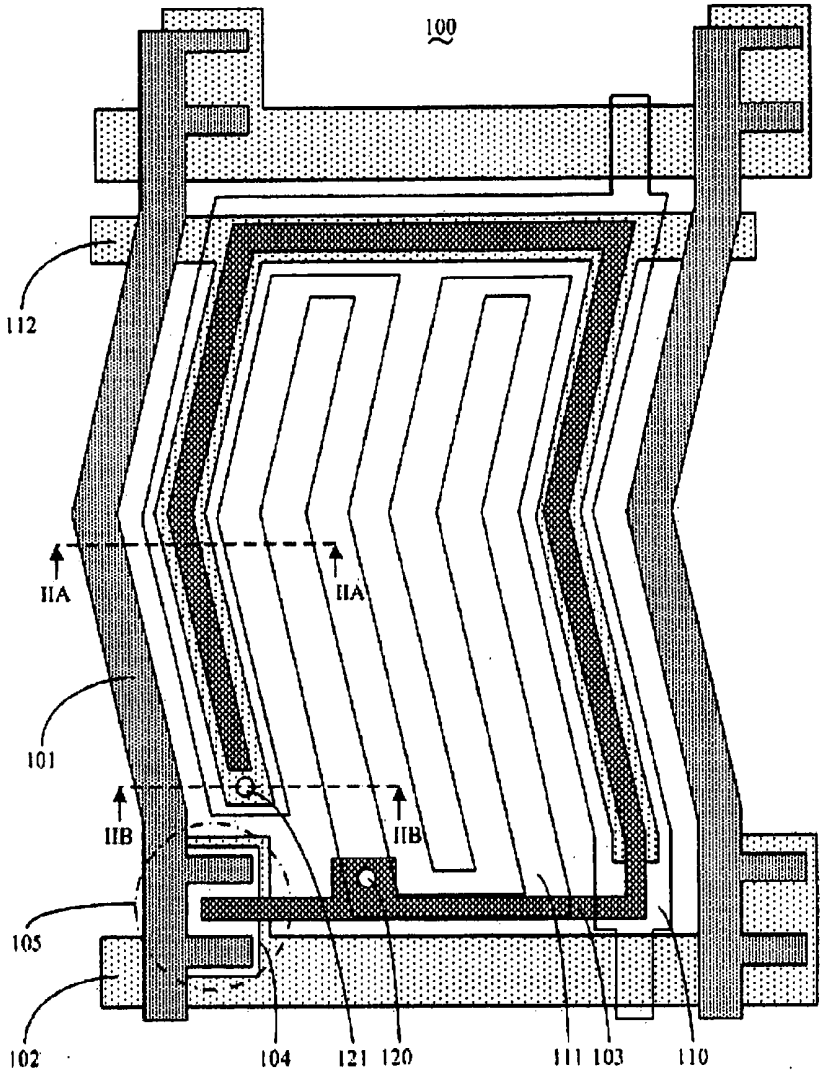
(57) **ABSTRACT**

An in-plane switching (IPS) liquid crystal display device (**100**) includes pixel units each having a storage capacitor. The storage capacitor is formed by a common electrode (**112**), a drain electrode (**103**), and a counter electrode (**110**). The common electrode is electrically coupled with the counter electrode. The counter electrode substantially covers the drain electrode, for shielding unexpected coupling effects on the drain electrode due to data signals on a data line (**101**) driving other pixels of the liquid crystal display device.



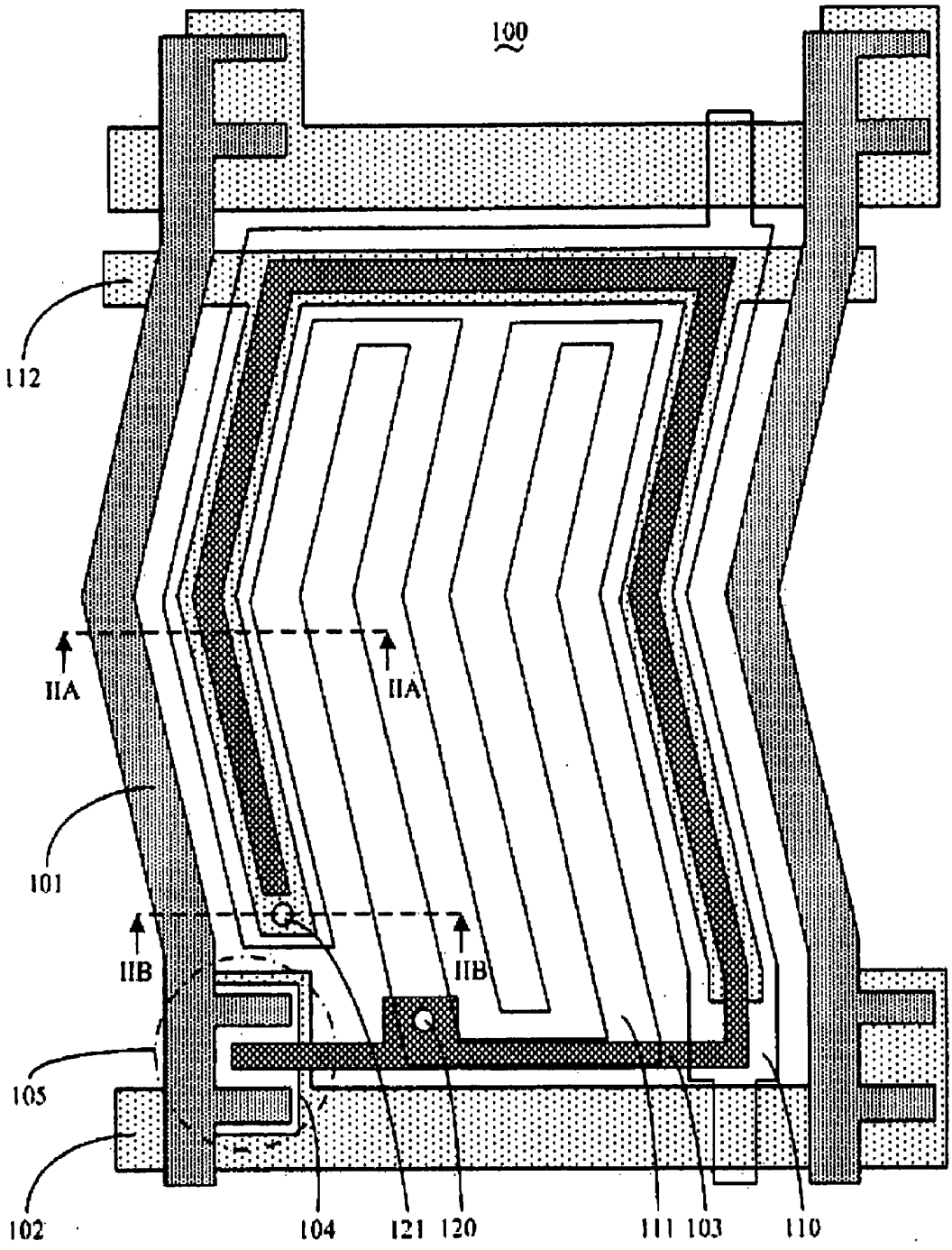


FIGURE 1

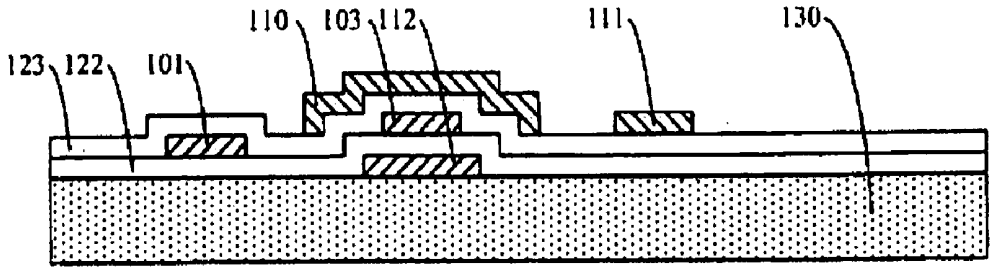


FIGURE 2A

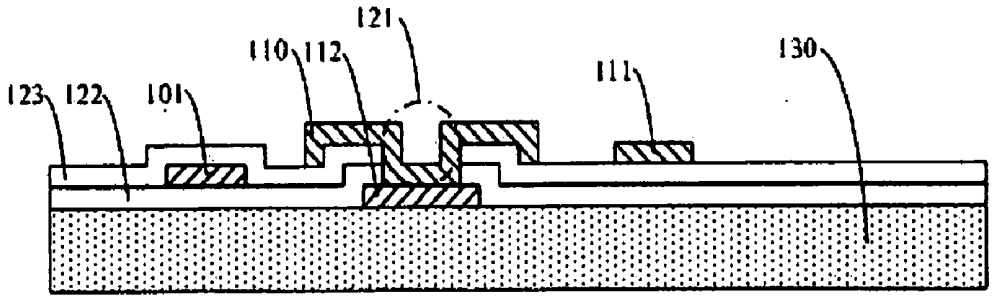


FIGURE 2B

IN-PLANE SWITCHING LIQUID CRYSTAL DISPLAY DEVICE HAVING STORAGE CAPACITORS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates generally to a liquid crystal display device utilizing in-plane switching mode, and more particularly to such a liquid crystal display device having a storage capacitor.

[0003] 2. Related Art

[0004] Liquid crystal displays have been burdened by limited viewing angles for many years. Many researchers in the art have invested huge amounts of time and effort in trying to find possible solutions for this shortcoming. One solution was developed by Masahito Ohe et al., and is disclosed in U.S. Pat. No. 5,600,464. This is the so-called liquid crystal display device with in-plane switching (IPS) mode.

[0005] In order for an IPS mode liquid crystal display device to have a higher aperture ratio, Seo et al. developed an "In-Plane Switching Mode Liquid Crystal Display Device Having a High Aperture Ratio," which is disclosed in U.S. Pat. No. 6,628,362 (the '362 patent). In particular, a storage capacitor having a reduced effective area for enlarging the aperture ratio is disclosed. Referring to **FIG. 2B** of the '362 patent, a circular mark **125** represents a group of electrodes, which are overlapped to form two storage capacitors. As shown, one storage capacitor is formed by a common electrode **109** and a data electrode **108**, while the other storage capacitor is formed by the data electrode **108** and a gate electrode **101**. However, due to the existence of unexpected coupling effects, such as a capacitive coupling effect, in a liquid crystal display device, especially in an IPS mode liquid crystal display device, the voltage of a pixel electrode is affected by data signals carried on a data signal line driving other pixels. This significantly reduces the quality of images displayed on the liquid crystal display device.

SUMMARY OF THE INVENTION

[0006] An objective of the present invention is to provide an IPS mode liquid crystal display device having a storage capacitor capable of shielding unexpected coupling effects.

[0007] In order to achieve the above objective, the present invention provides an in-plane switching liquid crystal display device that comprises a storage capacitor capable of shielding unexpected coupling effects such as a capacitive coupling effect. The liquid crystal display device comprises a substrate, a plurality of scanning lines, a plurality of data lines, and a plurality of thin film transistors. The scanning lines and the data lines are arranged on the substrate and cross each other thereby defining a plurality of pixel units. A first dielectric layer is interposed between the scanning lines and the data lines for mutual insulation. The thin film transistors are formed at crossing points of the scanning lines and the data lines. Each thin film transistor comprises a gate electrically coupling to the scanning line, a source electrically coupling to the data line, and a drain.

[0008] Each pixel unit comprises a common electrode, a drain electrode, and a counter electrode. The common electrode is formed on the substrate. The drain electrode is electrically coupled to the drain of the thin film transistor. A portion of the drain electrode is formed above a corresponding portion of the common electrode, with the first dielectric layer interposed between the drain electrode and the common electrode. A portion of the counter electrode is formed above a corresponding portion of the drain electrode, with a second dielectric layer interposed between the drain electrode and the counter electrode. The counter electrode is electrically coupled to the common electrode through a via. The common electrode, the counter electrode and the drain electrode cooperatively form a storage capacitor. In addition, the drain electrode comprises a pixel electrode electrically coupled to the drain electrode through a via. The pixel electrode is arranged substantially parallel to the counter electrode, for generating electric fields substantially parallel to the substrate. The counter electrode substantially covers the drain electrode, for shielding any unexpected coupling effects between the drain electrode and the data lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention is better understood by referring to the detailed description of the preferred embodiment taken in conjunction with the drawings, wherein:

[0010] **FIG. 1** is a top elevation illustrating a pixel unit of an IPS liquid crystal display device in accordance with one embodiment of the present invention, the pixel unit comprising a storage capacitor;

[0011] **FIG. 2A** is a cross-sectional view taken along line IIA-IIA of **FIG. 1**; and

[0012] **FIG. 2B** is a cross-sectional view taken along line IIB-IIB of **FIG. 1**.

DETAILED DESCRIPTION OF THE INVENTION

[0013] The present invention is hereinafter described in detail with reference to the accompanying drawings. **FIG. 1** illustrates a pixel unit of an in-plane switching (IPS) liquid crystal display device, while **FIG. 2A** and **FIG. 2B** illustrate cross-sectional views taken along line IIA-IIA and line IIB-IIB of **FIG. 1** respectively.

[0014] Referring to **FIG. 1**, a pixel unit of an IPS mode liquid crystal display device **100** is illustrated. Referring also to **FIGS. 2A and 2B**, the liquid crystal display device **100** comprises a plurality of data lines **101**, a plurality of scanning lines **102**, a first dielectric layer **122**, a second dielectric layer **123**, and a plurality of thin film transistors **105**. The data lines **101** and the scanning lines **102** are arranged on a substrate **130**, as shown in **FIGS. 2A and 2B**, and cross each other thereby defining a plurality of pixel units. The first dielectric layer **122** is interposed between the scanning lines **102** and the data lines **101** for mutual insulation. The thin film transistors **105** are formed at the crossing points of the scanning lines **102** and the data lines **101**. Each of the thin film transistors **105** comprises a gate electrically coupling to the scanning line **102**, a source electrically coupling to the data line **101**, a drain and a channel interposing between the gate, and the drain and the source. In this particular embodiment, an amorphous-silicon (a-Si) film **104** is employed as the channel of the thin-film transistor **105**. Other films, such as a poly-silicon film, may alternatively be employed as the channel of the thin-film transistor **105**.

[0015] Each pixel unit of the liquid crystal display device **100** comprises a common electrode **112**, a drain electrode **103**, and a counter electrode **110**. The common electrode **112** is formed on the substrate **130**. The first dielectric layer **122** is formed on the common electrode **112** and the substrate **130**. The drain electrode **103** is formed on the first dielectric layer **122**, such that a portion of the drain electrode **103** is formed substantially above a corresponding portion of the common electrode **112**. The drain electrode **103** is electrically coupled to the drain of the thin film transistor **105**. The second dielectric layer **123** is formed on the drain electrode **103**. The counter electrode **110** is formed on the second dielectric layer **123**, such that a portion of the counter electrode **110** is formed substantially above a corresponding portion of the drain electrode **103**. The counter electrode **110** is electrically coupled to the common electrode **112** through a via **121**. The common electrode **112**, the counter electrode **110** and the drain electrode **103** cooperatively form a storage capacitor. In addition, the drain electrode **103** comprises a pixel electrode **111**. In this particular embodiment, the pixel electrode **111** is electrically coupled to the drain electrode **103** through a via **120**. In other embodiments, the pixel electrode **111** may be one part of the drain electrode **103**. The pixel electrode **111** is arranged substantially parallel to the counter electrode **110**, for generating electric fields substantially parallel to the substrate **130**. As shown in **FIG. 1**, the counter electrode **110** in this particular embodiment is generally fork-shaped with three prongs, while the pixel electrode **111** is generally fork-shaped with two prongs corresponding to the prongs of the counter electrode **110**. However, it will be appreciated that the counter electrode **110** and the corresponding pixel electrode **111** may be formed to have other suitable shapes.

[0016] Referring to **FIG. 2A**, the counter electrode **110** is formed to have a substantially larger area than that of the drain electrode **103**, so that the counter electrode **110** substantially covers the drain electrode **103**. With this configuration, unexpected coupling effects, such as a capacitive coupling effect, on the drain electrode **103** due to data signals being carried on the data line **101** for driving other pixels can be shielded. Referring also to **FIG. 2B**, the counter electrode **110** is electrically coupled to the common electrode **112** through a via **121**.

[0017] While the present invention has been described in detail with reference to the illustrated embodiment, it will be appreciated that no limitation to the present invention is intended by the above descriptions. Various equivalents of the preferred embodiment described above will be apparent to those with ordinary skill in the art, and it is therefore contemplated that the present invention be defined according to the following claims in their broadest meaning. Consequently, any modifications or alterations of the preferred embodiments are considered within the scope of the present invention.

What is claimed is:

1. A storage capacitor for an in-plane switching liquid crystal display device, comprising:

a common electrode;

a first dielectric layer covering said common electrode;

a drain electrode disposed on said first dielectric layer above said common electrode, said drain electrode being electrically coupled to a pixel electrode;

a second dielectric layer covering said drain electrode and said first dielectric layer; and

a counter electrode disposed on said second dielectric layer above said drain electrode, said counter electrode being arranged substantially parallel to said pixel electrode for generating in-plane switching mode electric fields, and being electrically coupling to said common electrode.

2. The storage capacitor as recited in claim 1, wherein said counter electrode and said common electrode are electrically coupled through a via.

3. The storage capacitor as recited in claim 1, wherein said counter electrode substantially covers said drain electrode, for shielding unexpected coupling between said drain electrode and a data line.

4. An in-plane switching liquid crystal display device comprising:

a substrate;

a plurality of scanning lines and a plurality of data lines arranged on said substrate and crossing each other thereby defining a plurality of pixel units, wherein a first dielectric layer is interposed between the scanning lines and the data lines for mutual insulation; and

a plurality of thin film transistors formed at crossing points of the scanning lines and the data lines, each of the thin film transistors comprising a gate electrically coupling to the scanning line, a source electrically coupling to the data line, and a drain;

wherein each of the pixel units comprises:

a common electrode;

a drain electrode electrically coupled to the drain of the thin film transistor, a portion of said drain electrode being arranged above a corresponding portion of said common electrode, wherein the first dielectric layer is interposed between said drain electrode and said common electrode; and

a counter electrode electrically coupling to said common electrode, a portion of said counter electrode being arranged above a corresponding portion of said drain electrode, wherein a second dielectric layer is interposed between said drain electrode and said counter electrode.

5. The liquid crystal display device as recited in claim 4, wherein said counter electrode substantially covers said drain electrode for shielding unexpected coupling between said drain electrode and the data lines.

6. The liquid crystal display device as recited in claim 4, wherein said drain electrode further comprising a pixel electrode.

7. The liquid crystal display device as recited in claim 6, wherein said pixel electrode is arranged substantially parallel to said counter electrode for generating electric fields substantially parallel to said substrate.

8. The liquid crystal display device as recited in claim 4, wherein said common electrode and said counter electrode are electrically coupled through a via.

9. The liquid crystal display device as recited in claim 8, wherein said common electrode, said counter electrode and said drain electrode cooperatively form a storage capacitor.

10. An in-plane switching liquid crystal display device including:

pixel units each having a storage capacitor, said storage capacitor formed by a common electrode, a drain electrode, and a counter electrode wherein the common electrode is electrically coupled with the counter electrode and the counter electrode substantially covers the drain electrode for shielding unexpected coupling effects on the drain electrode due to data signals on a data line driving other pixels of the liquid crystal display device.

* * * * *

专利名称(译)	具有存储电容器的面内切换液晶显示装置		
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外部链接	Espacenet USPTO		

摘要(译)

面内切换（IPS）液晶显示装置（100）包括每个都具有存储电容器的像素单元。存储电容器由公共电极（112），漏电极（103）和对电极（110）形成。公共电极与对电极电耦合。对电极基本上覆盖漏电极，用于屏蔽由于驱动液晶显示装置的其他像素的数据线（101）上的数据信号而在漏电极上的意外耦合效应。