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(54) LIQUID CRYSTAL DISPLAY DEVICE

(76) Inventors: **Nagatoshi Kurahashi**, Mobara (JP); **Yoshiaki Nakayoshi**, Ooamishirasato (JP); **Kazuhiko Yanagawa**, Mobara (JP)

Correspondence Address:
ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889 (US)

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(57) **ABSTRACT**

A liquid crystal display device with pixel electrode and counter electrode on the same substrate, and at least one of the counter electrode overlap with video signal line and gate signal line having dielectric film therebetween, said dielectric film is comprised of a sequential lamination body of at least a protective film made of an inorganic material and a protective film made of an organic material, an opening is formed at part of said protective film made of the inorganic material underlying said counter electrode and the opening being filled with the protective film made of the organic material.

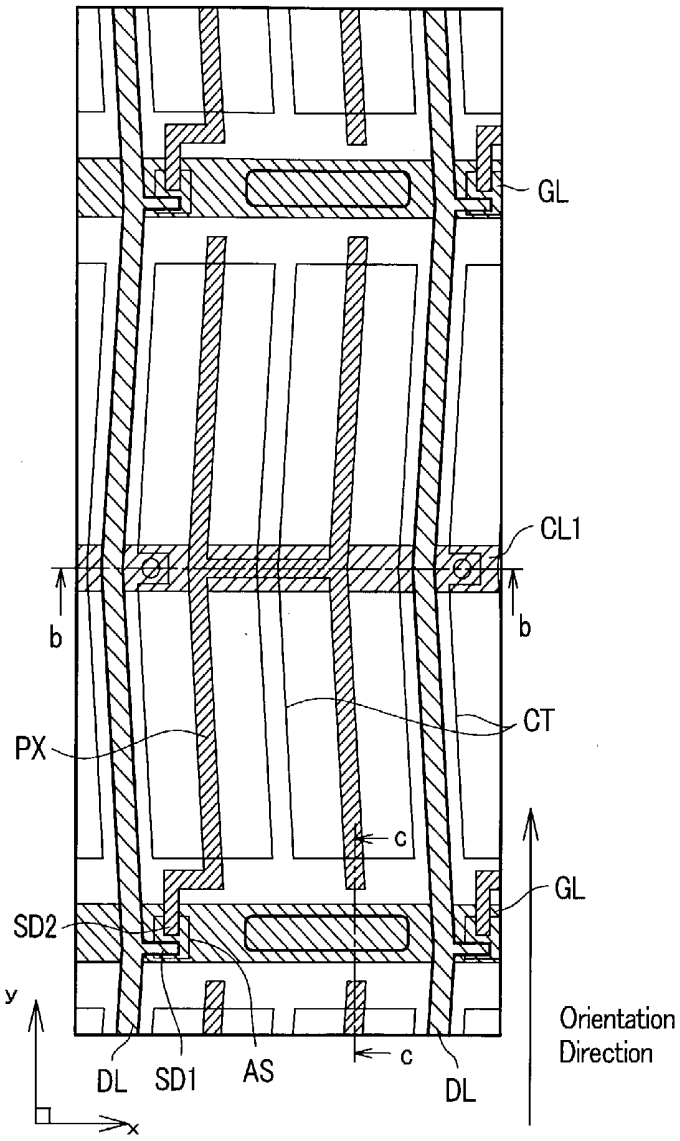


FIG. 1A

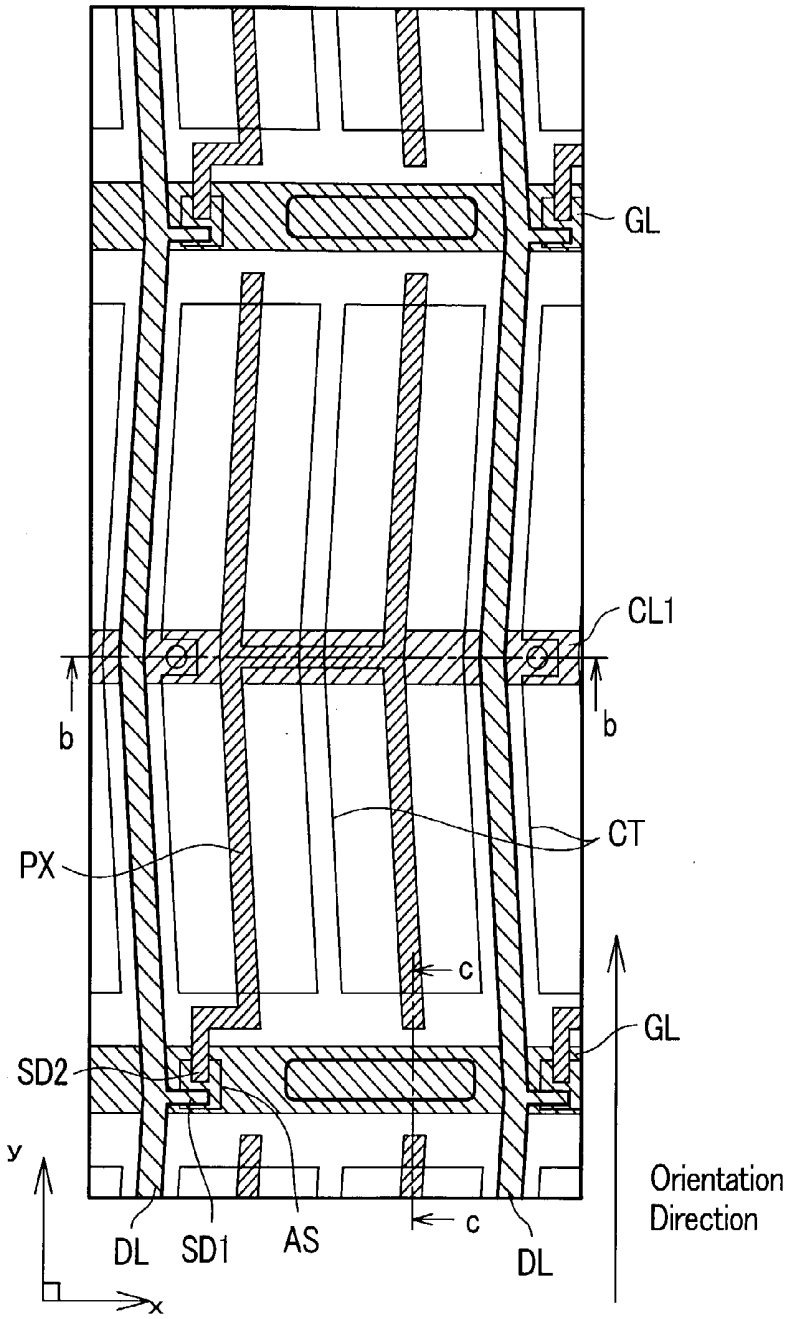


FIG. 1B

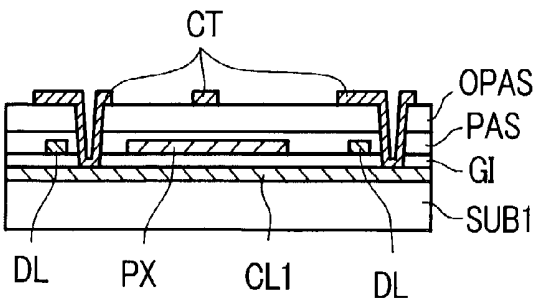


FIG. 1C

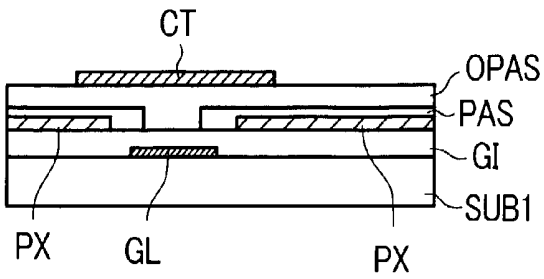


FIG. 2A

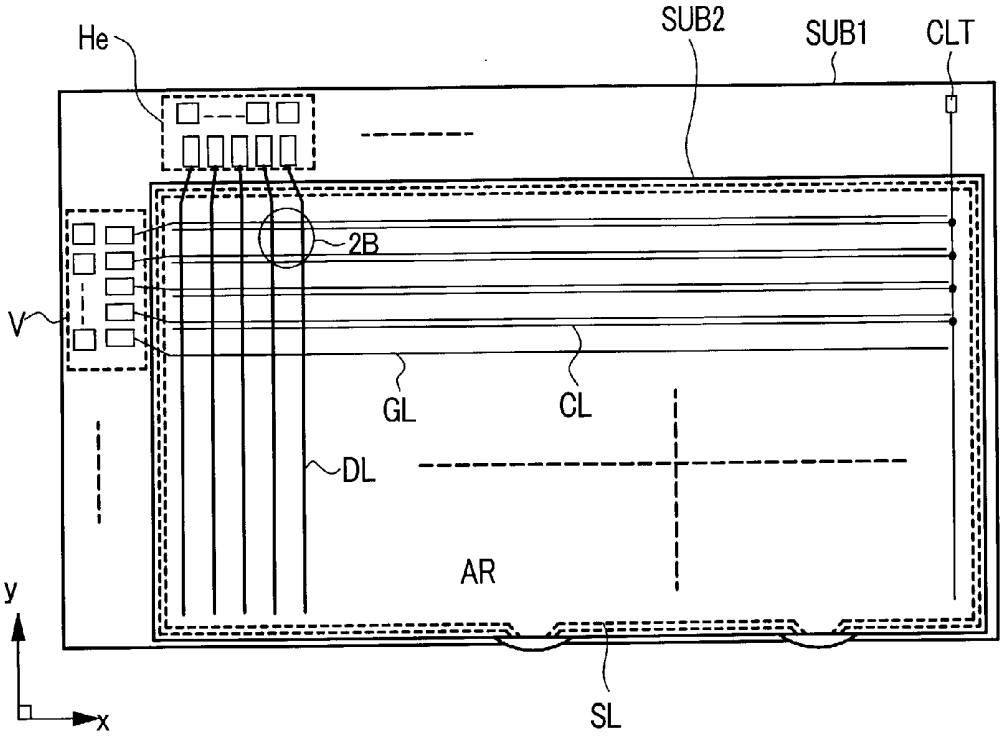


FIG. 2B

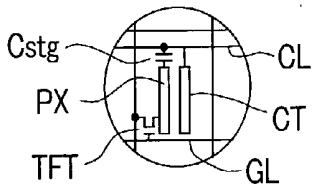


FIG. 3

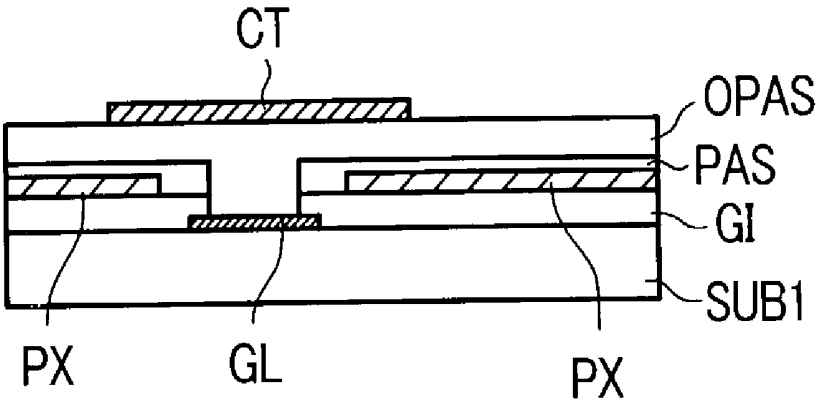


FIG. 4

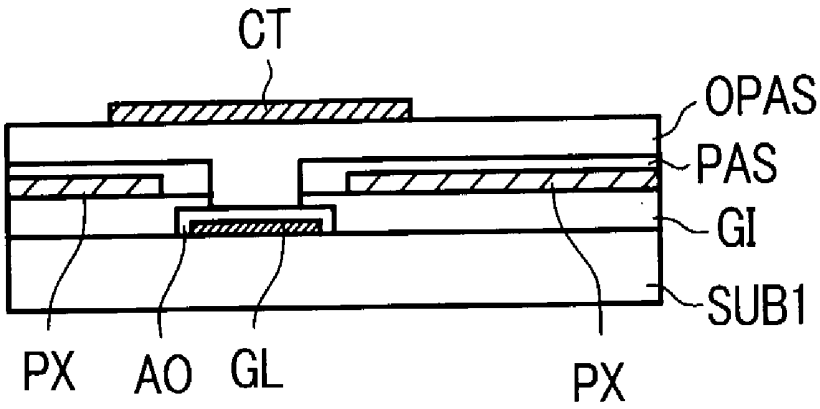


FIG. 5A

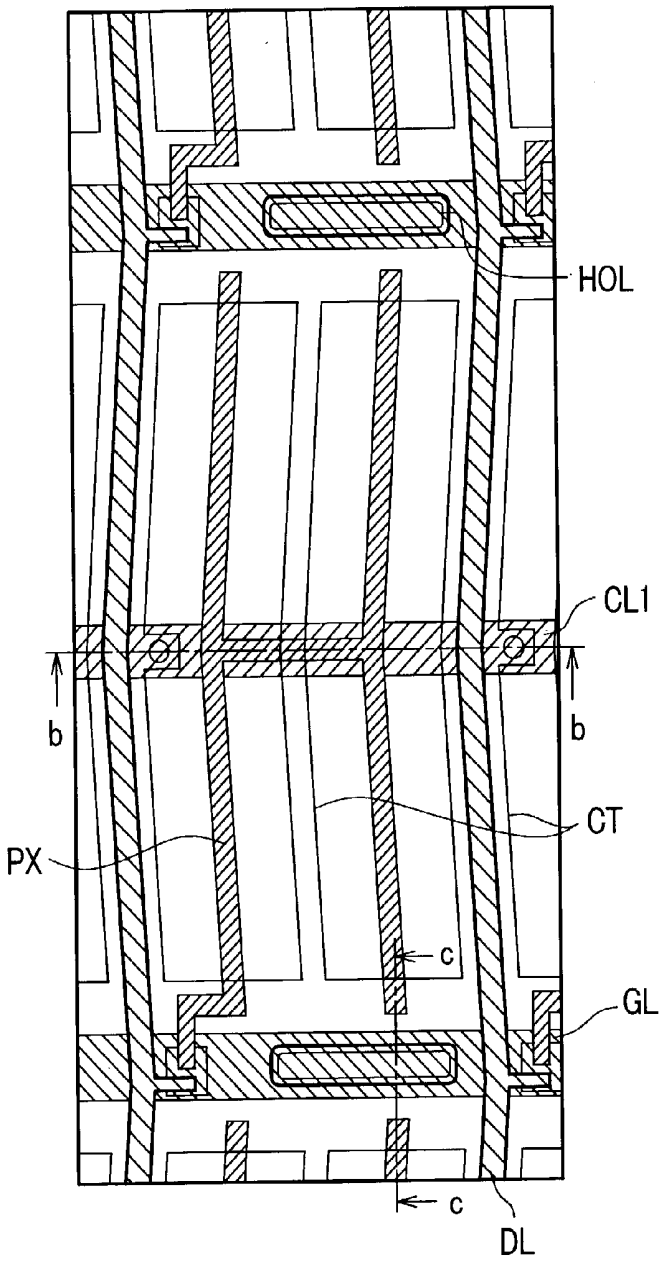


FIG. 5B

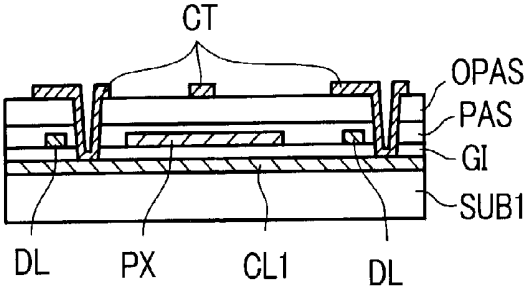


FIG. 5C

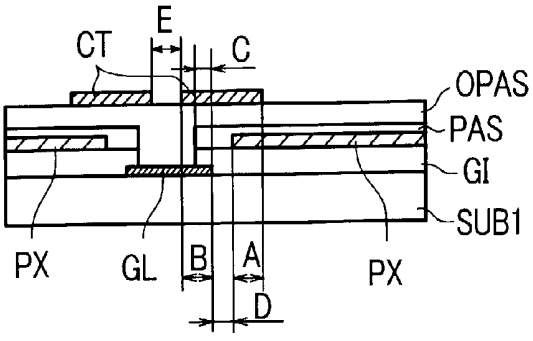


FIG. 6A

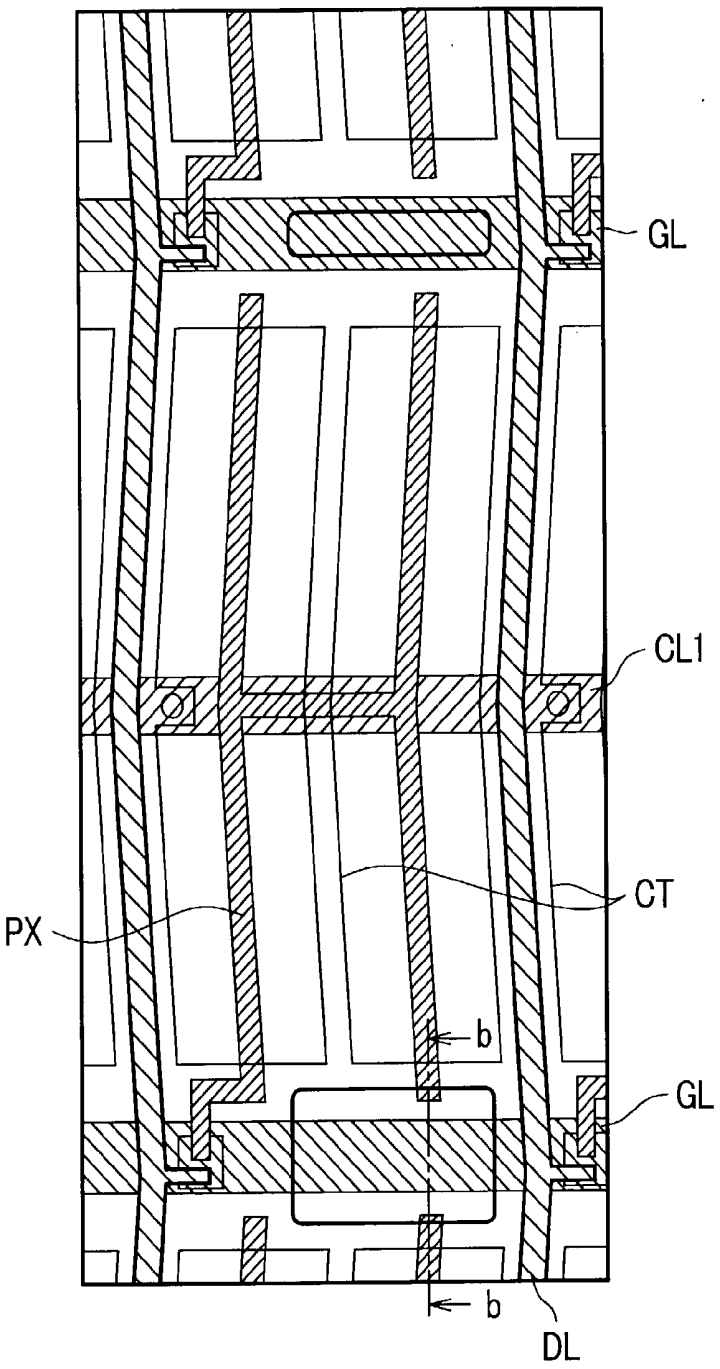


FIG. 6B

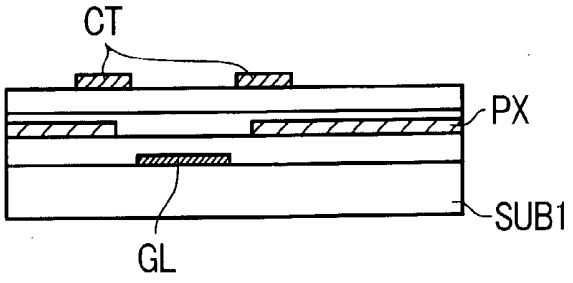


FIG. 7

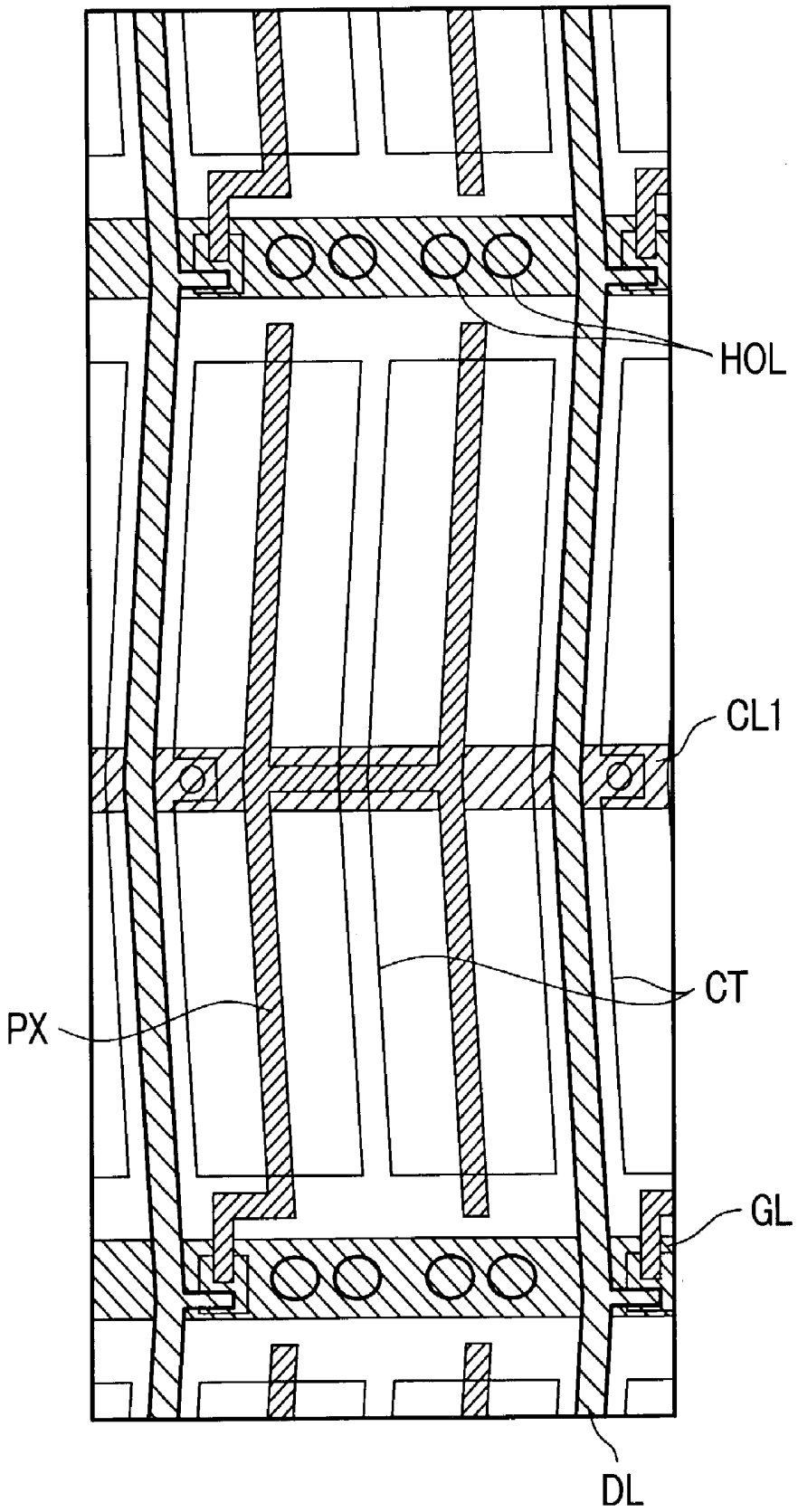


FIG. 8

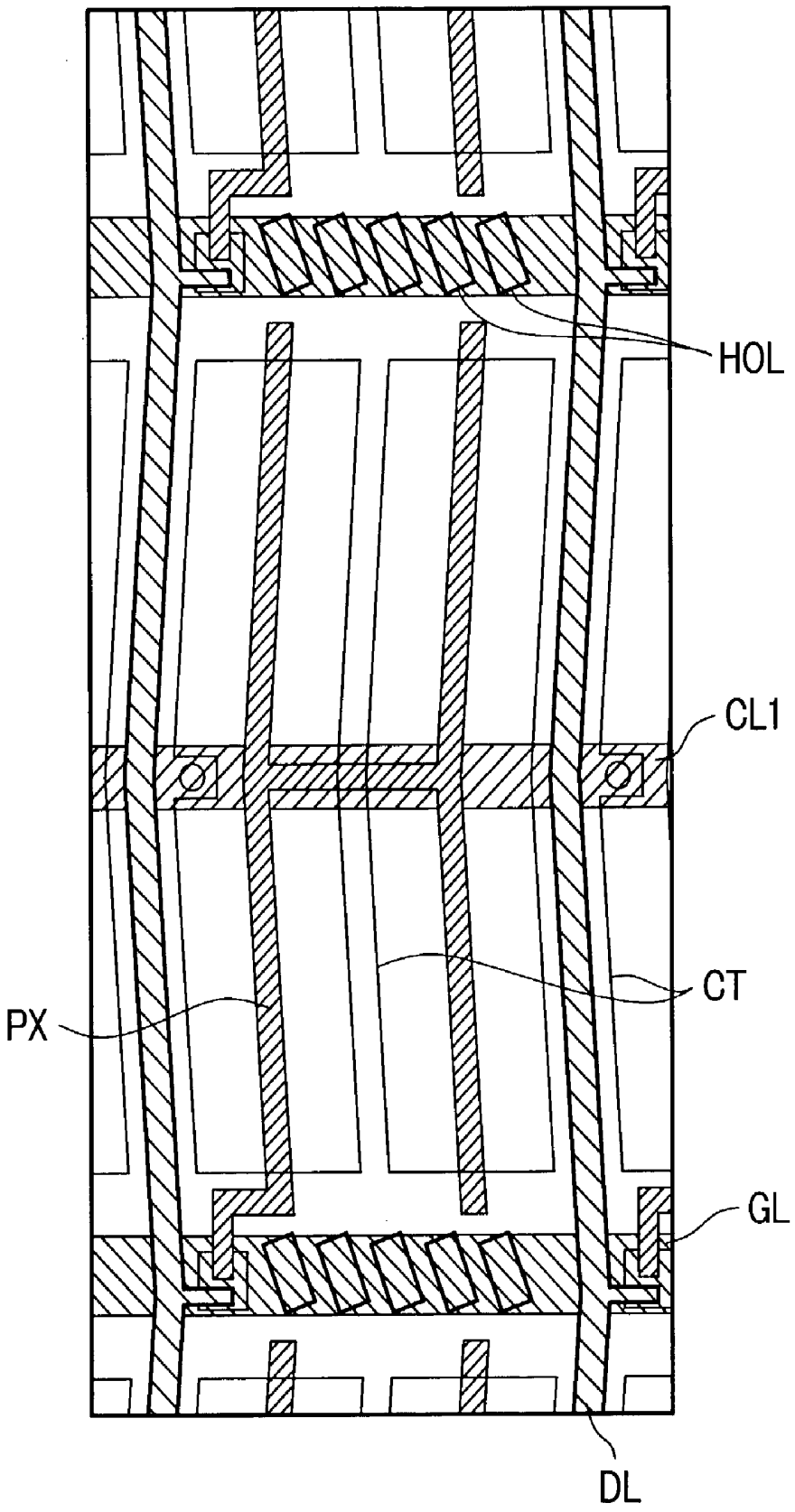


FIG. 9A

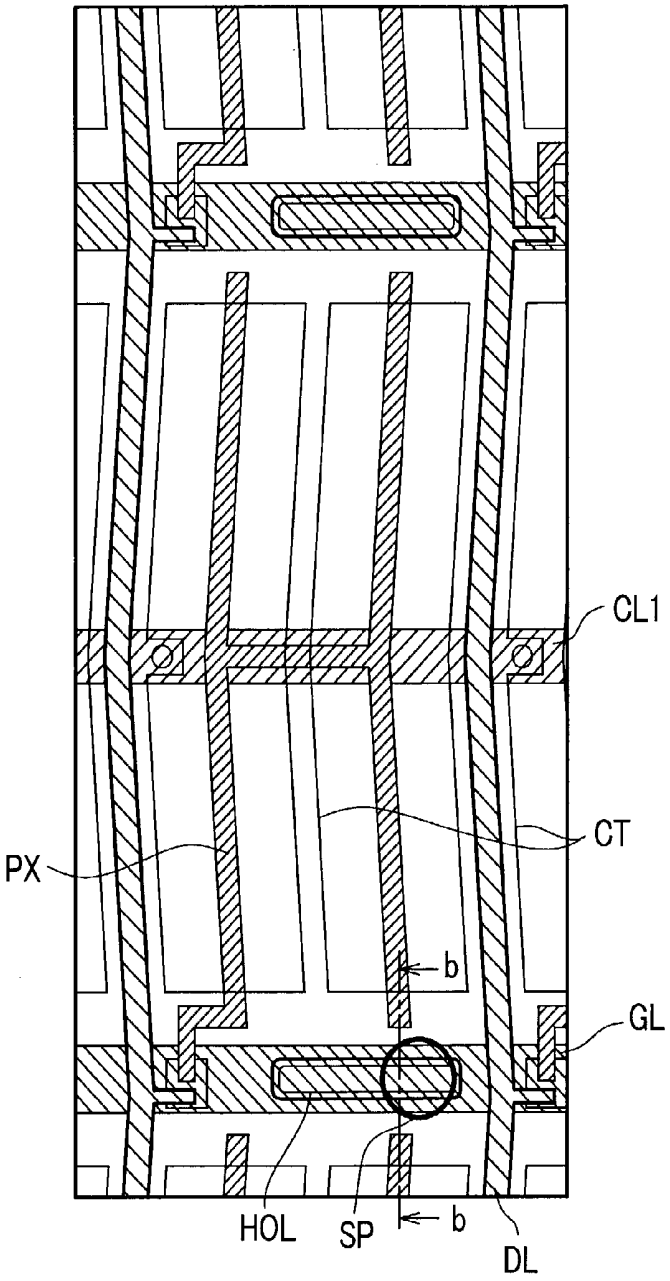


FIG. 9B

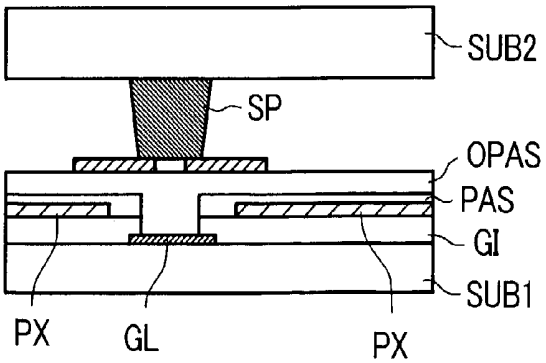


FIG. 10

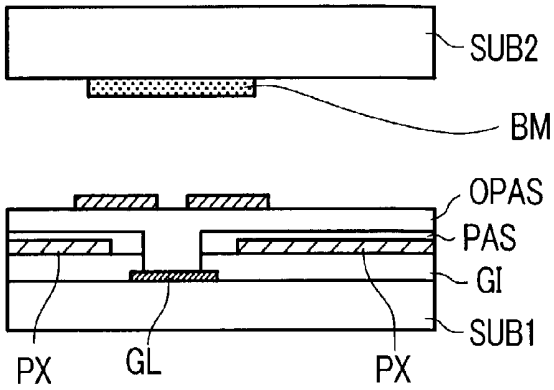


FIG. 11

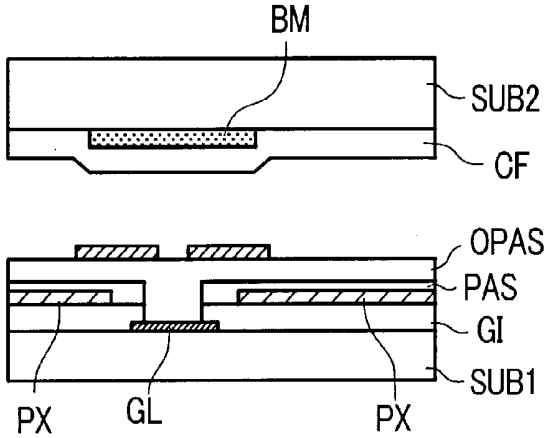


FIG. 13

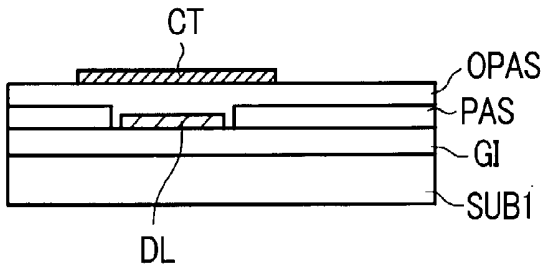


FIG. 14

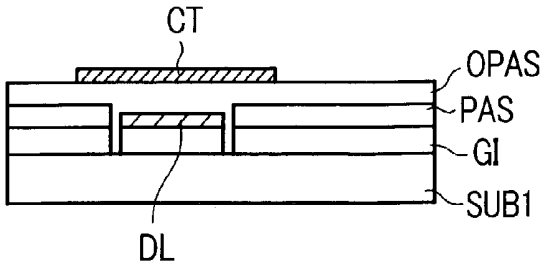


FIG. 12A

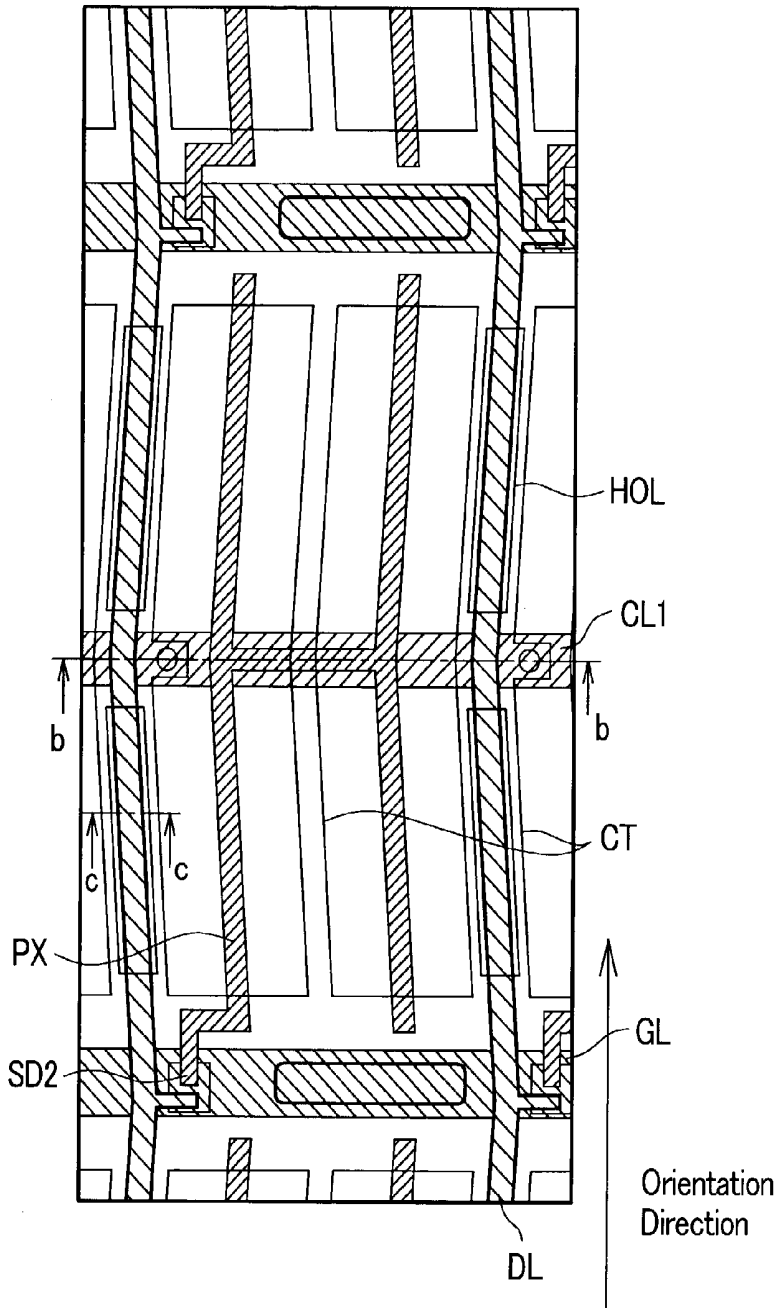


FIG. 12B

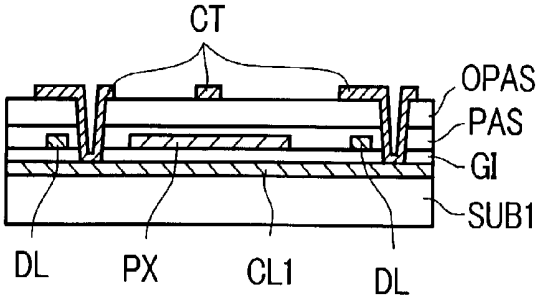


FIG. 12C

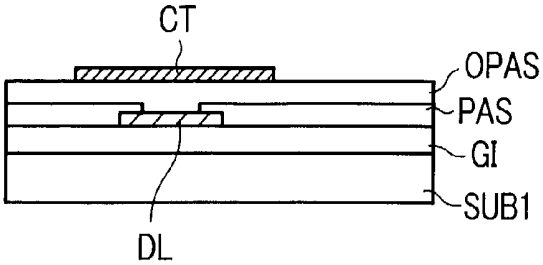


FIG. 15A

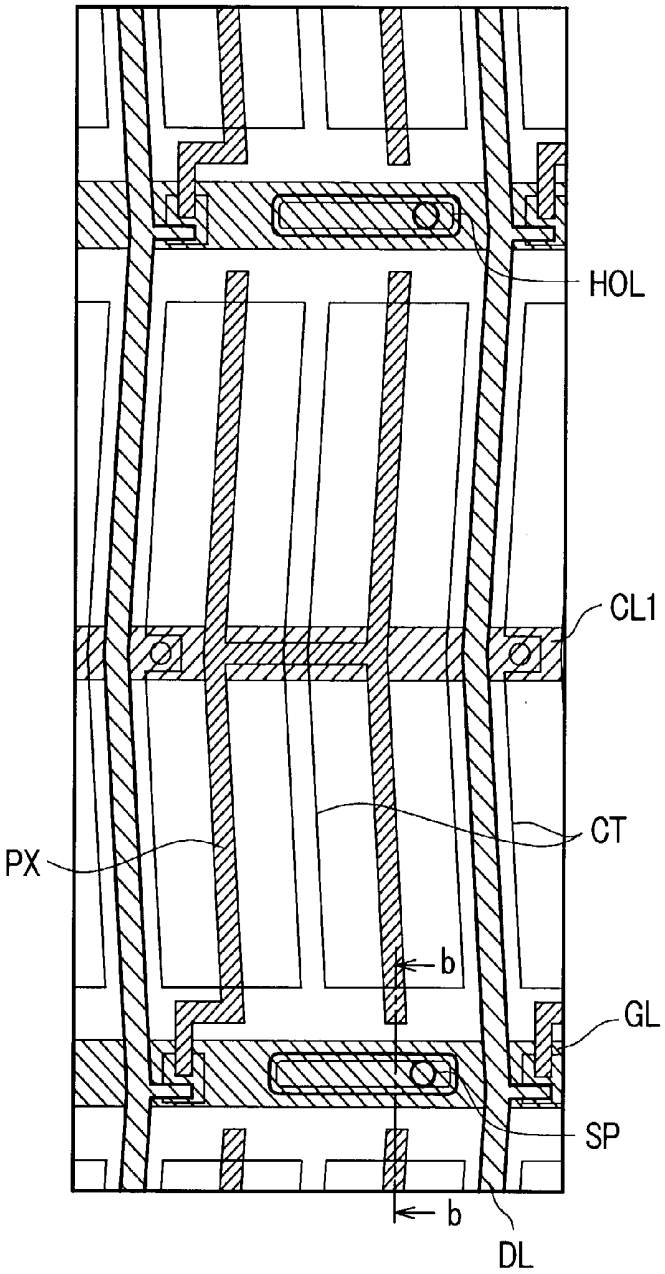


FIG. 15B

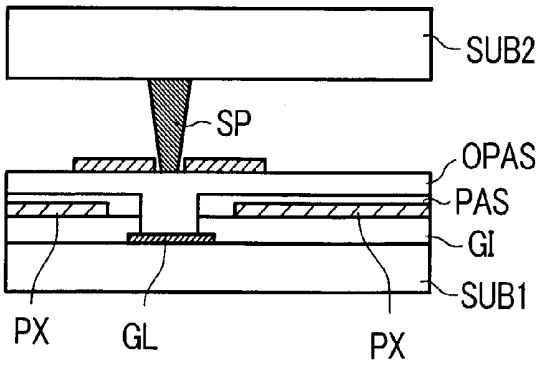


FIG. 16A

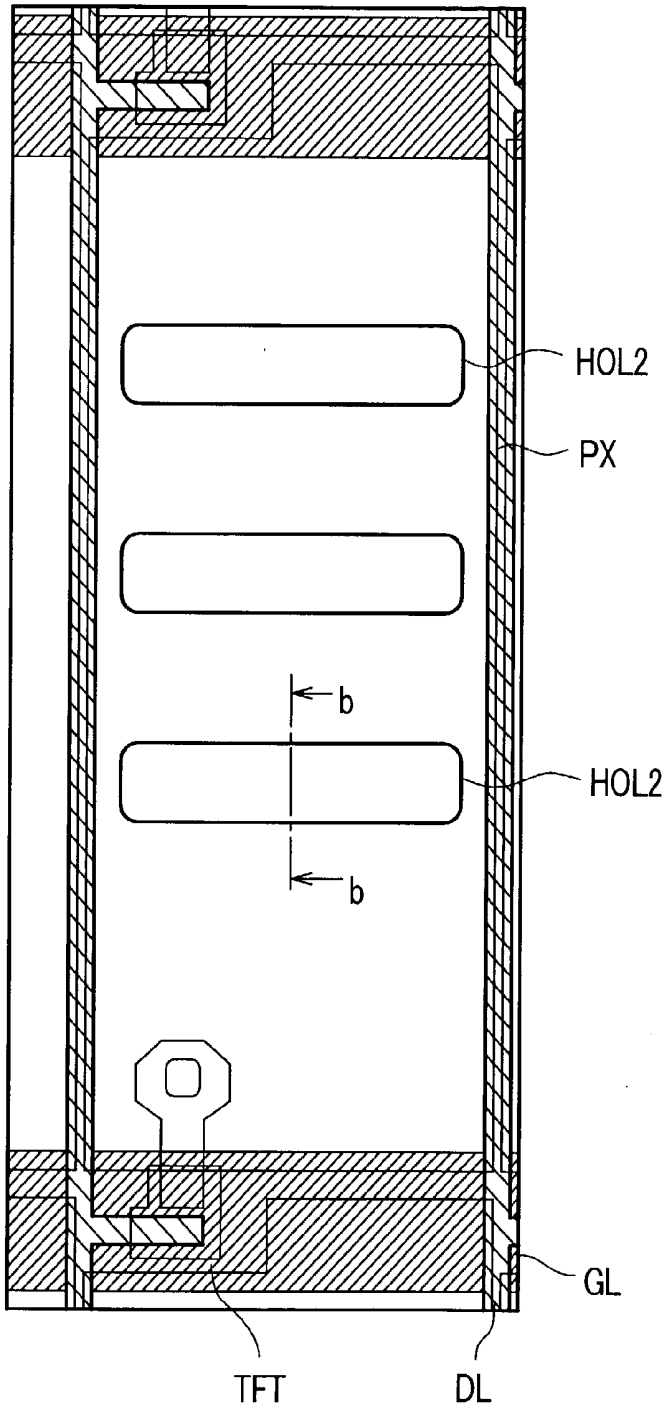
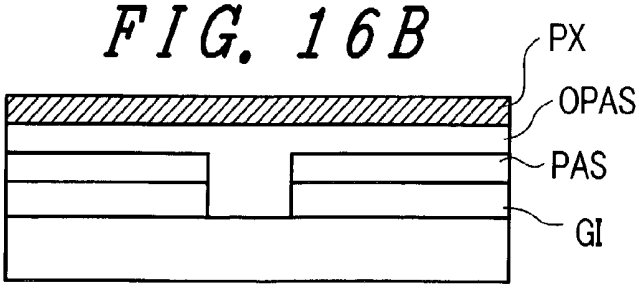


FIG. 16B



LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates generally to liquid crystal display devices and, more particularly, to a liquid crystal display device of the type employing the so-called lateral electric field scheme.

[0003] 2. Description of the Related Art

[0004] A liquid crystal display device of the so-called lateral electric field scheme type is arranged to comprise a picture element or "pixel" electrode and an opposite or "counter" electrode which permits creation of an electric field between this pixel electrode and itself in a pixel region on the liquid crystal-side surface of one substrate of respective substrates as disposed to oppose each other with a layer of liquid crystal material interposed therebetween, and liquid crystals are driven by certain components of the electric field which extend in almost parallel with the substrate.

[0005] And, the one that applies such arrangement to an active matrix type one is first designed to use as the pixel electrodes respective regions which are surrounded by a plurality of parallel-provided gate signal lines on or over the liquid crystal-side surface of the above-noted one substrate and a plurality of drain signal lines that are provided in parallel in such a way as to cross or intersect these respective gate signal lines.

[0006] And there are provided within each of these pixel regions a thin-film transistor which is made operative by a scanning signal from a gate signal line, the above-noted pixel electrode to which an image or video signal is supplied through this thin-film transistor from a drain signal line, and the counter electrode to which a signal for use as a reference with respect to the image signal is supplied.

[0007] The pixel electrode and the counter electrode are each formed as a band-like or strip-shaped pattern which extends in one direction, wherein each of these electrodes is ordinarily arranged to be formed of two or more components which are alternately disposed.

[0008] In this arrangement, the one is also known which is arranged so that the counter electrode is formed on or above the upper surface of a dielectric film that is formed to also cover its associated drain signal line while letting it be substantially coincide in center axis with the drain signal line and have a greater width than that of the drain signal line and also be formed along the drain signal line.

[0009] This is for the purpose of causing an electric flux line from the drain signal line to easily terminate at its overlying counter electrode to thereby prevent termination at the pixel electrode. If otherwise the electric flux line terminates at the pixel electrode, then this would result in unwanted production of noises.

[0010] And, counter electrode stated above is formed at the upper surface of a dielectric film that is formed to cover the gate signal line also in such a manner that the counter electrode is made integral with the counter voltage signal line, wherein a reference signal is to be supplied to each counter electrode through this counter voltage signal line.

SUMMARY OF THE INVENTION

[0011] However, it has been pointed out that the liquid crystal display device arranged in the way described above suffers from generation of a parasitic capacitance between the gate signal line and counter voltage signal line, which parasitic capacitance results in occurrence of waveform delays of a scan signal which is supplied to the gate signal line.

[0012] And, in recent years that the gate signal line tends to become larger in length with an increase in size of liquid crystal display devices, it has become an important goal to reduce the waveform delays of the scan signal.

[0013] The present invention has been made in view of the technical background and an advantage of the present patent application is to provide a liquid crystal display device which reduces waveform delays of scan signals being supplied to gate signal lines.

[0014] Another advantage of this invention is to provide a liquid crystal display device which suppress waveform delays of image signals as supplied to drain signal lines.

[0015] A brief explanation of the summary of representative ones of the inventive concepts as set forth in the description is as follows.

[0016] (1) A liquid crystal display device is such that a first substrate and a second substrate with a liquid crystal layer therebetween, a plurality of gate signal lines formed on the first substrate and a plurality of drain signal lines formed on the first substrate and intersect with the plurality of gate signal lines, a plurality of switching element operable by a scan signal from a gate signal line, at least a pixel electrode to which an image signal is supplied through the switching element from a drain signal line in each pixels, and at least a counter electrode for creating an electric field with the pixel electrode in each pixels, at least one of said counter electrode is arranged along a running direction of said drain signal line and overlap with the drain signal line with dielectric film therebetween, at least one of said counter electrode or counter voltage signal line integrated with the counter electrode is arranged along a running direction of said gate signal line and overlap with said gate signal line with dielectric film therebetween, and said dielectric film is comprised of a sequential lamination body of at least a protective film made of an inorganic material and a protective film made of an organic material, wherein an opening is formed at part of said protective film made of the inorganic material underlying at least either one of said counter voltage signal line and said counter electrode, the opening being filled with the protective film made of the organic material.

[0017] (2) A liquid crystal display device is such that a first substrate and a second substrate with a liquid crystal layer therebetween, a plurality of gate signal lines formed on the first substrate and a plurality of drain signal lines formed on the first substrate and intersect with the plurality of gate signal lines, a plurality of switching element operable by a scan signal from a gate signal line, at least a pixel electrode to which an image signal is supplied through the switching element from a drain signal line in each pixels, and at least a counter electrode for creating an electric field with the pixel electrode in each pixels, at least one of said counter electrode is arranged along a running direction of said drain

signal line and overlap with the drain signal line with dielectric film therebetween, at least one of said counter electrode or counter voltage signal line integrated with the counter electrode is arranged along a running direction of said gate signal line and overlap with said gate signal line with dielectric film therebetween, and said dielectric film is constituted from a sequential lamination body of a first protective film and a second protective film overlapping said first protective film and being lower in dielectric constant than said first protective film, wherein an opening is formed at part of said first protective film underlying at least either one of said counter voltage signal and said counter electrode, said opening being filled with said second protective film.

[0018] (3). A liquid crystal display device is such that a first substrate and second substrate with a liquid crystal layer therebetween, a plurality of gate signal lines formed on the first substrate and a plurality of drain signal lines formed on the first substrate and intersect with the plurality of gate signal lines, a plurality of switching element operable by a scan signal from a gate signal line, at least a pixel electrode to which an image signal is supplied through the switching element from a drain signal line in each pixels, and at least a counter electrode for creating an electric field with the pixel electrode in each pixels, at least one of said counter electrode is arranged along a running direction of said drain signal line and overlap with the drain signal line with dielectric film therebetween, at least one of said counter electrode or counter voltage signal line integrated with the counter electrode is arranged along a running direction of said gate signal line and overlap with said gate signal line with dielectric film therebetween, at least an opening is made in one of said counter voltage signal line and the counter electrode, and said an opening is arranged to partially overlap with the gate signal line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] **FIGS. 1A** to **1**C are drawings showing an arrangement of one embodiment of a pixel of a liquid crystal display device in accordance with the present invention.

[0020] **FIG. 2** is a drawing showing a configuration of one embodiment of the liquid crystal display device in accordance with this invention.

[0021] **FIG. 3** is a cross-sectional diagram showing another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0022] **FIG. 4** is a sectional drawing showing another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0023] FIGS. **5**A-**5**C are drawings showing a configuration of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0024] FIGS. **6**A-**6**C are drawings showing a configuration of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0025] **FIG. 7** is a drawing showing a plan view of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0026] **FIG. 8** is a drawing showing a plan view showing another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0027] **FIGS. 9A and 9B** are drawings showing a configuration of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0028] **FIG. 10** is a sectional diagram showing still another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0029] **FIG. 11** is a sectional diagram showing yet another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0030] FIGS. **12**A-**12**C are drawings showing a configuration of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0031] **FIG. 13** is a sectional drawing showing another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0032] **FIG. 14** is a sectional diagram showing another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0033] FIGS. **15**A-**15**B are drawings showing a configuration of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

[0034] FIGS. **16**A-**16**B are diagrams showing a configuration of another embodiment of the pixel of the liquid crystal display device in accordance with the invention.

DETAILED DESCRIPTION

[0035] Several preferred embodiments of the liquid crystal display device in accordance with the present invention will be explained with reference to the accompanying drawings below.

[0036] Embodiment 1.

[0037] <<Overall Arrangement>>

[0038] **FIG. 2** is an arrangement diagram showing one embodiment of the liquid crystal display device in accordance with this invention. Although **FIG. 2** is an equivalent circuit diagram, this diagram illustrates it in a way corresponding to the real geometrical layout thereof.

[0039] In **FIG. 2, a** pair of transparent substrates SUB**1**, SUB**2** are provided, which are disposed to spatially oppose each other with a layer of liquid crystal material being interposed therebetween. The liquid crystal is sealed therein by a sealing material SL which functions also to achieve fixation of one transparent substrate SUB**1** with respect to the other transparent substrate SUB**2**.

[0040] Gate signal line GL which extend in the "x" direction thereof and are provided in parallel to a "y" direction and drain signal line DL which extend in the y direction and are parallel-provided in the x direction are formed on or above the liquid crystal-side surface of the above-noted one transparent substrate SUB**1**.

[0041] Regions surrounded by respective gate signal lines GL and respective drain signal lines DL constitute pixel regions; simultaneously, a matrix-like ensemble or assembly of these respective pixel regions makes up a liquid crystal display unit AR.

[0042] In addition, in respective ones of those pixel regions that are parallel-provided in the "x" direction, a

common counter voltage signal line CL is formed which is designed to run within each of such pixel regions. This counter voltage signal line CL is the one that becomes a signal line for supplying a voltage for use as a reference with respect to image or video signals to a counter electrode CT of each pixel region as will be described later.

[0043] In each pixel region, there are formed a thin-film transistor TFT which is made operative by a scanning signal incoming from a gate signal line GL on its one side and a pixel electrode PX to which an image signal is supplied through this thin-film transistor TFT from a one-side drain signal line DL.

[0044] This pixel electrode PX is arranged to permit creation of an electric field between itself and the counter electrode CT connected to the counter voltage signal line CL, wherein this electric field is used to control the optical transmissivity of the liquid crystal used.

[0045] One end of each gate signal line GL is extended to go beyond the seal material SL, wherein such extended end constitutes a terminal to which an output terminal of a vertical scan driving circuit V. Additionally, an input terminal of the vertical scan drive circuit V is such that a signal is input thereto from a printed wiring board, which is externally provided on the outer side of a liquid crystal display panel.

[0046] The vertical scan drive circuit V is made up of a plurality of pieces of semiconductor devices, wherein a plurality of mutually neighboring gate signal lines GL are grouped together with a single semiconductor device being assigned on a per-group basis.

[0047] Similarly, one end of each drain signal line DL is extended to exceed the seal material SL, wherein such extended end constitutes a terminal to which an output terminal of an image/video signal driving circuit He. Additionally an input terminal of the image signal drive circuit He is such that a signal is input thereto from a printed wiring board that is disposed outside the liquid crystal display panel.

[0048] This image signal drive circuit He also is made up of a plurality of semiconductor devices, wherein a plurality of mutually neighboring drain signal lines DL are grouped together with a single semiconductor device being assigned on a per-group basis.

[0049] Note that the counter voltage signal lines CL are commonly connected together at their end portions on the right side in **FIG. 2**. A connect line thereof is extended to exceed the seal material SL and thus constitutes a terminal CLT at its extended end. From this terminal CLT, a voltage which becomes a reference with respect to an image signal(s) is to be supplied.

[0050] Each of the above-noted gate signal lines GL is arranged so that one of them is sequentially selected by a scan signal from the vertical scan circuit V.

[0051] The drain signal lines DL are arranged so that an image signal is supplied by the image signal drive circuit He to a respective one of these lines at a timing as synchronized with the selection timing of the gate signal line GL.

[0052] It should be noted that although in the above-stated embodiment the vertical scan drive circuit V and the image signal drive circuit He are shown as the semiconductor devices which are mounted on the transparent substrate SUB1, alternative arrangements are also possible: for example, semiconductor devices of the so-called tape carrier scheme type are also employable which are connected in such a manner as to bridge between the transparent substrate SUB1 and the printed wiring board; furthermore, in the case where the semiconductor layer of the thin-film transistor TFT discussed above is made of polycrystalline silicon (p-Si), ones are useable with more than one semiconductor element made of the polysilicon being formed on the transparent substrate SUB1's surface together with a wiring layer(s) associated therewith.

[0053] <<Pixel Arrangement>>

[0054] **FIGS. 1A** to 1C depict one embodiment of an arrangement of the pixel region stated supra, wherein **FIG. 1A** shows a plan view, **FIG. 1B** shows a cross-sectional view as taken along line b-b of **FIG. 1A**, and **FIG. 1C** shows a sectional view along line c-c of **FIG. 1A**.

[0055] In each drawing, a pair of gate signal lines GL which extend in the x direction and are parallel-provided in the y direction are first formed on the liquid crystal-side surface of the transparent substrate SUB1.

[0056] These gate signal lines GL are arranged to surround a rectangular area together with a pair of drain signal lines DL, which will be described later. This area is for constitution of a pixel region.

[0057] In addition, at the center of the respective gate signal lines GL, a counter voltage signal line CL1 is formed in such a manner as to run in parallel with the gate signal lines GL. For example, this counter voltage signal line CL1 is formed simultaneously during fabrication of the gate signal lines GL.

[0058] On the surface of the transparent substrate SUB1 with the gate signal lines GL and counter voltage signal line CL1 formed thereon in this way, a dielectric film GI made for example of SiO_2 is formed to also cover or coat the gate signal lines GL and others.

[0059] This dielectric film GI has a function as an interlayer dielectric film with respect to the gate signal lines GL and the counter voltage signal line CL1 in a fabrication region of the drain signal lines DL to be later described and also has in a formation region of thin-film transistors TFT to be later described a function as the gate insulation films thereof.

[0060] And, a semiconductor layer AS made for example of amorphous Si is formed at a surface of this dielectric film GI in such a manner as to partially overlie and overlap the gate signal lines GL.

[0061] This semiconductor layer AS is that of a thin-film transistor TFT, and it is possible, by forming above its upper surface a drain electrode SD1 and a source electrode SD2, to make up a metal insulator semiconductor (MIS) transistor of the inverse stagger structure type with part of a gate signal line used as its gate electrode.

[0062] Here, the drain electrode SD1 and the source electrode SD2 are arranged so that they are formed simultaneously upon formation of the drain signal lines DL.

[0063] More specifically, drain signal lines DL which are extended in the y direction and parallel-provided in the x direction are formed, part of which is extended up to the upper surface of the semiconductor layer AS to thereby form the drain electrode SD1; additionally, the source electrode SD2 is formed while being spaced apart from this drain electrode SD1 by a distance equivalent to the channel length of the thin-film transistor TFT.

[0064] In addition, this source electrode SD2 is formed in a way integral with a pixel electrode PX to be formed within the pixel region.

[0065] More specifically, the pixel electrode PX is constituted from a group of a plurality of (two in the drawing) electrodes which extend in the y direction within the pixel region and are parallel-provided in the x direction. One end of a single pixel electrode PX of them functions also as the source electrode SD2; additionally, over the counter voltage signal line CL of an almost central portion, they are arranged to achieve mutual electrical connection at a corresponding portion of another pixel electrode PX which neighbors thereupon.

[0066] A protective film is formed above the surface of the transparent substrate SUB1 with the thin-film transistor TFT, drain signal lines DL, drain electrode SD1, source electrode SD2 and pixel electrode PX formed thereon in the way discussed above. This protective film is a film which precludes direct contact of the thin-film transistor TFT with the liquid crystal material to thereby prevent degradation of the characteristics of such thin-film transistor TFT.

[0067] It should be noted that this protective film is comprised of a sequential lamination body of a protective film PAS that is formed of an inorganic material layer such as SiN for example and a protective film OPAS formed of an organic material layer such as for example resin or the like. The use of at, least the organic material layer as the protective film is aimed at reduction of the dielectric constant of the protective film per se.

[0068] Thus, an effect or effects may be achieved by arranging it as the sequential lamination body of the first protective film and second protective film and also by arranging the second protective film using materials less in dielectric constant than the first protective film.

[0069] Here, in the protective film PAS to be formed over the gate signal lines GL, more than one opening is formed at a portion(s) of it while letting the protective film OPAS be stacked or multilayered in such a way as to bury or fill this opening. The function of the opening as formed in the protective film PAS will be explained later.

[0070] In this case, in view of the fact that the dielectric film GI is made of SiO_2 by way of example, this is expected to function as a stopper during hole formation of the protective film PAS.

[0071] A counter electrode CT is formed on an upper surface of the protective film OPAS. This counter electrode CT is constituted from a group of a plurality of (for example three in the drawing) electrodes which are extended in the y direction and are parallel-provided in the x direction in a similar way to that of the pixel electrode PX stated previously, wherein each of these electrodes is laid out so that the pixel electrode PX is placed between adjacent ones of them when planarly looking at the layout pattern.

[0072] More specifically, the counter electrodes CT and pixel electrodes PX are disposed with equal distances in the order of a counter electrode CT, pixel electrode PX, counter electrode CT, pixel electrode PX, . . . , counter electrode CT in a range spanning from a drain signal line DL on one side up to a drain signal line DL on the other side.

[0073] Here, the counter electrodes CT that are positioned on the both sides of the pixel region are such that a portion thereof is formed to overlap a drain signal line DL and simultaneously is formed commonly with a corresponding counter electrode CT of its neighboring pixel region.

[0074] In other words, a counter electrode CT is caused to overlie a drain signal line DL with their center axes being made substantially identical to each other, wherein the width of the counter electrode CT is formed to be greater than that of the drain signal line DL. A counter electrode CT on the left side of the drain signal line DL is arranged to constitute one of respective counter electrodes CT of a left-side pixel region; a counter electrode CT on the right side makes up one of respective counter electrodes CT of a pixel region on the right side.

[0075] By forming the counter electrode CT greater in width than the drain signal line DL at part overlying the drain signal line DL in this way, there is obtainable an effect such as the capability to preclude unwanted termination of electric flux lines from the drain signal line DL at the counter electrode CT and also termination at the pixel electrode PX. The reason of this is as follows: in case the electric flux lines from the drain signal line DL terminate at the pixel electrode PX, this would result in generation of noises.

[0076] And, each counter electrode CT made up of multiple components is formed integrally with a material layer which is the same layer as it and is made of the same material that is formed to sufficiently cover the gate signal lines GL.

[0077] Here, the material layer to be formed integrally with the counter electrode CT is formed of an optically transparent conductive layer made of indium tin oxide (ITO), indium tin zinc oxide (ITZO), indium zinc oxide (IZO), tin oxide (SnO_2), indium oxide (In_2O_3) or other similar suitable materials.

[0078] Since the counter electrode CT comprised of these materials and the material layer as formed integrally therewith are relatively large in electrical resistance, employ the aforementioned pattern while at the same time permitting electrical connection to the counter voltage signal line CL1 via more than one through-hole to be formed to penetrate the protective film OPAS, the protective film PAS and the dielectric film GI. A reference signal is supplied to each counter electrode CT through the counter voltage signal line CL1.

[0079] It should be noted that a portion of the material layer to be formed integrally with the each counter electrode CT while sufficiently covering the gate signal line GL will be referred to as the counter voltage signal line CL hereinafter. Because this portion functions as a signal line used to supply the reference signal to the counter electrode CT

together with the counter voltage signal line CL1 which is formed at the same layer as the gate signal lines GL.

[0080] Here, more than one opening is formed at part of the protective film PAS that was formed over the gate signal lines GL in the way stated supra, wherein the material layer integral with the counter electrode CT is formed above the upper surface of the protective film OPAS made of an organic material layer in such a manner as to bury this opening also.

[0081] More specifically, any protective film PAS formed of an inorganic material layer does not exist between the material layer integral with the counter electrode CT and the gate signal line(s) GL; thus, a portion is expected to exist, in which the protective film OPAS comprised of the organic material layer having an increased film thickness with the thickness of it added thereto will be formed.

[0082] Due to this, a parasitic capacitance Cgs between a gate signal line GL and counter electrode CT decreases in value, which in turn attains an effect of reducing waveform delays of a scan signal being supplied to the gate signal line GL.

[0083] And, the material layer which is formed to sufficiently cover the gate signal lines GL is such that the end portion of each pixel electrode PX is positioned at its portion which is extruded from the gate signal line GL whereby a capacitive element Cstg is formed between the pixel electrode PX and the counter electrode CT, with the protective film PSV and the protective film OPAS as a dielectric film thereof.

[0084] This capacitive element Cstg is designed to have the function of allowing an image signal supplied to the pixel electrode PX to be stored or accumulated therein for a relatively long time period.

[0085] And, over the upper surface of the transparent substrate SUB1 with counter electrodes CT formed thereon in this way, an optical orientation or alignment film (not shown) is formed in such a manner as to cover the counter electrodes CT also. This alignment film is a film that is in direct contact with liquid crystals, wherein rubbing as formed on its surface is used to determine the initial alignment directions of liquid crystal molecules.

[0086] Embodiment 2.

[0087] **FIG. 3** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 1C**.

[0088] An arrangement different when comparing to that of **FIG. 1C** lies in that at a portion whereat an opening is defined in the protective film PAS, a hole is formed also in its underlying dielectric film GI which is exposed there from. In the case using this arrangement, similar effects are obtainable.

[0089] In this case, SiN which is the same as the material of the protective film PAS may alternatively be used as the material of the dielectric film GI.

[0090] Embodiment 3.

[0091] **FIG. 4** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 3**.

[0092] A different arrangement from that shown in **FIG. 3** is that aluminum (Al) or tantalum (Ta) is used as the material of gate signal lines GL, wherein a respective one is structured so that an oxide film of Al_2O_3 or Ta_2O_3 is formed on its surface by anodization techniques. In the case of employing this structure also, similar effects may also be obtained.

[0093] Embodiment 4.

[0094] **FIGS. 5A** to **5C** are arrangement diagrams showing yet another embodiment of the liquid crystal display device in accordance with the invention, which are drawings corresponding to FIGS. **1A-1C**, respectively.

[0095] Firstly, a difference in arrangement from that shown in FIGS. **1A-1C** is that in the counter voltage signal line CL as formed to overlap the part at which a hole is defined in the protective film PAS, a hole HOL is formed within the region of the hole so that the former hole is less in area than the latter.

[0096] In this case, as shown in **FIG. 5C**, when letting the width for overlap of a pixel electrode PX and counter electrode CT be "A," the width for overlap of a gate signal line GL and counter electrode CT be "B," the width for overlap of a protective film PAS and gate signal line GL be "C," the width of spacing between the gate signal line GL and pixel electrode PX be "D," the width of a hole of the counter voltage signal line be "E," and the width of a hole of the protective film PAS be "F," these values are set to be greater than zero (0).

[0097] The liquid crystal display device thus arranged in this way is capable of suppressing potential variations of the pixel electrode PX because the formation of the hole HOL in the counter voltage signal line CL reduces a parasitic capacitance between it and the gate signal line GL associated therewith.

[0098] Also note that in the steady state upon turning off of a thin-film transistor TFT, the capacitance Csc at the width A of an overlap between the pixel electrode PX and counter voltage signal line CL behaves to function as a capacitive element Cstg. If the counter voltage signal line CL is not formed, then a jumping voltage occurring due to the gate signal line GL of pixel electrode PX would increase.

[0099] And, in the steady state when the thin-film transistor TFT turns off, it is possible to minimize variations of the gate signal line GL by way of the capacitance Cgc at the width B of an overlap between the gate signal line GL and counter electrode CT and also the capacitance Csc at the width A of an overlap between the pixel electrode PX and counter electrode CT. If no holes are formed in the counter voltage signal line CL, then a potential variation of the gate signal line GL results in the counter voltage signal line CL varying in potential, which in turn causes the pixel electrode PX to potentially vary due to the capacitance Csc.

[0100] Additionally, provision of the width C of an overlap between the protective film PAS and gate signal line GL is aimed at preclusion of electrolytic corrosion of the gate signal line GL by letting at least peripheral portions of the gate signal line GL be covered by or coated with the protective film PAS in view of the fact that the electric field strength or intensity of the gate signal line GL can increase at the peripheral portions of gate signal line GL due to the presence of the counter voltage signal line CL.

[0101] Further, an arrangement is employed which reduces the parasitic capacitance Cgs between the gate signal line GL and pixel electrode PX by means of the width D, by which the gate signal line GL and the pixel electrode PX are spaced apart from each other.

[0102] Embodiment 5.

[0103] **FIG. 6A** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 5A**. Additionally, **FIG. 6B** shows a cross-sectional view as taken along line b-b of **FIG. 6A**.

[0104] A different arrangement from that of **FIG. 5A** is that the hole HOL which is formed in the counter voltage signal line CL being formed to overlap its associated gate signal line GL is formed so that its width is greater than the width of the gate signal line GL.

[0105] With such an arrangement, it becomes possible to significantly reduce the parasitic capacitance between the gate signal line GL and the counter voltage signal line CL, which in turn makes it possible to reduce a waveform delay of the gate signal line GL.

[0106] Embodiment 6.

[0107] **FIG. 7** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, wherein this is a drawing corresponding to **FIG. 6A**.

[0108] A different arrangement from that of **FIG. 6A** is that the hole HOL which is formed in the counter voltage signal line CL being formed to overlap the gate signal line GL is designed so that a plurality of ones are formed along the running direction of this gate signal line GL.

[0109] With such an arrangement also, it is possible to greatly reduce the parasitic capacitance between the gate signal line GL and counter voltage signal line CL, which in turn makes it possible to reduce a waveform delay of the gate signal line GL.

[0110] Embodiment 7.

[0111] **FIG. 8** is an arrangement diagram showing still another embodiment of the liquid crystal display device in accordance with the invention, wherein this is a drawing corresponding to **FIG. 7**.

[0112] Although in **FIG. 7** the holes HOL which are formed in the counter voltage signal line CL being formed to overlap the gate signal line GL is such that each hole is patterned into a round or circular shape, a rectangular shape pattern is used in **FIG. 8** while letting each hole of this rectangular shape be formed to have a little inclination or gradient with respect to the running direction of the gate signal line GL.

[0113] This is in order to reduce the leakage of an electric field from the gate signal line GL to the pixel region side.

[0114] Embodiment 8.

[0115] **FIG. 9A** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 5A**. Additionally, a cross-sectional view taken along line b-b of **FIG. 9A** is shown in **FIG. 9B**.

[0116] In this embodiment, a spacer which retains a gap between the transparent substrate SUB1 and transparent substrate SUB2 in the liquid crystal display unit AR is constituted from a spacer SP with its shape resembling a support rod or pillar, wherein this support pillar-like spacer is formed on the transparent substrate SUB2 side while at the same time causing its top portion to be positioned at a portion of the hole HOL of the counter voltage signal line CL.

[0117] The pillar-like spacer SP is the one that is fabricated by selective etching processes using a photolithography technique as applied to a resin film which is formed on the transparent substrate SUB2 side and which is made of acryl or polyimide or the like, wherein its relative dielectric constant is set smaller than that of liquid crystals.

[0118] Due to this, it becomes possible to further reduce the parasitic capacitance occurring between it and the drain signal line DL.

[0119] Embodiment 9.

[0120] **FIG. 10** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 9B**.

[0121] On the liquid crystal-side surface of the transparent substrate SUB2, a black matrix BM is formed so that it overlaps at least the gate signal line GL. This black matrix BM is structured for example from a resin layer with its relative resistance of $10^8\Omega\cdot cm$ or less or alternatively from a metal layer. The metal layer may be made from Cr by way of example. In this case, letting it have a stacked or multi-layered structure of Cr and Cr-oxide makes it possible to reduce the reflection factor or "reflectivity."

[0122] With such an arrangement, it is possible to shield any leakage electric field from the gate signal line GL owing to the black matrix BM.

[0123] Also note that in such the arrangement, further effects and advantages are achievable by forming on or above the surface of the black matrix BM a color filter CF or a planarization film (not shown) or the like which is formed to overlie the black matrix BM also by use of low-resistance materials as shown in **FIG. 11**.

[0124] Embodiment 10.

[0125] **FIGS. 12A** to **12C** are arrangement diagrams showing another embodiment of the liquid crystal display device in accordance with the invention, which are drawings corresponding to FIGS. **5A-5C** respectively.

[0126] A different arrangement from that of FIGS. **5A-5C** is that the more than one hole being formed in the protective film PAS is formed not only over the gate signal line GL but also over the drain signal line DL.

[0127] Holes HOL1 to be formed in the protective film PAS overlying a drain signal line DL are formed along this drain signal line DL while permitting exposure of a central portion excluding each peripheral portion in parallel with the running direction of the drain signal line DL.

[0128] Whereby, the protective film which is interposed between the drain signal line DL and the counter electrode CT becomes only a protective film OPAS formed of an

organic material layer; thus, it is possible to reduce the parasitic capacitance as formed between the drain signal line DL and counter electrode CT, which in turn attains an effect as to the ability to suppress waveform delays of respective signals being supplied to the drain signal line DL and the counter electrode CT respectively.

[0129] Embodiment 11.

[0130] **FIG. 13** is an arrangement diagram showing another embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 12C**.

[0131] A difference in arrangement from **FIG. 12C** lies in that the holes HOL1 are defined in the protective film PAS while arranging the drain signal line DL so that its each peripheral portion in parallel to the running direction of this line also is exposed.

[0132] In this case, it is desirable to use SiO_2 as the material of the dielectric film GI. This can be said because the hole-opening process of the protective film PAS results in the dielectric film GI having the function of a stopper.

[0133] Embodiment 12.

[0134] **FIG. 14** is an arrangement diagram showing another further embodiment of the liquid crystal display device in accordance with the invention, which is a drawing corresponding to **FIG. 13**.

[0135] A difference in arrangement from **FIG. 13** is that the dielectric film GI is comprised of SiN by way of example and also in that this dielectric film GI also is subjected to a hole-opening process, with the drain signal line DL as a mask, simultaneously during the hole-opening step of the protective film PAS.

[0136] Embodiment 13.

[0137] FIGS. **15A-15B** are arrangement diagrams showing another embodiment of the liquid crystal display device in accordance with the invention, which are drawings corresponding to FIGS. **9A-9B** respectively.

[0138] A difference in arrangement from FIGS. **9A-9B** is that the top portion of the support pillar-like spacer SP as formed on the transparent substrate SUB2 side is positioned within the hole HOL that was formed in the counter voltage signal line CL to thereby guarantee that it does not come into direct contact with the counter voltage signal line CL.

[0139] With such an arrangement, it is possible to attain an effect that any wipe displacement hardly occurs upon adding a pressure in the horizontal direction of a display screen (during wipe deviation test).

[0140] Embodiment 14.

[0141] **FIG. 16A** is a diagram showing a plan view of yet another further embodiment of the liquid crystal display device in accordance with the invention. In addition, **FIG. 16B** is a cross-sectional view taken along line b-b of **FIG. 16A**.

[0142] FIGS. **16A-16B** show a pixel structure of the type using the so-called longitudinal electric field scheme. First, a difference in arrangement from that of FIGS. **1A-1C** lies in its pixel electrode PX. This pixel electrode PX is so formed as to cover the entire area of a pixel region on the surface of a sequential lamination body which consists essentially of a protective film PAS that is made of an inorganic material and is formed to also cover a thin-film transistor TFT and a protective film OPAS made of an organic material.

[0143] And, this pixel electrode PX is comprised of a transparent conductive film made for example of indium tin oxide (ITO), indium tin zinc oxide (ITZO), indium zinc oxide (IZO), tin oxide (SnO_2), indium oxide (In_2O_3) or the like.

[0144] Peripheral part of the pixel electrode PX is formed to overlap the drain signal line DL and gate signal line GL to thereby enable pixels to improve in aperture ratio.

[0145] A counter electrode which causes an electric field to generate between it and the pixel electrode PX is constituted from a transparent conductive film such as for example ITO or else, which is formed on the liquid crystal-side surface of the other transparent substrate SUB2 in common to each pixel region.

[0146] In this case, a plurality of holes HOL2 are formed and arranged in the protective film PAS made of inorganic material within the pixel region and its underlying dielectric film GI, wherein each hole penetrates them.

[0147] In the case employing this arrangement, the protective film OPAS made of organic material to be formed on the upper surface of the protective film PAS is formed so that it is buried in the holes HOL2; thus, it is possible to prevent unwanted deviation of the protective film OPAS.

[0148] This remedy becomes necessary in light of the fact that the protective film OPAS made of organic material is such that deviation due to thermal hysteresis can easily take place therein.

[0149] As apparent from the foregoing explanations, according to the liquid crystal display device of the present invention, it is possible to reduce waveform delays of scan signals to be supplied to the gate signal lines.

[0150] It is also possible to reduce waveform delays of image or video signals being supplied to the drain signal lines.

What is claimed is:

1. A liquid crystal display device comprising:

first substrate and second substrate with a liquid crystal layer therebetween;

a plurality of gate signal lines formed on the first substrate and a plurality of drain signal lines formed on the first substrate and intersect with the plurality of gate signal lines;

a plurality of switching element operable by a scan signal from a gate signal line, at least a pixel electrode to which an image signal is supplied through the switching element from a drain signal line in each pixels, and at least a counter electrode for creating an electric field with the pixel electrode in each pixels;

wherein at least one of said counter electrode is arranged along a running direction of said drain signal line and overlap with the drain signal line with dielectric film therebetween, at least one of said counter electrode or counter voltage signal line integrated with the counter

electrode is arranged along a running direction of said gate signal line and overlap with said gate signal line with dielectric film therebetween, and

said dielectric film is comprised of a sequential lamination body of at least a protective film made of an inorganic material and a protective film made of an organic material, wherein an opening is formed at part of said protective film made of the inorganic material underlying at least either one of said counter voltage signal line and said counter electrode, the opening being filled with the protective film made of the organic material.

2. The liquid crystal display device according to claim 1, wherein at least an opening which has a smaller area than the opening formed at part of said protective film is formed in at least one of a counter voltage signal line or counter electrode overlying said protective film in which the opening is formed.

3. The liquid crystal display device according to claim 2, wherein the pixel electrode has a band-like pattern which is extended in the running direction of the drain signal line, and wherein one end of said pixel electrode being disposed adjacent to a hole formed in said counter voltage signal line is caused to overlap this counter voltage signal line and is spaced apart from the gate signal line.

4. The liquid crystal display device according to claim 2, wherein the switching element is formed of a thin-film transistor, wherein a sequential lamination body of a dielectric film for also use as a gate insulation film of the thin-film transistor and a protective film made of an inorganic material plus a protective film made of an organic material is formed above a gate signal line GL, and wherein a hole to be formed in said protective film made of the inorganic material is formed to penetrate said dielectric film at its lower layer.

5. The liquid crystal display device according to claim 4, wherein a hole to be formed in said protective film made of the inorganic material and in the dielectric film is formed within the region of the gate signal line.

6. A liquid crystal display device comprising:

first substrate and second substrate with a liquid crystal layer therebetween;

a plurality of gate signal lines formed on the first substrate and a plurality of drain signal lines formed on the first substrate and intersect with the plurality of gate signal lines;

a plurality of switching element operable by a scan signal from a gate signal line, at least a pixel electrode to which an image signal is supplied through the switching element from a drain signal line in each pixels, and at least a counter electrode for creating an electric field with the pixel electrode in each pixels;

wherein at least one of said counter electrode is arranged along a running direction of said drain signal line and overlap with the drain signal line with dielectric film therebetween, at least one of said counter electrode or counter voltage signal line integrated with the counter electrode is arranged along a running direction of said gate signal line and overlap with said gate signal line with dielectric film therebetween, and

said dielectric film is constituted from a sequential lamination body of a first protective film and a second protective film overlapping said first protective film and being lower in dielectric constant than said first protective film, wherein an opening is formed at part of said first protective film underlying at least either one of said counter voltage signal and said counter electrode, said opening being filled with said second protective film.

7. The liquid crystal display device according to claim 6, wherein at least an opening which has a smaller area than the opening formed at part of said protective film is formed in at least one of a counter voltage signal line or counter electrode overlying said protective film in which the opening is formed.

8. The liquid crystal display device according to claim 7, wherein the pixel electrode has a band-like pattern which is extended in the running direction of the drain signal line, and wherein one end of said pixel electrode being disposed adjacent to a hole formed in said counter voltage signal line is caused to overlap this counter voltage signal line and is spaced apart from the gate signal line.

9. The liquid crystal display device according to claim 7, wherein the switching element is formed of a thin-film transistor, wherein a sequential lamination body of a dielectric film for also use as a gate insulation film of the thin-film transistor and a first protective film plus a second film is formed above a gate signal line GL, and wherein a hole to be formed in the first protective film is formed to penetrate its underlying dielectric film for also use as the gate insulation film.

10. The liquid crystal display device according to claim 9, wherein said first protective film and a hole to be formed in this protective film is formed within the gate signal line.

11. A liquid crystal display device comprising:

first substrate and second substrate with a liquid crystal layer therebetween;

a plurality of gate signal lines formed on the first substrate and a plurality of drain signal lines formed on the first substrate and intersect with the plurality of gate signal lines;

a plurality of switching element operable by a scan signal from a gate signal line, at least a pixel electrode to which an image signal is supplied through the switching element from a drain signal line in each pixels, and at least a counter electrode for creating an electric field with the pixel electrode in each pixels;

wherein at least one of said counter electrode is arranged along a running direction of said drain signal line and overlap with the drain signal line with dielectric film therebetween, at least one of said counter electrode or counter voltage signal line integrated with the counter electrode is arranged along a running direction of said gate signal line and overlap with said gate signal line with dielectric film therebetween,

at least an opening is made in one of said counter voltage signal line and the counter electrode, and

said an opening is arranged to partially overlap with the gate signal line.

12. The liquid crystal display device according to claim 11, further comprising support pillar-like spacer formed on or above the liquid crystal-side surface of the second substrate, wherein a top portion of a support pillar-like spacer is provided in such a way as to oppose to said opening.

13. The liquid crystal display device according to claim 12, wherein said spacer is made of a material less in dielectric constant than said liquid crystal.

14. The liquid crystal display device according to claim 11, wherein said dielectric film has a first protective film and a second protective film overlapping the first protective film, wherein a hole is formed in the first protective film within a region overlapping said hole, and wherein the hole of the first protective film is filled with the second protective film.

15. The liquid crystal display device according to claim 14, wherein said first protective film is an inorganic film and wherein said second protective film is an organic film.

16. The liquid crystal display device according to claim **14**, wherein said second protective film is lower in dielectric constant than said first protective film.

17. The liquid crystal display device according to claim 11, further comprising a black matrix formed above the liquid crystal-side surface of the second substrate at least at a position opposing-said opening, wherein this black matrix is set in resistivity at 10^8 Ω·cm or less.

18. The liquid crystal display device according to claim 11, further comprising a black matrix formed above the liquid crystal-side surface of the second substrate at least at a position opposing said opening, wherein this black matrix is include at least a metal or metal-alloy material.

19. The liquid crystal display device according to claim 17, wherein said black matrix has a metal or metal-alloy.

20. The liquid crystal display device according to claim 18, wherein said black matrix contains therein chromium (Cr).

* * * * *

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申请(专利权)人(译)	仓桥NAGATOSHI NAKAYOSHI昭 柳川和彦		
当前申请(专利权)人(译)	仓桥NAGATOSHI NAKAYOSHI昭 柳川和彦		
[标]发明人	KURAHASHI NAGATOSHI NAKAYOSHI YOSHIAKI YANAGAWA KAZUHIKO		
发明人	KURAHASHI, NAGATOSHI NAKAYOSHI, YOSHIAKI YANAGAWA, KAZUHIKO		
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摘要(译)

一种液晶显示装置，其在同一基板上具有像素电极和对电极，并且至少一个对电极与视频信号线重叠，栅极信号线在其间具有介电膜，所述介电膜由以下的顺序层叠体构成。至少一种由无机材料制成的保护膜和由有机材料制成的保护膜，在由所述对电极下面的无机材料制成的所述保护膜的一部分上形成开口，并且所述开口填充有由所述保护膜制成的保护膜。有机材料。