



US 20040066360A1

(19) **United States**(12) **Patent Application Publication**  
Tobita(10) **Pub. No.: US 2004/0066360 A1**(43) **Pub. Date: Apr. 8, 2004**(54) **IMAGE DISPLAY UNIT**(52) **U.S. Cl. .... 345/87**(76) **Inventor: Youichi Tobita, Hyogo (JP)**(57) **ABSTRACT**

Correspondence Address:

**LEYDIG VOIT & MAYER, LTD****700 THIRTEENTH ST. NW****SUITE 300****WASHINGTON, DC 20005-3960 (US)**(21) **Appl. No.: 10/450,148**(22) **PCT Filed: Feb. 6, 2002**(86) **PCT No.: PCT/JP02/00991****Publication Classification**(51) **Int. Cl.<sup>7</sup> ..... G09G 3/36**

This color image display (1) includes: a liquid crystal cell (3) having a light transmittance varying according to a potential at a data holding node (N21); a scan circuit (5, 7, 8, 11) applying one of first and second potentials (VH, VL) to the data holding node (N21) in accordance with an image signal (DR, DG, DB, SN1, SN2); and a refresh circuit (22, 23, 25) performing refresh of a potential at the data holding node (N21) to a first potential in response to a refresh signal (REF) when the potential at the data holding node (N21) exceeds a threshold potential (VTN) of an N-type TFT, while performing no refresh of the potential at the data holding node (N21) when the potential at the data holding node (N21) does not exceed the threshold potential (VTN).

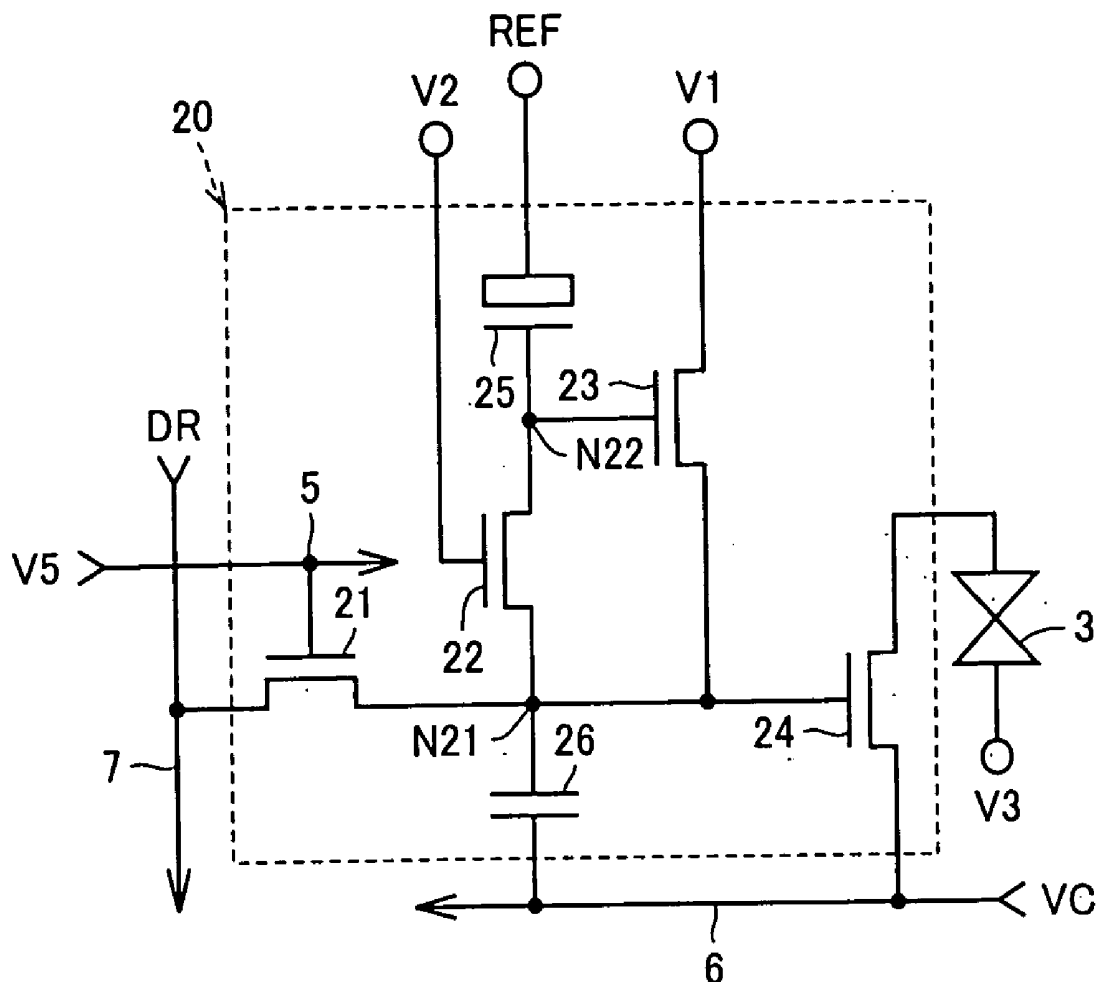


FIG. 1

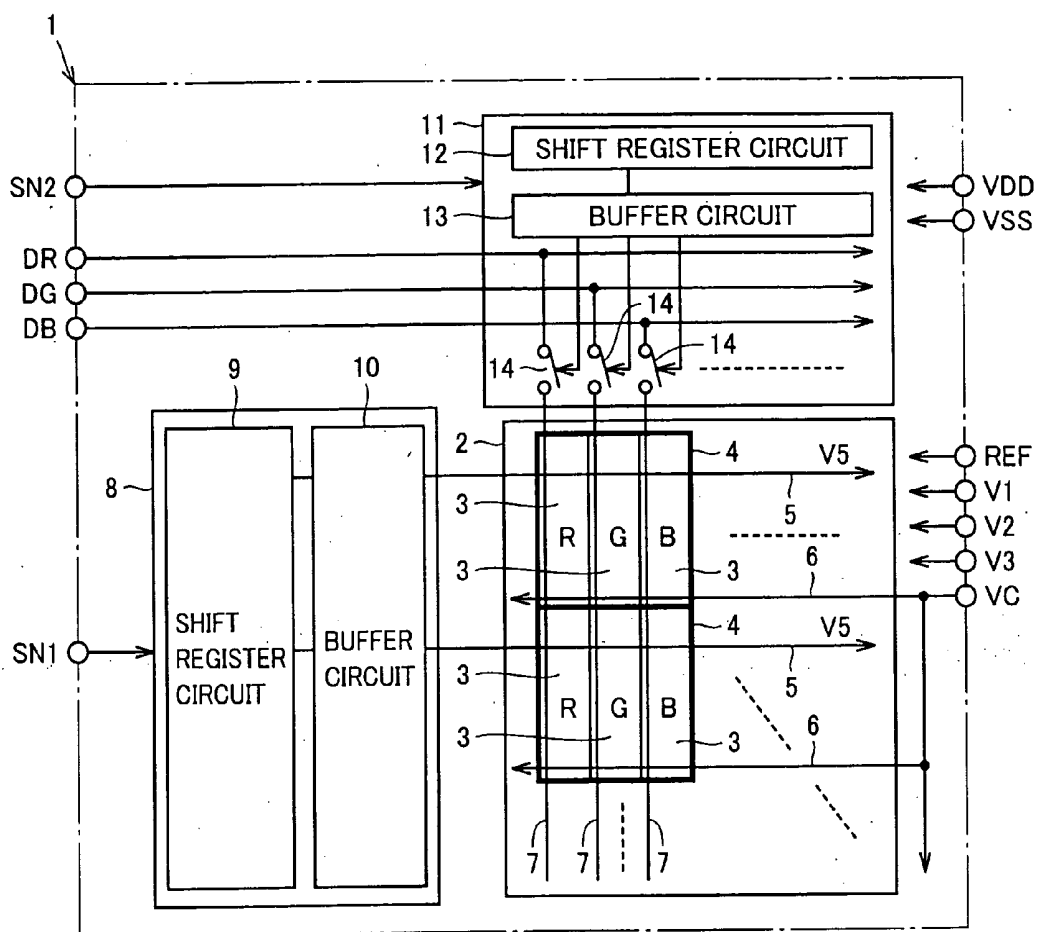


FIG.2

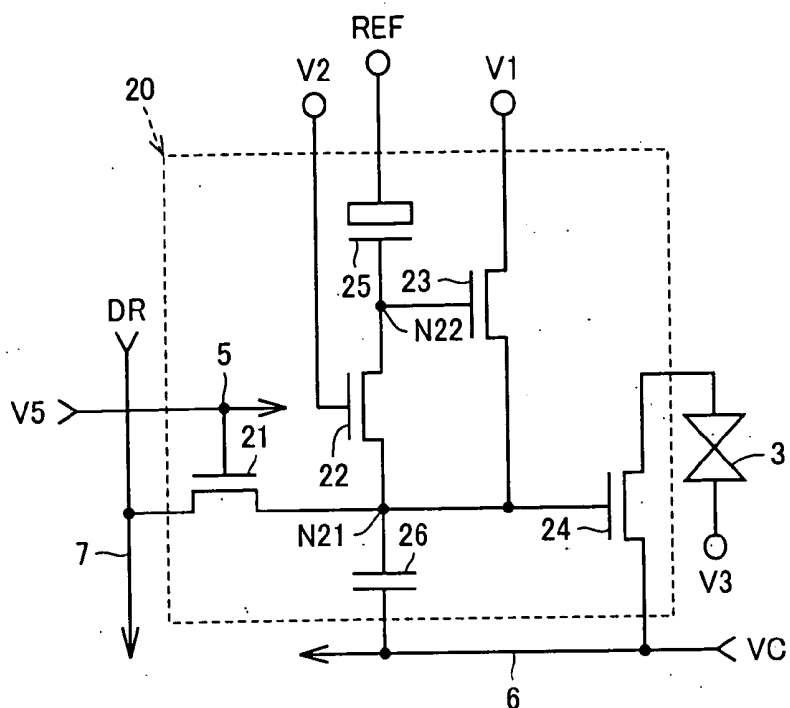


FIG.3

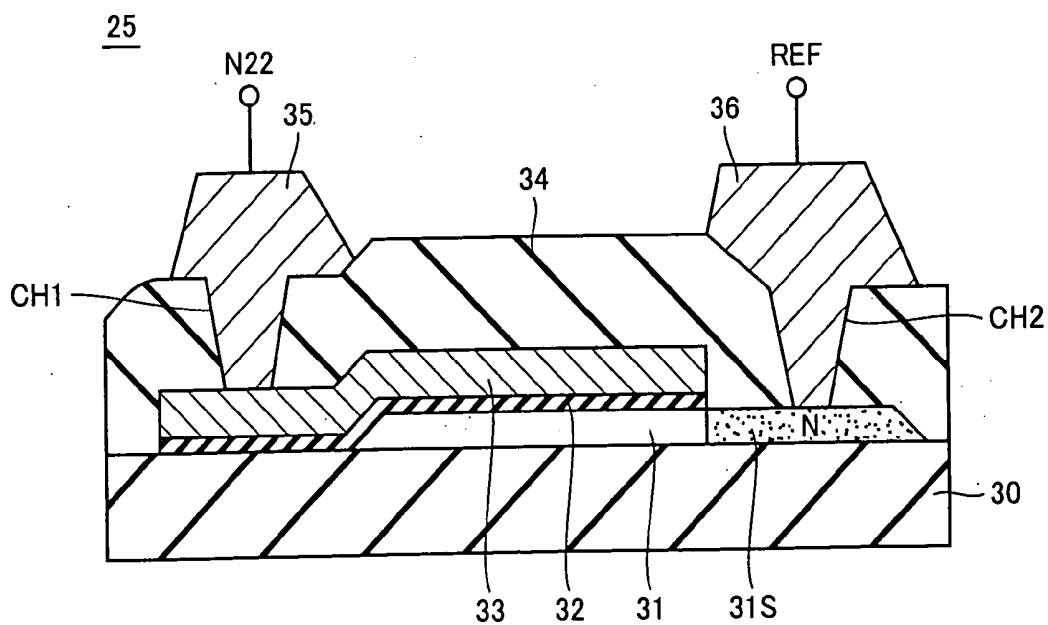


FIG. 4

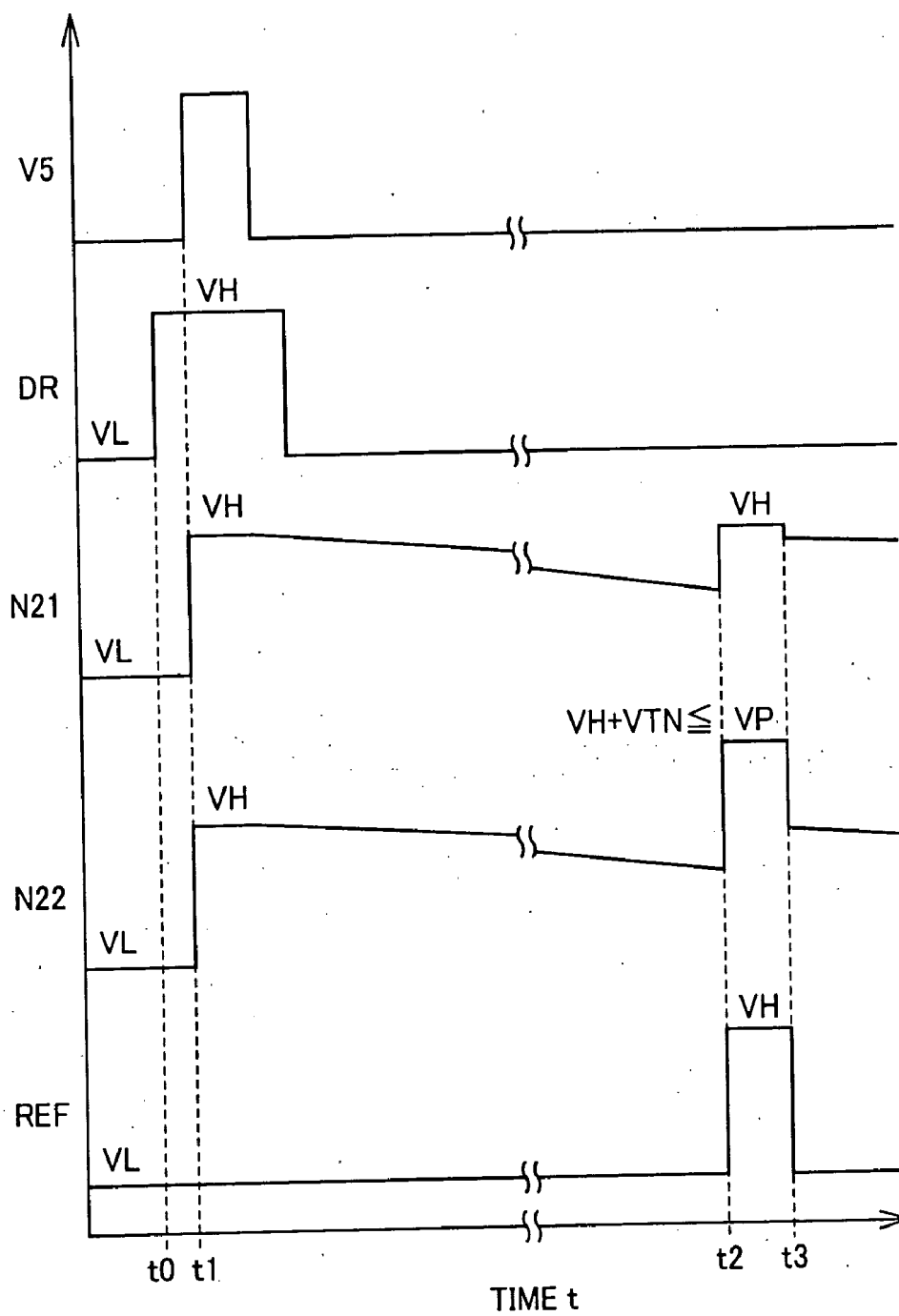
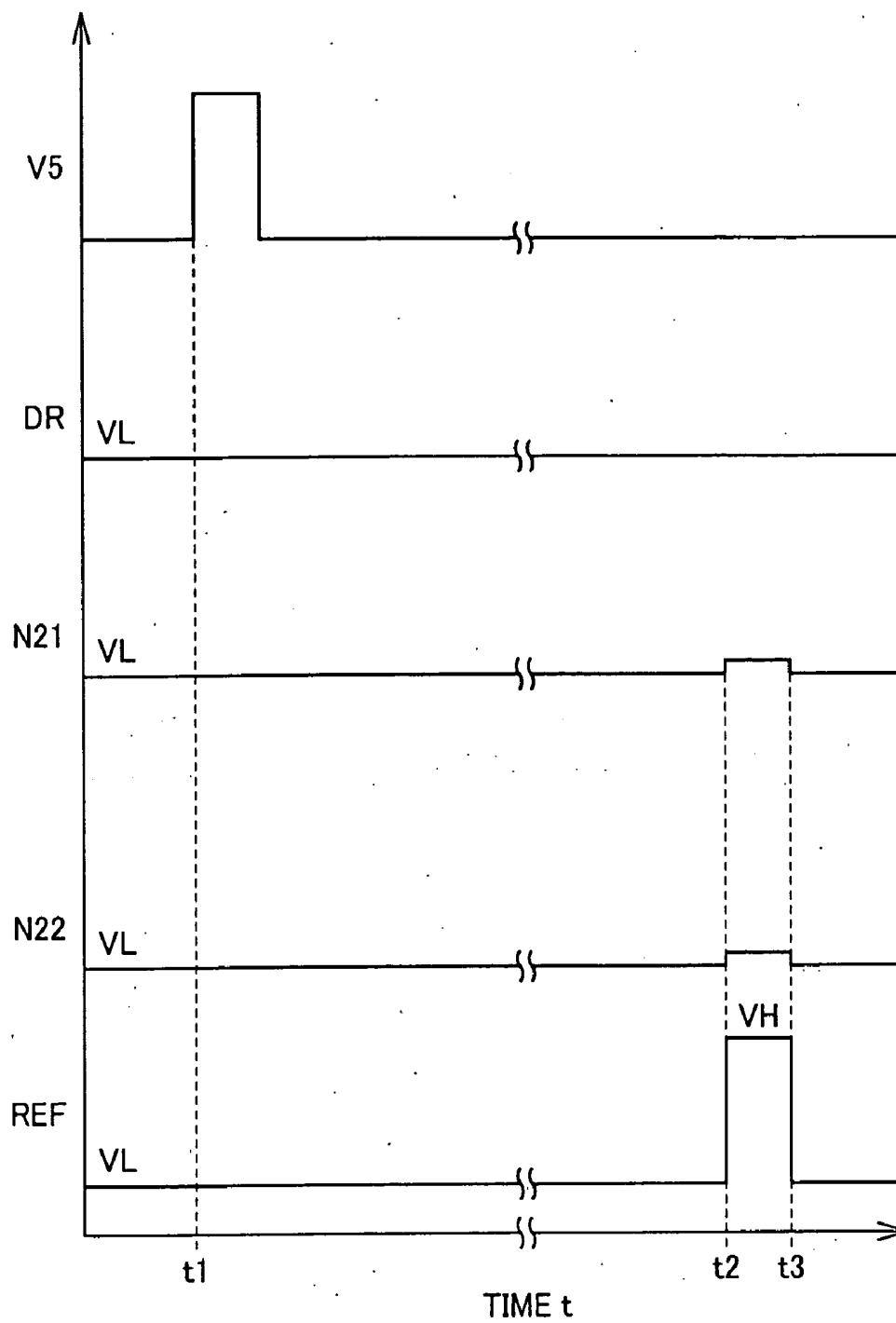


FIG. 5



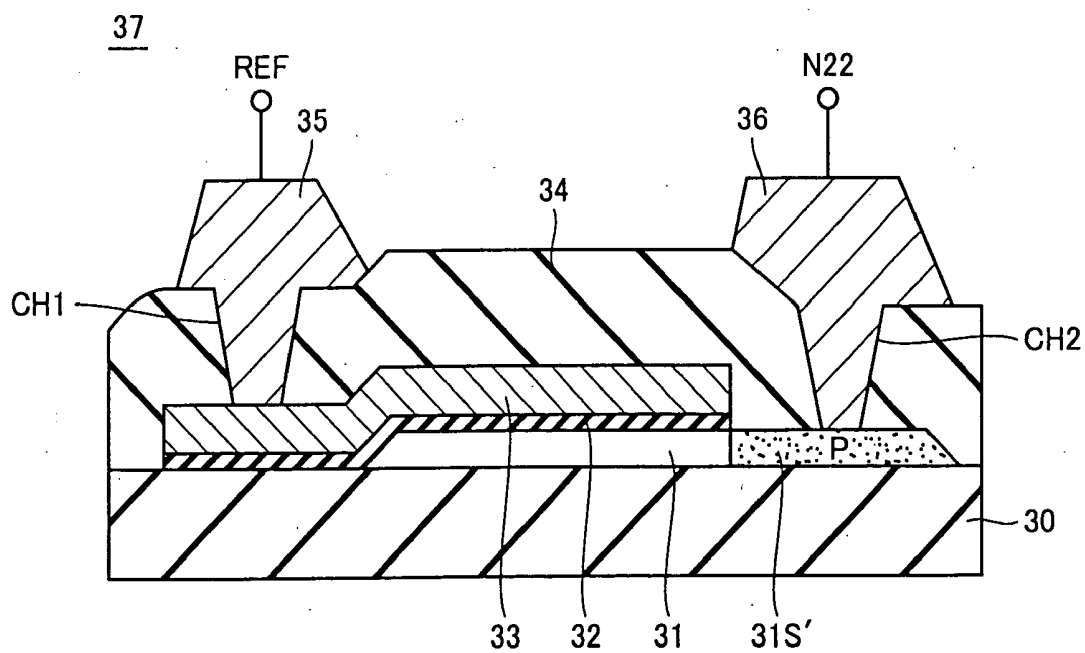




FIG.9

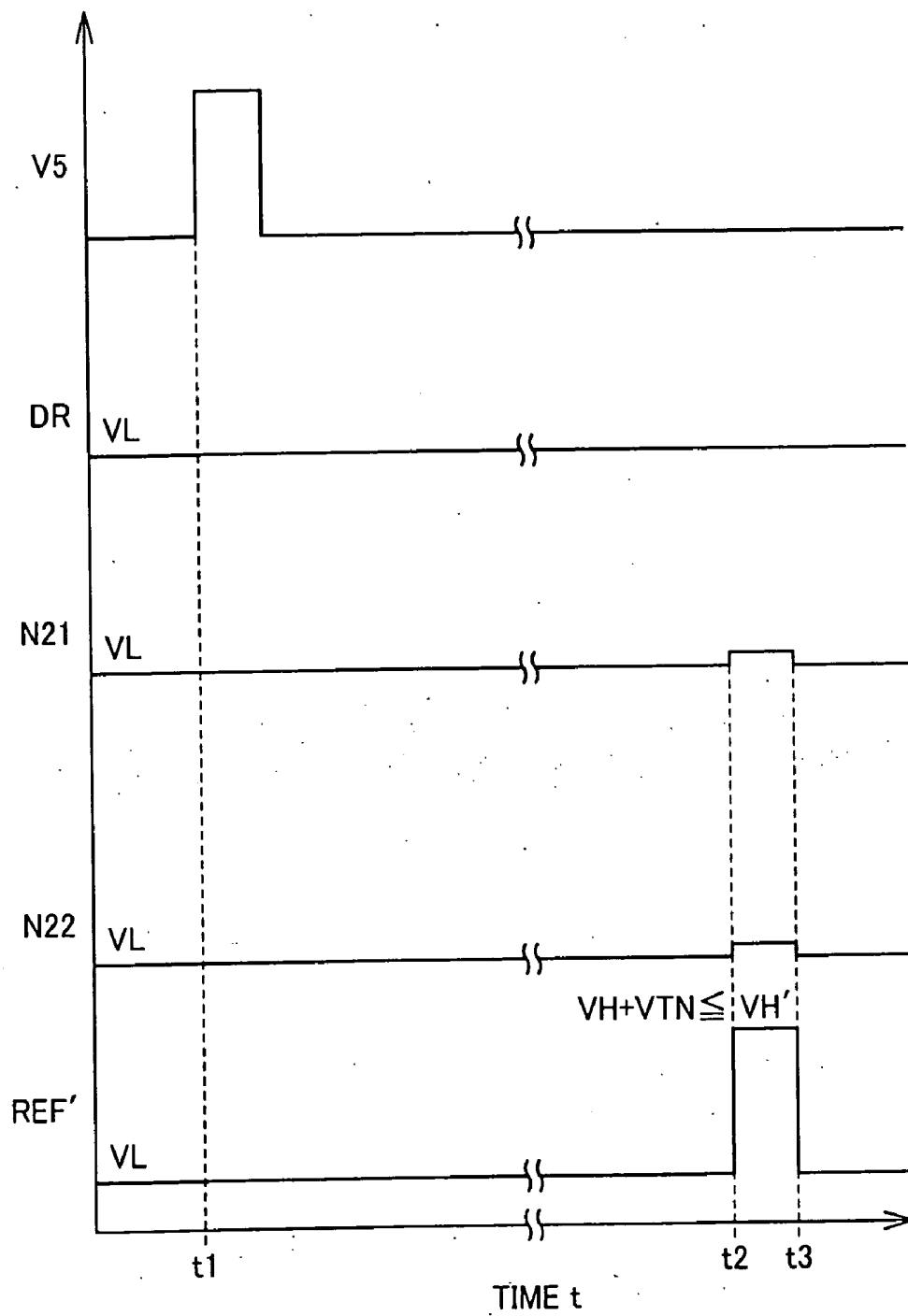




FIG.10

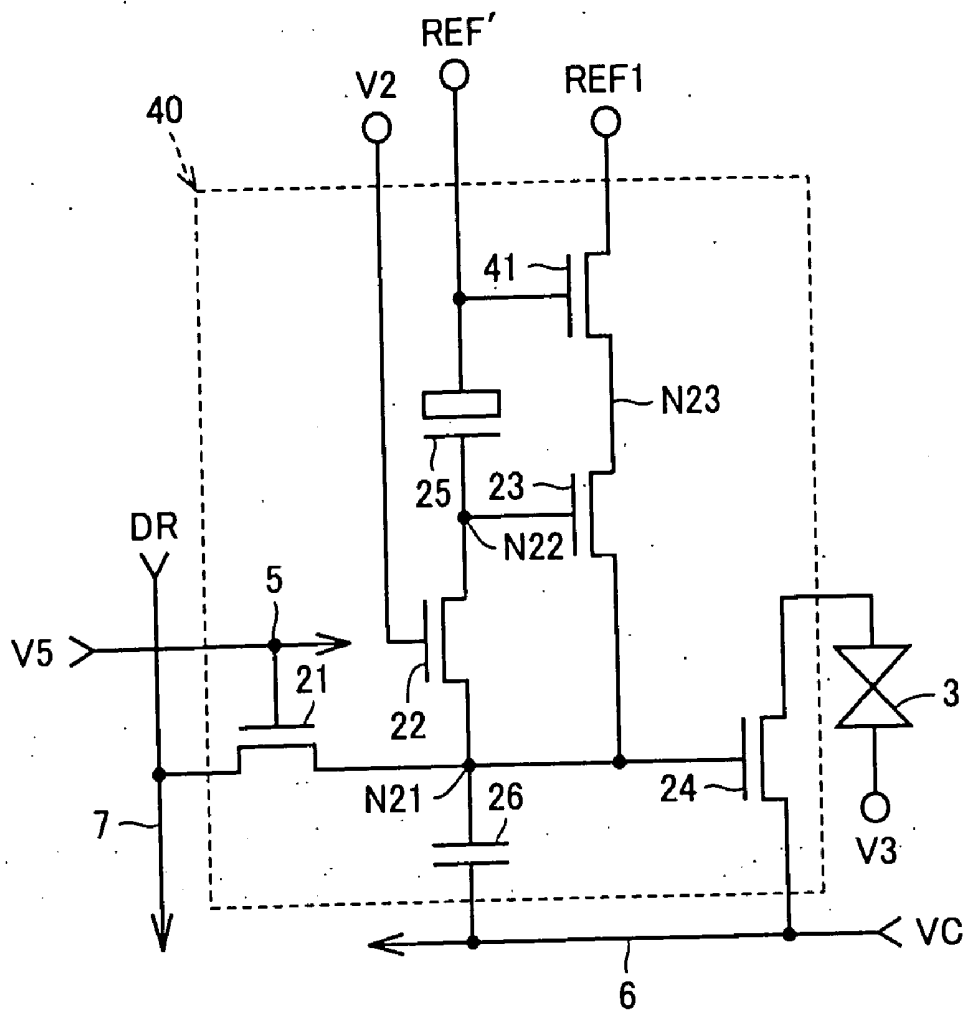


FIG.11

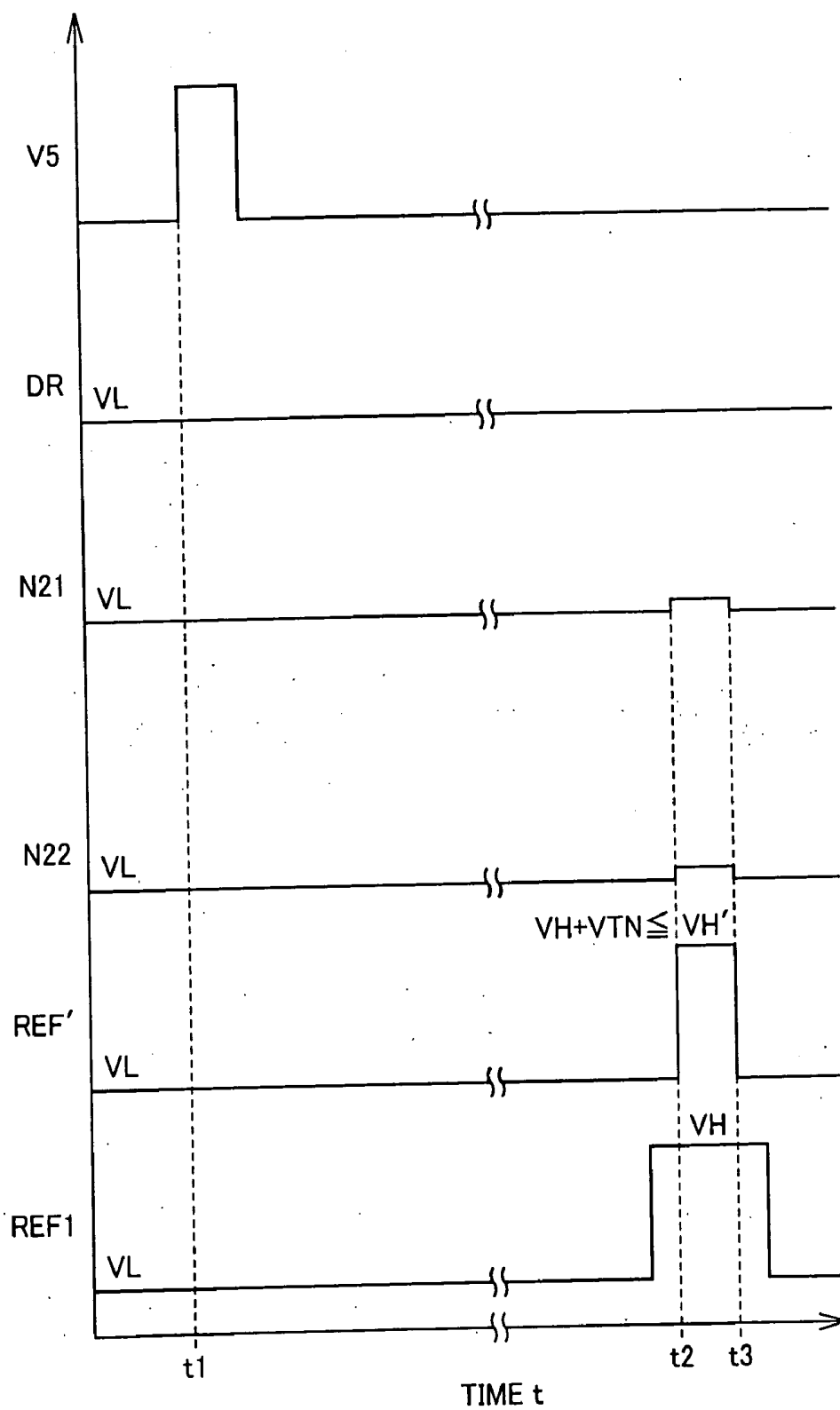






FIG.15

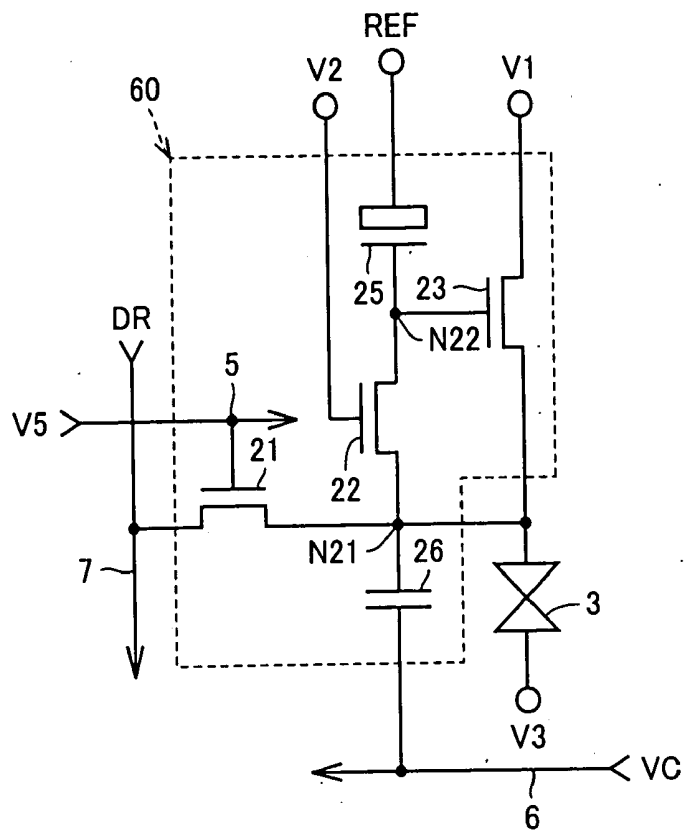


FIG.16

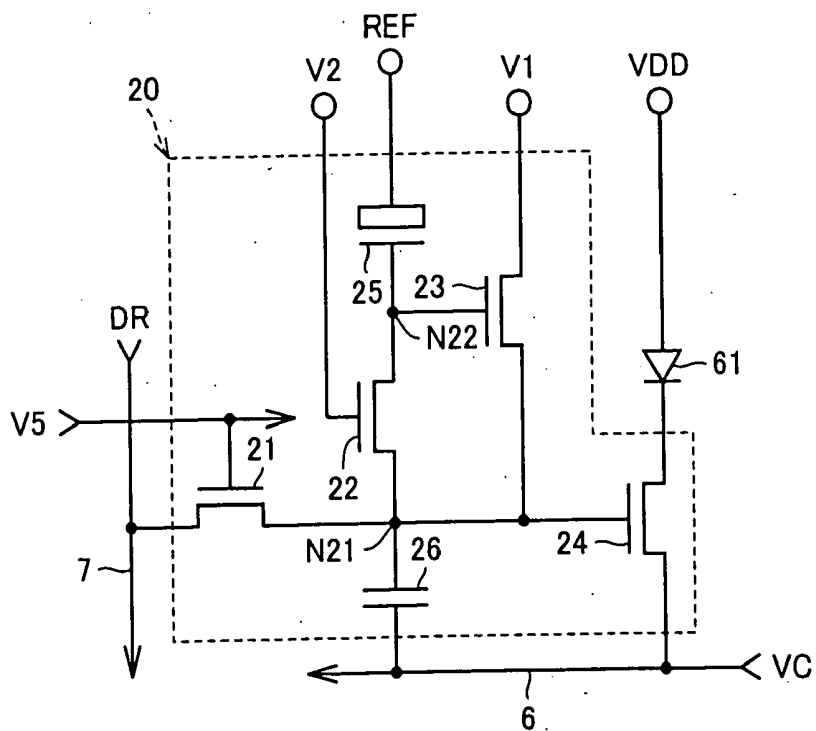


FIG.17 PRIOR ART

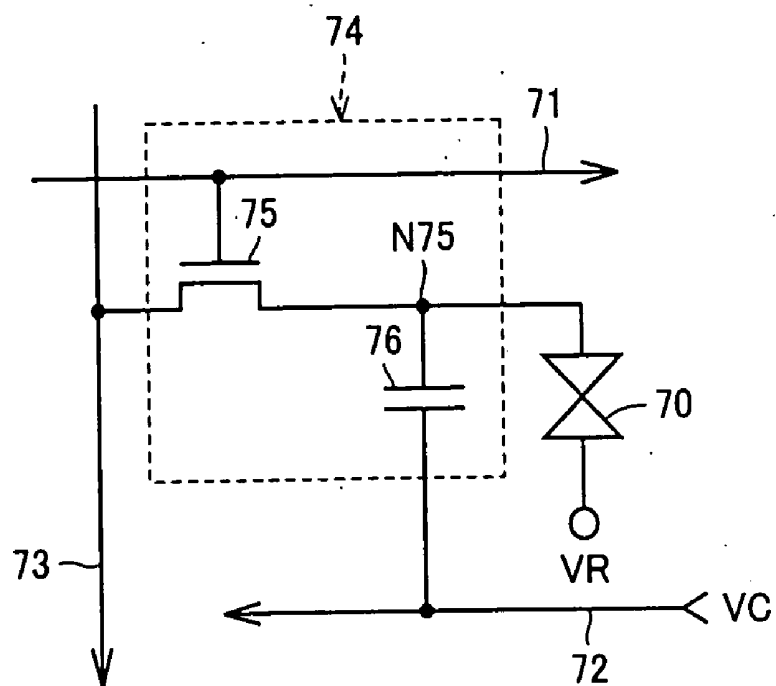
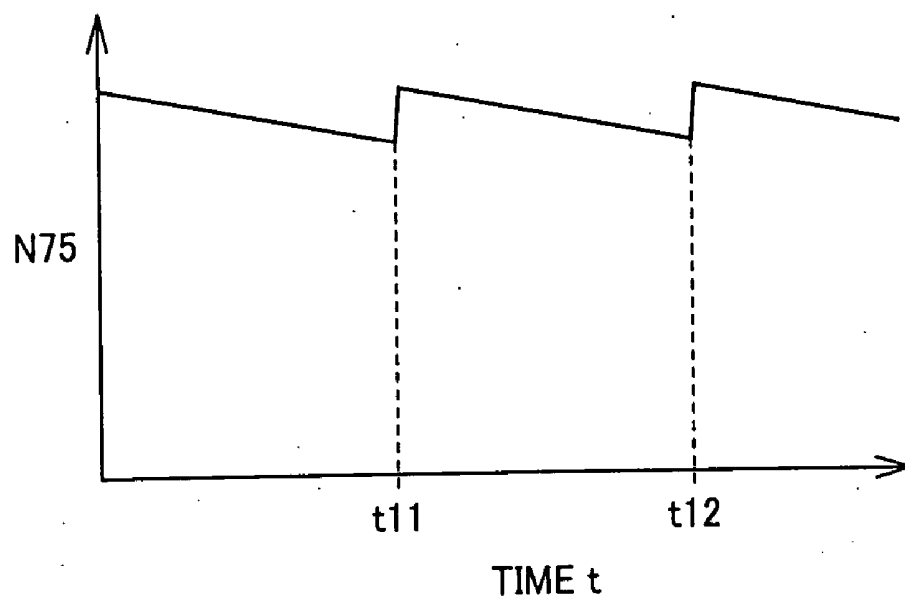


FIG.18 PRIOR ART



## IMAGE DISPLAY UNIT

### TECHNICAL FIELD

[0001] The present invention relates to an image display and, more particularly, to an image display that requires refreshing of a data signal.

### BACKGROUND ART

[0002] A liquid crystal display for displaying a still picture and a moving picture has conventionally been employed in a personal computer, a television receiver, a portable telephone, a portable information terminal and the like.

[0003] FIG. 17 is a circuit diagram showing a main part of such a liquid crystal display. In FIG. 17, this liquid crystal display includes a liquid crystal cell 70, a scan line 71, a common potential line 72, a data signal line 73 and a liquid crystal drive circuit 74, wherein liquid crystal drive circuit 74 includes an N-type TFT (Thin Film Transistor) 75 and a capacitor 76.

[0004] N-type TFT 75 is connected between data signal line 73 and a data holding node N75 and having the gate connected to scan line 71. Capacitor 76 is connected between data holding node N75 and common potential line 72. One electrode of liquid crystal cell 70 is connected to data holding node N75 and the other electrode thereof receives a reference potential VR. Common potential line 72 is applied with a common potential VC. Scan line 71 is driven by a vertical scan circuit (not shown) and data signal line 73 is driven by a horizontal scan circuit (not shown).

[0005] When scan line 71 is set to "H" level, N-type TFT 75 is made conductive to charge data holding node N75 to a level on data signal line 73 through N-type TFT 75. A light transmittance of liquid crystal cell 70 increases to the maximum when data holding node N75 is at "H" level, for example, while the light transmittance decreases to the minimum when data holding node N75 is at "L" level. Liquid crystal cells 70 are arranged in a plurality of rows and a plurality of columns to form one liquid crystal panel, on which one picture is displayed.

[0006] In such a liquid display, an electric charge of data holding node 75 gradually leaks to gradually decrease a potential thereof and to vary a light transmittance of liquid crystal cell 70 even when N-type TFT 75 is non-conductive. Therefore, as shown in FIG. 18, a data signal is refreshed, that is to say a data signal is rewritten to data holding node 75, at prescribed intervals.

[0007] In a conventional liquid crystal display, it was required that a plurality of scan lines 71 were selected one at a time and a data signal was rewritten to data holding nodes N75 corresponding to one selected scan line 71 while one selected scan line 71 was in a selected state, therefore, a problem has arisen that control for refreshing of a data signal becomes complex.

### DISCLOSURE OF THE INVENTION

[0008] Accordingly, it is a main object of the present invention to provide an image display capable of refreshing a data signal with ease.

[0009] An image display according to the present invention includes: a pixel display circuit displaying a pixel

density corresponding to a potential of a data holding node; a data write circuit applying one of first and second potentials to the data holding node in accordance with an image signal; and a refresh circuit performing refresh of a potential at the data holding node in response to a refresh signal when the potential at the data holding node exceeds a predetermined third potential between the first and second potentials while performing no refresh of the potential at the data holding node in response to the refresh signal when the potential at the data holding node does not exceed the third potential. Therefore, since a potential at the data holding node is refreshed by the refresh circuit when a refresh signal is supplied thereto, refresh of a data signal can be performed with ease.

[0010] Preferably, the refresh circuit includes a capacitor having one electrode receiving a potential at the data holding node, having the other electrode receiving the refresh signal, and a capacitance value of which varies according to a potential difference between the one electrode and the other electrode. In this case, a change in capacitance value of the capacitor according to a potential at the data holding node is used to make it possible to select whether or not refresh of the potential at the data holding node is performed.

[0011] Preferably, the capacitor includes an N-channel field effect transistor, having a gate electrode serving as the one electrode, and having at least one of first and second electrodes serving as the other electrode. In this case, a capacitance value of the capacitor increases when a positive voltage is applied between the one electrode and the other electrode of the capacitor.

[0012] Preferably, the capacitor includes a P-channel field effect transistor having a gate electrode serving as the other electrode, and having at least one of first and second electrodes serving as the one electrode. In this case, a capacitance value of the capacitor increases when a negative voltage is applied between the other electrode and the one electrode of the capacitor.

[0013] Preferably, the refresh circuit further includes: a first field effect transistor, connected between one electrode of the capacitor and the data holding node, and having a gate electrode receiving a first drive potential; and a second field effect transistor having a first electrode receiving a second drive potential, having a second electrode connected to the data holding node, and having a gate electrode connected to one electrode of the capacitor. In this case, the second field effect transistor is made conductive to refresh a potential at the data holding node when a potential at the one electrode of the capacitor exceeds a prescribed potential in response to a refresh signal, while the second field effect transistor does not made conductive to refresh no potential at the data holding node when a potential at the one electrode of the capacitor does not exceed a prescribed voltage in response to a refresh signal.

[0014] Preferably, the first drive potential is equal to a potential of the sum of the first potential and a threshold voltage of the first field effect transistor, and the second drive potential is equal to the first potential. An activation level of the refresh signal is equal to the first potential and a deactivation level thereof is equal to the second potential. In this case, a potential at the data holding node is refreshed to the first potential in response to transition of the second field effect transistor to a conductive state.

[0015] Preferably, the refresh circuit further includes a third field effect transistor, interposed between a node at the second drive potential and the first electrode of the second field effect transistor, having a gate electrode receiving the refresh signal. In this case, reduction is enabled in a leakage current from the node at the second drive potential to the data holding node.

[0016] Preferably, the first drive potential is equal to a potential of the sum of the first potential and the threshold voltage of the first field effect transistor, and the second drive potential is equal to the first potential. The activation level of the refresh signal is equal to a potential of the sum of the first potential and the threshold voltage of the third field effect transistor, and the deactivation thereof is equal to the second potential. In this case, a potential at the data holding node is refreshed to the first potential in response to transition of the second and third field effect transistors to a conductive state. Voltage drop in the third field effect transistor can be prevented from occurring.

[0017] Preferably, the second drive potential is applied only during a prescribed period including a period in which the refresh signal is set at the activation level. In this case, more reduction is enabled in leakage current from the node at the second drive potential to the data holding node.

[0018] Preferably, the refresh circuit further includes: a third field effect transistor, interposed between the node at the second drive potential and the first electrode of the second field effect transistor, having a gate electrode receiving a control signal in synchronism with the refresh signal. In this case, reduction is enabled in a leakage current from the node at the second drive potential to the data holding node.

[0019] Preferably, the first drive potential is equal to a potential of the sum of the first potential and the threshold voltage of the first field effect transistor, and the second drive potential is equal to the first potential. The activation level of the refresh signal is equal to the first potential and the deactivation level thereof is equal to a potential obtained by level shifting the second potential to the first potential side by a predetermined first voltage. The activation level of the control signal is equal to a potential of the sum of the first potential and a threshold voltage of the third field effect transistor, and the deactivation level thereof is equal to a potential obtained by level shifting the second potential to the side opposed to the first potential side by a predetermined second voltage. In this case, a potential at the data holding node is refreshed to the first potential in response to transition of the second and third field effect transistors to a conductive state. A change in potential at the data holding node can be suppressed to be small in the case where a potential at the data holding node is not refreshed.

[0020] Preferably, the second drive potential is applied only during a prescribed period including a period in which the refresh signal and the control signal are set at the activation levels. In this case, more reduction is enabled in leakage current from the node at the second drive potential to the data holding node.

[0021] Preferably, there is further provided a capacitor connected between the data holding node and a node at a reference potential. In this case, since a potential at the data holding node is maintained by the capacitor, a change becomes smaller in potential at the data holding node.

[0022] Preferably, the pixel display circuit includes a liquid crystal cell having one electrode connected to the data holding node, having the other electrode receiving a drive potential, and a light transmittance of which varies according to a potential at the data holding node. In this case, a pixel density varies according to a light transmittance of the liquid crystal cell.

[0023] Preferably, the pixel display circuit includes: a field effect transistor having a gate electrode connected to the data holding node, and having a first electrode receiving the reference potential; and a liquid crystal cell having one electrode connected to a second electrode of the field effect transistor, having the other electrode receiving a drive potential, and a light transmittance of which varies according to a conductive state/non-conductive state of the field effect transistor. In this case, the field effect transistor is brought into the conductive or non-conductive state according to whether or not a potential at the data holding node exceeds a threshold voltage of the field effect transistor to thereby cause a light transmittance of the liquid crystal cell to be the maximum or minimum.

[0024] Preferably, the pixel display circuit includes: a field effect transistor having a gate electrode connected to the data holding node, and having a first electrode receiving a first drive voltage; a switch circuit applying a second drive potential to a prescribed node in response to a reset signal, and connecting a second electrode of the field effect transistor to the prescribed node in response to a set signal; and a liquid crystal cell having one electrode connected to the prescribed node, having the other electrode receiving a reference potential, and a light transmittance of which varies according to a potential at the prescribed node. In this case, after a potential is written to the data holding node, a reset signal and a set signal are alternately inputted to thereby enable the prescribed node to take the first or second drive potential, which makes it possible to adjust a light transmittance of the liquid cell to the maximum or the minimum.

[0025] Preferably, the pixel display circuit includes: a field effect transistor having a gate electrode connected to the data holding node; and a light emitting element, connected in series with the field effect transistor between a node at a drive potential and a node at a reference potential, and a light intensity of which varies according to a current flowing in the field effect transistor. In this case, a pixel density varies according to a light intensity of the light emitting element.

[0026] Preferably, there are provided a plurality of pixel display circuits arranged in a plurality of rows and a plurality of columns, wherein the data write circuit includes: a plurality of scan lines provided correspondingly to the plurality of rows, respectively; a plurality of data signal lines provided correspondingly to the plurality of columns, respectively; field effect transistors, provided correspondingly to the respective pixel display circuits, each connected between the data holding node of a corresponding pixel display circuit and a corresponding data signal line, and each having a gate electrode connected to a corresponding scan line; a vertical scan circuit sequentially selecting the plurality of scan lines to drive a selected scan line to a select level and to cause a field effect transistor corresponding to the selected scan line to be made conductive; and a horizontal scan circuit sequentially selecting the plurality of data signal lines while one scan line is selected by the vertical scan



circuit to apply one of the first and second potentials onto a data line selected according to the image signal. In this case, an image in two dimensions can be displayed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0027] FIG. 1 is a circuit block diagram showing an overall configuration of a color liquid crystal display according to Embodiment 1 of the present invention.

[0028] FIG. 2 is a circuit diagram showing a configuration of a liquid crystal drive circuit provided correspondingly to each liquid crystal cell shown in FIG. 1.

[0029] FIG. 3 is a sectional view showing a construction of a capacitor 25 shown in FIG. 2.

[0030] FIG. 4 is a timing chart for describing an operation of the liquid crystal drive circuit shown in FIG. 2.

[0031] FIG. 5 is another timing chart for describing an operation of the liquid crystal drive circuit shown in FIG. 2.

[0032] FIG. 6 is a circuit diagram showing a modification example of Embodiment 1.

[0033] FIG. 7 is a sectional diagram showing a configuration of a capacitor 37 shown in FIG. 6.

[0034] FIG. 8 is a circuit diagram showing a main part of a color liquid crystal display according to Embodiment 2 of the present invention.

[0035] FIG. 9 is a timing chart for describing an operation of the liquid crystal drive circuit shown in FIG. 8.

[0036] FIG. 10 is a circuit diagram showing a modification example of Embodiment 2.

[0037] FIG. 11 is a timing chart for describing an operation of a liquid crystal drive circuit shown in FIG. 10.

[0038] FIG. 12 is a circuit diagram showing another modification example of Embodiment 2.

[0039] FIG. 13 is a timing chart for describing an operation of a liquid crystal drive circuit shown in FIG. 12.

[0040] FIG. 14 is a circuit diagram showing a main part of a color liquid crystal display according to Embodiment 3 of the present invention.

[0041] FIG. 15 is a circuit diagram showing a main part of a color liquid crystal display according to Embodiment 4 of the present invention.

[0042] FIG. 16 is a circuit diagram showing a main part of an image display according to Embodiment 5 of the present invention.

[0043] FIG. 17 is a circuit diagram showing a main part of a conventional liquid crystal display.

[0044] FIG. 18 is a timing chart for describing a problem in the conventional liquid crystal display.

#### BEST MODE FOR CARRYING OUT THE INVENTION

##### EMBODIMENT 1

[0045] FIG. 1 is a circuit block diagram showing an overall configuration of a color liquid crystal display according to Embodiment 1 of the present invention. In FIG. 1,

color liquid crystal display 1 includes a liquid crystal panel 2, a vertical scan circuit 8 and a horizontal scan circuit 11, and is driven by a power supply potential VDD and a ground voltage VSS applied externally.

[0046] Liquid crystal panel 2 includes: a plurality of liquid crystal cells 3 arranged in a plurality of rows and a plurality of columns; scan lines 5 and common potential lines 6 provided correspondingly to respective rows; and data signal lines 7 provided correspondingly to respective columns.

[0047] Liquid crystal cells 3 are grouped into sets of three cells in each row in advance. The three liquid crystal cells 2 of each set are provided with color filters for R, G and B, respectively. The three liquid crystal cells 3 of each set constitute one pixel 4.

[0048] A common potential VC is externally applied onto common potential lines 6. A refresh signal REF and drive potentials V1, V2 and V3 are externally applied to liquid crystal panel 2.

[0049] Vertical scan circuit 8 includes a shift register circuit 9 and a buffer circuit 10. Shift register circuit 9 generates a signal for sequentially selecting a plurality of scan lines 5 of liquid crystal panel 2 in synchronism with a horizontal and vertical synchronous signal SN1 supplied externally. Buffer circuit 10 buffers an output signal of shift register circuit 9 to supply the resulting signal to selected scan line 5. Therefore, the plurality of scan lines 5 of liquid crystal panel 2 are sequentially driven to "H" level at select level for a prescribed time on each scan line 5. When scan line 5 is driven to "H" level at select level, pixels 4 corresponding to scan line 5 are activated.

[0050] Horizontal scan circuit 11 includes a shift register circuit 12, a buffer circuit 14 and a plurality of switches 14. The plurality of switches 14 are provided correspondingly to a plurality of data signal lines 7, respectively, and are grouped into sets of three switches corresponding to respective sets of liquid crystal cells 2 in advance. One electrodes of three switches of each set receive data signals DR, DG and DB for R, G and B, respectively, and the other electrodes thereof are connected to corresponding three data signal lines 7, respectively. Shift register circuit 12 generates a signal sequentially selecting a plurality of switch sets in synchronism with horizontal synchronous signal SN2 supplied externally for a prescribed time to each switch set. Buffer circuit 10 buffers an output signal of shift register circuit 12 to supply the resulting signal to the control terminals of switches 14 of a selected set and to cause switches 14 to be made conductive. Therefore, data signals DR, DG and DB are sequentially supplied to the plurality of pixels 4 in a selected row.

[0051] When all pixels 4 of liquid crystal panel 2 are scanned by vertical scan circuit 8 and horizontal scan circuit 11, one image is displayed on liquid crystal panel 2.

[0052] FIG. 2 is a circuit diagram showing a configuration of a liquid crystal drive circuit 20 provided correspondingly to each liquid crystal cell 3. In FIG. 2, liquid crystal drive circuit 20 includes enhanced N-type TFTs 21 to 24 and capacitors 25 and 26, and not only is connected to corresponding liquid crystal cell 3, scan line 5, common potential line 6 and signal line 7, but also receives refresh signal REF and drive potentials V1 and V2. In FIG. 2, there is shown liquid crystal drive circuit 20 corresponding to R of R, G and B.

[0053] N-type TFT 21 is connected between corresponding data signal line 7 and data holding node N21, and the gate thereof is connected to corresponding scan line 5. Capacitor 26 is connected between data holding node N21 and common potential line 6. N-type TFT 24 is connected between one electrode of corresponding liquid crystal cell 3 and common potential line 6, and the gate thereof is connected to data holding node N21. The other electrode of liquid crystal cell 3 receives a drive voltage V3.

[0054] When scan line 5 is driven to "H" level at select level, N-type TFT 21 is made conductive, and data holding node N21 is charged at a potential on data signal line 7. When scan line 5 is driven to "L" level at non-select level, N-type TFT 21 is made non-conductive, and a potential at data holding node N21 is held by capacitor 26.

[0055] When data holding node N21 is at "H" level, N-type TFT 24 is made conductive, a drive voltage V3-VC is applied between electrodes of liquid crystal cell 3, and a light transmittance of liquid crystal cell 3 is maximized, for example. When data holding node N21 is at "L" level, N-type TFT 24 is made non-conductive, no drive voltage is applied between electrodes of liquid crystal cell 3, and a light transmittance of liquid crystal cell 3 is minimized, for example.

[0056] Since a potential at data holding node N21 gradually falls by gradual leakage of an electric charge of data holding node N21, a necessity arises for refreshing (rewriting) of a data signal at prescribed time intervals. N-type TFTs 22 and 23 and capacitor 25 constitute a refresh circuit.

[0057] N-type TFT 22 is connected between a node N22 and data holding node N21, and the gate thereof receives drive potential V2. Drive potential V2 is set to a potential  $VH+VTN$  obtained by adding a threshold voltage VTN of N-type TFT to "H" level VH of data signal DR. Therefore, no voltage drop occurs due to threshold voltage VTN of N-type TFT 22 to cause potentials at nodes N21 and N22 to be equal to each other.

[0058] The drain of N-type TFT 23 receives drive potential V1, the source thereof is connected to data holding node N21, and the gate thereof is connected to node N22. Drive voltage V1 is set to a prescribed potential equal to or higher than "H" level VH of data signal DR. It is herein assumed that  $V1=VH$ . When potentials at nodes N21 and N22 are equal to each other, N-type TFT 23 is non-conductive. When a potential at node N22 rises to  $VH+VTN$  or higher, N-type TFT 23 is made conductive to cause data holding node N21 to be at  $V1=VH$ .

[0059] Capacitor 25 is a capacitor of an N-type TFT (of an enhancement type) structure, the gate thereof is connected to node N22, and the source thereof receives refresh signal REF. When a gate to source voltage of capacitor 25 is higher than threshold voltage VTN of N-type TFT, capacitor 25 has a prescribed capacitance value. When a gate to source voltage of capacitor 25 is lower than threshold voltage VTN of N-type TFT, capacitor 25 has a considerably small capacitance value only corresponding to a parasitic capacitance.

[0060] FIG. 3 is a sectional view showing a configuration of capacitor 25. In FIG. 3, an intrinsic polysilicon film 31 is formed in a prescribed region on a surface of a glass substrate 30. Then, a gate insulating film 32 is formed so as

to cover part of intrinsic polysilicon film 31 and, further, a gate electrode 33 is laminated on gate insulating film 32. N-type impurity is injected into portion which is not covered by gate insulating film 32 and gate electrode 32 on intrinsic polysilicon film 31 to form a source region 31s. Then, an interlayer insulating film 34 is formed so as to cover all the region, a contact hole CH1 is opened from a surface of interlayer insulating film 34 to a surface of gate electrode 33, and a contact hole CH2 is opened from the surface of interlayer insulating film 34 to a surface of source region 31s. Then, aluminum electrodes 35 and 36 are formed so as to fill and cover contact holes CH1 and CH2. Aluminum electrode 35 (gate) is connected to node N22, and aluminum electrode (source) 36 receives refresh signal REF.

[0061] When a voltage higher than threshold voltage VTN of N-type TFT is applied between the gate and source, an N-type channel layer is formed on a surface of intrinsic polysilicon film 31 below gate electrode 33 to generate prescribed capacitance value between the gate and source.

[0062] When a voltage lower than threshold voltage VTN of N-type TFT is applied between the gate and source, no N-type channel layer is formed on the surface of intrinsic polysilicon film 31; therefore, a capacitance value between the gate and source is a considerably small value only corresponding to a parasitic capacitance.

[0063] Note that a configuration may be adopted in which not only is a gate electrode formed in the central portion on the surface of the intrinsic polysilicon film with a gate insulating film interposed therebetween in a similar way to the case of an ordinary TFT, but impurity is also injected at both sides of the gate electrode to form a source region and a drain region and, in addition, not only is the gate electrode connected to one aluminum electrode, but the source region and the drain region are connected commonly to the other aluminum electrode to form a capacitor.

[0064] FIG. 4 is a timing chart for describing an operation of liquid crystal drive circuit 20 in the case where data signal DR is at "H" level VH. In FIG. 4, in an initial state, potential V5 on scan line 5 is set to "L" level, data signal DR is set to "L" level VL, nodes N21 and N22 are reset to "L" level VL, and refresh signal REF is set to "L" level.

[0065] At time t0, data signal DR is raised from "L" level VL to "H" level VH and, then, at time t1, potential V5 on scan line 5 is raised from "L" level to "H" level. Thereby, N-type TFT 21 is made conductive to raise nodes N21 and N22 from "L" level VL to "H" level VH. When a prescribed time elapses thereafter, potential V5 on scan line 5 is lowered to "L" level and, then, data signal DR is also lowered to "L" level. When potential V5 on scan line 5 is raised to "L" level, N-type TFT 21 is made non-conductive to cause potentials at nodes N21 and N22 to be held by capacitor 26. Since potential VH at data holding node N22 is higher than threshold potential VTN of N-type TFT 24, N-type TFT 24 is made conductive to apply drive voltage V3-VC between electrodes of liquid crystal cell 3 and to, for example, maximize a light transmittance of liquid crystal cell 3.

[0066] When liquid crystal cell is left in this state, potentials at nodes N21 and N22 are gradually lowered by leakage current. When a potential at node N21 is lowered to a value lower than threshold potential VTN of N-type TFT 24,

N-type TFT is made non-conductive to vary a light transmittance of liquid crystal cell 3 from the maximum to the minimum. Therefore, refresh of a data signal is performed at prescribed time  $t_2$  before potentials at nodes N21 and N22 are lowered to a value lower than threshold potential VTN of N-type TFT 24.

[0067] Since, at time  $t_2$ , potentials at nodes N21 and N22 are higher than threshold potential VTN of N-type TFT, an N-type channel layer is generated in intrinsic polysilicon film 31 of capacitor 25, and capacitor 25 has a prescribed capacitance value. At time  $t_2$ , when refresh signal REF is raised from "L" level VL to "H" level VH, a potential at node N22 is raised to a boosted potential VP ( $\geq VH + VTN$ ) by capacitive coupling to cause N-type TFT 23 to be made conductive and to raise node N21 to drive potential  $V_1 = VH$ . Thereby, potential VH at data holding node N21 has been refreshed. At time  $t_3$ , when refresh signal REF is lowered from "H" level VH to "L" level VL, potentials at nodes N21 and N22 are lowered by capacitive coupling, but since a capacitance value of capacitor 26 is sufficiently larger than a capacitance value of capacitor 25, potentials at nodes N21 and N22 are maintained at "H" level VH.

[0068] FIG. 5 is a timing chart for showing an operation of liquid crystal drive circuit 20 in the case where data signal DR is at "L" level VL. In FIG. 5, data signal DR is fixed at "L" level VL. Therefore, at time  $t_1$ , potential V5 on scan line 5 is raised to "H" level and kept there for a prescribed time and even if N-type TFT 21 is in a conductive state only for a prescribed time, nodes N21 and N22 are maintained as is at "L" level VL.

[0069] At time  $t_2$ , when a prescribed time is elapsed from time  $t_1$ , since potentials at nodes N21 and N22 are lower than threshold potential VTN of N-type TFT, no N-type channel layer is generated in intrinsic polysilicon film 31 of capacitor 25, and a capacitance value of capacitor 25 has a considerably small value only corresponding to a parasitic capacitance. Therefore, even if, at time  $t_2$ , refresh signal REF is raised from "L" level VL to "H" level VH, nodes N21 and N22 are maintained almost at "L" level VL. Therefore, in this case, a potential at data holding node N21 is not refreshed. At time  $t_3$ , even when refresh signal REF is lowered from "H" level VH to "L" level VL, nodes N21 and N22 are maintained at "L" level VL since a capacitance value of capacitor 25 is small.

[0070] In Embodiment 1, since no necessity arises for driving scan line 5 and data signal line 7 at the time of refreshing a data signal, a refresh control can be implemented with ease. Furthermore, since no necessity arises for operating vertical scan circuit 8 and horizontal scan circuit 11 at the time of refreshing a data signal, power consumption can be reduced.

[0071] In a modification example of FIG. 6, capacitor 25 having an N-type TFT structure is replaced with a capacitor 37 having a P-type TFT (of an enhancement type) structure. Capacitor 37 is, as shown in FIG. 7, of a structure in which N-type source region 31s of capacitor 25 is replaced with a P-type source region 31s'. The gate of capacitor 37 receives refresh signal REF and the source thereof is connected to node N22. In this modification example as well, there is obtained the same effect as in Embodiment 1.

## EMBODIMENT 2

[0072] In Embodiment 1, description has been given that when nodes N21 and N22 are at "L" level VL, N-type TFT is made non-conductive. However, a case arises where a considerably small current (an off current) flows in N-type TFT 23 even at a gate to source voltage of 0 V due to a fluctuation in characteristics of N-type TFT 23. In this case, potentials at nodes N21 and N22 have even a chance to be gradually raised due to a considerably small current and to eventually cause potentials at nodes N21 and N22 to exceed threshold voltage VTN of N-type TFT 24. In Embodiment 2, it is aimed to solve this problem.

[0073] FIG. 8 is a circuit diagram showing a configuration of a liquid crystal drive circuit 40 of a color liquid crystal display according to Embodiment 2 of the present invention, and the figure is to be compared with FIG. 2. Referring to FIG. 8, liquid crystal drive circuit 40 is different from liquid crystal drive circuit 20 of FIG. 2 in that N-type TFT 41 is added and that a refresh signal REF' is supplied instead of refresh signal REF. The drain of N-type TFT 41 receives drive potential V1, the source thereof is connected to the drain (a node N23) of N-type TFT 23, and the gate thereof receives refresh signal REF'. Refresh signal REF' is different from refresh signal REF in that "H" level of refresh signal REF', as shown in FIG. 9, is not VH, but a prescribed potential VH' equal to or higher than  $VH + VTN$ .

[0074] In FIG. 8, when refresh signal REF' is set to "L" level VL (0 V) in the case where nodes N21 and N22 are at "L" level, a considerably small off current flows in N-type TFTs 23 and 41 to gradually raise potentials at nodes N21 and N23. When a potential at node N23 is raised, however, a gate to source voltage of N-type TFT 41 takes a negative voltage; therefore, no off current flows in N-type TFT 41 to cease a rise in potentials at nodes N21 and N23.

[0075] When refresh signal REF' is set to "H" level VH', N-type TFT 41 is made conductive. At this time, since "H" level VH' of refresh signal REF' is set to  $VH + VTN$  or higher, no voltage drop occurs due to threshold voltage VTN of N-type TFT 41.

[0076] Note that needless to say that capacitor 25 of an N-type TFT structure is replaced with capacitor 37 of a P-type TFT structure shown in FIGS. 6 and 7.

[0077] When refresh signal REF' is raised from "L" level to "H" level in the case where data holding node N21 is at "L" level, potentials at nodes N21 and N22 are somewhat raised due to a considerably small capacitance value of capacitor 25. In order to cause a rise, at this time, in potentials at nodes N21 and N22 to be smaller, a necessity arises for minimize a capacitance value of capacitor 25 under conditions where an N-type channel layer is hard to be generated in intrinsic polysilicon film 31 of capacitor 25. Therefore, a configuration may be adopted in which "L" level of refresh signal REF' is set not to VL (0 V) but to a positive potential VL' (for example 1 V) to thereby maintain a gate to source voltage of capacitor 25 at a negative voltage.

[0078] In a modification example of FIG. 10, refresh signal REF1 is supplied to the drain of N-type TFT 41 of liquid crystal drive circuit 40 instead of drive potential V1. As shown in FIG. 11, refresh signal REF1 is kept at "H" level VH only during a period (from time  $t_2$  to time  $t_3$ ) when refresh signal REF' is at "H" level VH and prescribed

periods before and after the period (from time t2 to time t3) while being kept at "L" level VL during the other periods. Therefore, a leakage current flowing in N-type TFTs 23 and 41 can be smaller. Note that in this modification example as well, needless to say that capacitor 25 of an N-type TFT structure may be replaced with capacitor 37 of a P-type TFT structure shown in FIGS. 6 and 7.

[0079] In a modification example of FIG. 12, the gate of N-type TFT 41 and the source of capacitor 25 of liquid crystal drive circuit 40 are disconnected, refresh signal REF<sup>1</sup> is supplied to the source of capacitor 25, refresh signal REF2 is supplied to the gate of N-type TFT 41, and refresh signal REF1 is supplied to the drain of N-type TFT 41. As shown in FIG. 13, "L" level of signal REF<sup>1</sup> is not VL=0 V, but a positive potential VL'=VL+ΔV1 and "H" level of signal REF<sup>1</sup> is VH. For example, ΔV1 is 1 V. Under such a condition, a capacitance value of capacitor 25 in the case where nodes N21 and N22 are at "L" level can be smaller. Furthermore, "L" level of signal REF2 is not VL=0 V, but a negative potential VL'=VL-ΔV2 and "H" level of signal REF2 is VH'. For example, ΔV2 is 1 V. Under such a condition, a leakage current in N-type TFT 41 in the case where signal REF2 is at "L" level VL' can be smaller.

#### EMBODIMENT 3

[0080] FIG. 14 is a circuit diagram showing a main part of a color liquid crystal display according to Embodiment 3 of the present invention, and the figure is to be compared with FIG. 2.

[0081] In FIG. 14, the color liquid crystal display is different from color liquid crystal display 1 of Embodiment 1 in that liquid crystal drive circuit 20 is replaced with a liquid crystal drive circuit 50, that a set line 54 and a reset line 55 are added, and that a drive potential VC' and a reference potential VLC are newly introduced. Set line 54 and reset line 55 are driven, for example, by a vertical scan circuit.

[0082] Liquid crystal drive circuit 50 is constituted of liquid crystal drive circuit added with N-type TFTs 51 and 52 and a capacitor 53. Capacitor 26 is connected between node N21 and node N24. Node N24 receives drive potential VC=VL supplied externally. A potential at data holding node N21 is maintained by capacitor 26.

[0083] N-type TFTs 24 and 51 are in series connected between node N24 and a node 51. The gate of N-type TFT 24 is connected to data holding node N21. The gate of N-type TFT 51 receives a set signal ST through set line 54.

[0084] When set signal ST is at "L" level at non-select level, N-type TFT 51 is made non-conductive. When set signal ST is set to "H" level at select level, N-type TFT 51 is made conductive. When data holding node N21 is at "L" level, N-type TFT 24 is made non-conductive and node 51 does not vary as is at drive potential V3. When data holding node N21 is at "H" level, N-type TFT 24 is made conductive to set node N51 to drive potential VC'.

[0085] The drain of N-type TFT 52 receives drive potential V3=VH, the source thereof is connected to node N51, the gate thereof receives reset signal RST through reset line 55. Capacitor 53 is connected between node N51 and common potential line 6.

[0086] When reset signal RST is at "L" level at non-select level, N-type TFT 52 is made non-conductive and a potential at node N51 is maintained as it is. When reset signal RST is set to "H" level at select level, N-type TFT 52 is made conductive and node N51 is reset to drive potential V3.

[0087] One electrode of liquid crystal cell 3 is connected to node N51 and the other electrode thereof receives reference potentials VLC=VL. When node N51 is reset to drive potential V3, a light transmittance of liquid crystal cell 3 takes, for example, the maximum value, while when node N51 is set to drive voltage VC', a light transmittance of liquid crystal cell 3 takes, for example, the minimum value.

[0088] Then, description will be given of an operation of the color liquid crystal display. In a data write period, scan line 5 is set to "H" level at select level to cause N-type TFT 21 to be made conductive and to write a potential on data signal line 7 to data holding node N21. When scan line 5 is set to "L" level at non-select level, N-type TFT 21 is made non-conductive to thereby, cause a potential at data holding node N21 to be maintained by capacitor 26.

[0089] In a data holding period, reset signal RST and set signal ST are sequentially set to "H" level for a prescribed time T2 at intervals of a prescribed time T1 (T2<T1). In such an operation, when data holding node N21 is at "H" level, node 51 is set to drive potential VC' while when data holding node N21 is at "L" level, node N51 is reset to drive potential V3.

[0090] Since a potential at data holding node N21 is gradually varied by a leakage current, a necessity arises for performing refresh of data at intervals of prescribed time T3 (T3>T1) in a data holding period. The refresh of a data signal is performed with N-type TFTs 22 and 23, and capacitor 25. Since a refresh method for a data signal is the same as in Embodiment 1, no description thereof will be repeated.

[0091] In Embodiment 3 as well, there can be obtained the same effect as in Embodiment 1.

#### EMBODIMENT 4

[0092] FIG. 15 is a circuit diagram showing a liquid crystal drive circuit 60 of a color liquid crystal display according to Embodiment 4 of the present invention, and the figure is to be compared with FIG. 2.

[0093] Referring to FIG. 15, liquid crystal drive circuit 60 is different from liquid crystal drive circuit 20 of FIG. 2 in that N-type TFT 24 is deleted. One electrode of liquid crystal cell 3 is connected directly to data holding node N21.

[0094] When data holding node N21 is at "H" level VH, a voltage between electrodes of liquid crystal cell 3 is at 0 V and a light transmittance of liquid crystal cell 3 takes, for example, the minimum value. When data holding node N21 is at "L" level, a voltage between electrodes of liquid crystal cell 3 is at VH and a light transmittance of liquid crystal cell 3 takes, for example, the maximum value. The potential of data holding node N21 is refreshed using N-type TFTs 22 and 23 and capacitor 25.

[0095] In Embodiment 4 as well, there can be obtained the same effect as in Embodiment 1.

## EMBODIMENT 5

[0096] FIG. 16 is a circuit diagram showing a main part of an image display according to Embodiment 5 of the present invention, and the figure is to be compared with FIG. 2.

[0097] Referring to FIG. 16, the image display is different from color liquid crystal display 1 of Embodiment 1 in that liquid crystal 3 is replaced with an organic EL (electroluminescence) element 61. Organic EL element 61 is connected between a node at power supply potential VDD and the drain of N-type TFT 24 of drive circuit 20.

[0098] When data holding node N21 is at "H" level, N-type TFT 24 is made conductive to cause a current to flow in organic EL element 61 and to cause organic EL element 61 to emit light. When data holding node N21 is at "L" level, N-type TFT 24 is made non-conductive to cause no current to flow in organic EL element 61 and to cause organic EL element 61 to emit no light. A potential at data holding node N21 is refreshed using N-type TFTs 22 and 23, and capacitor 25.

[0099] In Embodiment 5 as well, there can be obtained the same effect as in Embodiment 1.

[0100] Note that the same effect can be obtained in the case where organic EL element 61 is interposed between the source of N-type TFT 24 and common potential line 6, and power supply potential VDD is supplied to the drain of N-type TFT 24.

[0101] Furthermore, a display element of another kind may be used instead of organic EL element 61.

[0102] Needless to say that the embodiments and modification examples described above may be properly combined.

[0103] The embodiments disclosed this time should be considered to be presented by way of illustration and are not to be taken by way of limitation in all aspects. It is intended that the spirit and scope of the present invention are shown not by the above description but by the appended claims and include all modification or alterations within the scope of the appended claims and the scope equivalent thereto.

1. An image display comprising:

a pixel display circuit (3, 24, 51, 52, 61) displaying a pixel density corresponding to a potential of a data holding node (N21);

a data write circuit (5, 7, 8, 11, 21) applying one of first and second potentials (VH, VL) to said data holding node (N21) in accordance with an image signal (DR, DG, DB, SN1, SN2); and

a refresh circuit (22, 23, 25, 37, 41) performing refresh of a potential at said data holding node (N21) in response to a refresh signal (REF, REF', REF'') when the potential at said data holding node (N21) exceeds a predetermined third potential (VTN) between said first and second potentials (VH, VL) while performing no refresh of said potential at said data holding node (N21) in response to said refresh signal (REF, REF', REF'') when the potential at said data holding node (N21) does not exceed the third potential (VTN).

2. The image display according to claim 1, wherein

said refresh circuit (22, 23, 25, 37, 41) includes a capacitor (25, 37) having one electrode receiving the potential at said data holding node (N21), having the other electrode receiving said refresh signal (REF, REF', REF''), and a capacitance value of which varies according to a potential difference between said one electrode and the other electrode.

3. The image display according to claim 2, wherein

said capacitor (25, 37) includes an N-channel field effect transistor (25), having a gate electrode serving as said one electrode, and having at least one of first and second electrodes serving as said the other electrode.

4. The image display according to claim 2, wherein

said capacitor includes a P-channel field effect transistor (37) having a gate electrode serving as said the other electrode, and having at least one of first and second electrodes serving as said one electrode.

5. The image display according to claim 2, wherein

said refresh circuit (22, 23, 25, 37, 41) further includes:

a first field effect transistor (22), connected between one electrode of said capacitor (25, 37) and said data holding node (N21), and having a gate electrode receiving a first drive potential (V2); and

a second field effect transistor (23) having a first electrode receiving a second drive potential (V1), having a second electrode connected to said data holding node (N21), and having a gate electrode connected to one electrode of said capacitor (25, 37).

6. The image display according to claim 5, wherein

said first drive potential (V2) is equal to a potential (VH+VTN) of the sum of said first potential (VH) and a threshold voltage (VTN) of said first field effect transistor,

said second drive potential (V1) is equal to said first potential (VH), and

an activation level of said refresh signal (REF) is equal to said first potential (VH) and a deactivation level thereof is equal to said second potential (VL).

7. The image display according to claim 5, wherein

said refresh circuit (22, 23, 25, 37, 41) further includes: a third field effect transistor (41), interposed between a node at said second drive potential (V1) and the first electrode of said second field effect transistor (23), having a gate electrode receiving said refresh signal (REF').

8. The image display according to claim 7, wherein

said first drive potential (V2) is equal to a potential (VH+VTN) of the sum of said first potential (VH) and the threshold voltage (VTN) of said first field effect transistor (22),

said second drive potential (V1) is equal to said first potential (VH), and

an activation level of said refresh signal (REF') is equal to a potential (VH+VTN) of the sum of said first potential (VH) and the threshold voltage (VTN) of said third field effect transistor (41), and a deactivation level thereof is equal to said second potential (VL).

9. The image display according to claim 8, wherein said second drive potential (V1) is applied only during a prescribed period including a period (t2 to t3) in which said refresh signal (REF') is set at said activation level.
10. The image display according to claim 5, wherein said refresh circuit (22, 23, 25, 37, 41) further includes: a third field effect transistor (41), interposed between the node at said second drive potential (V1) and the first electrode of said second field effect transistor (23), having a gate electrode receiving a control signal (REF2) in synchronism with said refresh signal (REF').
11. The image display according to claim 10, wherein said first drive potential (V2) is equal to a potential (VH+VTN) of the sum of said first potential (VH) and the threshold voltage (VTN) of said first field effect transistor (22),
- said second drive potential (V1) is equal to said first potential (VH),
- an activation level of said refresh signal (REF") is equal to said first potential (VH) and a deactivation level thereof is equal to a potential (VL+ΔV1) obtained by level shifting said second potential (VL) to said first potential (VH) side by a predetermined first voltage (ΔV1), and
- an activation level of said control signal (REF2) is equal to a potential (VH+VTN) of the sum of said first potential (VH) and a threshold voltage (VTN) of said third field effect transistor (41), and a deactivation level thereof is equal to a potential (VL-ΔV2) obtained by level shifting said second potential (VL) to the side opposed to said first potential (VH) side by a predetermined second voltage (ΔV2).
12. The image display according to claim 11, wherein said second drive potential (V1) is applied only during a prescribed period including a period (t2 to t3) in which said refresh signal (REF") and said control signal (REF2) are set at the activation levels.
13. The image display according to claim 1, further comprising:
- a capacitor (26) connected between said data holding node (N21) and a node (6) at a reference potential (VC).
14. The image display according to claim 1, wherein said pixel display circuit (3, 24, 51, 52, 61) includes a liquid crystal cell (3) having one electrode connected to said data holding node (N21), having the other electrode receiving a drive potential (V3), and a light transmittance of which varies according to a potential at said data holding node (N21).
15. The image display according to claim 1, wherein said pixel display circuit (3, 24, 51, 52, 61) includes:
- a field effect transistor (24) having a gate electrode connected to said data holding node (N21), and having a first electrode receiving the reference potential (VC); and
  - a liquid crystal cell (3) having one electrode connected to a second electrode of said field effect transistor (24), having the other electrode receiving a drive potential (V3), and a light transmittance of which varies according to a conductive state/non-conductive state of said field effect transistor (24).
16. The image display according to claim 1, wherein said pixel display circuit (3, 24, 51, 52, 61) includes:
- a field effect transistor (24) having a gate electrode connected to said data holding node (N21), and having a first electrode receiving a first drive voltage (VC');
  - a switch circuit (51, 52) applying a second drive potential (V3) to a prescribed node (N51) in response to a reset signal (RST), and connecting a second electrode of said field effect transistor (24) to said prescribed node (N51) in response to a set signal (ST); and
  - a liquid crystal cell (3) having one electrode connected to said prescribed node (N51), having the other electrode receiving a reference potential (VLC), and a light transmittance of which varies according to a potential at said prescribed node (N51).
17. The image display according to claim 1, wherein said pixel display circuit (3, 24, 51, 52, 61) includes:
- a field effect transistor (24) having a gate electrode connected to said data holding node (N21); and
  - a light emitting element (61), connected in series with said field effect transistor (24) between a node at a drive potential (VDD) and a node at a reference potential (VC), and a light intensity of which varies according to a current flowing in said field effect transistor (24).
18. The image display according to claim 1, comprising:
- a plurality of pixel display circuits (3, 24, 51, 52, 61) arranged in a plurality of rows and a plurality of columns, wherein
- said data write circuit includes:
- a plurality of scan lines (5) provided correspondingly to said plurality of rows, respectively;
  - a plurality of data signal lines (7) provided correspondingly to said plurality of columns, respectively;
  - field effect transistors (21), provided correspondingly to the respective pixel display circuits (3, 24, 51, 52, 61), each connected between the data holding node (N21) of a corresponding pixel display circuit (3, 24, 51, 52, 61) and a corresponding data signal line (7), and each having a gate electrode connected to a corresponding scan line (5);
  - a vertical scan circuit (8) sequentially selecting said plurality of scan lines (5) to drive a selected scan line (5) to a select level and to cause a field effect transistor (21) corresponding to said selected scan line (5) to be made conductive; and
  - a horizontal scan circuit (11) sequentially selecting said plurality of data signal lines (7) while one scan line (5) is selected by said vertical scan circuit (8) to apply one of said first and second potentials (VH, VL) onto a data line (7) selected according to said image signal (DR, DG, DB, SN1, SN2).

|                |                                                                                                                                             |         |            |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------|---------|------------|
| 专利名称(译)        | 图像显示单元                                                                                                                                      |         |            |
| 公开(公告)号        | <a href="#">US20040066360A1</a>                                                                                                             | 公开(公告)日 | 2004-04-08 |
| 申请号            | US10/450148                                                                                                                                 | 申请日     | 2002-02-06 |
| [标]申请(专利权)人(译) | 飞田YOUICHI                                                                                                                                   |         |            |
| 申请(专利权)人(译)    | 飞田YOUICHI                                                                                                                                   |         |            |
| 当前申请(专利权)人(译)  | 三菱电机株式会社                                                                                                                                    |         |            |
| [标]发明人         | TOBITA YOUICHI                                                                                                                              |         |            |
| 发明人            | TOBITA, YOUICHI                                                                                                                             |         |            |
| IPC分类号         | G02F1/133 G09G3/20 G09G3/32 G09G3/36 H05B33/08                                                                                              |         |            |
| CPC分类号         | G09G3/2011 G09G3/3258 G09G3/3618 G09G3/3648 G09G2300/0417 G09G2320/02 G09G2300/0842 G09G2300/0852 G09G2300/0861 G09G2300/0866 G09G2300/0426 |         |            |
| 其他公开文献         | US7145543                                                                                                                                   |         |            |
| 外部链接           | <a href="#">Espacenet</a> <a href="#">USPTO</a>                                                                                             |         |            |

#### 摘要(译)

该彩色图像显示器 ( 1 ) 包括：液晶单元 ( 3 )，其透光率根据数据保持节点 ( N21 ) 的电位而变化;扫描电路 ( 5,7,8,11 ) 根据图像信号 ( DR，DG，DB，SN1，SN2 ) 将第一和第二电位 ( VH，VL ) 之一施加到数据保持节点 ( N21 ) ;当数据保持节点 ( N21 ) 的电位超过a时，刷新电路 ( 22,23,25 ) 响应刷新信号 ( REF )，将数据保持节点 ( N21 ) 的电位刷新为第一电位。当数据保持节点 ( N21 ) 处的电位不超过阈值电位 ( VTN ) 时，N型TFT的阈值电位 ( VTN )，而不执行数据保持节点 ( N21 ) 处的电位的刷新。

